SOLUTIONS

Module:	Digital Circuit Design		
Module Code	EBU4202	Paper	A
Time allowed	2hrs	Filename	Solutions_1617_EBU4202_A
Rubric	ANSWER ALL FOUR QUESTIONS		
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Question 1

a) Fill in the table by putting the correct numbers in different bases by doing suitable conversion. Write your answers in the table directly.
Show **THREE** places in any fractional part.

Decimal	Binary	Octal	Hexadecimal
			221.A60
		123.300	

[12 marks]

Answers:
[2] each correct answer in red.
[-0.5] if either integer or fractional part is wrong.

Decimal	Binary	Octal	Hexadecimal
545.648	1000100001.101	1041.514	221.A60
83.375	1010011.011	123.300	53.600

b) Figure Q1b) shows a particular floating point format.

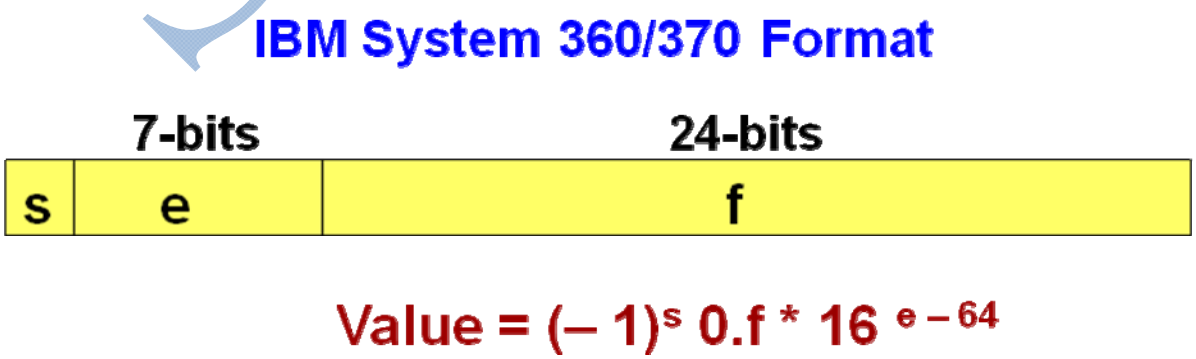


Figure Q1b)

Express the decimal number 0.04 in this format to 8 fractional places. [5 marks]

Answer:
Convert 0.04_{10} to binary:
0.04x2=0.08 MSB
0.08x2=0.16
0.16x2=0.32
0.32x2=0.64
0.64x2=1.28
0.28x2=0.56
0.56x2=1.12
0.12x2=0.24 [2 marks]
So $0.04_{10}=0.00001010_2$ to 8 fractional places
$=1.010_2 \times 2^{-5}$
$=1.01 \times 2^{(59-64)}$
$1.01 \times 2^{(111011-64)}$ [2 marks]
Therefore floating point format is: 0 /0111011 /01000000000000000000000 [1 mark]

c) Convert the decimal numbers 173 and 97 to 8 bit binary and then obtain the value of $(173_{10}-97_{10})$ using 2^s complement arithmetic. State the answer in HEX. [6 marks]

Answer:
$173_{10}=10101101_2$ [1 mark]
$97_{10}=01100001_2$ [1 mark]
2^s complement of 01100001=10011110+1=10011111 [1 mark]
10101101+1001111=101001100 [1 mark]
Leading 1 is an overflow bit [1 mark]
Therefore answer is $01001100=76_{10}=4C_H$ [1 mark]

d) A particular data transmission system uses single bit even parity.
Can an error be detected if the data sent = 01010011 and the data received = 01010010? [2 marks]
Answer:
Received value has odd number of 1's (so doesn't obey even parity) [1 mark] so error is detected (1 bit flipped) [1 mark]

Question 2

a) State and briefly explain THREE advantages of digital electronics as compared with analogue electronics.

[6 marks]

Answer:

Three from:
Noise immunity: The output from analogue circuits are subject to noise and component parameter variations, but digital devices have built-in noise immunity
Flexibility/programmability: digital circuits can be more readily modified/reprogrammed to perform different functions
Speed: digital circuits can operate more quickly than analogue circuits
Economy: Mass production of complex functions is possible, allowing complex functionality in small physical space
[6 marks:1 for each heading, 1 for each explanation. Any other valid advantage will gain the relevant marks]

b) Two technologies used in the manufacture of logic gates are TTL and CMOS. Compare gates using these two technologies in terms of speed and power dissipation.
[4 marks]

Answer:

	T_p (ns)	***P*** (mW)	***Noise Margin*** (mV)	***Fan-out***
TTL	9	10	400 (OH); 400 (OL)	10
CMOS	18	0.01 (static)	1050 (OH); 1340 (OL)	≤ 50

Answer:
From the table, TTL is faster than CMOS [2 marks: 1 for data, 1 for statement]
CMOS dissipates less power than TTL [2 marks: 1 for data, 1 for statement]

c) Let ABCD represent a 4 bit BCD number.

i) Draw the truth table for a combinational logic circuit that produces a '1' output when the input ABCD is an odd number and also when the number is 2. The input combination 0000 is not allowed to occur.

ii) Draw the Karnaugh map for this circuit.

iii) From the Karnaugh map, determine a minimal expressions for the output expressed in SoP form and in all NAND form.

iv) Using a truth table, show the state of the output for each of the "can't happen" input states as a result of the minimisation.

v) Draw the circuit diagrams for the minimal SoP and all NAND implementations of the function.

vi) Does the circuit have a static race hazard? Justify your answer.

[15 marks]

Answer:

i) The truth table is:

A	B	C	D	F(A,B,C,D)
0	0	0	0	X
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

[2 marks for correct truth table]

ii) The Karnaugh map is: [2 marks for the correct map]

CD	00	01	11	10
AB				
00	X	1	1	1
01	0	1	1	0
11	X	X	X	X
10	0	1	X	X

iii) A minimal SoP expression is: F=A'.B'+D [2 marks]

Applying de Morgan's theorem, the all NAND expression is: F=(D'.(A'.B')')' [2 marks]

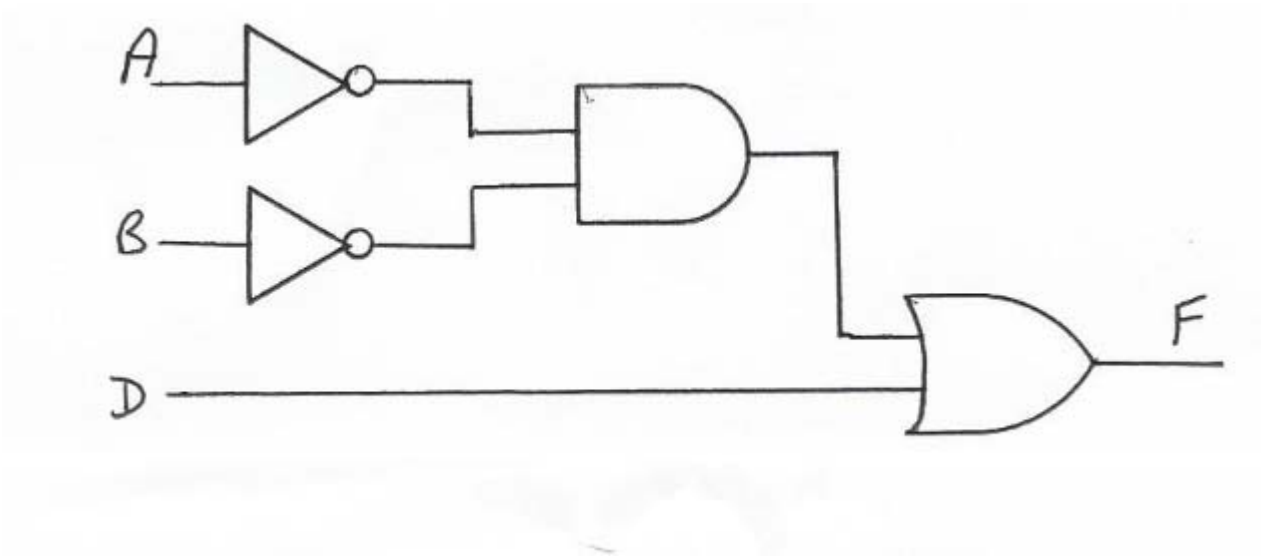
iv) The resulting output states are:

A	B	C	D	F(A,B,C,D)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

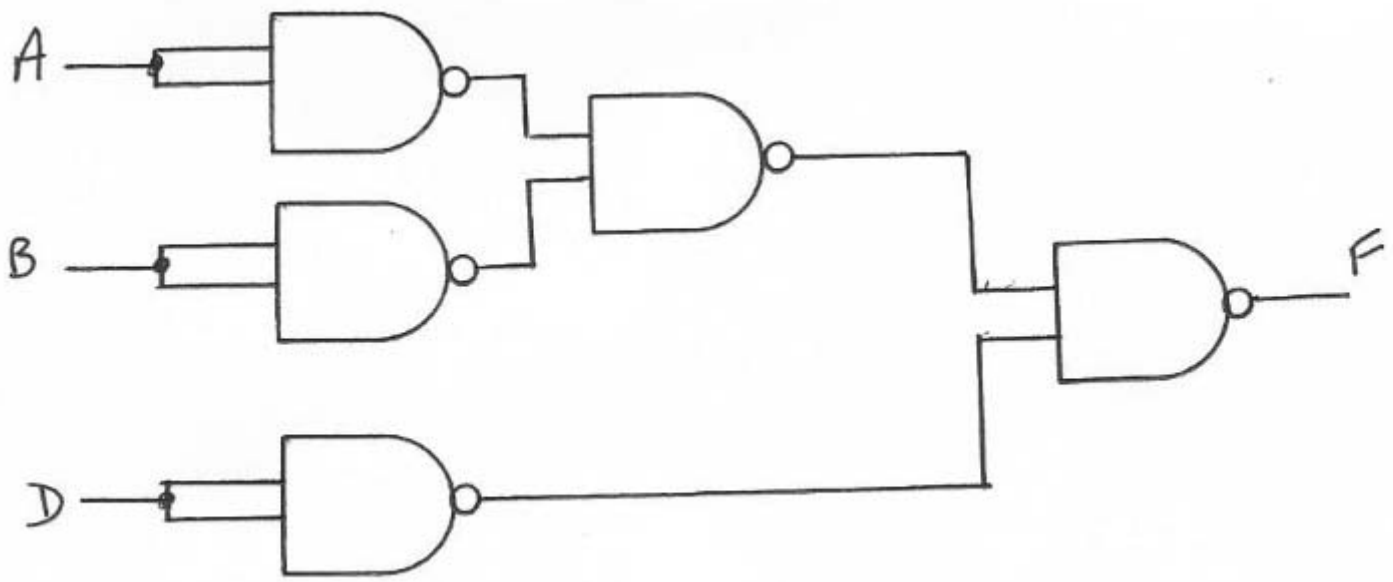
[1 mark]

v) The circuit diagrams are:

SoP:



All NAND:



[4 marks: 2 marks for each correct diagram]

vi) The circuit does not have a static race hazard [1 mark] because the map groupings overlap [1 mark].

Question 3

Figure Q3 shown a simple motor-shaft position encoder circuit. As the machine moves, the encoder shaft is rotating clock-wise manner, making and breaking the light beam between LED and phototransistor, thereby generating clock pulses to increase the counter circuit.

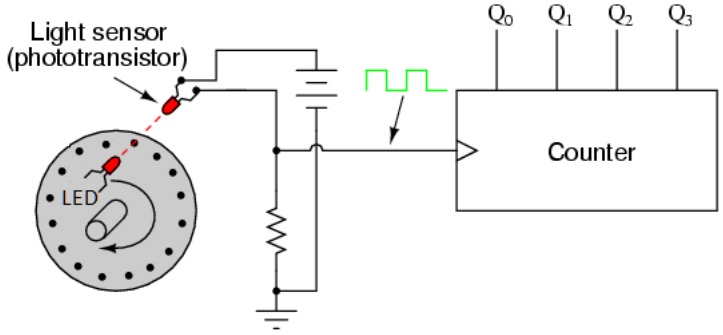


Figure Q3

Design a digital counter circuit using D flip-flops to track the angular position of the motor-shaft down to a precision of 22.5 degree.

i) Derive truth table for the counter which include present state, next state and the D flip-flop transition table to complete the input to D flip-flops.

[8 marks]

Present state	Next state	D flip-flop input			
(Q3, Q2, Q1, Q0)	(Q3, Q2, Q1, Q0)	D3	D2	D1	D0
0000	0001	0	0	0	1
0001	0010	0	0	1	0
0010	0011	0	0	1	1
0011	0100	0	1	0	0
0100	0101	0	1	0	1
0101	0110	0	1	1	0
0110	0111	0	1	1	1
0111	1000	1	0	0	0
1000	1001	1	0	0	1
1001	1010	1	0	1	0
1010	1011	1	0	1	1
1011	1100	1	1	0	0
1100	1101	1	1	0	1
1101	1110	1	1	1	0
1110	1111	1	1	1	1
1111	0000	0	0	0	0

2 marks for the correct “Present state” table; otherwise 0 marks
2 marks for the correct “Next state” table; ; otherwise 0 marks
4 marks for the correct “D flip-flop input table; ; otherwise 0 marks

ii) Construct the K-maps and finding out the minimised logic expressions for the input to D flip-flops.

[12 marks]

Q3 Q2 \ Q1 Q0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	1	0	1
10	1	1	1	1

D3 = Q3Q2′ + Q3Q0′ + Q3Q1′ + Q3’Q2Q1Q0

Q3 Q2 \ Q1 Q0	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	1	0	1
10	0	0	1	0

D2 = Q2Q0′ + Q2Q1′ + Q2’Q1Q0

Q3 Q2 \ Q1 Q0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

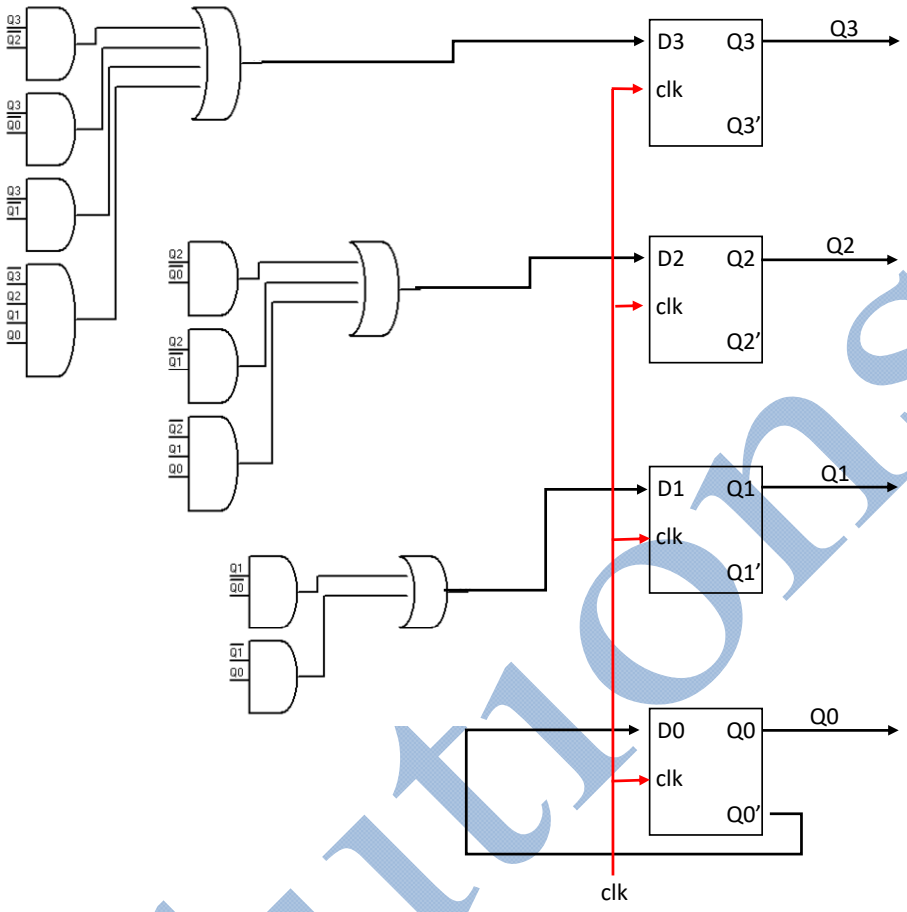
D1 = Q1’Q0 + Q1Q0′ = Q1 ⊕ Q0

Q3 Q2 \ Q1 Q0	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

D0 = Q0′

Each D input, 1 marks for the correct k-map and 2 marks for the correct minised logic expressions

iii) Draw the designed counter circuit.
[5 marks: 1 for each input logic, 2 for bistables]
Answer



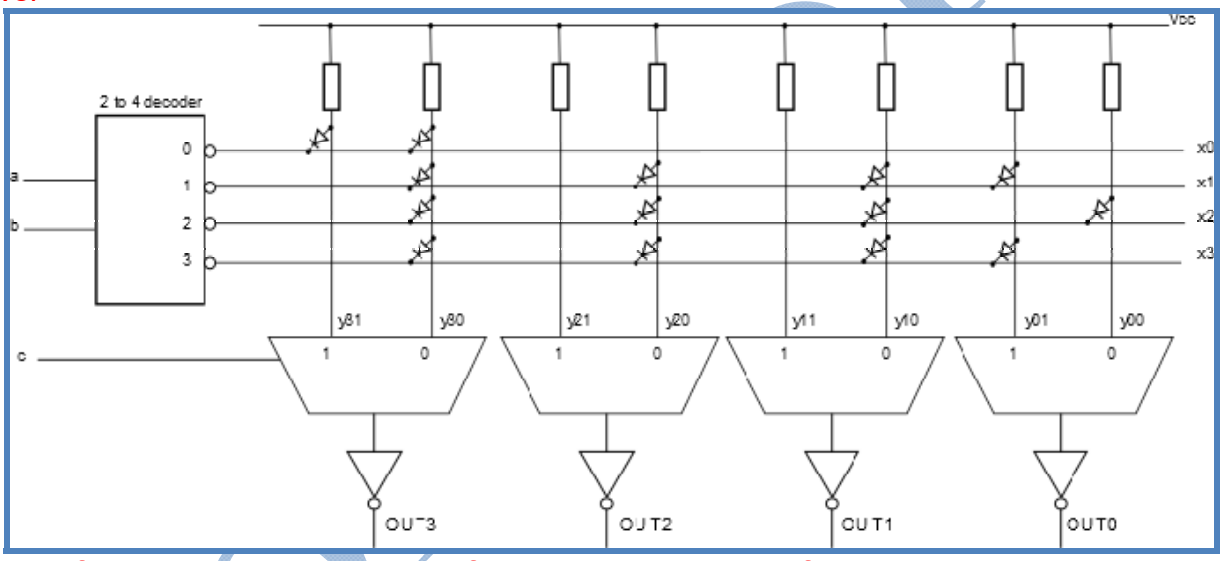
Question 4

a) Design an 8 x 4-bit read-only memory (ROM) circuit pre-programmed with the data shown in the Table Q4. (Hint: diodes, decoder, multiplexer etc. are required in the ROM circuit).

Address	Data (4-bit)
0	8
1	14
2	15
3	14
4	8
5	1
6	0
7	1

[15 marks]

Answer



[5 marks for 2 to 4 decoder, 5 marks for the diodes, 5 marks for the MUX]

b) Suppose we have a microcontroller system with 4096 Bytes of static RAM:

i) With each memory chip having a capacity of 256 bytes, how many memory chips are required to make up the total DRAM capacity?

[1 marks]

4096/256 = 16 chips

ii) How many address bits required to access the total DRAM capacity?

[1 marks]

Log(4096) / log(2) = 12 bits

iii) How many address bits are required to select the memory chips?

[1 marks]

Log (16) / (log 2) = 4

iv) Draw a block diagram of a circuit using a decoder so that all 4096 bytes of memory can be addressed.

[7 marks]

Answer: [3 marks for the correct use of 4 to 16 decoder, 2 marks for memory chips, 2 marks for the address bus and lines]