EBU4202 Digital Circuit Design 2018-19
Week 3 Tutorial

1) Consider the circuit shown in Figure 1. Answer the following questions:
   a. What is the name for this type of flip-flop?
   b. Imagine that S_L now goes low. R_L remains high. Use your knowledge of the operation of gates to determine the new values of Q and QN

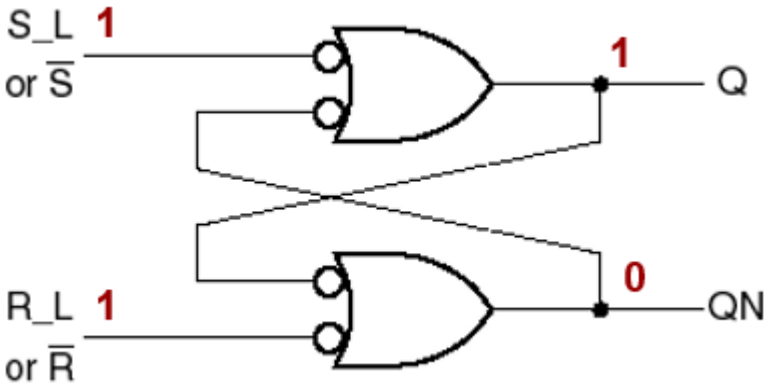

Figure 1: Circuit diagram of a flip-flop

2) Consider the circuit shown in Figure 2. Answer the following questions:
   a. What is the name for this type of flip-flop?
   b. Imagine that S now goes low. R = 0 and C = 1. Use your knowledge of the operation of gates to determine the new values of Q and QN
   c. Imagine that C now goes low. S = 0 and R = 0. Use your knowledge of the operation of gates to determine the new values of Q and QN
   d. Imagine that C now goes high. S = 1 and R = 0. Use your knowledge of the operation of gates to determine the new values of Q and QN

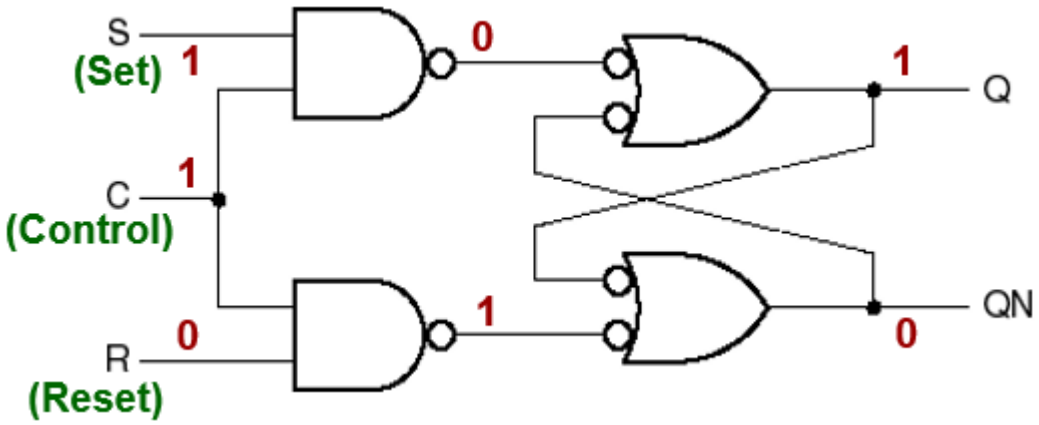

Figure 2: Circuit diagram of a flip-flop

3) Consider the circuit shown in Figure 3. Answer the following questions:
    a. What is the name for this type of flip-flop?
    b. Imagine that C now goes high. D = 1. Use your knowledge of the operation of gates to determine the new values of Q and QN
    c. Imagine that D now goes low. C = 1. Use your knowledge of the operation of gates to determine the new values of Q and QN
    d. Imagine that C now goes low. D = 0. Use your knowledge of the operation of gates to determine the new values of Q and QN

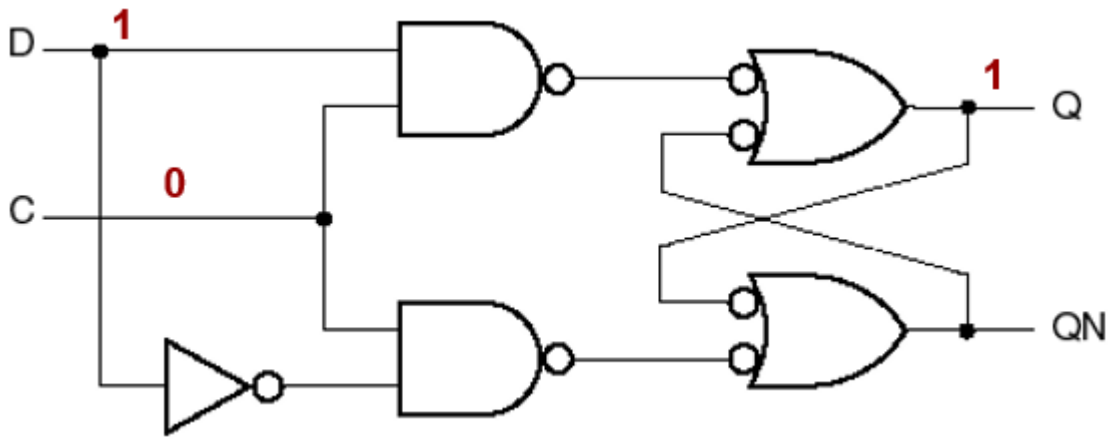

Figure 3: Circuit diagram of a flip-flop

4) What is a synchronous state machine?

5) In the context of bistable elements and state machines, what is meant by the term "metastability"?

6) Explain the difference between a Moore and Mealy machine.

7) What is the minimum number of flip-flops required to store 35 states?

8) Consider an SR latch. What is the maximum clock frequency for a circuit having a maximum delay T_D? How can the circuit become unstable?

9) Consider the circuit shown in Figure 4. Answer the following questions.

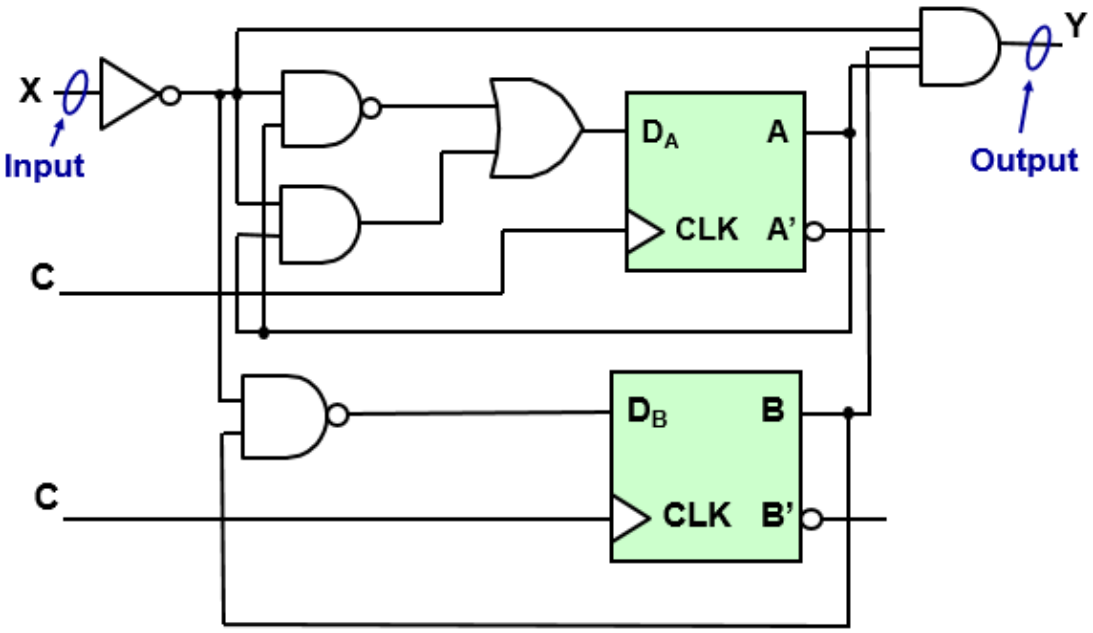

Figure 4: Circuit diagram for the first section of a FSM

a. What type of FSM is depicted in Figure 1?
b. Draw-up: input, next state, and output equations for the FSM depicted in Figure 1.
c. Based on your answers to question 6)b) prepare the: transition table, state table, and state/output table.
d. Finally draw the state diagram for the FSM shown in Figure 1.

10) Design an autonomous sequential circuit, based on JK-type bistables, which generates the following sequence of states: 000, 010, 111, 101, 100 110. The transition table of JK Flip-Flop is given in Figure 5 below. Note: You must draw the circuit diagram, but there is no need to draw the state diagram.

J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q

Figure 5: Transition Table for Edge Triggered JK Flip-Flop