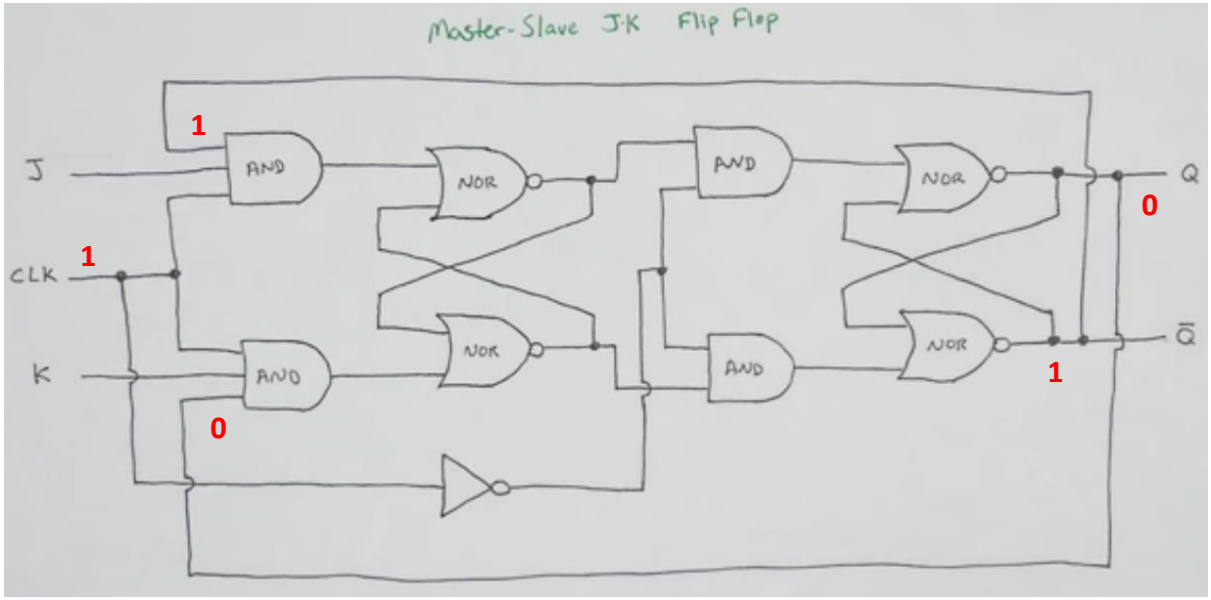
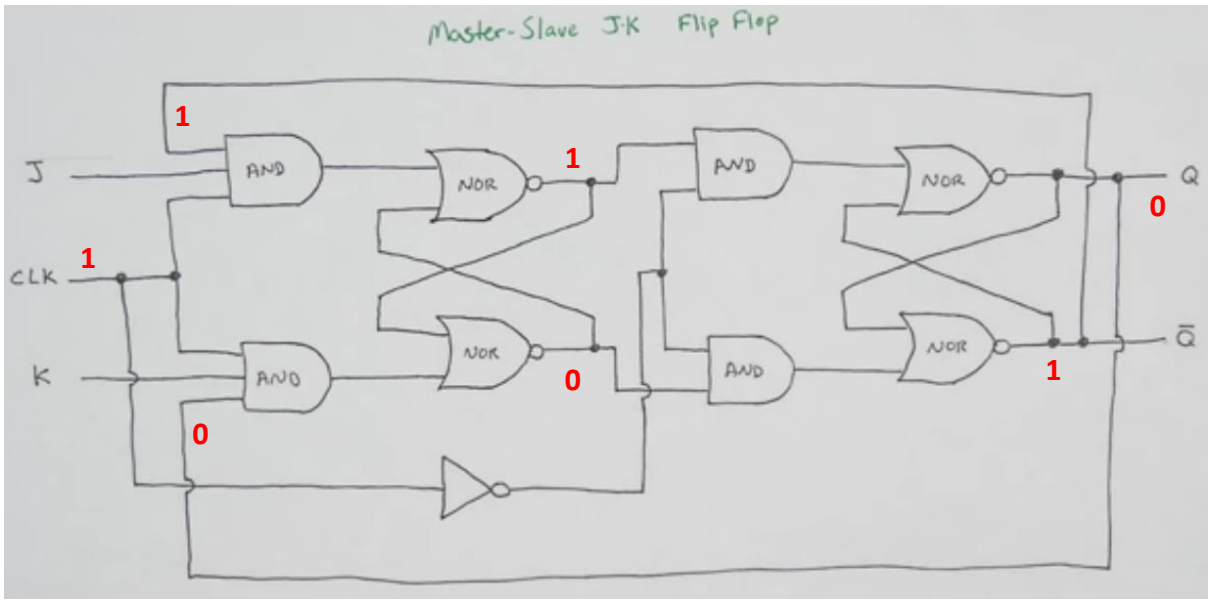
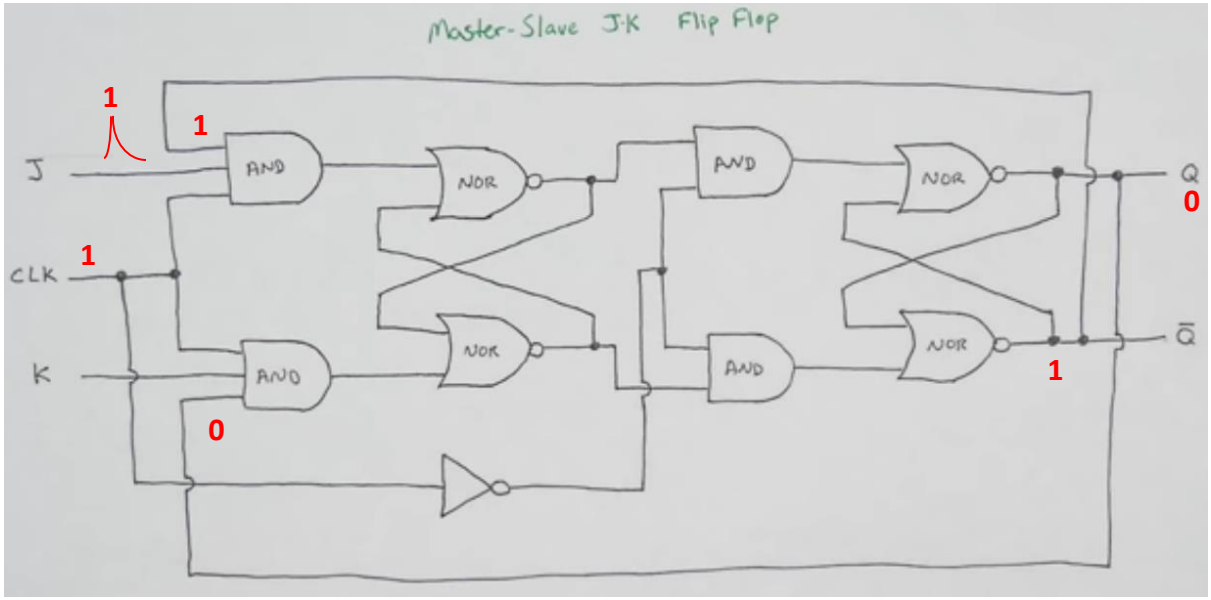
The following example illustrates the 1's catching problem that can occur in Master Slave JK flip-flops. Consider the circuit shown below.



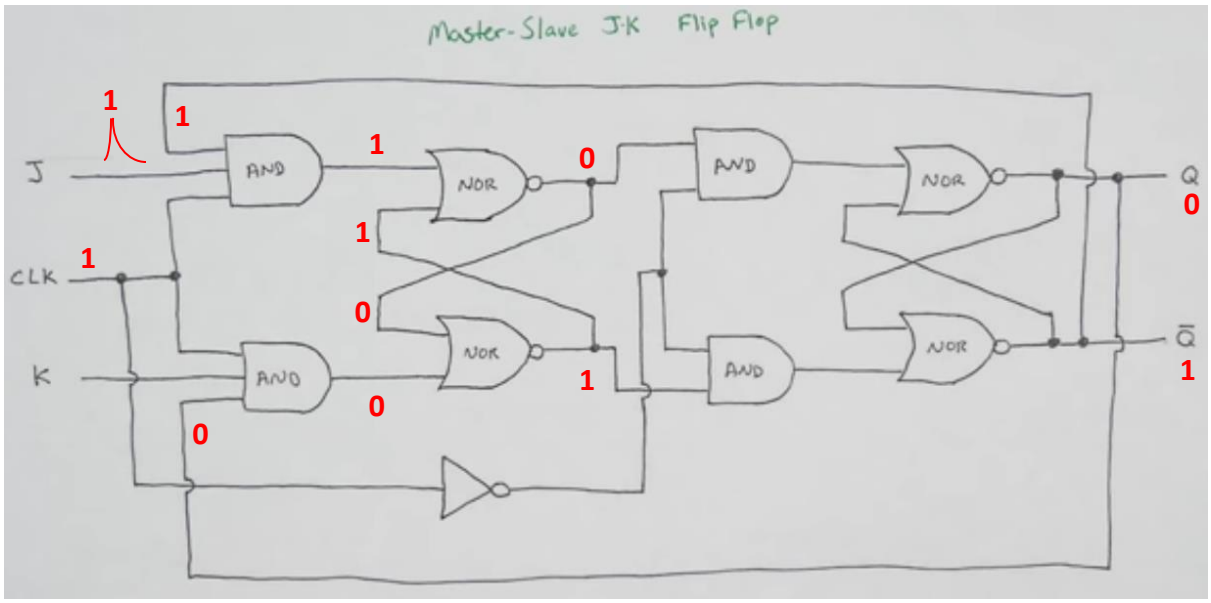
Let's see how these inputs propagate through the circuit



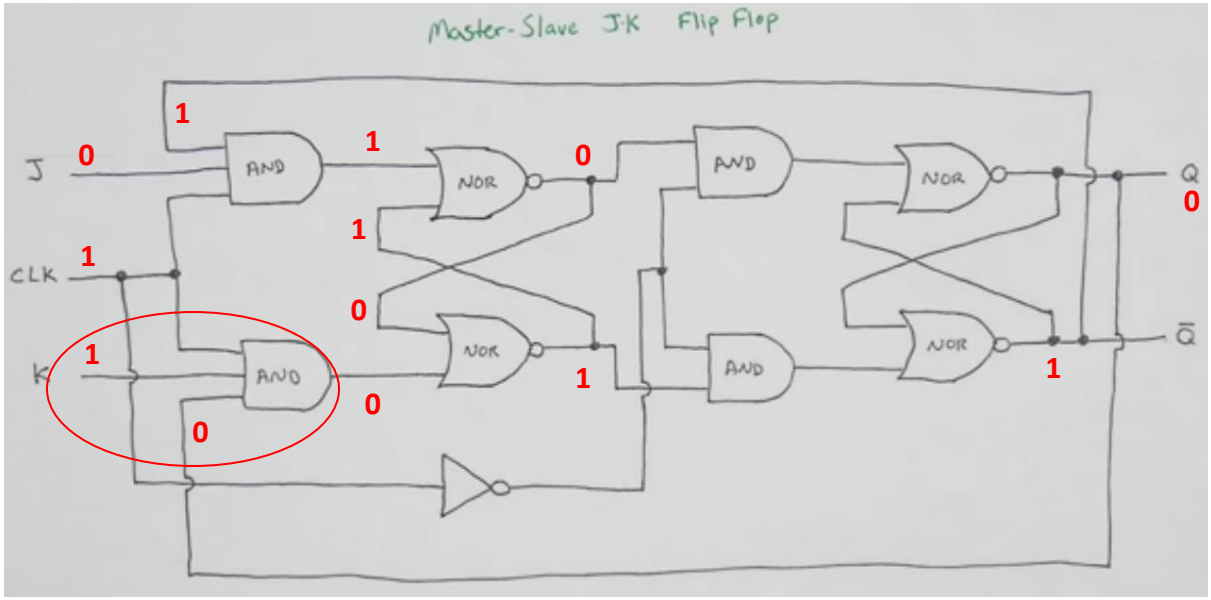
Now consider what happens if a glitch occurs on the J input



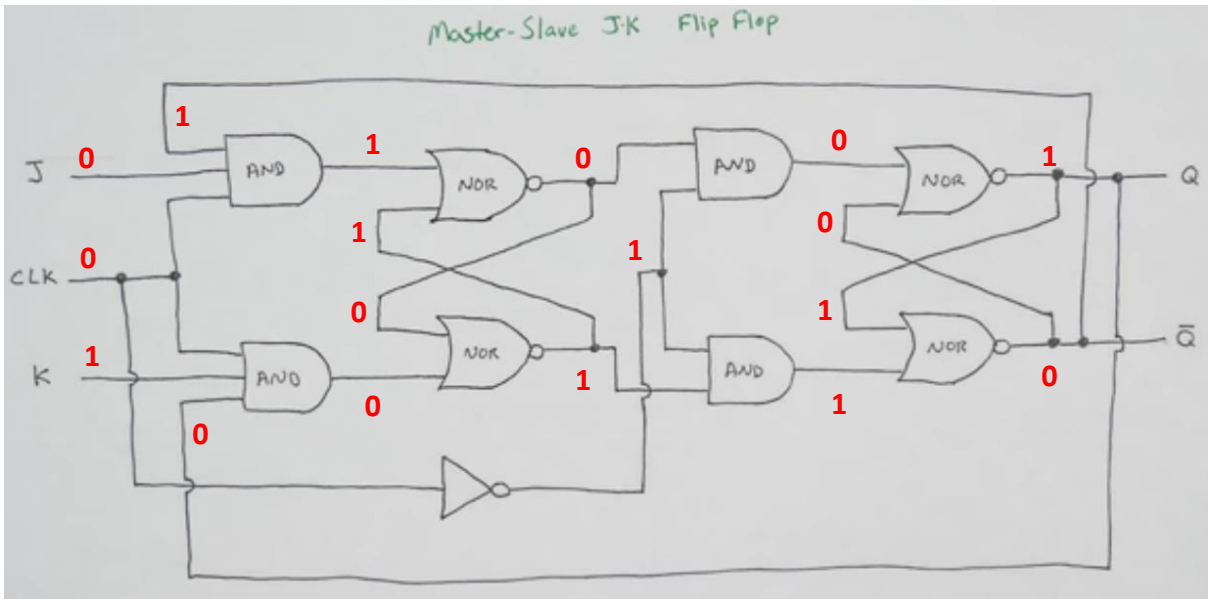
Let's see how this glitch propagates through the circuit



Now let's see what happens if the J becomes 0 and K becomes 1. Q_{Slave} is ANDed with K. $Q_{Slave} = 0$, therefore the output of the AND gate is zero. For this reason, the Q_{Master} output remains unchanged.



Now consider that the clock goes to 0. Now the slave flip-flop is activated and $Q_{Master} = 1$.



So, from this example, we see that a glitch on the input can propagate all the way through to the output.