Q1

- Using a 5-variable Karnaugh Map, find the minimal PoS for the Switching Algebra function,

G(M, N, O, P, Q) = ∑m(1, 2, 5, 8, 11, 12, 16, 20, 21, 22, 24) + d(0, 4, 6, 28, 31)

M = 0

NO \ PQ	00	01	11	10
00				
01				
11				
10				

M = 1

NO \ PQ	00	01	11	10
00				
01				
11				
10				

Q2

- A small company has 100 shares of stock, and each share entitles its owner to 1 vote at a stockholders' meeting.
- There are only 4 shareholders: Mr Adams owns 10 shares, Mrs Brown owns 20 shares, Ms Cayman owns 30 shares and Mr Davidson owns 40 shares. A two-thirds majority is required in order to pass a measure at a stockholders' meeting.
- An important and sensitive vote is coming up and it has been decided that a degree of secrecy is necessary. This is to be achieved by providing each stockholder with a switch that can be switched one way for "yes" and another way for "no". A *switching circuit is to be designed* to turn on a light if the vote achieves the required two-thirds majority.
- Assume that the switch provide logic **1** for "yes" and logic **0** for "no".
  - Identify those combinations of shareholders that hold between them two-thirds or more of the shares, and write the Boolean expression that describes the required behaviour of the switching circuit. Then derive the simplest Boolean expression for this circuit in the form of a PoS, using a Karnaugh map.
  - Your answer must also include clearly the variables and their meaning (i.e. inputs and output) of your resulting switching circuit.

Let us denote the following Boolean variables:

A – vote from Mr Adams (A = 1 is a “yes” vote; A = 0 is a “no” vote)

B – vote from Mrs Brown (B = 1 is a “yes” vote; B = 0 is a “no” vote)

C – vote from Ms Cayman (C = 1 is a “yes” vote; C = 0 is a “no” vote)

D – vote from Mr Davidson (D = 1 is a “yes” vote; D = 0 is a “no” vote)

The combinations of shareholders that lead to a majority of at least two-thirds (i.e., > 66.7%) are:

CD (70% majority); ABD (70% majority); ACD (80% majority); BCD (90% majority); ABCD (100% majority).

(Mr Adams owns 10 shares, Mrs Brown owns 20 shares, Ms Cayman owns 30 shares and Mr Davidson owns 40 shares)

- Therefore, the required logic function is:

$$F(A,B,C,D) = CD + ABD + ACD + BCD + ABCD$$

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A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

AB \ CD	00	01	11	10
00				
01				
11				
10				

MPS of F:

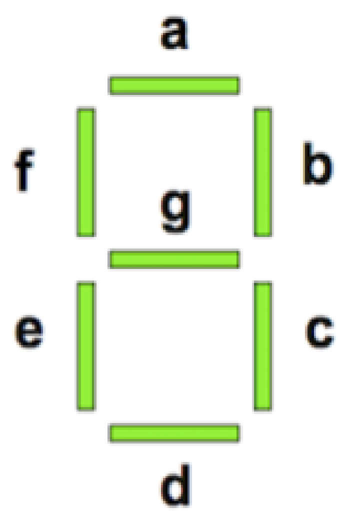
Q3

- ***Problem***: Suppose an alarm is to sound if the key is in the ignition and the door is open, ***or*** if the key is out of the ignition and the brake is off, ***or*** if the door is open and the brake is off. At all other times, the alarm must be silent.
- Derive a logic equation for the alarm going off.

Q4

A binary-to-hexadecimal code converter will be designed. Given a 4-bit binary input WXYZ, the code converter generates the 7-bit output necessary to display the hex characters ‘0’, ‘1’, ‘2’, ‘3’, ‘4’, ‘5’, ‘6’, ‘7’, ‘8’, ‘9’, ‘A’, ’b’, ’C’, ’d’, ’E’ and ‘F’ as follows:

Figure below shows the naming of each LEDs in a 7- segments display:



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- Produce a truth table for the segment ‘a’ in the 7-segments display.
- Use a Karnaugh map to find a minimal sum of products for output “a”.

Q5

A washing machine alarm tone (**Z**) is designed so that it accepts 3 input signal lines. Line **A** is from the machine door control, whereas lines **B** and **C** are from the wash cycles or states control unit. The following two conditions apply:

- The "door of the washing machine is closed" is represented by **A=1**, otherwise **A=0**.
- The remaining 2 inputs (**B** and **C**) decide the position or the state of the wash (i.e., there are 4 different wash cycles numbered **0-3**, equivalent to **00**, …, **11**).

1)Write the Truth Table for the washing machine alarm tone (**Z**) that produces a *logic 1* (i.e., it rings the alarm bell) when the washing machine has the door closed and the wash cycle is in one of the following states: state **0**, state **1** or state **3**.

2)Write the *minterm expansion* for **Z** and simplify algebraically to a minimum *Sum of Products* form. Show all your work.

3) Draw a clearly labelled circuit logic diagram for the minimised equation.

4) Rewrite the simplified design obtained in *part ii)* as a NAND gate implementation. How many logic gates are now necessary to implement this circuit design?

Q6

Consider the following problem description: “Design a combinational circuit that detects number **1** and prime numbers in the range **0-7**, based on the combined value of its inputs.” Answer the following questions with reference to the problem description above:

1) Write the Truth Table for this circuit, indicating clearly all its inputs and output.

2) Derive a Switching Algebra expression for the circuit, based on the Truth Table obtained in *part 1)*, and then simplify it using appropriate Switching Algebra theorems.

3) Draw a clearly labelled circuit logic diagram for the minimised equation.

Q7

Consider the combinational circuit described by the Switching Algebra expression:

$$F(A,B,C,D) = ABC' + ACD' + AB'D + BC'D.$$

1)Expand the expression above into a *canonical Sum of minterms.*

2)Simplify the expression above using a *Karnaugh Map* and give your answer in the form of a *minimal Product of Sums*, showing all your work.