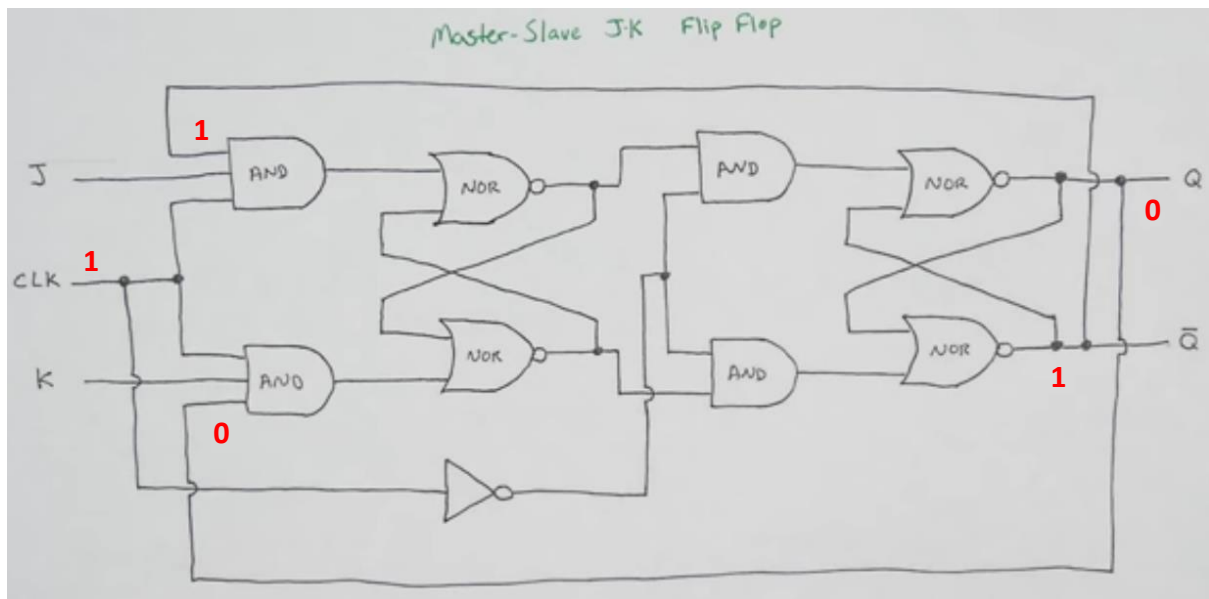
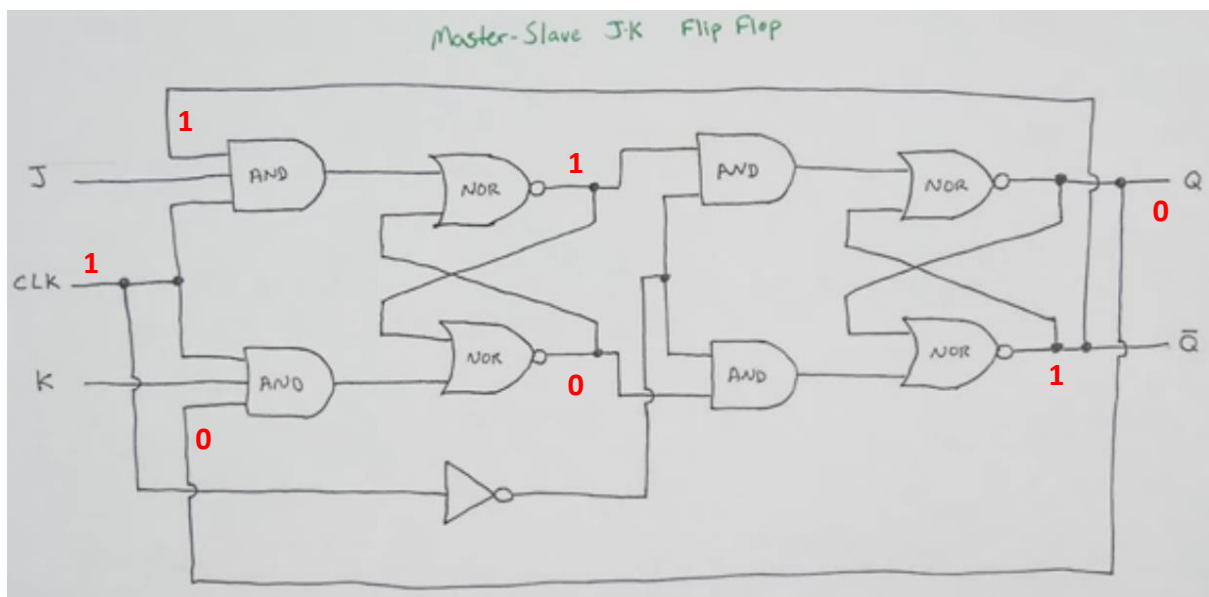


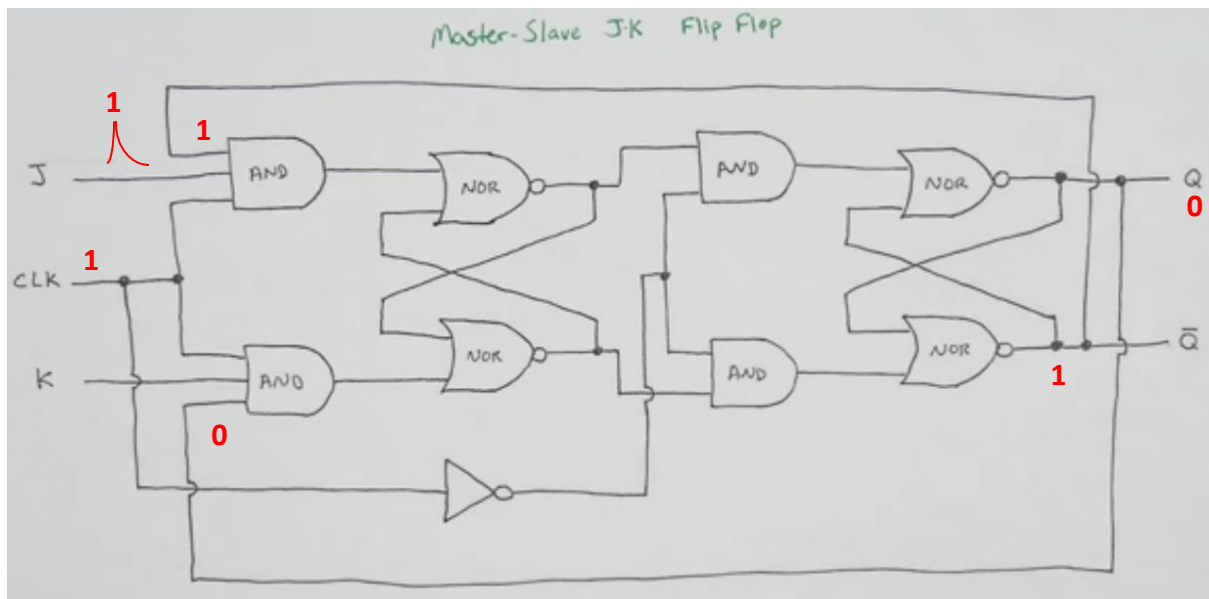
The following example illustrates the 1's catching problem that can occur in Master Slave JK flip-flops. Consider the circuit shown below.



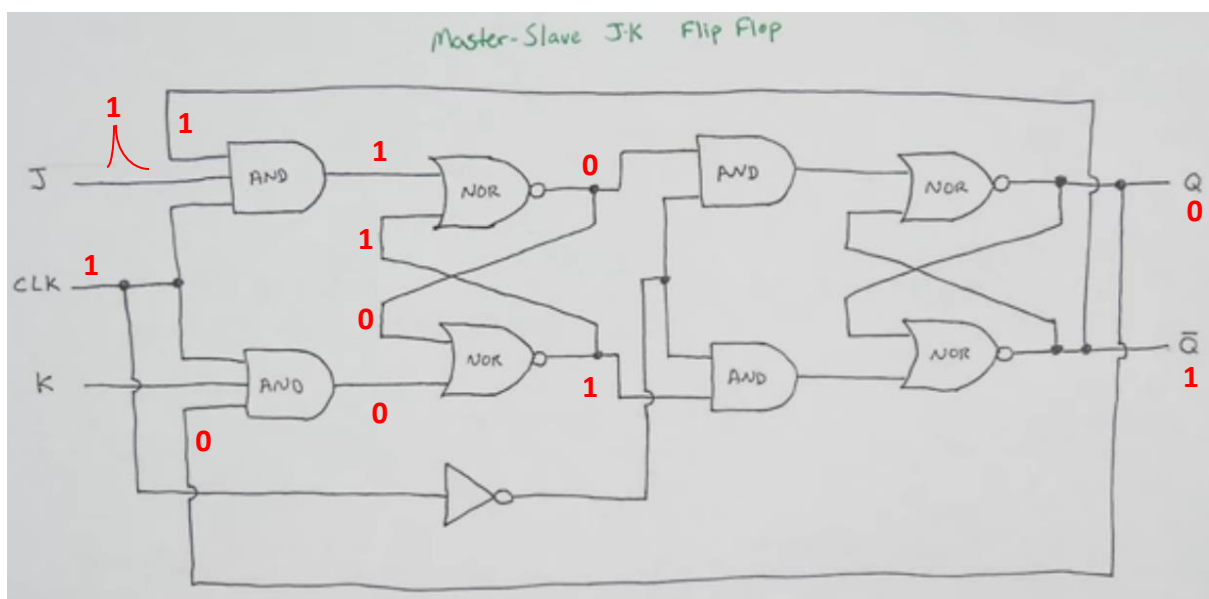
Let's see how these inputs propagate through the circuit



Now consider what happens if a glitch occurs on the J input



Let's see how this glitch propagates through the circuit



Master-Slave J-K Flip Flop

The diagram illustrates a Master-Slave J-K Flip Flop circuit. The inputs are J (0), K (1), and CLK (1). The outputs are Q (0) and Q-bar (1). The circuit consists of two main stages: a Master stage and a Slave stage. The Master stage is composed of two AND gates, two NOR gates, and an inverter. The Slave stage is composed of two AND gates and two NOR gates. The inputs J and K are connected to the Master stage. The output of the Master stage is connected to the Slave stage. The output of the Slave stage is connected to the final outputs Q and Q-bar. The values 0 and 1 are indicated at various points in the circuit, showing the state of the signals. A red circle highlights the input K and its connection to the Master stage.

Master-Slave J-K Flip Flop

The diagram illustrates a Master-Slave J-K Flip Flop circuit. It consists of two main stages: a Master stage and a Slave stage, both implemented as J-K flip-flops. The inputs are J=0, K=1, and CLK=0. The outputs are Q=1 and Q1=0. The circuit uses AND, NOR, and NOT gates to implement the J-K flip-flop logic. The Master stage has inputs J and K, and the Slave stage has inputs J and K. The clock signal CLK is connected to the clock inputs of both stages. The output of the Master stage is Q, and the output of the Slave stage is Q1.