Revision

* Introduction
* Bistable Elements
* Latches & Flip-Flops
* Analysis Procedure
* Design Procedure

Chapter 7 – “Digital Design: Principles and Practices” book

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Leaning Objectives for the Session

By the end of the session all students will be able to:

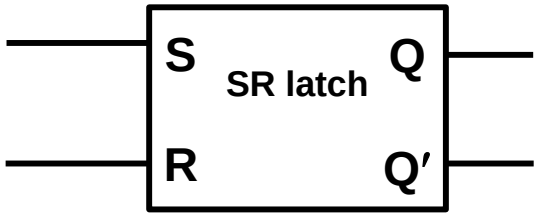
1)recognise the different types of latches and flip-flops, introduced in this module.

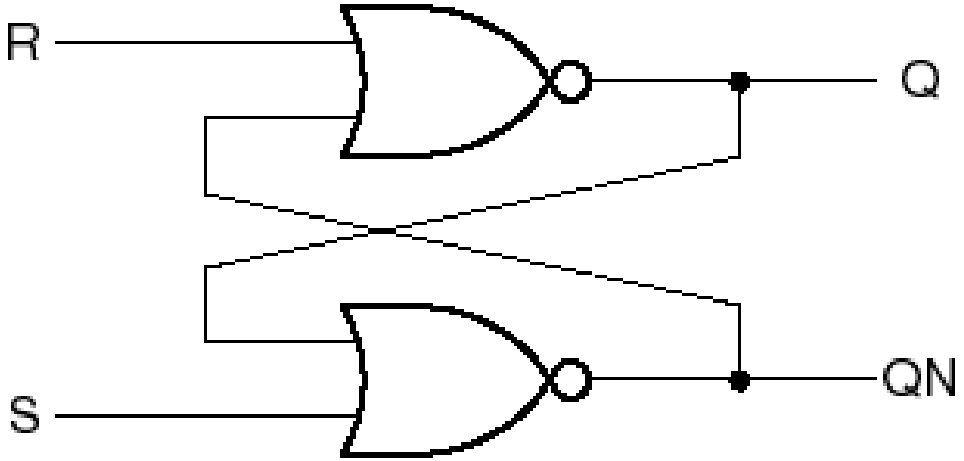
2)explain the differences and similarities between these different latches and flip-flops.

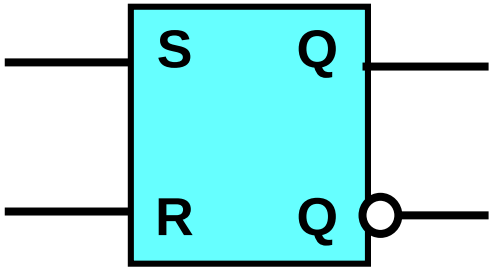
3)analyse different types of latch and flip-flop to understand how a change on the input will affect the outputs.

Latches

- SR latch – Simplest type.







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Latches and Flip-Flops

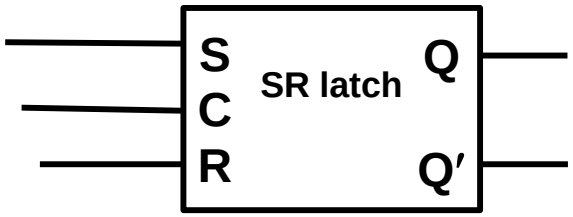
- SR latch – Simplest type.

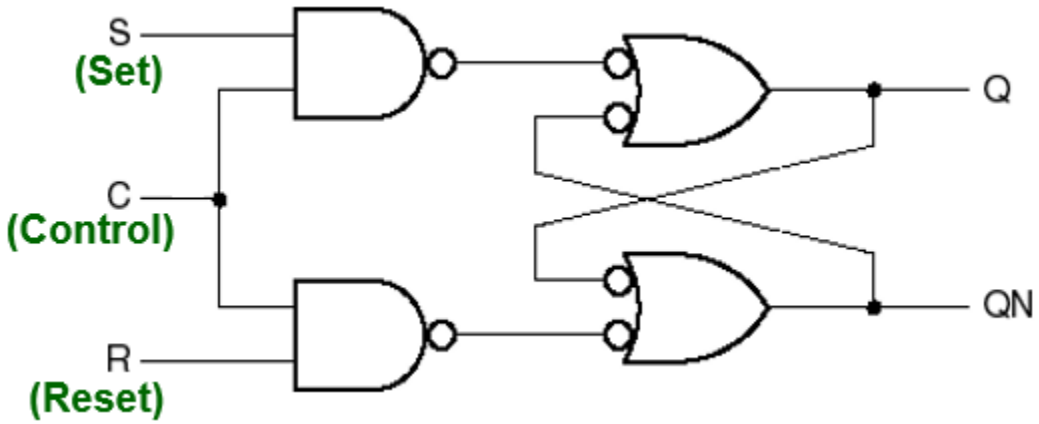
Inputs		*Outputs*	
S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

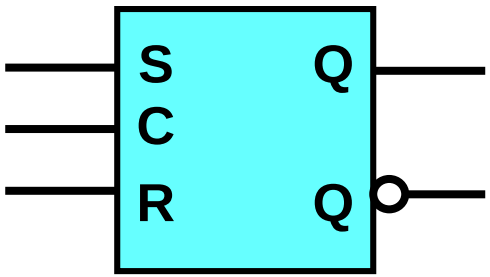
Illegal (invalid) operation when both inputs are ***True***.

Latches

- SR latch with control line – Same as SR but AND gate connected to each input. The same control signal is applied one input of each AND gate. Other input is S or R, respectively.







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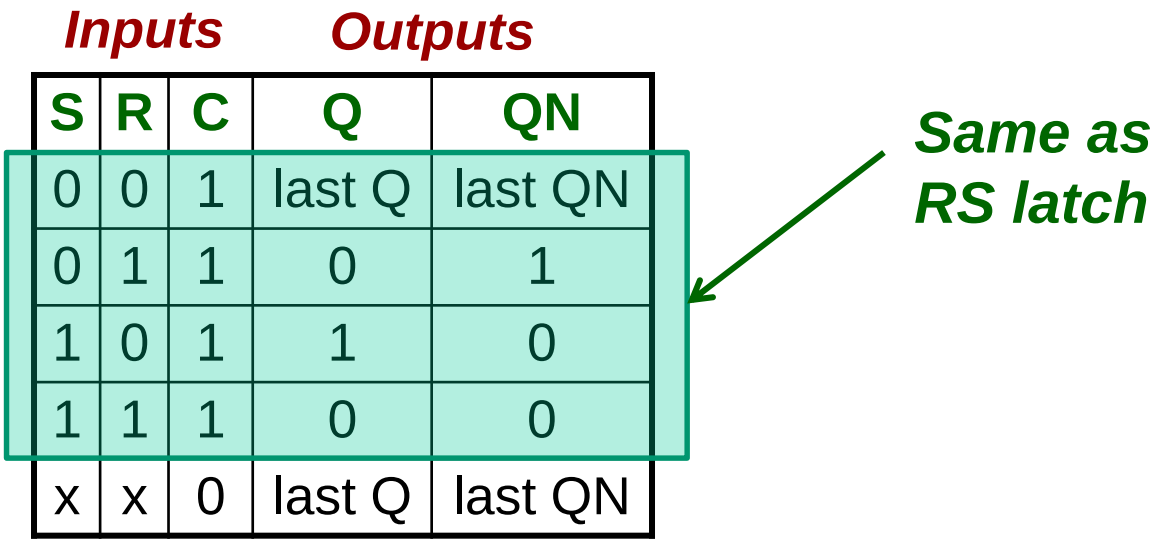
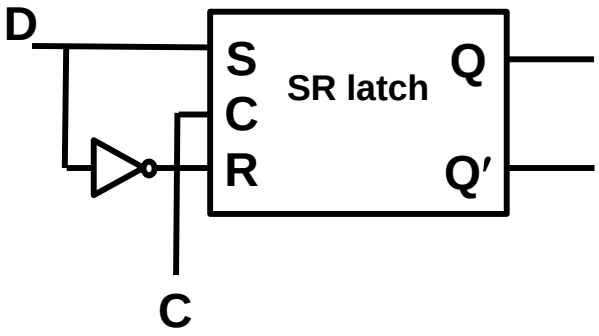
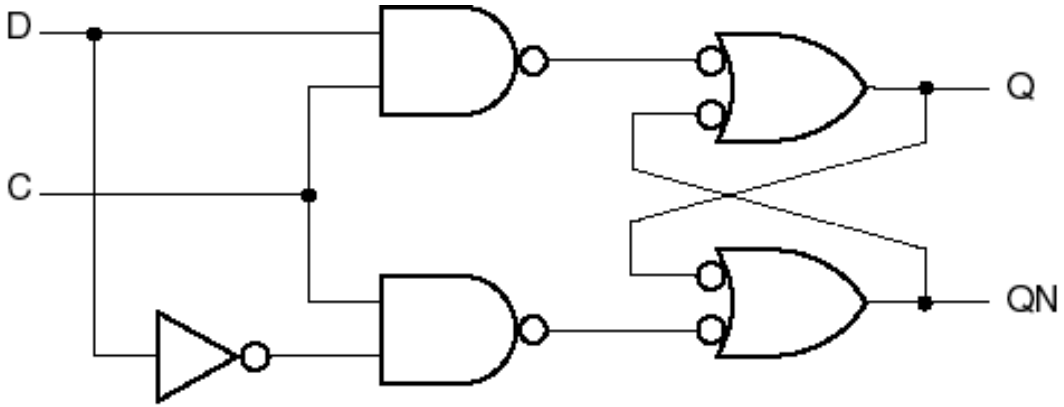
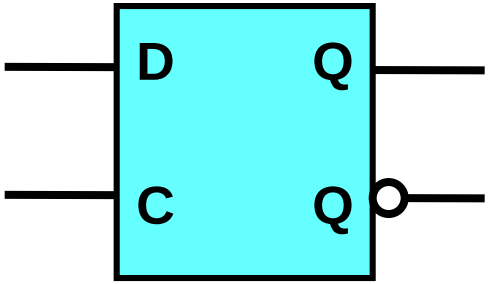


Latches

- D(-type) latch – Same as SR but has only 1 input D (equivalent to S). R = D' ≡ S'. Solves problem of S = R = 1 being presented to latch which caused it to give an illegal output, namely: Q = Q' = 0







Latches

- D(-type) latch – Same as SR but has only 1 input D (equivalent to S). R = D' ≡ S'. Solves problem of S = R = 1 being presented to latch which caused it to give an illegal output, namely: Q = Q' = 0

Inputs		*Outputs*	
C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

***reset* state**

***set* state**

Latches

Same as RS latch

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

RS latch

S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	0	0
x	x	0	last Q	last QN

RS latch with control

C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

D latch

Latches

Latch stores last state

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

RS latch

S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	0	0
x	x	0	last Q	last QN

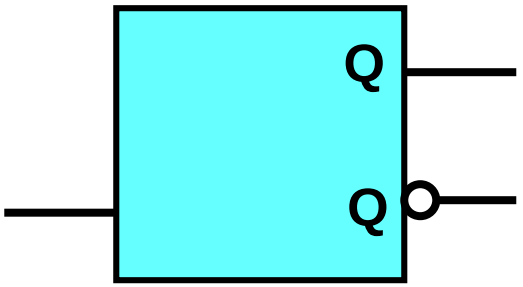
RS latch with control

C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

D latch

Latches

- The circuit symbol of a latch is a rectangular box with 2 outputs, Q and Q' and 1 or more inputs.



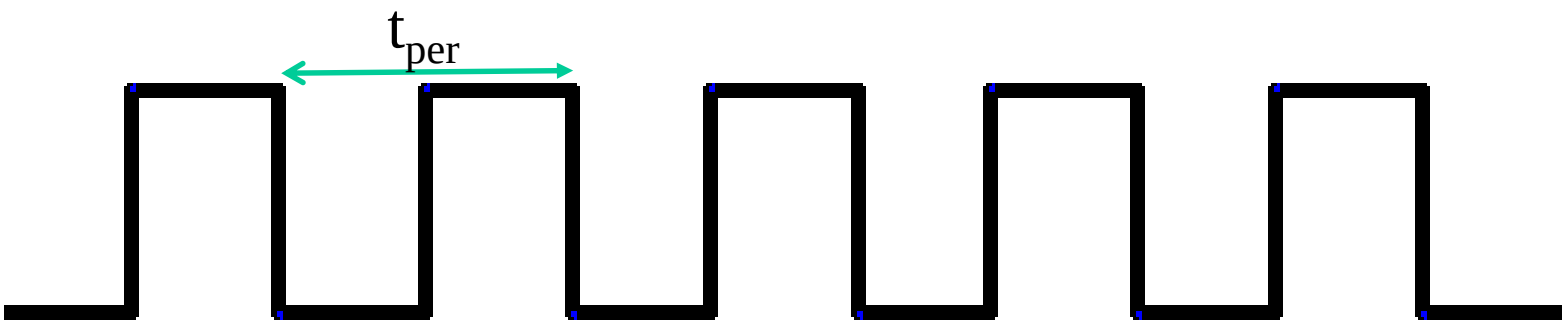
Difference between Latch and Flip-Flop

- Difference between latch and flip-flop – **Latch** has no clock input so its operation is **not synchronized** with the clock. **Flip-flop** has a clock input so its operation **is synchronized** with the clock

- Only flip-flop is suitable for use in a synchronous sequential circuit

Clock Signal

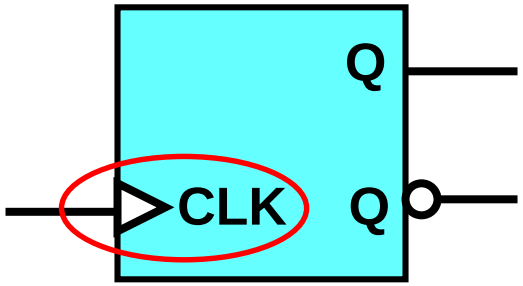
- Image below shows a typical clock signal



frequency = $1/t_{per}$

Clock Signal

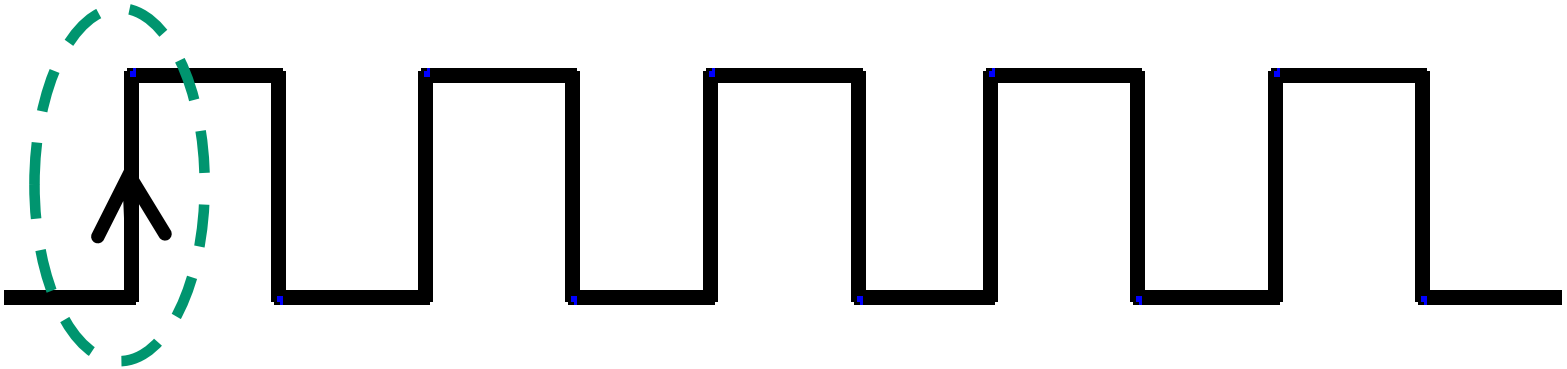
- In the circuit symbol for a flip-flop we use a triangle and the letters CLK to denote that the flip-flop is triggered on a clock edge.



- An edge triggered flip-flop will ignore the inputs while the clock pulse is at a constant level. It will only set the outputs on clock pulse transitions.

Clock Signal

- There are 2 edges associated with the clock.



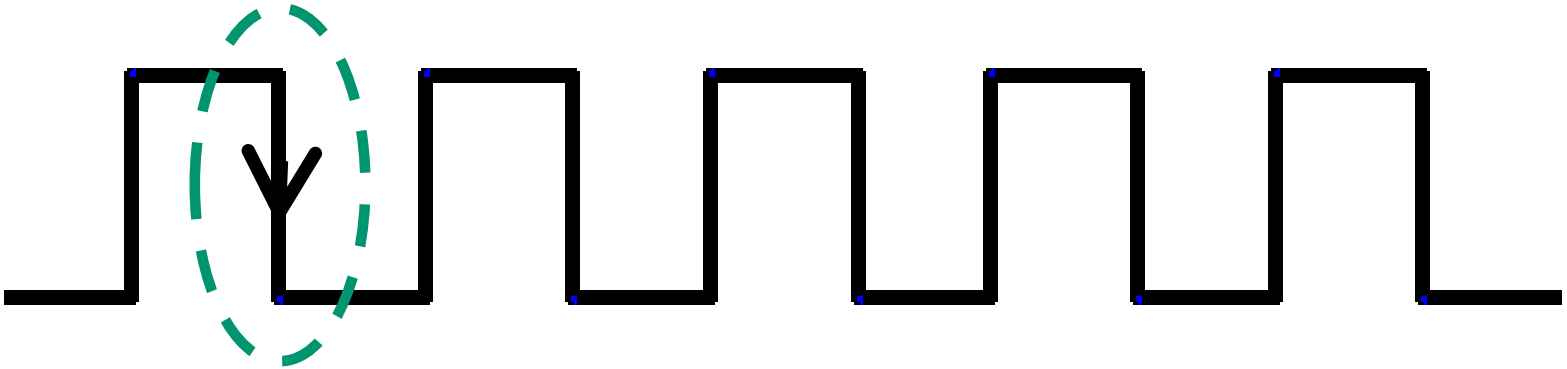
Rising edge

Denoted  in a truth table

- Could trigger flip-flop from either the rising or falling edge of the clock.

Clock Signal

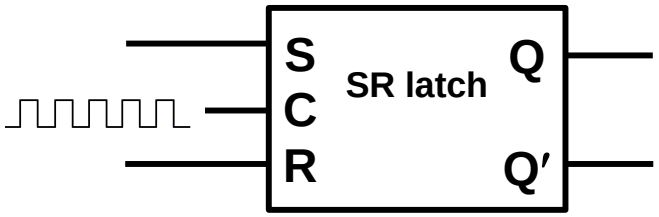
- There are 2 edges associated with the clock.



- Could trigger flip-flop from either the rising or falling edge of the clock.

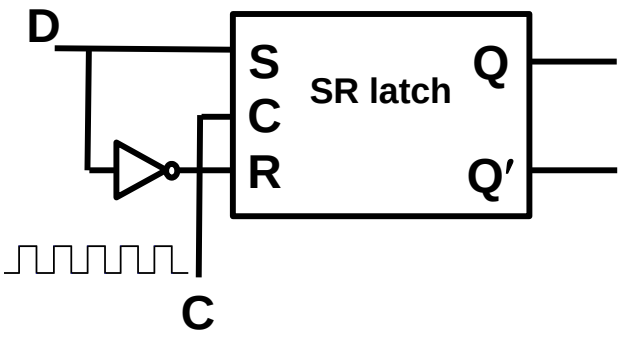
Flip-Flops

- The SR flip-flop – Same as SR latch with control line but the control line attached to a clock signal.



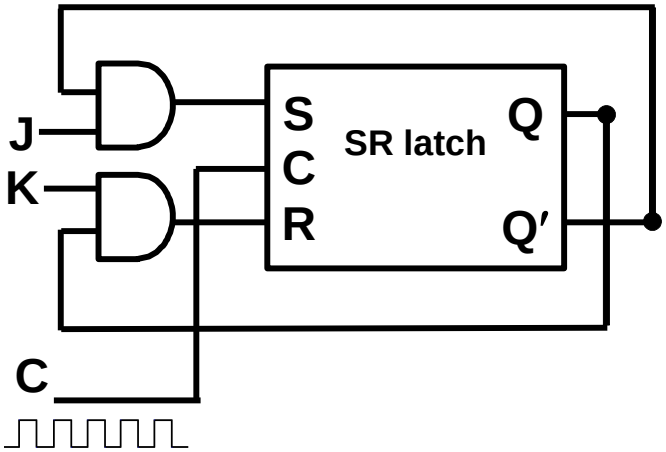
Flip-Flops

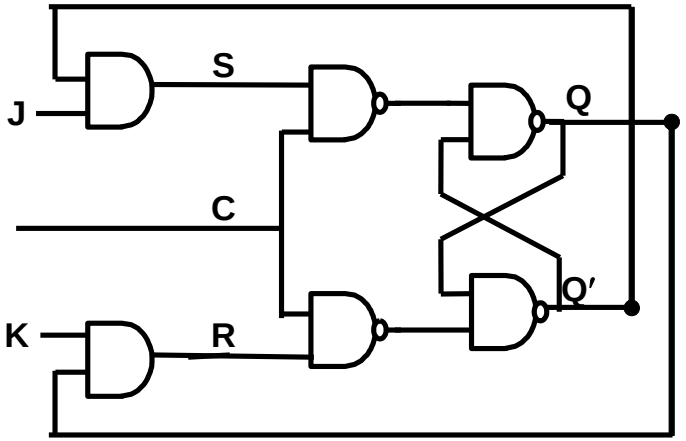
- The D flip-flop – Same as D latch but includes a clock input

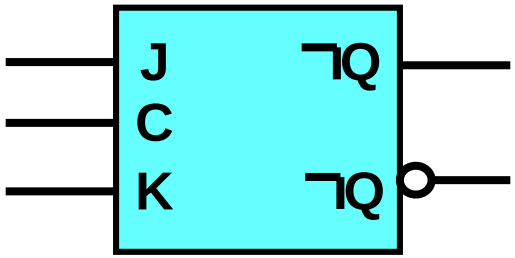


Flip-Flops

- A JK flip-flop – Same as SR flip-flip but additional AND gates are added before the S and R inputs. One inputs to AND gate on S is connected to Q'. One inputs to AND gate on R is connected to Q







Flip-Flops

- A JK flip-flop – Normally edge triggered.

J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q

Flip-flop stores last state

Flip-Flops

- A JK flip-flop – Normally edge triggered.

J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q

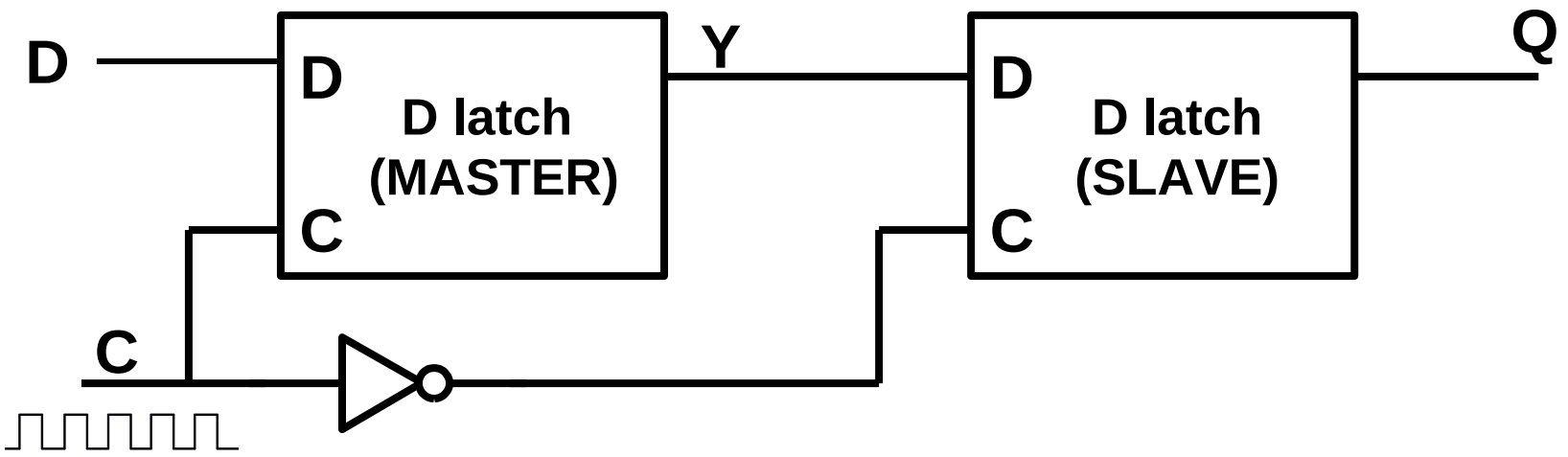
Same as RS latch

- Notice that, unlike for the RS flop-flop, there is no illegal state. Due to the feedback from output to input S and R are always different

Flip-Flops

- Master Slave – The name for a way of ganging together flip-flop. Output of Master flip-flop is connected to input of Slave flip-flop. Clock input to Slave is inverted with respect to that of Master.

- Figure below shows Master Slave connection of D flip-flops



Flip-Flops

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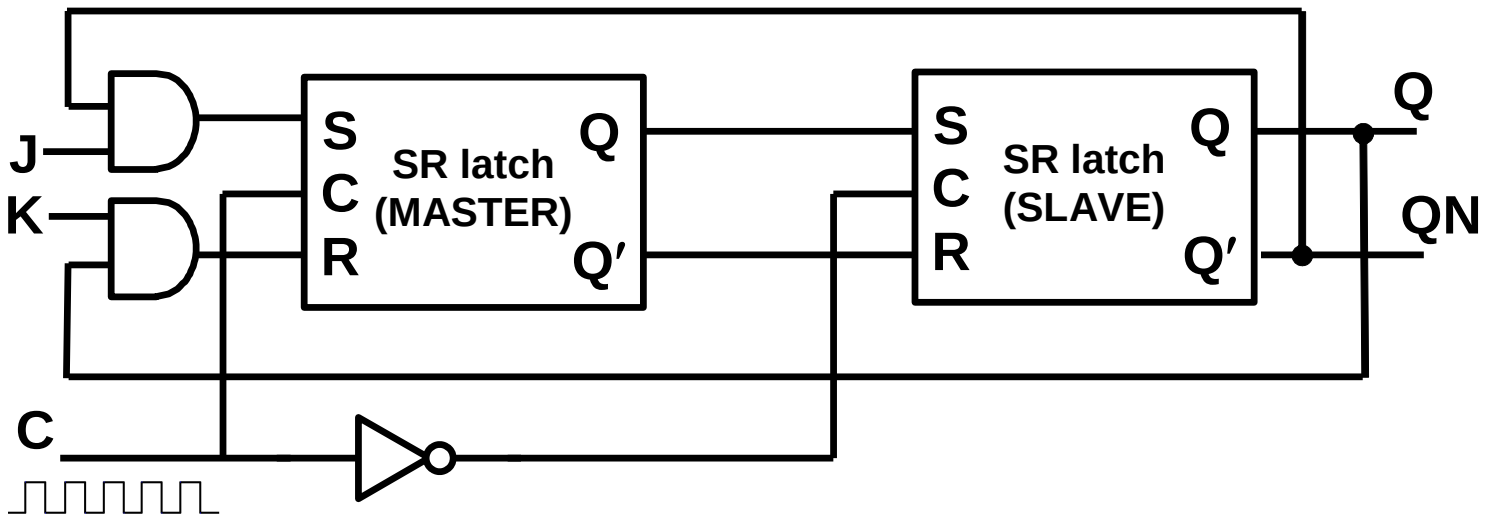
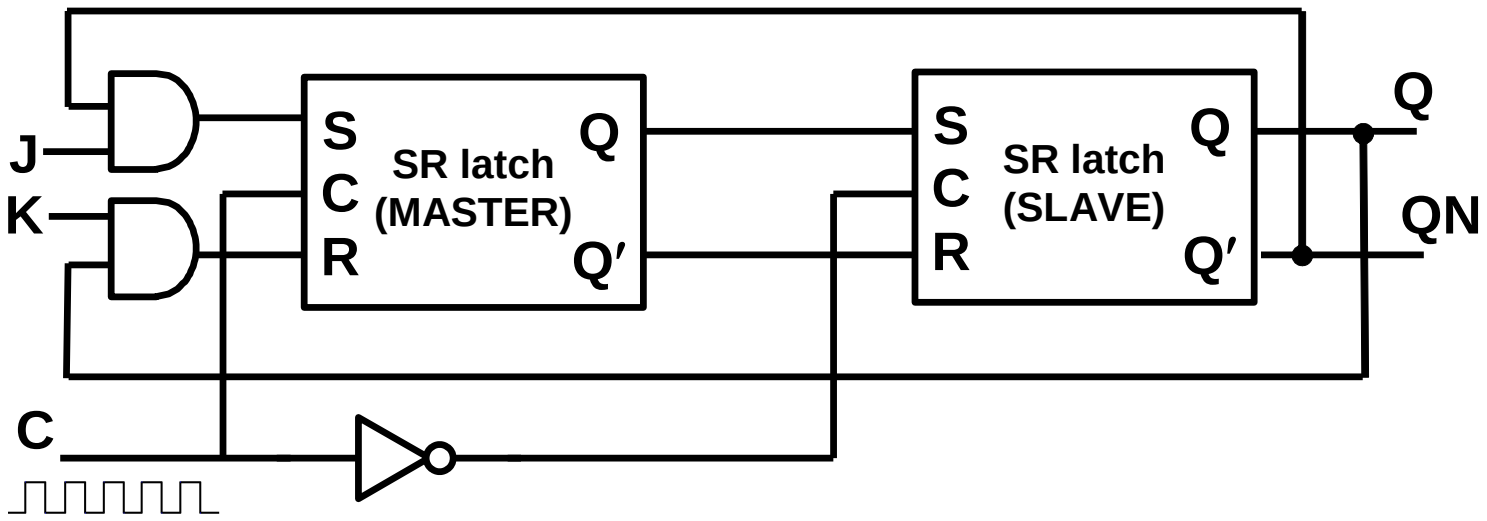


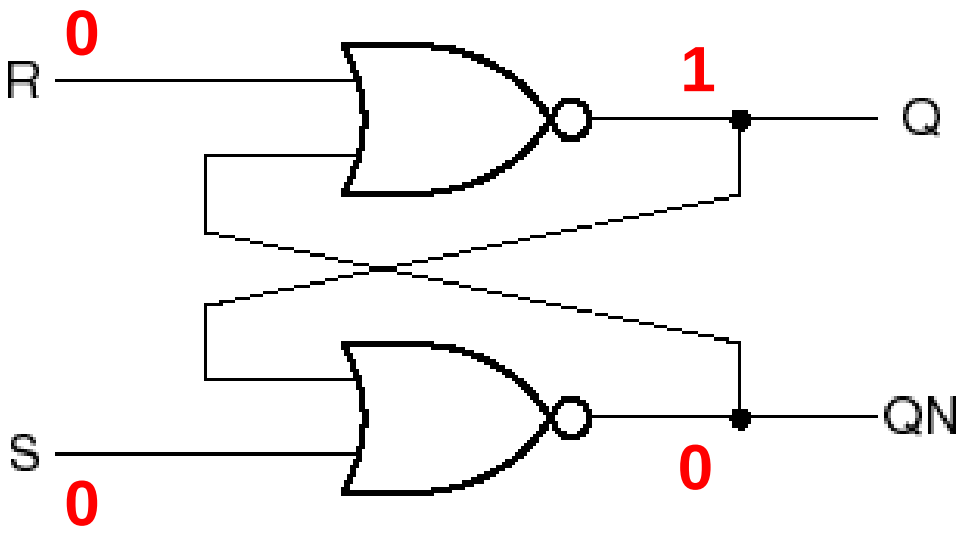
Flip-Flops

- Figure below shows Master Slave connection of JK flip-flops



Analysis of Flip-Flop Operation

- Figure below shows an SR latch. Assume that we find it in this initial condition



OR gate Truth table →

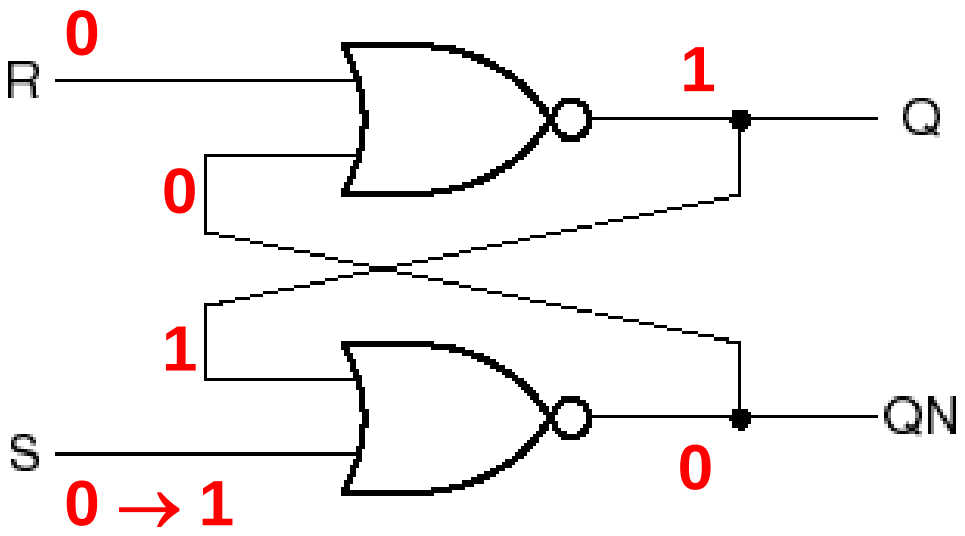
Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

RS latch

Analysis of Flip-Flop Operation

- Figure below shows an SR latch. Assume that we now raise S high (i.e. S = 1)



OR gate Truth table →

Input A	Input B	Output F
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0	1	1
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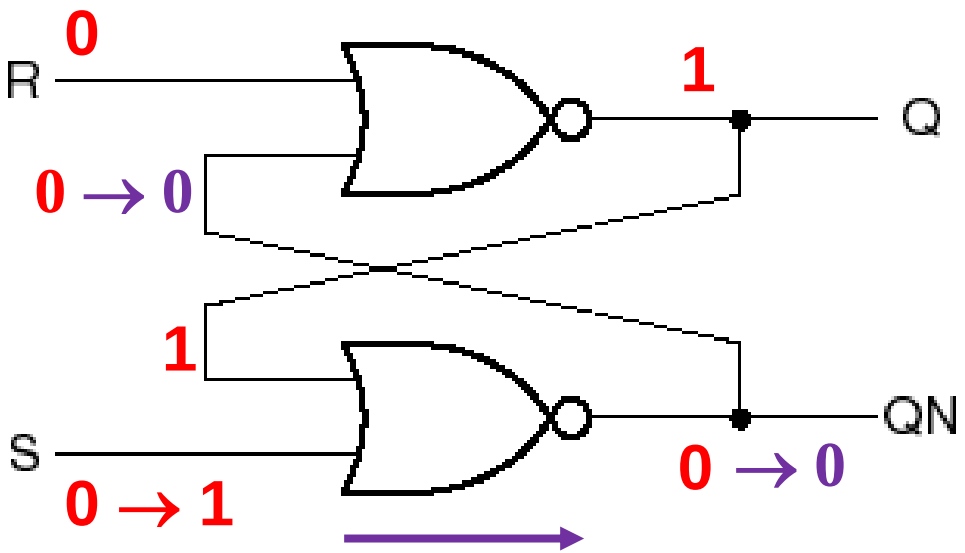

t_delay = Propagation delay through gate

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0	0	0
0	1	1
1	0	1
1	1	1

S	R	Q	QN
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RS latch

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Analysis of Flip-Flop Operation

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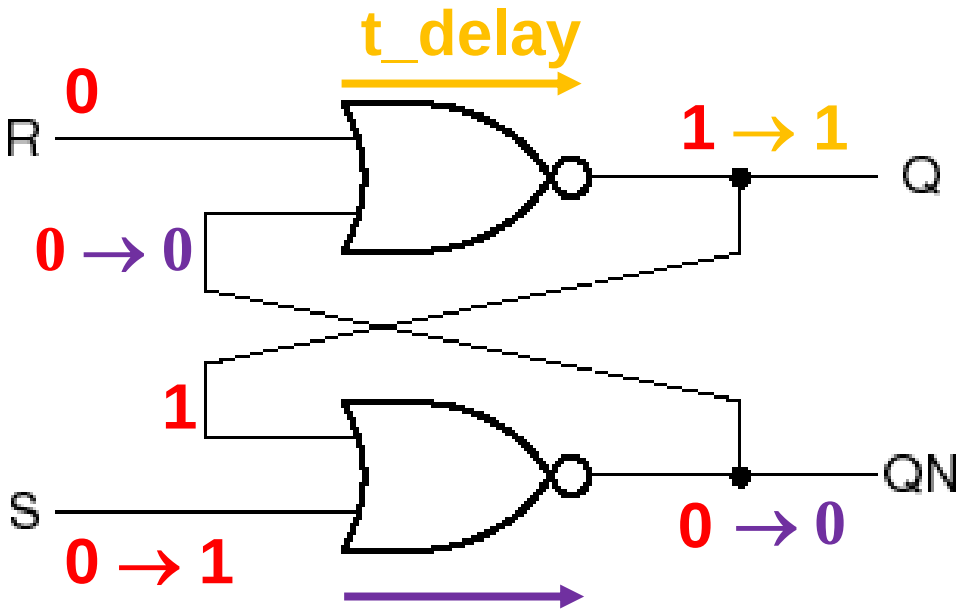

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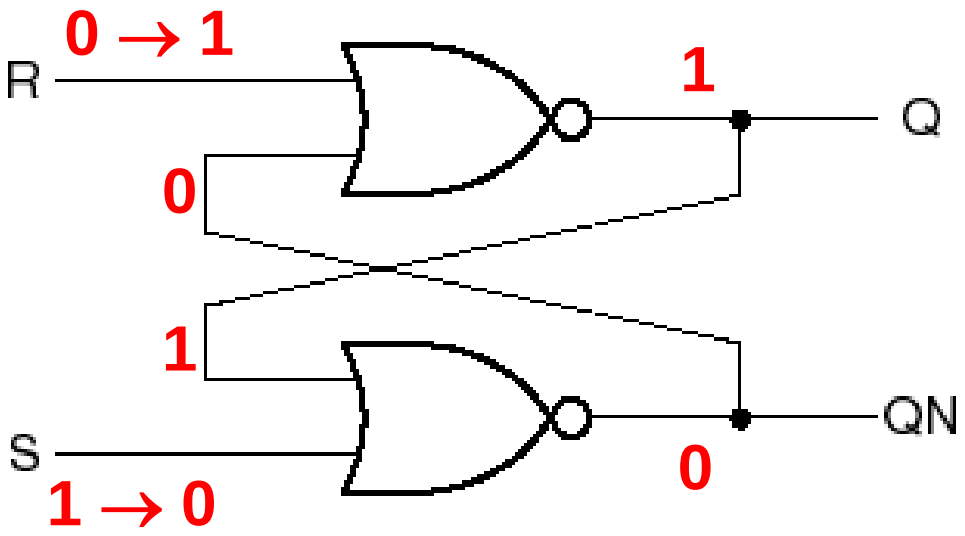
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

RS latch

Analysis of Flip-Flop Operation

- Figure below shows an SR latch. Now assume that we set S low (i.e. S = 0) and set R high (i.e. R = 1) in that order.



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RS latch

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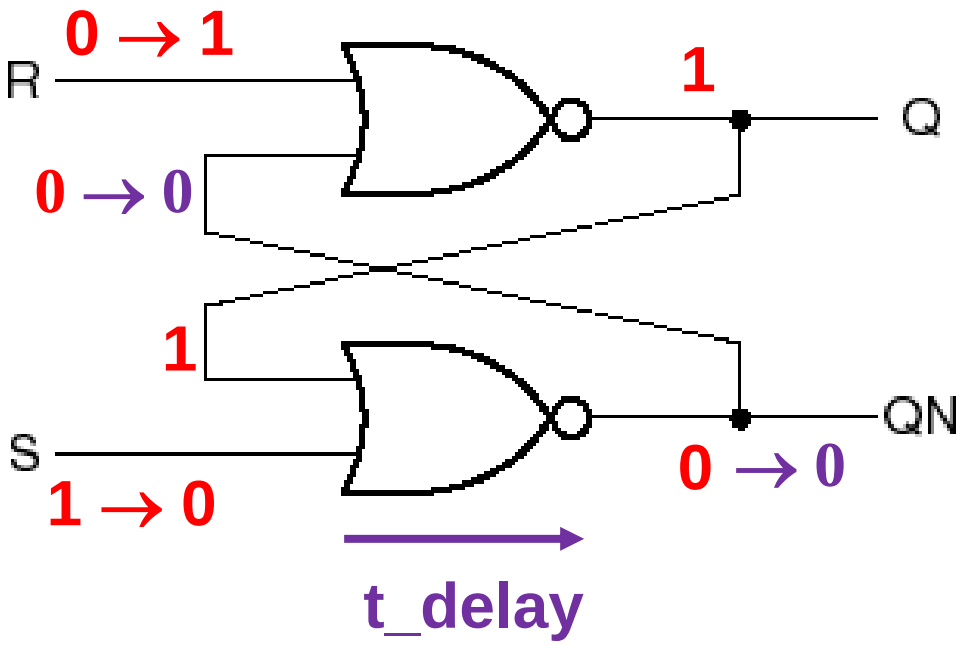

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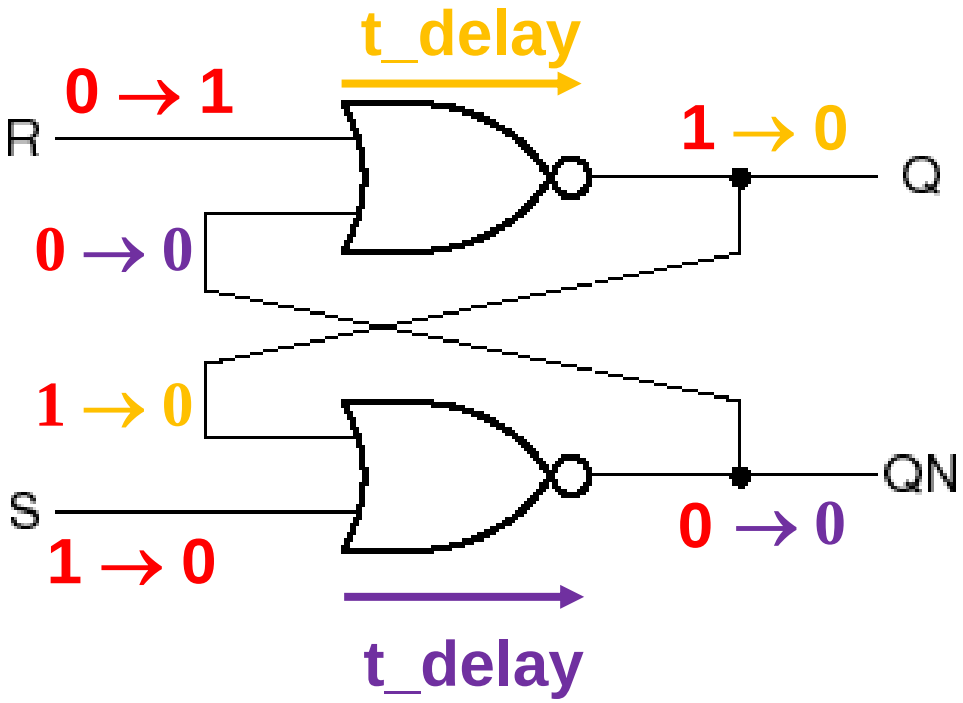

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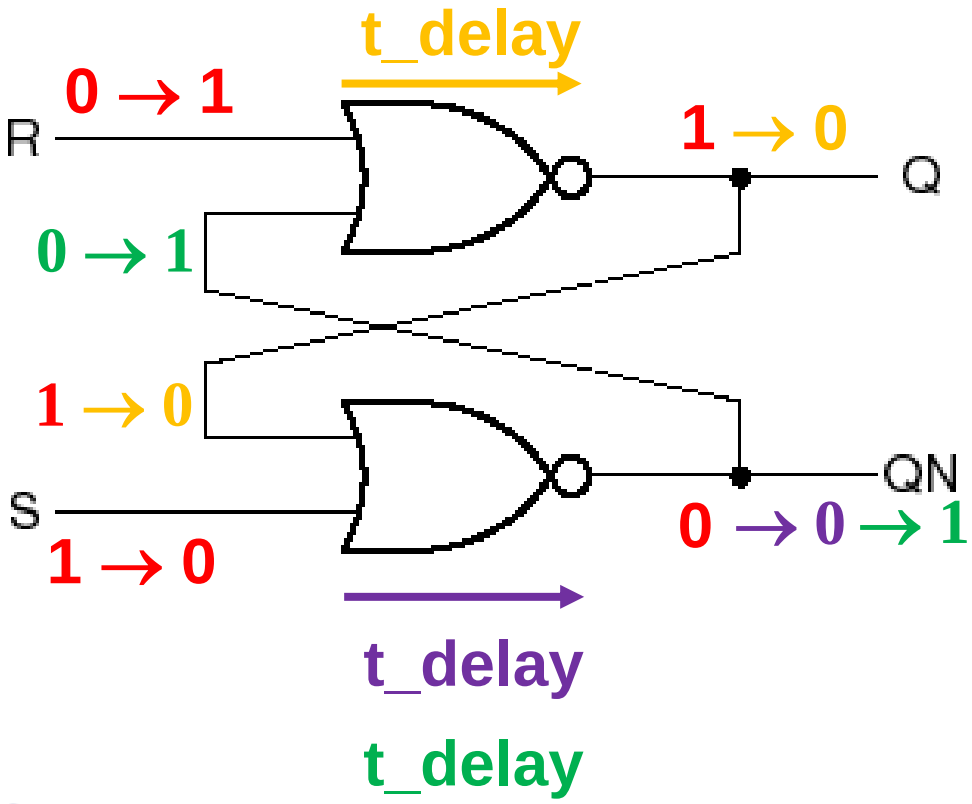

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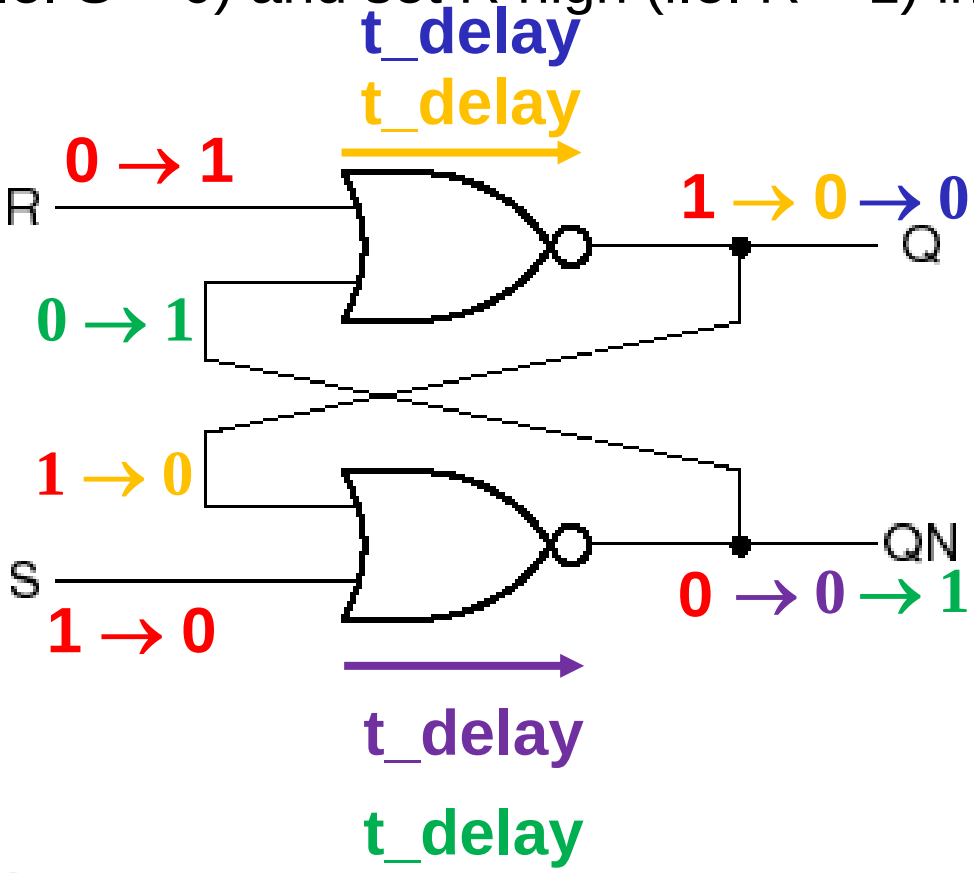

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0	0	last Q	last QN
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1	1	0	0

RS latch

Leaning Objectives for the Session

So hopefully you are now able to:

1)recognise the different types of latches and flip-flops, introduced in this module.

2)explain the differences and similarities between these different latches and flip-flops.

3)analyse different types of latch and flip-flop to understand how a change on the input will affect the outputs.