EBU4202 Digital Circuit Design 2018-19
Week 3 Tutorial Sample Solution (Updated)

1) Consider the circuit shown in Figure 1. Answer the following questions:
   a. What is the name for this type of flip-flop?
   b. Imagine that S_L now goes low. R_L remains high. Use your knowledge of the operation of gates to determine the new values of Q and QN

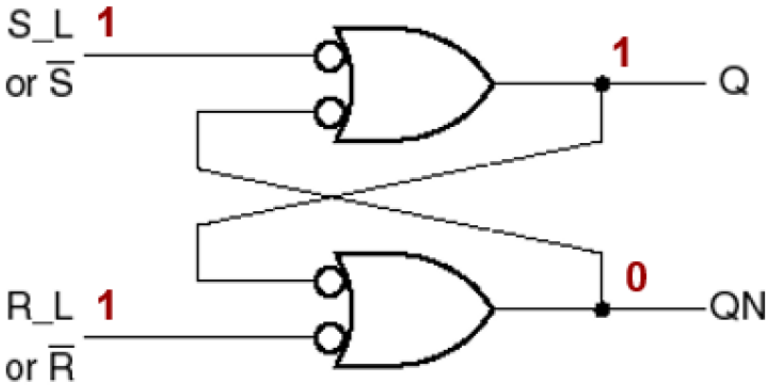


Figure 1: Circuit diagram of a flip-flop

Answer: a. S-bar R-bar latch or SR latch with NAND gates. b. Q = 1, QN = 0.

2. Consider the circuit shown in Figure 2. Answer the following questions:
   a. What is the name for this type of flip-flop?
   b. Imagine that S now goes low. R = 0 and C = 1. Use your knowledge of the operation of gates to determine the new values of Q and QN
   c. Imagine that C now goes low. S = 0 and R = 0. Use your knowledge of the operation of gates to determine the new values of Q and QN
   d. Imagine that C now goes high. S = 1 and R = 0. Use your knowledge of the operation of gates to determine the new values of Q and QN

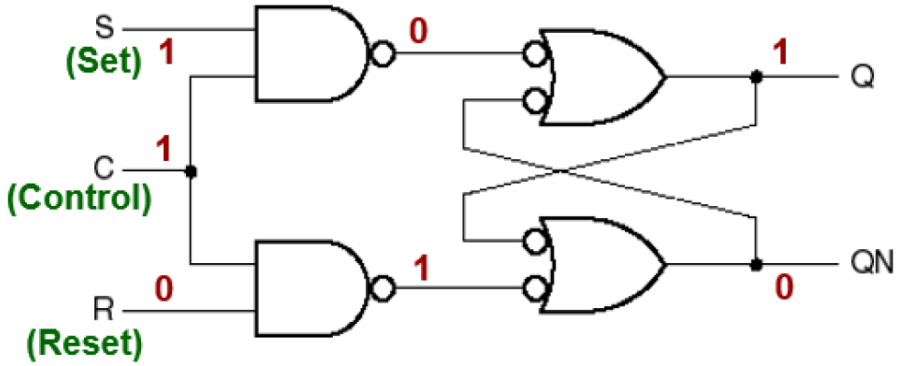


Figure 2: Circuit diagram of a flip-flop

Answer: a. SR latch with control input / with enable
b. c. d. Q = 1, QN = 0.

3. Consider the circuit shown in Figure 3. Answer the following questions:
   a. What is the name for this type of flip-flop?
   b. Imagine that C now goes high. D = 1. Use your knowledge of the operation of gates to determine the new values of Q and QN
   c. Imagine that D now goes low. C = 1. Use your knowledge of the operation of gates to determine the new values of Q and QN
   d. Imagine that C now goes low. D = 0. Use your knowledge of the operation of gates to determine the new values of Q and QN

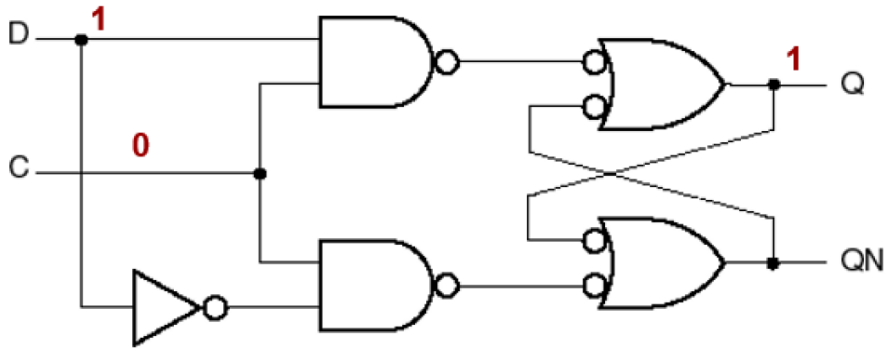
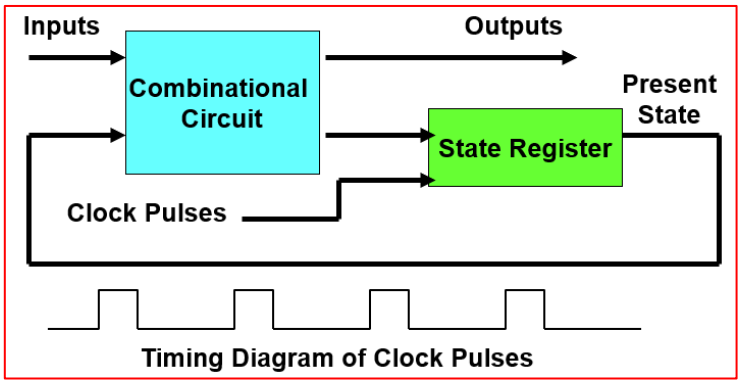


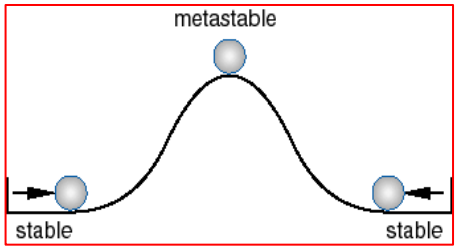
Figure 3: Circuit diagram of a flip-flop

Answer:
a. D latch with control input. b. Q = 1, c. Q = 0, d. Q = last Q (Q = 0).

4. What is a synchronous state machine?
Answer: A synchronous state machine is one in which the inputs are processed, and the outputs provided upon receipt of a clock pulse.

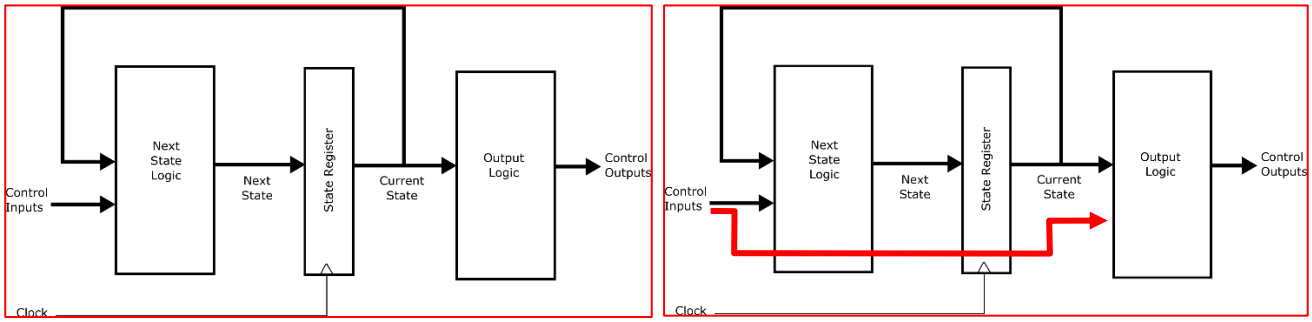


5. In the context of bistable elements and state machines, what is meant by the term "metastability"?
Ans: Metastable occurs at the point where both inputs are halfway between 0 and 1. It is not a valid state! Sequential circuits could stay in metastable forever if it wasn't for noise. Many digital designers, products, and companies have been damaged by this phenomenon.



6. Explain the difference between a Moore and Mealy machine.

Answer: In a Moore machine the output depends only on the current state.
In a Mealy machine the output depends on both its input & current state.



7. What is the minimum number of flip-flops required to store 35 states?

Answer: $2^5 = 32$, $2^6 = 64$. So we require 6 flip-flops.

8. Consider an SR latch. What is the maximum clock frequency for a circuit having a maximum delay TD? How can the circuit become unstable?

Answer:

$$F_{max} < \frac{1}{T_D}$$

The circuit will become unstable when clock > Fmax.

9. Consider the circuit shown in Figure 4. Answer the following questions.

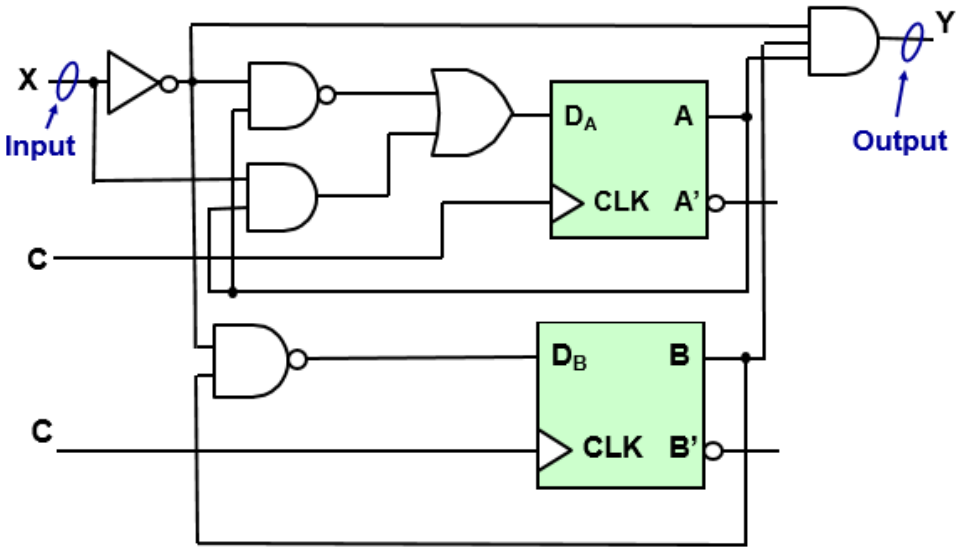


Figure 4: Circuit diagram for the first section of FSM

a. What type of FSM is depicted in Figure 1?

Answer: This is a Mealy machine because the output is a function of the current state and the input.

b. Draw-up: input, next state, and output equations for the FSM depicted in Figure 4.

Answer:

Input equations: **DA = (X'.A)' + X.A and DB = (X'.B)'**

Next state logic: **Q* = DA**

Output equation: **Z = X'.A.B**

c. Based on your answers to question 6)b) prepare the: transition table, state table, and state/output table.

Answer: Firstly, we need to derive the transition equations. This is achieved by substituting the input equations into the next state equations, so:

A* = DA = (X'.A)' + X.A

B* = DB = (X'.B)'

Inspection of these equations suggests that there is scope for simplification.

A* = (X + A') + X.A [T13]

B* = X + B' [T13]

Below we derive the transition table. [N.B. Please note that this is for your own calculation and convenience. It is not necessary for you to show this table in the exam, if you show the transition table.]

X	A	B	X + A'	X.A	A*	X + B'	B*
0	0	0	1		1	1	1
0	0	1	1		1		
0	1	0				1	1
0	1	1					
1	0	0	1		1	1	1
1	0	1	1		1	1	1
1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	1

The transition table is given below:

		X	
B	A	0	1
0	0	11	11
0	1	10	11
1	0	01	11
1	1	00	11
		B*A*	

Let: C = 00, D = 01, E = 10, F = 11
The state table is given below

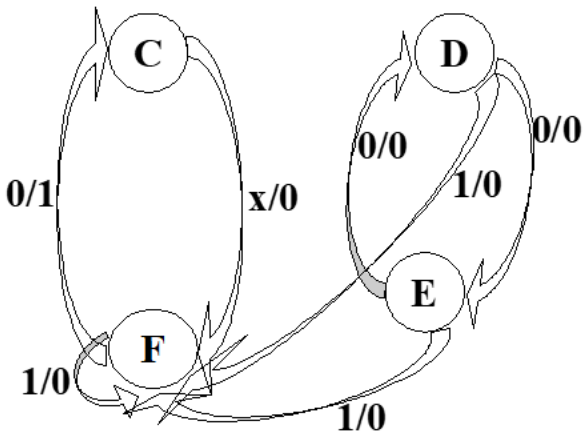
	X	
S	0	1
C	F	F
D	E	F
E	D	F
F	C	F
	S*	

Remember the output equation is: Y = (X'.A.B)

Derive the value of the output as a function of the input and the current state and form the State/Output table as below.

	X	
S	0	1
C	F,0	F,0
D	E,0	F,0
E	D,0	F,0
F	C,1	F,0
	S*,Y	

d. Finally draw the state diagram for the FSM shown in Figure 4.
Answer: The state diagram is given below

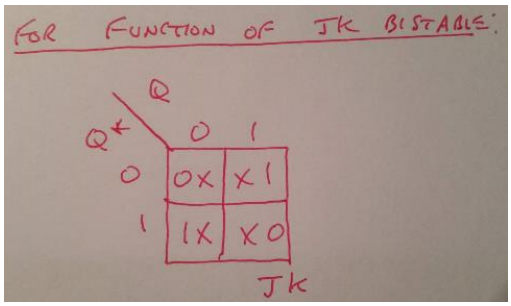


10. Design an autonomous sequential circuit, based on JK-type bistables, which generates the following sequence of states: 000, 010, 111, 101, 100 110. The transition table of JK Flip-Flop is given in Figure 5 below. Note: You must draw the circuit diagram, but there is no need to draw the state diagram.

J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q

Figure 5: Transition Table for Edge Triggered JK Flip-Flop

Answer: Recall:



Current → Next	J	K
0 → 0	0	X
0 → 1	1	X
1 → 0	X	1
1 → 1	X	0

Use the JK transition table to complete entries in the table corresponding to the inputs to J and K. [N.B.: You can skip the 'cannot happen' states in this table and put the sequence of present states as given in the question. Both methods are correct.]

Present State			Next State			JK inputs		
Q_A	Q_B	Q_C	Q_A^*	Q_B^*	Q_C^*	J_AK_A	J_BK_B	J_CK_C
0	0	0	0	1	0	0x	1x	0x
0	0	1	-	-	-	-	-	-
0	1	0	1	1	1	1x	x0	1x
0	1	1	-	-	-	-	-	-
1	0	0	1	1	0	x0	1x	0x
1	0	1	1	0	0	x0	0x	x1
1	1	0	0	0	0	x1	x1	0x
1	1	1	1	0	1	x0	x1	x0

Now draw 6 Karnaugh maps, one for each of the J and K inputs, in terms of the present states:

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	0	1	x	x
	1	-	-	x	x

$J_A = Q_B$

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	x	x	1	0
	1	-	-	0	0

$J_B = Q_B.Q_C'$

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	1	x	x	1
	1	-	-	x	0

$J_B = Q_C'$

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	x	0	1	x
	1	-	-	1	x

$K_B = Q_A$

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	0	1	0	0
	1	-	-	x	x

$J_C = Q_A'.Q_B$

Input Logic K-Map		Q_AQ_B			
		00	01	11	10
Q_C	0	x	x	x	x
	1	-	-	0	1

$K_C = Q_B'$

Draw the circuit diagram: