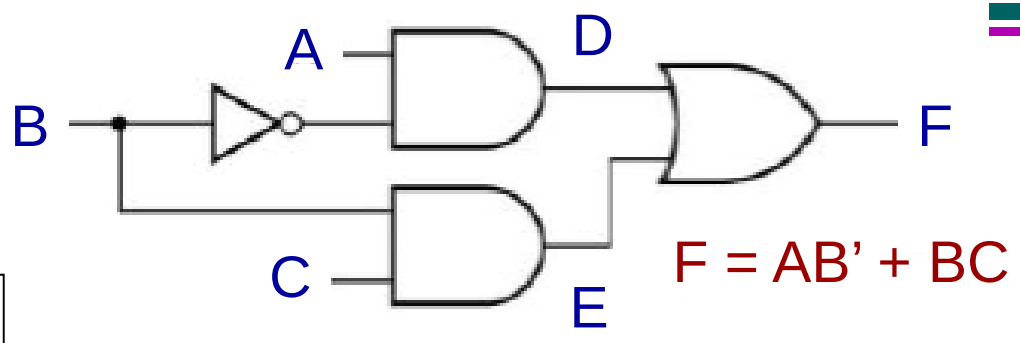
Timing Hazards and *Output Glitches* (1/3)

- *Output glitch*: A momentary unexpected output change (short pulse) when an input changes; usually caused by gate propagation delays.
- *Hazards*: A timing hazard exists in a combinational circuit when it produces an *output glitch* when one or more inputs change.
  - Static Hazards (*static-1* and *static-0*): when 1 input variable changes, the output changes momentarily before stabilising on the correct value.
    - Can usually be fixed by adding redundant logic (*Consensus Theorem – T11*).
  - Dynamic Hazards: possibility of an output changing more than once as a result of a single input change.

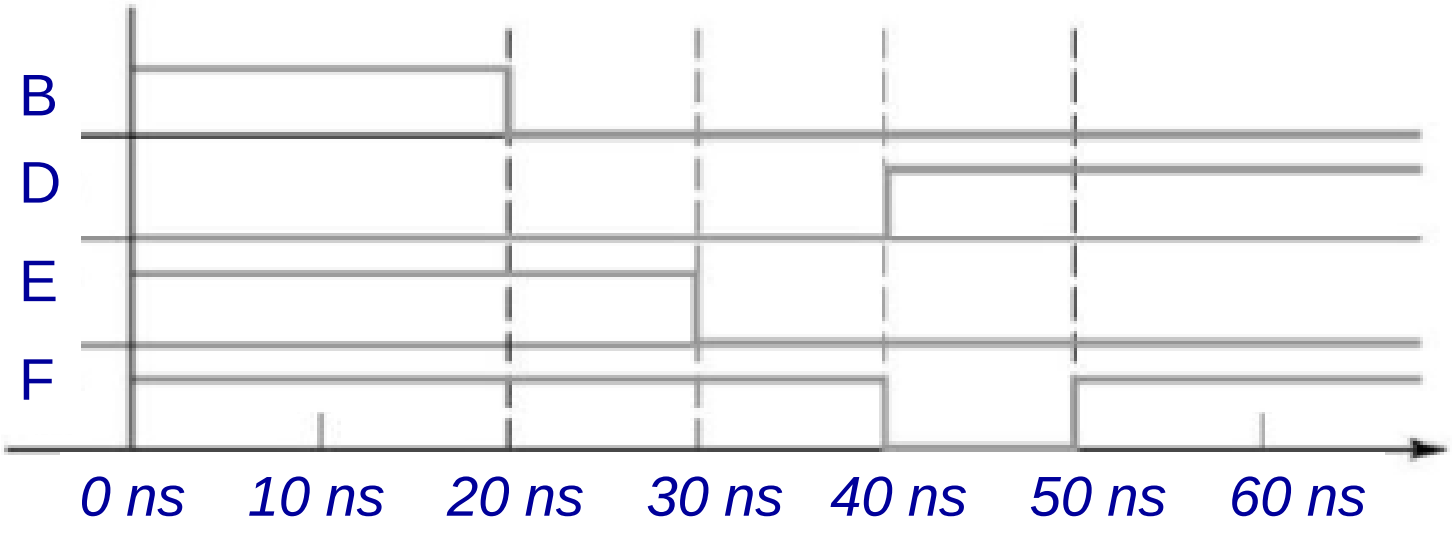
Timing Hazards and *Output Glitches* (2/3)

- Example of *static-1 hazard*:



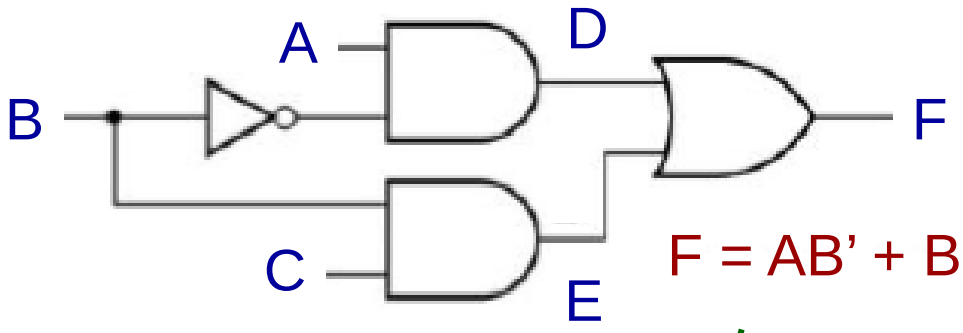
A \ BC	00	01	11	10
0	0	0	1	0
1	1	1	1	0

1-hazard



Timing Hazards and *Output Glitches* (3/3)

- Example of *static-1 hazard (cont.)*:



F = AB’ + BC

A \ BC	00	01	11	10
0	0	0	1	0
1	1	1	1	0

removing the
static-1 hazard

F = AB’ + BC + AC