EBU4202 Digital Circuit Design 2017-18

Week 2 Tutorial

1. Simplify the circuit shown in Figure 1, using a Karnaugh map. Your answer must include:

a) The initial Boolean expression for the output of the circuit (X).
b) Its expansion into a standard PoS.
c) The Karnaugh map itself, which must be clearly labelled and include all the required groupings to derive the simplified expression.

Which of the Karnaugh map's Prime Implicants are not Essential Prime Implicants? Explain.

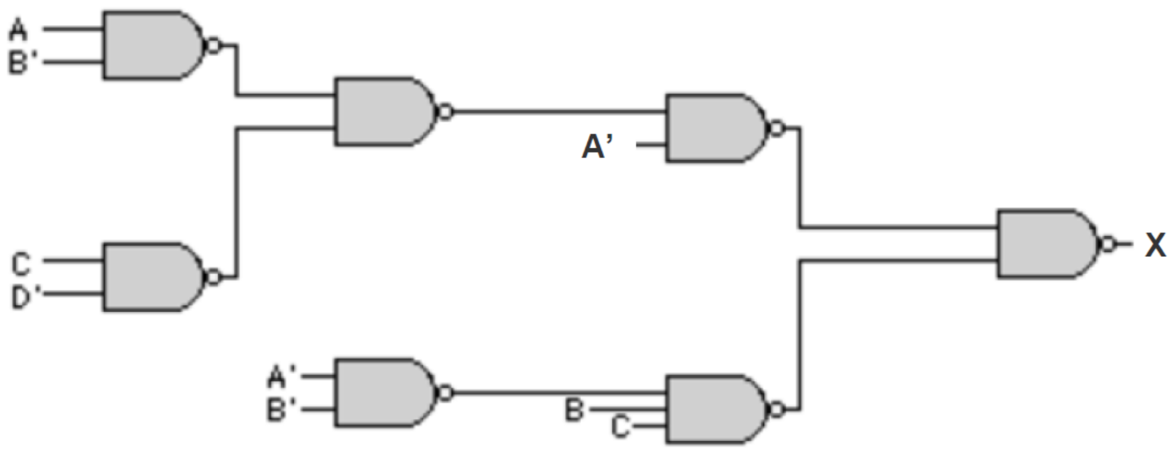

Figure 1

Answer:

From the circuit diagram in **Figure 1**, it can be seen that:
$X(A, B, C, D) = ([((AB')'.(CD')')'.A']'.[(A'B')'.BC]')'$.
We can then write this expression as,
$X(A, B, C, D) = ([((AB')'.(CD')')'.A']'.[(A'B')'.BC]')'$
$= ((AB').(CD')')'.A' + (A'B')'.BC$ -> using (T13)
$= (AB' + CD').A' + (A + B).BC$ -> using (T13)
$= A'CD' + ABC + BC$ -> using (T8), (T5'), (T6'), (T3')
$= A'CD' + BC$ -> using (T9)
We can now start expanding this expression into a standard PoS and have:
$= C.(A'D' + B)$ ->using (T8)
$= C.(A' + B).(D' + B)$ ->using (T8')
$= (C + AA').(A' + B + CC').(B + CC' + D')$ ->using (T5'), (T1)
$= (C + A).(C + A').(A' + B + C).(A' + B + C').(B + C + D').(B + C' + D')$ ->using (T8')
$= (A+BB'+C).(A'+BB'+C).(A'+B+C+DD').(A'+B+C'+DD').(AA'+B+C+D').(AA'+B+C'+D')$
->using (T5'), (T1)
$= (A+B+C).(A+B'+C).(A'+B+C).(A'+B'+C).(A'+B+C+D).(A'+B+C+D').(A'+B+C'+D).$
$(A'+B+C'+D').(A+B+C+D').(A'+B+C+D').(A+B+C'+D').(A'+B+C'+D')$ -> using (T8')

= (A+B+C+D).(A+B+C+D').(A+B'+C+D).(A+B'+C+D').(A'+B+C+D).(A'+B +C+D').
(A'+B'+C+D).(A'+B'+C+D').(A'+B+C+D).(A'+B+C+D').(A'+B+C'+D).(A'+B+C'+D').
(A+B+C+D').(A+B+C'+D').(A'+B+C'+D') -> using (T5'), (T1)
= (A+B+C+D).(A+B+C+D').(A+B'+C+D).(A+B'+C+D').(A'+B+C+D).(A'+B+C+D').
(A'+B'+C+D).(A'+B'+C+D').(A'+B+C'+D).(A'+B+C'+D').(A+B+C'+D') -> using (T3')

= $\prod$M(0000_2, 0001_2, 0100_2, 0101_2, 1000_2, 1001_2, 1100_2, 1101_2, 1010_2, 1011_2, 0011_2)

= $\prod$M(0, 1, 3, 4, 5, 8, 9, 10, 11, 12, 13) -> standard PoS

The Karnaugh map is,

AB \ CD	00	01	11	10
00	0	0	0	1
01	0	0	1	1
11	0	0	1	1
10	0	0	0	0

The simplified circuit can then be written as:
X(A, B, C, D) = C.(A' + B).(B + D')
All groupings are Essential Prime Implicants because each of them contains some *maxterms* that are not covered by other prime implicants.

2. Using a 5-variable Karnaugh Map, find the minimal PoS for the Boolean function,

G(M, N, O, P, Q) = Σm(1, 3, 5, 8, 10, 12, 16, 20, 21, 25) + d(0, 4, 7, 28, 30).

Answer:
The minimal Product of Sums for **G** is found by grouping all the cases when **G** is **0**, and reading values as *maxterms*. In this case, the minimal expression is found by including three of the "don't care" cases marked with an **X**. Therefore,

NO \ PQ	00	01	11	10
00	X	1	1	0
01	X	1	X	0
11	1	0	0	0
10	1	0	0	1

M = 0

NO \ PQ	00	01	11	10
00	1	0	0	0
01	1	1	0	0
11	X	0	0	X
10	0	1	0	0

M = 1

Therefore, the simplest PoS expression for **G** is
G(M,N,O,P,Q) = (M+N'+Q')(O'+P')(N+P'+Q)(M'+N'+Q)(M'+P')(M'+N'+O')(M'+N+O+Q').

3. Design a combinational circuit with three inputs **x**, **y** and **z**, and three outputs **A**, **B** and **C**. When the binary input is a value below ***5***, the binary output is one greater than the input; otherwise, the binary output is one less than the input. Your answer must include all the required steps i.e., the Truth Table, the Karnaugh maps and the circuit diagram for a minimum cost solution (in terms of the number of logic gates required), i.e. using least number of logic gates.

Answer:
Let us consider the following: **xyz** represents the circuit's input value, where **x** is the MSB; **ABC** is the circuit's output with **A** being the MSB. Therefore e.g., when xyz = 000_2, then ABC = 001_2; when xyz = 010_2, then ABC = 011_2; when xyz = 100_2, then ABC = 011_2 and so on.

The Truth Table is

Inputs			Outputs		
x	**y**	**z**	**A**	**B**	**C**
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

The outputs can then be written as *sums of minterms*,
A = Σm(3, 4, 5, 6, 7); B = Σm(1, 2, 7); C = Σm(0, 2, 4, 6).

We will use Karnaugh maps to minimise the representation of each output **A**, **B** and **C**:

x \ **yz**	**00**	**01**	**11**	**10**
0	0	0	1	0
1	1	1	1	1

So A = Σm(3, 4, 5, 6, 7) = x + yz -> 2 gates required

x \ yz	00	01	11	10
0	0	1	0	1
1	0	0	1	0

So B = $\Sigma m(1, 2, 7) = x'y'z + xyz + x'yz'$
$= (x'y' + xy)z + x'yz'$ -> using (T8)
$= (x \oplus y)'z + (x + z)'y$ -> 5 gates required

x \ yz	00	01	11	10
0	1	0	0	1
1	1	0	0	1

So C = $\Sigma m(0, 2, 4, 6) = z'$ -> 1 gate required
The circuit diagram is then,