

## **SOLUTIONS**

### **EBU4202 Mock Class Test/Tutorial 22 March 2019 (E-Commerce)/12 April (IoT)**

#### **Question 1**

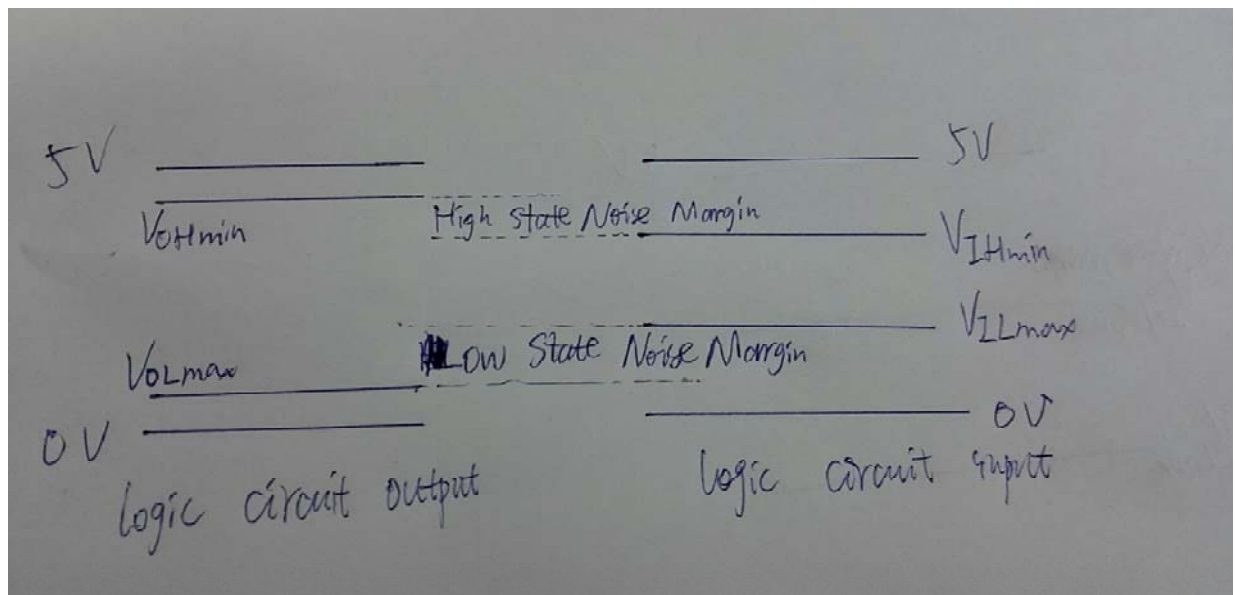
- i) In the context of digital circuit devices, briefly explain the meaning of each of the terms “fan-out”, “power dissipation” and “propagation delay”. [3 marks]
- ii) Using a suitable diagram, explain what are  $V_{ILmax}$ ,  $V_{IHmin}$ ,  $V_{OLmax}$  and  $V_{OHmin}$ , what is meant by the term “Low Level Noise Margin” and “High Level Noise Margin”. [6 marks]
- iii) State what is meant by the terms “Positive Logic” and “Negative Logic”. [2 marks]

#### **Answers:**

i) fan-out: the number of device inputs that a device output can be connected to without the voltage being outside the range for a valid logic level [1 mark]

Power dissipation: the power consumed from the power supply by the logic device [1 mark]

Propagation delay: the time taken from a change of logic level at the input of a logic device to a change at the output of the device [1 mark]



ii)

[2 mark] for the diagram

$V_{ILmax}$  denotes the maximum input voltage that can be recognized as a low state; [1 mark]

$V_{IHmin}$  denotes the minimum input voltage that can be recognized as a high state; [1 mark]

$V_{OLmax}$  denotes the maximum output voltage in the low state; [1 mark]

$V_{OHmin}$  denotes the minimum output voltage in the high state; [1 mark]

The low level noise margin is the difference between  $V_{OLmax}$  and  $V_{ILmax}$  (or  $V_{OLmax} - V_{ILmax}$ ) [1 mark]

The high level noise margin is the difference between  $V_{OHmin}$  and  $V_{IHmin}$  (or  $V_{IHmin} - V_{OHmin}$ ) [1 mark]

iii) In positive logic, low is 0 and high is 1. In negative logic, low is 1 and high is 0. [2 mark]

## Question 2

Let ABCD represent a 4 bit BCD number.

i) Draw the truth table for a combinational logic circuit that produces a '1' output when the input ABCD is either a prime number or a perfect square. The input combination 0000 is not allowed to occur. (A prime number is a number that can only be divided by itself or 1.) [5 marks]

ii) Draw the Karnaugh map for this circuit and show the prime implicants. [5 marks]

iii) From the Karnaugh map, determine a minimal expression for the output expressed in SoP form. [2 marks]

iv) Using a truth table, show the state of the output for each of the "can't happen" input states as a result of the minimisation. [1 mark]

v) Draw the circuit diagram for the minimal SoP implementation of the function.

[2 marks]

vi) Convert the logic function to all NAND form and draw the circuit diagram.

[4 marks]

## Answers

i) BCD is the range 0 to 9 where 10 to F do not occur [1 mark]

Prime numbers are 1, 2, 3, 5, 7 [1 mark]

Perfect squares are 1, 4, 9 [1 mark]

The truth table is:

A	B	C	D	F(A,B,C,D)
0	0	0	0	X
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

[2 marks for correct truth table]

ii) The Karnaugh map is:

AB	00	01	11	10
CD				
00	X	1	X	0
01	1	1	X	1
11	1	1	X	X
10	1	0	X	X

[5 marks: 2 marks for correct map, 1 for each correct prime implicant]

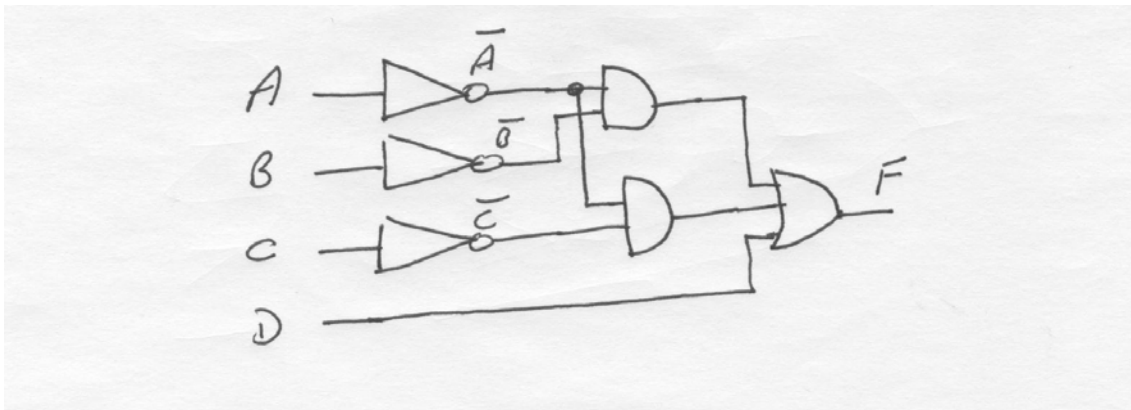
iii) A minimal expression is:  $F = A'.C' + A'.B' + D$  [2 marks]

iv) The resulting output states are:

A	B	C	D	F(A,B,C,D)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

[1 mark]

v) The circuit diagram is:



[2 marks]

vi) Using De Morgan's Theorem, the all NAND form is:

$$F = [(A'.C')'.(A'.B')'.D']' \quad [2 \text{ marks}]$$

Circuit diagram:

[2 marks]

