Overview: Digital Circuits

* **Logic Signals**
* **Logic Families**
* **IC Fabrication**
* **CMOS Logic**

Chapters 1 & 3 – "Digital Design: Principles and Practices" book

***Note**: Some pictures in this topic were extracted from the web.*

Logic Signals & Gates

- Logical signals are often called *low* and *high*, to refer to the values *0* and *1* (not necessarily in this order!).

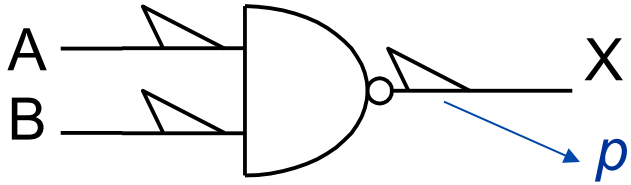
- Also, *low* often corresponds to algebraically lower voltages while *high* corresponds to higher voltages.

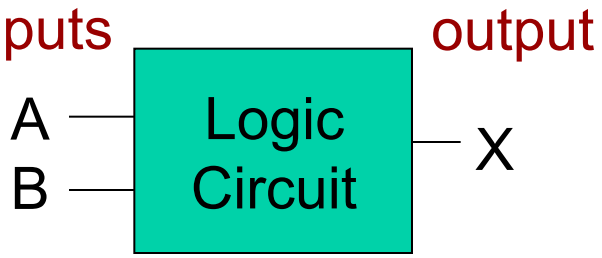
- Types of logic:
  - *Positive Logic* assigns *0* to *low* and *1* to *high*.
  - *Negative Logic* assigns *0* to *high* and *1* to *low*.

The most natural type.

Not often used.

Positive and Negative Logic





- **Truth tables**:

Negative Positive

A	B	X
1	1	0
1	0	1
0	1	1
0	0	1

A	B	X
0 V	0 V	5 V
0 V	5 V	0 V
5 V	0 V	0 V
5 V	5 V	0 V

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Logic Value	Voltage Level
0	L
1	H

Logic Value	Voltage Level
0	H
1	L

Signal Variation

- A binary value represents a wide range of voltages, so digital signals are highly immune to voltage variation!

- **Example** *(typical ranges)*:
  - For a CMOS gate, its *high* ranges from *3.5* V to *5.0* V while its *low* ranges from *0* V to *1.5* V.

- **Note**: *CMOS* means Complementary MOS, and *MOS* (short for Metal-Oxide Semiconductor Field-Effect) is a type of transistor with low power consumption and high level of integration.

Operation of Logic Gates

- "Ideal" Logic Gates:
  - *Input* and *output voltages* are at either the high or the low value specified for the *logic family*.
  - *Inputs* draw no current from whatever drives them, and *outputs* can supply as much current as necessary for whatever follows.
  - *Any change to an input* will immediately be *reflected on the output*.

Real logic gates operate under several restrictions!

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* **Logic Signals**
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* **CMOS Logic**

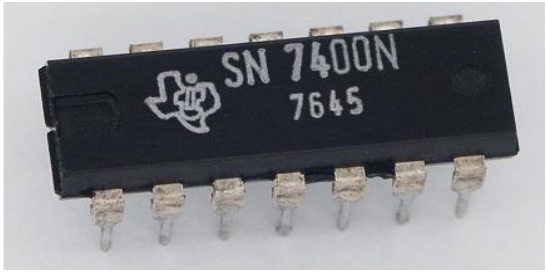
More *detailed information* at (especially important if you are taking the 3rd year courses EBU5335 and EBU5475): http://www.opamp-electronics.com/tutorials/digital_theory_ch_003.htm.

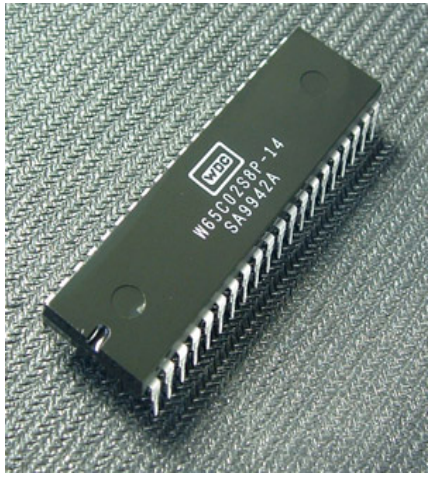
Chapters 1 & 3 – "Digital Design: Principles and Practices" book

Logic Families

There are *other logic families* and *sub-families* (but *out of scope* here).

- **Logic family**: Collection of different IC chips that have similar input, output, and internal circuit characteristics, but perform different logic functions.
  - Thus, chips from different logic families may not be compatible.
- Two **most common logic families**:
  - *Transistor-Transistor Logic* (TTL), and
  - *Complementary Metal-Oxide Semiconductor field effect transistor* (CMOS).
- **Differences between TTL and CMOS**: materials, fabrication methods, and electrical behaviours.





Logic Levels: TTL & CMOS

- **CMOS** (*Complementary MOS*): built on MOS transistors.
  - *(*) Logic values*:

    0 → voltages: *0-1.5* Volts; ***1*** → voltages: *3.5-5.0* Volts.

  - Used by most large-scale ICs (e.g., microprocessors and memory).

(*) Typical values only.

- **TTL** (*Transistor-Transistor Logic*): built on bipolar junction transistors.
  - *(*) Logic values*:

    0 → voltages: *0-0.8* Volts; ***1*** → voltages: *2.0-5.0* Volts.

  - Once used for small to medium-scale applications, now usually replaced by CMOS devices. TTL components can still be found in university labs.

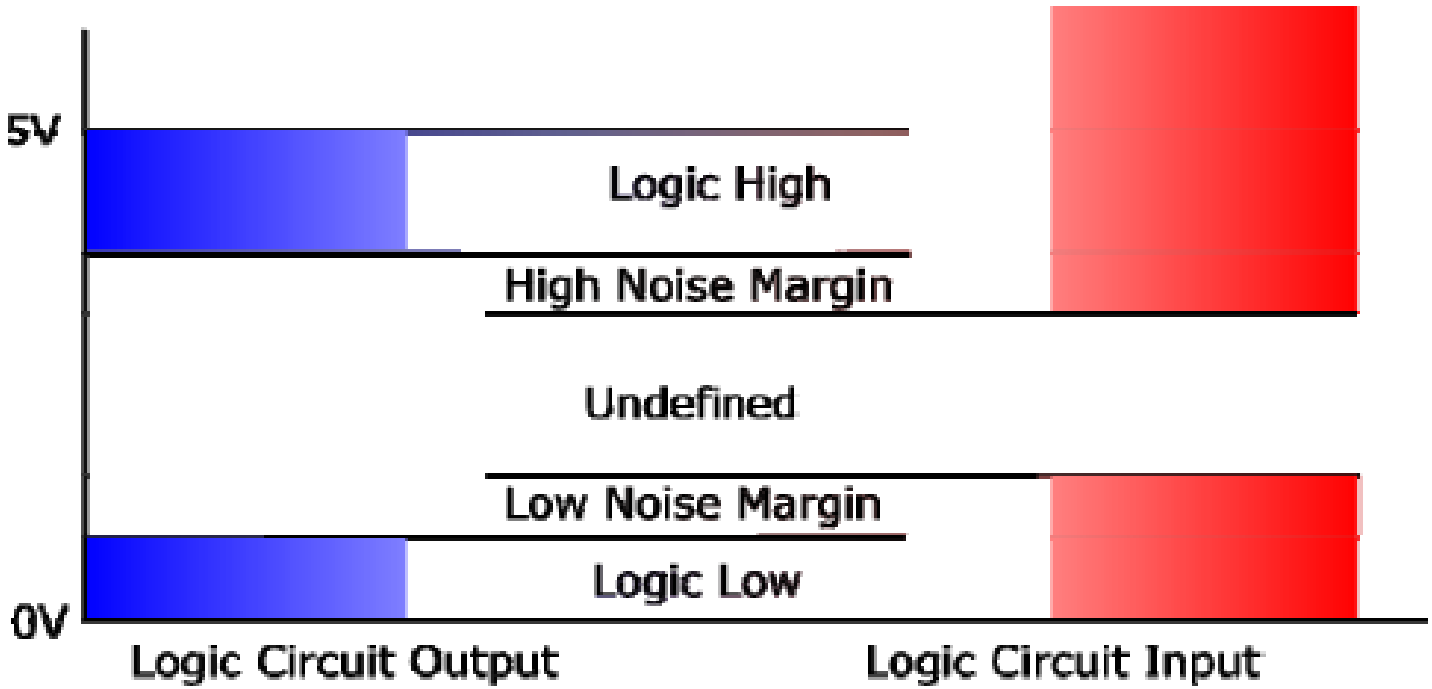
Logic Family Parameters

- Characteristics of digital logic families are compared by analysing the circuit of the basic gate in each family, using *parameters*:
  - Fan-out, Fan-in (measured in *number of inputs*)
  - Power Dissipation (measured in *watts*): *power consumed by the gate* that must be available from the power supply.
  - Propagation Delay (measured in *seconds*)
  - Noise margin (measured in *volts*)

	T_p (ns)	***P*** (mW)	***Noise Margin*** (mV)	***Fan-out***
TTL	9	10	400 (OH); 400 (OL)	10
CMOS	18	0.01 (static)	1050 (OH); 1340 (OL)	≤ 50

T_p: propagation delay
P: power dissipation per gate

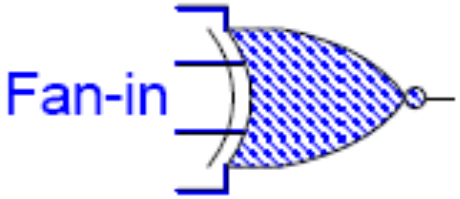
Logic Levels



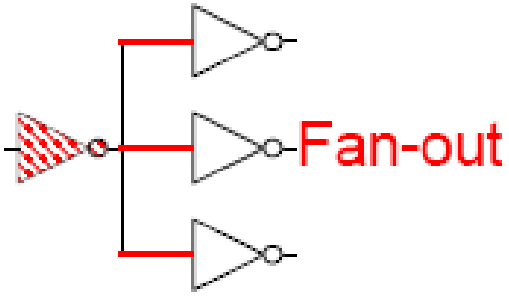
- *Different logic families* may have different logic levels.
- Noise Margin: *maximum external noise voltage* that can be added to an input signal *without causing an undesirable change in the circuit output*.

Fan-in & Fan-out: Definition

- ***Fan-in*** refers to the number of inputs a gate can have in a particular logic family.
  - In other words, it's the number of inputs that a gate can practically have.



- ***Fan-out*** refers to the maximum number of logic inputs that an output can drive reliably.
  - It depends not only on the *characteristics of the output*, but also depends on the *characteristics of the input*.



Fan-in & Fan-out: Characteristics

- **Fan-in**:
  - Too many inputs for a gate may lead to significant delay.
  - The number of inputs on most CMOS gates is limited to between *4* and *6*.
  - Gates with a large number of inputs can be made faster and efficient by cascading gates with fewer inputs.
- **Fan-out**:
  - If too much fan-out is connected to an output, the DC noise margin may not be adequate.
  - Fan-out may also affect speed.

Impedance (*aka* resistance for very simple circuits)

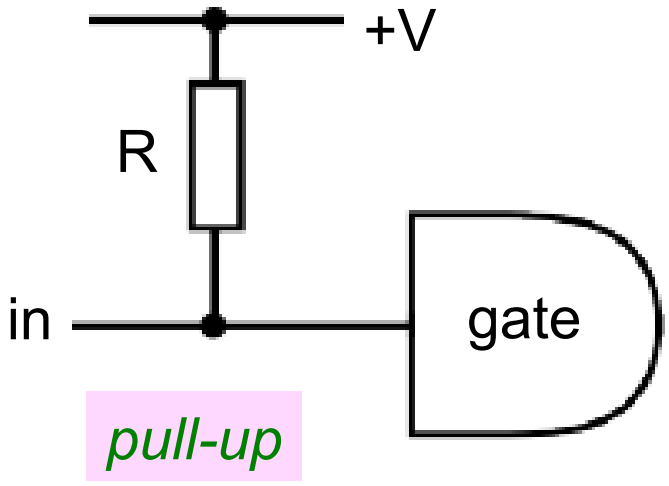
- Impedance: measure of the *overall opposition* of a circuit to current.
- Input impedance (as "seen" by anything connected to the input of a circuit) should be *at least 10 times higher* than the output impedance of the circuit supplying a signal to the input.
  - This is to avoid the input *overloading* the source of the signal and reducing the strength (voltage) of the signal by a substantial amount.
- If an output impedance is *too high*, it will be unable to supply a sufficiently strong signal to the load because most of the signal's voltage will be "lost" inside the circuit driving current through the output impedance; the load could be e.g., the input impedance of another circuit.

Ideal values for impedance (i.e., what is assumed when designing circuits at gate and system level of abstraction):

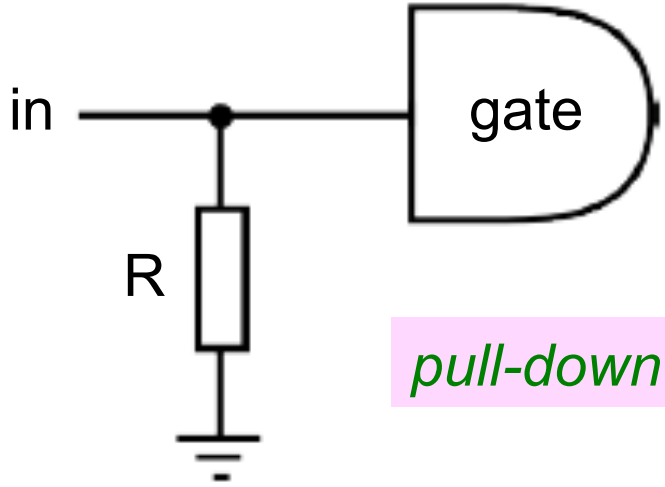
$$Z_{in} = \infty \quad // \quad Z_{out} = 0.$$

Unused Inputs

- Digital devices can only deal with *signals* that have *well defined logic levels* (i.e., a *0* or a *1*).
- *Floating signals* can cause unpredictable behaviour in circuits.
- *Pull-up* and *pull-down resistors*: ensure that given no other input, a circuit assumes a default value (i.e., a *1* or a *0*, respectively).



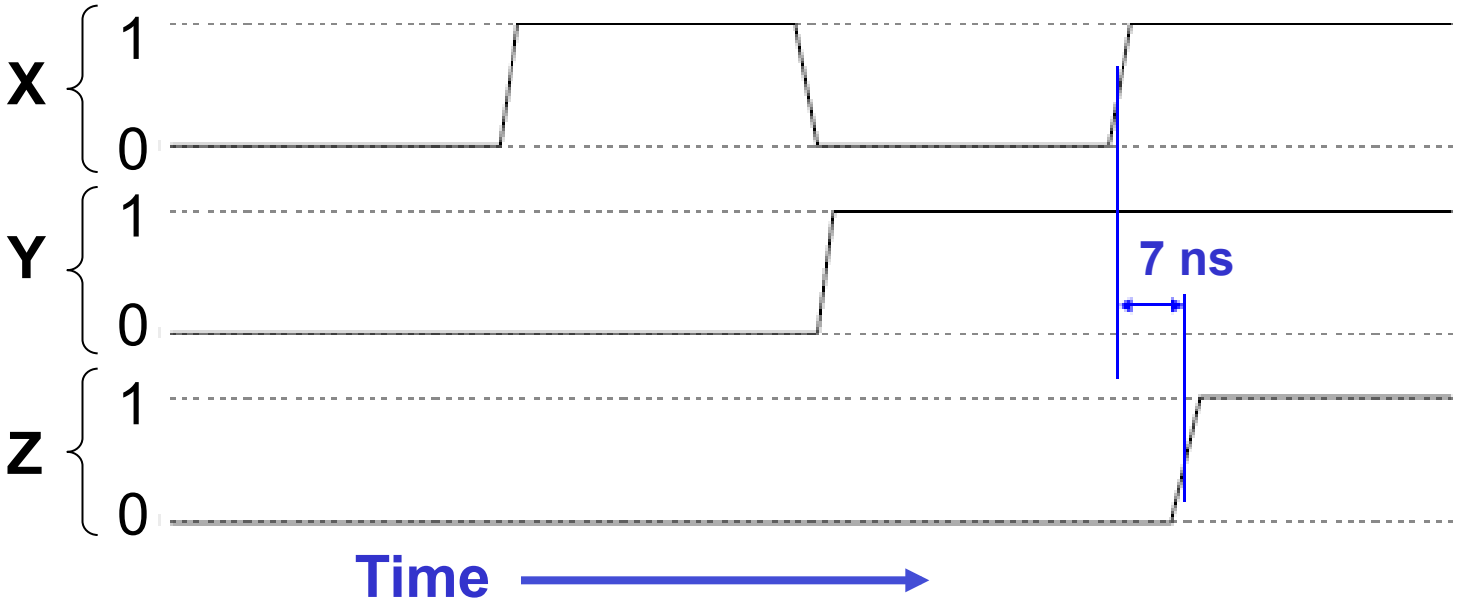
pull-up



pull-down

Timing Diagrams

- Dimensions on which logic circuits work: truth tables & time.
- Timing diagrams: describe how a circuit behaves in response to varying input signals over time.
  - Show that signals do not change between *0* and *1* instantaneously, and there is a transition period between input and output.



Speed, Propagation Delay & Data Sheets

- Speed limitations:
  - *Delay encountered by a signal* going through a single gate.
  - *Number of levels* in the circuit.
- Propagation delay: the amount of time needed for a change in the input signal to produce a change in the output signal.
- Data sheet of a chip (or digital device): specifies the device's logical and electrical characteristics, as well as operating conditions.

To ensure the device works properly, the operating conditions must be satisfied.

Example: Data Sheet

Note: Taken from course textbook (page 98).

Table 3-3 Manufacturer's data sheet for a typical CMOS device, a 54/74HC00 quad NAND gate.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:

Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\,V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0\,V$		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	−0.7	−1.2	V
I_{OS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ μA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ μA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	μA

Overview: Digital Circuits

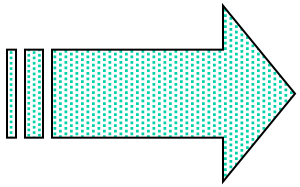
* Logic Signals
* Logic Families
* IC Fabrication → Self-study topic (*)
* CMOS Logic

Chapters 1 & 3 – "Digital Design: Principles and Practices" book

(*) This is complemented by a video shown in class.

ICs: back to basics

- **Integrated Circuits** (ICs) are made of silicon, which in turn is created from sand. However, the manufacturing process of ICs is extremely complex and expensive.



Silicon and ICs

- ***Silicon*** is a semiconductor. This means that it can be altered to act as either a conductor, allowing electricity to flow, or as an insulator preventing the flow of electricity.
- **Silicon chips**:
  - have a surface area of similar dimensions to a thumb nail (or even smaller);
  - are 3-dimensional structures composed of microscopically thin layers (perhaps as many as 20) of insulating and conducting material on top of the silicon.

Silicon Ingots: Definition

- Semiconductor devices are produced from *silicon ingots*.
- ***Silicon ingots*** is the name given to silicon in a single crystal form.
- ***Ingots*** are produced in a number of ways, but essentially, high purity silicon is melted down and then formed into ***cylindrical rods*** as shown below.

Silicon ingots are made to the customer's specifications (usual diameter ~15-20cm).

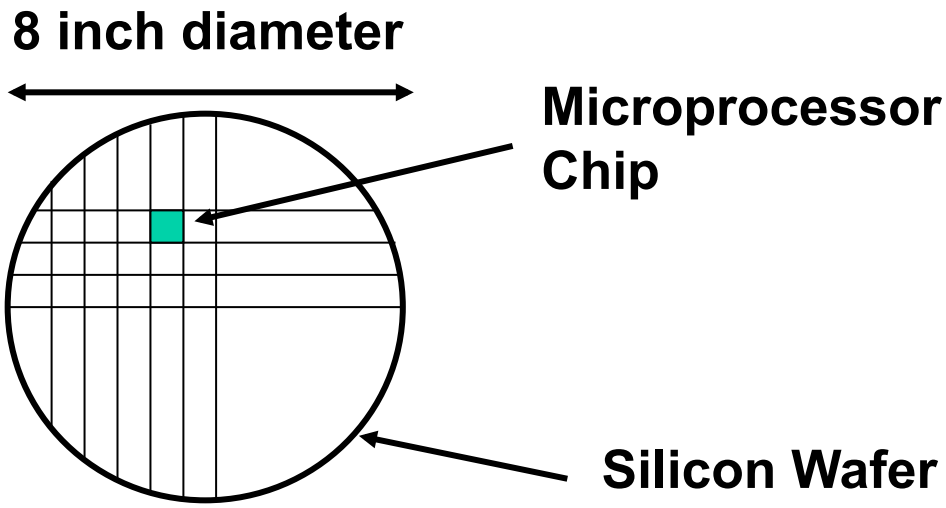
Wafers *versus* Silicon Ingots

- **Rods** (or *silicon ingots*) are sliced into very thin *wafers*, using special diamond cutting technology.
- **Wafers**:
  - are treated (i.e., polished and chemically treated) to remove any roughness and/or damage;
  - are very thin (usually only *0.06mm* in width).
- **ICs** are built from the *wafers*.

Silicon ingot and the *wafers* that are cut from the ingot.

Creating ICs on Wafers

- Wafers are divided up so that many chips can be printed on them.



Finished wafers.

- How are all connectors, resistors, transistors and capacitors added to the wafer to make up an IC?
  - New (very thin) layers are added to the original wafer.
  - Each additional layer defines more and more of the completed IC.

The Die

- **Wafers** *versus* **chips**: One wafer can yield hundreds of finished chips, that are cut individually using a diamond saw.
- **Die**: The industry term for individual chips.
- ***Die size*** varies depending on the chip:
  - The larger the individual chip's die size, the greater the waste of silicon area when a fault arises on a chip.
  - ***Example***: If a wafer is divided to make 40 chips and 10 random faults occur, then there'll be a wastage of 25%. ***But*** if the wafer is divided to make 200 chips and 10 random faults occur, then wastage will be only 5%.

Wafer Yield

- **Yield of the wafer**: The percentage of functioning chips.
- Yields vary substantially depending on:
  - complexity of the device being produced;
  - feature size used.
- **Acceptable yield values**:
  - any yield value of 50% is reported;
  - yield values of 80% to 90% are regarded as very good.

Producing good yield values is important, since a single short circuit, caused by two wires touching in a *30*+ *million* transistor chip, is enough to cause chip failure!

Feature Size

- **Feature Size**: Refers to the size of a transistor or to the width of the wires connecting transistors on the chip. ***Examples***:
  - One micron (i.e., 1/1000 of a millimetre) ***used to be*** a common feature size.
  - State of the art chips are now using sub-micron feature sizes between 0.25 (in 1997) to 0.13 (in 2001) (i.e., between 250 and 130 nanometres).

The smaller the feature size, the more transistors there are available on a given chip area.

Smaller Feature Size (1/2)

- **Advantages**:
  - A greater number of transistors per die means a smaller die size, and this means more chips per wafer.
  - A microprocessor using a smaller feature size than its predecessor will be smaller, run faster and use less power.
  - Since more of these smaller chips can be obtained from a single wafer, each chip will cost less (this is one of the reasons for cheaper processor chips).
  - A reduced feature size makes it possible to build more complex microprocessors, e.g., the Pentium III which uses around 30 million transistors.

Smaller Feature Size (2/2)

- **Disadvantages**:
  - A reduced feature size means an increase in the density of transistors per chip area, and this has led to power consumption and power dissipation problems.
    - ***Example***:
      - CPUs typically dissipate about the same heat per square inch as an electric cooker generates (and sometimes require cooling fans or water cooling systems).

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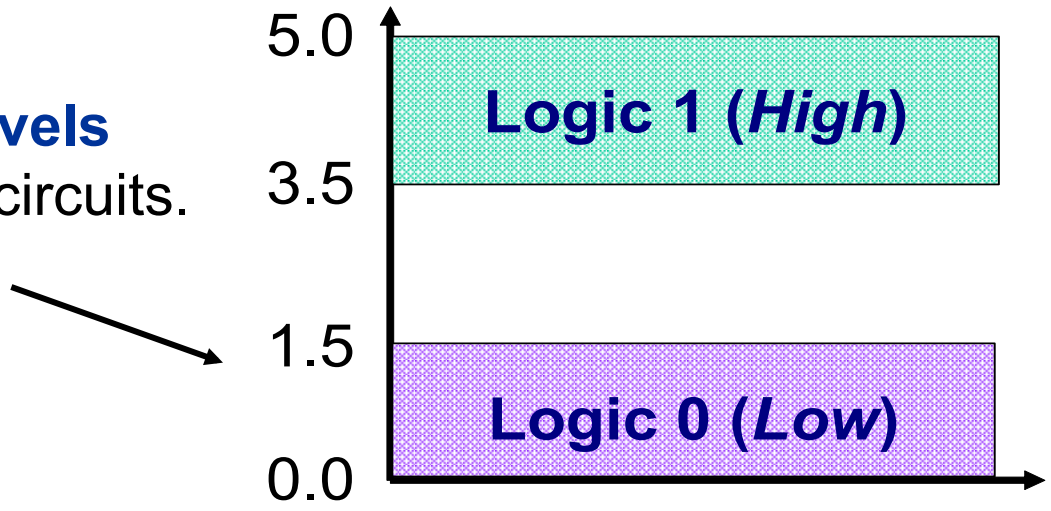
* IC Fabrication
* CMOS Logic

Chapters 1 & 3 – "Digital Design: Principles and Practices" book

CMOS Logic

- As seen before:
  - The **building blocks** in CMOS are MOS transistors.
  - CMOS operates from a *5* volts power supply (*usually!*).
- The ***Voltage-logic connection*** is interpreted as follows:

Typical **Logic levels** for CMOS logic circuits.



MOS Transistors

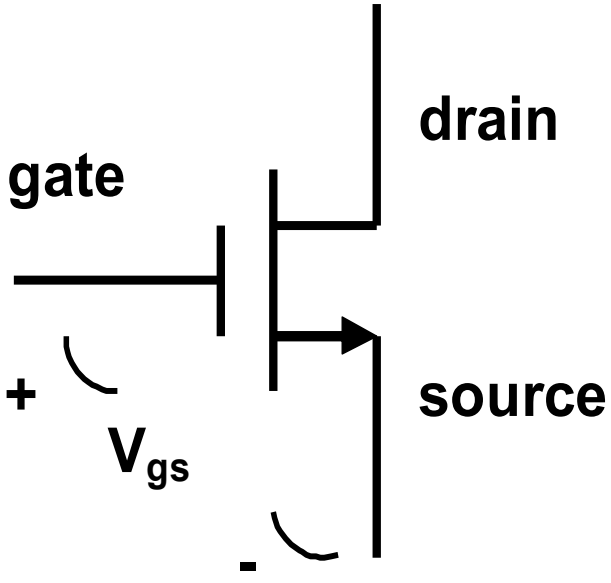
- **MOS transistor**: a 3-terminal device.
  - The voltage applied to one terminal controls the resistance between the remaining two terminals.
  - The **three terminals** are:
    - *Gate;*
    - *Source;*
    - *Drain.*

The ***names*** *refer to the type of semiconductor material* used for the resistance-controlled terminals.

- **Types of MOS transistors**:
  - *n-channel*
  - *p-channel*

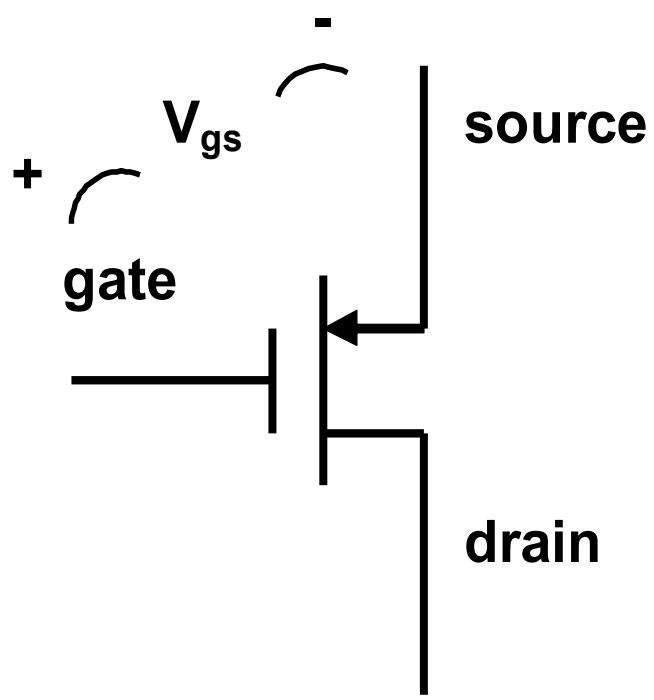
N-Channel MOS (NMOS) Transistor

- ***Drain*** on NMOS: usually is at a *higher* voltage than the ***source***.
- **Notation**:
  - V_{gs} = voltage from ***gate*** to ***source***
  - R_{ds} = resistance from ***drain*** to ***source***
- **How it works**:
  - $V_{gs} \geq 0$ (usually).
  - If $V_{gs} = 0$, then R_{ds} will be very high (so, *no output*).
  - If voltage on the ***gate*** is increased (i.e., increase on V_{gs}), then R_{ds} decreases (so, *there is an output*).



P-Channel MOS (PMOS) Transistor

- ***PMOS*** operation similar to ***NMOS***, but ***drain*** is usually at a *lower* voltage than the ***source***.
- **Notation**:
  - V_{gs} = voltage from ***source*** to ***gate***
  - R_{ds} = resistance from ***source*** to ***drain***
- **How it works**:
  - $V_{gs} \leq 0$ (usually).
  - If $V_{gs} = 0$, then R_{ds} will be very high (so, *no output*).
  - If voltage on the ***gate*** is decreased (i.e., decrease on V_{gs}), then R_{ds} decreases (so, *there is an output*).

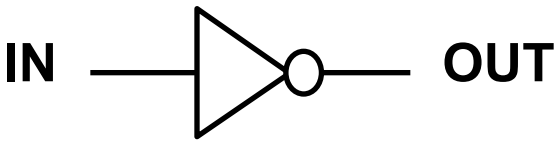


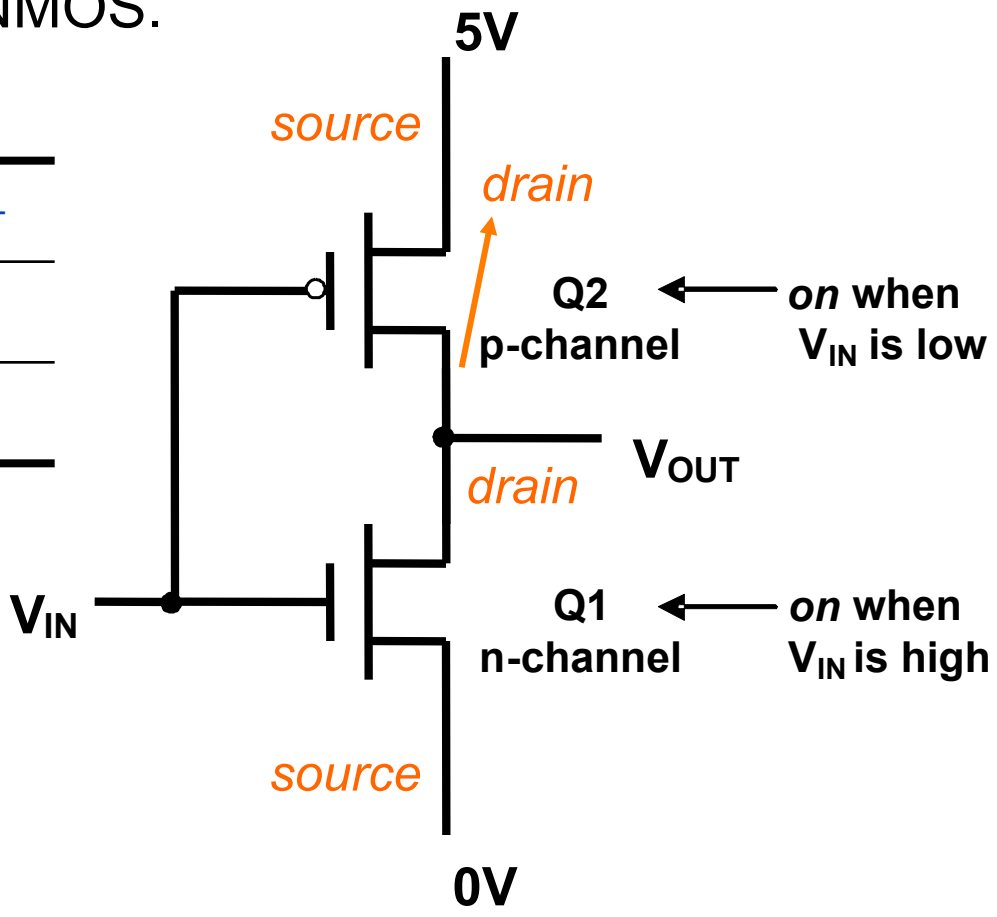
CMOS Inverter

- **CMOS inverter circuit**: the simplest CMOS circuit, requires only one each of a PMOS and an NMOS.
- ***Functional behaviour***:

V_{IN}	Q1	Q2	V_{OUT}
0V (L)	off	on	5V
5V (H)	on	off	0V

- ***Logic symbol***:



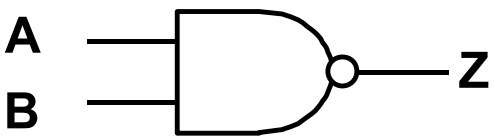


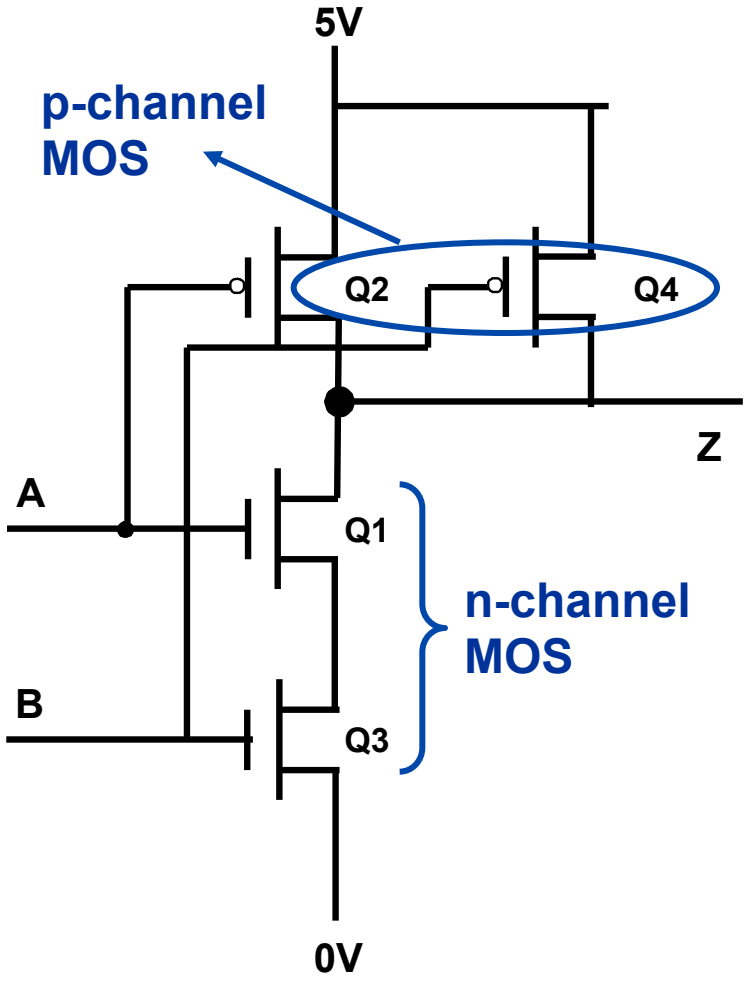
CMOS 2-Input NAND

- **CMOS NAND circuit**: a *k*-input gate uses both *k* PMOS and *k* NMOS transistors.
- ***Functional behaviour***:

A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

- ***Logic symbol***:



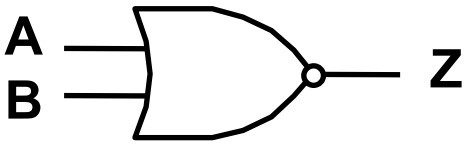


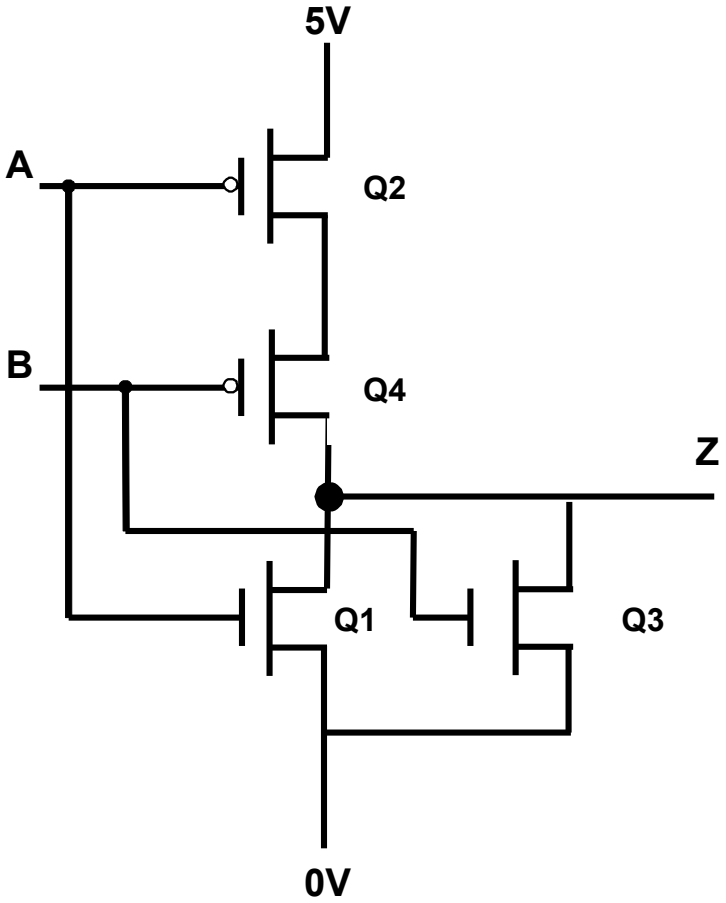
CMOS 2-Input NOR

- **CMOS NOR circuit**: a *k*-input gate uses both *k* PMOS and *k* NMOS transistors.
- ***Functional behaviour***:

A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

- ***Logic symbol***:





CMOS Electrical Properties

- The electrical behaviour of a CMOS gate can be characterised by its *electrical properties*. They include, apart from *logic voltage levels*:
  - *Noise margins* → How much noise it takes to corrupt a worst-case output voltage into a value that can not be recognised by an input.
  - *Fan-out* → Number of inputs that the gate can drive/feed without exceeding its worst-case specifications.
  - *Speed (propagation delay)* → Time necessary for a change in the input signal to result in a change to the output signal.
  - *Power consumption* → Most CMOS circuits have low *static power dissipation*.

Dilemma faced in electronic design – increasing the *speed* (i.e., decreasing the *propagation delay*) typically results in higher *power dissipation*, and vice versa.