SOLUTIONS

Module:	Digital Circuit Design		
Module Code	EBU4202	Paper	B
Time allowed	2hrs	Filename	Solutions_1617_EBU4202_B
Rubric	ANSWER ALL FOUR QUESTIONS		
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Question 1

a) Fill in the table by putting the correct numbers in different bases by doing suitable conversion. Write your answers in the table directly.
Show **THREE** places in any fractional part.

Decimal	Binary	Octal	Hexadecimal
	1011001.100		
55.620			

[12 marks]

Answer
[2] each correct answer in red.
[-0.5] if either integer or fractional part is wrong.

Decimal	Binary	Octal	Hexadecimal
89.500	1011001.100	131.400	59.800
55.620	110111.100	67.475	37.9EB

b) Figure Q1b) shows a particular floating point format.

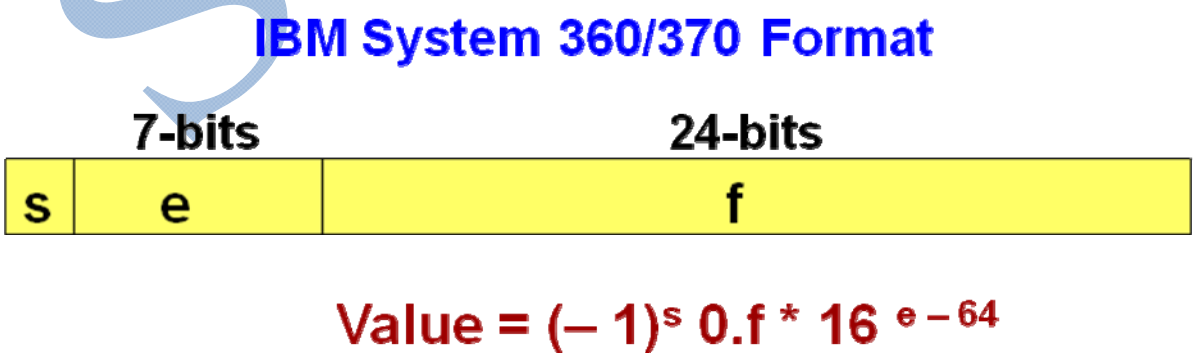


Figure Q1b)

Express the decimal number 0.06 in this format to 8 fractional places. [5 marks]

Answer:
Convert 0.06_{10} to binary:
0.06x2=0.12 MSB
0.12x2=0.24
0.24x2=0.48
0.48x2=0.96
0.96x2=1.92
0.92x2=1.84
0.84x2=1.68
0.68x2=1.36 [2 marks]
So $0.06_{10}=0.00001111_2$ to 8 fractional places
$=1.111_2 \times 2^{-5}$
$=1.111 \times 2^{(59-64)}$
$=1.111 \times 2^{(111011-64)}$ [2 marks]
Therefore floating point format is: 0 /0111011 /11100000000000000000000 [1 mark]

c) Convert the decimal numbers 213 and 126 to 8 bit binary and then obtain the value of (213_{10}-126_{10}) using 2^s complement arithmetic. State the answer in HEX. [6 marks]

Answer:
$213_{10}=11010101_2$ [1 mark]
$136_{10}=10001000_2$ [1 mark]
2^s complement of 10001000=01110111+1=1111000 [1 mark]
11010101+1111000=101001101 [1 mark]
Leading 1 is an overflow bit [1 mark]
Therefore answer is $01001101=77_{10}=4D_H$ [1 mark]

d) A particular data transmission system uses single bit odd parity.
Can an error be detected if the data sent = 01000101 and the data received = 01010010 ? [2 marks]

Answer:
Received value has an odd number of 1's (so obeys odd parity) [1 mark] , so no error is detected (there are 4 bits flipped) [1 mark].

Question 2

a) i)The basic gates used in the design of digital circuits are fabricated into Integrated Circuits. Briefly state the classification of Integrated Circuits based on complexity.

[4 marks]

ii) Modern integrated circuit fabrication techniques allow the on-chip devices to be very small. Briefly explain two advantages.
[2 marks]

Answer: i)

Name	Number of Gates
SmallScale Integration (**SSI**)	< 20
MediumScale Integration (**MSI**)	20 – 200
LargeScale Integration (**LSI**)	200 – 200000
Very LargeScale Integration (**VLSI**)	≈ 1 million **transistors**

[4 marks: 1 each]

ii)

The two advantages are:
Device operation is fast because of the short interconnections [1 mark]
Very complex circuits can be produced in a very small package [1 mark]

b) Two technologies used in the manufacture of logic gates are TTL and CMOS. Compare gates using these two technologies in terms of noise margin and fan out.
[4 marks]

Answer:

	T_p (ns)	P (mW)	Noise Margin (mV)	Fan-out
TTL	9	10	400 (OH); 400 (OL)	10
CMOS	18	0.01 (static)	1050 (OH); 1340 (OL)	≤ 50

Answer:
CMOS has a greater noise margin than TTL
CMOS has a greater fanout than TTL.
[4 marks:2 for the data, 2 for the statements]

c) Let ABCD represent a 4 bit BCD number.

i) Draw the truth table for a combinational logic circuit that produces a '1' output when the input ABCD is an even number and also when the number 9. The input combination 0000 is not allowed to occur.

ii) Draw the Karnaugh map for this circuit.

iii) From the Karnaugh map, determine a minimal expressions for the output expressed in SoP form and in all NAND form.

iv) Using a truth table, show the state of the output for each of the "can't happen" input states as a result of the minimisation.

v) Draw the circuit diagrams for the minimal SoP and all NAND implementations of the function.

vi) Does the circuit have a static race hazard? Justify your answer.

[15 marks]

Answer:

i) The truth table is:

A	B	C	D	F(A,B,C,D)
0	0	0	0	X
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

[2 marks for correct truth table]

ii) The Karnaugh map is:

CD	00	01	11	10
AB				
00	X	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	1	X	X

[2 marks for correct map]

iii) A minimal SoP expression is: F=A+D' [2 marks]

Applying de Morgan's theorem, the all NAND expression is: F=(A'.D)' [2 marks]

iv) The resulting output states are:

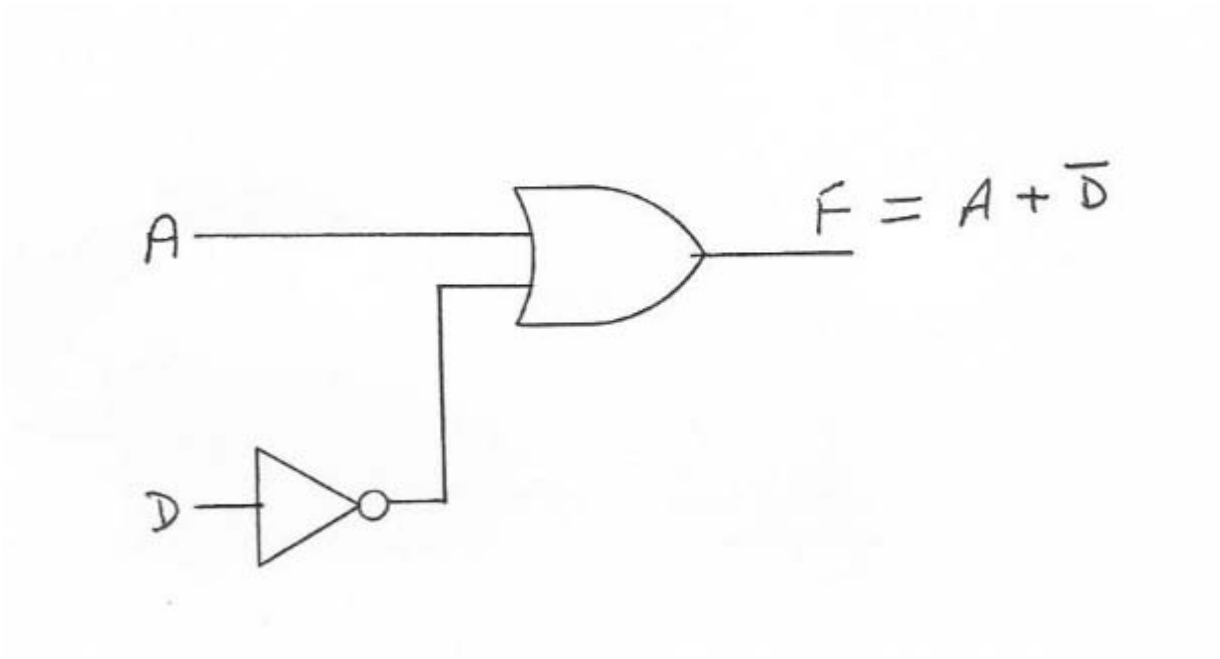
A	B	C	D	F(A,B,C,D)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

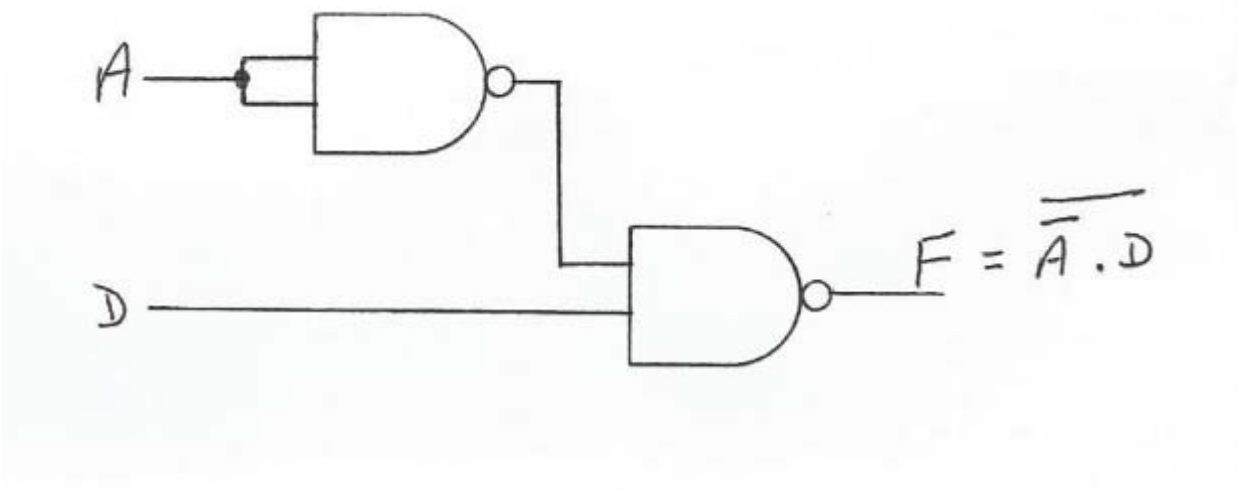
[1 mark]

v) The circuit diagrams are:

SoP:



All NAND:



[4 marks: 2 for each correct diagram]

vi) The circuit does not have a static race hazard [1 mark] because the map groupings overlap[1 mark].

Question 3

Figure Q3 shown a simple motor-shaft position encoder circuit. As the machine moves, the encoder shaft is rotating clock-wise manner, making and breaking the light beam between LED and phototransistor, thereby generating clock pulses to increase the counter circuit.

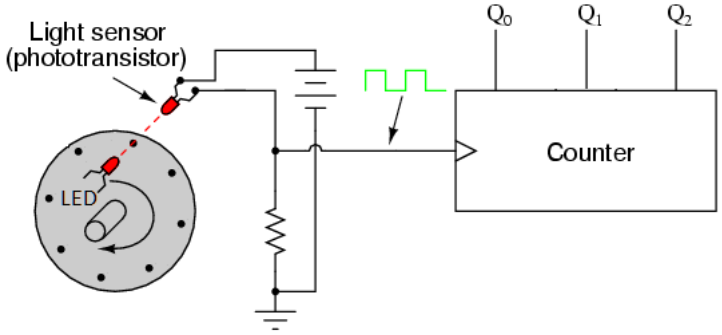


Figure Q3

Design a digital counter circuit using D flip-flops to track the angular position of the motor-shaft down to a precision of 45 degree.

i) Derive truth table for the counter which include present state, next state and the D flip-flop transition table to complete the input to D flip-flops.

[8 marks]

Present state (Q2, Q1, Q0)	Next state (Q2, Q1, Q0)	D flip-flop input		
		D2	D1	D0
000	001	0	0	1
001	010	0	1	0
010	011	0	1	1
011	100	1	0	0
100	101	1	0	1
101	110	1	1	0
110	111	1	1	1
111	000	0	0	0

2 marks for the correct "Present state" table; otherwise 0 marks
2 marks for the correct "Next state" table; ; otherwise 0 marks
4 marks for the correct "D flip-flop input table; ; otherwise 0 marks

ii) Construct the K-maps and finding out the minimised logic expressions for the input to D flip-flops.

[12 marks]

Q2\Q1 Q0	00	01	11	10
0	0	0	1	0
1	1	1	0	1

D2 = Q2Q0' + Q2Q1' + Q2'Q1Q0

Q2 \ Q1 Q0	00	01	11	10
0	0	1	0	1
1	0	1	0	1

D1 = Q1Q0' + Q1'Q0

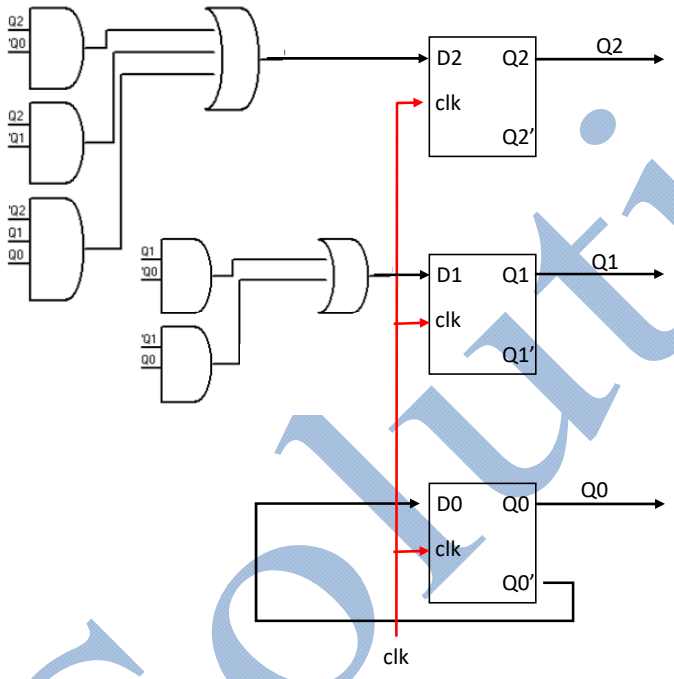
Q2 \ Q1 Q0	00	01	11	10
0	1	0	0	1
1	1	0	0	1

D0 = Q0'

Each D input, 1 marks for the correct k-map and 2 marks for the correct minised logic expressions

iii) Draw the designed counter circuit.
[5 marks: 1 for each input logic, 1 for each bistable]

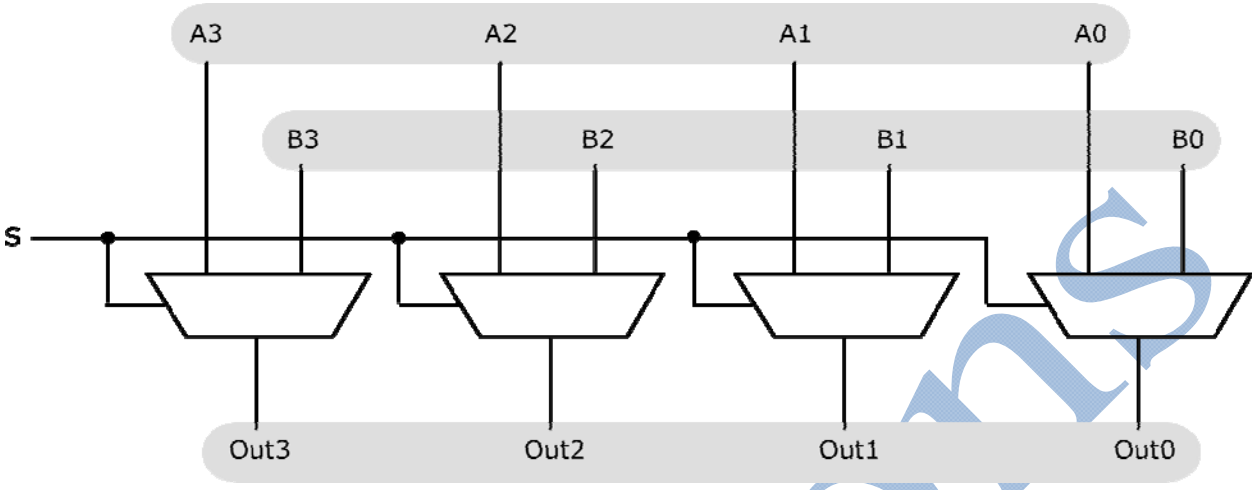
Answer



Question 4

a) Using a suitable diagram, explain the internal implementation of a 2-input 4-bit MUX.
[5 marks]

Answer:



Selects between two 4-bit binary number inputs
Made up of 4 parallel 2-input 1-bit selectors
[3 marks for diagram, 2 marks for brief explanation]

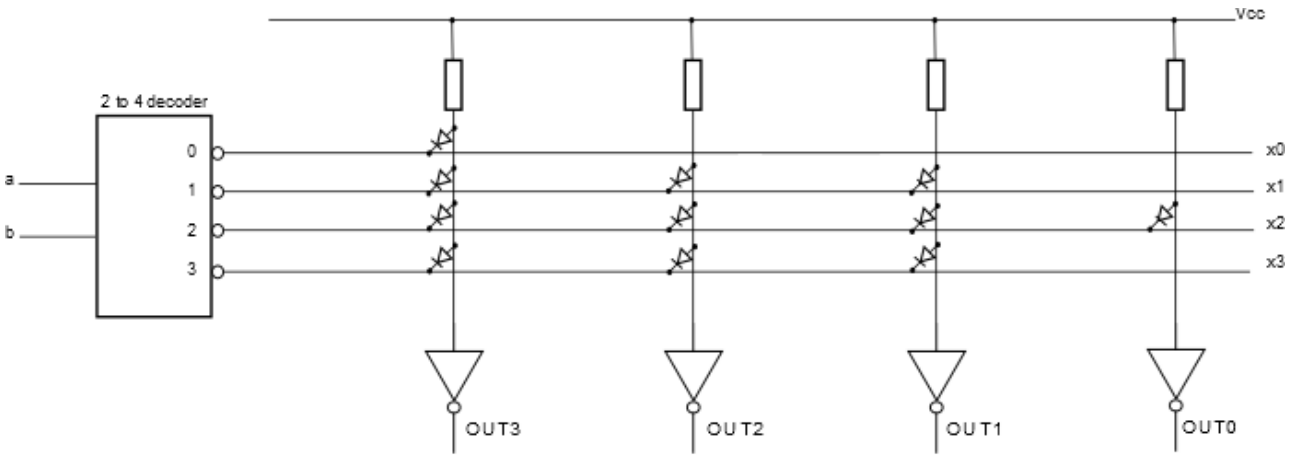
b) Explain the difference and similarity between ROM and RAM.
[8 marks]

ROM and RAM are both random access [2 mark]. Every location in both types of memory can be accessed in the same length of time [2 mark].
ROM is non-volatile, ie, contents of memory are retained when power is removed. [2 mark]
RAM is volatile, ie, contents of memory are lost when power is removed[2 mark].

c) Design an 4 x 4-bit read-only memory (ROM) circuit pre-programmed with the data shown in the Table Q4. (Hint: diodes, decoder, multiplexer etc. are required in the ROM circuit).
[12 marks]

Address	Data (4-bit)
0	8
1	14
2	15
3	14

Answer



[6 marks for 2 to 4 decoder, 6 marks for the diodes & buffers]