Digital Circuit Design

Queen Mary University of London

Course Code: EBU4202

School of Electronic Engineering and Computer Science

Lab Sheet 1: Introduction to Digital Logic	Date: ______________________
Student's Surname, First Name (in English): ______________________	Student's BUPT Number, Class Number: ______________________
Email Username (102*xxxxx*): ______________________	Total Mark (out of **25**): ______________________

IMPORTANT:

(a) In advance of the lab session: Print this Lab Sheet, read it and complete all the indicated "Preparatory Work".
(b) Write all your answers on this Lab Sheet, where indicated.
(c) Use additional A4 sheets of paper if you require more space to write your answers, ensuring that the question numbers are indicated clearly.
(d) Before handing in your Lab Sheet, make sure that you fill in the Table above with your personal details, ***and*** staple any additional answer sheets (with your name written on them) together with this Lab Sheet.
(e) Any question marked with the symbol **(***)** requires that you demonstrate your work to one of the TAs.

1. Learning Objectives

The aims of this Lab Session are to:

(a) set up a *breadboard* that you will use to build and test all your digital circuits ***and***,
(b) reinforce the ideas on the operation of the basic set of digital logic gates (i.e., AND, NAND, OR, NOR and NOT) by testing a series of 5 integrated circuits and completing their truth tables.

You will then combine a small number of gates to produce other simple functions. In later experiments, you will use these gates as building blocks to construct more complex functions (e.g., *adders* and *multipliers*).

2. Preparatory Work

Question 2.1 [2 Marks] – Write down below the expected truth tables for all the above gates and for the Exclusive-OR (XOR) function, indicating clearly both the inputs and outputs. Also write down De Morgan's theorem ***and*** use it to prove that the circuit shown in **Figure 13** is equivalent to the Exclusive-OR function. Show all your work and calculations.

Answer to Question 2.1

3. Apparatus

All the experiments are performed on a general-purpose logic board or "breadboard" (see **Figure 1**) with a fixed hardware configuration, into which integrated circuits can be inserted. Designs are implemented by pushing leads or components into the board. Beneath the surface, a fixed network of connections is used to connect the logic elements as required. Switches for setting input conditions and LED indicators for observing outputs or checking logic levels within a complex circuit are implemented by using a combination of an LED and a 220 Ohms resistor, connected to a power supply.

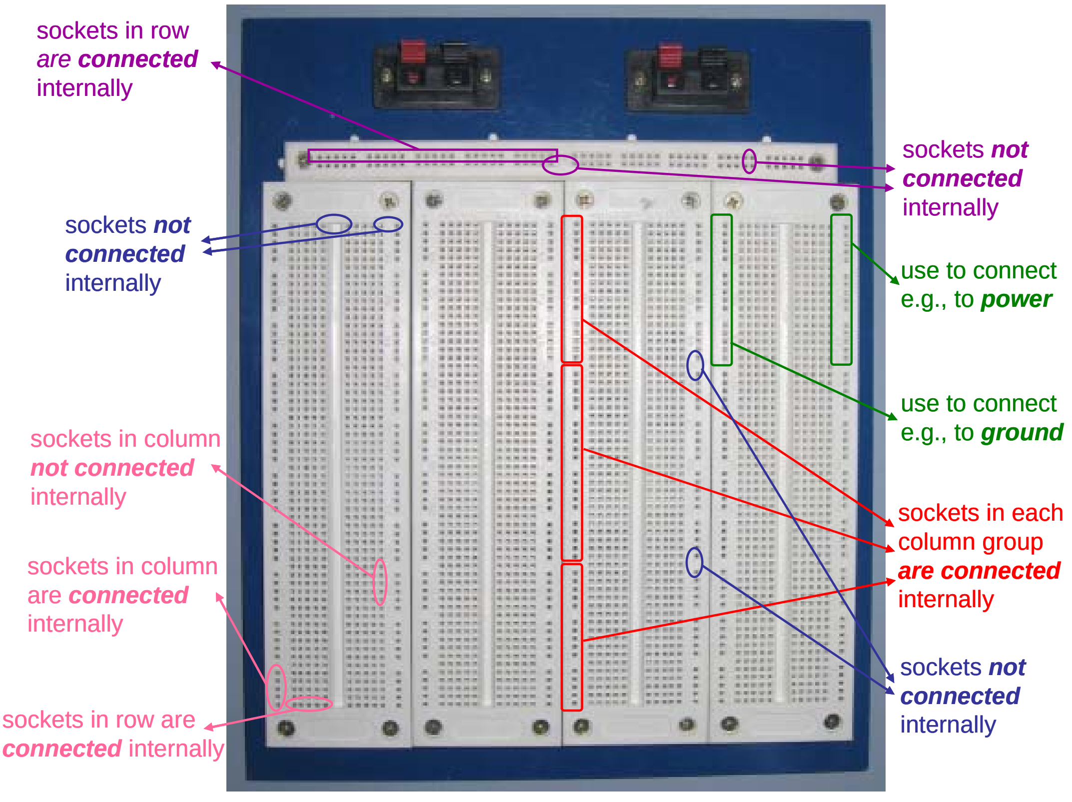

Figure 1 – "Breadboard" (Model: SYB-118) panel layout.

4. Familiarisation

The "breadboard" has many tiny holes (also called *sockets*) into which the electronic components are pushed. It consists of three main areas (see **Figure 2**):

1. <u>Top Zone</u> → This has two sets of connectors (red and black – from left to right). Usually, you will connect the red (*Va*) and black (*Gnd*) connectors to the Power Supply Unit.
2. <u>Middle Zone</u> (2 rows, in 10 separate sets) → These rows are usually connected to the Power Supply Unit, once you have used the red and black connectors mentioned in the previous bullet point. Both rows can be used for connecting to ***power*** (*+5 volts*) or to ***ground*** (*0 volts*). However, it is useful to use the following convention: use each row for one purpose only (i.e., either ***ground*** or ***power***).
3. <u>Bottom Zone</u> (4 sets, each containing: 2 five-wide columns and 2 single columns) → This is the area where all the electronic components (including those in **Figure 5**) will be pushed into. Again, each of the single columns in this area can be used for connecting to ***ground*** or ***power***, through a connection to one of the sets in the Middle Zone. **Figure 1** illustrates how each of the columns can be used.

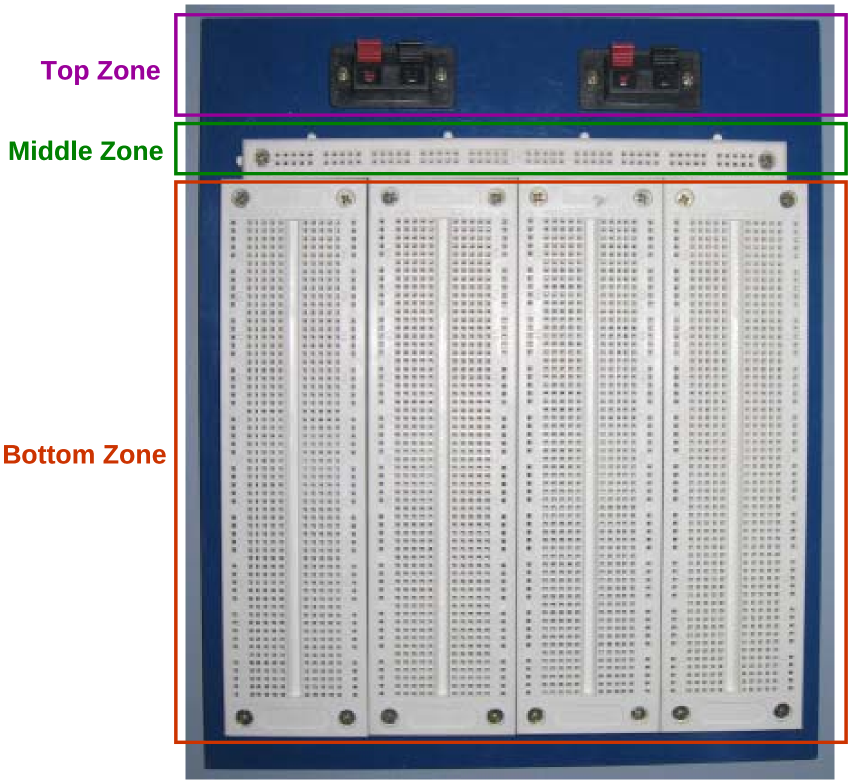

Figure 2 – "Zones" of the Breadboard.

All the ICs you will be using are inside so-called 'Dual In-Line' packages (also known as DIL or DIP). There is always a marker on the top surface at one end of the package to indicate *pin 1* (see **Figure 3**); the ICs used in this experiment have only 14 pins. This marker is usually a *notch* or a small circular depression. The remaining pins are then numbered anticlockwise from *pin 1*.

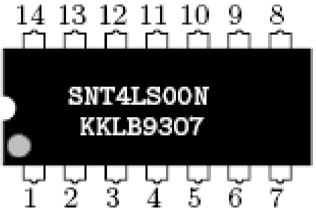

Figure 3 – Example of 14-pin IC.

Notes:
1. It is usually a good idea to have all ICs in the same orientation[1] to avoid confusion when connecting them up.
2. Although most logic diagrams do not show Power Supply connections, your circuits will not function without them! (See also Section 6 – "Logic Gates".)

In the SIL Commoned Resistors used for the configured breadboard, *pin 1* is identified by a mark (a dot), whereas in the LED Bar Graph Array, *pin 1* is labelled as the so-called anode mark. See **Figure 4** for a representation of *pin 1* in these components.

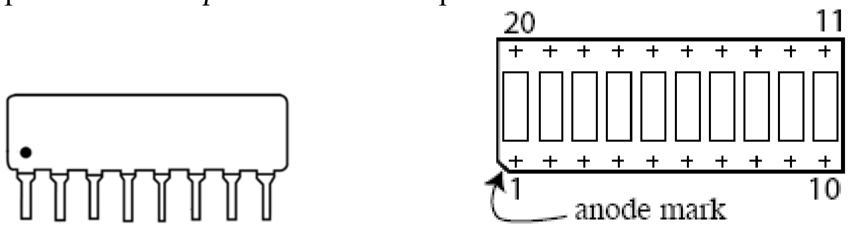

Figure 4 – Identification of *pin 1* in SIL Commoned Resistors and LED Bar Graph Arrays.

5. Setting up the Breadboard

Before you can start building and testing digital circuits, you need to set up the *breadboard*. This requires an understanding of how the *breadboard* works, as well as the electronic components below:

- ✓ Power Supply Unit
- ✓ Breadboard (see **Figure 1**)
- ✓ Connecting Wires
- ✓ LED Bar Graph Array (10 elements; 2 not used) → It consists of 10 Light Emitting Diodes and is used to provide a visual indication of an analogue voltage signal.
- ✓ 8-Channel Darlington Driver IC (ULN2803A) → An electronic switch that provides an output signal to drive output subsystems requiring high current.
- ✓ 2 SIL Commoned Resistors (220 *ohms*; 9-pin) → This is a Single-In-Line package of 9 resistors with one common connection; its function is to reduce the flow of electric current.
- ✓ DIL Switch (8 way) → It provides switches that close when pressed. The output signal from a given switch goes high when that switch is pressed.

You can find a representation of the last four components in **Figure 5** (together with profile representations in **Figure 4**), but please note that some components available in your lab may look slightly different e.g., you may have to use several individual resistors instead of the SIL Commoned Resistor shown below. Your lab supervisors will be able to advise if alternative components (but with the same functionality) need to be used instead.

[1] This applies in general, but it does not apply to the orientation of the LED Bar Graph Array (as shown by **Figure 6**).

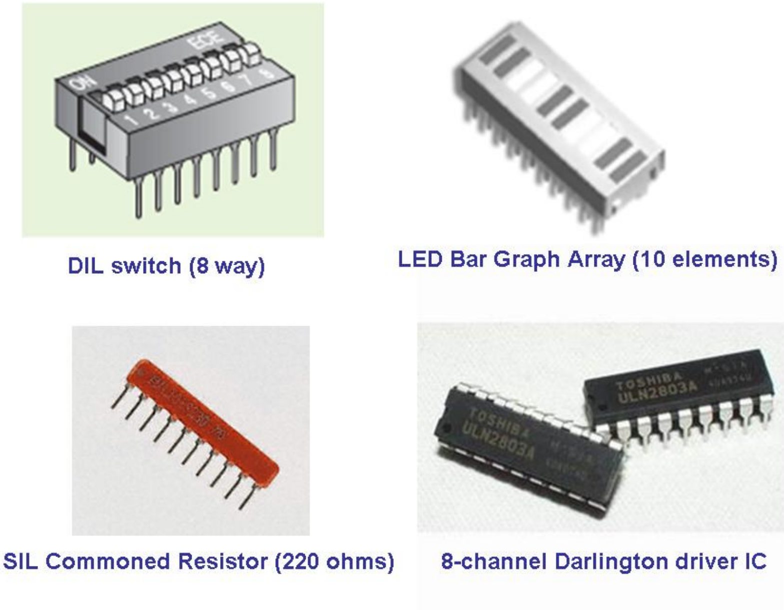

Figure 5 – Some electronic components for the *breadboard*.

Figure 6 shows the configuration required to set up the *breadboard*, using the com ponents listed before. Make sure you assemble the components as indicated (<u>including any alternative components you may have to use</u>), and then test its operation by doing the following:

1. Start with the Power Supply Unit turned OFF: You should not see any LEDs in the LED Bar Graph Array turned ON.
2. Switch the Power Supply Unit ON.
3. Switch e.g., switch 5 in the DIL Switch to ON: You should see the corresponding LED light be turned ON.
4. Turn switch 5 back to OFF: You should see the corresponding LED light be turned OFF.
5. Try *Steps 3* and *4* for other switches in the DIL Switch.

IMPORTANT: This *breadboard* conf iguration will be used in a ll of the hardware labs of this course. Therefore, you should take notes on the step s that you were required to follow to set up the *breadboard*, as this will save you time when starting the other hardware labs later in the semester.

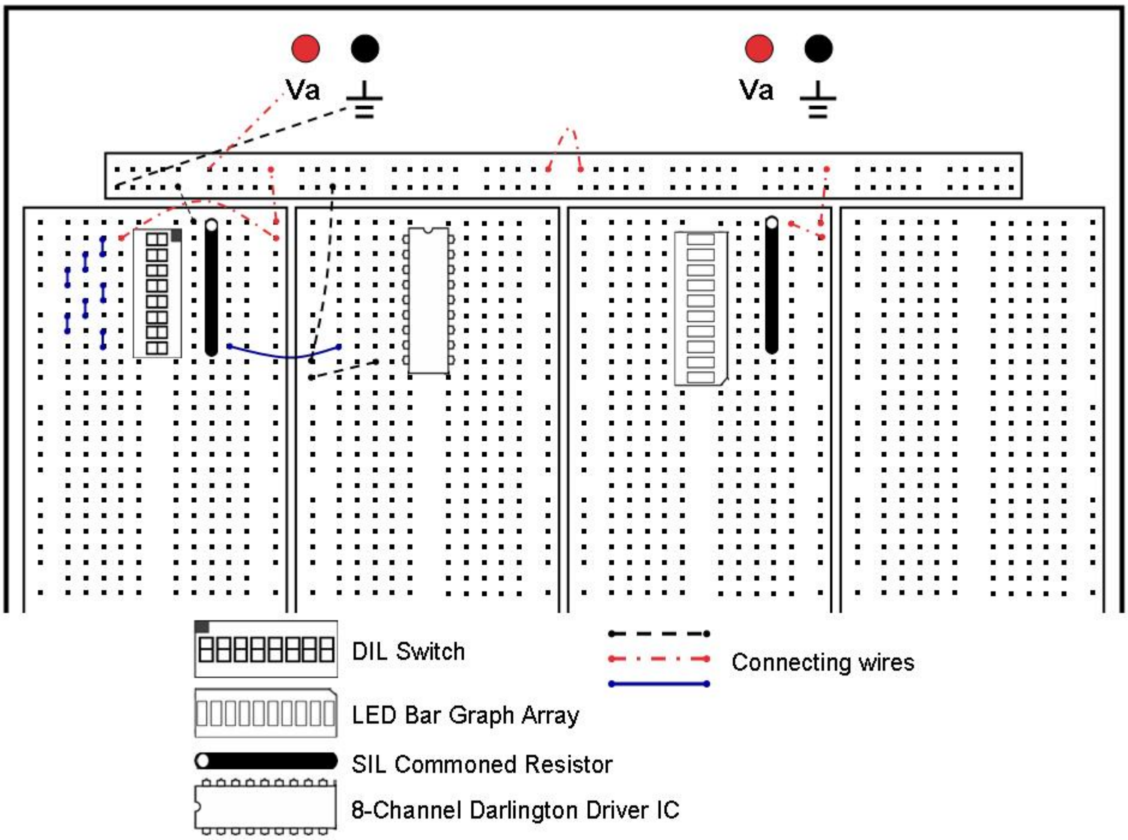

Figure 6 – The *breadboard* configuration[2].

6. Logic Gates

For this experim ent, you will be using the followi ng TTL (Transistor-Transistor Logic) integrated circuits (**Figure 7** through to **Figure 11** show the ICs viewed from the top):

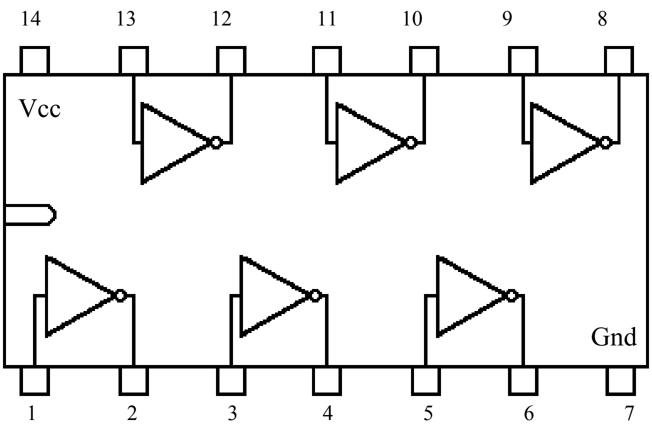

Figure 7 – 7404 Hex inverters (labelled *HD74LS04P*) i.e., 6 NOT gates in one IC.

[2] This configuration assumes that all the components are exactly as in **Figure 5** – if this is not the case, your lab supervisors (*aka* Teaching Assistants) will be able to advise of any required adjustments to the *breadboard* configuration.

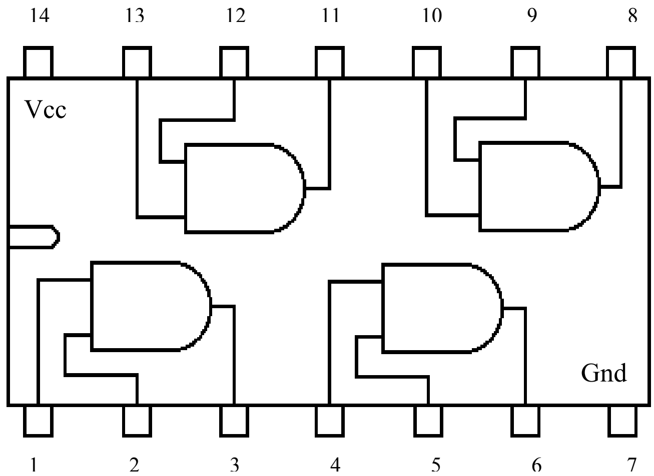

Figure 8 – 7408 (labelled *HD74LS08P*) quadruple 2-input AND gates.

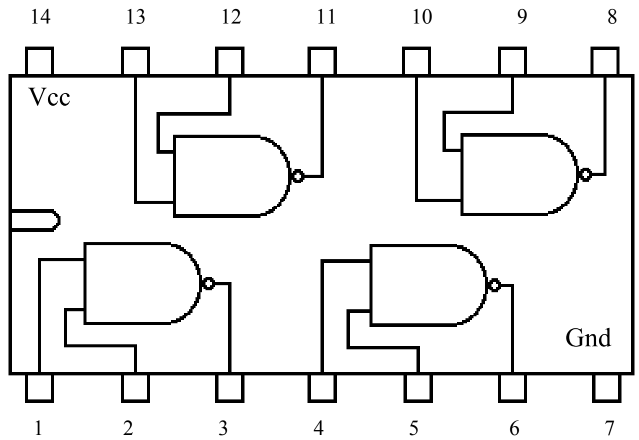

Figure 9 – 7400 (labelled *HD74LS00P*) quadruple 2-input NAND gates.

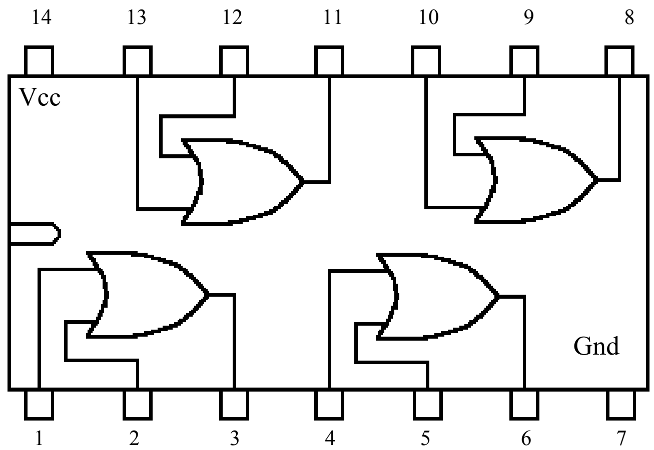

Figure 10 – 7432 (labelled *HD74LS32P*) quadruple 2-input OR gates.

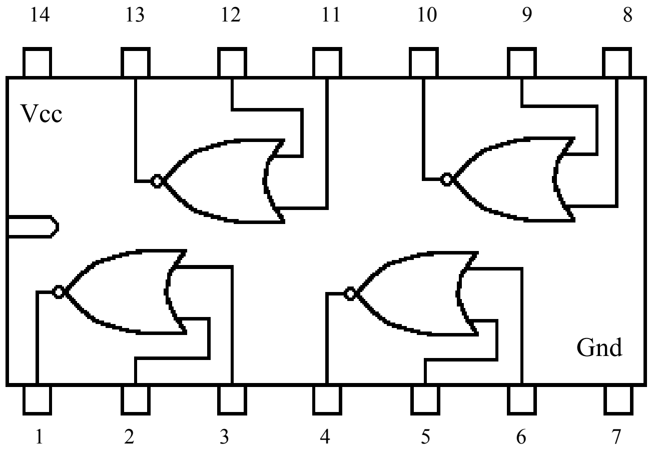

Figure 11 – 7402 (labelled *HD74LS02P*) quadruple 2-input NOR gates.

Looking at any of the 2-input gates, if we designate the two inputs as ***x*** and ***y*** and the output as ***z***, then at any time the variables ***x***, ***y*** and ***z*** are each at a logic state of either "0" or "1". Logic "0" is represented as a voltage typically between *0* and *0.8 volts*, and logic "1" in the range of 2 to *5 volts*. The same applies to the inverter, although it only has one input, ***x***, and one output, ***z***. Output ***z*** is a function of the inputs, the functions being **NOT** (inverter), **AND**, **NAND**, **OR** or **NOR** using the ICs listed above.

7. Experiments

EXPERIMENT 1 – Verifying the Truth Tables

(***) Question 7.1.1 [4 Marks] – Complete the **Table 1** below by testing each IC of *Section 6 – "Logic Gates"* (i.e., from **Figure 7** through to **Figure 11**) in turn.

Inputs		**Outputs (*z* = *f* (*x*, *y*))**				
X	***Y***	***x'***	***x.y***	**(*x.y*)'**	***x+y***	**(*x+y*)'**
0 0						
0 1		-				
1 0						
1 1		-				

Table 1 – ***Answer to Question 7.1.1***: Testing of 74 Series TTL Circuits.

Note: The prime symbol (′) in **Table 1** indicates inversion, as defined in the course textbook.

You only need to test one gate on each IC. Connect the input(s) to the DIL Switch, via the SIL Commoned Resistor (on the left of **Figure 6**) and the output to an LED in the LED Bar Graph Array, via the 8-Channel Darlington Driver IC. Set the switches first to '0' and look at the output LED. 'ON' indicates logic '1', and 'OFF' indicates logic '0'. Note the result in the appropriate place in the table.

Continue with the remaining switch combinations and then test the next IC. If any of the results are not as you expected, double check that the connections are correct (e.g., have you connected the power pins?). Then go over your experimental procedure again. If it looks as though the IC may be faulty, ask for another one and repeat the experiment.

Question 7.1.2 [2 Marks] – Describe in your own words:

a) What is the aim of **Experiment 1** (i.e., what is the purpose of the experiment)?

Answer to Question 7.1.2 – a)

b) What method did you follow to execute **Experiment 1** (i.e., what steps were required to execute the experiment)?

Answer to Question 7.1.2 – b)

EXPERIMENT 2 – Alternative Implementations of Functions

(***) Question 7.2.1 [4 Marks] – Implement the circuits in **Figure 12** and complete their truth tables. Compare the results with functions in **Experiment 1**; what conclusions can you derive?

Answer to Question 7.2.1

Note: The circles on the inputs to the AND and OR gates indicate inversion, which you may implement in any one of the 3 ways that you should have discovered by now.

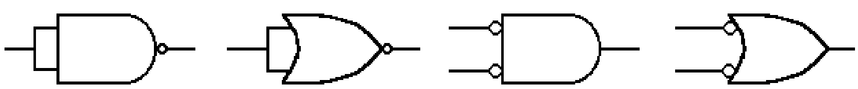

Figure 12 – Functions to be implemented.

Question 7.2.2 [3 Marks]

a) What logic function do the first two circuits (of **Figure 12**) represent?

Answer to Question 7.2.2 – a)

b) The 3rd and 4th circuits in **Figure 12** should have identical Truth Tables to two of the functions tested in **Experiment 1**. If so, write down the Boolean equation for each identical pair (for example, the 4th function in **Figure 12** is written $x' + y'$). What important Theorem do the two equations illustrate?

Answer to Question 7.2.2 – b)

Question 7.2.3 [2 Marks] – Describe in your own words:

a) What is the aim of **Experiment 2** (i.e., what is the purpose of the experiment)?

Answer to Question 7.2.3 – a)

b) What method did you follow to execute **Experiment 2** (i.e., what steps were required to execute the experiment)?

Answer to Question 7.2.3 – b)

EXPERIMENT 3 – The Exclusive OR (XOR) Function

The Exclusive OR function is used less frequently than the other standard forms that you have used so far, and so is not available directly on an IC. However, it can be implemented in a number of different ways; probably the simplest way is using all four gates on a 7400 IC.

(***) Question 7.3.1 [5 Marks] – Build and test the circuit shown in **Figure 13** and complete the truth table.

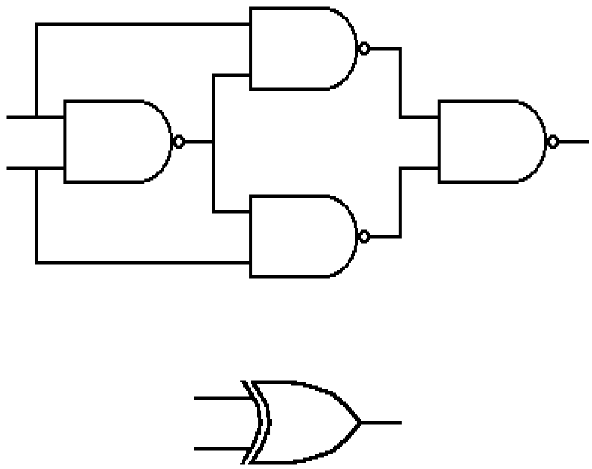

Figure 13 – The Exclusive OR function, using NAND gates and the XOR logic symbol.

HINT: Use only one IC. Draw your proposed chip diagram in the space provided below and then, referring to **Figure 9**, write appropriate *pin* numbers against all the gate connections. Connect up the circuit using your diagram as a guide. This will make fault finding much easier for you and the demonstrators – remember that if you need help, the demonstrator will not be able to follow an undocumented mess!

<u>Answer to Question 7.3.1</u>

Question 7.3.2 [1 Mark]

a) What is the Boolean equation for the XOR gate? (**Note**: This should be evident from the Truth Table.)

<u>Answer to Question 7.3.2</u>

Question 7.3.3 [2 Marks] – Describe in your own words:

a) What is the aim of **Experiment 3** (i.e., what is the purpose of the experiment)?

<u>Answer to Question 7.3.3 – a)</u>

b) What method did you follow to execute **Experiment 3** (i.e., what steps were required to execute the experiment)?

<u>Answer to Question 7.3.3 – b)</u>

END OF Lab Session 1: Introduction to Digital Logic