

# LAB A-02 Report

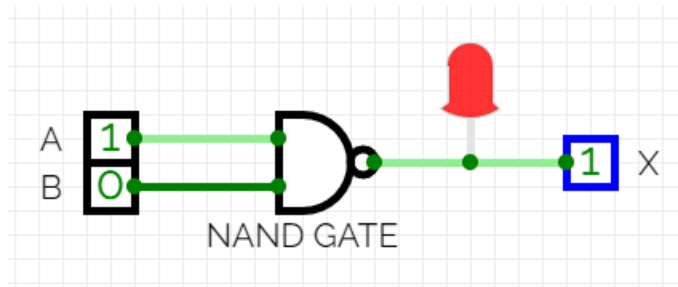
TT0L – Group 0

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Q1.

(i) 2 Input NAND GATE:

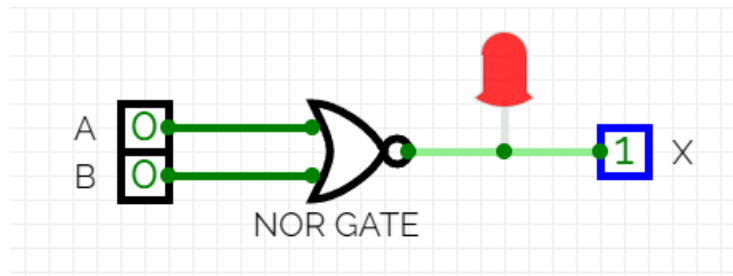


Boolean Expression:

Truth Table:

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

(ii) 2 Input NOR GATE:

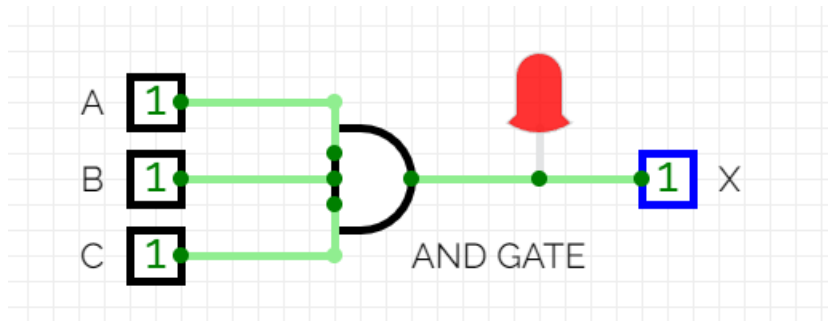


Boolean Expression:

Truth Table:

A	B	
0	0	
0	1	
1	0	
1	1	

(iii) 3 Input AND GATE:

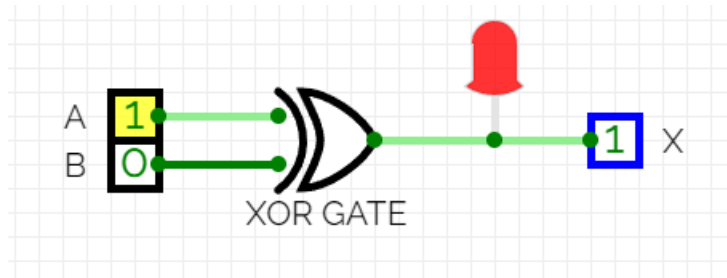


Boolean Expression:

Truth Table:

A	B	C	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(iv) 2 Input XOR GATE:



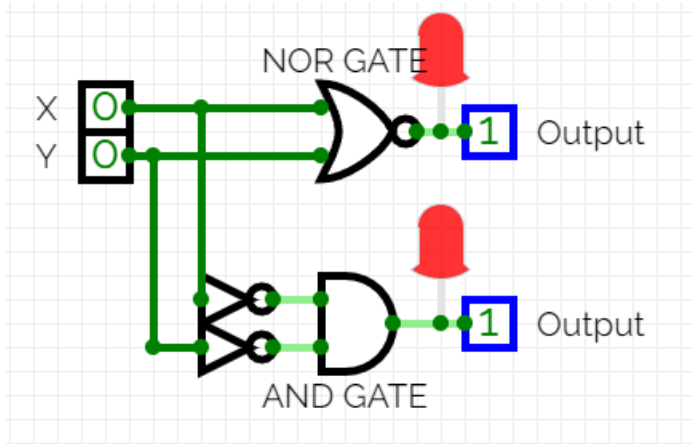
Boolean Expression:

Truth Table:

A	B	
0	0	
0	1	
1	0	
1	1	

Q2.

a. NOR gate equivalent to a Negative AND gate:

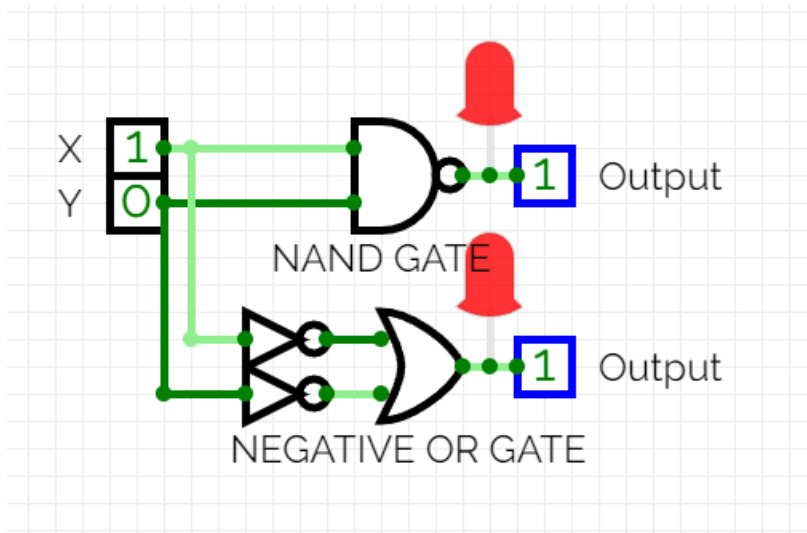


Boolean Expression:

Truth Table:

X	Y	

b. NAND gate equivalent to a Negative OR gate:



Boolean Expression:

Truth Table:

X	Y	

Q3.

NOR GATE:

8 4 2 1 Lmao IDK y I have this.....

A = 10 = 1010

B = 13 = 1101

$C = 7 = 0111$

NOR = 0000

Q4.

NAND GATE:

$A = 6 = 0110$

$B = 9 = 1001$

$C = 11 = 1011$

NOR = 1111

Q5.

a. NAND GATE

Timing Diagram:

b. XOR GATE

Timing Diagram: