LAB A5 Report

TT0L - GROUP 0

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1. Design a 3 input priority encoder circuit. The inputs are a3a2a1, with a3 having the lowest priority and a1 the highest. The outputs are y2y1, indicating the encoded highest-priority active input, and v, the valid output which indicates that at least one input is active. (Note: Priority input a3 is encoded as 11, a2 as 10 and a1 as 01)
Perform the following:

I. Construct the truth table

a3	a2	a1	y2	y1	v
0	0	0	x	x	0
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	0	1	1

II. Simplify the Boolean expressions for y2, y1 , and v using Karnaugh map techniques.

a3/a2a1	00	01	11	10
0	x	0	0	1
1	1	0	0	1

$y2 = \overline{a1}$

a3/a2a1	00	01	11	10
0	x	1	1	0
1	1	1	1	0

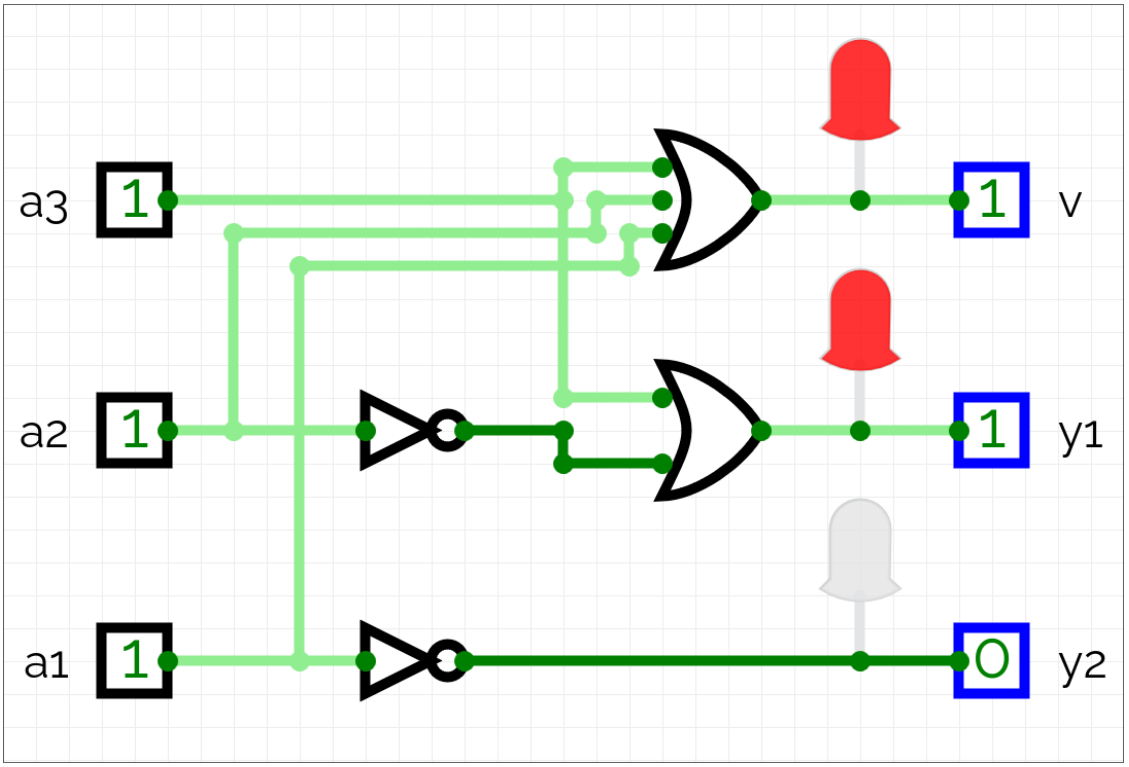
$y1 = \overline{a2} + a1$

a3/a2a1	00	01	11	10
0	0	1	1	1
1	1	1	1	1

$v = a3 + a2 + a1$

III. Draw the logic diagram with necessary basic logic gates.

IV. Verify your design experimentally



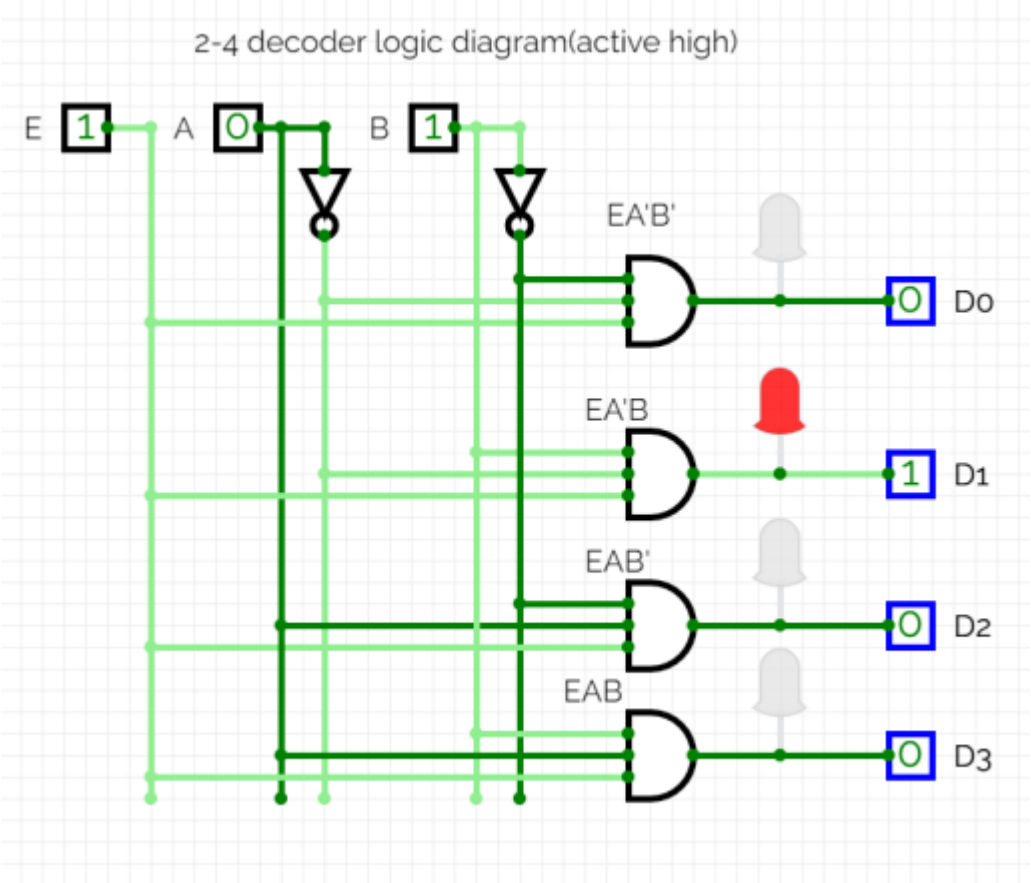
2. Design and construct a 3 to 8 decoder circuit using 2-line-to-4-line decoder and also other logic gates needed.
Perform the following:

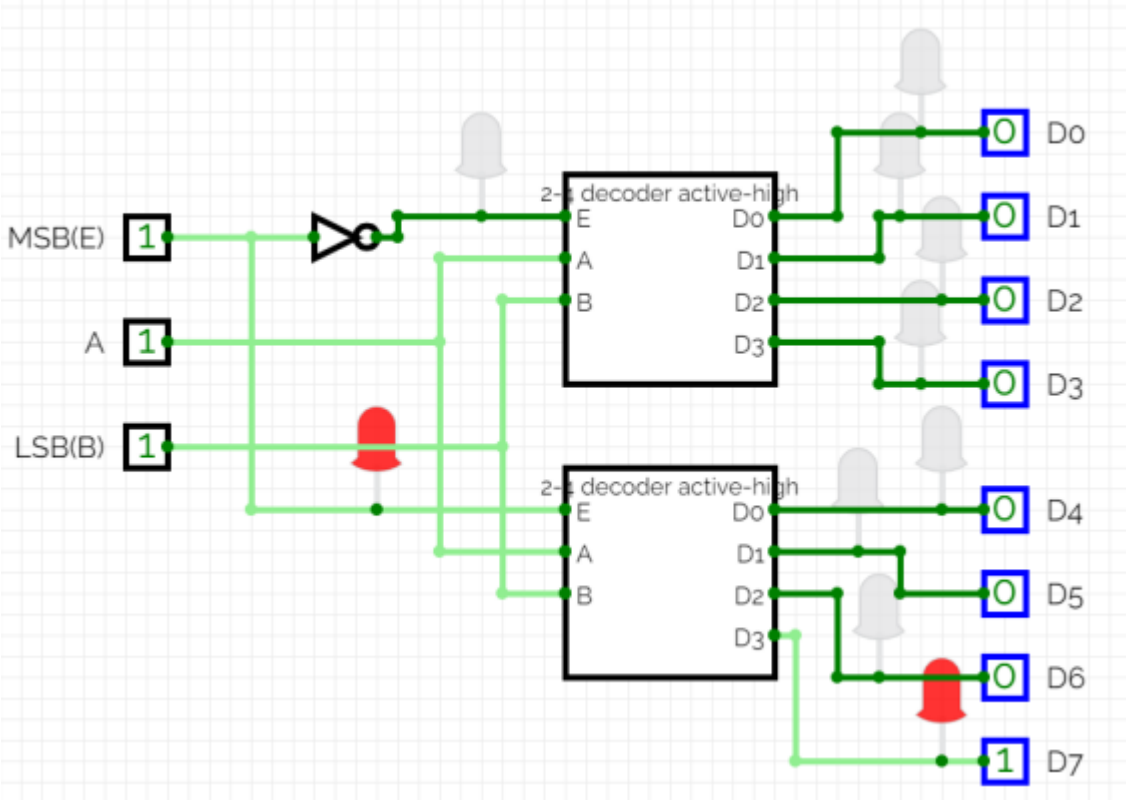
I. Form the truth table for higher order decoder (3 to 8 decoder)

X	Y	Z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

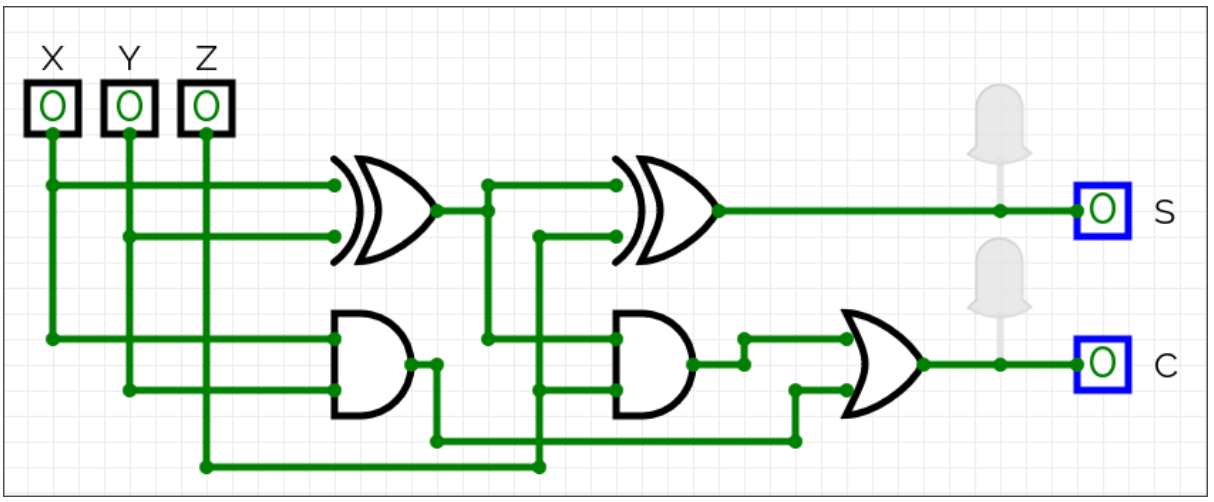
A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

E	A	B	D0	D1	D2	D3
0	X	X	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

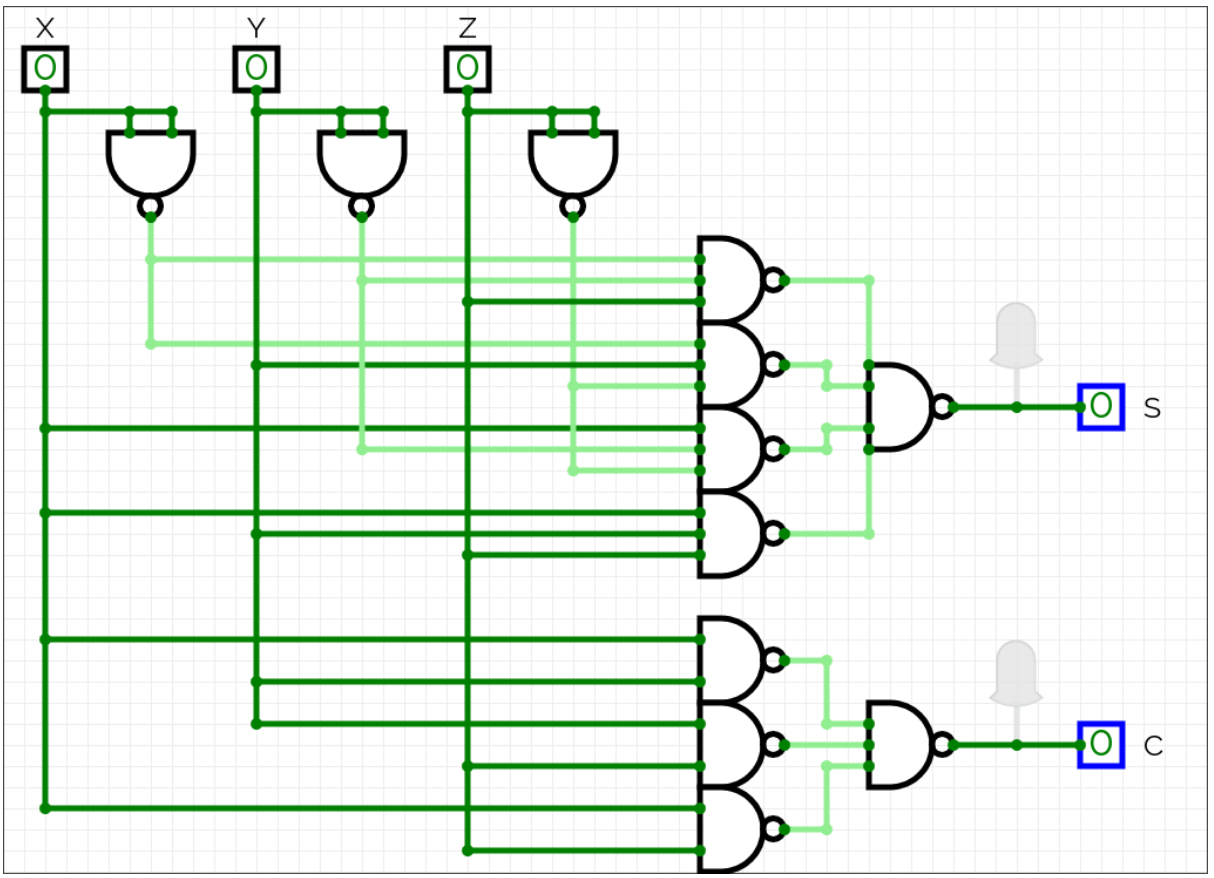




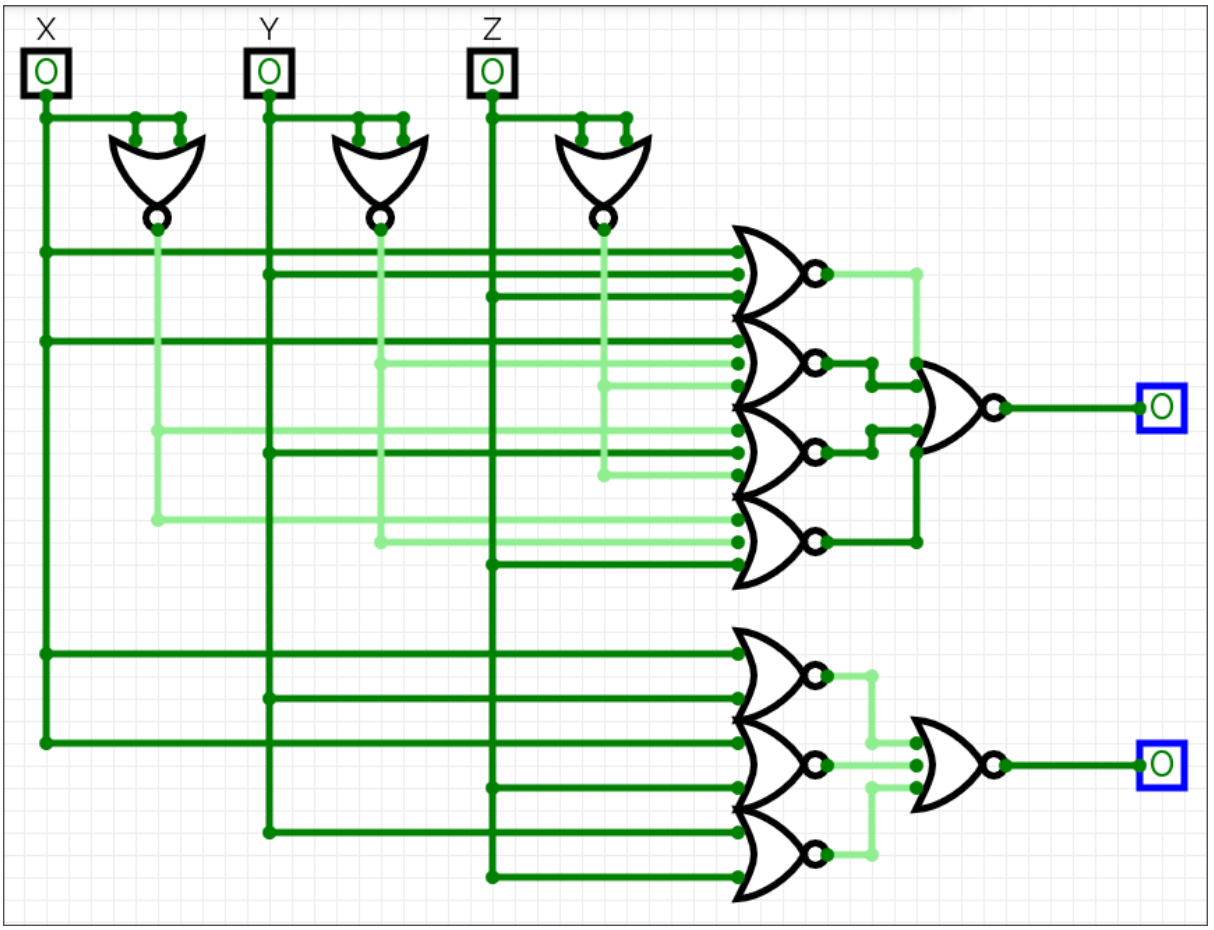
3. Design a full adder circuit using
   I. Two half adders



II. Using only NAND gates



III. Using Only NOR gates

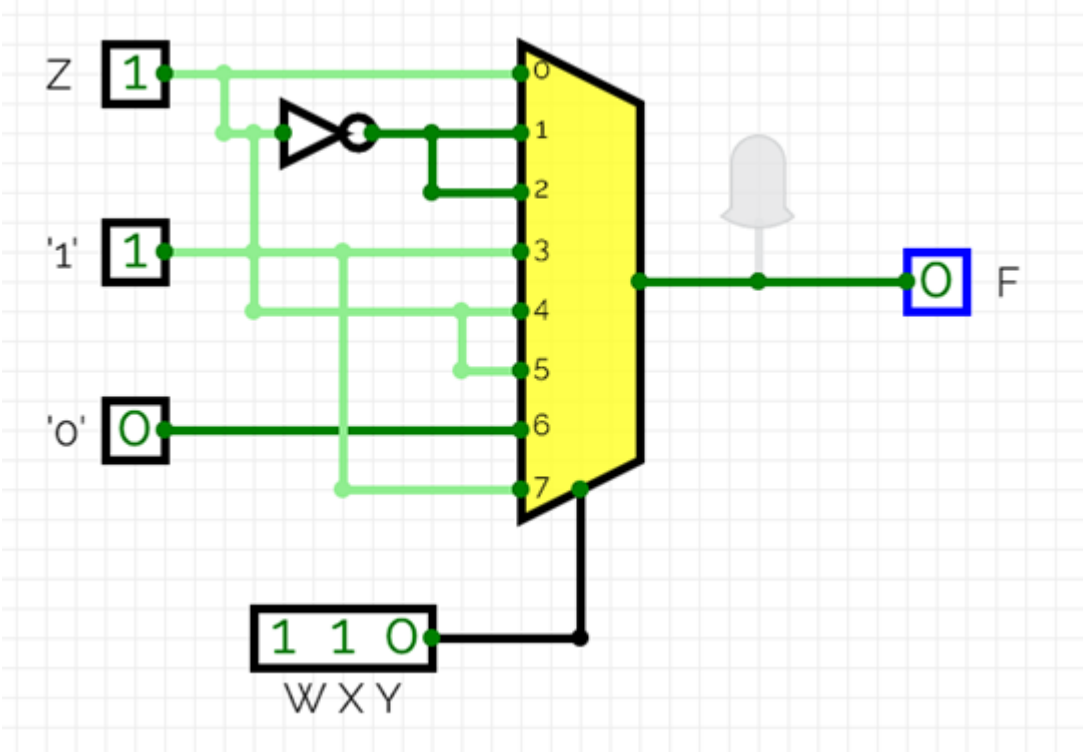


4. Implement the following Boolean expression

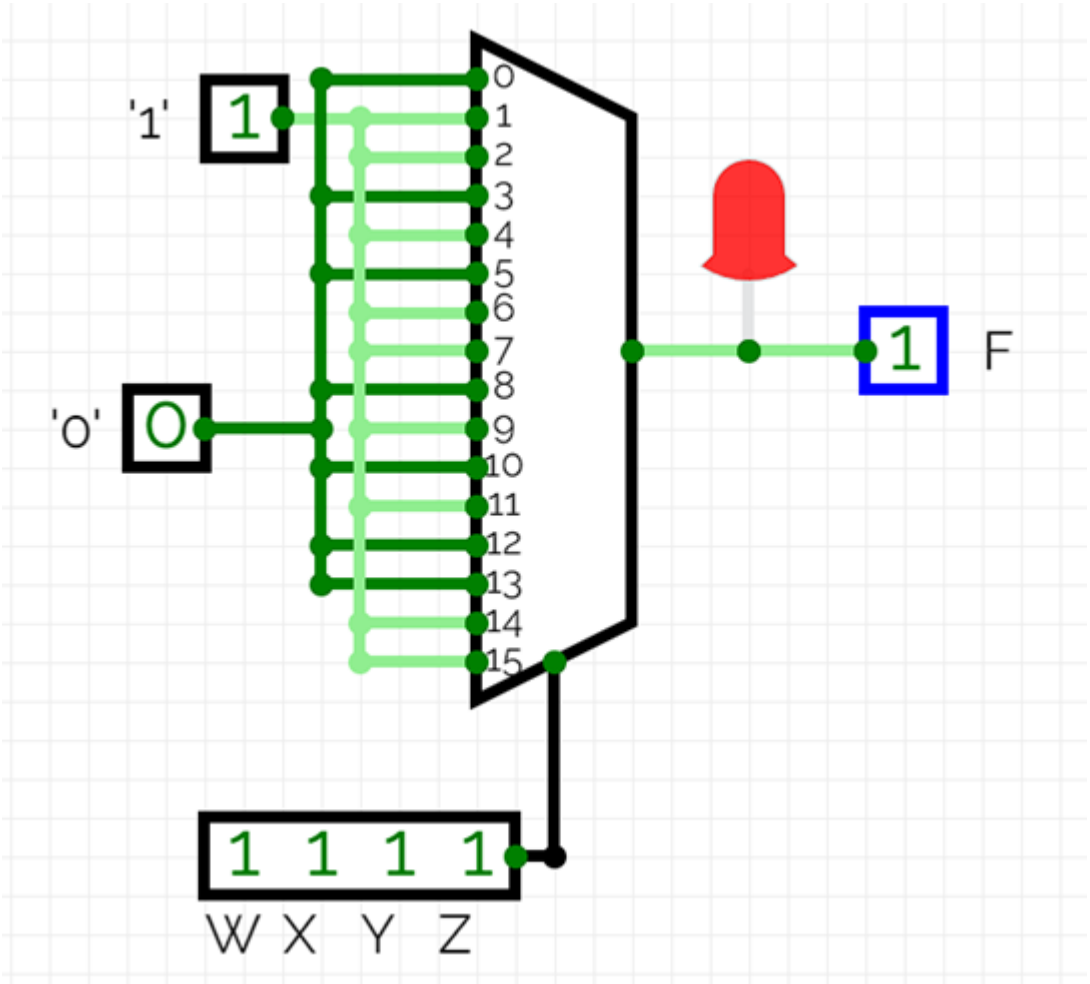
$$F(W, X, Y, Z) = \Sigma\, m(1,\ 2,\ 4,\ 6,\ 7,\ 9,\ 11,\ 14,\ 15)$$

W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	1 F=Z
0	0	1	0	1
0	0	1	1	0 F=Z’
0	1	0	0	1
0	1	0	1	0 F=Z’
0	1	1	0	1
0	1	1	1	1 F=1
1	0	0	0	0
1	0	0	1	1 F=Z
1	0	1	0	0
1	0	1	1	1 F=Z
1	1	0	0	0
1	1	0	1	0 F=0
1	1	1	0	1
1	1	1	1	1 F=1

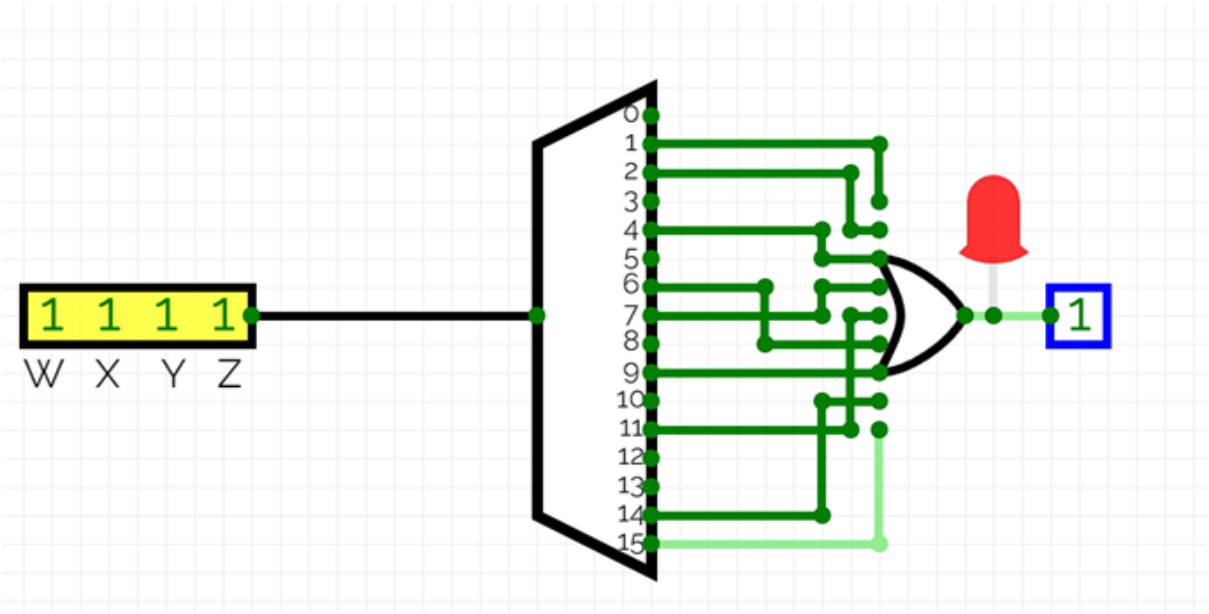
I. Using 8×1 MUX and the needed logic gates



II. Using 16 ×1 MUX and the needed logic gates



III. Using a suitable decoder and an OR gate



5. Design code converter circuits for the following problems.

I. 3-bit Gray-to- binary code converter

Gray Code	Binary
000	000
001	001
011	010
010	011
110	100
111	101
101	110
100	111

g2/g1g0	00	01	11	10
0	0	0	0	0
1	1	1	1	1

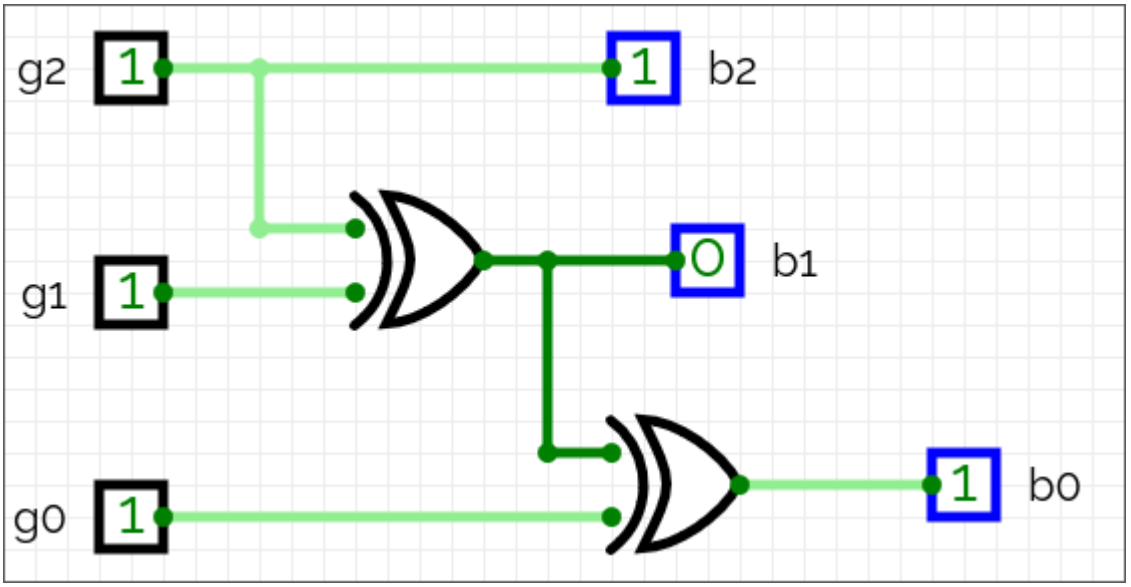
$b2 = g2$

g2/g1g0	00	01	11	10
0	0	0	1	1
1	1	1	1	1

$b1 = g1 \oplus b2$

g2/g1g0	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$b0 = g0 \oplus b1$



II. 3-bit Binary-to-Gray code converter

Binary b2b1b0	Gray Code g2g1g0
000	000
001	001
010	011
011	010
100	110
101	111

110	101
111	100

b2/b0b1	00	01	11	10
0	0	0	0	0
1	1	1	1	1

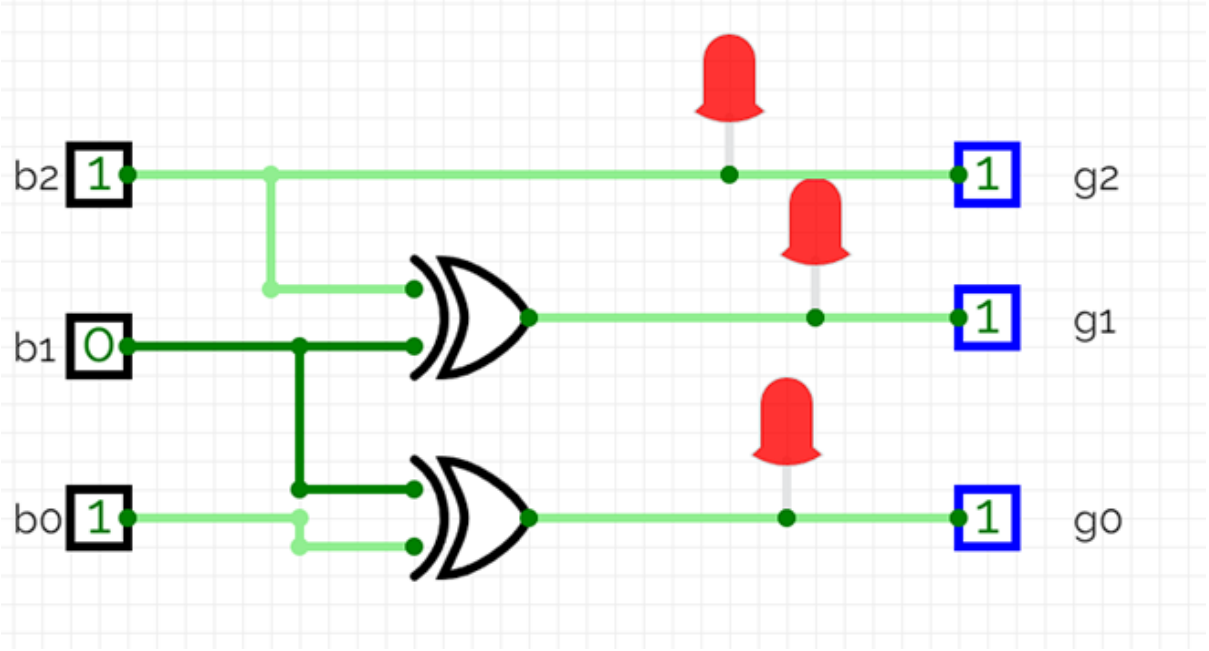
$g2 = b2$

b2/b0b1	00	01	11	10
0	0	0	1	1
1	1	1	0	0

$g1 = b1 \oplus g2$

$g0 = b0 \oplus b1$

b2/b0b1	00	01	11	10
0	0	1	0	1
1	0	1	0	1



III. (8 4 -2 -1) BCD code to (Excess 3) BCD code converter

INPUTS				OUTPUTS			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	1	1	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	0	1	1	1	0	0	0
1	0	1	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	0	0	1	0	1	1
1	1	1	1	1	1	0	0

AB/CD	00	01	11	10
00	0	X	X	X
01	0	0	0	0
11	X	X	1	X
10	1	1	1	1

$W = A$

AB/CD	00	01	11	10
00	0	X	X	X
01	1	1	1	1
11	X	X	1	X
10	0	0	0	0

$X = B$

AB/CD	00	01	11	10
00	1	X	X	X
01	1	1	0	0
11	X	X	0	X
10	1	1	0	0

$Y = C'$

AB/CD	00	01	11	10
00	1	X	X	X
01	1	0	0	1
11	X	X	0	X

10	1	0	0	1

$Z = D'$