SENSING GMSL Video Capture Card Q&A

1. Product user manual

【CoaxCapture】 GMSL Video Capture Card_User Maunal_V1.2_EN.pdf

2. Driver package download

	Content	
Supported kernel versions of the driver package	Support kernel version 5.xx.xx Kernel version 6.xx.xx is not currently supported	
Driver package download link	pcie_v4l2_sdk_ubuntu_SHAb57105dd-20240913_def.zip	
OpenCV usage related	SENSING CCG3 Collection Card OpenCV Application Process (Q&A)	

3. Capture card adaptation checklist?

CCG3 capture card compatible camera list

4. Error reported when executing step 1. How to solve it?

Before using the driver, you need to compile it. The `Driver` directory contains a `Makefile` that can build both the driver and application programs. You can either build the entire project using the top-level `Makefile` , or you can navigate to individual directories and compile them separately.

To build the driver:

代码块

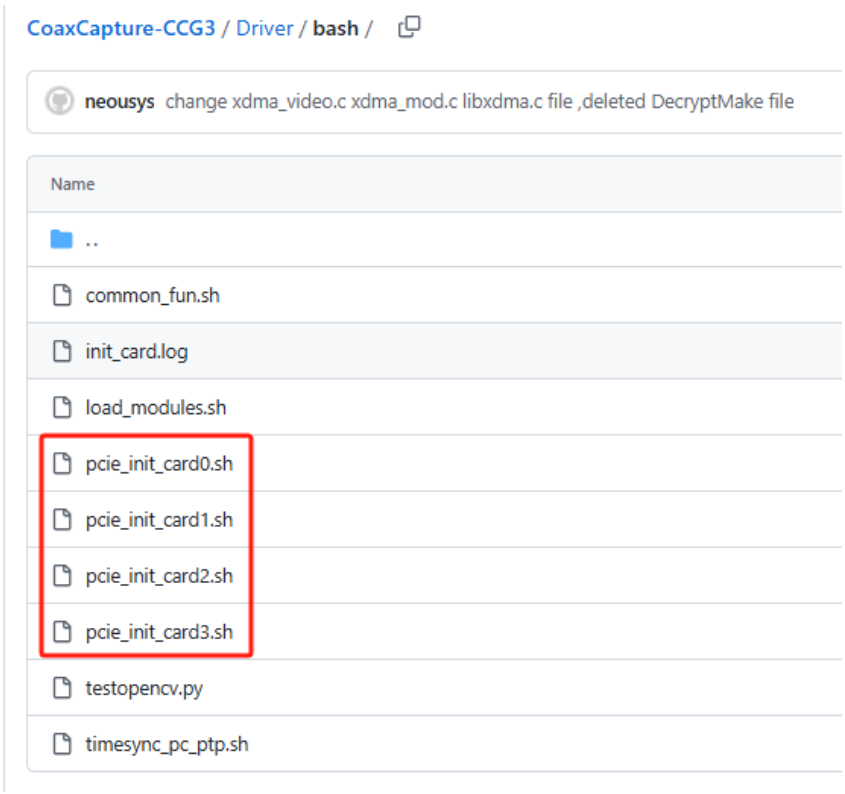
```
1  make
```

If you need to clean the build directory and rebuild from scratch:

```
代码块
1   make clean
2   make
```

5. How to configure the parameters in the initialization script when the CCG3 Card is connected to different models of cameras?

A: When connecting different cameras, the corresponding configuration files are changed through the following pcie_init_cardx.sh .



For example pcie_init_cardx.sh in the last part of the document,

camera_serdes_type[0]=1

value:

0 : The GMSL camera value is written as "0" to indicate that it is connected to the SENSING GMSL camera

1 : GMSL2 (6G) camera value Write "1" to indicate that it is connected to the camera of SENSING GMSL2

2 : GMSL2F (3G) camera value Write "2" to indicate that it is connected to the camera of SENSING GMSL2F

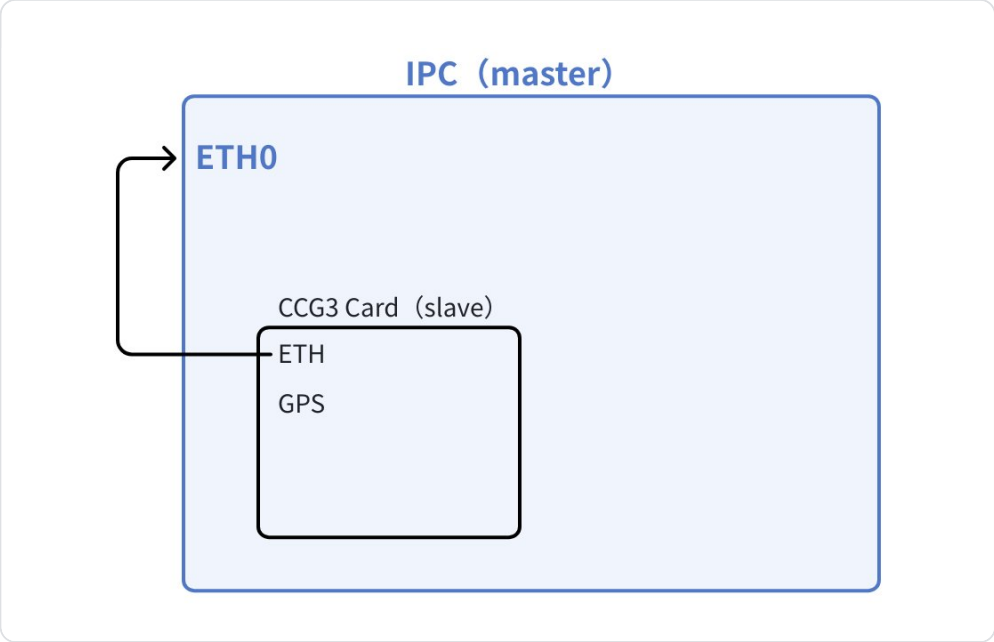
```
代码块
```

```
<文件名：pcie_init_cardx.sh>

#camera 0-7 value: 0:GMSL camera  1:GMSL2(6G) camera  2:GMSL2F(3G) camera
camera_serdes_type[0]=1
camera_serdes_type[1]=1
camera_serdes_type[2]=1
camera_serdes_type[3]=1
camera_serdes_type[4]=1
camera_serdes_type[5]=1
camera_serdes_type[6]=1
camera_serdes_type[7]=1
camera_serdes_cfg ${camera_serdes_type[@]}
echo "Serdes Params Init Processed!"
```

6. How to synchronize the image capture card?

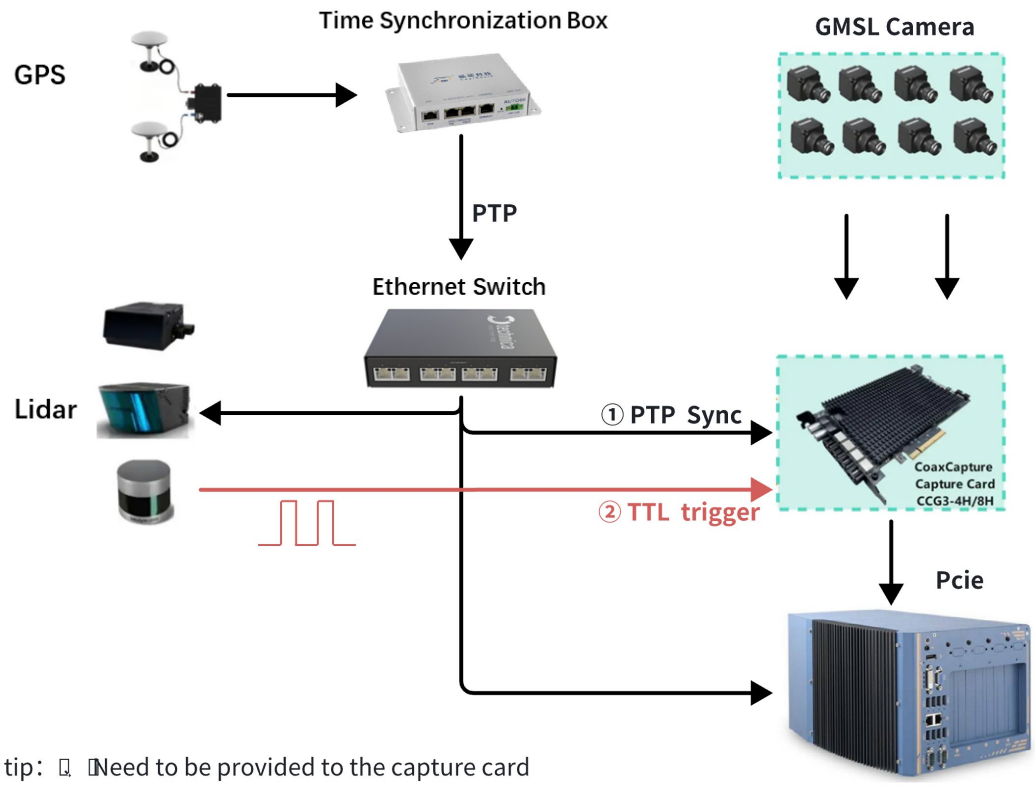
Answer:

Scheme one (the simplest scheme): Operation Instructions for Direct Connection between [SENSING CCG3] and [IPC] - PTP Time Synchronization



Option 2:

Detailed instructions can refer to this document: SENSING CCG3 Image Capture Card] Time Synchronization Through External PTP Operation Instructions V1.2



The overall framework diagram of the system is shown above. The GPS and Time Synchronization Box provide a unified time reference for the entire system through the PTP protocol. This time will be given to the LiDAR, CCG3 Card, and industrial computer through the PTP protocol. In this way, the time source of the entire system is unified. Then, through an external TTL trigger (as shown in red above), it is connected to the GPS interface of the CCG3 Card, which can trigger synchronous multi-channel cameras at the same time.

7. Trigger function:

7.1 TTL(PPS) trigger usage method 1:

The CCG3 Card [GPS] interface defines the following two interfaces (**red, green**), which are used to access an external TTL trigger square wave. And configure the corresponding script parameters.

The GPS on the baffle is an aviation socket for connecting GPS signals. It needs to be connected with the aviation plug end of the cable in the following diagram. Note that the red point of the plug corresponds to the red point of the socket. The other end of the cable is defined in the following diagram:

Red	White	Green	Blue	Black	Bold Black
PPS Signal	UART_RX	GND	None	UART_TX	Enclosure

pcie_init_cardx.sh>

```
# Trigger mode config {0:no trigger; 1:reserved; 2:inner trigger; 3:external trigger}
card_trigger_signal_mode                "3"

# card external signal input fps config.
# Camera external output fps config.
# The following two configurations are valid only when card_trigger_signal_mode is "3".
card_external_signal_input_fps          "1" Hz
camera_external_output_fps              "20" Hz

# Camera inner output fps config
camera_inner_output_fps                 "30" Hz
```

7.2 TTL(internal） trigger usage method 2:

If there is no external TTL trigger , the CCG3 Card can also generate a variable TTL trigger internally (only applicable to camera synchronization on a single CCG3 Card), which can be flexibly set through the parameters in the script (the red settings below: indicates that the CCG3 Card generates a 30hz synchronous TTL signal internally).

pcie_init_cardx.sh>

```
# Trigger mode config {0:no trigger; 1:reserved; 2:inner trigger; 3:external trigger}
card_trigger_signal_mode                "2"

# card external signal input fps config.
# Camera external output fps config.
# The following two configurations are valid only when card_trigger_signal_mode is "3".
card_external_signal_input_fps          "1" Hz
camera_external_output_fps              "20" Hz

# Camera inner output fps config
camera_inner_output_fps                 "30" Hz
```

8. Timestamp problem?

Answer: The specific explanation is as follows:

- Because the module itself has no concept of time, that is, it does not synchronize or obtain external time information, so it will not have a timestamp.
- The timestamp used by actual customers is the time on the platform (industrial computer or PTP) obtained by the CCG3 Card. In principle, after the CCG3 Card receives each frame of image data, it will put the time information obtained from the platform at this moment into the corresponding frame of image data. This time source can be the time when the external trigger signal rising edge arrives (default setting), or the time after the CCG3 Card receives a complete frame of image (parameter setting).
- To view this timestamp synchronously, you can refer to the V4l2 framework (as shown in the standard instructions below). Each frame of image data will have a structure array for storing time information.

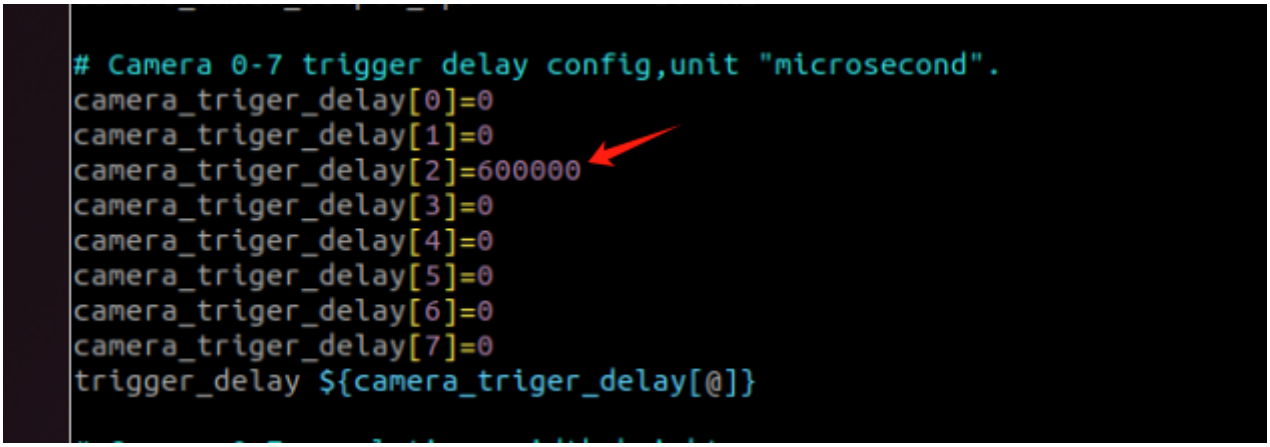
If your problem is don't know how to get the timestamp.
You can reference to the v4l2-ctl tools source code is public.

Current the timestamp is Monotonic mode if you want to change it you have to modify the vi4_fops.c

```
nvidia@nvidia-desktop:~$ v4l2-ctl --stream-mmap --stream-count=3 -d /dev/video0 --verbose
VIDIOC_QUERYCAP: ok
VIDIOC_REQBUFS: ok
VIDIOC_QUERYBUF: ok
VIDIOC_QBUF: ok
VIDIOC_QUERYBUF: ok
VIDIOC_QBUF: ok
VIDIOC_QUERYBUF: ok
VIDIOC_QBUF: ok
VIDIOC_QUERYBUF: ok
VIDIOC_QBUF: ok
VIDIOC_STREAMON: ok
        Index     : 0
        Type      : Video Capture
        Flags     : mapped
        Field     : None
        Sequence  : 0
        Length    : 10450944
        Bytesused: 10450944
        Timestamp: 73428.009795s (Monotonic, End-of-Frame)

        Index     : 1
        Type      : Video Capture
        Flags     : mapped
```

9. How to set the value of delay time?

Answer: It should be less than one frame time, for example, 3ms. Now it is 600ms, which is incorrect.



10. Can the CCG3-8H model's 8-channel CCG3 Card be connected to a PCIE x4 bus? Is the CCG3-4H model's 4-channel CCG3 Card an x4 or x8 bus?

Answer: The CCG3 Cards are all PCIe Gen3.0 * 8lane electrical signals (x8 bus), which need to be inserted into a slot with a width of at least x8. The electrical signal can be * 4lane, but the bandwidth will be reduced.

11. Does the SENSING image CCG3 Card need an external trigger signal to support the external trigger of the camera?

Answer: Both external and internal triggers are supported. If there is an external trigger signal, you can directly access the external signal through the following GPS port (the definition of GPS port can be found in the user manual). If there is no external signal, the CCG3 Card itself can also generate a trigger synchronization signal, which can be set in our driver lighting script.

12. When the capture card is connected to multiple cameras, is there a requirement for resolution and frame rate, such as whether it can be mixed with arbitrary resolution?

Answer:The resolution supports the current SENSING 1 - 8M cameras。 A, B, C, D, E, F, G, and H on the baffle correspond to the 8 cameras numbered 0, 1, 2, 3, 4, 5, 6, and 7. "Route A" refers to the route close to the aviation socket, and the other routes are adjacent to it in sequence. It should be noted that A(0) and B(1) must be connected to the same type of camera, C(2) and D(3)

must be connected to the same type of camera, E(4) and F(5) must be connected to the same type of camera, and G(6) and H(7) must be connected to the same type of camera.

13. Whether the bandwidth is sufficient when six 2MP are connected, and whether there is a calculation formula for PCIE demand bandwidth and video stream bandwidth?

A:The following is the maximum bandwidth support of the CCG3 capture card:

	PCIe protocol
	pcie3.0
x4lane	Max 8M camera 30fps x 4 Max 3M camera 30fps x 8
x8lane	Max 8M camera 30fps x 8

a. Recommended value, industrial computer in addition to the CCG3 Card, camera, and do some display, run other programs occupy bandwidth, occupy memory, bandwidth can reach 60% -70% of the following data. (The following red is the theoretical maximum value, green is the recommended maximum value)

pcie2.0

X4lane: PCIe bus bandwidth 2GB/s * 70% = 1.4GB/s

X8lane: PCIe bus bandwidth 4GB/s * 70% = 2.8GB/s

pcie3.0

X4lane: PCIe bus bandwidth 3.9GB/s * 70% = 2.7GB/s

X8lane: PCIe bus bandwidth 7.8GB/s * 70% = 5.4GB/s

b. Each camera occupies bandwidth

	Example	**Lane Rate**	**Occupy bandwidth (30Hz)**	**Occupy bandwidth (20Hz)**	**Occupy bandwidth (10Hz)**	**Remarks**	**Calculation example**
SENSING 8M camera	AR0820 full resolution	**1188 Mbps/lane**	**594 MB**	**396 MB**	**198 MB**	**Lane Rate * 4/8 = Bandwidth (MB)**	Bandwidth required for 8 SENSING 8M cameras at 30Hz: 594Mx8 = 4.7Gbps < 5.4Gbps（pcie3.0 * 70%）
SENSING 5M camera	IMX490 full resolution	**758.4 Mbps/lane**	**379.2 MB**	**252.8 MB**			
SENSING 3M camera	ISX031 full resolution	**462 Mbps/lane**	**231MB**	**154MB**			
SENSING 2M camera	AR0233	**297 Mbps/lane**	**148.5 MB**	**99 MB**			

14. The PPS + NMEA timing reserved for the CCG3 Card. Are there any special requirements for these two signals?

A: It is not recommended to use the CCG3 Card as the master timing .

15. Is the reserved gPTP used as the Master side or the Slave side?

Answer: Slave side.

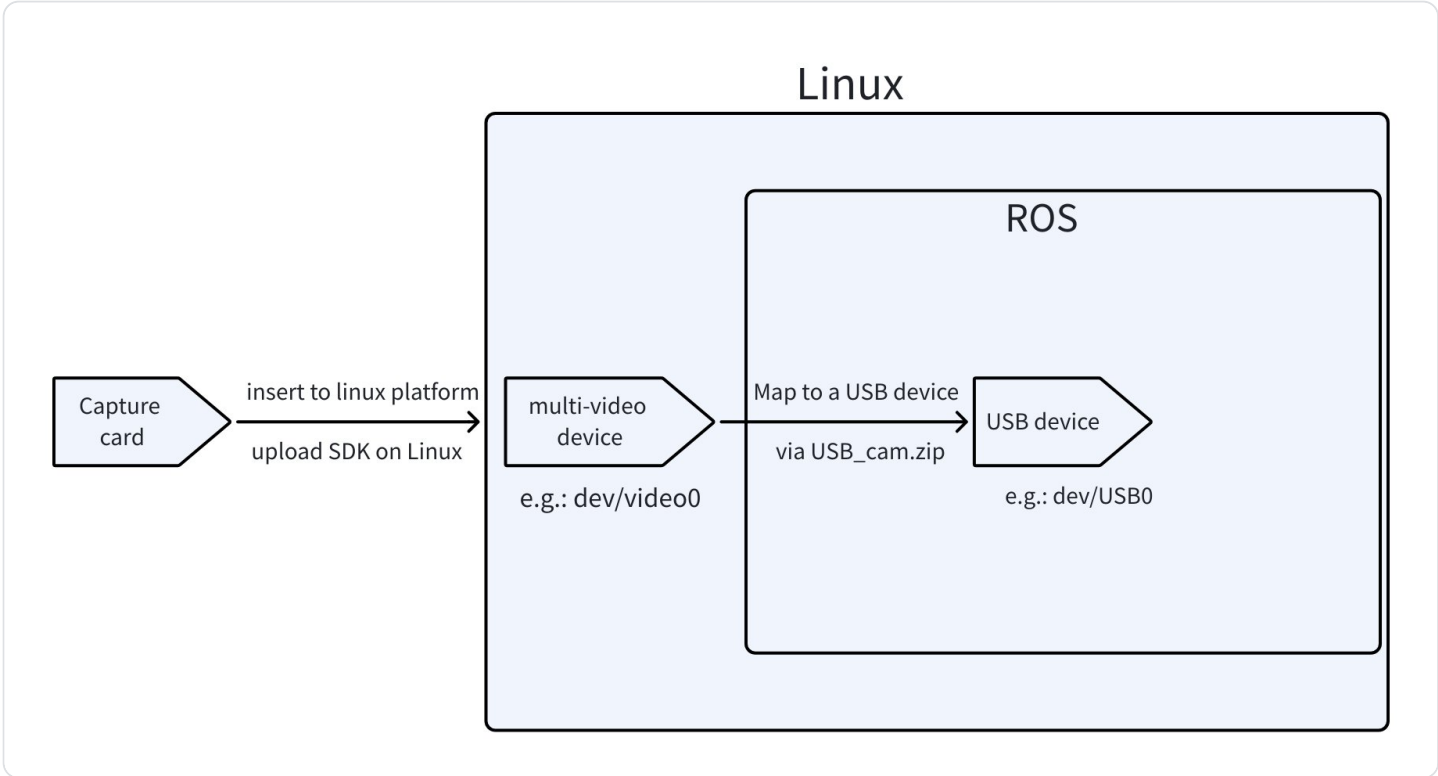
16. Our software is currently using ROS2 Iron + Ubuntu 22.04. We may upgrade to Ubuntu 24.04 and later versions of ROS2?

A : Currently supports 18.04, 20.04, 22.04 (can only support the following 6.xxx (starting with 5.xxx)), temporarily does not support 24.04 .

17. Is there a demo program for ROS2 ?

Currently, we are not developing the ROS application layer. You can refer to the ROS found online below for use. The theoretical usage is to install the ROS-related drivers and dependencies, use the code below, change the corresponding resolution and format in the code, and then map the video device in the capture card to a USB device that can be recognized at the ROS level for use.

usb_cam.zip



18. Are drivers currently available for Ubuntu 22 or 24? Are there any plans to support these versions in the future?

A: Currently, the driver is adapted according to the kernel version. Kernel version 5.xx.xx is supported, but kernel version 6.xx.xx is not currently supported.

19. Is the internal program update of CCG3 Card supported?

1. Ping board 192.168.2.11 to ensure that the board and PC network is connected.
2. Copy the upgrade script pcie_zu-update.sh and firmware pcie_zu_fw - 1.3.51 - 20230401.tar.gz to your PC, then execute the following command to upgrade the firmware:

```
sudo ./pcie_zu-update.sh pcie_zu_fw-*.tar.gz
```

pcie_zu_fw-1.3.58-20240529-YUV.tar.gz
33.34MB

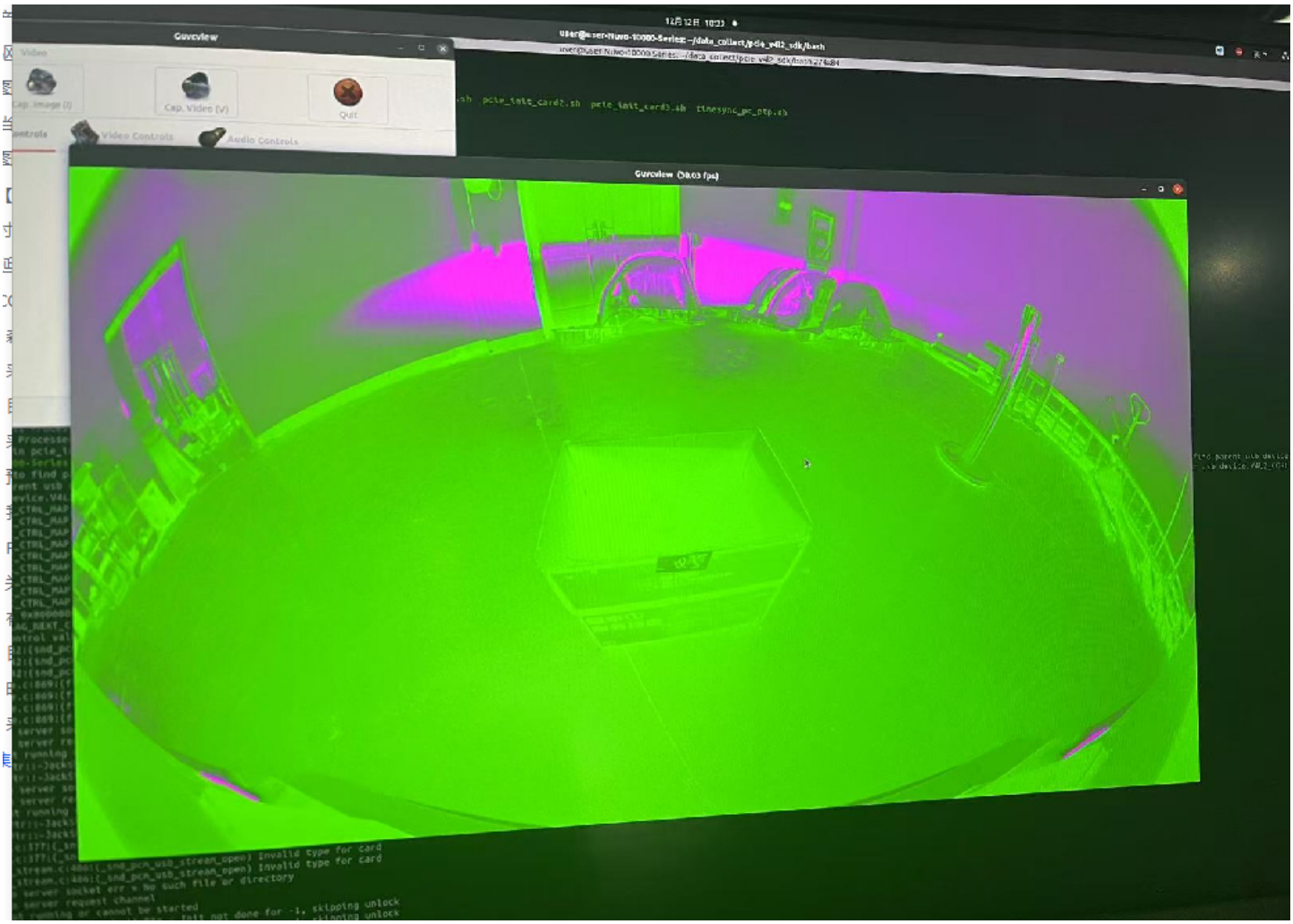
Please refer to the following image for firmware upgrade.

```
ubuntu@ubuntu-MS-7D42:~/sensing/ota/tools$ sudo ./pcie_zu-update.sh ../pcie_zu_fw-1.3.40-20221120-RC7.tar.gz
[sudo] password for ubuntu:
./pcie_zu-update.sh VER: v1.2
ota package: /home/ubuntu/sensing/ota/pcie_zu_fw-1.3.40-20221120-RC7.tar.gz

> 2, check if exist only one ota file

> 3, copy update file to /ldc partition
pcie_zu_fw-1.3.40-20221120-RC7.tar.gz

> 4, run update script in pcie_zu
---------time: 20180309_203534---------

ota-update.sh VER: v1.8

>>1, check if exist only one ota file
>>1.1, find ota file /ldc/pcie_zu_fw-1.3.40-20221120-RC7.tar.gz
BOOT.BIN
boot.scr
tar: BOOT.BIN: time stamp 2022-11-20 08:12:44 is 148304228.567866029 s in the future
image.ub
tar: boot.scr: time stamp 2022-09-30 15:19:34 is 143923438.567531409 s in the future
pcie_zu_ota.json
tar: image.ub: time stamp 2022-11-20 08:12:24 is 148304207.271726507 s in the future
tar: pcie_zu_ota.json: time stamp 2022-11-20 08:13:43 is 148304286.271440817 s in the future

>>2, check ota files md5
>>2.1, new ota version: 1.3.40-20221120-RC7

>>2.2, check md5 boot.scr
>>2.2.1, NEW_SCR_MD5: befa0e2955eea1a7cdeb27bd98139837
>>2.2.2, BASE_SCR_MD5: befa0e2955eea1a7cdeb27bd98139837

>>2.3, check md5 image.ub
>>2.3.1, NEW_IMG_MD5: 600ba3f86eacc2785223523356835dff
>>2.3.2, BASE_IMG_MD5: 8a8b7e98593afae4c869330e8839fa3b

>>2.4, check md5 BOOT.BIN
>>2.4.1, NEW_BOOT_MD5: d504ed3773b6598e93b45bd4c73247f8
>>2.4.2, BASE_BOOT_MD5: 96a8d290a5b54037057ae6a18b0aeafb

>>3, check if need modify
```

🥖 Note: pcie_zu-update.sh if there is no execution permission (only rw without x), add **bash** when executing the upgrade script, that is, sudo bash./pcie_zu-update.sh pcie_zu_fw - * .tar.gz.

3. After the upgrade is successful, restart the industrial computer, ensure that the board is powered off, and power on again.

20. How to change the normal green image of the CCG3 Card?



As shown in the above figure, it can be solved by changing the video_output_yuv_format field below. The first column represents each channel, and the second column represents the image format displayed by the channel. It can be modified to "UYVY" or "YUYV".

```
timestamp_src 1

# Camera input format conversion config {0 or 1}
camera_input_format_conversion[0]=0
camera_input_format_conversion[1]=0
camera_input_format_conversion[2]=0
camera_input_format_conversion[3]=0
camera_input_format_conversion[4]=0
camera_input_format_conversion[5]=0
camera_input_format_conversion[6]=0
camera_input_format_conversion[7]=0
camera_format_set ${camera_input_format_conversion[@]}

#Camera anc config {0 disable  anc or 1 enable anc}
camera_anc_enable[0]=0
camera_anc_enable[1]=0
camera_anc_enable[2]=0
camera_anc_enable[3]=0
camera_anc_enable[4]=0
camera_anc_enable[5]=0
camera_anc_enable[6]=0
camera_anc_enable[7]=0
camera_anc_set ${camera_anc_enable[@]}

# Video output yuv format  config {"YUYV" or "UYVY"}
video_output_yuv_format 0 "UYVY"
video_output_yuv_format 1 "UYVY"
video_output_yuv_format 2 "UYVY"
video_output_yuv_format 3 "UYVY"
video_output_yuv_format 4 "UYVY"
video_output_yuv_format 5 "UYVY"
video_output_yuv_format 6 "UYVY"
video_output_yuv_format 7 "UYVY"
```

If it is the second card video8-video15:

```
# Video output yuv format   config {"YUYV" or "UYVY"}
video_output_yuv_format 8 "UYVY"
video_output_yuv_format 9 "UYVY"
video_output_yuv_format 10 "UYVY"
video_output_yuv_format 11 "UYVY"
video_output_yuv_format 12 "UYVY"
video_output_yuv_format 13 "UYVY"
video_output_yuv_format 14 "UYVY"
video_output_yuv_format 15 "UYVY"
```

21. CCG3 Card i2c access camera method?

Method 1: When accessing the ETH network port of the CCG3 Card, standard I2C commands can be used.

The I2C usage method of [SENSING CCG3 Image Capture Card]

Method 2: When unable to access the ETH network port of the CCG3 Card, you can use the I2C command encapsulated on the CCG3 Card.

Usage of I2C Read-Write Interface of SENSING CCG3 Image Capture Card

22. Does the CCG3 Card driver support gstreamer?

A: Not currently supported.

23. How to modify the timestamp representative value

(1) In the script pcie_init_card0.sh, the configuration is as follows:

```
# Camera time stamp  source {0: vsync; 1:fsync; 2:frame transfer done; }
timestamp_src 1
```

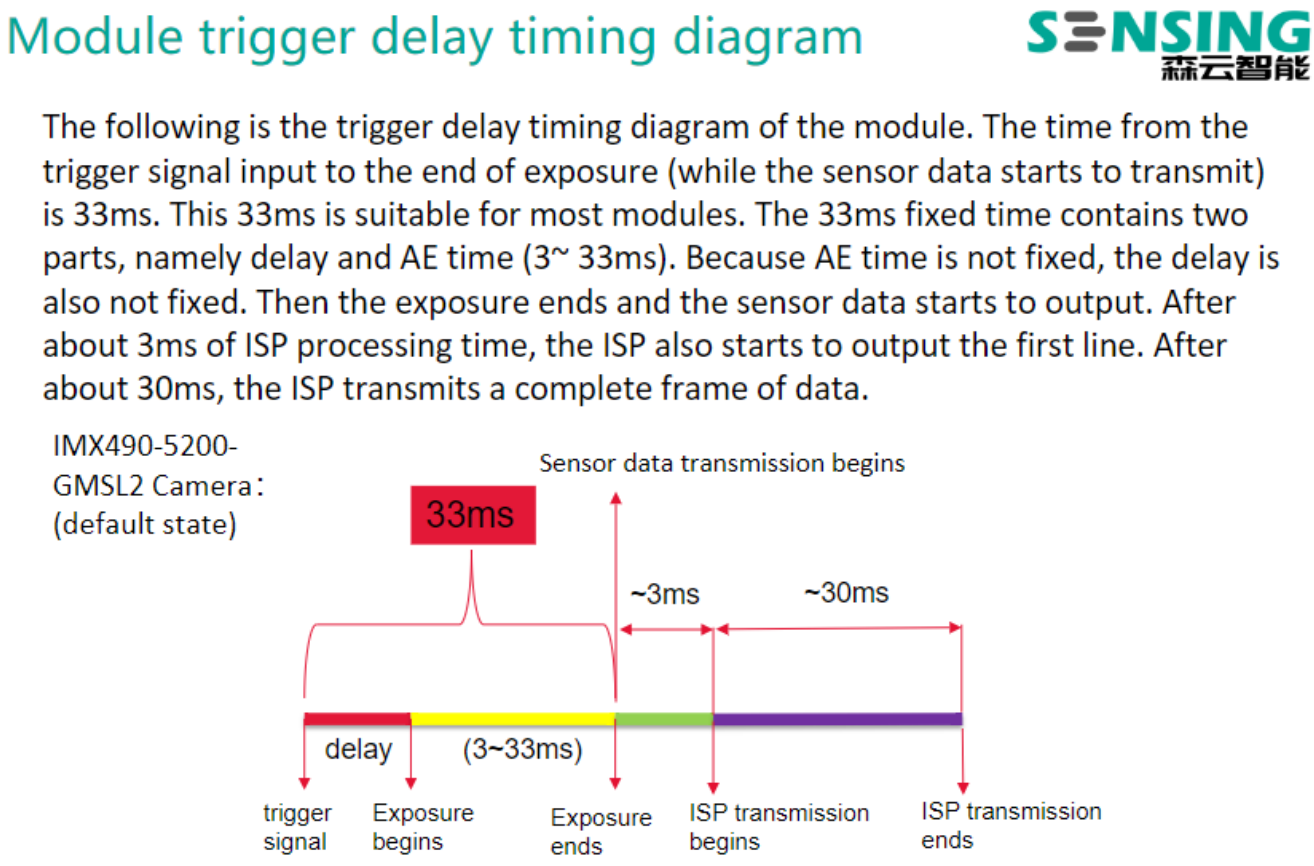
1. Trigger time;

0: The moment when the first line of ISP starts outputting;

2: ISP last line output end time.

Principle explanation: The specific parameter principle described above is shown in the following figure, which refers to the total time delay from the triggering moment of the module

to the end of the ISP output. The timing delay varies among different modules, and is for reference only. See the figure below.



After setting the function items to match the camera in this script, execute the pcie_card * .sh script in the bash directory to initialize all channel cameras

24. Can't open the device node in Opencv in Python?

A: With the old version of the SDK package, the detailed operation can refer to the description of this document: SENSING CCG3 Collection Card OpenCV Application Process (Q&A)

25. Will additional latency be introduced when the application layer reduces the frame rate through queuing/dequeuing mechanisms?

Answer:The queue mechanism will introduce a delay increment proportional to the queue depth when reducing the frame rate.

Reason:

a. **Load impact of decoder queues: High frame rate (HFR) and high resolution (UHD) reduce inter-frame spacing and increase the arrival rate of decoder queues. If decoding speeds do not match, queue build-up results in a significant increase in tail latency.**
b. **Frame queues usually store pending frames in the order of receipt. When there are outdated frames at the front end of the queue that have not been processed for a long time, the submission of subsequent new frames will be forcibly blocked, even if these new frames have timed out.**