# Monolithic 3D Integrated Circuits: Recent Trends and Future Prospects

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***Abstract*—Monolithic 3D integration technology has emerged as an alternative candidate to conventional transistor scaling. Unlike conventional processes where multiple metal layers are fabricated above a single transistor layer, monolithic 3D technology enables multiple transistor layers above a single substrate. By providing vertical interconnects with physical dimensions similar to conventional metal vias, monolithic 3D technology enables unprecedented integration density and high bandwidth communication, which plays a critical role for various data-centric applications. Despite growing number of research efforts on various aspects of monolithic 3D integration, commercial monolithic 3D ICs do not yet exist. This tutorial brief provides a concise overview of monolithic 3D technology, highlighting important results and future prospects. Several applications that can potentially benefit from this technology are also discussed.**

***Index Terms*—Three-dimensional integrated circuits, monolithic integrated circuits, through-silicon vias, fabrication, physical design, thermal management, testing, neural networks, security, computer applications.**

## I. Introduction

As TWO-DIMENSIONAL geometry scaling of conventional transistors is coming to an end, International Roadmap for Devices and Systems (IRDS) predicts that monolithic 3D integration technology (here termed as Mono3D technology) will be one of the critical performance boosters [1]. Mono3D technology represents a radical departure from conventional fabrication technologies where transistors are first patterned via the front-end-of-line (FEOL) portion of the process, followed by the patterning of multiple interconnect layers via the back-end-of-line (BEOL) process. Unlike other vertical integration technologies, manufacturing multiple transistor layers on a single substrate in Mono3D technology exhibits unique opportunities for providing extremely dense ICs.

In the past two decades, the semiconductor industry has witnessed significant improvements in various forms of vertical integration technologies, such as the through silicon via (TSV) based 3D integration (also referred to as chip stacking) and lateral integration of multiple dies placed on the same interposer substrate for higher bandwidth communication (also referred to as 2.5D integration). The number of commercial applications that utilize these TSV-based and, relatively, more established forms of vertical integration, has steadily increased. For example, there are commercial FPGAs and GPUs that utilize interposer based 2.5D integration to increase density while significantly reducing the interconnect overhead [2]–[5]. Commercial products of TSV-based systems include primarily memory arrays, such as the Hybrid Memory Cube (HMC) [6] and High Bandwidth Memory (HBM) [7], which are multi-layer DRAM chips. Most recently, commercial integration of multiple logic chiplets has been demonstrated in a face-to-face configuration with TSVs [5].

Although TSV-based 3D technologies enable significant benefits in system-level performance, power consumption, and form factor, compared to typical 2D integration, these technologies suffer from a noticeable asymmetry between the transistor dimensions and the dimensions of the TSVs. The channel length of modern transistors has reached sub-10 nm dimensions, whereas the diameter of modern TSVs is in the range of several micrometers. This large gap is a significant limitation on the density/granularity of TSV-based die stacking. For example, a typical TSV with several micrometers of diameter exhibits a capacitance in the range of tens of femtofarads, which is equivalent to approximately 100 gates (with fanout of two) in a relatively old 45 nm technology node [8], [9]. In the 7 nm technology node, a TSV is equivalent to approximately several thousand gates in terms of load capacitance, thereby consuming significant dynamic power and causing *RC* delay [10]. Monolithic 3D technology mitigates these problems by reducing the dimension of vertical interconnects, referred to as monolithic inter-tier vias (MIVs), down to nanometers, thereby enabling unprecedented levels of integration density and granularity [11]. Recognizing the high potential of Mono3D, this tutorial brief provides a concise overview on multiple facets of monolithic 3D integration technology while outlining existing research directions and highlighting future prospects.

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TABLE I
A QUALITATIVE COMPARISON BETWEEN 2.5D, TSV-BASED 3D, AND MONO3D INTEGRATION TECHNOLOGIES

| Integration technology | Commercial Availability | CAD tools | Design-for-test |
|---|---|---|---|
| INTERPOSER-BASED 2.5D | NVIDIA and AMD GPUs [3], [4], Xilinx and Intel FPGAs [2], [5], Samsung I-Cube [21], TSMC CoWoS and InFO [22], [23]. | Existing 2D CAD tools used for die designs. Chip/package/board co-design for heterogeneous integration under development [24]. | Standardized test-port interface: IEEE 1838 [25], [26]. |
| DIE STACKED 3D | Commercial fabrication for memory stacking [6], [27], Intel's LakeField processor [28] and Samsung's X-Cube [29]. | Various CAD tools developed for 3D design. Chip/package/board co-design for heterogeneous integration under development [30], [31]. | Standardized test-port interface: IEEE 1838 [25]. |
| MONO3D | SRAM arrays and CNFET, NVM integration demonstrated [16], [20]. No commercial production yet. | Tools that are integrated with existing flows [32]–[34] have been proposed, but no standard CAD flow yet. | Low cost dual-BIST DfT architecture proposed for MIV-testing but not standardized [35]. |

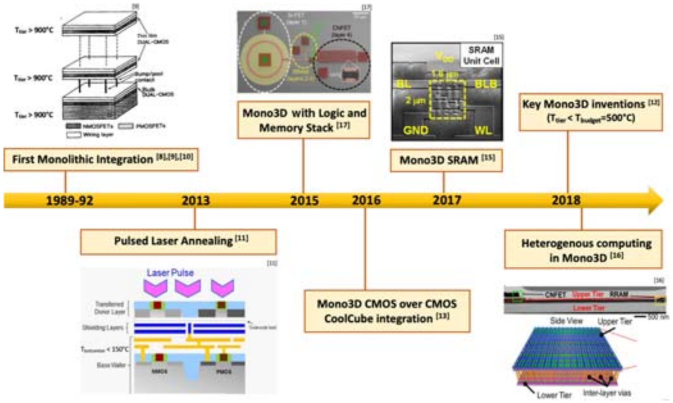
First Monolithic Integration [8],[9],[10]
Mono3D with Logic and Memory Stack [17]
Mono3D SRAM [15]
Key Mono3D inventions [12] ($T_{tier} < T_{budget}$=500°C)
1989-92
2013
2015
2016
2017
2018
Pulsed Laser Annealing [11]
Mono3D CMOS over CMOS CoolCube integration [13]
Heterogenous computing in Mono3D [16]
SRAM Unit Cell
BL
BLB
GND
WL
2 µm
Laser Pulse
CNFET
Upper Tier
RRAM
Lower Tier
Side View
Inter-layer vias

Fig. 1. Chronological timeline of primary developments in the fabrication process of MONO3D ICs.

## II. MONO3D FABRICATION PROCESS

A chronological timeline illustrating the primary developments in the fabrication process of MONO3D technology is shown in Fig. 1. The development of a sequential fabrication process to construct multiple transistor layers on a single substrate dates back to late 80s [12], [13]. These early studies relied on laser beam recrystallization to form multiple silicon-on-insulator (SOI) layers on top of the p-type substrate. A single device layer contained only one type of transistor, thereby reducing the number of process steps related to well formation and ion implantation. Since these layers were subject to 900°C temperature during device fabrication, doped polysilicon interconnects were utilized in these early implementations due to its ability to withstand high temperatures. Correct operation of the devices was demonstrated by measuring I-V characteristics in each layer. However, the SOI devices exhibited approximately 4× higher threshold voltage variation.

A primary challenge in building MONO3D structures is to ensure the reliability of devices within the bottom layer that can be degraded by the temperature and processing time required to fabricate high quality transistors at upper layers. Another related challenge is to manufacture multiple low resistivity interconnect (and low-k dielectric) layers for the first device layer since routability becomes an important concern due to very high density integration. These issues limit the processing temperature of upper layers below 500°C, referred to as the thermal budget constraint.

Several steps in traditional FEOL processes require temperatures much higher than 500°C, such as activation of the implanted impurities and annealing to fix the crystal defects encountered during ion implantation. One approach is to rely on pulsed laser annealing and activation, assuming that the thickness of the transistor silicon layer is sufficiently small (in the range of 20 nm) [14]. In this approach, lasers with pulse widths below 100 ns are used to momentarily increase the temperature of the higher layers above 1400°C. Thin shielding layers are used to ensure that the temperature that diffuses to the bottom layers remains below 150°C. This pulsed laser based recrystallization and activation enables low resistance polysilicon gates for the upper layers [15]. Another key fabrication-level enabler for MONO3D technology is high quality growth of silicon by using low temperature epitaxy [15]. In this approach, traditional surface preparation techniques were replaced with a low temperature process including a combination of dry and wet etch preparation. A silicon epitaxial layer was built with good selectivity and crystallinity at 500°C.

Another risk when fabricating upper layer devices is contamination since the wafer is reintroduced to FEOL processes after a contaminated backend process where interconnects and vias were built. A three step contamination control strategy was proposed [15], consisting of etching the wafer bevel edge (shown to be the most critical contamination source) to remove the deposited metals, decontamination via wet cleaning, and encapsulation of the wafer bevel.

These developments in manufacturing enabled the demonstration of MONO3D ICs with relatively low complexity. For example, transistor-on-transistor integration with alignment accuracy in the range of nanometers was shown [16]. Successful MONO3D integration of an SRAM array with sufficient stability has also been achieved [17], [18]. Finally, carbon nanotube field-effect transistors and non-volatile resistive memory were successfully integrated with conventional silicon based devices on a MONO3D platform [19], [20].

## III. MONO3D DESIGN METHODOLOGIES

In this section, the latest advances related to physical design, thermal integrity, and testing methodologies of MONO3D technology are described. A broad qualitative comparison of these challenges (including commercial status) for 2.5D, TSV-based 3D, and MONO3D integration is provided in Table I.

### A. Physical Design

Over the recent years, developing pseudo-3D tools for monolithic integration has gained significant attention [36]. These studies make some process or technology file

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modifications to “trick” the 2D engine to produce quality 3D designs.

Shrunk-2D (S2D) [32] was the first commercial-quality tool in which the entire design area is shrunk by 50% by scaling the dimensions of the original 2D chip and the standard cells by a factor of $1/\sqrt{N}$, where $N$ is the number of tiers. The metal width and pitch are also scaled by the same factor, keeping the $RC$ per unit length fixed. The 2D P&R engine is applied to this shrunk design before the cells are blown up and partitioned to their respective tiers. This tool, however, does not estimate $RC$ parasitic impedance accurately and also expects the commercial 2D engines to handle dimensions smaller than their capability. Another tool called Compact-2D [33] was proposed with more accurate timing characterization and lesser legalization issues than S2D. However, it does not support simultaneous timing closure for all the tiers, and hence, leading to performance degradation. Alternatively, Cascade2D tool [34] performs a design-aware partitioning at the RTL stage. The placement, routing and timing closure are simultaneous for both the tiers, which significantly improves the timing characteristics of the design, unlike the other two flows.

A detailed comparative study was performed between the three algorithms on RISC-V Rocketcore processor using identical 3D footprints [37]. The comparison showed that though, S2D and Compact-2D have large total negative slacks compared to Cascade2D, the total wirelength and overall power consumption for Cascade 2D was 21.4% and 7.5% greater than conventional 2D, respectively. However, the total wirelength of S2D and Compact-2D was, respectively, 12.2% and 10.5% lower than the conventional 2D. The overall power consumption of S2D and Compact-2D was also shown to be 7.1% and 8% lower than conventional 2D, respectively. This increase in the wirelength and power is attributed to the tier-partitioning strategy and MIV planning strategies in Cascade2D being unsuitable for flattened gate-level designs.

Another important physical design issue in MONO3D ICs is routing congestion since the chip footprint is significantly reduced (20% to 40%), but the overall number of available metal layers does not significantly increase [38]–[40]. This issue was investigated by Yan *et al.* [40], [41] by developing a MONO3D cell library and two-layer PDK in 45 nm technology node [42]. The pull-down nMOS transistors of the cells and the I/O pins are placed on the upper layer whereas the pull-up pMOS transistors are placed on the bottom layer. The connections among the layers are achieved via intra-cell MIVs, thereby permitting the use of existing 2D placement tools. An example is provided in Fig. 2, where a 2D and MONO3D implementations of a 128-point FFT operating at 500 MHz are illustrated. It was demonstrated that increasing the number of routing tracks per cell from 8 to 10 slightly increases the die-level footprint of the 128-point MONO3D FFT core, but reduces the overall wirelength (due to less routing congestion). Furthermore, the timing characteristics are significantly enhanced since the coupling capacitances are reduced. As compared to 2D, a MONO3D FFT core (with 10 routing tracks) reduces the footprint by approximately 37% while also achieving approximately 13% reduction in overall power consumption. Using this library, the effect of successive in-place optimization (IPOs) on partitioned tiers produced either by a greedy bin-based Fidducia-Mattheyses or a displacement-based legaliser is presented [43], where a single BEOL connecting the tiers and few IPOs yield higher PPA for the explored circuits.

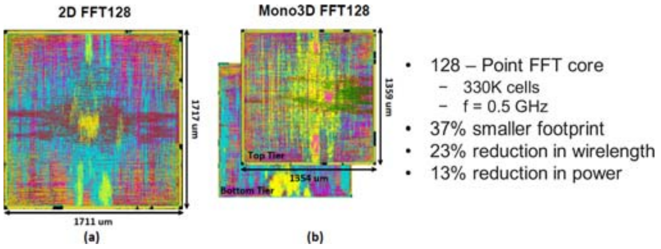

Fig. 2. A fully placed and routed 128-point FFT in 45 nm technology using: (a) conventional 2D, (b) transistor-level MONO3D technology with two layers.

Although there have been several academic efforts to develop complete end-to-end design flows, developing commercially available tools that leverage the integration, power, and performance benefits provided by MONO3D still remains an open problem. Thermal aspects are an integral part of the design process and should be considered while optimizing for other parameters, as explored in the following section.

### B. Thermal Integrity

A major limitation in 3D ICs is effective heat dissipation from tiers away from the heat sink/spreader. MONO3D systems face additional thermal issues due to the higher device integration density, routing congestion, and strong inter-tier thermal coupling. These characteristics further differentiate MONO3D technology from TSV-based 3D ICs. Several works have presented techniques to alleviate thermal challenges in MONO3D systems. Careful design of power delivery networks (PDN) can help reduce chip temperatures by up to 5% [44] while ignoring the effect of PDNs leads to overestimated chip temperatures [45]. Nano-pillars were placed at design time in transistor-level MONO3D systems for heat dissipation from selected hot spot regions, and 53% reduction in temperature was shown through finite element method simulations [46].

A two-tier MONO3D system is modeled by Samal *et al.* [47]. Strong inter-tier thermal coupling (i.e., similar temperature across tiers) is demonstrated due to a thin dielectric in-between and a non-linear regression model is constructed to estimate chip temperatures. However, the lateral heat flow is ignored due to the thin tiers. In comparison, they show that the tier away from the heat spreader for a similar TSV-based system, is hotter than that in the MONO3D system due to higher vertical resistance (since vertical heat flow path is longer) and presence of a thick bonding layer between tiers.

Two-tier MONO3D and TSV-based 3D IC are modeled along with the metal layers [48] using HotSpot-6.0 [49] (an architecture level thermal simulator). Synthetic power profiles are simulated by placing one hot spot at the center of the bottom tier (closer to heat sink) and four hot spots in the upper tier (away from heat sink), each with a power density of 750 W/cm$^2$. The results are shown in Fig. 3. It can be observed that thermal coupling helps in effective heat dissipation of the

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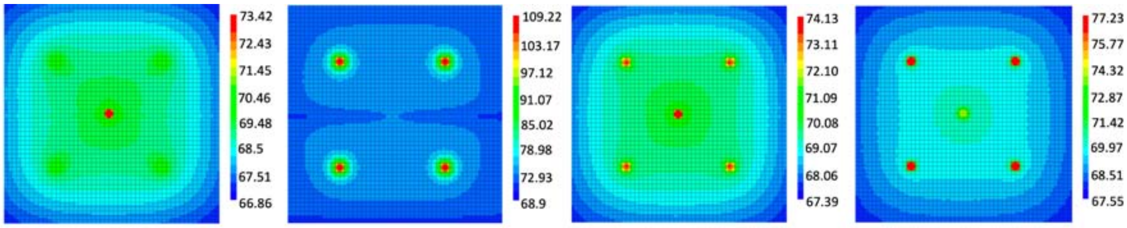

(a) Bottom tier (TSV-based 3D) (b) Upper tier (TSV-based 3D) (c) Bottom tier (MONO3D) (d) Upper tier (MONO3D)

Fig. 3. Thermal maps of the TSV-based 3D and MONO3D ICs.

upper tier to the heat sink in MONO3D (note the lower temperature in Fig. 3(d) than in Fig. 3(b)). Alternatively, thermal coupling may cause hot spots in the upper tier that form similar hot spots in the bottom tier (note the additional hot spots in Fig. 3(c) in comparison to Fig. 3(a)). Higher localization of the hot spots in the MONO3D IC can also be seen, thus demonstrating lower lateral thermal coupling. Several power profiles are also simulated by varying hot spot distribution, size, and area. Despite the limited lateral heat flow, this flow of heat should not be ignored as it may under-estimate hot spots by ≈4°C in tiers away from heat sink. These results demonstrate the specific thermal challenges that should be considered while designing MONO3D ICs to ensure thermal integrity.

### C. Design-for-Test

MONO3D ICs exhibit unique test challenges due to multiple transistor layers and dense MIVs. Aggressive scaling of the thickness of the inter-layer dielectric and the increased densities of MIVs (30 million per mm$^2$) [50] are the primary cause of functional and timing faults in MONO3D systems [51]. Typical fault models for testing the MIVs are similar to the interconnect fault models in 2D ICs and can be broadly categorized as shorts, opens and stuck-at-faults. For the testing of such faults, the conventional ATPG-based methodologies tend to fall short primarily because all the test vectors should be propagated through the multiple tiers and the MIVs, adding significant amount of constraints to the tool, demanding built-in self-test (BIST) solutions for MONO3D technology [52].

A solution was proposed to enhance the observability and controllability of MIVs by using a die-wrapper register cell on both ends of MIV [53]. The BIST technique proposed by Koneru *et al.* employs interface scan cells connected to twisted-ring counter on a dedicated test layer targeting the testing of opens and shorts in MIVs [54]. The cost per die savings were inferred to be as high as 40% when compared to the similar technique employed for TSV-based 3D IC that mandates the insertion of die wrapper register. However, both of these methods incur a significant area overhead. Recently, a low-cost dual-BIST architecture was proposed using XOR gates to detect opens, shorts and stuck-at faults [52]. In that work, only two test patterns are used for exhaustive testing of all MIV fault scenarios combined and the test responses are compacted using 2-bit signatures at the output. The maximum area and power overheads of the BISTed designs reported are 2.6% and 9% when compared to a standard design [35].

The TSV-based pre-bond strategies cannot be adapted to MONO3D testing predominantly because bare MIVs cannot be exposed and the existing wafer-probing techniques cannot support the MIV pitch that is on the order of 100 to 200 nm [52]. The post-bond strategies also cannot be extended to MONO3D because of the significant increase in the number of MIVs used. Consequently, the above mentioned works have proposed several novel BIST solutions for MONO3D technology, which continues to be an active field of research.

## IV. EMERGING APPLICATIONS FOR MONO3D

### A. Near- and In-Memory Computing

Computing near- or in-memory is a promising and popular approach to surmount the challenges relating to the well-known “memory wall” issue. Consequently, several methods that enable computing in the DRAM memory chips [55], [56] or near non-volatile memories [57] have been developed. The high MIV density of MONO3D circuits makes them well suited for these computing paradigms.

Due to the physical proximity of the device layers in MONO3D circuits, the two aforementioned approaches are hardly distinguishable. Rather a better way to discern the use of these two paradigms in MONO3D circuits is to observe the related partition granularity [58]. Thus, near-memory computing is better served by MONO3D technology if block-level partition is utilized. Alternatively, in-memory computing is underpinned by transistor-level integration. The former exploits the massive interconnect density enabled by the MIVs and the low delay of these interconnects. On the other hand, the latter can utilize one of the device layers to deploy the additional bit-wise logic operations without disrupting the density of the memory array and maintaining most of the original performance.

A recent example of near-memory computing with MONO3D combines a processing tier with a layer of resistive RAM (ReRAM) on top, extending the RADAR accelerator architecture in three physical dimensions. The use of MONO3D improves the execution of the Smith-Waterman algorithm by three orders of magnitude compared to 2D implementation [59], while an effort to speed up the same algorithm on a FPGA [60] yields a considerably lower improvement of 330×.

Alternatively, a cell enabling in-memory computing through transistor-level partitioning has been presented [61]. The cell consists of nine transistors (9T) and can implement

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NAND/AND, NOR/OR, and XOR/XNOR operations, in addition to storing a bit, within a memory cycle. The key idea of this 9T cell is to maintain the storage (SRAM) cell in one of the device layers and implement the remaining three transistors used for the logic operations in the upper device layer. Although this structure does not result in the minimum footprint, a savings of 51% is achieved as compared to a 2D implementation of the same 9T cell. Furthermore, since the memory array is not disrupted, the memory density compared to a 2D SRAM array remains unaltered. These recent examples demonstrate the presently unexplored potential of using MONO3D for upcoming non von Neumann architectures.

### B. Deep Neural Networks

Deep Neural Networks (DNNs) have become popular for a wide range of applications, such as image recognition or speech recognition [62]. DNN accelerators are also designed to satisfy the high throughput and memory bandwidth demands of DNNs [63]–[66]. However, high energy consumption in DNNs (due to heavy computation and data movement) is a major design concern. Since MONO3D offers high interconnect density and power/performance benefits over 2D, there is a growing interest towards designing energy-efficient MONO3D DNN accelerators.

Yu *et al.* reduced the memory footprint of CNNs by encoding the activation and weight for sparsity, and then interfacing the CNN accelerator with a MONO3D non-volatile RAM to significantly improve bandwidth using MIVs [67]. The reported average improvement in execution time, power dissipation, and energy efficiency are up to 16×, 4.5×, and 69×, respectively, for CNN training/inference w.r.t. Nvidia GeForce GTX 1080 Ti. While some works (e.g., [67], [68]) have utilized the high-density MIVs in a block-level integration to highlight the benefits of MONO3D, other works (e.g., [69], [70]) have used various partitioning techniques to achieve an energy-efficient ASIC design. Chang *et al.* have performed gate-level partitioning for the MAC units and block-level for the SRAMs for two DNN architectures [69]. 22.3% and 6.2% improvement in iso-performance power consumption and performance, respectively, were shown against a 2D baseline. Do *et al.* designed a two-layer GPU scratchpad memory using MONO3D to enable fast SRAM access by enabling concurrent row and column accesses, thus improving the system performance by 46.3% [70]. These works benefit from the reduced wirelength, but do not consider thermal issues.

A temperature-aware optimization flow to design a near-optimal energy-efficient systolic DNN accelerator in MONO3D mobile systems, under user-specified performance/thermal constraints is presented [71]. The optimization flow highlights the performance and temperature tradeoffs by showing that DNNs with a large number of MAC operations and higher dynamic power (such as VGG19 [72]) can result in high chip temperatures, which further increases temperature-dependent leakage due to tight inter-tier thermal coupling. The net increase in total power can result in thermal violations. While all of these works have demonstrated the benefits offered by MONO3D, there is still scope for developing standard performance and power models to help in designing DNN accelerators using different MONO3D partitioning techniques, utilizing the available bandwidth, while also accounting for thermal awareness.

### C. Hardware Security

The past decade has experienced a proliferation of research literature related to the hardware security aspects of 3D ICs [73], [74]. A majority of the work specific to MONO3D is based on circuit-level obfuscation techniques that broadly encompass logic locking and layout camouflaging. Camouflaging technique is used to thwart reverse engineering attacks by making modifications to the layout. A layout-level camouflaging technique is proposed for transistor-level MONO3D circuits by using dummy contacts [75]. The camouflaged MONO3D ISCAS '89 benchmark circuits are shown to exhibit, on average, power and area savings of, respectively, 6.3% and 47.5% compared to a conventional 2D IC at the expense of 27.4% timing degradation. Logic locking employs key-controlled logic gates for protection against IP piracy and reverse engineering attacks. In a recent work, the pull-down and pull-up networks of MONO3D cells in separate tiers are locked using parallel or serial locking transistors and camouflaged contacts, independently [76]. Therefore, one leaking tier does not compromise the entire design.

Due to exacerbated thermal issues, 3D systems (and particularly MONO3D ICs) can be more vulnerable to thermal side channel analysis attacks and thermal covert channels [77]. These attack models have not received much attention for MONO3D ICs. Recently, a thermal-aware side channel shielding technique was proposed for 3D ICs by generating custom activity patterns [78]. Another work developed thermally-aware floorplanning strategies to mitigate the thermal side-channel leakage [79]. However, both of these works are based on TSV-based 3D ICs. Similarly, covert communication through lateral thermal coupling between two cores has been demonstrated on a multicore 2D system with throughputs on the order of 50 bits per second [80]. Even though thermal side channel leakage or thermal covert channels are relatively low bandwidth processes, the strong vertical thermal coupling between the layers of a MONO3D IC (see Section III-B and Fig. 3) can potentially increase this capacity. For example, consider a MONO3D multicore system where one of the cores has access to sensitive information. This information can be covertly transmitted to another core located at the bottom layer. Such attack is possible provided that a temperature-based communication channel is established between those two cores by leveraging strong thermal crosstalk. This phenomenon can be a critical security breach for MONO3D ICs, particularly for sandboxed systems where the data that belongs to an application or core should be protected from other applications and cores.

## V. CONCLUSION AND FUTURE PROSPECTS

In this tutorial brief, the current status of MONO3D technology is presented with emphasis on both fabrication- and design-level developments. The primary process challenges

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related to thermal budget constraint, high quality silicon growth, and contamination are discussed, including existing approaches to these issues. At the design-level, important results on design automation, thermal integrity, and design-for-test are provided with emphasis on unique MONO3D characteristics. Three specific applications that can potentially benefit from MONO3D technology are also presented.

Lack of experimental results is a primary limitation related to most of the existing work on MONO3D ICs. Similarly, the fabrication-level constraints and design-level tools/methodologies are not sufficiently coupled, thereby making these methods less applicable. A stronger interaction between fabrication and design is anticipated and required in the future, as the MONO3D process matures and more opportunities arise for fabrication. These experimental results can also facilitate the detailed characterization and modeling of inter-tier process variations, which remain a primary concern for MONO3D technology. Existing cost models for MONO3D circuits can also benefit from these results. In the mean time, cross-layer design methods that go beyond physical design automation will enable system-level design space exploration while simultaneously considering important design objectives such as efficiency, performance, and thermal integrity. These methodologies and models should properly consider the fundamental partition approaches that MONO3D supports as each of these approaches will most likely be better suited for specific applications.

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