Experiment 5 - Design of an Operational Amplifier Using Multisim

ELEC271

April 25, 2022

Abstract

This report shows the design process of an operational amplifier according to specific requirements. Then, Multisim will be used to verify whether the design result meets all the requirements. Finally, this report will also point out some errors produced during the process and the suggestions to improve these errors.

Declaration

I confirm that I have read and understood the University's definitions of plagiarism and collusion from the Code of Practice on Assessment. I confirm that I have neither committed plagiarism in the completion of this work nor have I colluded with any other party in the preparation and production of this work. The work presented here is my own and in my own words except whereI have clearly indicated and acknowledged that I have quoted or used figures from published or unpublished sources (including the web). I understand the consequences of engaging in plagiarism and collusion as described in the Code of Practice on Assessment (Appendix L).

Contents

1 Introduction

1.1 Background

Operational Amplifier is a device that has properties required for the ideal amplification. Therefore, it can be used to perform mathematical operations, signal filtering and many other fields. It has two input ports (inverting input and non-inverting input) and one output port, which is shown in Figure 1.

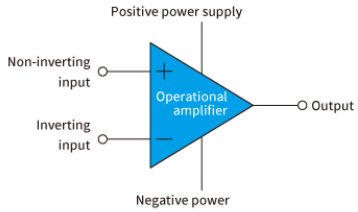

Figure 1: Operational Amplifier[1]

1.2 Theorey

Common Emitter Amplifier (CE) and Emitter Follower Amplifier (EF):

The load connects to the emitter of the Emitter follower amplifier or the collector of the common emitter amplifer. The voltage gain of CE is high while the gain of EF is low. Emitter follower is usually used to match impendence but not identify voltage gain.

Current Mirror:

It connects the base of the two transistors and ensures the two collectors have the same current value.

Differential Amplifier:

Differential amplifier can amplify the difference between two signals. However, if two input signals are same, the differential amplifier does not have amplify property.

Early Voltage:

It is an important parameter used in the design process. This value can be obtained by analysing the curve of the transistor, which is shown in Figure 2. In this design, the early voltages are 74.03(npn) and 115.7(pnp).

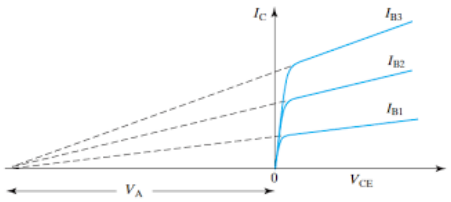

Figure 2: Early Voltage[2]

1.3 Objective

The design objectives are shown below:

- Differential input impedance greater than 100 kΩ.
- Voltage gain greater than 500,000.
- Output impedance less than 1 kΩ.
- Output voltage to be approximately zero volts for zero input.
- Frequency response down to dc (0 Hz).
- Supply voltage ±9 V.
- Total current consumption not greater than 5 mA.

2 Materials and methods

2.1 Calculation

Based on the analysis of part I. The β for pnp BJT is about 233, while for the npn BJT is about 179. The graphs can be found in the result section. What is more, the early voltage for npn transistor is 74.03 while pnp transistor is 115.7.

The total current is no more than 5mA and there are 5 path lines for the circuit. Thus, the value of I_{c6} can be assumed as 1mA. Moreover, the Differential input impedance is defined as $120k\Omega$ and output resistance is 800Ω.

- R_1

  We can calculate the value of R_1 based on the following steps

  $$R_1 = \frac{V_{cc} + V_{EE} - V_{BE}}{I_{C6}} = \frac{9 + 9 - 0.6}{1m} = 17.4k\Omega \tag{1}$$

- R_2

  Assume the input resistance of the differential amplifier is $120k\Omega$. Then, we can get the equation below:

  $$R_{id} = 2 * r_{be} = \frac{2\beta}{g_m} = \frac{2\beta}{40I_{c1}} \tag{2}$$

  According to the properties of differential amplifier. we have

  $$I_{c1} = I_{c2} = \frac{1}{2}I_{c5} \tag{3}$$

  Then, we can calculate the value of I_{c5}

  $$I_{c5} = \frac{\beta_{pnp}}{10 \times R_{id}} = \frac{233}{10 \times 120k} = 1.942 \times 10^{-4}A \tag{4}$$

  Q5 and Q6 constitute a widlar current mirror. Therefore, the following equation can be obtained

  $$I_{c5} \times R_2 = V_T \ln \frac{I_{c6}}{I_{c5}} \tag{5}$$

  The value of R_2 is about 211.042Ω.

- R_3 and R_4

  Firstly, several parameters should be calculated

$$r_{ce2} = \frac{V_{A(pnp)}}{I_{c2}} = \frac{115.7}{1.0415 \times 10^{-4}} = 1.111M\Omega \tag{6}$$

$$r_{ce4} = \frac{V_{A(npn)}}{I_{c4}} = \frac{74.03}{1.0415 \times 10^{-4}} = 7.108 \times 10^5\Omega \tag{7}$$

$$r_{be9} = \frac{\beta_{npn}}{g_m} = \frac{179}{40I_{c6}} = 4.475k\Omega \tag{8}$$

$$r_{ce8} = \frac{V_{A(pnp)}}{I_{c6}} = \frac{115.7}{1m} = 115.7k\Omega \tag{9}$$

$$r_{ce9} = \frac{V_{A(npn)}}{I_{c9}} = \frac{74.03}{1m} = 74.03k\Omega \tag{10}$$

$$r_{ce2}//r_{ce4} = \frac{r_{ce2} \times r_{ce4}}{r_{ce4} + r_{ce2}} = 4.334 \times 10^5\Omega \tag{11}$$

$$r_{ce8}//r_{ce9} = \frac{115.7k \times 74.03k}{115.7k + 74.03k} = 4.514 \times 10^4\Omega \tag{12}$$

  Suppose $R_{in}^{EF} = 10R_{out}^{DA}$. Derive this equation, the value of R_4 can be calculated.

$$R_{out}^{DA} = r_{ce2}//r_{ce4} \tag{13}$$

$$R_{in}^{EF} = r_{be7} + (1 + \beta_{npn})(R_4//r_{be9}) \tag{14}$$

  The value of r_{be7} can be expressed as the following equation:

$$V_{BE} = I_{c7} * R_4 \tag{15}$$

$$r_{be7} = \frac{\beta_{npn} * R_4}{40 * V_{BE}} \tag{16}$$

  The value of R_4 is about 474.104kΩ

  Suppose the output resistance is 800Ω. Thus, the following equations can be used to calculate the value of R_3

$$R_{out} = \frac{r_{be10} + r_{ce9}//r_{ce8}}{1 + \beta_{npn}}//R_3 \tag{17}$$

  R_3 is about 198.883kΩ.

The differential gain is about

$$A_{vd} = \frac{1}{2V_T}\frac{V_{An}V_{Ap}}{V_{An} + V_{Ap}} = 902.891 \tag{18}$$

The gain of CE stage is about

$$A_{Vce} = \frac{1}{V_T}\frac{V_{An}V_{Ap}}{V_{An} + V_{Ap}} = 1805.781 \tag{19}$$

2.2 The result circuit

Apply calculated resistance values. The circuit is shown in Figure 3.

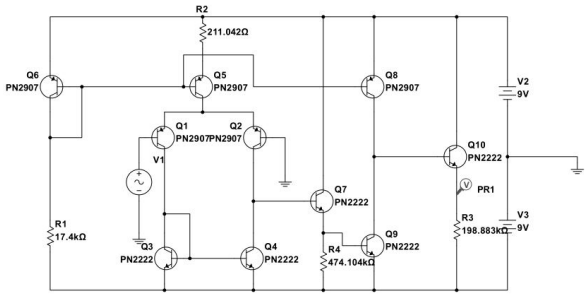

Figure 3: Operational Amplifier

3 Results

3.1 Part I

The circuit for Part I is shown in Figure 4.

Figure 4: BJT circuit

Then, set up the parameters show in Figure 5.

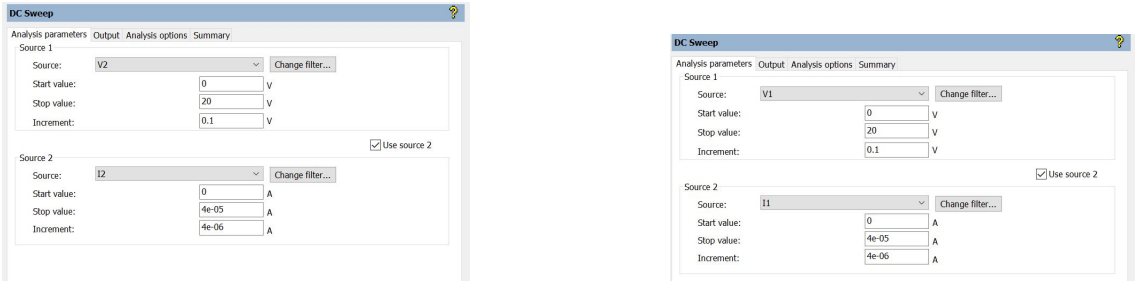

Figure 5: Value for the two transistors

The DC sweep result for npn transistor is shown in Figure 6.

The value of β_{npn} is

$$\frac{\Delta I_C}{\Delta I_B} = 179 \tag{20}$$

The DC sweep result for pnp transistor is shown in Figure 7.

The value of β_{pnp} is

$$\frac{\Delta I_C}{\Delta I_B} = 233 \tag{21}$$

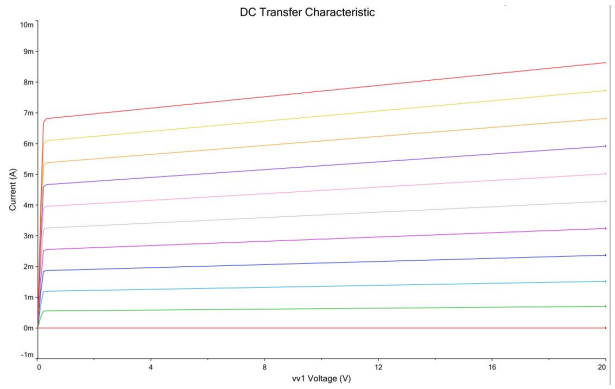

Figure 6: DC sweep result for npn

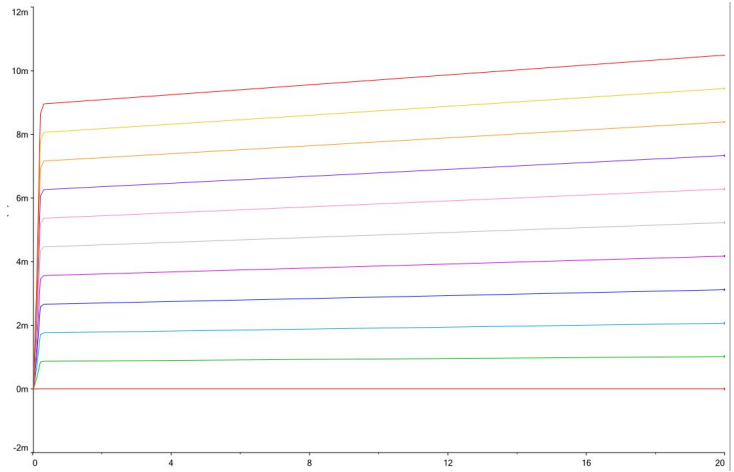

Figure 7: DC sweep result for pnp

3.2 Part II Task 2

The circuit is shown in Figure 8.

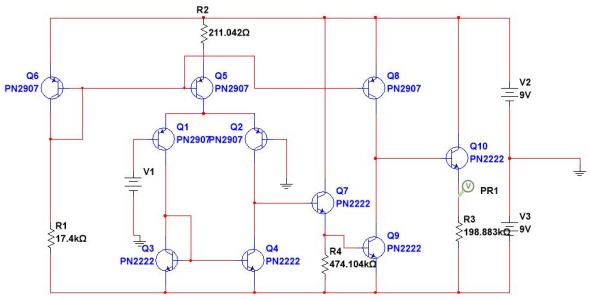

Figure 8: Operational Amplifier

The parameters for the DC sweep values are shown in Figure 9.

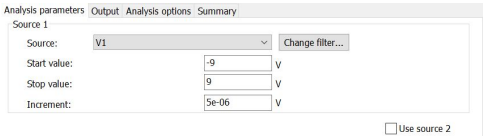

Figure 9: DC sweep parameters

By simulating the circuit, the result is shown in Figure 10.

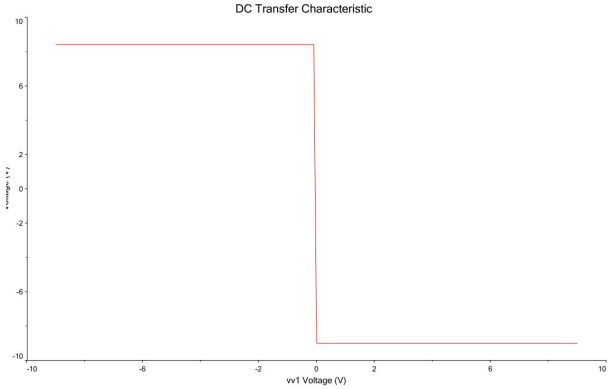

Figure 10: DC sweep for the operational amplifier

3.3 Part II Task 3

By analyzing the plot in Figure 10, it can be seen that the region should be defined between -120μV and -100μV. The parameters can be seen in Figure 11.

By changing the region, the new DC sweep result is shown in Figure 12.

In Figure 12, the coordinates for the two corner points are (-115.684μ, 8.333) and (-103.110μ, -8.996). Therefore, the gain A_{ol} can be calculated by the following equation. That is the ratio

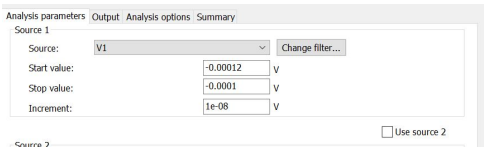

Figure 11: DC sweep parameters

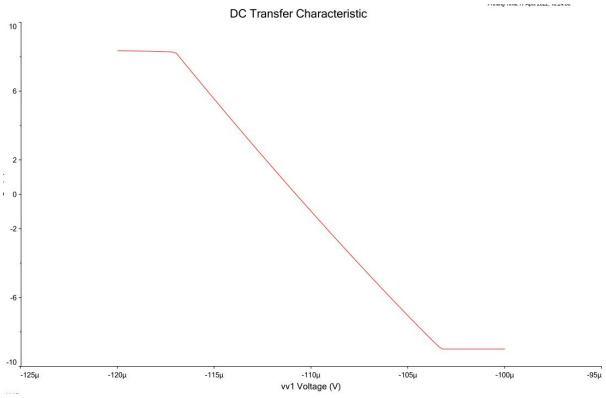

Figure 12: DC sweep results

of Δy over Δx between the two corner points.

$$A_{ol} = \frac{8.333 - (-8.996)}{(-115.684\mu) - (-103.110\mu)} = -1276631.796 \tag{22}$$

3.4 Part II Task 4

It can be found that the output is close to zero volts when the DC offset is about -110.793μV. The plot is shown in Figure 13.

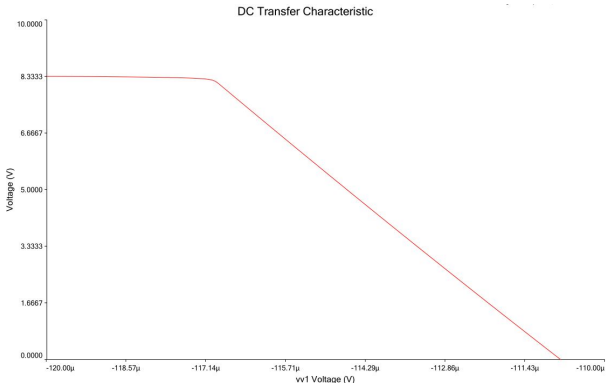

Figure 13: DC sweep results

3.5 Part II Task 5

The circuit for this part is shown in Figure 14.

The parameters for the input source is shown in Figure 15.

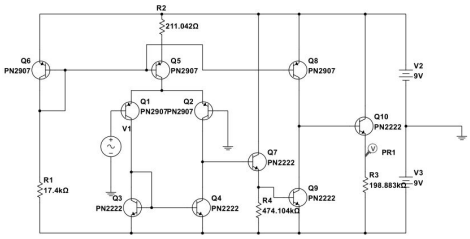

Figure 14: Operational Amplifier

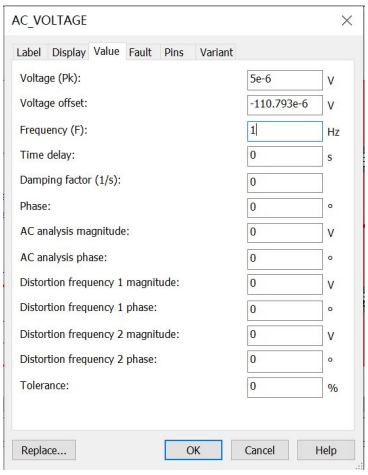

Figure 15: Input value

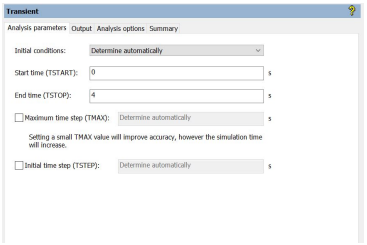

Figure 16: Transient parameters

The parameters for the transient circuit is shown in Figure 16.

By simulating the circuit, the result can be found in Figure 17.

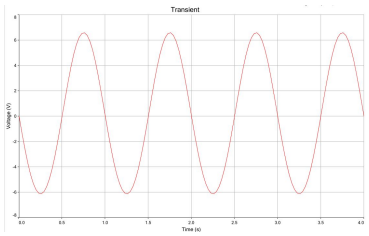

Figure 17: Transient result

The maximum value of the signal is about 6.636V, while the minimum value is about -6.207V. Thus, the gain can be calculated by the following equation:

$$A_v = \frac{A_{max} - A_{min}}{2V_{in}} = \frac{6.648 - (-6.118)}{2 \times 5 \times 10^{-6}} = 1276000 \tag{23}$$

The value is larger than the required gain (500,000). Moreover, the AC gain result is close to the previous DC gain result. When the input voltage is about 6μV, the simulation output is quite similar to Figure 18.

When the magnitude of the input signal continues to increase, the simulation result will become a square wave rather than the expected sine waveform. For example, when input values are 10×10^{-6}V and 2V, the output waveform will distort. It can be seen in Figure 18 and Figure 19. Therefore, it is essential to choose a suitable input range. The input value for this circuit should be around 5μV to 6μV.

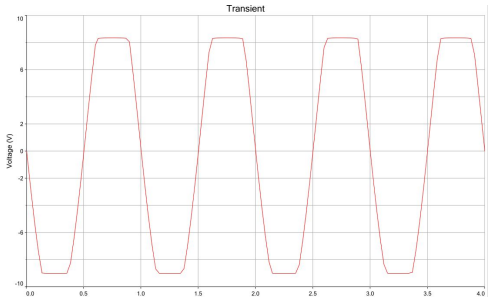

Figure 18: Transient result (10×10^{-6}V)

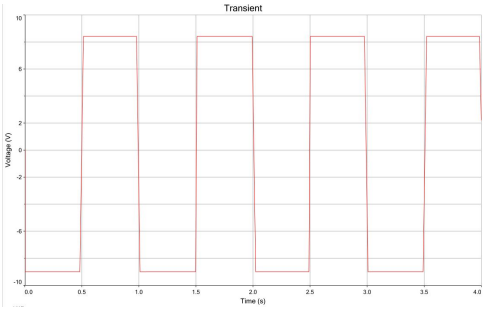

Figure 19: Transient result (2V)

3.6 Part II Task 6

Based on the circuit in Figure 14, the parameters for the transfer functions are shown in Figure 20.

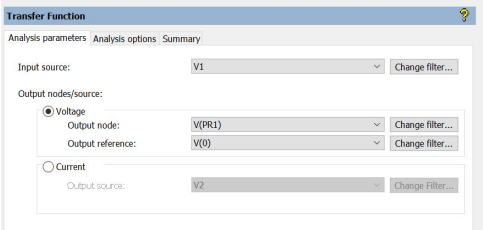

Figure 20: Transfer function parameters

The result is shown in Figure 21.

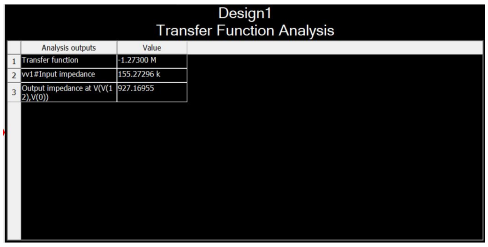

Figure 21: Transfer function result

From the result, the absolute value of the transfer function is close to the simulation result that has been done in Part II Task 5. Both the absolute values in Part II Task 5 and 6 are lower than the calculated value in Part II Task 3. The input resistance is more than 150kΩ, which is much higher than the theoretical value (120kΩ). For the output resistance, the value is about 927.170Ω, which is below the required value 1kΩ. But it is higher than the theoretical value (800Ω).

3.7 Part II Task 7

The simulation result with all the values is shown in Figure 22.

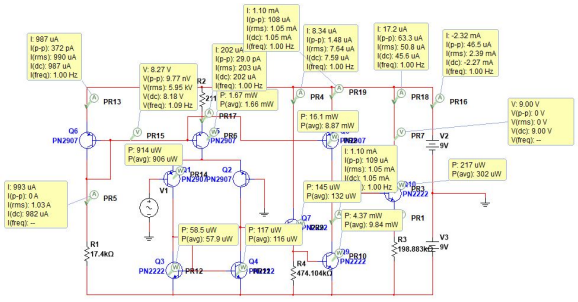

Figure 22: Simulation result

The magnitude of total current is about 2.32mA, which is much smaller than the required value

5mV. In addition, changing the input voltage to 0V, the DC output voltage is about 4.57mV, which is closer to the required value 0V.

What is more, it is also find that the gain of the differential amplifier is about 1140, which is larger than the calculated value. For the CE stage, the gain is about 1909.77, which is also larger than the calculated value.

3.8 Part III Task 1

The circuit for this task is shown in Figure 23.

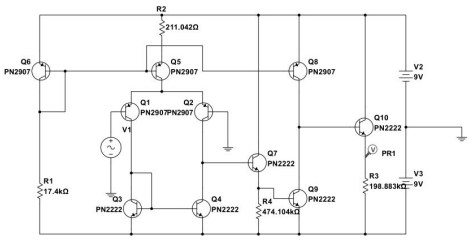

Figure 23: Operational Amplifier

The settled parameters can be seen in Figure 24.

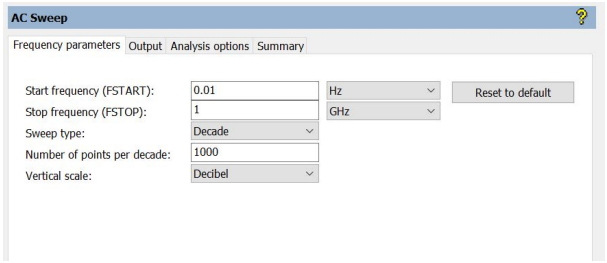

Figure 24: AC sweep parameters

The simulation result is shown in Figure 25.

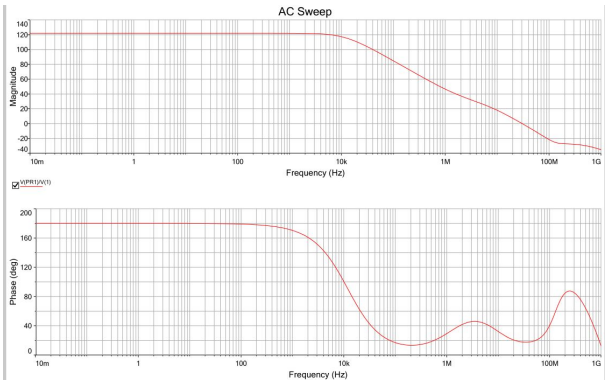

Figure 25: AC sweep parameters

The gain can be expressed by dB according to the following equation:

$$dB = 20 \times \log_{10} gain \tag{24}$$

From the upper magnitude graph, the magnitude of the flat part of the gain is about 122.096dB. Therefore, the gain is about 1272916.746, which also proves the correctness of the design. When the frequency increases to about 7.66kHz, the circuit reaches the corner frequency, which the gain will reduce to 119.197dB. After that, the gain will continue to decrease to the minus value.

For the lower phase graph, the phase remains unchanged in low frequency. Therefore, the angle of the gain is steady. Based on these analyses, the amplifier has a stable gain in the low-frequency range. The phase margin is about 17.793 degree.

3.9 Part III Task 2

After adding a 30 pF compensating capacitor , the circuit is changed to Figure 26.

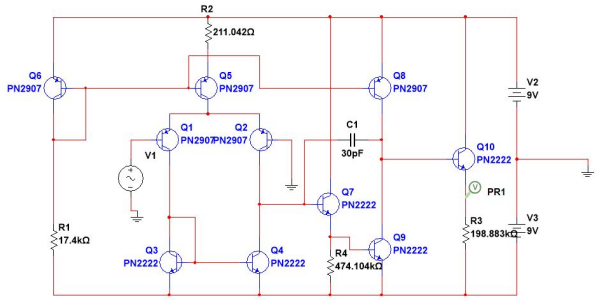

Figure 26: Operational amplifier circuit

The AC sweep is similar to what has been shown in Figure 24.

The simulation result is shown in Figure 27.

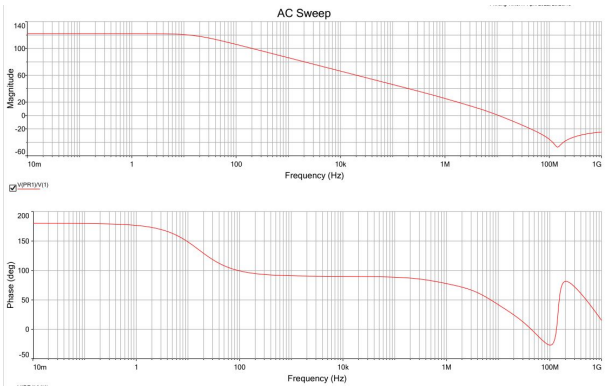

Figure 27: AC sweep result

From the upper graph, the magnitude of the gain is still around 122.2dB. That means the capacitor has no effect on the response of the gain. When the frequency increases to approximately 15.64Hz, it reaches the 3dB point. The frequency value is higher than the frequency shown in Part III Task 1.

For the lower phase graph, compared to the circuit without the capacitor, it can be seen that the phase remains stable in a range from 100 to 1MHz. The phase margin is about 39.285 degree.

4 Discussion

4.1 General Question

- What can you deduce about the stability of your amplifier from the Bode plots in Part III?
  - This operational amplifier is designed using the open-loop system. The stability is evaluated by the phase or gain margin. Phase margin is the difference between the phase shift and the 180° phase. Phase shift refers to the voltage gain intersecting with the 0dB axis. The gain margin is the difference between the voltage gain(in decibel) and zero decibel at a 180° phase [3].
  - The way of obtaining phase margin is shown in Figure 28. Firstly, find the intersection point of the gain wave with 0dB axis and record the horizontal coordinates. Then, find the phase value using the same horizontal coordinates. For the two conditions in Part III, the phase margins are 17.793° and 39.285°.

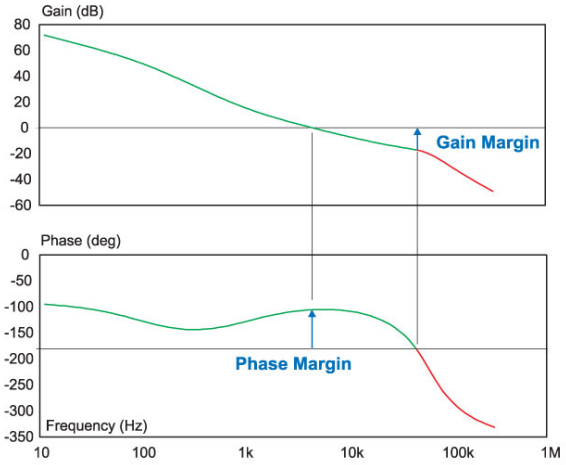

Figure 28: Phase margin[3]

  - For the result in Part III, the circuit with capacitor is more stable. What is more, in order to avoid slow time response speed, the suitable phase margin is defined between 45° and 75°.

- What is the purpose of the "Phase compensating capacitor"?
  - From Part III result, the compensation capacitor increases the phase margin while reducing the system bandwidth. But it has no effect in the low-frequency range. In detail, the reduction of bandwidth leads to the 0dB point becoming smaller. The smaller point results in a bigger phase margin, which means a more stable system [4].
  - By observing the result, the compensating capacitor can increase the stability of the amplifier. Therefore, the purpose of the capacitor is to increase the stability of the amplifier.

4.2 Design Specification

The design specification is shown in the following table.

Parameters	Specification	Your value	Comment on the value obtained
Differential input impedance	> 100 k	155.273kΩ	The result meets the requirement but has a large difference with the assumption (120kΩ)
Open loop voltage gain	> 500,000	1275210.599	The result gain is much bigger than the required value. The detail can be seen in Part II result
Output impedance	< 1 k	927.170Ω	The result is smaller than the required value. But it is larger than the assumption value (800Ω)
DC output voltage	~0 V	-4.57mV	The simulation result generally achieves the goal since the value is very small.
DC offset voltage	None given	-110.793μV	The detail can be seen in Part II Task 4
Frequency response	Down to DC (0 Hz)	Maximum 122.2dB	The gain reduces from 122.2dB to minus value with the increase of frequency
Total current consumption	< 5 mA	2.32mA	The simulation result is smaller than the requirements
Bandwidth with compensation capacitor	None given	18Hz	The detail can be seen from Part III Task 2.

More details are shown below:

- Open-loop voltage gain

  The required open-loop gain is more than 500,000. From the Part II result, the magnitudes of open-loop gains are 1273000, 1276000 and 1276631.796. It is clear that the operational amplifier has a very high voltage gain which meets the requirement. Even considering the effect of errors, the simulation results still meet the requirements.

- DC offset voltage

  The value of DC offset voltage is about -110.793μV. There is no specific requirement for this value. This voltage is not a parameter that can be designed directly. It can be obtained by simulating after setting all the resistor and capacitor values.

- DC output voltage

  DC output voltage is about -4.57mV, which is approximated to 0V. Thus, it also meets the requirement. However, in reality, this value can not be eliminated due to the internal situation of the circuit.

- Total current consumption

  The total current consumption is about 2.32mA, which is lower than the required value 5mA. For an amplifier, this value is expected to be as small as possible. With a low current consumption value, the circuit can save power.

- Frequency response

The gain is about 122.2dB. After adding the capacitor to the circuit, the value is not changed. The gain will change with the increase of frequency range. The expression is shown below:

$$A_V = -g_m \times R_t \times \frac{r_{b'e}}{(r_{b'e} + r_{b'b} + R_s)(1 + j\frac{f}{f_H})} \tag{25}$$

As the equation shows, when the frequency is much smaller than the f_H, the voltage gain reaches the maximum magnitude. What is more, the phase difference is 180°. That is the reason for part III, the graph has the flat region in the low-frequency region.

- Bandwidth with compensation

  The bandwidth of the circuit with compensation capacitor is about 39.285Hz, which is much larger than the circuit without it. This is caused by Miller's Effect. The value can be obtained by simulation, which is shown in Part III.

4.3 Error Analysis

- The problem with the gain

  By following the calculation steps shown in the design notes, it can be found that the theoretical value of the total gain is much larger than the result. That is because all the CC gains are supposed to 1 during the calculation. But the simulation value of the gain Q7 is about 0.56, which can be seen in Figure 29. That causes errors.

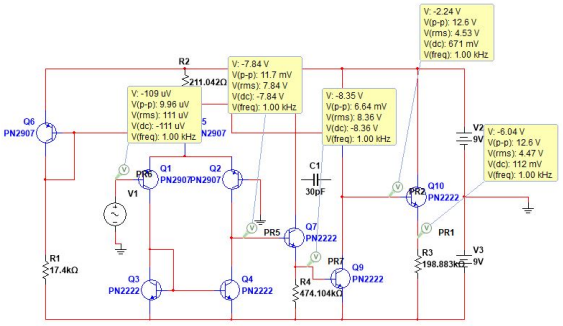

Figure 29: Simulation result

In order to make the simulation value close to the calculation value, a resistor with a bypass capacitor might be used to increase the gain.

- The assumption value and the simulation result of resistance.

  The assumption values are 120kΩ and 800Ω, while the simulation results are about 155.273kΩ and 927.170Ω. The difference between the simulation result and theoretical result may cause by the approximation during the calculation process. For example, the base resistance is ignored during the calculation, which is not ignored during the simulation process.

- The value of voltage gain

  The magnitudes are 1272916.746, 1273000, 1276000 and 1276631.796, which are different from each other. This might be caused by the increment setting for the simulation. The smaller increment value set, the more accurate simulation result will be. However, the

simulation models chosen are different, the amplitude set for the sources are also different, and the choice of the number of steps may have different degrees of impact on the accuracy of the simulation.

- The calculation for four resistances

  The calculated values for these resistances are based on the assumptions and approximations, such as the value of β. Therefore, the resistor values are not accurate. What is more, in reality, resistors do not have value with several decimal numbers. Therefore, it is impossible to adjust to the expected value accurately.

4.4 Suggestions

Some methods that can be taken to reduce error.

- Make less approximation

  Some approximations can be replaced by more accurate calculations. For instance, use the following equation to calculate the value of r_{be}, but not $r_{be} = \frac{\beta}{40I_C}$.

$$r_{be} = \frac{\beta V_T}{I_C} \tag{26}$$

- Use more steps to do simulation

  In order to make the result more accurately, more steps are required to set for simulation. However, it may require computers have high quality. Therefore, a powerful computer can help to improve the simulation result.

- Use accurate magnitude of β

  The value of β is obtained by observing the DC sweep result, which is shown in Part I. This method can be improved by taking smaller steps between every two steps of I_B. Thus, more sets of I_C and I_B can be measured, and the solutions are more reliable.

5 Conclusion

In general, all the objectives are achieved. All the simulation results meet the requirements. Errors are also analyzed, and corresponding suggestions are provided in the discussion section. Despite the achievements, there are still some limitations, such as the approximation methods in the calculation process. These limitations can be improved by using corresponding methods, which has been provided in the previous section. In the future, Transcendental equations can be taken to reduce errors. By using this method, equations can be generated according to inequality relationships, and the result can be a range of value rather than a particular value. Moreover, the compensation components can be designed more scientifically by adding the capacitor in series with a resistor. In this way, a more scientific result can be obtained.

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