第 6 章 时序逻辑电路

Sequential Logic Circuits

§ 6.1 概述 Introduction

时序电路

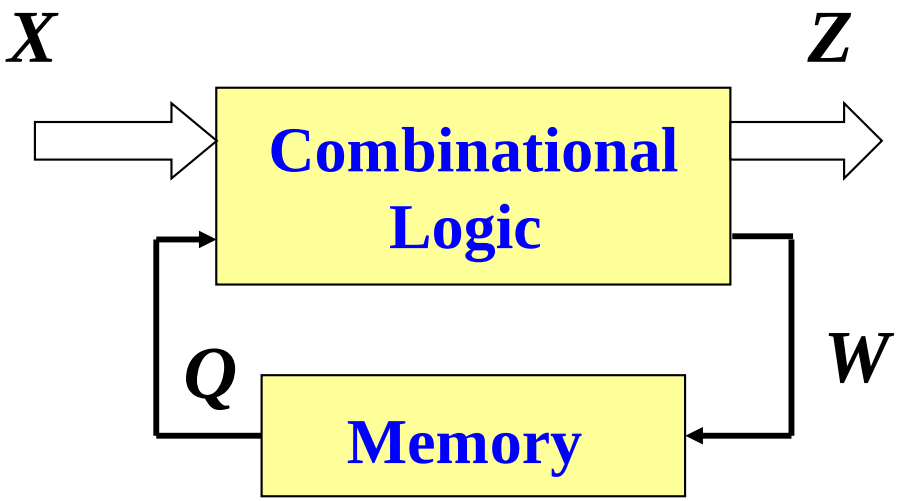
- 输出
  - 输入
  - 以前状态　　记忆
- 基本单元: FF (逻辑门 + 反馈线)

逻辑电路

- 同步　所有的触发器在*CLK* 同一边沿触发
- 异步

时序电路结构:

组合电路 + 记忆元件



***X*：外输入**

***Z*：外输出**

W*: 控制输入 -- *J, K, D, T

***Q*: 触发器输出（状态）**

外输入 X　　控制输入 W

外输出 Z　　状态　Q

关系：

输出方程　$Z = F(X, Q)$

驱动方程　$W = H(X, Q)$

特征方程　$Q^{n+1} = G(W, Q^n)$

按照电路中输出变量是否和输入变量直接相关

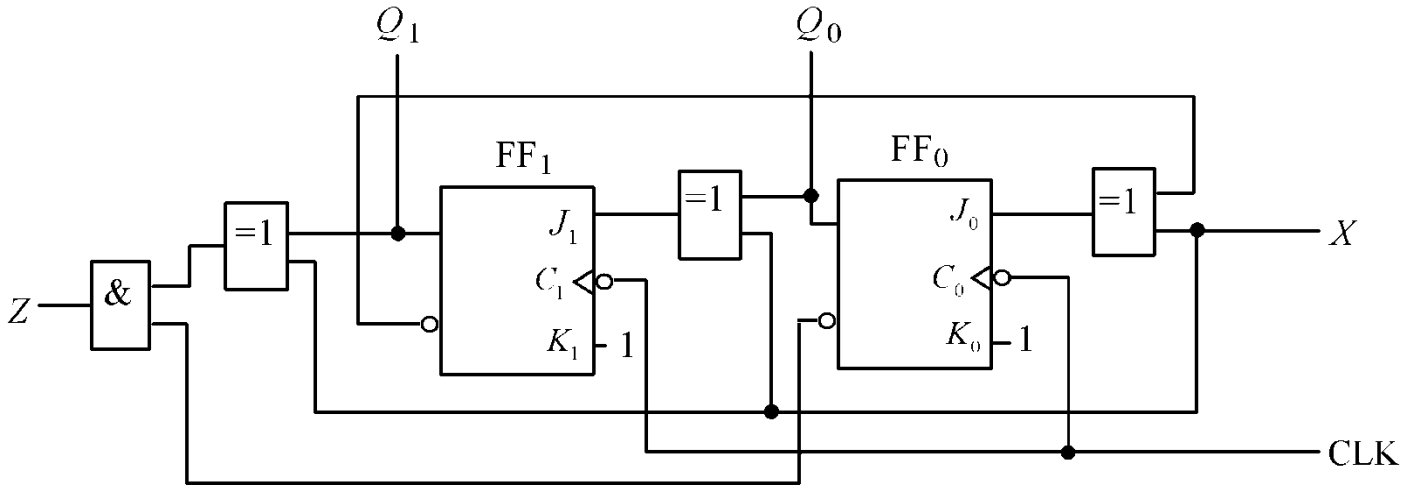
时序电路
- 米里型 (Mealy)　输出 Z { Q^n, X
- 莫尔型 (Moore)　输出 $Z \sim Q^n$

§6.2 同步时序电路分析

Sequential Logic Circuits Analysis

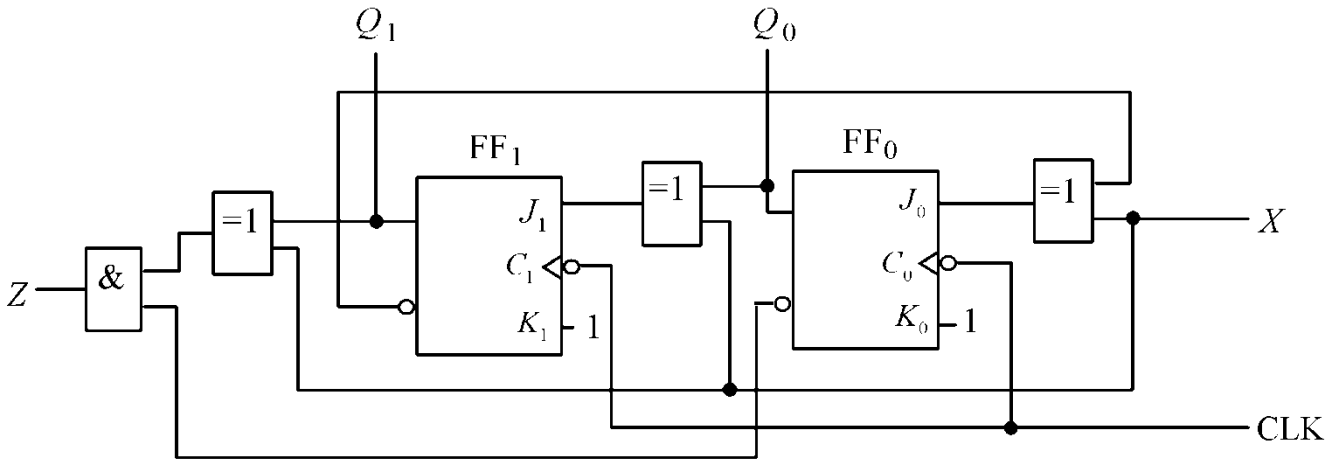
分析：已知电路，描述电路原理及功能.

例1：分析下图时序逻辑电路



1) 输入 X 控制输入 J_0, K_0, J_1, K_1

输出 Z 状态 Q_1 (MSB), Q_0



2) 方程

输出方程 $Z = (X \oplus Q_1^n) \cdot \overline{Q_0^n}$

驱动方程

$$\begin{cases} J_0 = X \oplus \overline{Q_1^n} \\ K_0 = 1 \end{cases} \qquad \begin{cases} J_1 = X \oplus Q_0^n \\ K_1 = 1 \end{cases}$$

特征方程

$$\begin{cases} Q_0^{n+1} = J_0\overline{Q_0^n} + \overline{K_0}Q_0^n = (X \oplus \overline{Q_1^n}) \cdot \overline{Q_0^n} \\ Q_1^{n+1} = J_1\overline{Q_1^n} + \overline{K_1}Q_1^n = (X \oplus Q_0^n) \cdot \overline{Q_1^n} \end{cases}$$

3) 状态表和状态图

已知：输入 X，Q^n

求：输出 Z，Q^{n+1}

$$Q_1^{n+1} = (X \oplus Q_0^n) \cdot \overline{Q_1^n}$$

$$Q_0^{n+1} = (X \oplus \overline{Q_1^n})\overline{Q_0^n}$$

$$Z = (X \oplus Q_1^n) \cdot \overline{Q_0^n}$$

状态表

	X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Z
X=0	0	0	0	0	1	0
	0	0	1	1	0	0
	0	1	0	0	0	1
	0	1	1	0	0	0
X=1	1	0	0	1	0	1
	1	0	1	0	0	0
	1	1	0	0	1	0
	1	1	1	0	0	0

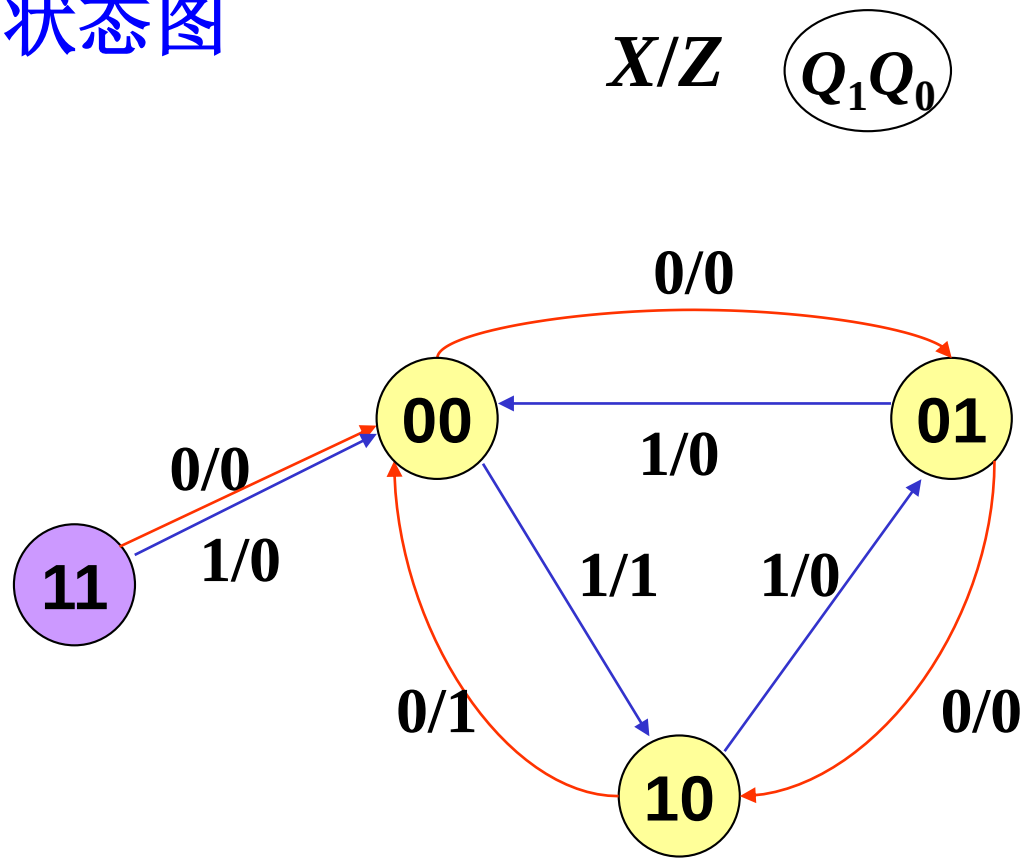
X=0

$$\begin{cases} Q_1^{n+1} = Q_0^n \cdot \overline{Q}_1^n \\ Q_0^{n+1} = \overline{Q_1^n} \cdot \overline{Q_0^n} = \overline{Q_1^n + Q_0^n} \\ Z = Q_1^n \cdot \overline{Q_0^n} \end{cases}$$

X=1

$$\begin{cases} Q_1^{n+1} = \overline{Q_0^n} \cdot \overline{Q_1^n} \\ Q_0^{n+1} = Q_1^n \cdot \overline{Q_0^n} \\ Z = \overline{Q_1^n} \cdot \overline{Q_0^n} \end{cases}$$

状态图



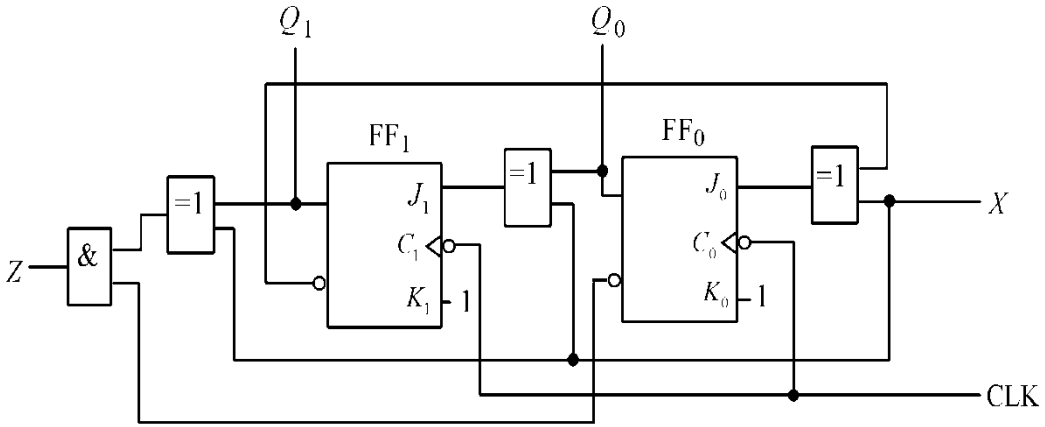
状态表

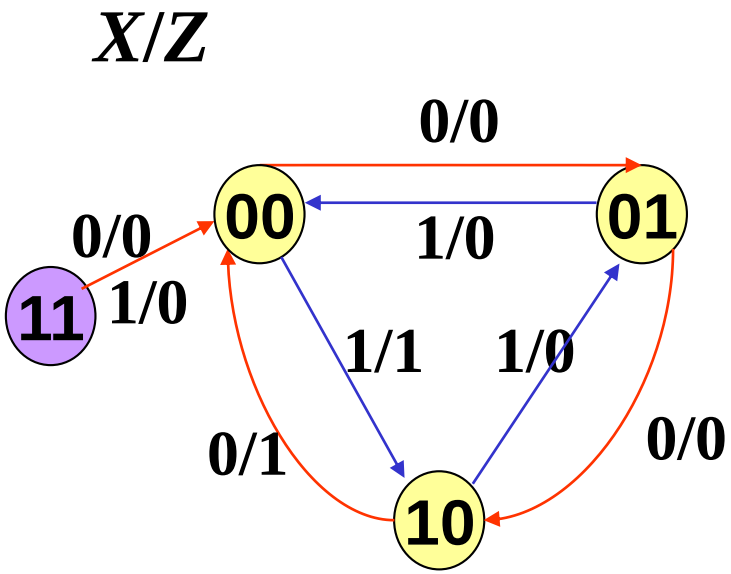
X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Z
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	0	1	0
1	1	1	0	0	0

⟶ 对应一个*CLK*　　输出*Z*是原状态下的输出。

每条转换线对应真值表的一行

4) 电路功能



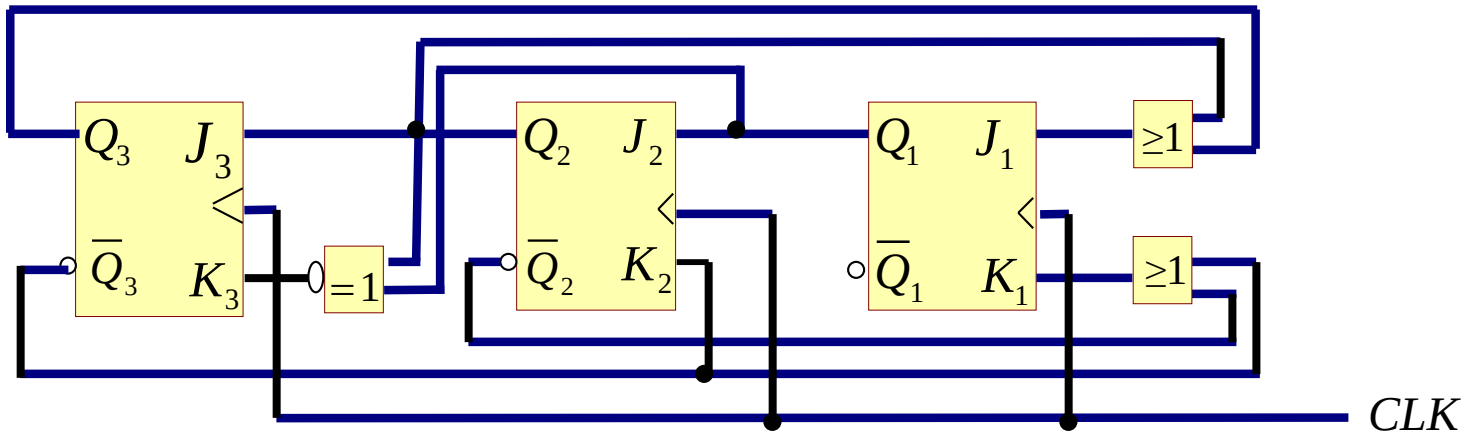


状态图主循环：模 3 加减双向计数器

X=0, M-3 加法计数：Z＝1，进位输出；

X=1, M-3 减法计数：Z＝1，借位输出。

例 2. 分析下图时序电路



无外输入，无外输出

$$\begin{cases} J_3 = Q_2^{\,n} \\ K_3 = \overline{Q_2^{\,n} \oplus Q_1^{\,n}} \end{cases} \qquad \begin{cases} J_2 = Q_1^{\,n} \\ K_2 = \overline{Q}_3^{\,n} \end{cases} \qquad \begin{cases} J_1 = Q_2^{\,n} + Q_3^{\,n} \\ K_1 = \overline{Q}_2^{\,n} + \overline{Q}_3^{\,n} = \overline{Q_2^{\,n} Q_3^{\,n}} \end{cases}$$

$$Q_3^{n+1} = J_3\overline{Q_3^n} + \overline{K}_3 Q_3^n = Q_2^n\overline{Q_3^n} + (Q_2^n \oplus Q_1^n)Q_3^n$$

$$Q_2^{n+1} = J_2\overline{Q_2^n} + \overline{K}_2 Q_2^n = Q_1^n\overline{Q_2^n} + Q_3^n Q_2^n$$

$$Q_1^{n+1} = J_1\overline{Q_1^n} + \overline{K}_1 Q_1^n = (Q_2^n + Q_3^n)\overline{Q_1^n} + Q_2^n Q_3^n Q_1^n$$

Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

$$Q_3^{n+1} \begin{cases} Q_2^n & Q_3^n = 0, \\ Q_2^n \oplus Q_1^n & Q_3^n = 1, \end{cases}$$

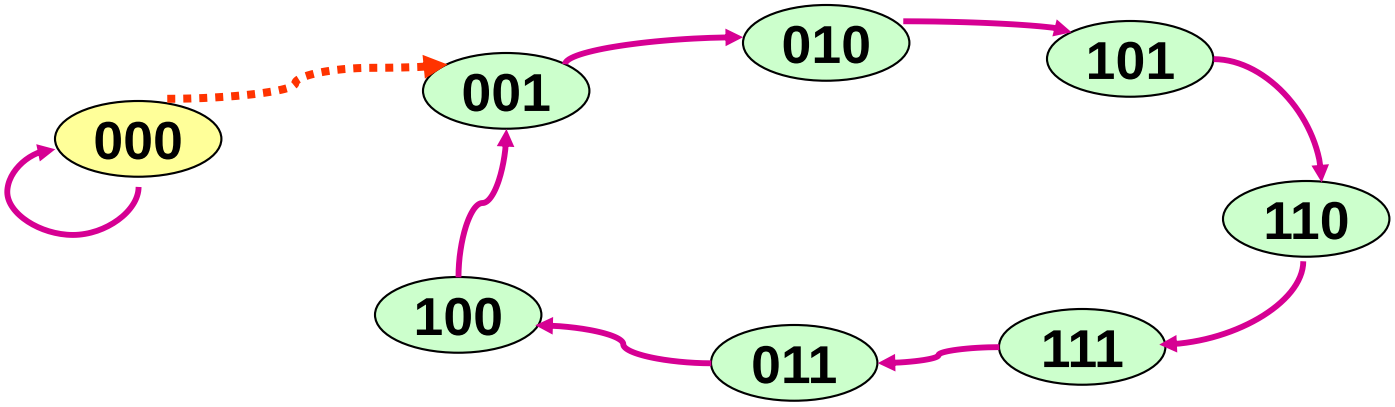
$$Q_2^{n+1} \begin{cases} Q_1^n & Q_2^n = 0, \\ Q_3^n & Q_2^n = 1, \end{cases}$$

$$Q_1^{n+1} \begin{cases} Q_2^n + Q_3^n & Q_1^n = 0, \\ Q_2^n Q_3^n & Q_1^n = 1, \end{cases}$$

Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

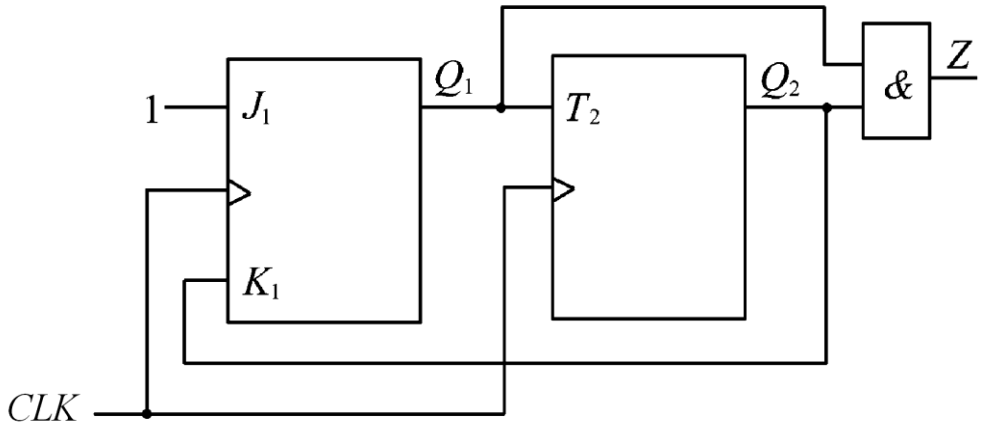
000 孤立状态

自启动



课堂练习

分析题图所示的同步时序电路，画出状态图。



解： $J_1 = 1, \quad K_1 = Q_2^n,$

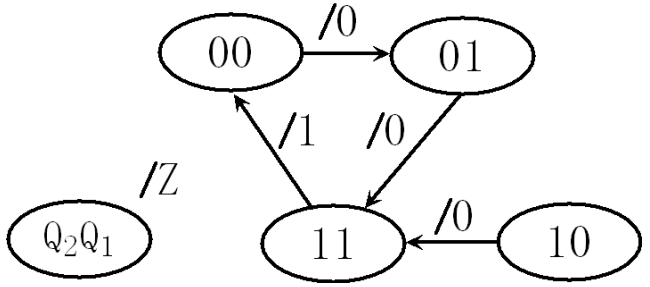
$T_2 = Q_1^n,$

$Z = Q_2^n Q_1^n$

$$Q_1^{n+1} = J_1\overline{Q_1^n} + \overline{K}_1 Q_1^n$$
$$= \overline{Q_1^n} + \overline{Q_2^n} Q_1^n$$
$$= \overline{Q_1^n} + \overline{Q_2^n}$$

$$Q_2^{n+1} = T_2 \oplus Q_2^n = Q_1^n \oplus Q_2^n$$

Q_2^n	Q_1^n	Q_2^{n+1}	Q_1^{n+1}	Z
0	0	0	1	0
0	1	1	1	0
1	0	1	1	0
1	1	0	0	1



§6.3 同步时序电路设计

Synchronous Sequential Circuit Design

已知 → 功能或状态图

求 → 电路

设计步骤:

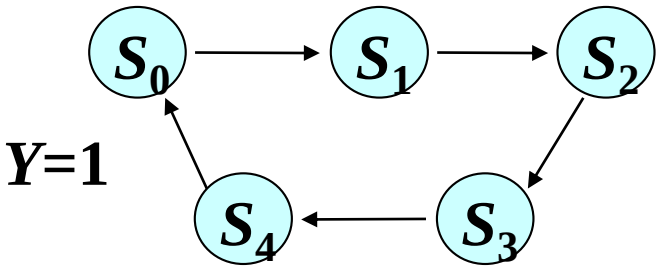
1) 确定状态和状态图
2) 状态化简
3) 状态分配 (编码)
4) 选择触发器类型
5) 状态方程Q^{n+1}及控制输入– ***J, K, D, T***
6) 画出电路
7) 自启动

例 1. 设计同步5进制加法计数器 (例6.4)

1) 确定状态及状态图

M-5 计数器，5 个状态：S_0, S_1, S_2, S_3, S_4

在计数脉冲*CLK*作用下，5 个状态周期性变换, 在 S_4 状态下进位输出 $Y = 1$ 。



2) 状态化简

M-5, 5 个状态， 不须再化简

3) 状态分配、编码

$2^{n-1} \le$状态数 $\le 2^n$　　n：二进制位数　　3位

S_0 ⟹ 000

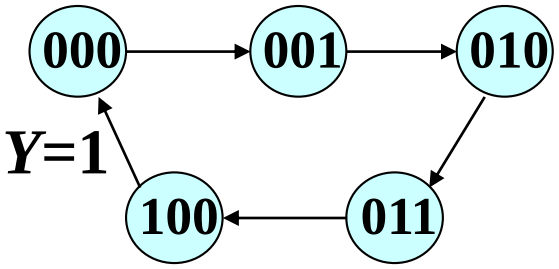
S_1 ⟹ 001

S_2 ⟹ 010

S_3 ⟹ 011

S_4 ⟹ 100

状态图



状态表

Q_3^n Q_2^n Q_1^n	Q_3^{n+1} Q_2^{n+1} Q_1^{n+1}	Y
0 0 0	0 0 1	0
0 0 1	0 1 0	0
0 1 0	0 1 1	0
0 1 1	1 0 0	0
1 0 0	0 0 0	1

4) 选择 FF，确定状态方程Q^{n+1}及输入

方法 1：先不确定用哪种触发器

由状态表填卡诺图

状态表

Q_3^n	Q_2^n	Q_1^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1

Q_3^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	0
1	0	1	Φ	Φ

Q_2^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	1	Φ	0
1	1	0	Φ	Φ

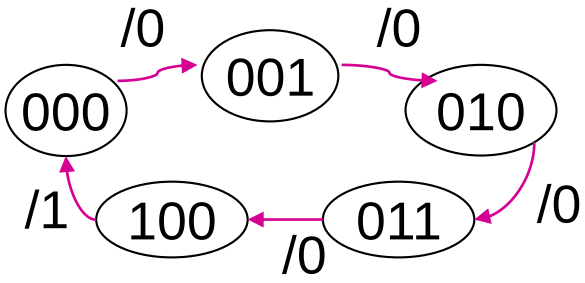
Q_1^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	1	Φ	0
1	0	0	Φ	Φ

Z

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	1
1	0	0	Φ	Φ

直接填卡诺图



5个 有效状态　$5 < 2^3$　3 个FF

$Q_3^nQ_2^nQ_1^n$ —/Z→ $Q_3^{n+1}Q_2^{n+1}Q_1^{n+1}$

Z

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	1
1	0	0	Φ	Φ

Q_3^{n+1}

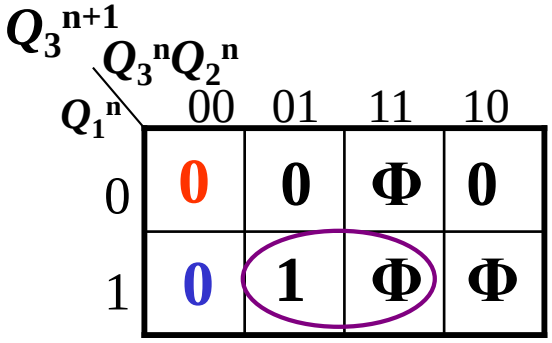
Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	0
1	0	1	Φ	Φ

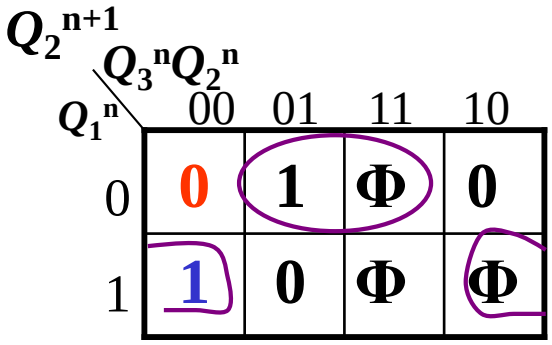
Q_2^{n+1}

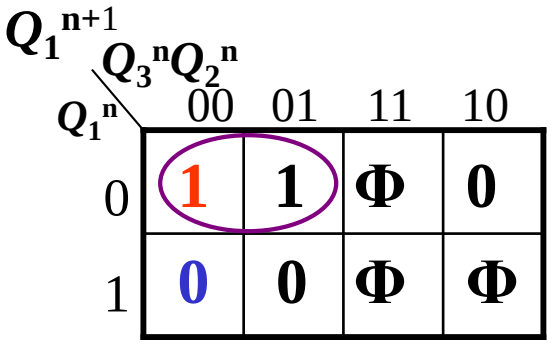
Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	1	Φ	0
1	1	0	Φ	Φ

Q_1^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	1	Φ	0
1	0	0	Φ	Φ







$$Q_3^{n+1} = Q_2^nQ_1^n$$

$$= D_3$$

$$D_3 = Q_2^nQ_1^n$$

$$Q_2^{n+1} = Q_1^n\bar{Q}_2^n + \bar{Q}_1^nQ_2^n$$

$$= Q_1^n \oplus Q_2^n$$

$$= T_2 \oplus Q_2^n$$

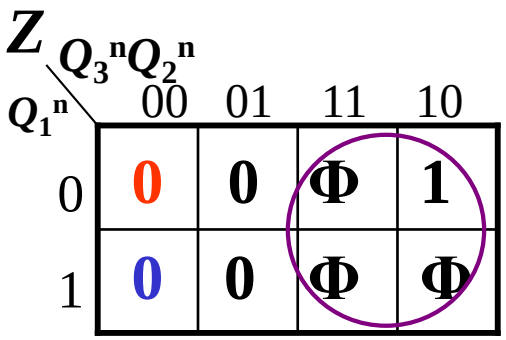
$$T_2 = Q_1^n$$

$$Q_1^{n+1} = \bar{Q}_3^n\bar{Q}_1^n$$

$$= D_1$$

或

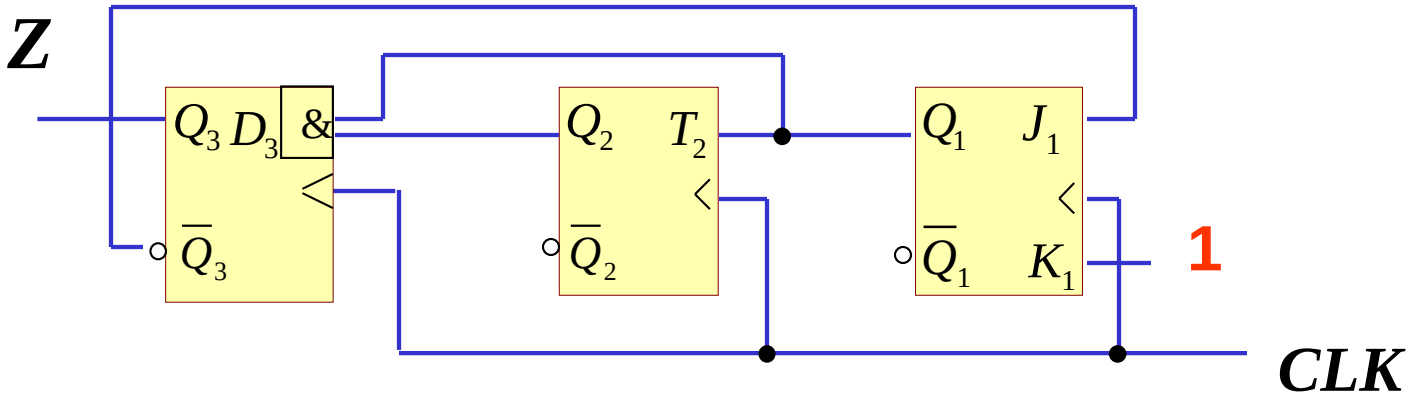
$$\begin{cases} J_1 = \overline{Q_3}^n \\ K_1 = 1 \end{cases}$$



$$Z = Q_3^n$$

$D_3 = Q_2^n Q_1^n$　　$T_2 = Q_1^n$　　$\begin{cases} J_1 = \overline{Q}_3^n \\ K_1 = 1 \end{cases}$　　$Z = Q_3^n$

5）电路



与门可以省略　　同步5进制加法计数器

方法 2: 确定用哪种触发器

4) 选择 FF

选 JK-FFs

5) 状态方程Q^{n+1}及控制输入– J, K

状态图

Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1

JK-FF 驱动表

$Q^n \to Q^{n+1}$		J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

$Q_2^n \Rightarrow Q_2^{n+1}$		J_2
0	0	0
0	0	0
0	0	0
0	1	1
1	0	X
X	X	X
X	X	X
X	X	X

得到 2#-FF 控制输入 J_2 驱动卡诺图

J_2	$Q_1^nQ_0^n$ 00	01	11	10
Q_2^n 0	0	0	1	0
1	×	×	×	×

状态图

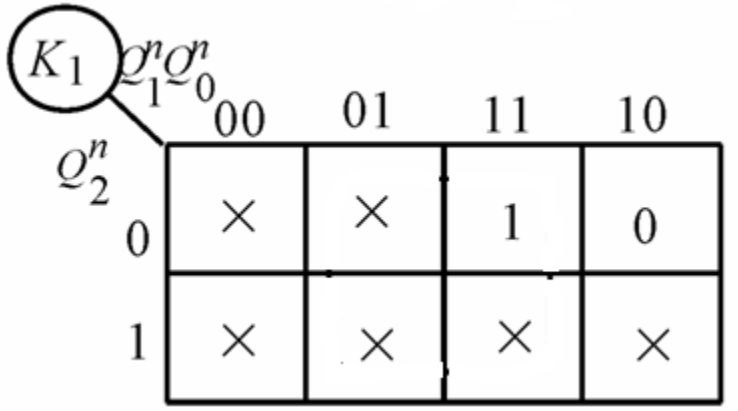
Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1

JK-FF 驱动表

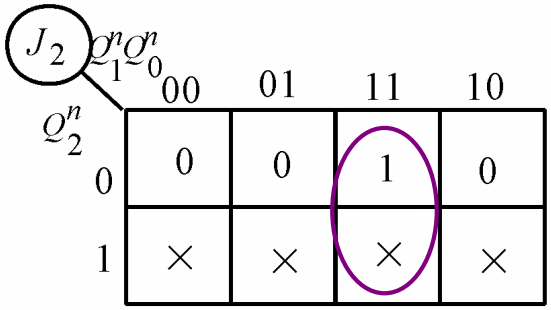
$Q^n \to Q^{n+1}$		J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Q_1^n	$\Rightarrow$	Q_1^{n+1}	K_1
0		0	X
0		1	X
1		1	0
1		0	1
0		0	X
X		X	X
X		X	X
X		X	X

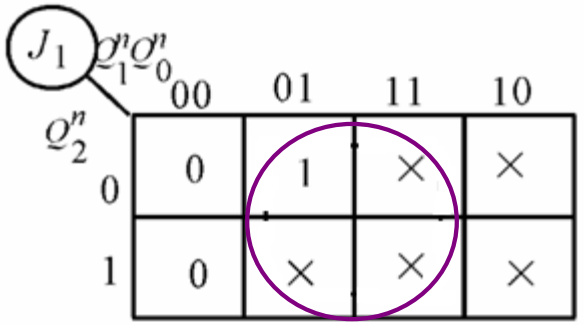
得到 1#-FF 控制输入 K_1 驱动卡诺图



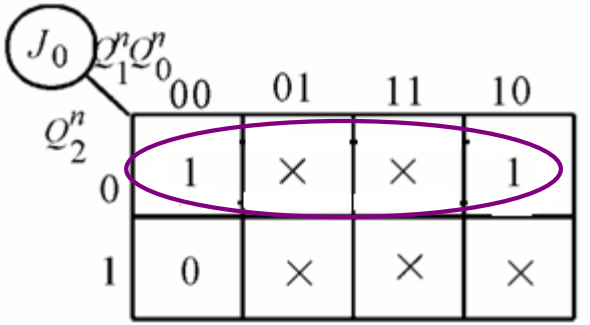
得到各个触发器控制输入驱动卡诺图及控制输入



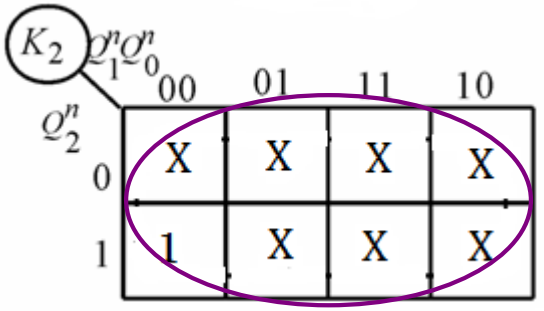
$$J_2 = Q_1^n Q_0^n$$



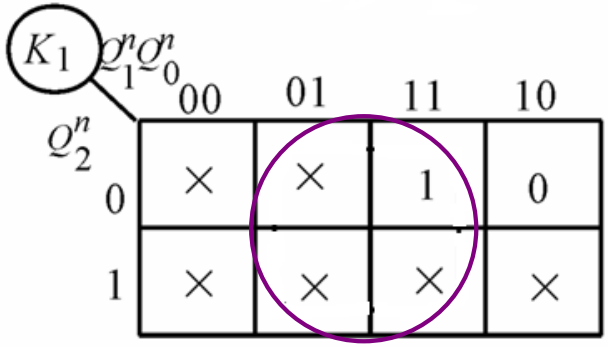
$$J_1 = Q_0^n$$



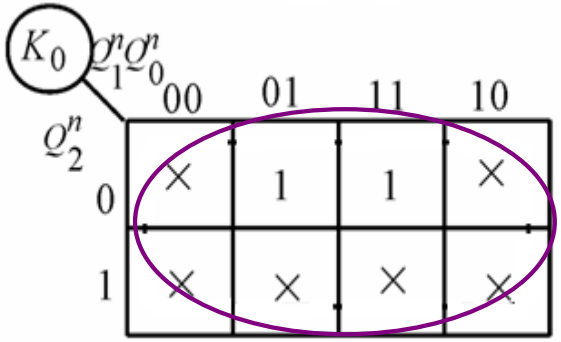
$$J_0 = \overline{Q_2^n}$$



$$K_2 = 1$$

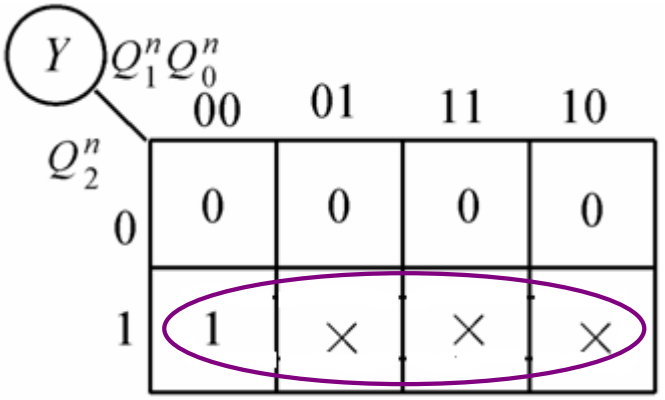


$$K_1 = Q_0^n$$



$$K_0 = 1$$

输出卡诺图



状态表

Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	0	1

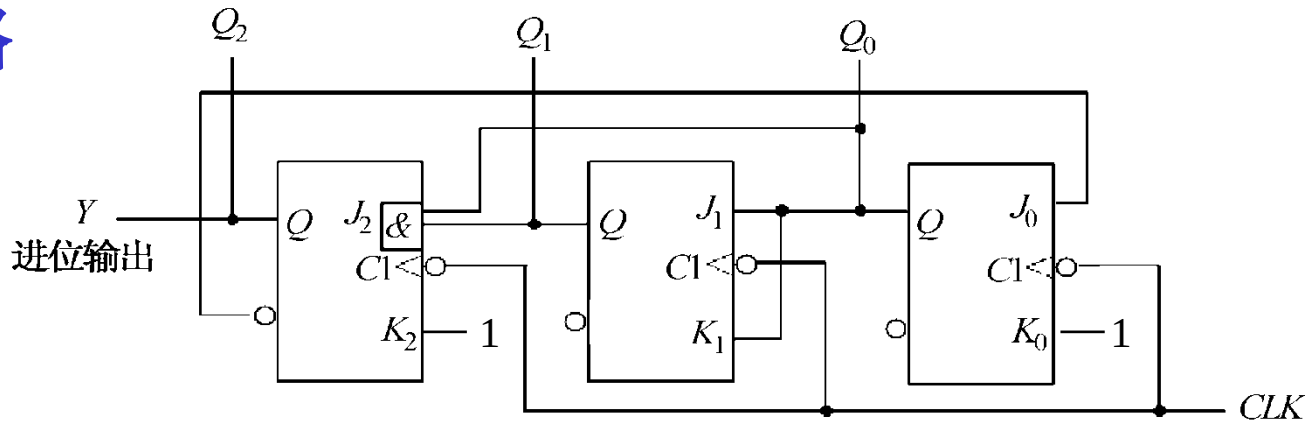
$$Y = Q_2^n$$

$$\begin{cases} J_2 = Q_1^nQ_0^n \\ K_2 = 1 \end{cases}$$

$$\begin{cases} J_1 = Q_0^n \\ K_1 = Q_0^n \end{cases}$$

$$\begin{cases} J_0 = \overline{Q_2^n} \\ K_0 = 1 \end{cases}$$

6) 电路



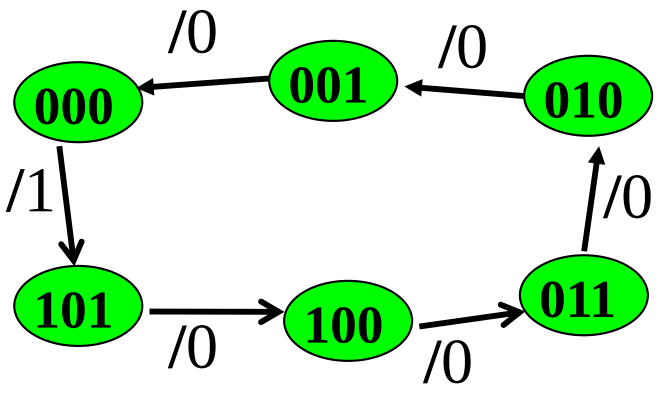
用JK-FF实现同步5进制加法计数器

例 2.　设计 M-6 减法计数器

6 个状态　　直接用3位数编码　　$Q_3Q_2Q_1$

借位输出 Z

/ Z



Z

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	0

Q_3^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	1

Q_2^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	1
1	0	1	Φ	0

Q_1^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	1	Φ	1
1	0	0	Φ	0

Q_3^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	1

$$Q_3^{n+1} = \overline{Q_3}\ \overline{Q_2}\ \overline{Q_1} + Q_3Q_1$$

$$D_3 = \overline{Q_3}\ \overline{Q_2}\ \overline{Q_1} + Q_3Q_1$$

Q_2^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	0	0	Φ	1
1	0	1	Φ	0

$$Q_2^{n+1} = Q_2Q_1 + Q_3\overline{Q_1}$$

$$D_2 = Q_2Q_1 + Q_3\overline{Q_1}$$

Q_1^{n+1}

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	1	Φ	1
1	0	0	Φ	0

$$Q_1^{n+1} = \overline{Q_1}$$

$$D_1 = \overline{Q_1}$$

Z

Q_1^n \ $Q_3^nQ_2^n$	00	01	11	10
0	1	0	Φ	0
1	0	0	Φ	0

$$Z = \overline{Q_3}\ \overline{Q_2}\ \overline{Q_1}$$

电路图略

例 3. (例6.5)

设计一个串行数据检测器。该检测器有一个输入端 X。电路的功能是对输入信号进行检测。当连续输入三个1（以及三个以上1）时，该电路输出 $Y = 1$，否则输出 $Y = 0$。

1）根据设计要求，设定状态，画出状态转换图。

S_0 —初始状态或没有收到1时的状态；

S_1 —收到一个1后的状态；

S_2 —连续收到两个1后的状态；

S_3 —连续收到三个1（以及三个以上1）后的状态。

X=1，收到一个 “1”

S_0—初始状态或没有收到1时的状态；

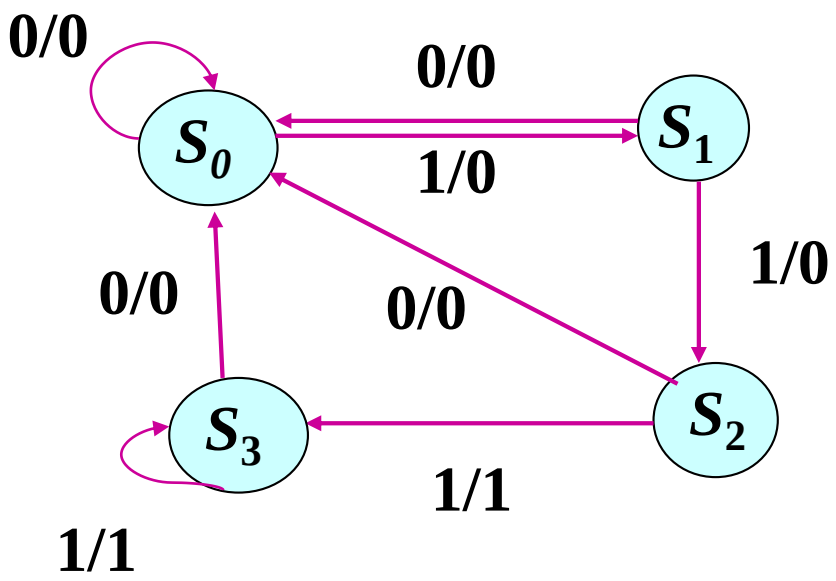
S_1—收到一个1后的状态；

S_2—连续收到两个1后的状态；

S_3—连续收到三个1（以及三个以上1）后的状态。

X=1, 收到一个 “1”

输入三个1（以及三个以上1）时，输出Y = 1



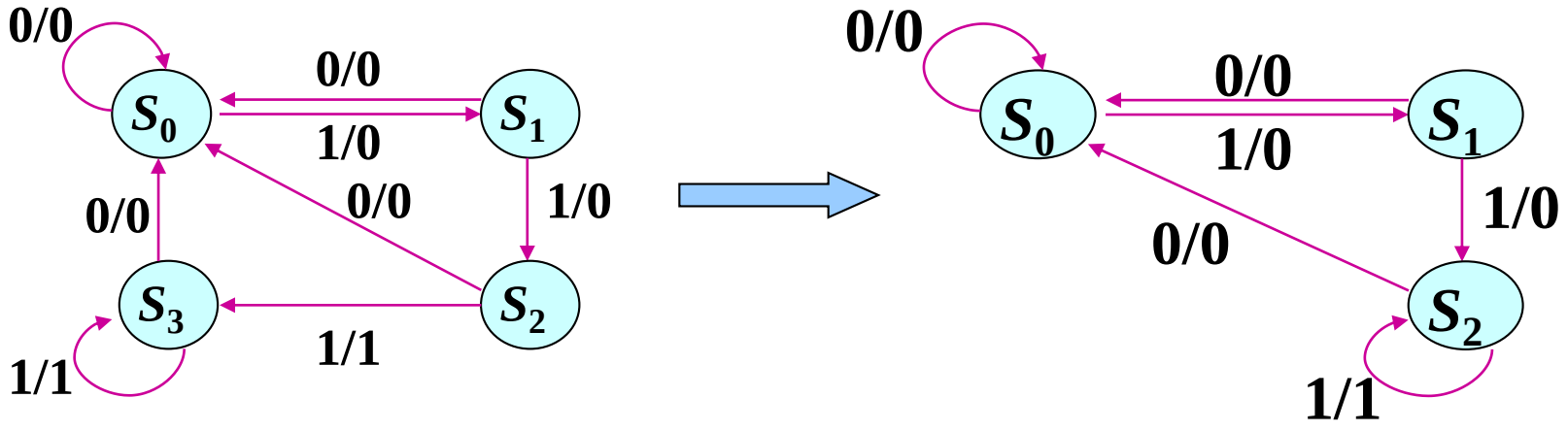
2）状态化简

状态化简： 合并等效状态

等效状态:

在相同的输入条件下，输出相同、次态也相同的状态。

S_2 和 S_3 是等效状态，将S_2 和 S_3 合并为S_2



3）状态分配、编码

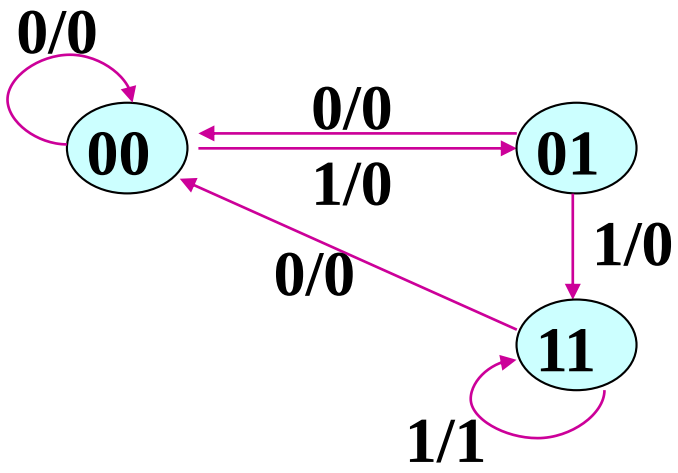
Set $S_0 = 00$

$S_1 = 01$

$S_2 = 11$

编码可以不连续

编码后的状态图



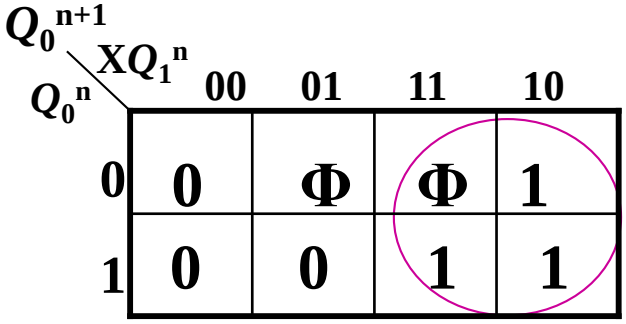
状态表

X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	Φ	Φ	Φ
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	Φ	Φ	Φ
1	1	1	1	1	1

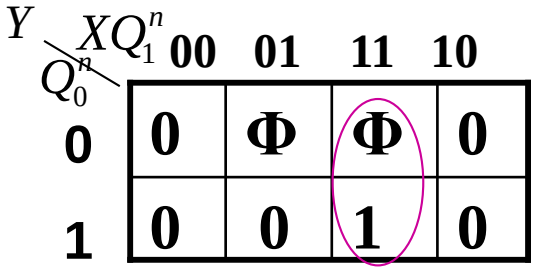
4) 选触发器及控制输入

X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	Φ	Φ	Φ
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	Φ	Φ	Φ
1	1	1	1	1	1

$$Q_1^{n+1} = XQ_0^n = D_1 \qquad D_1 = XQ_0^n$$



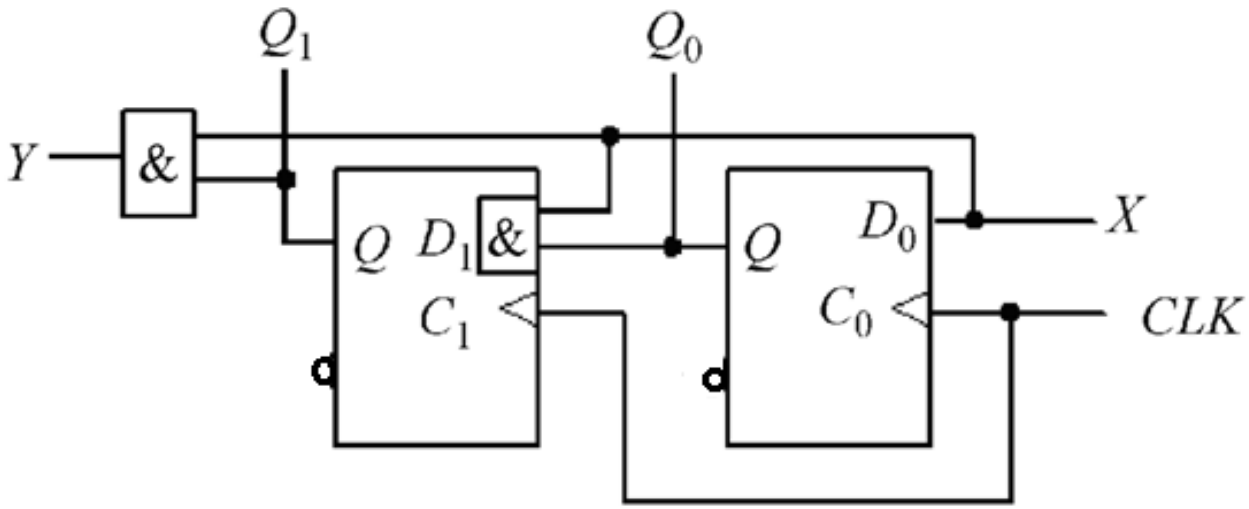
$$Q_0^{n+1} = X = D_0 \qquad D_0 = X$$

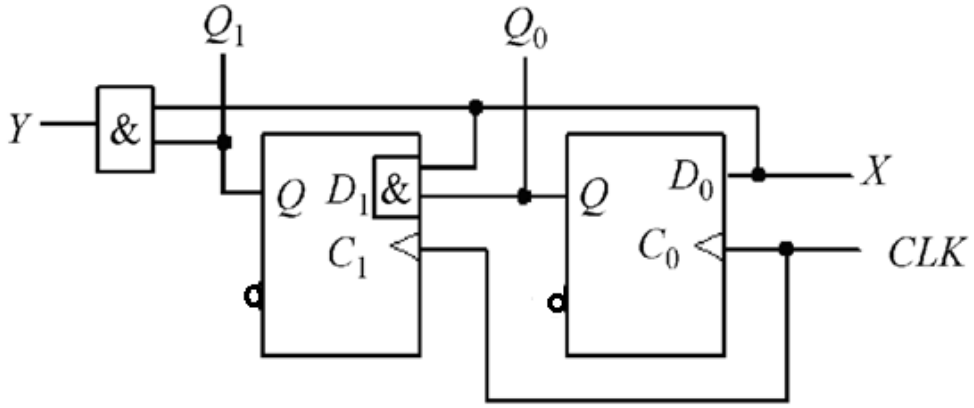


$$Y = XQ_1^n$$

5) 电路

2 D-FFs $D_1 = XQ_0^n$ $D_0 = X$ $Y = XQ_1^n$





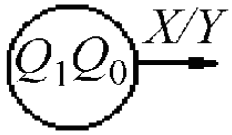
$$Q_1^{n+1} = XQ_0^n$$

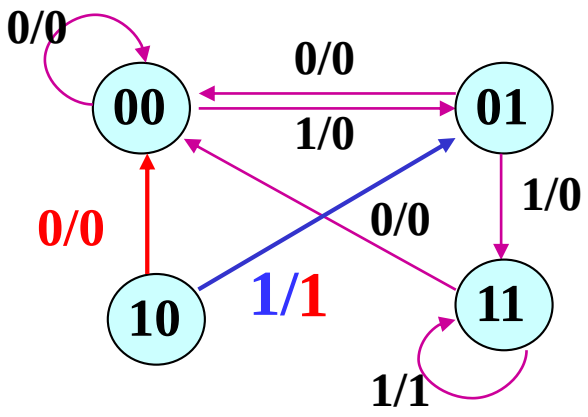
$$Q_0^{n+1} = X$$

$$Y = XQ_1^n$$

6）自启动

从电路的状态图分析





可以自启动

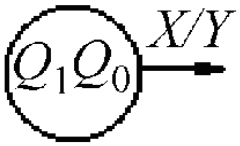
但其功能错误，

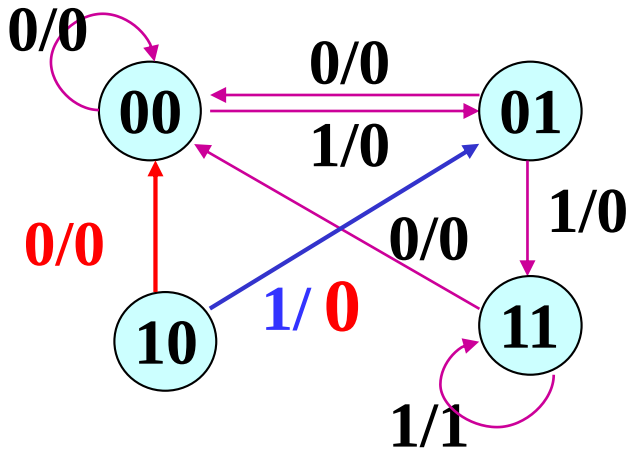
输出应设置为0，才符合题意

检测 连续输入三个及以上个1时，电路输出$Y = 1$。

自启动

让110对应的输出为0.





状态表

X	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	1	1	1

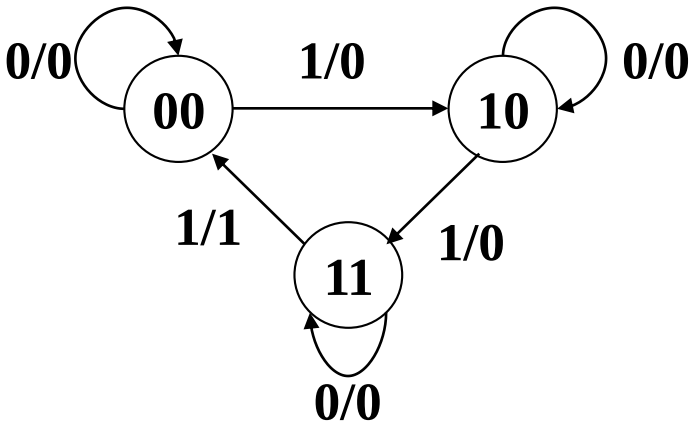
Y / XQ_1^n / Q_0^n	00	01	11	10
0	0	0	0	0
1	0	0	1	0

$Y = XQ_1^nQ_0^n$

既实现自启动，也符号题意.

可以在最初设计时就考虑自启动问题.

例 4. 按照下面状态图设计电路 (例6.6)



状态表 (根据状态图)

X/*Z*

X	Q_2^n	Q_1^n	Q_2^{n+1}	Q_1^{n+1}	Z
0	0	0	0	0	0
0	0	1	ϕ	ϕ	ϕ
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	ϕ	ϕ	ϕ
1	1	0	1	1	0
1	1	1	0	0	1

确定状态及状态表

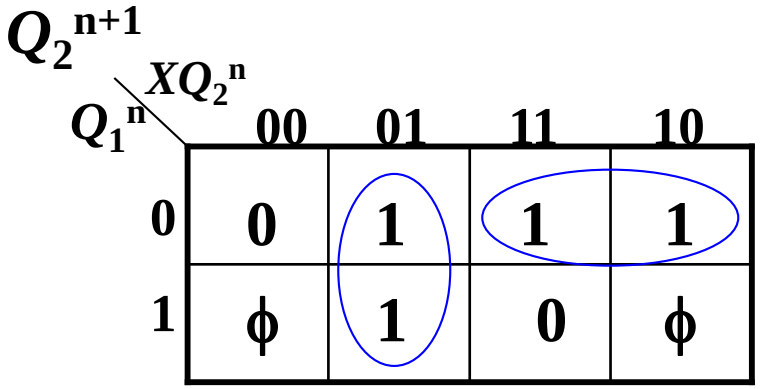
状态数 ⟹ (确定) FF 个数

n FFs → 2^n 状态

$2^{n-1} \le$ 状态数 $\le 2^n$ → *n* FFs

$3 < 2^2$ 需要 2 个 FF

选择 FF (K-map, 圈 *1*)



2# FF

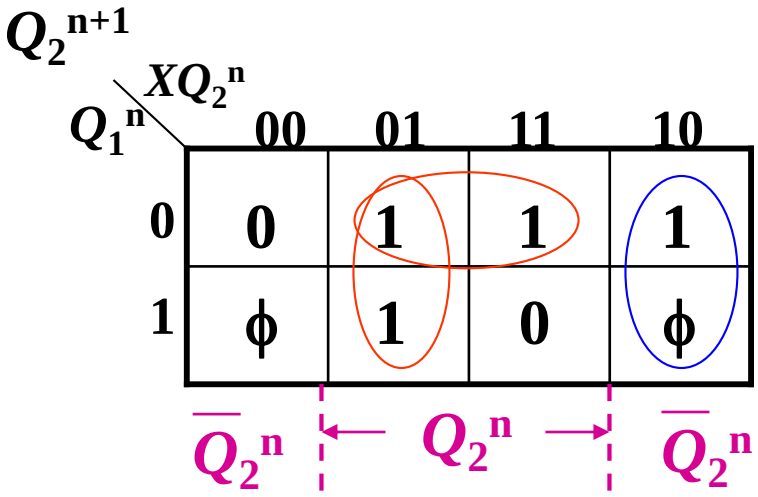
$$Q_2^{n+1} = \overline{X}Q_2^n + X\overline{Q_1}^n$$

2 个圈，选择 JK-FF

$$Q_2^{n+1} = J_2\overline{Q}_2^n + \overline{K}_2Q_2^n$$

找到 $J_2 = ?$ $K_2 = ?$

不能按上面方法圈，必须圈成 $Q_2^{n+1} =$ ___ $\overline{Q}_2^n +$ ___ Q_2^n



$$Q_2^{n+1} = X\overline{Q}_2^n + (\overline{X} + \overline{Q}_1^n)Q_2^n$$

$$= X\overline{Q}_2^n + \overline{XQ_1}^n Q_2^n$$

$$\therefore \begin{cases} J_2 = X \\ K_2 = XQ_1^n \end{cases}$$

能找到系数（控制变量）时尽量化简；找不到系数时，牺牲化简也要找到系数。

X	Q_2^n	Q_1^n	Q_2^{n+1}	Q_1^{n+1}	Z
0	0	0	0	0	0
0	0	1	ϕ	ϕ	ϕ
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	ϕ	ϕ	ϕ
1	1	0	1	1	0
1	1	1	0	0	1

1# FF

Q_1^{n+1}

Q_1^n \ XQ_2^n	00	01	11	10
0	0	0	1	0
1	ϕ	1	0	ϕ

$\rightarrow \overline{Q}_1^n$

$\rightarrow Q_1^n$

JK-FF

$$Q_1^{n+1} = J_1\overline{Q}_1^n + \overline{K}_1 Q_1^n$$

$$= XQ_2^n\overline{Q}_1^n + \overline{X}Q_1^n$$

$$\therefore \begin{cases} J_1 = XQ_2^n \\ K_1 = X \end{cases}$$

输出 Z

Z

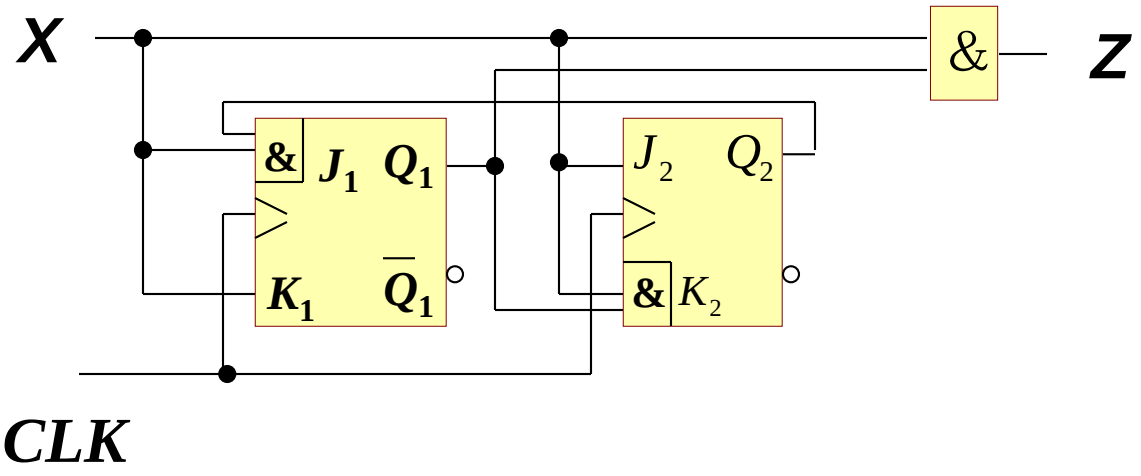
Q_1^n \ XQ_2^n	00	01	11	10
0	0	0	0	0
1	Φ	0	1	Φ

$$Z = XQ_1^n$$

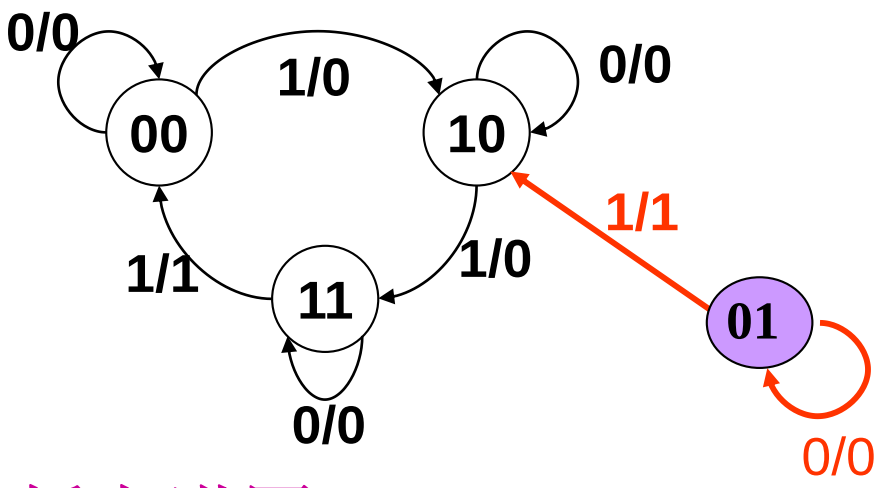
电路

$$\begin{cases} J_2 = X \\ K_2 = XQ_1^n \end{cases}$$

$$\begin{cases} J_1 = XQ_2^n \\ K_1 = X \end{cases}$$



讨论：01 状态



Q_2^{n+1} \ XQ_2^n / Q_1^n	00	01	11	10
0	0	1	1	1
1	0	1	0	1

Q_1^{n+1} \ XQ_2^n / Q_1^n	00	01	11	10
0	0	0	1	0
1	1	1	0	0

Z \ XQ_2^n / Q_1^n	00	01	11	10
0	0	0	0	0
1	0	0	1	1

分析卡诺图 K-map

$XQ_2^nQ_1^n$ = 001, (Z=0)

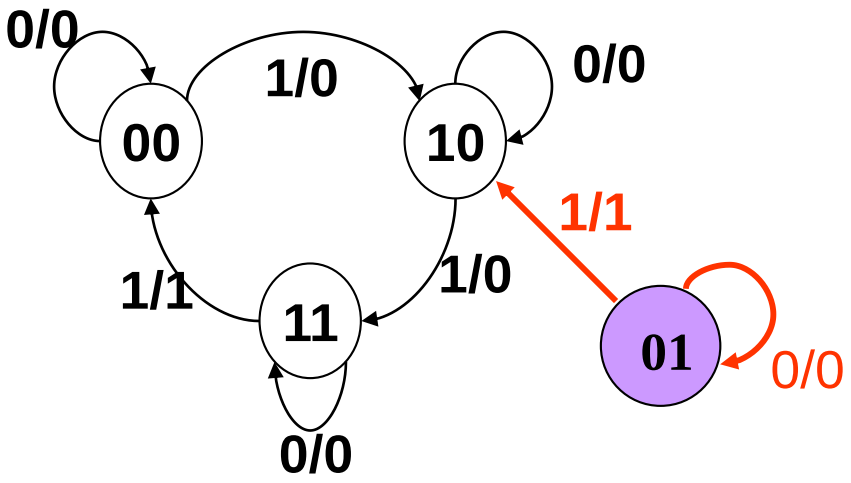
Next state $Q_2^{n+1}Q_1^{n+1}$ =01,

$XQ_2^nQ_1^n$ = 101时, (Z=1)

Next state $Q_2^{n+1}Q_1^{n+1}$ =10,

实现自启动

但是要分析输出的物理意义（即电路功能）是否正确。



此电路为可控模3加法计数器。

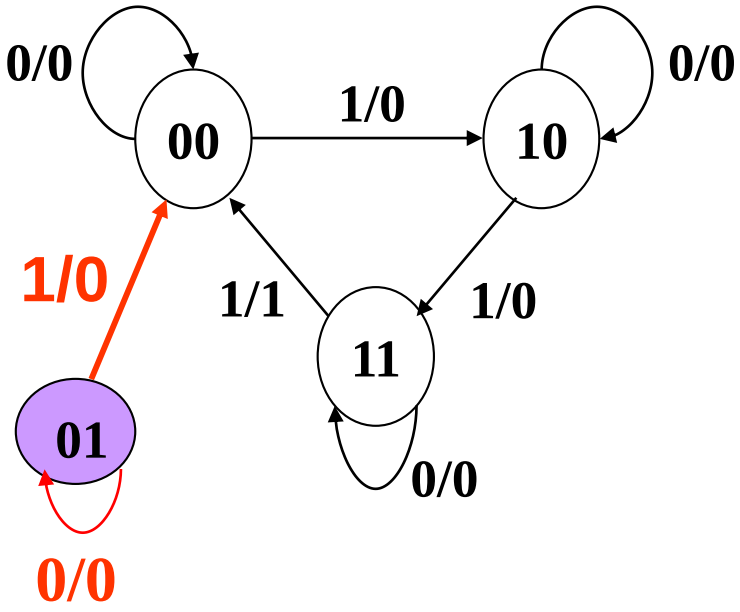
X=0，保持原状态；
X=1，作加法计数。

输出Y=1，为进位输出。

显然自启动之后电路功能出现错误。

应该将X=1时01状态的输出设为0。

在设计电路时



X=0，保持原状态；
X=1，作加法计数（从0开始）。

在填状态表时不能填 ϕ

状态表

X	Q_2^n	Q_1^n	Q_2^{n+1}	Q_1^{n+1}	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	0	0	1

才能符合电路要求

例5. 设计一个自动售饮料机的逻辑电路。它的投币口每次只能投入一枚五角或一元的硬币。投入一元五角钱硬币后，机器会自动给出一杯饮料；投入两元（两个一元）硬币后，在给出饮料的同时找回一枚五角硬币。

解:

输入: {投入 ¥1.0, A=1; 投入 ¥0.5, B=1}

输出: {出饮料, Y=1; 找钱, Z=1}

状态:

3个状态

S_0 : 初始 (未投币)

S_1 : 投入 ¥0.5,

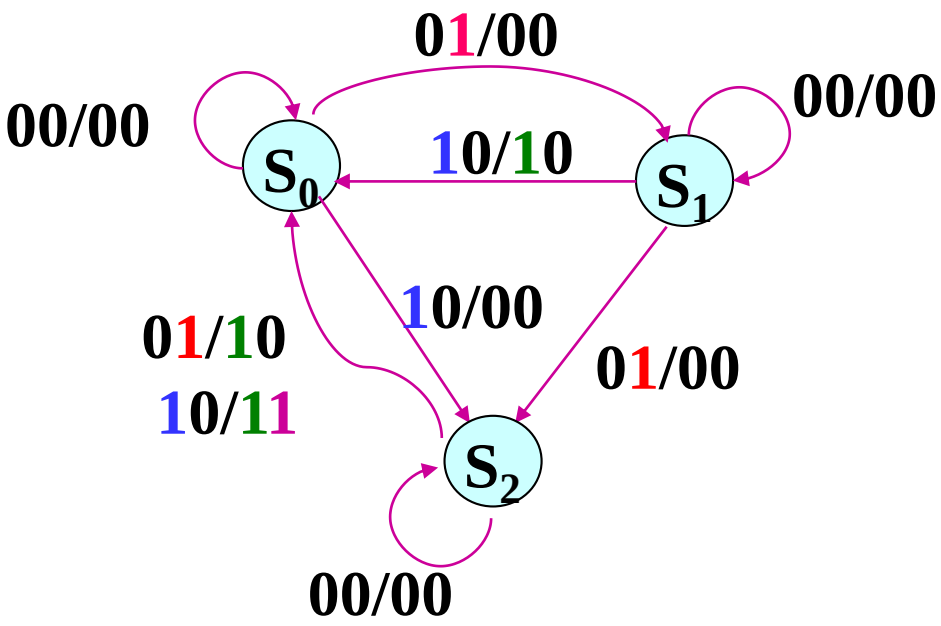
S_2 :投入 ¥1.0 (一个 ¥1.0 或两个 ¥0.5)

再投入 ¥0.5, 返回 S_0, 输出 Y=1, Z=0;

再投入¥1.0, 返回 S_0, 输出 Y=1, Z=1 (找回 ¥0.5).

多输入，多输出

AB /YZ



S_0: 投入 ¥0.5, S_1

S_0:投入¥1.0, S_2

S_1:投入¥0.5, S_2

S_1:投入¥1.0, S_0
饮料

S_2:投入¥0.5, S_0
饮料

S_2:投入¥1.0, S_0
饮料 和 找钱

A：¥1.0
B：¥0.5
Y：饮料
Z：找钱

S_0：初始
S_1：¥0.5
S_2：¥1.0

$Q_1^nQ_0^n$

编码

$S_0 \rightarrow 00$

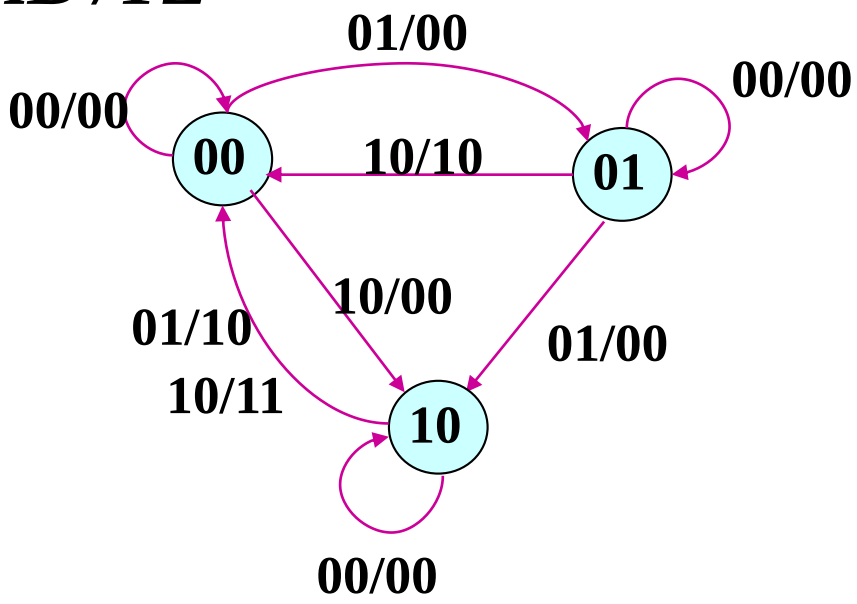
$S_1 \rightarrow 01$

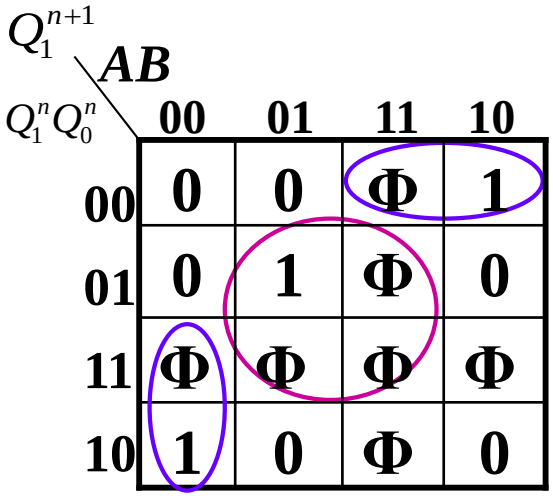
$S_2 \rightarrow 10$

状态表：

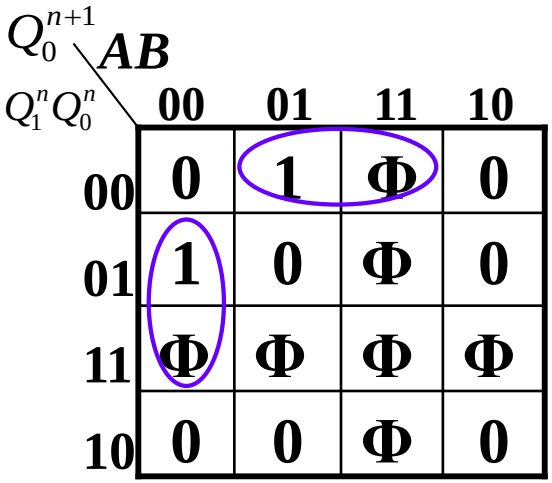
$A\ B\ Q_1^n\ Q_0^n$	$Q_1^{n+1}\ Q_0^{n+1}\ Y\ Z$
0 0 0 0	0 0 0 0
0 0 0 1	0 1 0 0
0 0 1 0	1 0 0 0
0 0 1 1	Φ Φ Φ Φ
0 1 0 0	0 1 0 0
0 1 0 1	1 0 0 0
0 1 1 0	0 0 1 0
0 1 1 1	Φ Φ Φ Φ
1 0 0 0	1 0 0 0
1 0 0 1	0 0 1 0
1 0 1 0	0 0 1 1
1 0 1 1	Φ Φ Φ Φ
1 1 0 0	Φ Φ Φ Φ
1 1 0 1	Φ Φ Φ Φ
1 1 1 0	Φ Φ Φ Φ
1 1 1 1	Φ Φ Φ Φ

AB /YZ

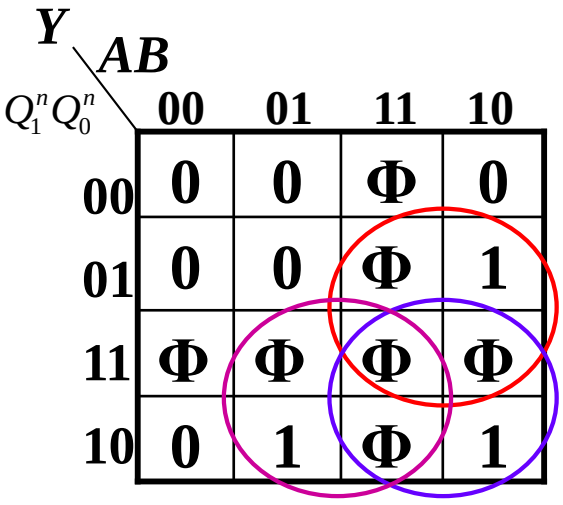




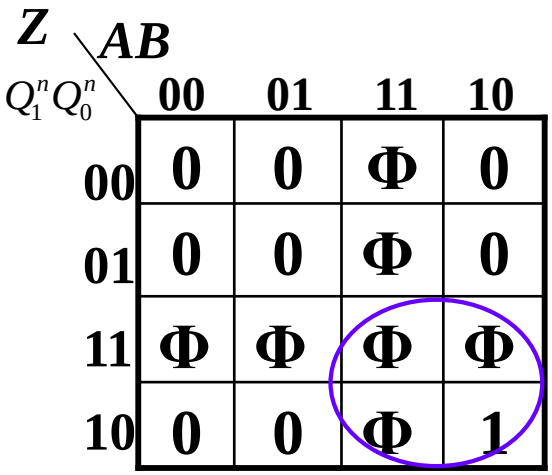
$$Q_1^{n+1} = BQ_0 + A\overline{Q}_1\overline{Q}_0 + \overline{A}\cdot\overline{B}Q_1$$



$$Q_0^{n+1} = B\overline{Q}_1\cdot\overline{Q}_0 + \overline{A}\cdot\overline{B}Q_0$$



$$Y = AQ_0 + AQ_1 + BQ_1$$



$$Z = AQ_1$$

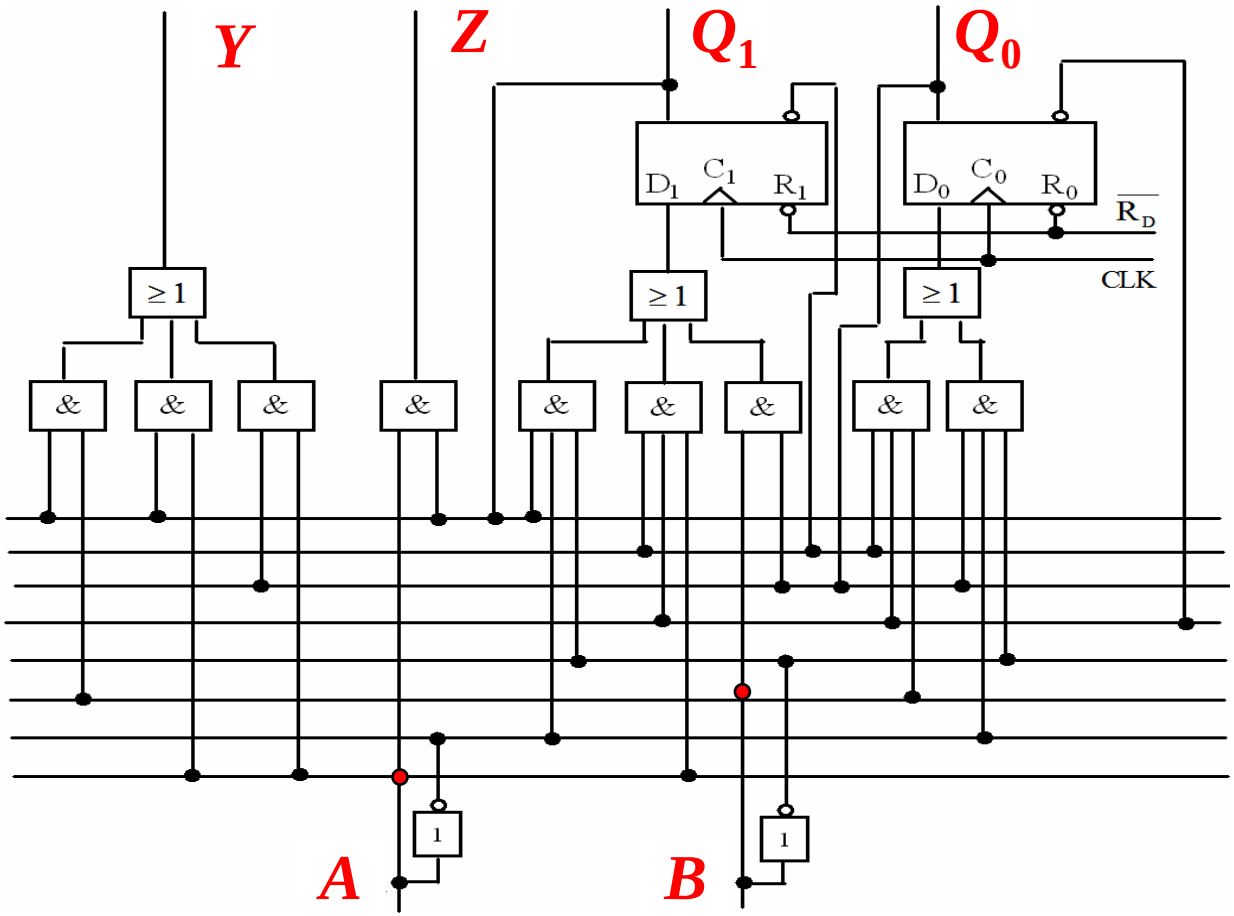
用 D-FF

$$D_1 = BQ_0 + A\overline{Q}_1\overline{Q}_0 + \overline{A}\cdot\overline{B}Q_1$$

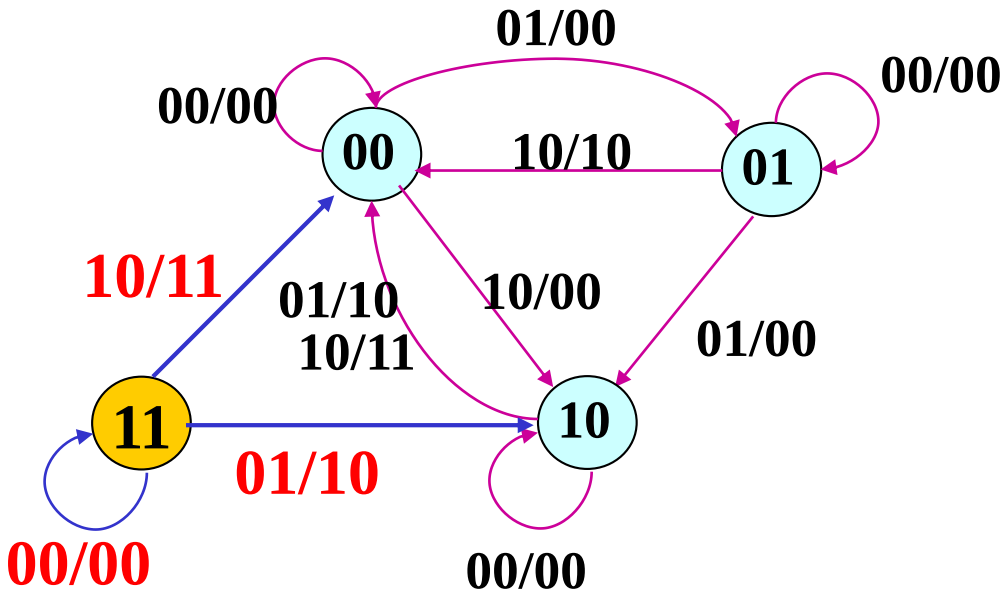
$$D_0 = B\overline{Q}_1\cdot\overline{Q}_0 + \overline{A}\cdot\overline{B}Q_0$$

$$Y = AQ_0 + AQ_1 + BQ_1$$

$$Z = AQ_1$$



由电路得到状态图



在电路处于“11”状态时，

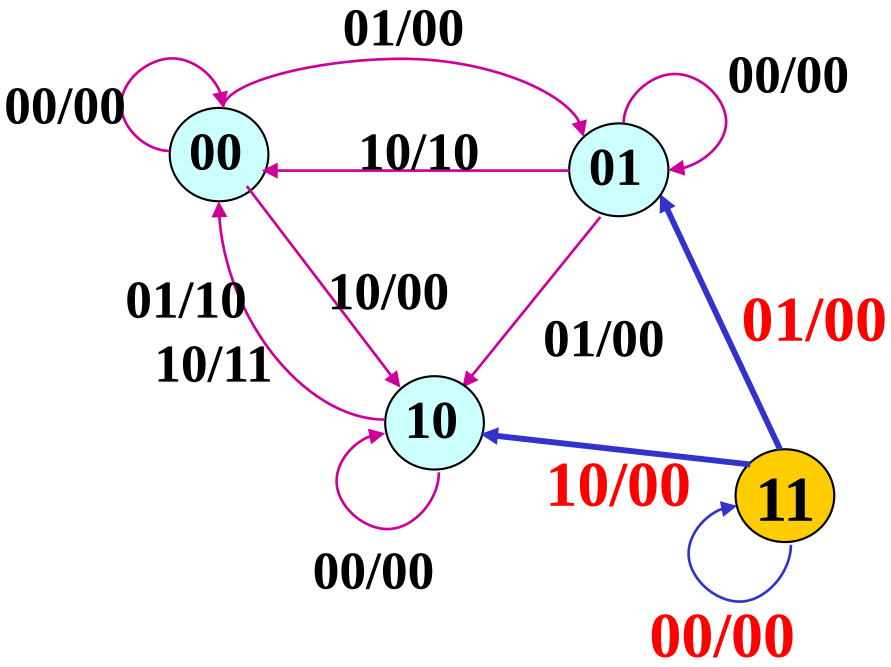
若 AB = 00 (无输入)，Q_1Q_0 = 11, 电路不能自启动;

若AB = 01 或 10, 电路可以自启动，但是找钱系统出错;

A：¥1.0
B：¥0.5
Y：饮料
Z：找钱

所以，电路初始工作时，应首先将 $\overline{R}_D$ 设置为低电平，电路状态从“00”开始.

电路状态图应设计成：



状态表：

A	B	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	1	1
1	0	1	1	1	0	0	0
1	1	0	0	Φ	Φ	Φ	Φ
1	1	0	1	Φ	Φ	Φ	Φ
1	1	1	0	Φ	Φ	Φ	Φ
1	1	1	1	Φ	Φ	Φ	Φ

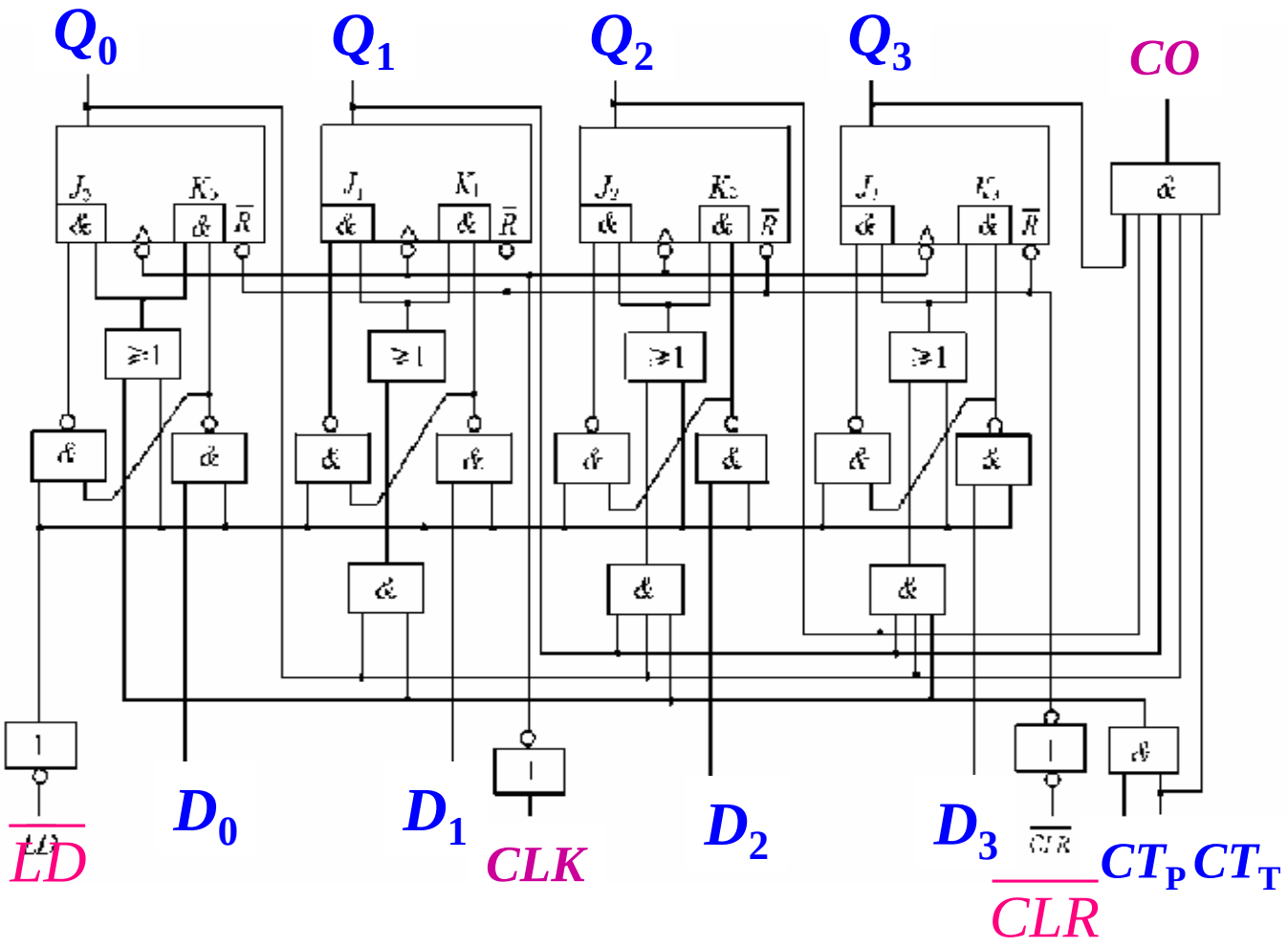
§6.4 计数器 Counter

计数器: 记录*CLK*个数的电路

6.4.1 集成计数器 74161

74161: 二进制同步模16加法计数器，
异步清0功能.

计数器74161 电路

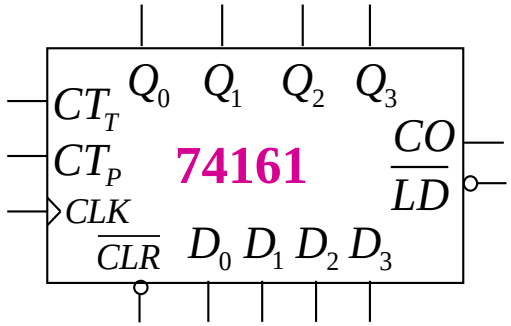


$Q_3Q_2Q_1Q_0$

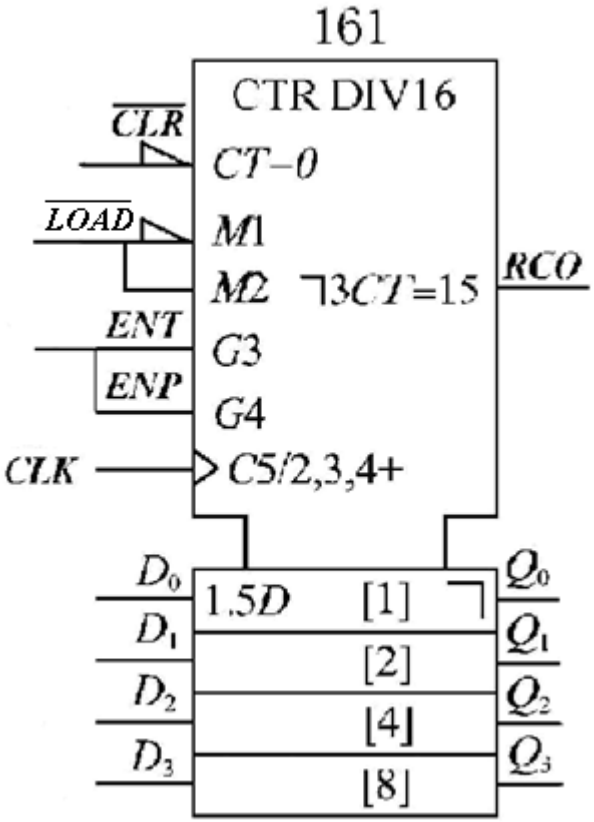
$D_3D_2D_1D_0$

符号

MSB



IEEE



输出 $Q_3\,Q_2\,Q_1\,Q_0$

数据输入 $D_3\,D_2\,D_1\,D_0$

异步清零 $\overline{CLR}$

控制端 $ENT\,(CT_T)$, $ENP\,(CT_P)$

预置端 $\overline{LOAD}$ $\left(\overline{LD}\right)$

进位输出 $RCO\,(CO)$

74161 功能表

$\overline{CLR}$	$\overline{LD}$	ENT	ENP	CLK	$D_0\,D_1\,D_2\,D_3$	功能
0	X	X	X	X	X X X X	Direct set 0
1	0	X	X	↑	$D_0D_1D_2D_3$	Load 预置
1	1	0	X	X	X X X X	保持 RCO=0
1	1	X	0	X	X X X X	保持
1	1	1	1	↑	X X X X	M-16 计数

$Q_3Q_2Q_1Q_0 = 0000$

$Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$

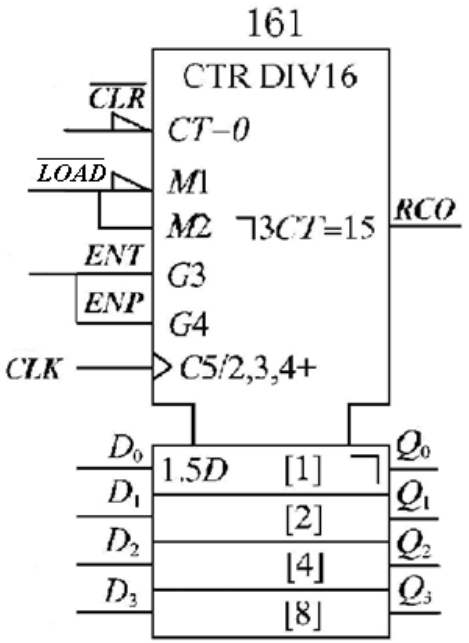
$RCO = ENT \cdot Q_3 \cdot Q_2 \cdot Q_1 \cdot Q_0$

计数时，$ENT = 1$,

当$Q_3Q_2Q_1Q_0 = 1111$时，（M-16）

$RCO = 1$.

其他时刻，$RCO = 0$



例1: 用 74161 实现模11加法计数器　(例6.7)

方法1: 预置归 0 法 （$\overline{LD}$）

$ENT = ENP = 1,\ \overline{CLR} = 1,\qquad D_3D_2D_1D_0 = 0000$

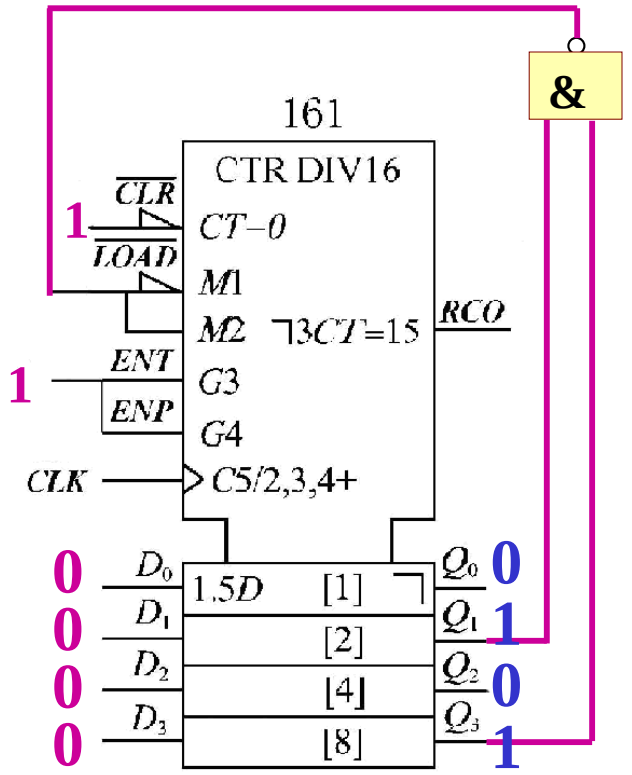
最大状态 1010　最大状态中1端连入一个与非门

输出 $\rightarrow \overline{LD}$

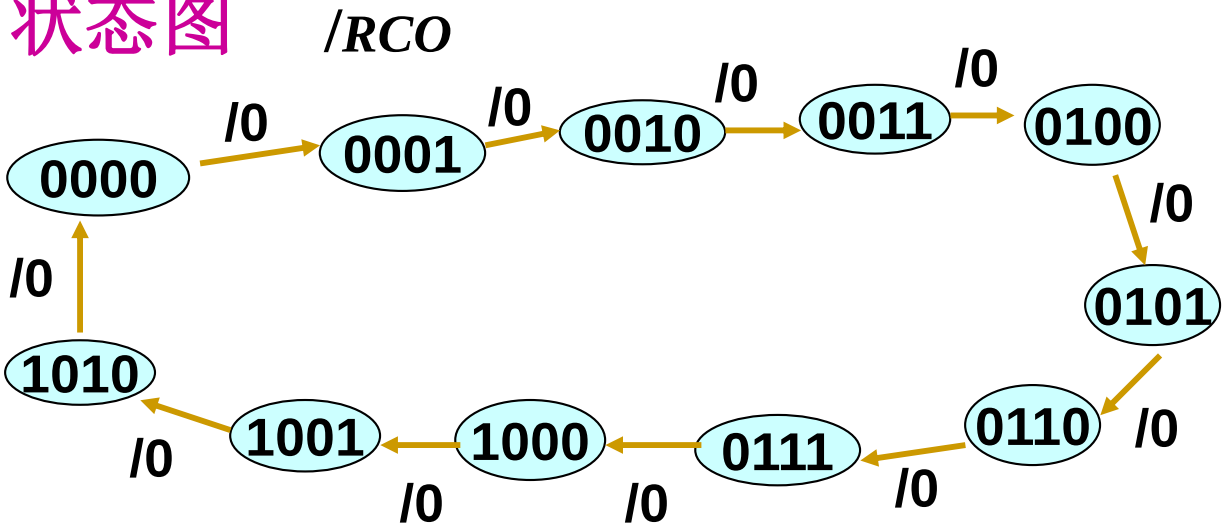
0 →9，与非门 = 1
($\overline{LD}$=1), 计数

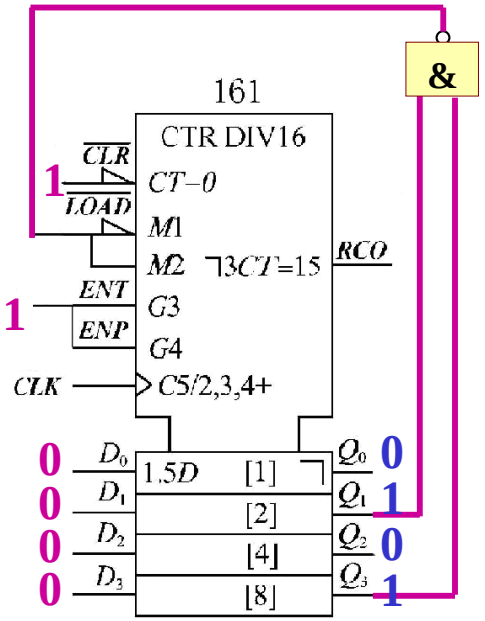
10^{th} CLK 到来,
$Q_3Q_2Q_1Q_0$=1010, $\overline{LD}$=0

下一个 CLK (11^{th}) 到来,
$Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0 = 0000$

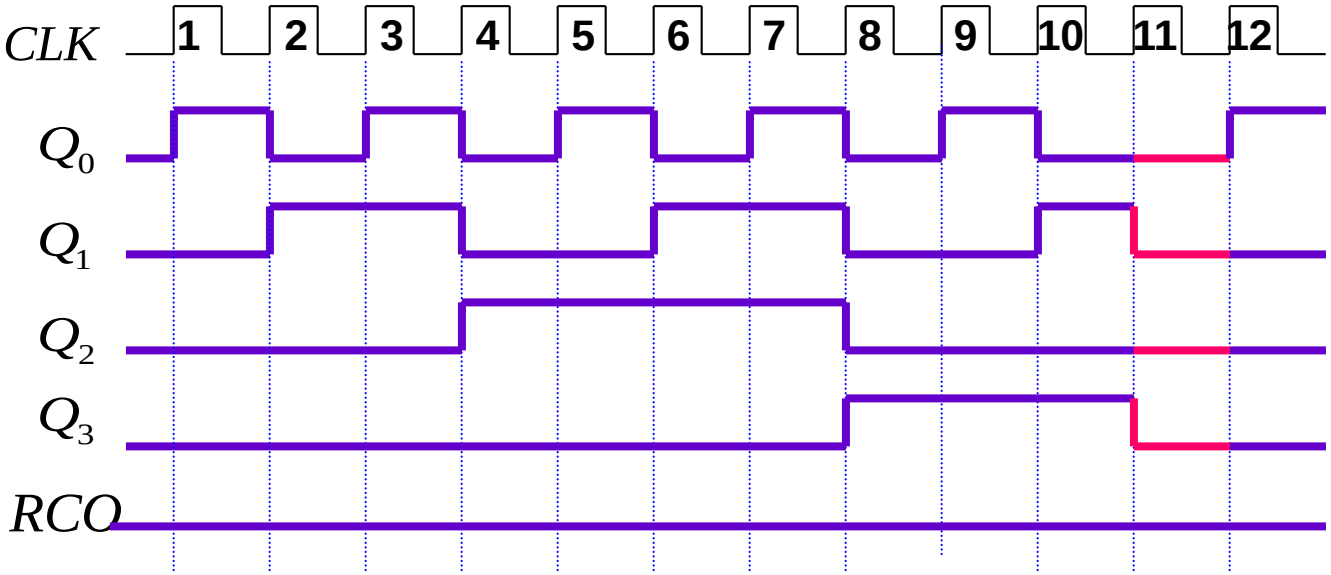


状态图





波形图



Q_0 二分频电路

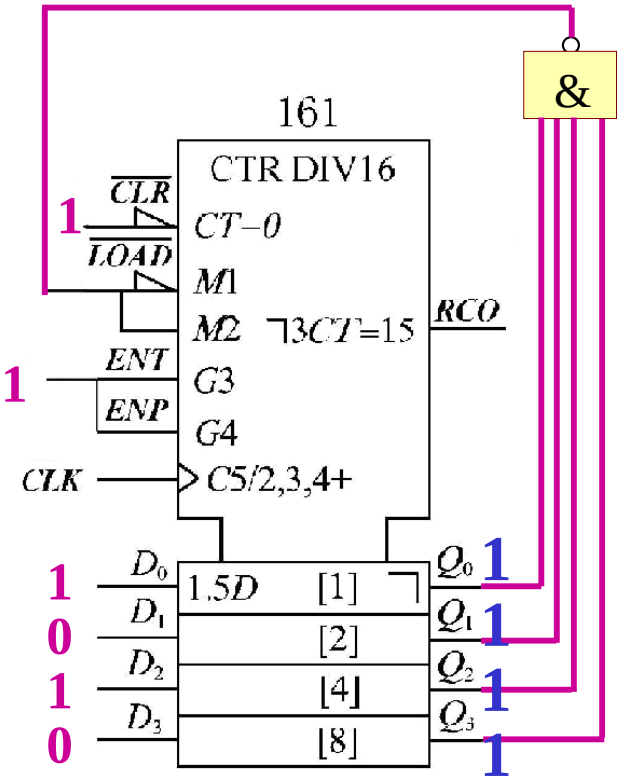
四分频电路

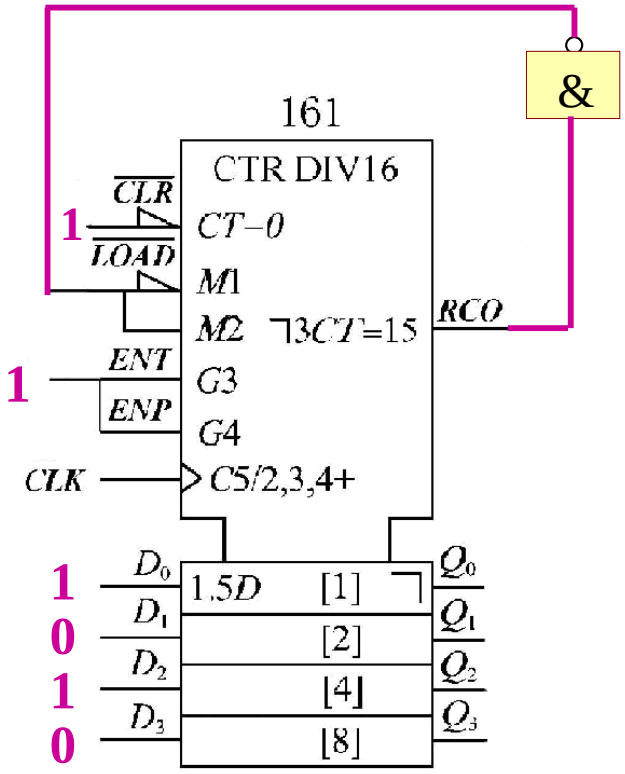
方法 2: 预置补数法

0000 ~ 1111
16 个状态

0000 ~ 1010
11 个状态

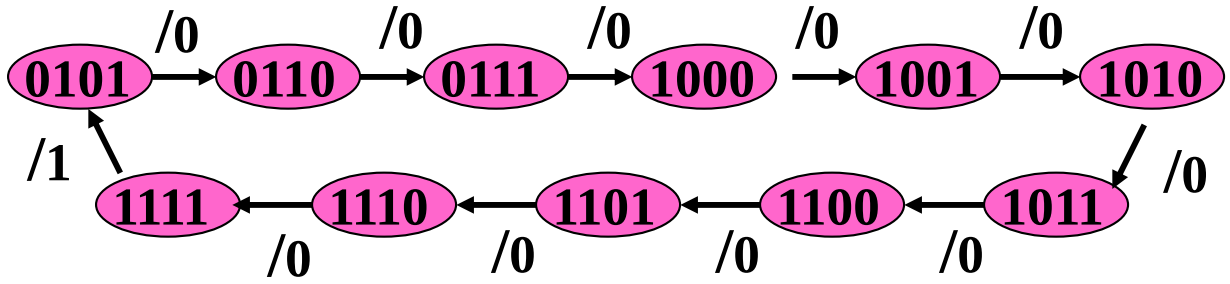
5 (0101) ~ 15 (1111)
11 个状态





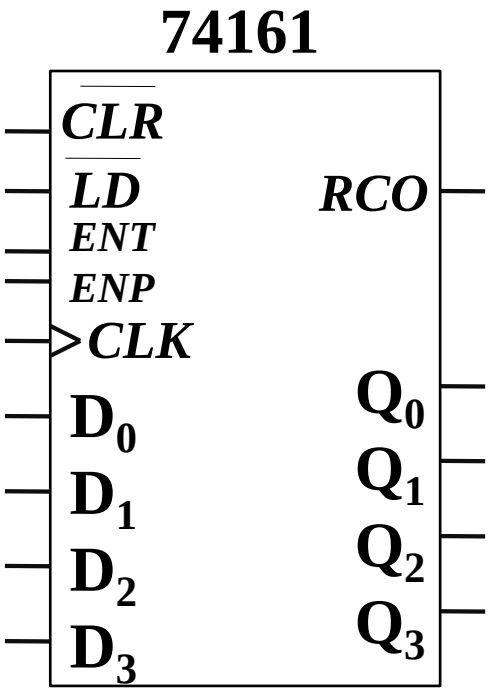
状态图

/RCO



课堂练习：

用预置补数法接模11计数器。要求初始状态为 3 .



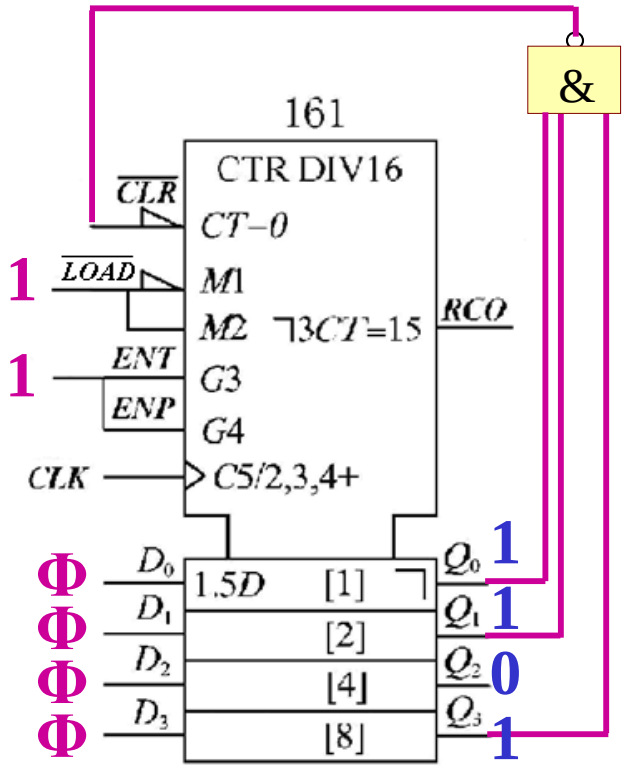
方法 3: 反馈归 0 法 （$\overline{CLR}$）

$ENT = ENP = \overline{LD} = 1$

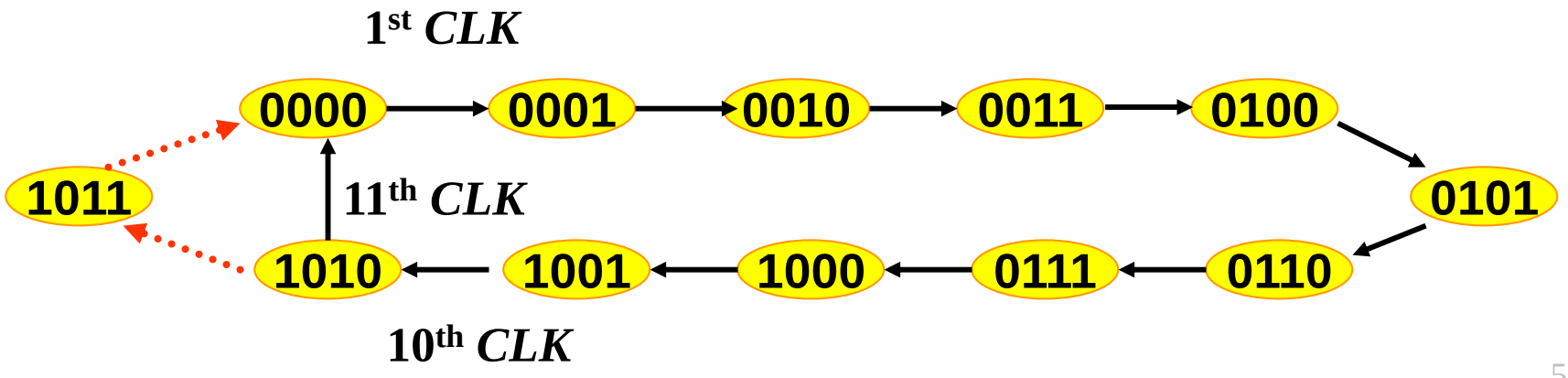
$D_3D_2D_1D_0 = \Phi\ \Phi\ \Phi\ \Phi$

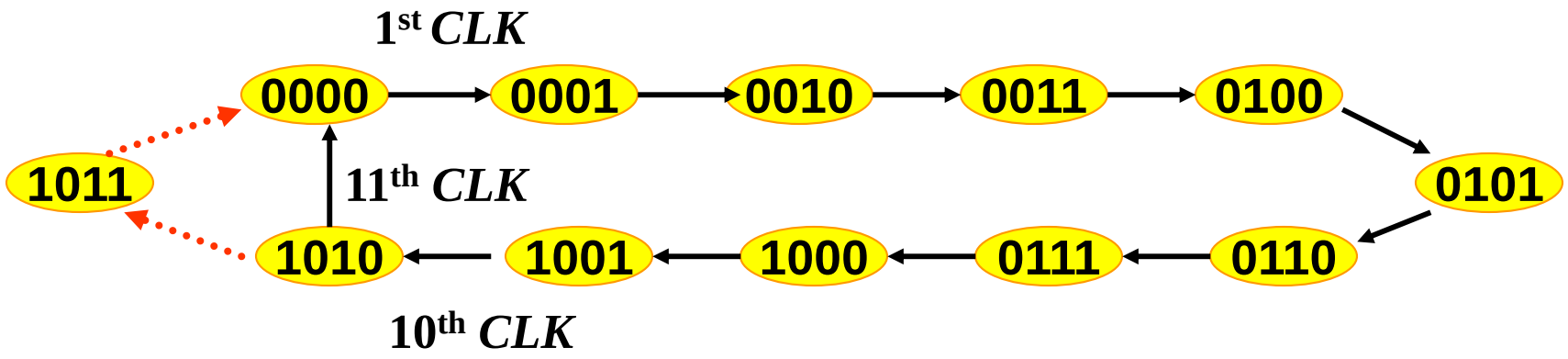
$Q_3Q_2Q_1Q_0 = 1011$

与非门 → C$\overline{LR}$

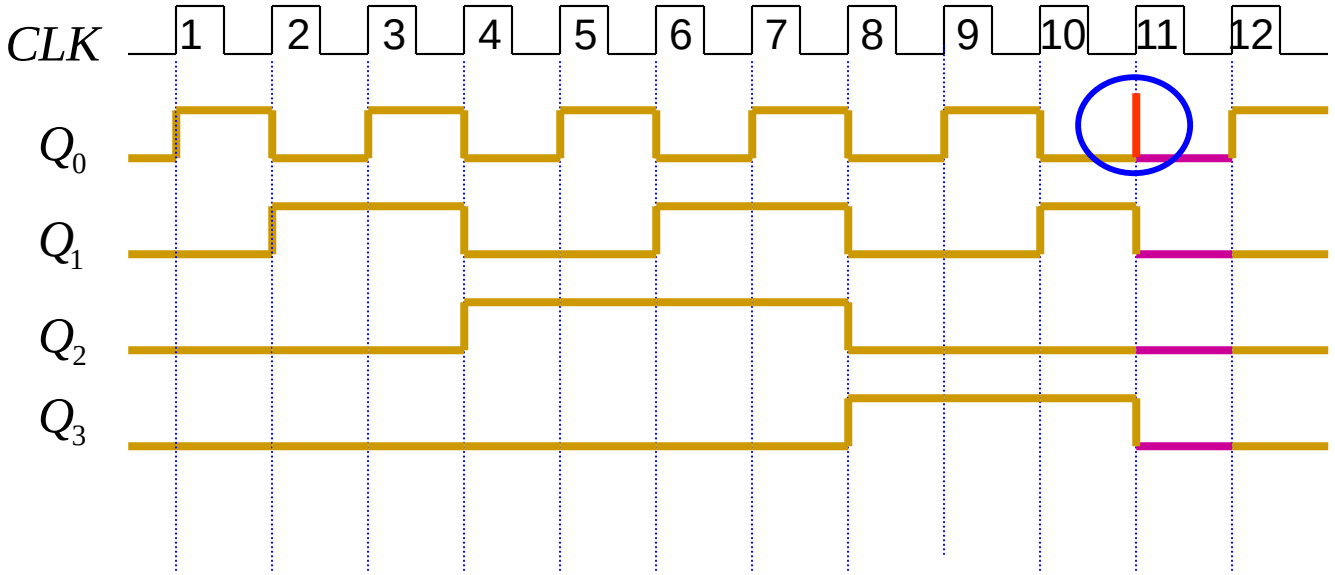


状态图





波形图

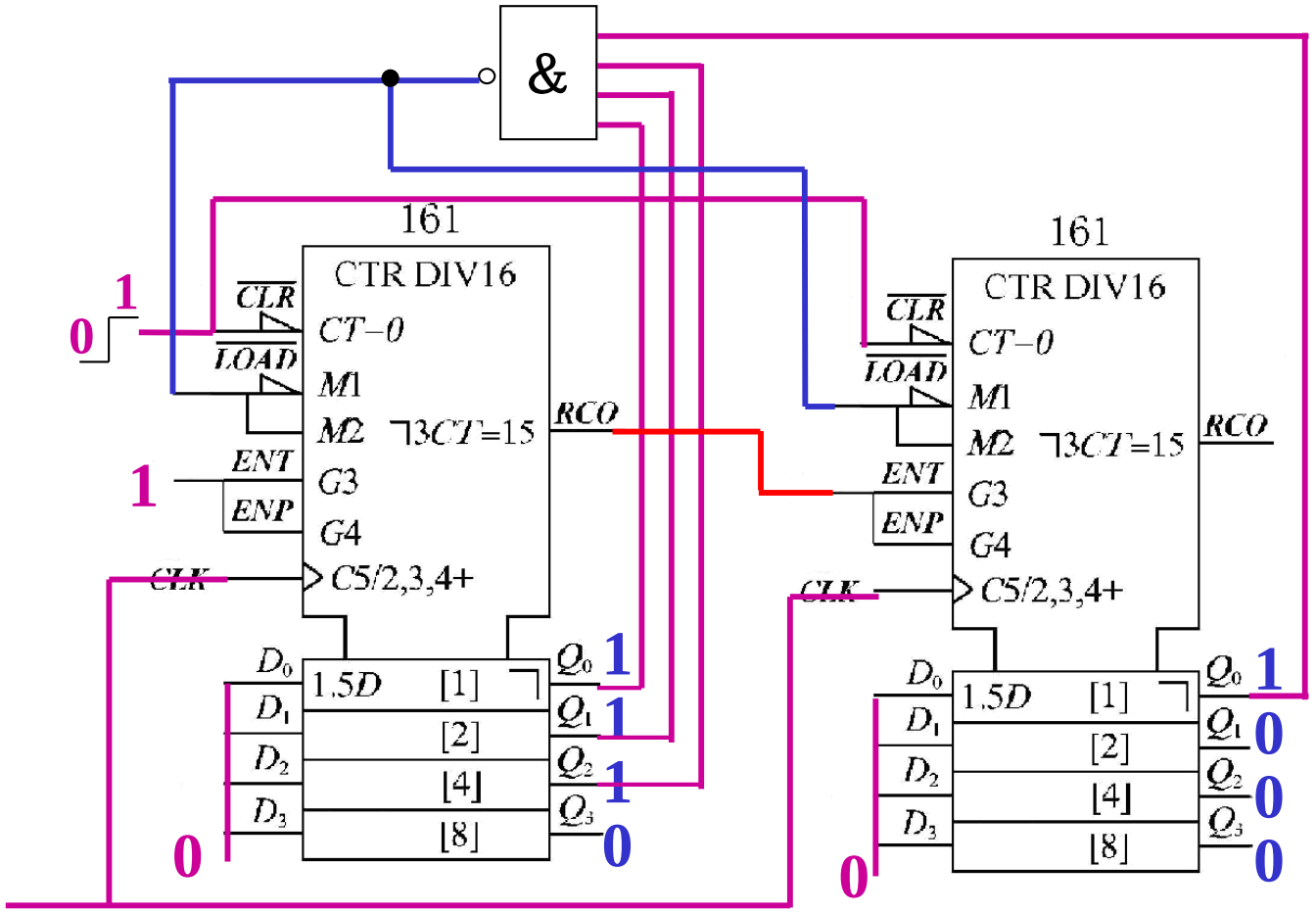


毛刺
（假信号）

方法1最好，用$\overline{LD}$端归0。　　用虚线连接不稳定状态

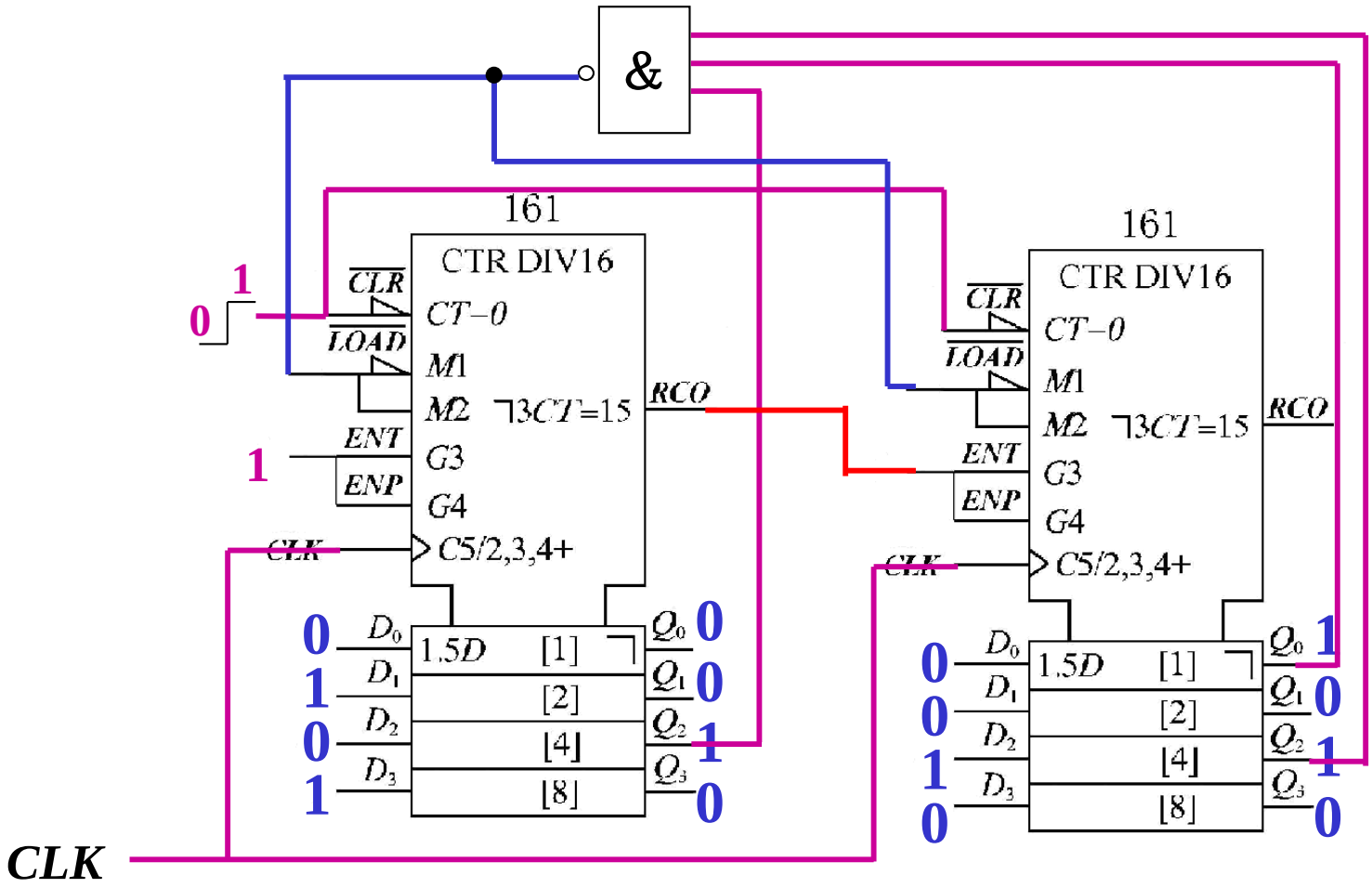
例 2：用74161 设计模 24 计数器

最大状态: 23 (10111)　　**两个 74161**



例 3：求下图计数器电路的模值.

M = ?



终点： 01010100 ＝ 84

补： 01001010 ＝ 74

M = 84 – 74 + 1 = 11

6.4.2 IC 计数器 74160 (M-10)

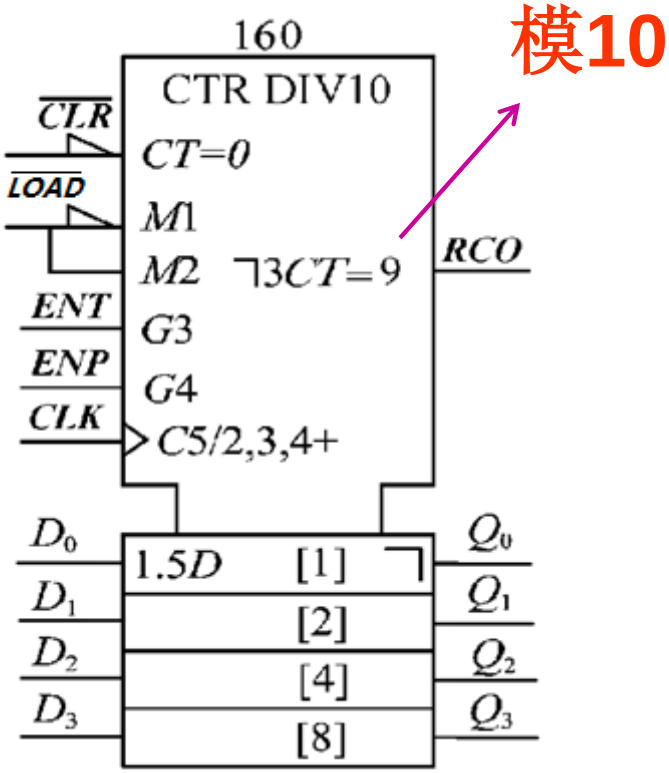
(8421BCD码同步加法计数器)

模10, 其它与74161相同. 异步清0

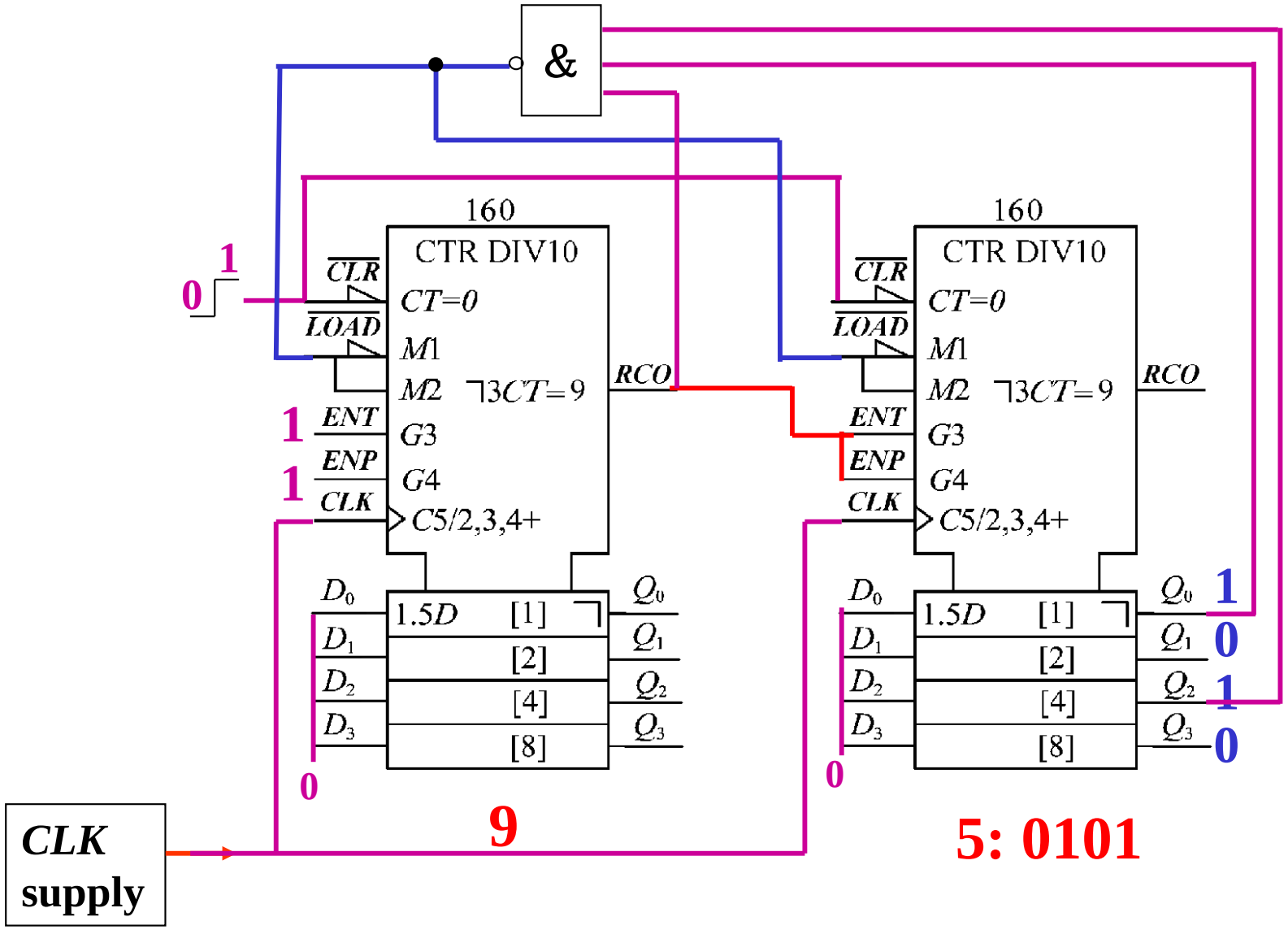
$$RCO = ENT \cdot Q_3 \cdot Q_0$$

当 $Q_3Q_2Q_1Q_0$ = 1001,

RCO = 1



例: 用74160 设计一个 60 s 计数器.

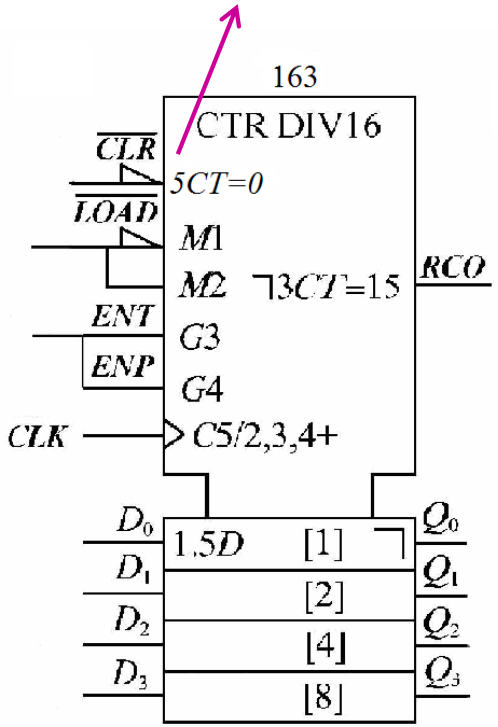


6.4.3 IC 计数器 74163 (M-16)

同步清0，其它与 74161相同（模16）

图中：5*CT*=0 在 5 端有效时清0

*CLK*有效边沿



74163 功能表

$\overline{CLR}$	$\overline{LD}$	ENT	ENP	CLK	$D_0\,D_1\,D_2\,D_3$	功能
0	X	X	X	↑	X X X X	Direct set 0
1	0	X	X	↑	$D_0\,D_1\,D_2\,D_3$	Load 预置
1	1	0	X	X	X X X X	保持 *RCO*=0
1	1	X	0	X	X X X X	保持
1	1	1	1	↑	X X X X	M-16 计数

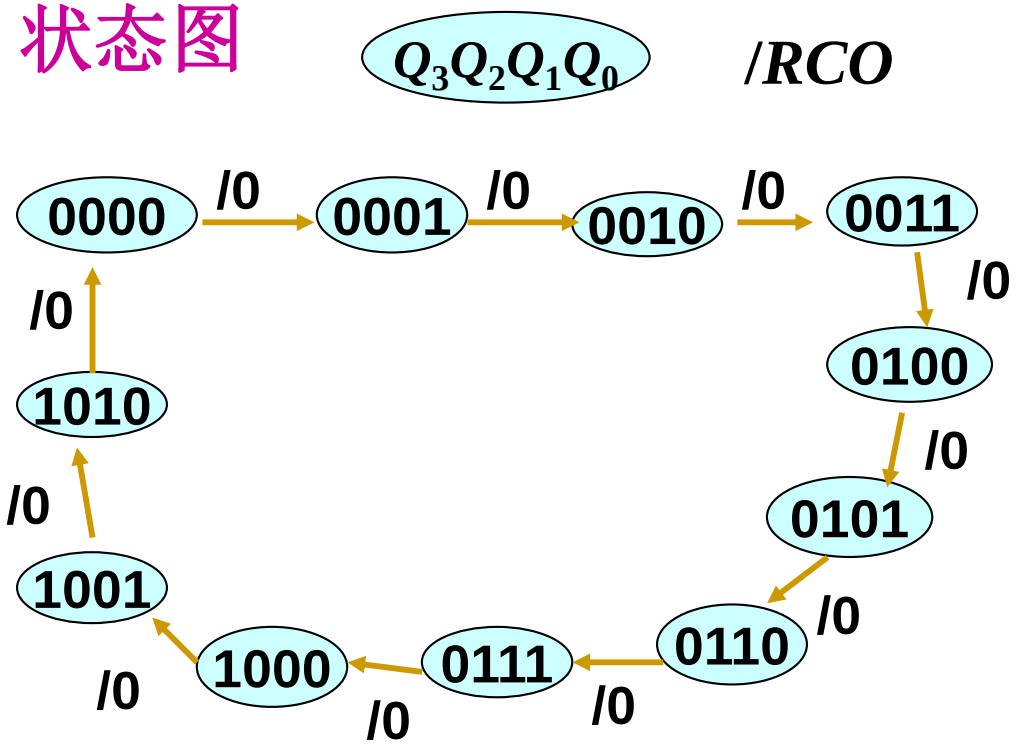
同步清零0: 当$\overline{CLR}$ =0 时，下一个 *CLK* 到达，

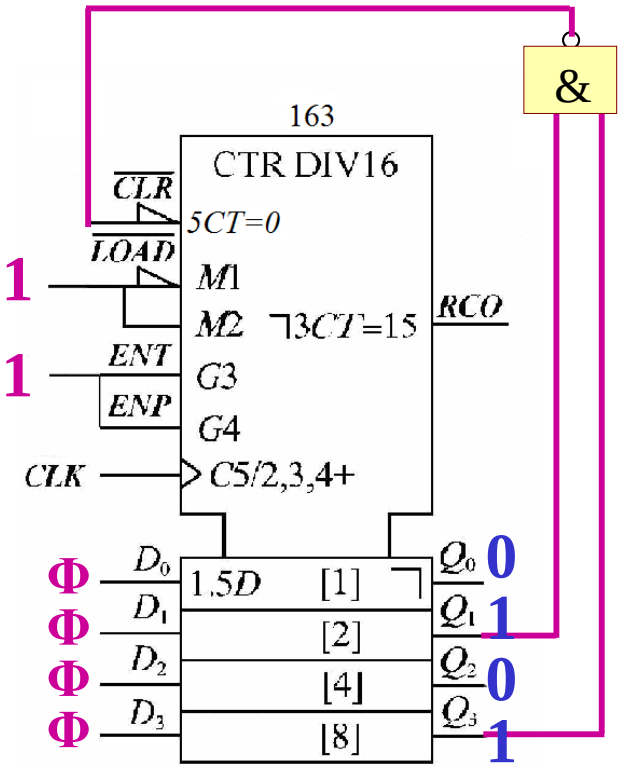
$Q_3Q_2Q_1Q_0$ = 0000

例：用74163的同步清零功能设计一个模11计数器.
($\overline{CLR}$)

最大状态 1010

状态图





没有毛刺

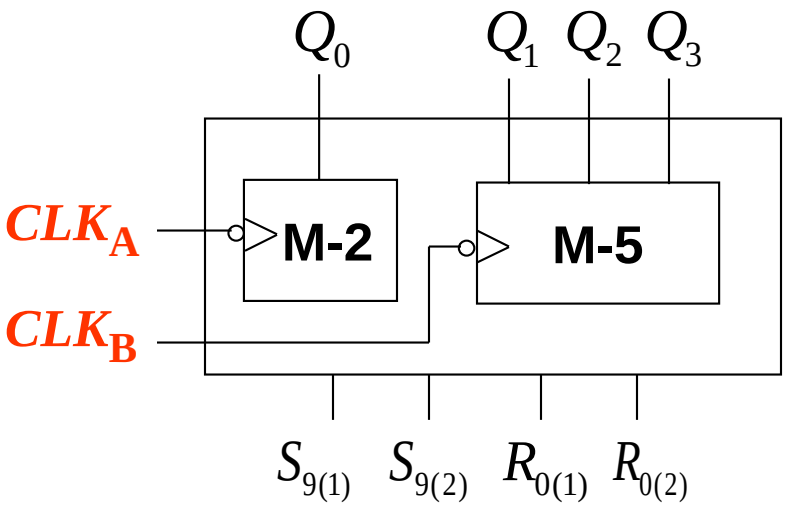
用 $\overline{LD}$ 端，与74161相同，初始为0000.

6.4.4 IC 计数器 74290

1. 74290 功能

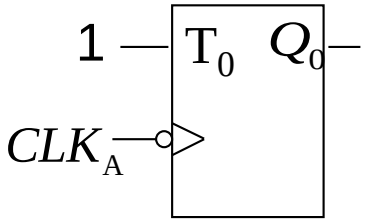
模 2-5-10 异步计数器

框图

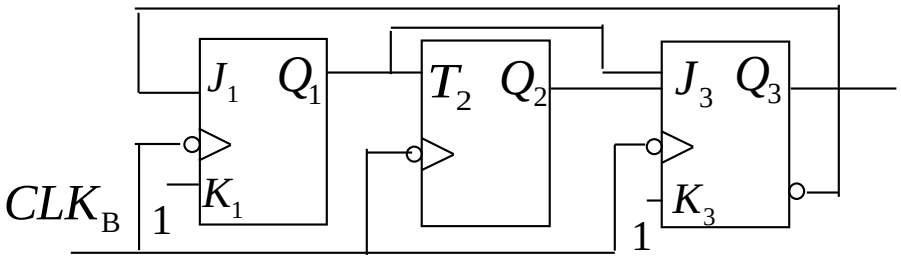


两个独立的下降沿FF

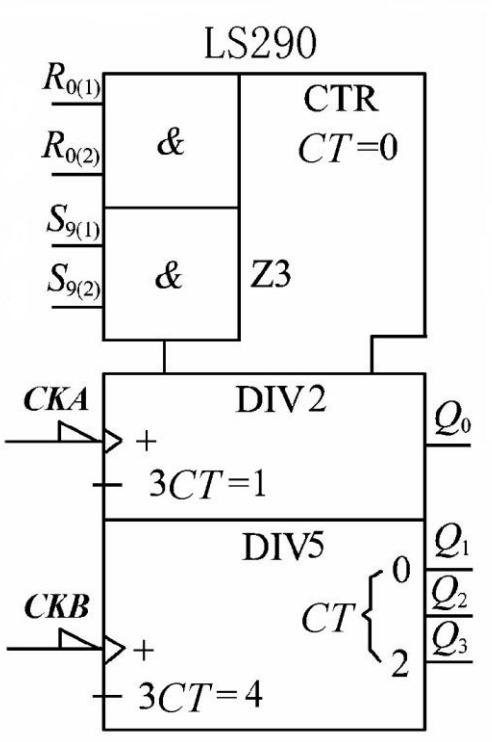
M-2 计数器，输出 Q_0



M-5 计数器，输出 $Q_3Q_2Q_1$



功能



(1) 异步清0

当 $\begin{cases} S_{9(1)} \cdot S_{9(2)} = 0 \ \text{(low)} \\ R_{0(1)} = R_{0(2)} = 1 \ \text{(high)} \end{cases}$

$Q_3Q_2Q_1Q_0 = 0000$

(2) 异步置9

当 $S_{9(1)}=S_{9(2)}=1$

$Q_3Q_2Q_1Q_0 = 1001$

(3) 计数

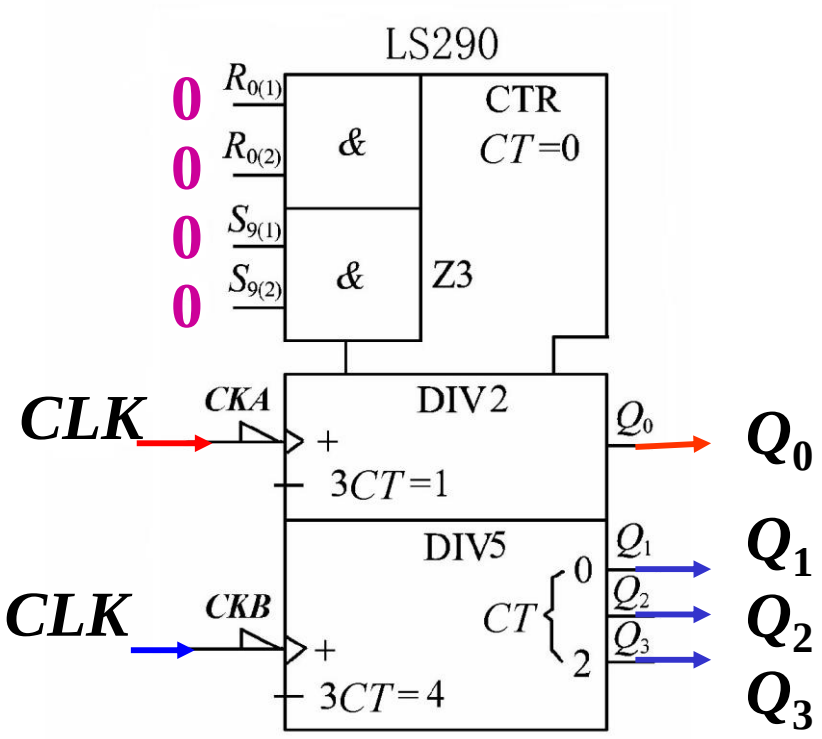
当 $\begin{cases} S_{9(1)} \cdot S_{9(2)} = 0 \\ R_{0(1)} \cdot R_{0(2)} = 0 \end{cases}$

同时满足，*CLK*下降沿实现计数

2. 74290应用

(1) 模 2 计数器

$$\begin{cases} S_{9(1)} \cdot S_{9(2)} = 0 \\ R_{0(1)} \cdot R_{0(2)} = 0 \end{cases}$$



CLK 从 CLK_A 接入, Q_0 输出, 实现 模 2加计数

(2) 模 5 计数器

$$\begin{cases} S_{9(1)} \cdot S_{9(2)} = 0 \\ R_{0(1)} \cdot R_{0(2)} = 0 \end{cases}$$

CLK 从 CLK_B 接入, $Q_3Q_2Q_1$输出, 实现 模 5加计数

两种用法完全独立。构成更大模数时， 需外接线连接

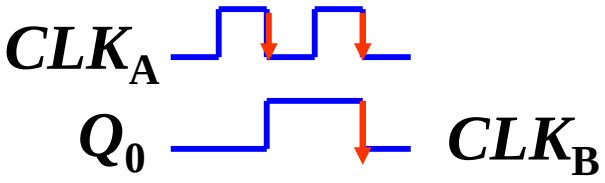
(3) 8421BCD 码模10 计数器

$S_{9(1)} \cdot S_{9(2)} = 0$，　$R_{0(1)} \cdot R_{0(2)} = 0$

CLK 接 CLK_A，

$Q_0 \longrightarrow CLK_B$

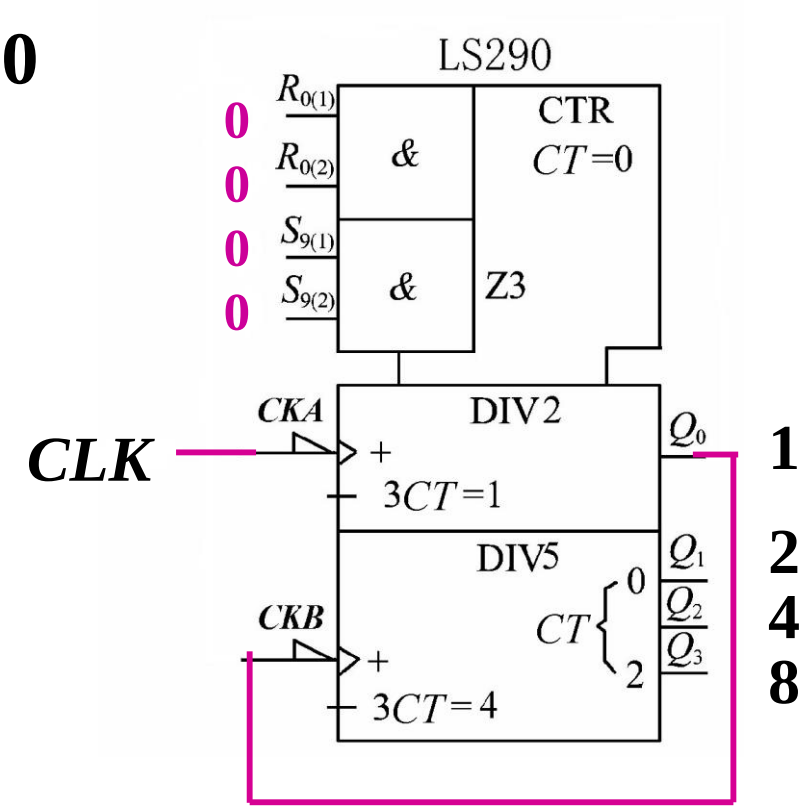
在 Q_0 下降沿(CLK_B 1 → 0), M-5 计数.

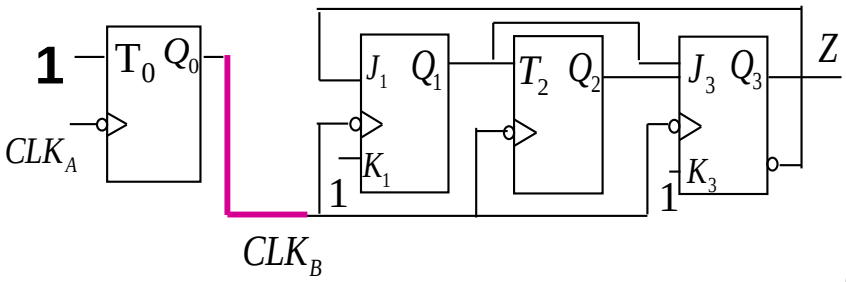


触发 M-5 计数

输出位权

$Q_3Q_2Q_1Q_0$: 8 4 2 1





(4) 8421 BCD码任意进制计数器

“直接置 0 R_0 ”高电平清 0

例：M-7 计数器

① $CLK \rightarrow CLK_A$

② 接: 8421 BCD 模10

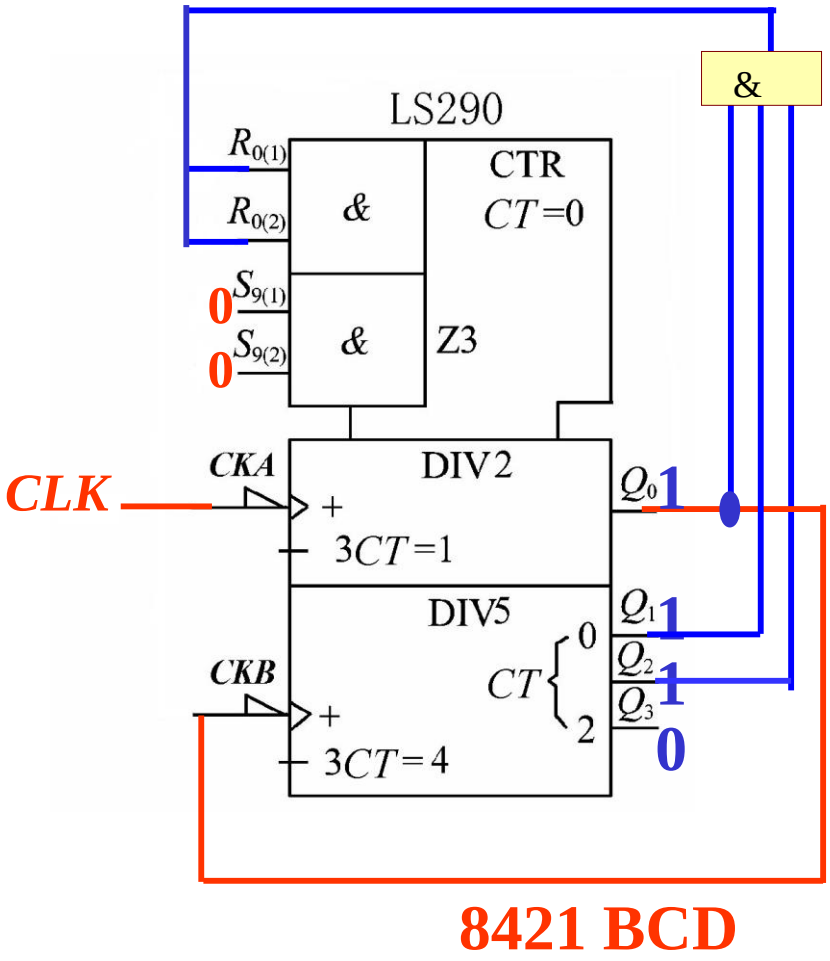
$Q_0 \rightarrow CLK_B$

③ $S_{9(1)} = S_{9(2)} = 0$

④ 输出 $Q_3Q_2Q_1Q_0 = 0111$

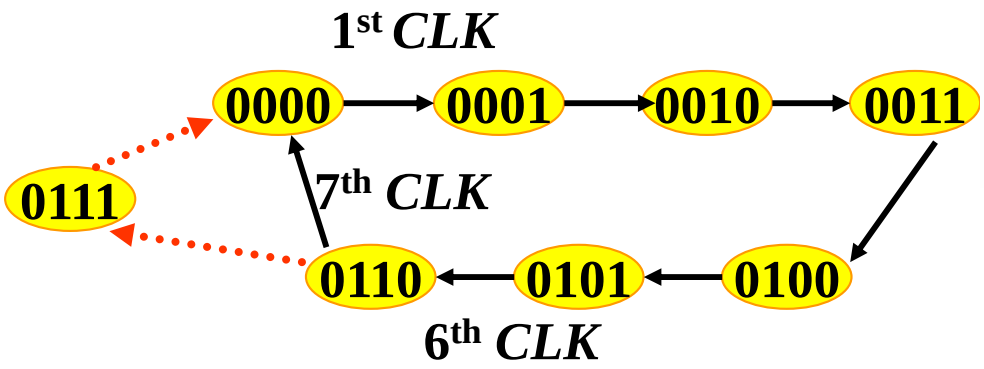
→ 与门

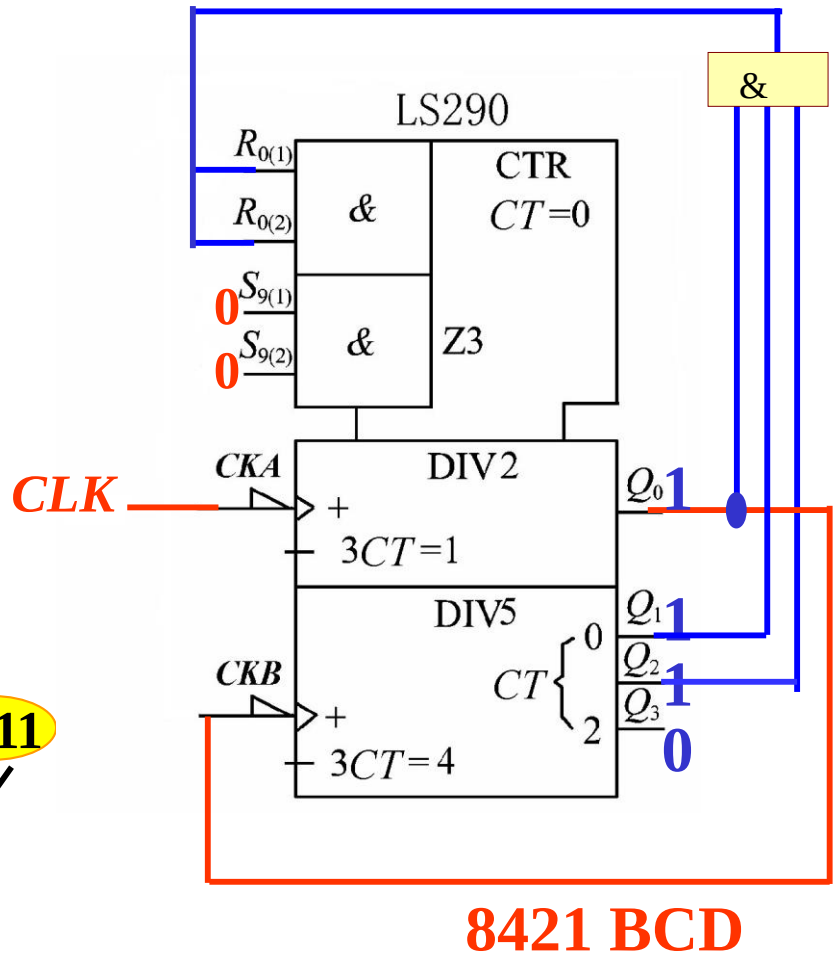
⑤ 与门 → R_0 (直接清0)



当$Q_3Q_2Q_1Q_0$ = 0111时，立即清0，0111只是一闪，出现 毛刺

主循环7个状态：
0000 ~ 0110.





不稳定状态用虚线连接

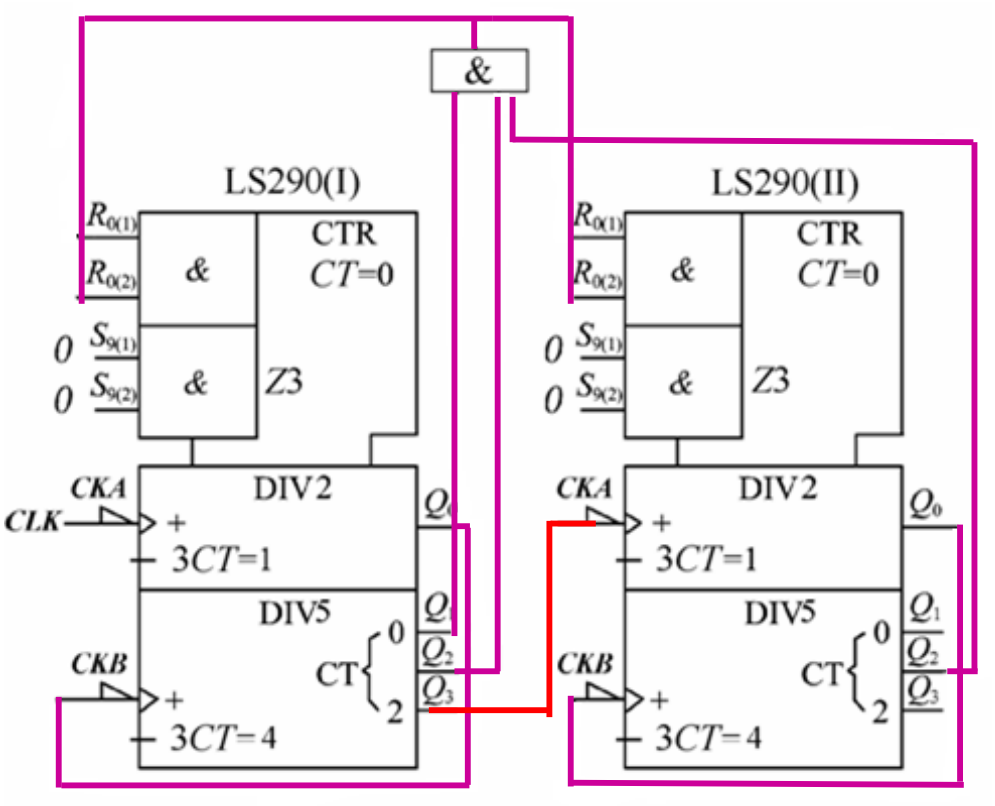
(5) 8421 BCD 级联计数器

当计数模值>10　　74290 级联

例: 用74290 设计一个 8421BCD 码模 46 计数器.

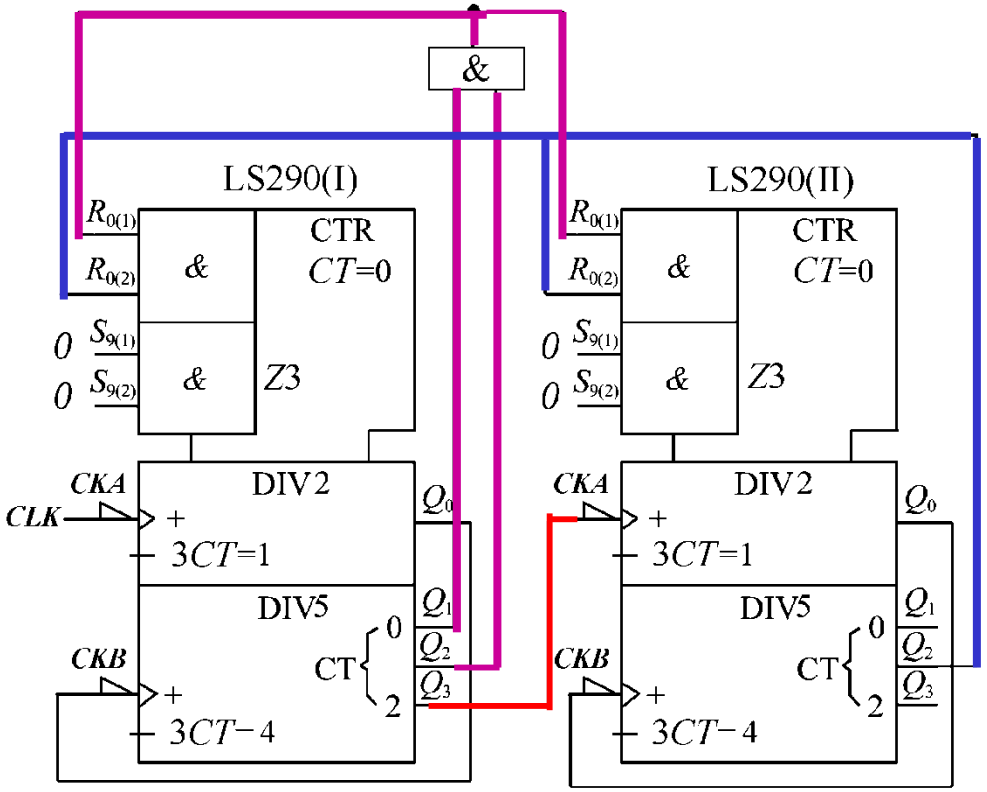
8421 十进制

进位



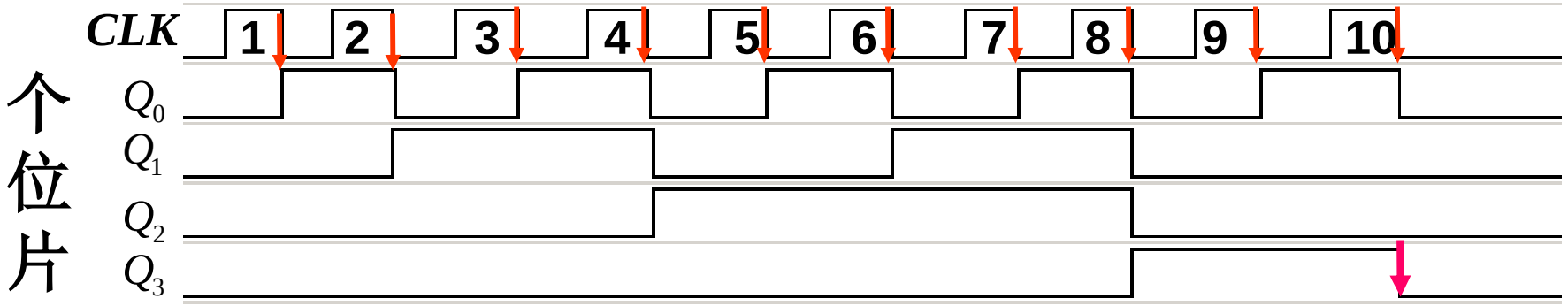
个位：6 (0110)　　十位：4 (0100)

电路连接方式也可以



注意：进位

波形：



利用Q_3第10个*CLK*下降沿触发十位片的CLK_A　(不用连Q_0Q_3)

§6.5 寄存器 Registers

寄存器用于寄存一组二进制代码。主要由触发器构成。

一个触发器能够存储 1 位二进制代码，所以用 *n* 个触发器组成的寄存器可以存储一组 *n* 位二进制信息。

寄存器广泛地应用于各类数字系统和数字计算机中。移位型寄存器在数字通信中的应用极其广泛。如在计算机串行数据通信中，需要发送的信息总是先放在发送端的移位寄存器中，然后由移位寄存器将其逐位移出。接收端的寄存器逐位从线路上接收信息，收完一个完整的数据后才从移位寄存器中取走数据。

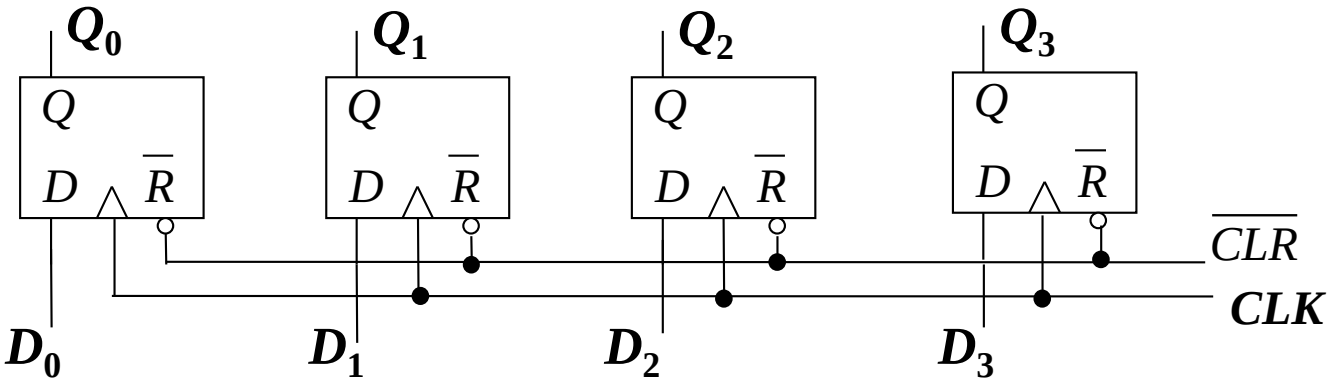
6.5.1 寄存器分类

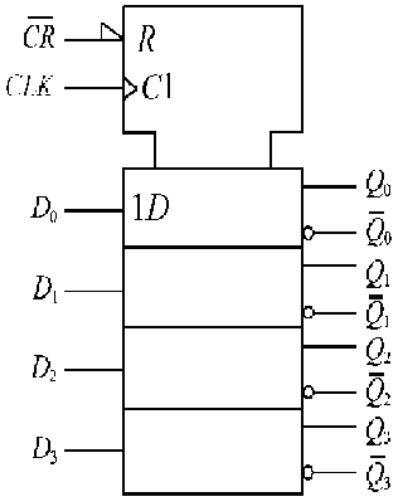
Classifications of Registers

1. 并入/并出型寄存器

例如，4个 D-FFs 构成寄存器

74LS175



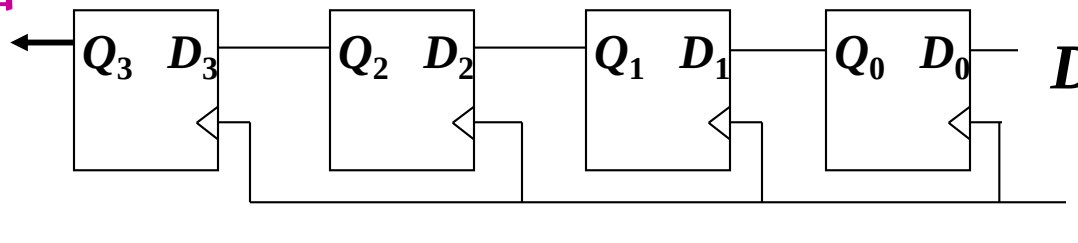


在*CLK* 正边沿, 4 个数据并行输入，状态

$Q_3Q_2Q_1Q_0 = D_3D_2D_1D_0$ 并行输出

2．左移串入/串出型寄存器

数据串出



数据串入

shift left

一个*CLK* 到来, 左移一位.

例：

初始 $Q_3Q_2Q_1Q_0$ =1001

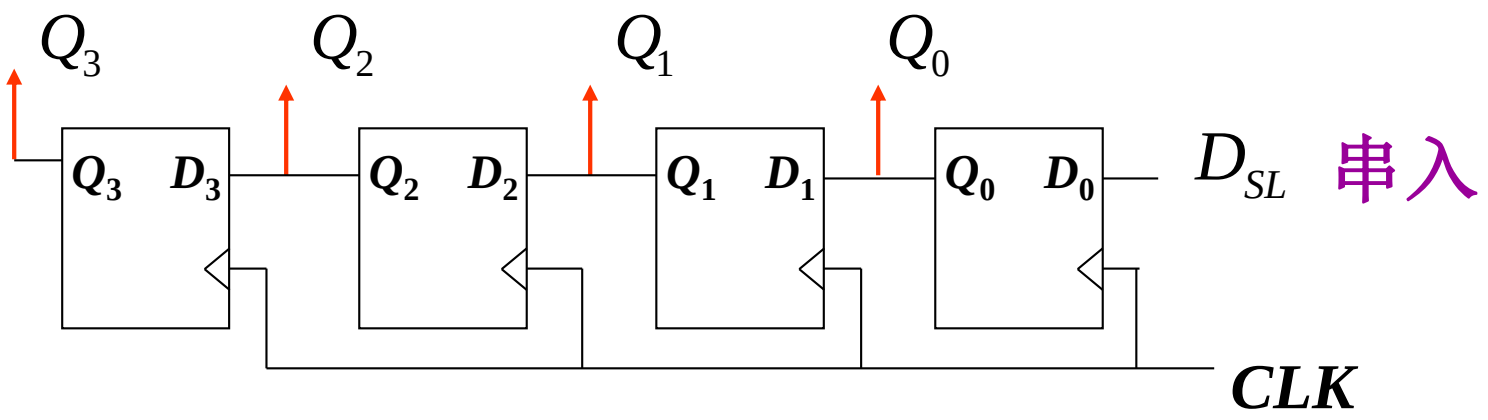
串入: 1011 (D_{SL}),

CLK	串出	$Q_3Q_2Q_1Q_0$ 串入
	1	1 0 0 1 1 0 1 1
1	0	0 0 1 1
2	0	0 1 1 0
3	1	1 1 0 1
4	1	1 0 1 1

4 个*CLK* 后, $Q_3Q_2Q_1Q_0$ =1011

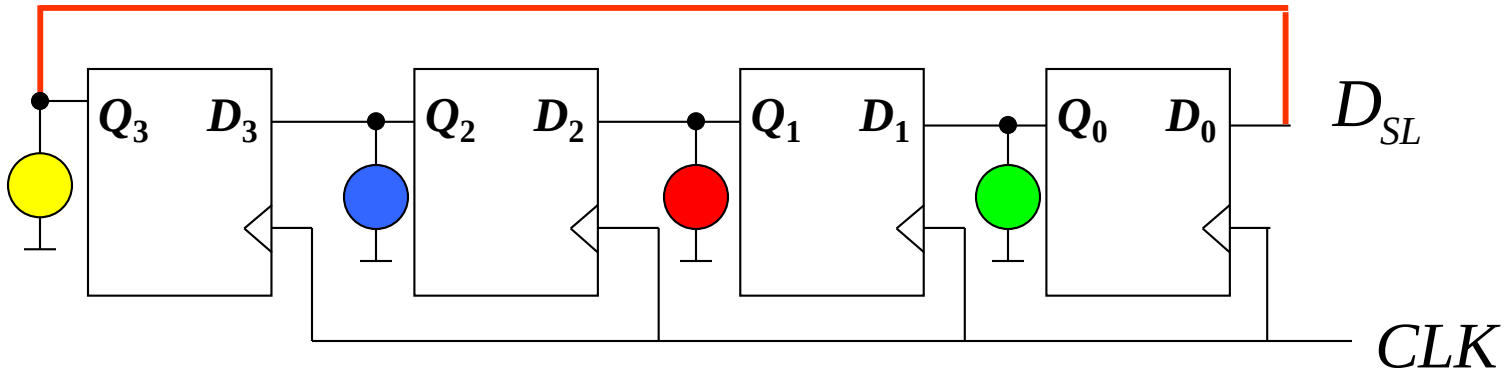
3. 左移串入/并出型寄存器

并行输出



4. 左移环型寄存器

串出端与串入端相连



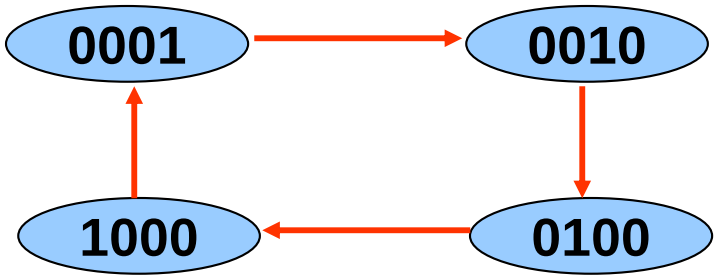
各FF 输出接彩灯

当输出为 0001时，接高电平的灯亮

灯亮时间：

取四位中只有一个1 的状态为主循环

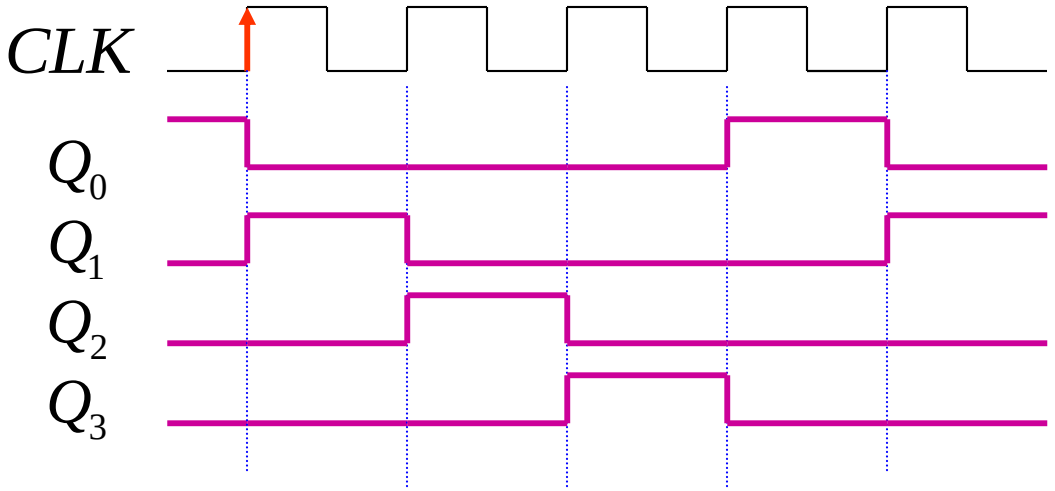
状态图



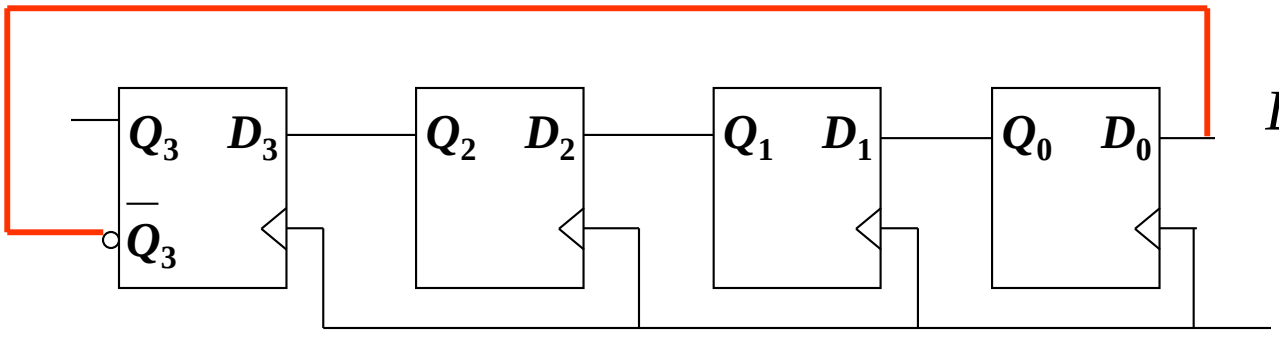
环形计数器

注意：***n* FFs → *n* 个状态 → 模 *n***

波形图

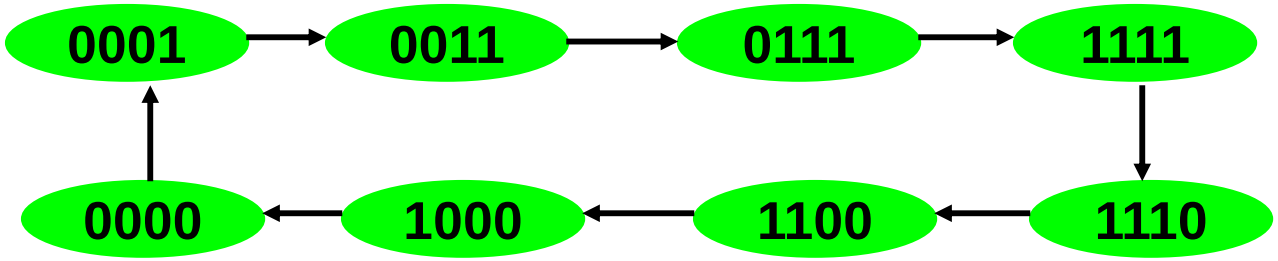


5. 左移扭环寄存器



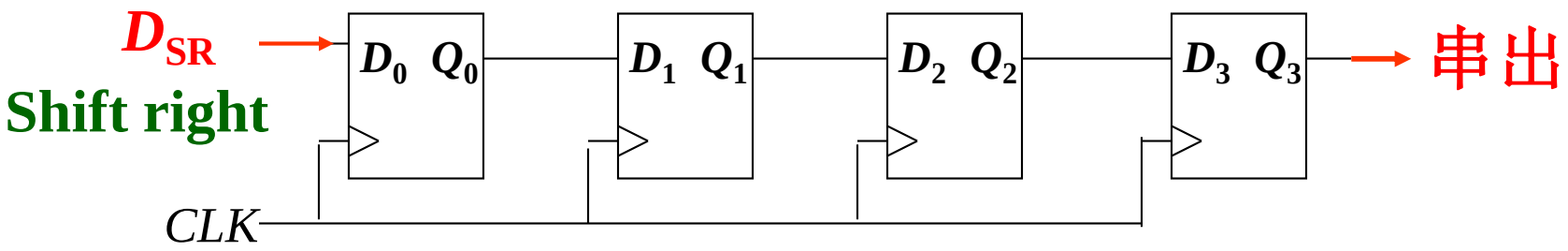
D_{SL} $\overline{Q}_3 \rightarrow D_{SL}$

初始 $Q_3Q_2Q_1Q_0$ =0001 状态图：$Q_3Q_2Q_1Q_0$

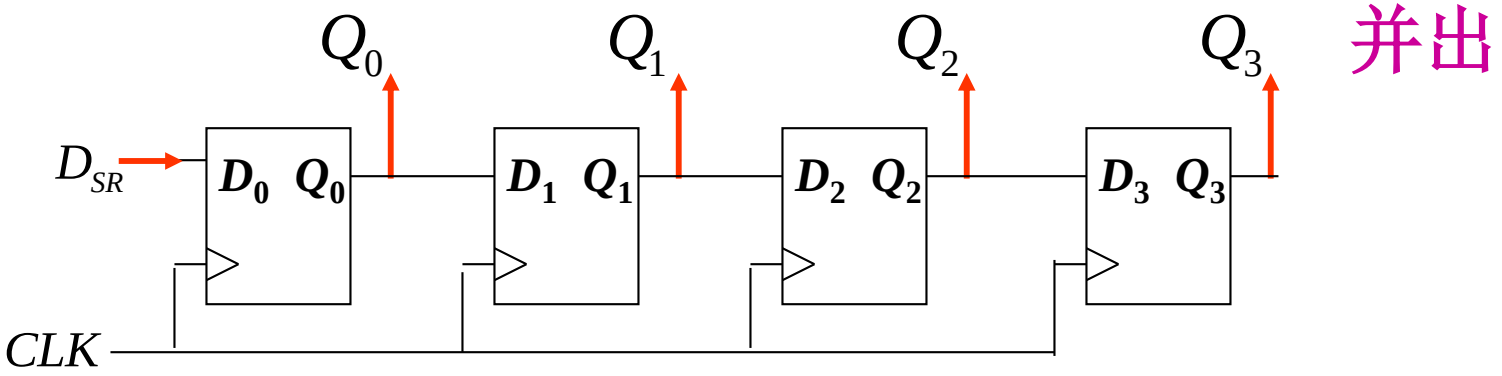


扭环计数器 n FF → 模 $2n$

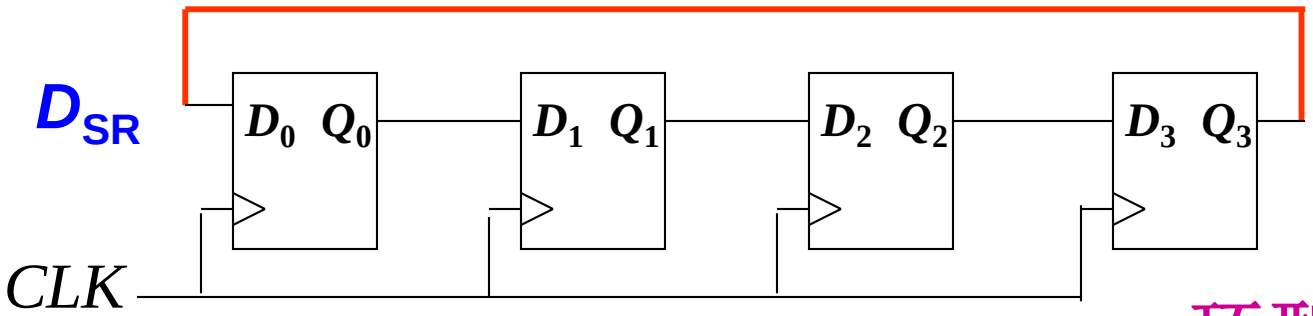
6. 右移串入/串出寄存器



7. 右移串入 /并出寄存器

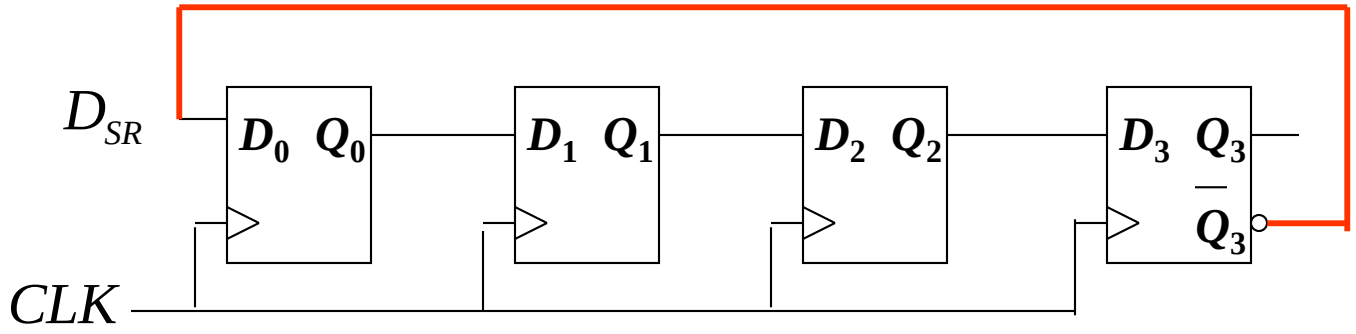


8. 右移环型寄存器



环型计数器

9. 右移扭环寄存器

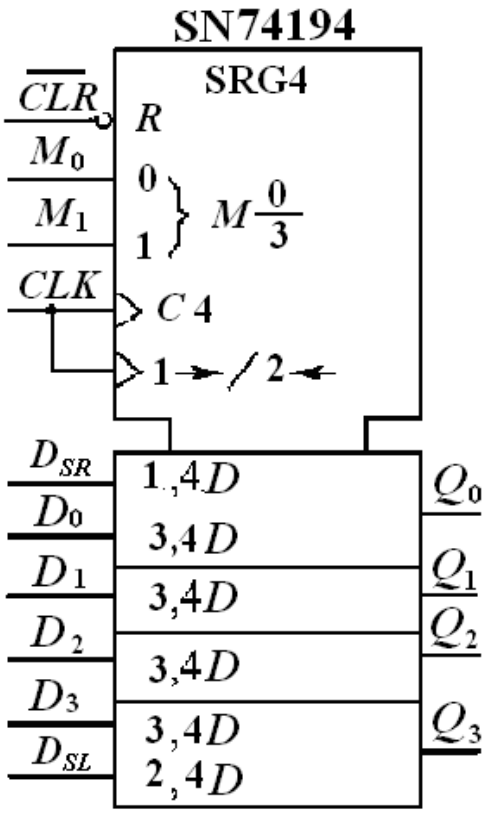


扭环计数器

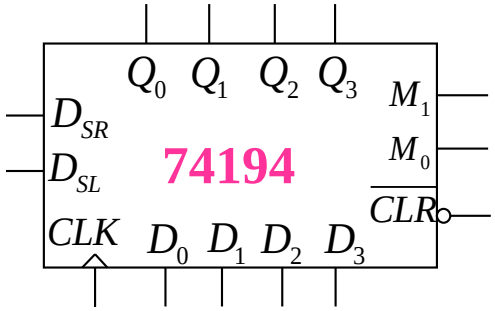
6.5.3 集成寄存器 74194　IC Register 74194

多功能寄存器：四位并行存取双向移位寄存器

电路 P. 139　符号



IEEE



D_{SR}在Q_0一侧，D_{SL}在Q_3一侧

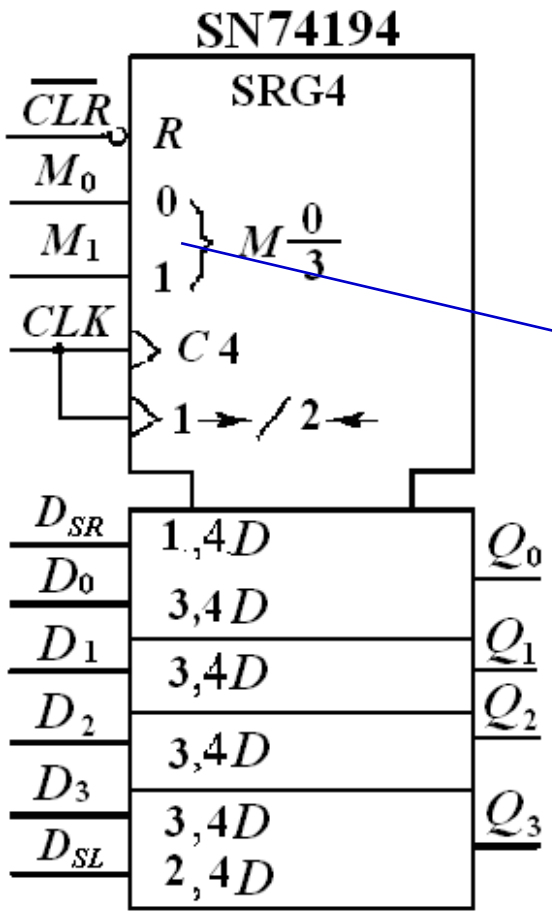
$Q_3Q_2Q_1Q_0$ 数据输出

$D_3D_2D_1D_0$ 数据输入

D_{SR} D_{SL} 串入

1→ shift right

2← shift left



$\overline{CLR}$ = 0, 异步清0

CLK 正边沿触发

M_1 M_0 控制 (模式)，M_1 高位

M_1 M_0 组成4种模式

74194 功能

M_1 M_0	功 能
0 0	保持
0 1	右移
1 0	左移
1 1	并入

Q_0 Q_1 Q_2 Q_3

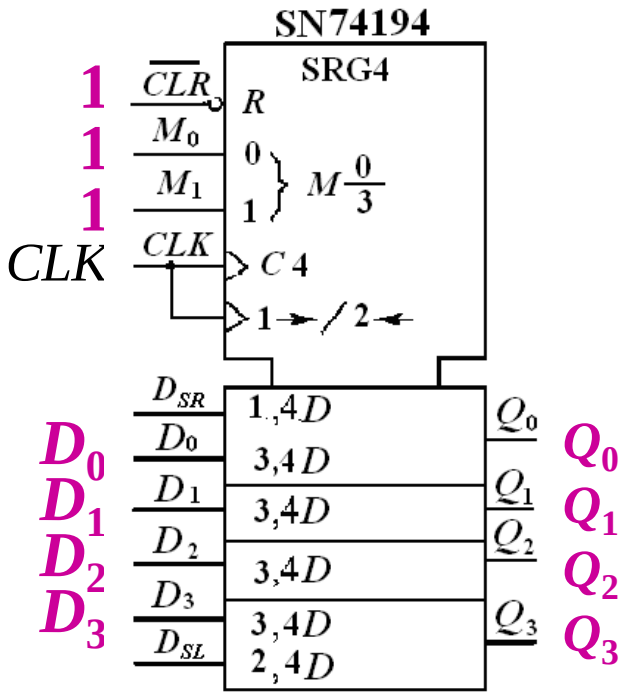
↑ ↑ ↑ ↑

D_0 D_1 D_2 D_3

实现前面 9 种功能

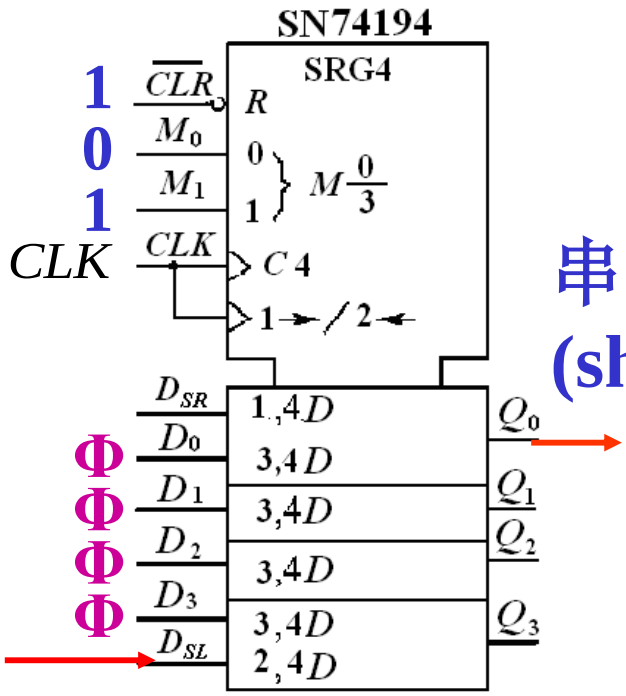
注：$Q_0Q_1Q_2Q_3$ 只有排列顺序，没有高、低位。

(1) 并入/并出



并入　　并出

(2) 左移串入/串出

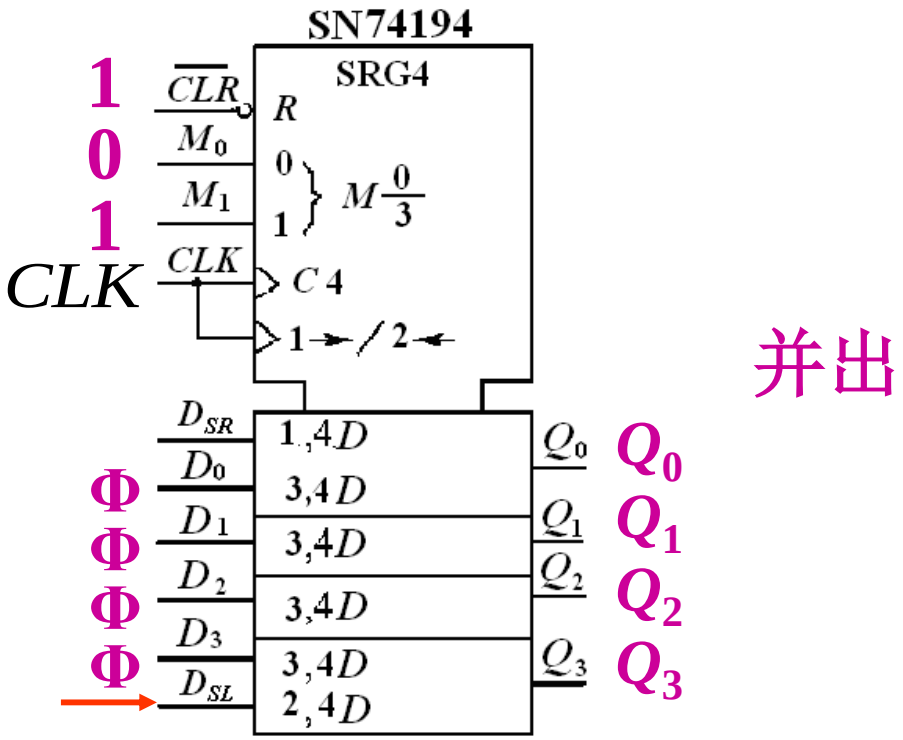


串出
(shift left)

串入
shift left

经过4个触发器

(3) 左移串入 / 并出


SN74194
SRG4
1
0
1
CLK
CLR
M0
M1
CLK
R
0
1
M 0/3
C 4
1→/2←
DSR
D0
D1
D2
D3
DSL
1,4D
3,4D
3,4D
3,4D
3,4D
2,4D
Q0
Q1
Q2
Q3
Φ
Φ
Φ
Φ
Q0
Q1
Q2
Q3
并出
串入
shift left

(4) 左移环形

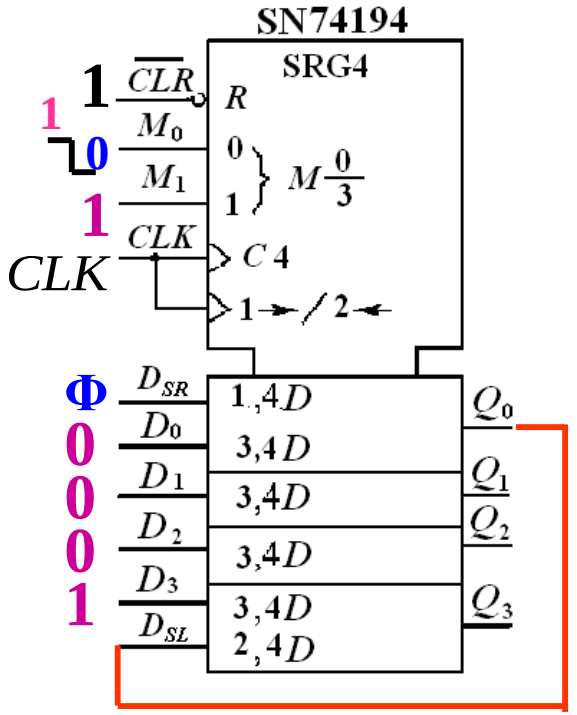
$Q_0 \rightarrow D_{SL}$

先置 M_1=1, M_0=1, 在 *CLK* 上升沿并入,

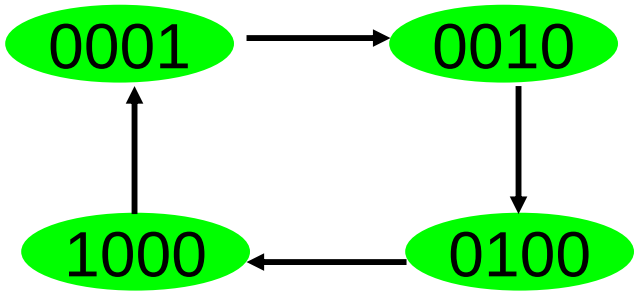
$Q_0Q_1Q_2Q_3$ =

$D_0D_1D_2D_3$ =0001

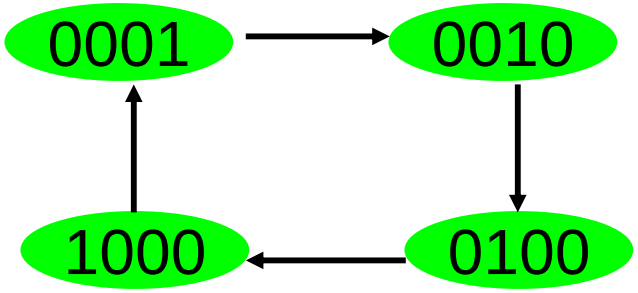
再置 M_0 =0, *CLK* 边沿到来 → 左移 → M-4 计数



一个1为主循环 $Q_0Q_1Q_2Q_3$



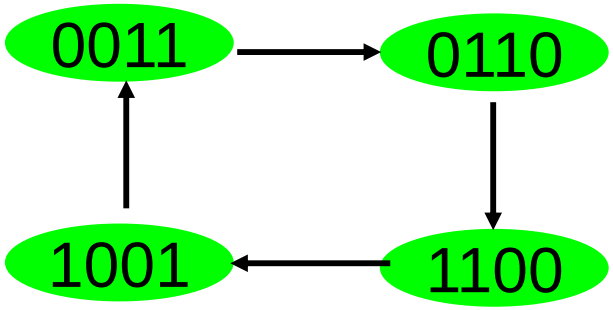
一个1为主循环 $Q_0Q_1Q_2Q_3$ 左移环形的其他置数方式：



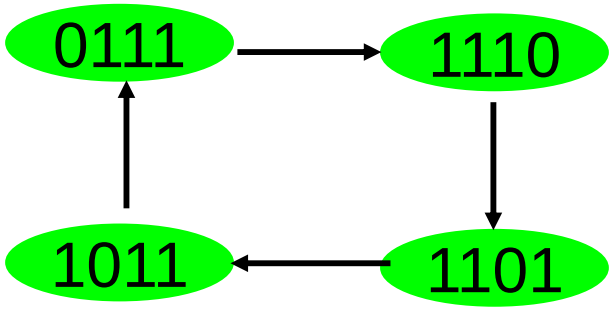
0000

1111

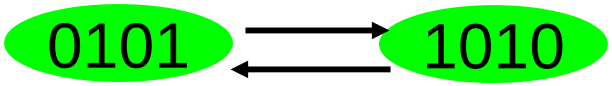
保持



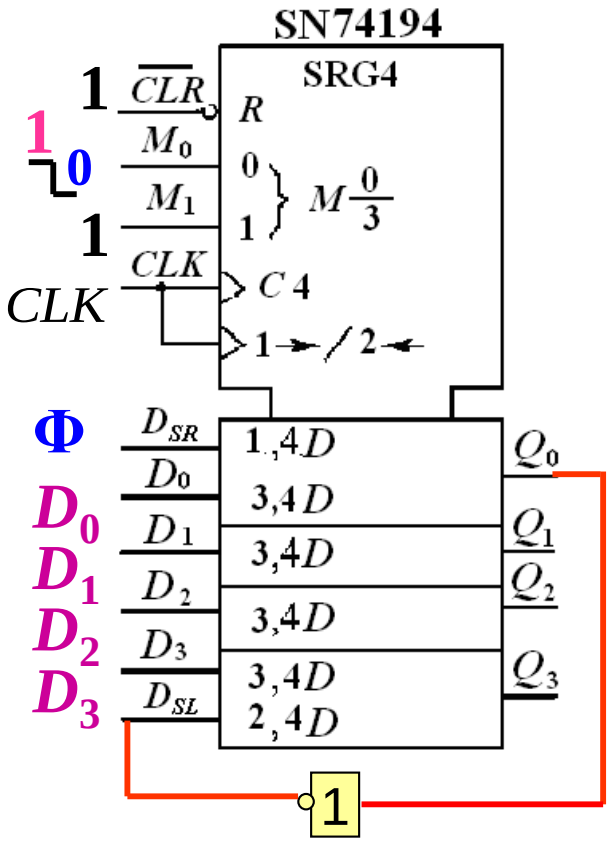
M-4环形计数器



M-4环形计数器



(5) 左移扭环寄存器



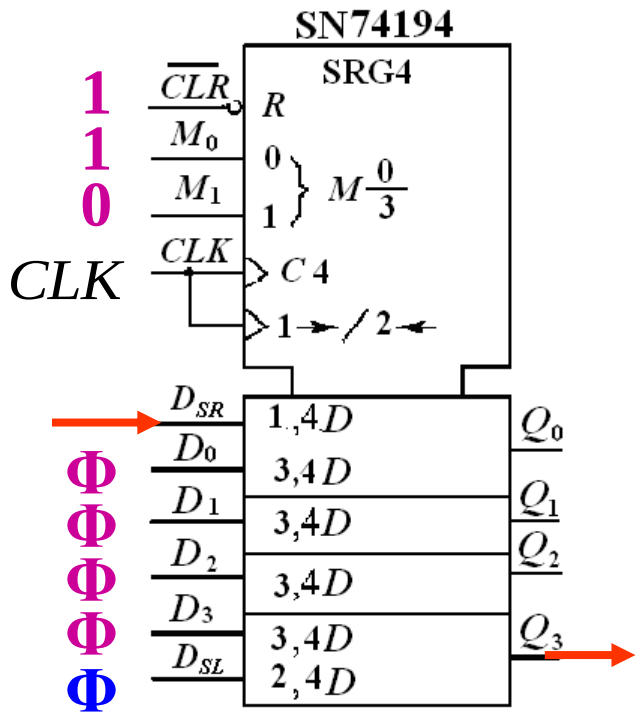
M_1= 1,

$$M_0=\begin{cases}1, \text{并入} \\ \quad Q_0Q_1Q_2Q_3 = D_0D_1D_2D_3 \\ 0, \text{扭环}\end{cases}$$

$\overline{Q}_0$ connect to D_{SL}

$D_0D_1D_2D_3$ 接Φ，都可以构成扭环

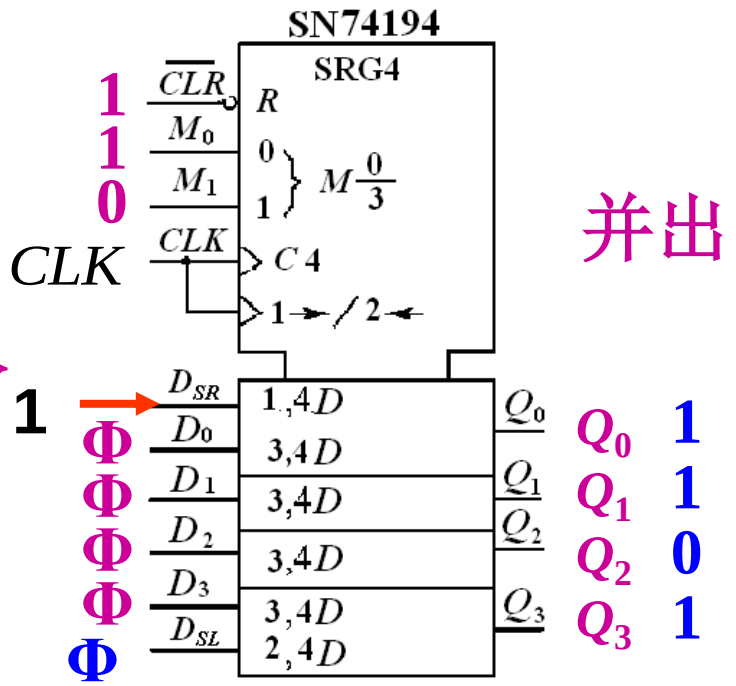
(6) 右移串入/串出寄存器



串入
shift right

串出
shift right

(7) 右移串入/并出寄存器



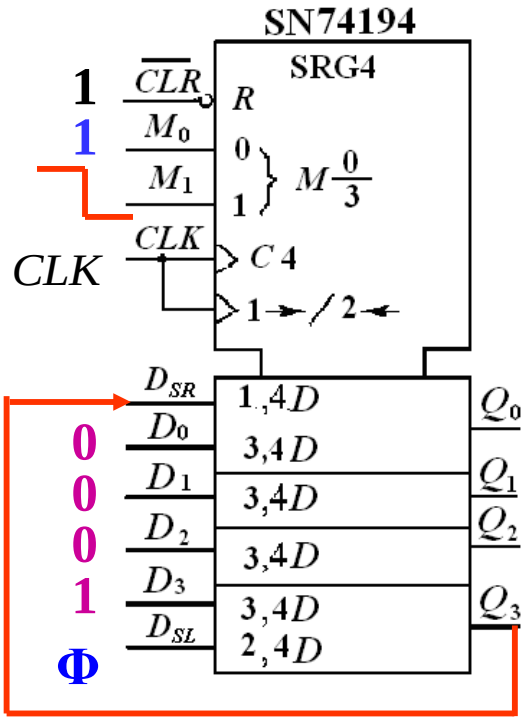
串入
1 1 0 1

并出

Q_0 1
Q_1 1
Q_2 0
Q_3 1

4个 *CLK* 后

(8) 右移环形寄存器



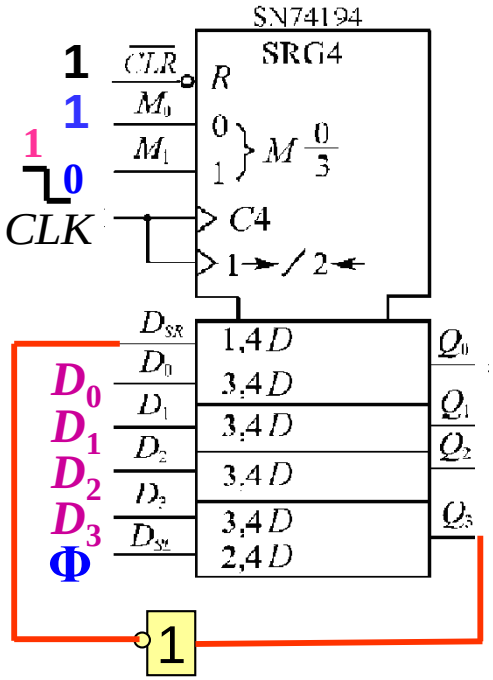
$Q_3 \rightarrow D_{SR}$

$M_0 = 1$

$$M_1 = \begin{cases} 1, CLK\text{ 到} \\ \quad Q_0Q_1Q_2Q_3 = D_0D_1D_2D_3 \\ 0, CLK\text{ 到} \\ \quad \text{右移环形} \end{cases}$$

模 4 计数器

(9) 右移扭环寄存器



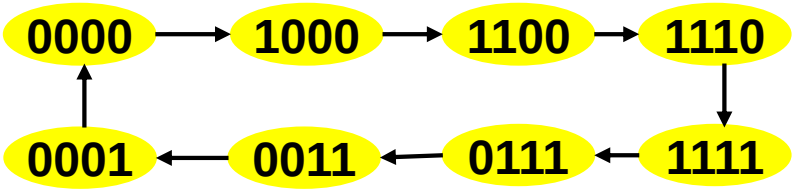
$\overline{Q}_3$ 接 D_{SR}

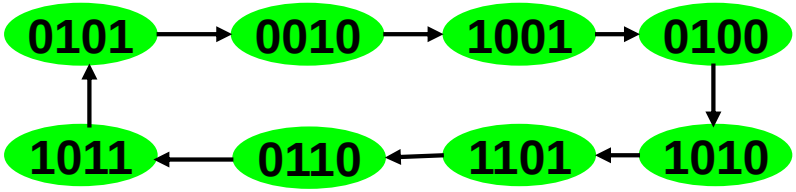
M_0= 1,

$$M_1=\begin{cases}1, \text{并入}\\ Q_0Q_1Q_2Q_3 = D_0D_1D_2D_3\\ 0, \text{扭环}\end{cases}$$

$D_0D_1D_2D_3$ 接Φ，都可以构成扭环

只有两种状态图 $Q_0Q_1Q_2Q_3$



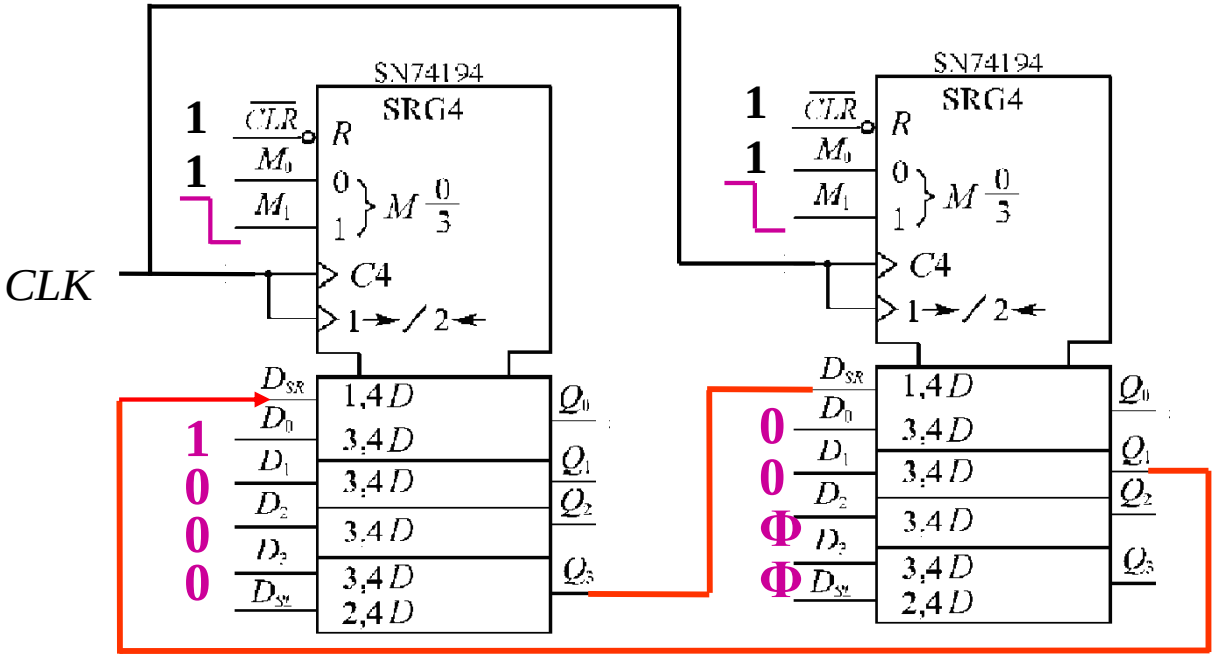


注意：从并入的$D_0D_1D_2D_3$开始循环　模 8 计数器

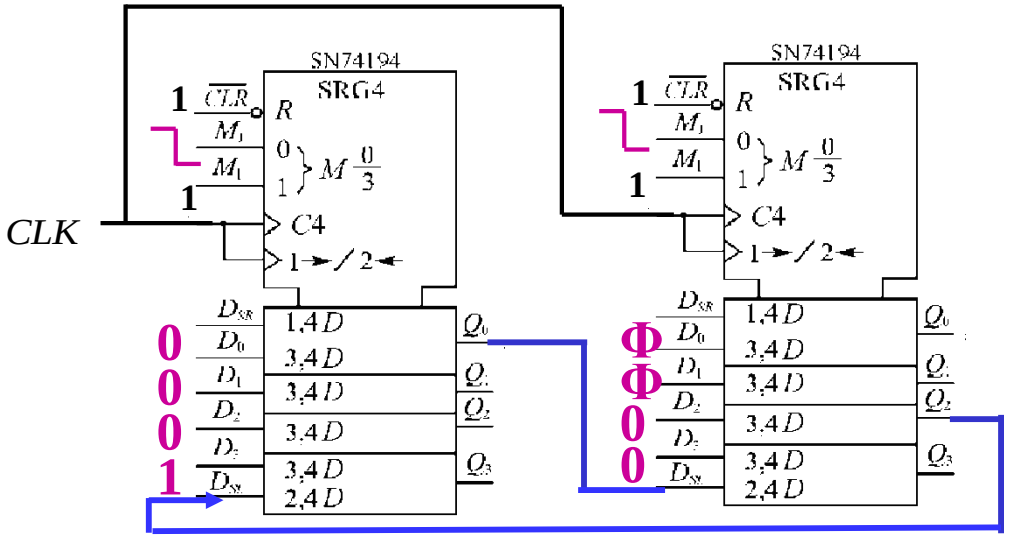
例1. 用74194 设计模 6 环形计数器

6 FFs

右移

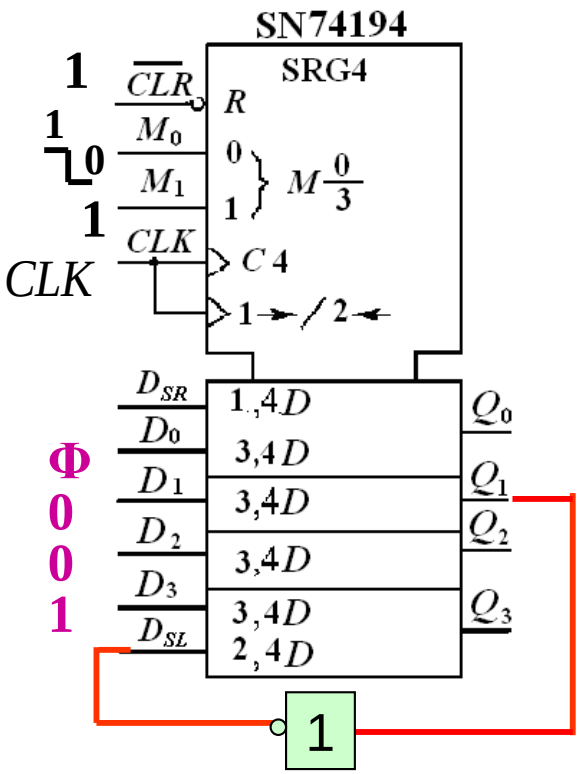


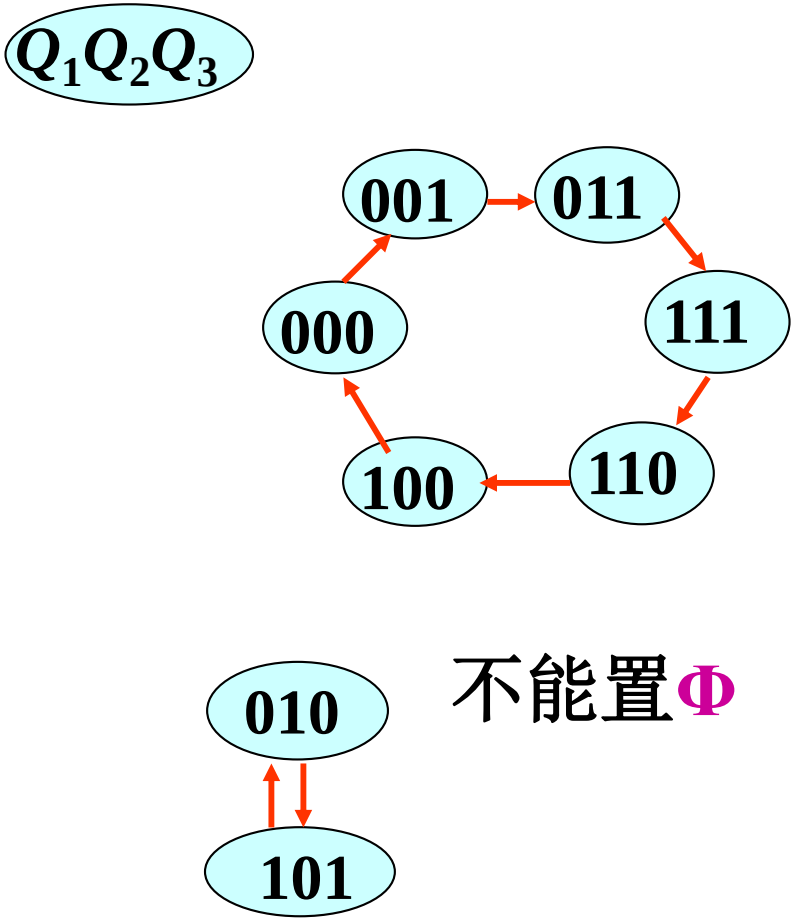
左移



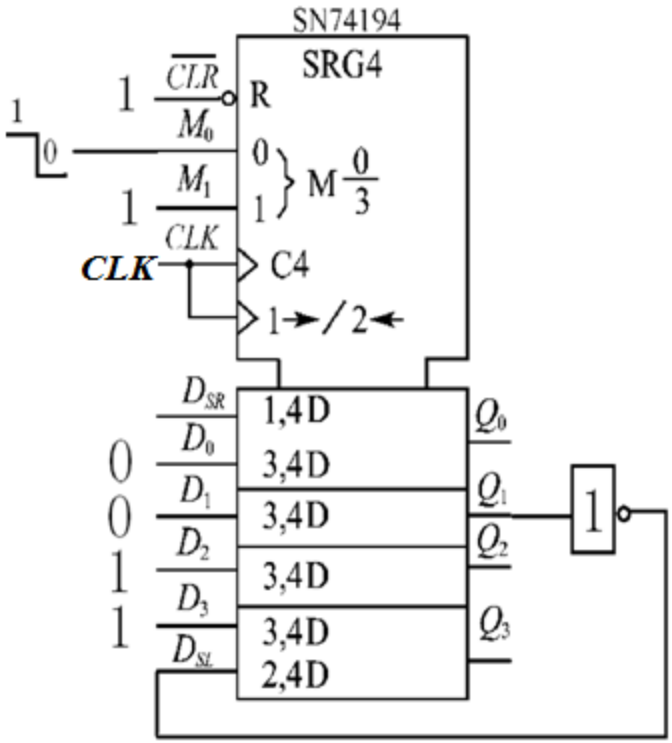
例2. 用74194设计模6 扭环计数器，画出状态图

3 FFs **Shift left**

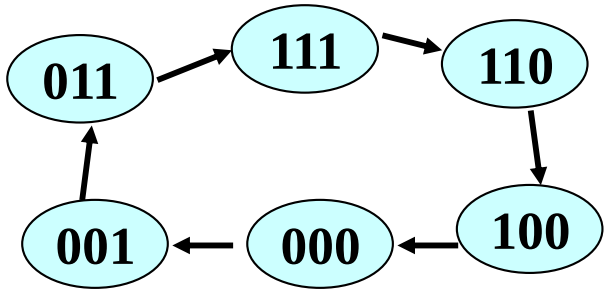




例3：分析如图所示的芯片功能，画出状态图。

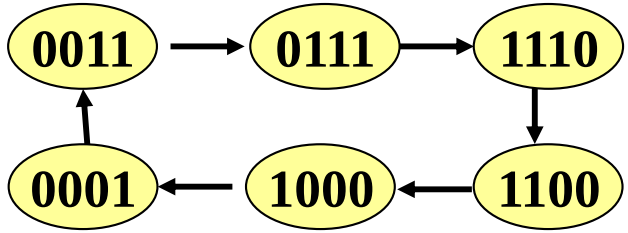


$Q_1Q_2Q_3$ 左移扭环



M - 6

$Q_0Q_1Q_2Q_3$



§6.6 序列信号发生器

Series Signal Generator

计数器和寄存器的应用

序列信号: 一组特定的循环数字信号

序列信号发生器:

- Counter-type 计数型
- Shift-type 移位型

6.6.1 计数型序列信号发生器

Counter-type Series Signal Generator

例：

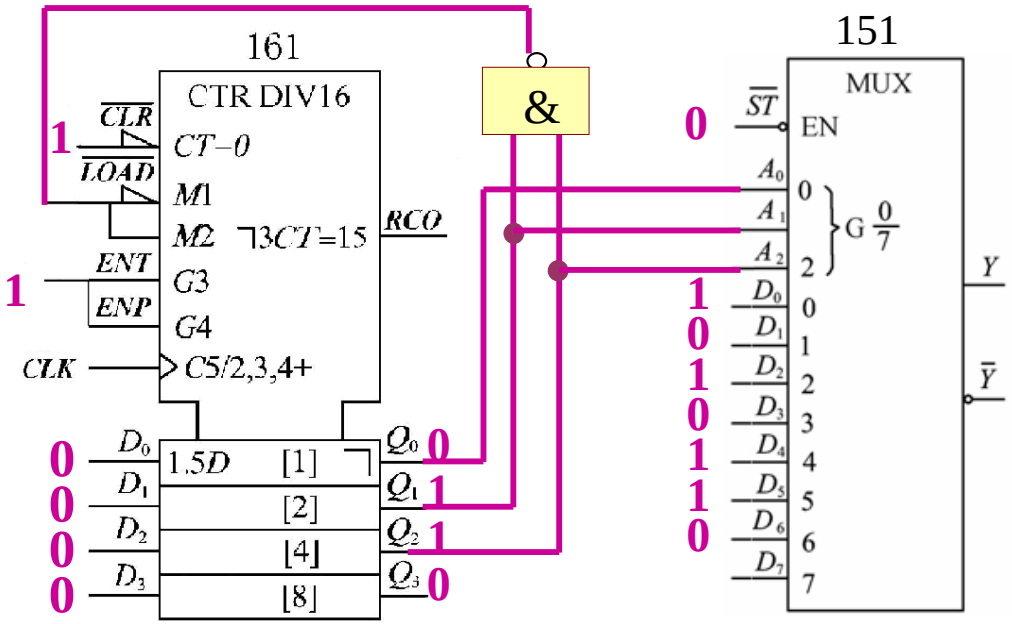
设计一个产生7位序列信号 1010110 的序列信号发生器（时间顺序: 从左到右）.

结构：

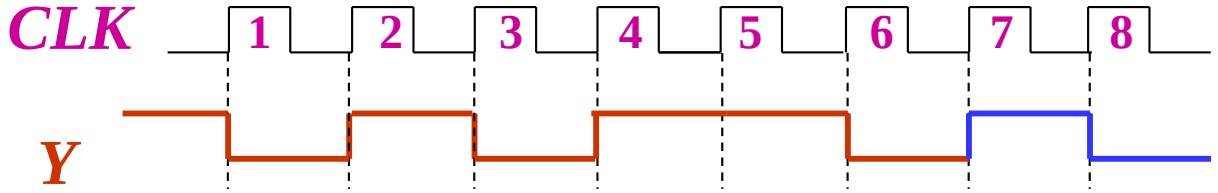
M-7 计数器 → 7 位 → 74161

8-1 MUX → 选择 1010110 → 74151

(M-7)

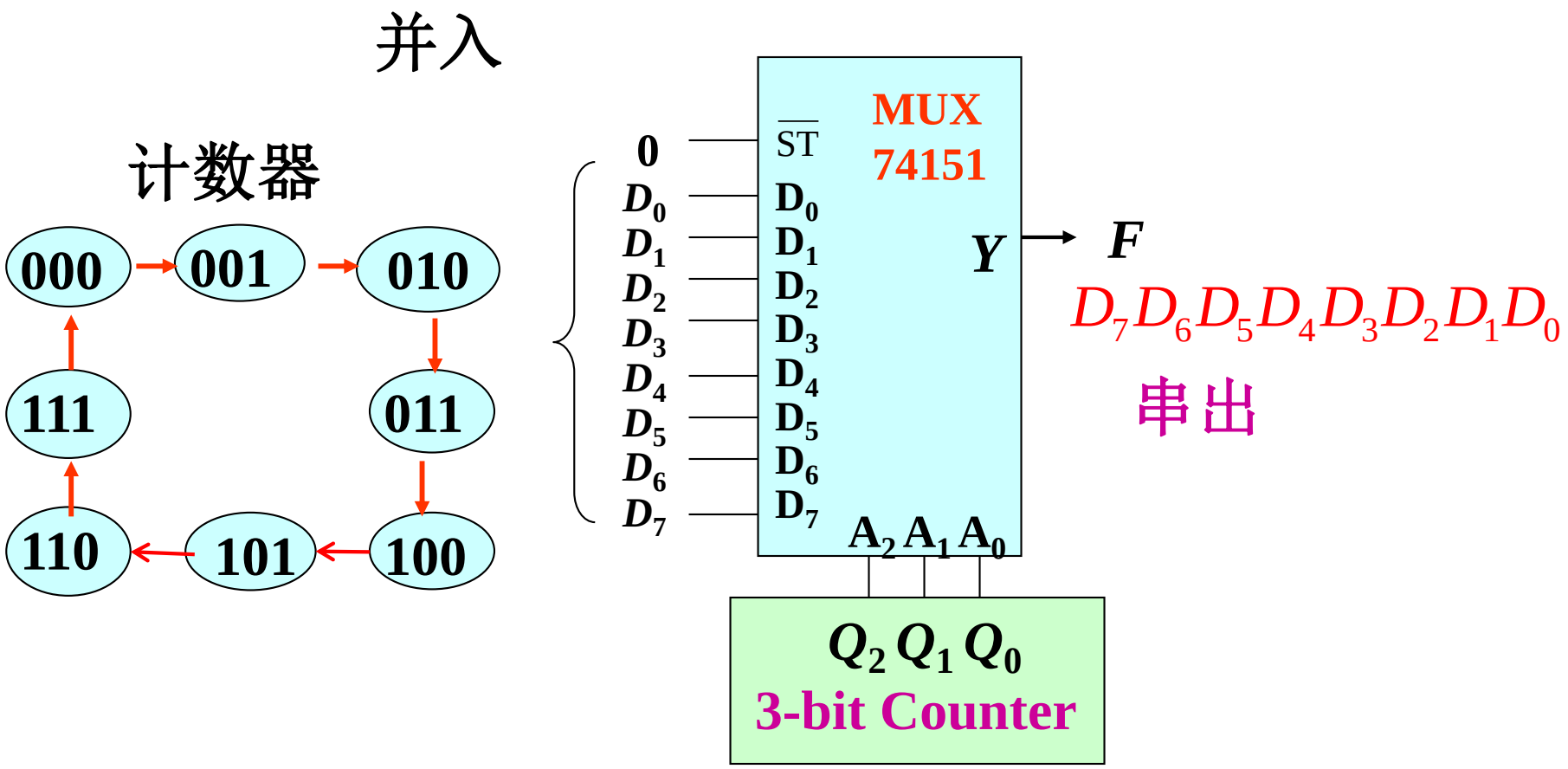

161
CTR DIV16
CLR
CT=0
LOAD
M1
M2
3CT=15
RCO
ENT
G3
ENP
G4
CLK
C5/2,3,4+
1.5D
[1]
[2]
[4]
[8]
&
151
MUX
ST
EN
G 0/7
Y
0110101 = Y

波形

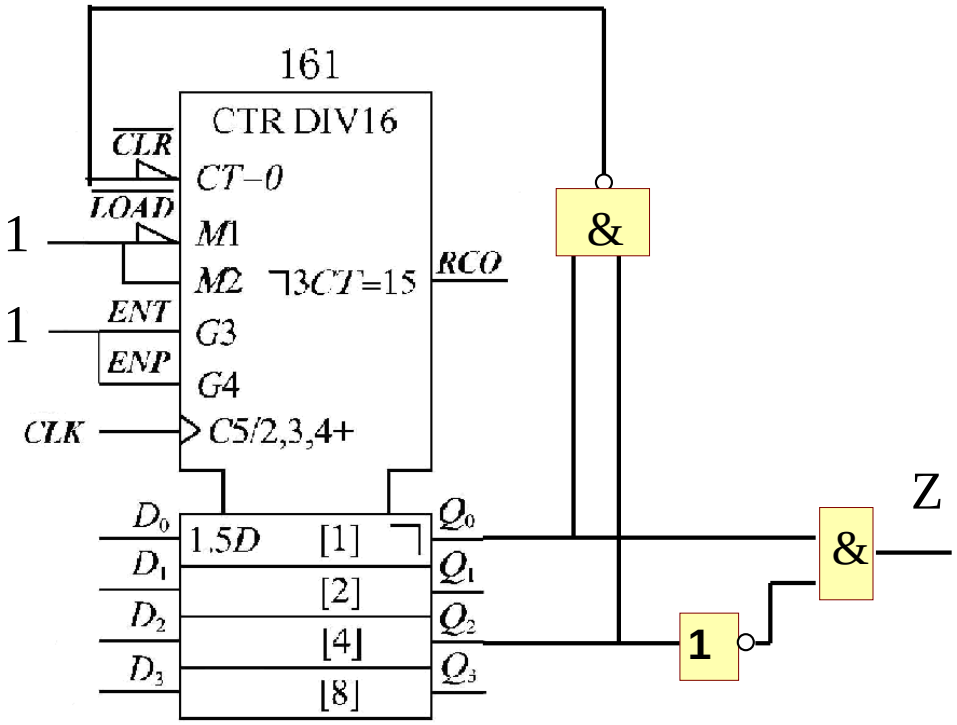

CLK
Y
1
2
3
4
5
6
7
8

例2. 用序列信号发生器实现数据并/串转换

Counter and MUX



例3 . 分析下图电路.



74161 : M-5 计数器

(000) ~ (100)　(110) 毛刺

$$Z = Q_0 \cdot \overline{Q}_2$$

输出为原状态的输出

状态表

Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Z
0	0	0	0	0	1	0
0	0	1	0	1	0	1
0	1	0	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	0	0	0

计数器从000 到100 循环, 相应的输出为 **01010.**

电路功能：产生 **01010** 序列信号的序列信号发生器.

作业:

6.2　　6.3

6.8　　6.9

6.12　　6.15

6.19　　6.21