# Lab 4

## Files Provided:

Same code is as Lab 3.

## Your Job:

**Part 1:** Create a three staged pipelined SMIPS processor. The three stages are as follows:

1. Fetch, Decode, Register Read,

2. Execute, Memory

3. Writeback

Your solution should execute instructions correctly and maximize performance. You will need to deal with data hazards for this lab. Scoreboarding is one way to achieve this goal.

Determine the throughput of your solution. Have you really maximized performance? Do all of your rules fire every cycle?

**Part 2:** Add bypassing to your pipeline. Determine the throughput of your solution. Have you really maximized performance? Do all of your rules fire every cycle?

答：时钟周期有：

Cycles = 46873

Insts = 21628

Cycles = 14680

Insts = 6873

Cycles = 6338

Insts = 3020

Cycles = 19119

Insts = 9909

Cycles = 773

Insts = 369

Cycles = 48016

Insts = 21100

平均为Cycles/ Insts:

(46873/21628 + 14680/6873 + 6338/3020 + 19119/9909 + 773/369 + 48016/21100)/6 = 2.12

Insts/Cycles = 0.47

## Submitting Your Solution

Provide all of the files that you changed in the same format as Lab 1 (but, of course, using Lab4 as the prefix to the directory.) Provide the answers to the questions in an answers.txt file.