PORT	, AF(AF2	AF5	AF6	AF7	AF8	AF9	AF14	CMP1 CMP2 CMP3 CMP4 CMP5 CMP6 CMP7	OP1 OF	P2 OP3 OP4	ADC	DAC1	配置	
TOKI	SYS		TIM3 TIM15	SPI1 SPI2	TIM1 SPI3			TIM15 CAN	USB		Of 1 Of	12 013 014		DACI		
)	CH1				CTS	OUT			INM INP			ADC1_IN1		X KEY	
		CH2				RTS		CH1N		INP	VINP	VINP	ADC1_IN2		X	
	2	CH3				TX		CH1		INM	VOUT		ADC1_IN3		O EXP	
	3	CH4	CHO	NICC	NGG	RX		CH2		INP	VINP/M	MINID	ADC1_IN4	OLIT1	O EXP	
4	1 -	CIII	CH2	NSS	NSS	CK				INM INM INM INM INM INM	MDID MD		ADC2_IN1 ADC2_IN2		O EXP	
		CH1 CH1	CH1	SCK MISO	BKIN		OUT			INM INM INM INM INM INM	VINP VIN VO	the state of the s	ADC2_IN2 ADC2_IN3	0012	O EXP O EXP	
	7				CH1N		OUT			INP	VINP VI		ADC2_IN3 ADC2_IN4		O EXP	
PA	MC		CHZ	WOSI	CH1	CK	001			11/1	VIINI VII	INI	ADC2_IN4		X EXI	
) IVIC				CH2	TX		BKIN							O U1 TX	
1	0	BKIN			CH3	RX									O U1 RX	
1	1			MOSI	CH1N	CTS	OUT	RX	DM						X USB DM	
1	2	CH1			CH2N	RTS	OUT	TX	DP						X USB_DP	
1	3 JTM	CH1N				CTS									X SWDIO	
1	4 JTCI				BKIN	TX									X SWCLK	
1	5 JTD			NSS	NSS	RX									X UWB_CS	
()		СН3		CH2N					INP	VII	NP VINP	ADC3_IN12		X ADC_BA	Τ
	1		CH4		CH3N		OUT					VOUT	ADC3_IN1		O EXP	
	2	CYV2		COV	COV	my.				INM		VINM	ADC2_IN12		O EXP	**
	JIDO	CH2	CIII	SCK	SCK	TX									X UWB_SCI	
	т	CH1 BKIN	CH1 CH2	MOSI	MISO MOSI	RX CK									X UWB_SD X UWB SD	
	5	CH1N	СП2	MOSI	MOSI	TX									X UWB_SD	
	7	CHIN				RX									X UWB EX	
PB	3	CH1				TOX	OUT	RX							X UWB WA	
	9	CH1					OUT	TX							X UWB RS	
1	0	СН3				TX				INM		VINM VINM			O EXP	
1	1	CH4				RX				INP		VINP			O EXP	
1	2			NSS	BKIN	CK				INM		VOUT	ADC4_IN3		O EXP	
1	3				CH1N	CTS				INP		VINP VINP	-		O EXP	
1	4	CH1			CH2N	RTS				INP	VII	NP	ADC4_IN4		O EXP	
1	5	CH2	CH1N	MOSI						INM			ADC4_IN5		O EXP	
1															X LED_B	
PC 1	4														X LED_G	
1	5														X LED_R	