Lab 4: BJT as a Voltage Amplifier: Common Emitter Mode Part 2: the Demo

Prerequisite:

You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.

You must have solved Part 1 of this lab assignment – design of a BJT in Common Emitter mode as a voltage amplifier of Gain = –10 and other design specifications as per Part 1. A working LTSpice simulation of the full circuit will be used in matching your measurements of the built-up circuit to the ones predicted from LTSpice.

In case you are not confident of your design from Part 1, the official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Grand goal: Part 2

Demonstrate a working circuit of a BJT configured as a voltage amplifier.

Input provided must be ±0.3V @ f=1.17kHz. With the design specification of Gain = –10 , we expect to see an output voltage swing of ∓3V (negative sign is implicit in the design!)

To help you demonstrate your circuit building expertise and earn piece-wise marks, we have split up the circuit demo into separate parts

Level 0: Function generator (FG) is it still working?) 10

Demonstrate that the FG built earlier and used several times in the past labs is still working! Include a photo of your built-up FG with **no load** connected at the output except the DSO probes. Set the output potentiometer to produce a sawtooth waveform of ±0.3V @ f~1.17kHz

This will be your input for subsequent testing, so we make sure that FG is functioning correctly.

Clear photo of standalone FG circuit with DSO output trace at ±0.3V amplitude and ID in frame expected. This is basically to check that the FG is working OK, since we will soon be mystified by reduction in amplitude when our newly built CE voltage amplifier is connected.

Level 1: Voltage amplifier circuit build Sanity check 10

From LTSpice simulation of circuit as designed in Part 1, you should have a clear prediction of the node voltages at various points in your amplifier circuit with no v_{in} applied.

Build your amplifier with 1 BJT. Keep the FG disconnected completely from V_{CC} (since that seems to cause issues with V_{CC} fluctuation as the Q_i in the FG itself slam back and forth from saturation to cutoff). Also don't connect the output of the FG to the input of your amplifier yet.

Using a DMM, check the DC voltages at various nodes in your circuit: V_{CC}, and the BJT terminals C,B,E. Match the measured values to your expectations from design calculations and LTSpice simulation and list them here

This will give you confidence that your BJT voltage amplifier circuit is built correctly and BJT is biased into forward-active mode

V_C ~ 4V (design is for 4.5V, but batteries drained by now in week 3 + V_{cc} funny business – DMM just provides avg DC reading)

V_B ~ 0.9 to 1.1 V

V_E 0.3 to 0.4V (have designed for 0.47V) LTSpice shows AC modulation 0.28V-0.36V even if v_{in} absent, due to V_{CC} modulation by the FG. FG is included in the simulation by default as per instruction given to students to design their circuits on top of the published FG LTSpice simulation. DMM shows avg reading between 0.28V ~ 0.36V

Level 2: Voltage amplifier working with $v_{in} = 0.3V$ 20

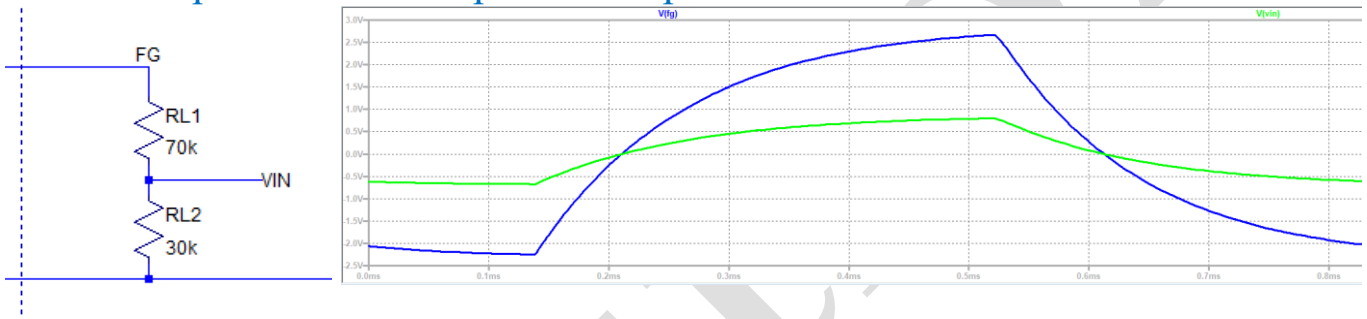
Connect the full end-to-end circuit together: FG → RC-CR shaper → newly built BJT voltage amplifier as per the full LTSpice simulation design of Lab 4, Part 1

Turn power ON and double check the power indicator light, that V_{CC} is indeed reaching your breadboard!

Now your FG *should* be putting out a ±0.3V sawtooth voltage waveform (checked in Level 0) and the newly built BJT common-emitter voltage amplifier

should be ready to amplify that voltage (checked in Level 1)
Proceed to test the combination by connect output of your FG to v_{in} of your BJT amplifier. Answer the following questions by performing the hardware checks sequentially – this will help you characterize and understand the built circuit.

2.1) Does the input impedance R_{inp} of your BJT amplifier cause loading on your FG output, pulling down v_{in} amplitude? For example, V(FG) driving a 100k potentiometer load should be putting out a ±2.5V output. A 30k:70k split of the potentiometer should give you ±0.75V as v_{in} to your newly built BJT amplifier circuit as per the LTspice simulation:



After connecting output of your FG to v_{in} of your BJT amplifier with a 30:70 split ratio of your potentiometer, do you in fact get ±0.75V swing of v_{in}?
Explain quantitatively why not?

2.1.A) Amplifier input R_{inp} loads the FG output. Explain how? **4**

Use equations, calculate the effective impedance loading the FG. There is the resistor divider in the 100kΩ potentiometer and R_{inp} of the amplifier to be taken into account!

Load on FG is R_{inp} of the CE amplifier. R_{inp} ~ 12kΩ with our choice of R_{BB1} & R_{BB2} in Part 1. Exact value will depend on student's choice of R_{BB1}, R_{BB2} but R_{inp} will be $\mathcal{O}$(kΩ) as per design procedure

R_{inp} appears in parallel with RL2 of the FG output potentiometer. So the FG output is really divided in the ratio RL1 : RL2||R_{inp} Since the latter quantity is now reduced (RL2 was already $\mathcal{O}$(kΩ),

so RL2||R_{inp} will be halved best case, could be worse.

NOTE AND HINT FOR THE FUTURE:

this design specification of R_{inp} comes about as a secondary feature of the other prior design specs – you can turn the design process around and make R_{inp} the starting point of your design process!

2.1.B) INPUT DEMO 5

Instead of re-designing and re-building the whole circuit (big headache when you are likely within a few hours of the submission deadline!), simply adjust the potentiometer setting – you should be able to find some ratio of RL1:RL2 that gets you

$v_{in} \sim \pm 0.3$V at $f \sim 1$kHz

Put a photo of your setup here with DSO measurement of v_{in}

2 Photos expected with captions. Note that for this case FG output is in fact connected to the DC verified CE voltage amplifier.

Photo 1 (this question 2.1.b): output of FG which is sent as v_{in} into the CE amplifier

What is the value of RL1:RL2 you ended up using to get $\pm 0.3 v_{in}$ swing? Does it match your calculation of Part 2.1.A? **1 mk bonus**

Note that it is incorrect to measure these resistors *while they are connected in the circuit.* You will have to apply some skill to take the potentiometer out of the circuit. Safest is to plug it into another blank area of your breadboard and use little probe wires to measure the resistor divider values. Of course, don't forget to put it back correctly in the circuit without changing the value!

This is a general principle of practical electronics – if you try to measure values of components like resistors with a DMM while they are connected in the circuit, you will end up measuring the value in parallel with all the other nearby (and sometimes far away) circuit nodes. You may find out later in life that this makes it very difficult to debug fully assembled complex PCB's with many components of which one or two may have malfunctioned.

2.1.C) OUTPUT DEMO 10

Probe v_{out} of your amplifier circuit. With effectively infinite impedance of your DSO probe, you should get close to the simulated voltage gain from $v_{in} = \pm 0.3$V

Put a photo of your circuit (with ID) and a DSO measurement of v_{out} highlighting the measured amplitude of v_{out} and hence the measured voltage gain

Photo 2 (2.1.C): v_{out} from CE amplifier, indicating $v_{out} \sim G \times v_{in}$

Actually measured gain may be in the range of $G \sim -7$ *to* -9 due to component tolerances. Typically students measure w.r.t peak values where V_{CC} misbehavior may be causing problems. It will be asymmetrical in the two half cycles of v_{in} (why??)

If measured $|G| << 9$, detailed investigation must be provided, else −3 marks

Level 3: Explore limits of voltage amplification **10**

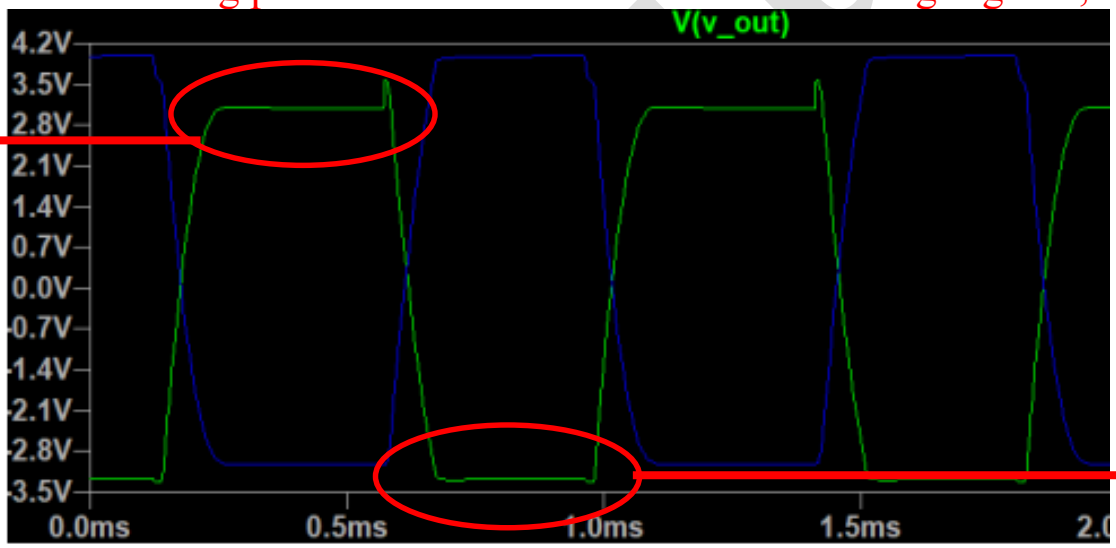
With v_{in}=±0.3V swing, you can see that the amplification is (mostly) linear and fixed except for some artifacts near the extremes. Thus the amplifier is able to amplify any v_{in} in the range 0 – ±0.3V

Increase v_{in} to higher values by adjusting the potentiometer of the FG.
Put a photo of your measurements here when you see deviation from linear gain.
Make a note of what is the value of v_{in} swing when v_{out} does not show a smooth amplified sawtooth waveform, but flattened edges near the extremities. Is the flattening present at both positive and negative extremities of v_{out}? **5**

See nonlinearity "flattening" at extremities when v_{in} reaches ~ ±0.5V.
Photo expected indicating v_{out} flattening near extermities at both ends

Provide quantitative explanation of why you see a deviation from linear gain **5**

LTSpice simulation plot or DSO screen photo both acceptable for this question.
The following points and numerical values must be highlighted, each for 2.5 mark



CUTOFF: v_{out} clips at +3V : at that point, absolute $V_C = V_{CQ} + v_{out}$ ~ 7.5V getting close to V_{CC}
So I_C through R_C falls close to 0 and Q1 is cut-off **2.5 mk**

SATURATION: v_{out} clips at -3V : at that point, absolute $V_C = V_{CQ} - v_{out}$ = ~ *1.5V and* $V_B = V_{BQ} - v_{in}$ ~ 1.2V – 0.3V ~ 0.9V. Since V_B is close to V_C we are close to breaking the CB revese bias condition, and getting Q1 to saturation. Exact deviations will depend on component values and bias voltages hence some asymmetry is to be expected (revise 2.1.C above!) **2.5 mk**