

Lab 3: BJT as a current source: Emitter Follower

[80 + 20 advanced]

Prerequisite:

You must have a working simulation and physical implementation of a waveform Function Generator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.

The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

Stop time = 101m

Time to start saving data = 100m

Maximum time step = 0.01m

This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ $f \sim 1kHz$

Grand goal:

Design a BJT based circuit that has no voltage gain, but is able to amplify a small input current to a large output current. In terms of impedance, it means that the final circuit design must have very high input impedance and very low output impedance. This is very attractive for practical applications, since most electro-mechanical devices are driven by current.

Note about terminology of ‘current’ used in this assignment:

- 1) We consider the traditional Kirchoff’s Law current I in the circuit design and analysis. This current can be flowing in either direction across two nodes in a circuit. Though as explained in the introduction session, inside an NPN/PNP transistor, the current I flows exclusively from the Collector to the Emitter.
- 2) The term AC current used here refers to a time-varying current, and is denoted in small case i . In contrast, a DC current denoted by capital letter I is one whose value remains constant with time. Generalizing, a DC voltage is one which is constant in time (like the 9V supply to your circuit), and an AC voltage is one which varies as a function of time, like the output of your FG.
- 3) If V_{out} is supplying current to the load, we say the circuit is ‘sourcing current’. Vice-versa, if current is being pulled *into* the circuit from the load, we say the circuit is ‘sinking current’

Part (A) Circuit Design

Fig 1 shows the basic structure of a current amplifier circuit . In principle, since $I_C = \beta I_B$ this is all you need to crack this lab assignment! or... is it?

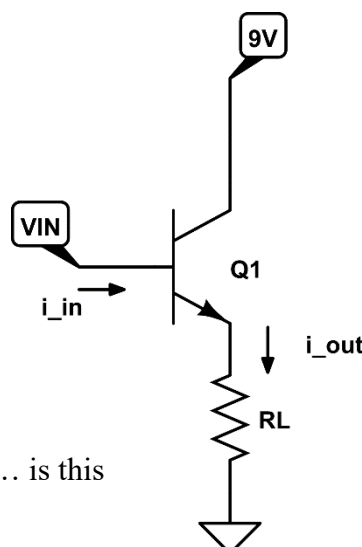


Fig 1:
The BJT current amplifier... is this
all there is to it?

Level 0: The “crack”

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If V_{in} is an AC voltage whose value can be both positive and negative,

0.1 What are the assumed conditions required for $i_{out} = \beta i_{in}$? List all: **1**

The transistor must be in the active mode, i.e. the EBJ must be forward biased and the CBJ must be reverse biased.

0.2 What are the necessary absolute and relative voltage conditions required at the C, B, E terminals of Q1 to use it as a current amplifier? **1**

$$V_{BE} = V_B - V_E = 0.7V \text{ and } V_{CB} = V_C - V_B > 0V$$

0.3 Including the load R_L as a part of your circuit is always a recipe for disaster. Will the circuit still work as a current amplifier as per design specifications if the following things happen? (explain your answers fully)

a) if R_L burns out due to excessive current? In electrical terms, $R_L \rightarrow \infty$?

1

Yes, it will work.

Or

b) R_L short-circuits due to Q1-E accidentally touching GND? **1**

No, it will not work

Or

c) R_L is frequency dependent, i.e. $Z_L = f(\omega)$ where f is not known **1**

No, it will not work

Level 1: Basic Design

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After having understood the limitations of the skeleton circuit of Fig 1 in Level 0 design a practical current amplifier using 1 NPN transistor with the following design parameters:

1. deliver PEAK power to load _____ = 5mW
2. Assume purely resistive load R_L _____ = 500 Ω
3. V_{CC} _____ = 9V
4. Amplifier has a high-pass f_{3dB} _____ = 100 Hz
(i.e. noise in V_{in} below 100Hz will be rejected)
5. Transistor β _____ = 300

Typical application scenario: an audio amplifier for headphones. The coil driving the speaker diaphragm in your headphones has $\mathcal{O}(100\Omega)$ resistance. Given the small size of the speaker in the headphone, 80mW peak power should drive it up to ear-splitting volume.

You will find that with the basic design, the amplifier circuit itself consumes power from V_{CC} *even if there is no V_{in} applied*. We will calculate this idle power dissipation, and ways to avoid it in Level 2 and Level 3

Here is the step-by-step design procedure:

From cracking Level 0, it is obvious that the BJT terminal voltages must be setup such that it always remains in the forward-active operation mode. Here are ways in which this can be accomplished, without too much complexity:

DC Design: Give your calculation steps for each of the questions below

- 1) Pick a value of I_C that must flow at the ‘quiet’ operating point. This is called the quiescent current I_{CQ} . Even when V_{in} is 0, the transistor must be ready to supply a range $I_{CQ} \pm \delta I$.

Choose $I_{CQ} = 10\text{mA}$

Since PEAK power delivery is specified, What δI do you expect to deliver to the load *if* the load were directly connected to E as in Fig 1?

1

3.16 mA

- 2) You *don't* want to include R_L in the core circuit of your amplifier! Yet you must use a resistor at the emitter to fix a DC value of V_E . Call this resistor R_E and calculate its value to set the DC value of V_E to be approximately half of V_{CC} . What is R_E ?

450 Ohms

1

3) Use a resistor divider with resistors R_{B1} & R_{B2} to set the bias voltage V_B such that BE junction is always forward biased. There are three competing considerations in choosing suitable values of R_{B1} & R_{B2}

- a. Base current I_B at DC must be kept very small $\sim \frac{I_Q}{\beta}$ When the BE junction is forward biased, it has an equivalent resistance of $r_e = \frac{25mV}{I_Q}$
The effective resistance 'looking into' the base is thus $R_B = \beta(r_e + R_E)$
 R_{B1} in series with R_{B2} must provide a preferred current path to ground from V_{CC} than R_B . i.e. $(R_{B1} || R_{B2}) \ll R_B$
- b. R_{B1} and R_{B2} are in series from V_{CC} to ground, hence this path will *always* pass DC current and contribute to the amplifier's idle power dissipation.
- c. R_{B1} & R_{B2} will play a role in the $f_{3dB} = 100\text{Hz}$ filter so you might have to iterate with the AC design below:

What is your choice of R_{B1} & R_{B2} ?

1

$R_{B1} = 22\text{k Ohms}$ and $R_{B2} = 33\text{k Ohms}$

AC Design:

We want the amplifier to have a high-pass filter at $f_{3dB} = 100\text{Hz}$. Keeping the core DC amplifier design as finalized above, we can add on high pass filters at the input and output.

4) It is easier to start at the output side. Add a single component high pass filter before R_L . What is the value of this component?

1

$3.18\mu\text{F}$

5) Now at the input side, we must take into account the entire input impedance of the amplifier circuit (*including R_L reflected through the amplifier*)

Take this input impedance to be $R_{inp} = (R_{B1} || R_{B2}) || \beta(r_e + R_E || R_L)$

Calculate R_{inp} with the previously chosen component values

11.5k Ohms

Accordingly add a single component series high pass filter for $f_{3dB}=100\text{Hz}$.

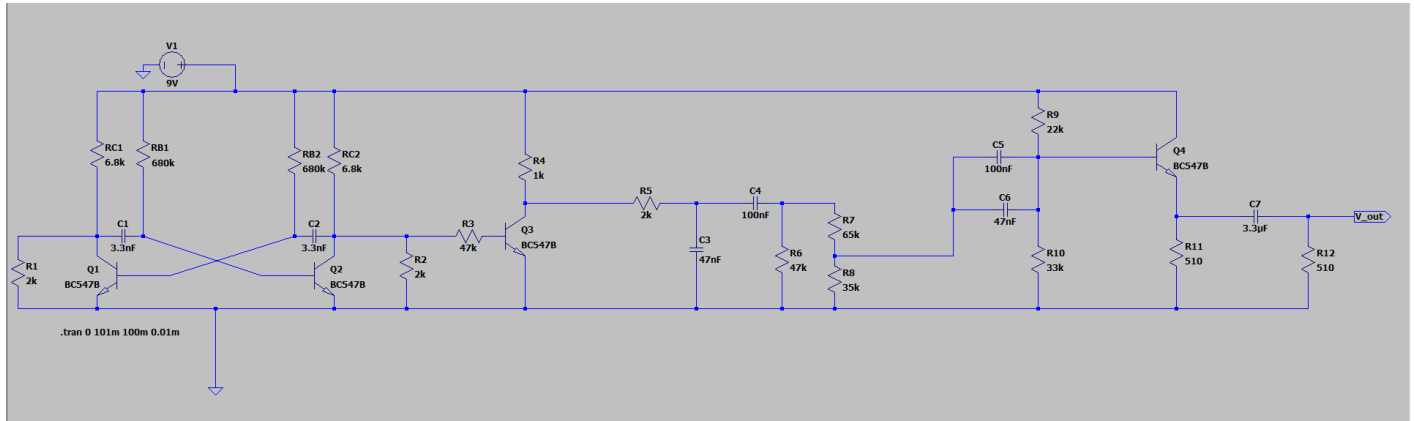
What is the value of this component?

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138nF

Paste a circuit diagram of the current amplifier created in LTSpice as per the above design calculations here. Provide the simulated test results:

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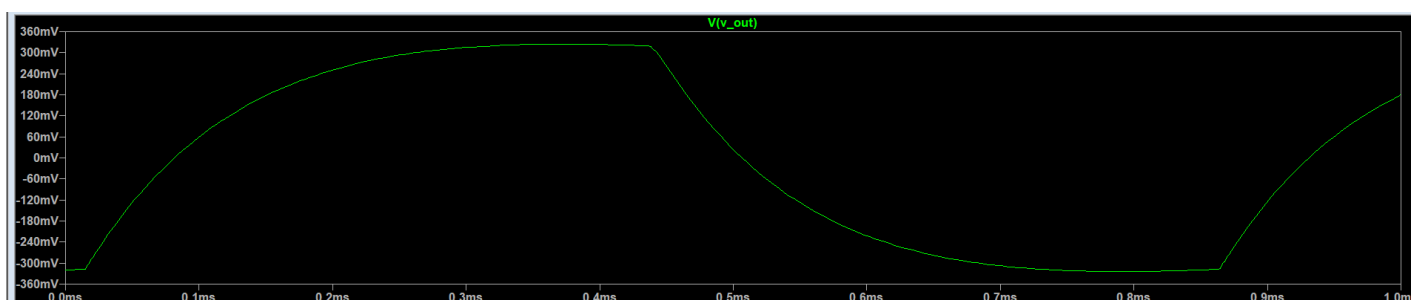
Simulations:

Use the FG simulation done earlier to provide V_{in} to your amplifier circuit. This will be a frequency $f \sim 1.17\text{kHz}$ so it should sail through the 100Hz high-pass cutoff frequency of your amplifier.

Specify V_{in} to have a pk-pk signal of 1V, centered around 0V. i.e. V_{in} should swing between +0.5V and -0.5V. Measure current delivered to the load R_L both as a current probe in LTSpice, and the voltage across R_L which you will measure in the circuit demo

Try a few higher values of V_{in} pk-pk variation: 1.5V, 2V, 2.5V Do you observe a trend? Is there a reason for the circuit's (mis)behavior?

Put your simulation output plots here:



Level 2: Circuit Demo

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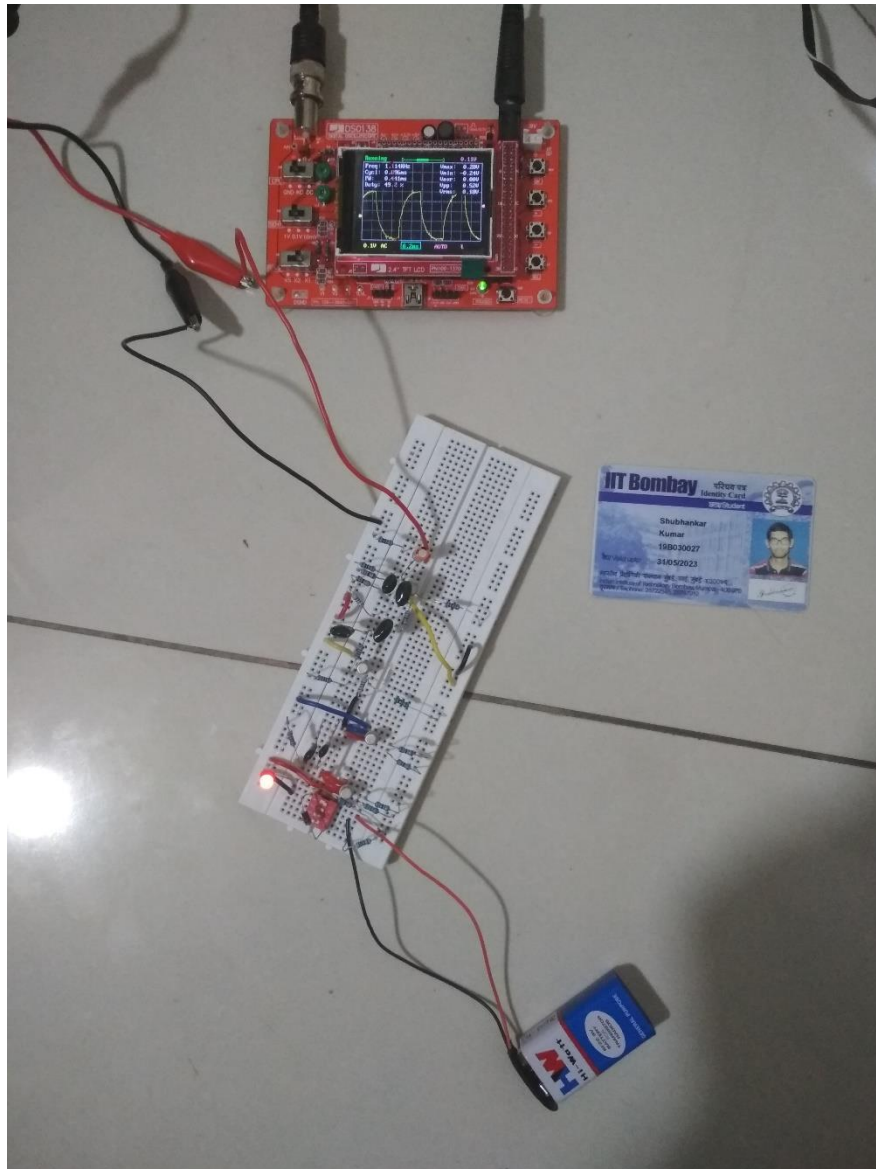
Build the circuit as designed and simulated in Level 1.

Use the FG as per standard design built earlier to provide V_{in} to your amplifier circuit..

Before connecting V_{in} and poking around with the DSO, follow the usual debugging steps: check DC voltage values at each significant node of the circuit to make sure they match the simulation and your circuit is wired up correctly. It's a good idea to explicitly write them down, since variations caused by component value tolerances may affect performance.

Connect V_{in} and probe the voltage across R_L . Provide photos of your full setup with ID card in the frame as usual.

Dividing by R_L allows you to re-calibrate the measured waveform V_{RL} into a current R_L



Based on your measurements, determine the current gain $\frac{I_L}{I_{in}}$ actually achieved in your circuit. Is it symmetrical for both polarities of V_{in} ?

Current gain = $(630\mu A)/(11\mu A) = 57.2$

Yes, it is symmetrical for both polarities of V_{in}

Level 2: Power analysis

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For the following analysis, it is adequate to consider the peak power consumption. RMS power formulae are applied for sinusoidal waveforms, but our test waveform is *not* a sinusoid. So you may simply take $V \cdot I$ products at the peak values.

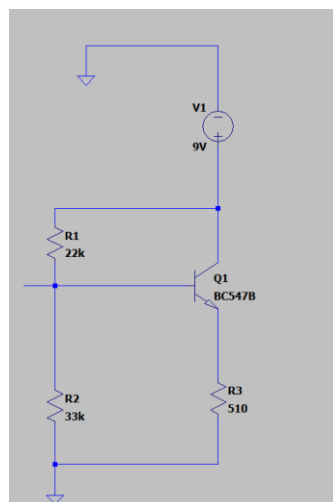
1) DC power consumption at idle. Disconnect V_{in} and V_{out} : Now your amplifier is ON and idling at DC. It is ready to amplify current, but there is no input to be amplified.

Measure the power consumed by the amplifier circuit from V_{CC} in idle condition at the Q-point

Find a clever method to do this without disturbing the circuit operation

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Power consumed = $V \cdot I = (5.7V) \cdot (860\mu A) = 4.9mW$



2) AC power consumption during amplification. Now apply a bipolar V_{in} input as earlier, and again measure the peak power consumed from V_{CC} (a suitable modification of the method used in 1.a) might be useful)

Keep the power consumed by the FG circuit and the load R_L as separate quantities. Power consumed by the FG can be measured independently and

subtracted, *before* connecting it to the amplifier to get AC power measurement during amplification. Power delivered to the load is measured separately below.

What is the power consumed by the amplifier circuit itself during AC operation?

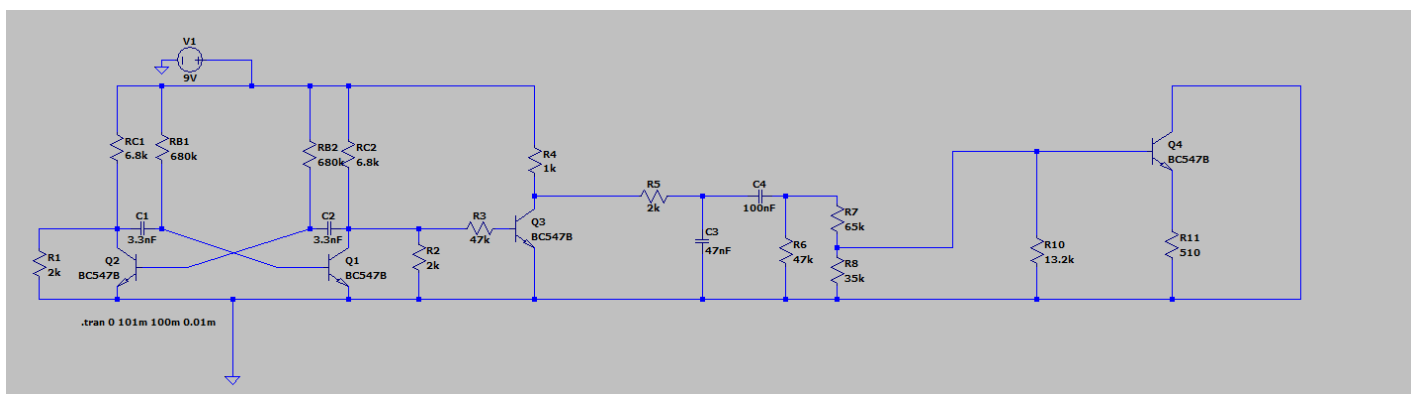
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$$\text{Power consumed} = (2.5\text{V}) \cdot (200\mu\text{A}) = 0.5\text{mW}$$

- 3) What is the power delivered to the load? (re-verify the Level 2 result)
Accordingly what is the ratio of power delivered to the load to the power consumed within the amplifier circuit itself?

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$$\text{Power delivered} = V \cdot I = (9\text{V}) \cdot (80\text{nA}) = 0.72\mu\text{W}$$



- 4) Provide a detailed analysis of why the current amplifier is unable to deliver the peak power specification to R_L .

- > Did you go wrong somewhere in the step-by-step calculations?
- > Was some operation assumption violated?
- > Is there a fundamental limitation to this circuit design that will never let it the desired peak power delivery specification?

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There is a fundamental limitation to the circuit design, due to which the desired peak power delivery cannot be achieved. In this case, the Voltage and currents are not constant.

Therefore, we don't get the maximum power, but rather, the RMS values are taken (which are lower than the peak values). Hence, the power delivered is less than the peak power.

Level 3: Optimize design to reduce power consumption 20

[Advanced bonus question]

3.1 Provide a rough circuit idea along the lines of Fig 1, to solve the main problem with power dissipation in amplifier v/s poor efficiency in delivering power to the load

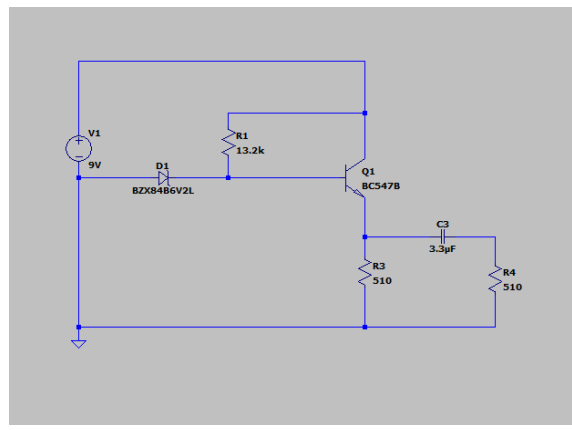
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One can add a Zener diode connected to the base of the transistor. This would filter out some voltages and hence, the power consumption by the transistor can be controlled accordingly.

3.2 Fill out your circuit idea of (3.1) as a full-fledged LTSpice simulation. Use the same design parameters as Level 1.

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Insert your circuit design image and the LTSpice simulation results here.



3.3 Build a working circuit as per your full design of (3.2) and demonstrate that it achieves close to the desired power delivery to the load

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As usual, provide a photo of your working circuit with your ID card and the measured DSO waveforms highlighting what is better about your Level 3 design