

PH231 Endsemester exam.A – Spring 2021

[50]

Prerequisite:

You must have a working LTSpice simulation and physical implementation of a waveform Function Generator (FG) that swings to both positive and negative voltages, as used in previous labs.

The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Add a 100 μ F (electrolytic) capacitor from V_{CC} to GND for the FG, and for the all other active modules involving BJT's, both in simulation and the built circuit. As discussed in lecture session, this prevents V_{CC} fluctuations caused by FG BJT's switching

Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

Stop time = 101m

Time to start saving data = 100m

Maximum time step = 0.01m

This skips the initial transients in the first 100ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ $f \sim 1\text{kHz}$

Exam.A Increase gain of voltage amplifier

Fig 1 shows the final design of a Common Emitter voltage amplifier from Lab 4. Use the component values shown in Fig 1 as the starting point for your design in this endsem assignment. You may have used different base bias resistor values & C_{in} , C_{out} in your own solution – please replace those with the standardized values shown in Fig 1

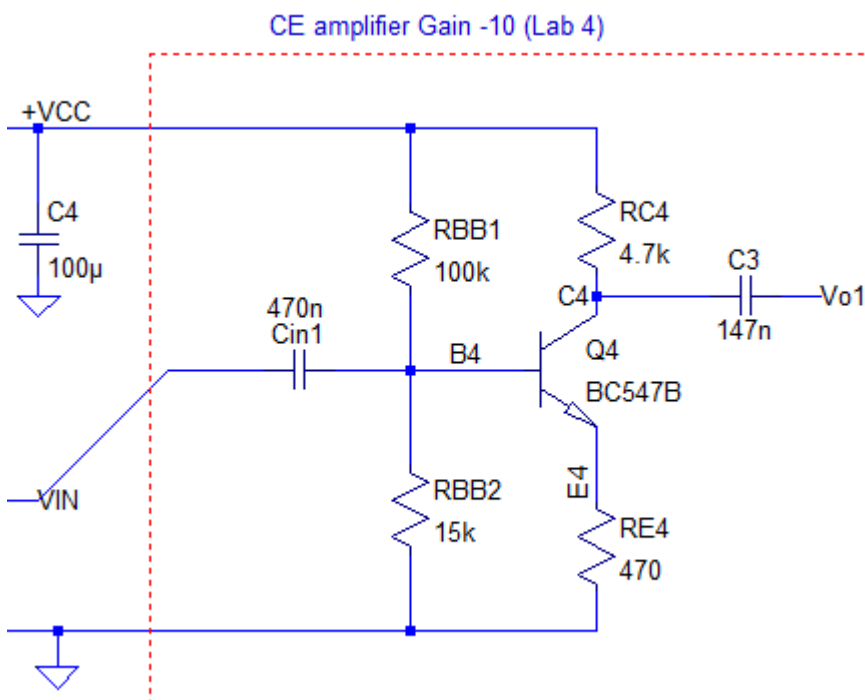


Fig 1: CE voltage amplifier
(model solution for Lab 4)

Use this as the starting point for this exam:

Design specifications used to arrive at this design were:

1. Assume $V_{CC} = 9\text{V}$ constant, and $Q1 \beta = 300$
2. Use $I_Q = 1\text{mA}$
3. Circuit gain = **-10**
4. high-pass $f_{3dB} = 100\text{ Hz}$
5. $v_{in} = \pm 0.3\text{V}$ @ 1.17 kHz

Level 1 Analyze and determine limits of performance

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(revision Lab 4)

Implement the above circuit model in LTSpice. You can answer the following questions using a combination of LTSpice simulation results and pen+paper calc

1. At the Q point ($v_{in} = 0$) what are the node voltage values at the BJT Q4 terminals? 1

$V_{B Q}$	V_{CQ}	$V_{E Q}$
1.15V	4.12V	0.44V

[explanatory note, not a question]:

As you may remember the design sequence for the Q-point is:

- set V_C at $\sim \frac{1}{2}V_{CC}$ to ensure maximum possible swing of v_{out}
- set V_E at $\sim 0.05 - 0.1V_{CC}$ ensuring that for chosen value of I_{CQ} , R_E dominates over r_e
- this gives V_B at Q-point required for forward active operation.

Apart from the DC value at B of $V_{B|Q}$ the input v_{in} is applied at B, hence the voltage at B is $V_B = V_{B|Q} + v_{in}(t)$. So we should have a clear idea of what is the range of voltage variation allowed at B, such that the BJT always remains forward active.

The following questions guide you towards the correct answer:

2. What are the allowed Upper and Lower limits of V_B to keep Q4 forward-active?

Upper limit voltage allowed for V_B ? 2.45V

1

Lower limit voltage allowed for V_B ? 0.225V

- What happens to V_C when V_B exceeds upper limit?
- What happens to V_C when V_B falls below the lower limit?

3. You have designed the circuit for $I_{CQ} = 1\text{mA}$. What is the actual value of I_{CQ} obtained with the component values used in the design? 1

1.1mA

4. What is I_B at the Q-point? 1

Keep in mind that this will be different in the simulation and the practically built circuit: the simulated model uses BC547B (easy to include in LTSpice) whereas in the breadboard circuit we use BC107

-0.1mA

5. With the above voltage & current parameters and the chosen passive component values what is the voltage gain expected from the circuit? Give your derivation with all the relevant formulae and the approximations/assumptions made: 1

$$v_{out} = -R_C i_C$$

$i_e = v_E R_E \sim v_B R_E$ since $V_{BE} = 0.7V$ is fixed (setting $r_e + R_E \sim R_E$)

Using $v_B = v_{in}$ and $i_C = i_E$ when β is large

We combine the above equations to get: $v_{out} = -R_C(i_E) = -R_C(v_B/R_E) = -(R_C/R_E)v_{in}$

Level 2.A Increase AC gain (concept crack)

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As discussed in the session notes, the main thing preventing us from reducing the denominator R_E in gain $-\frac{R_C}{R_E}$ is that we must keep $R_E \gg r_e$. It's the reason why R_E was put in the emitter leg in the first place!

1. What component can be **added** to the circuit such that terminal voltages of Q4 at DC remain unaffected, and yet we can analyze the AC behavior independently?

A capacitor C_{new} can be added parallel to R_E between the emitter and the ground.

2. With correct answer to question 1, it would be logical next step to add another component that comes into play only in AC operation. This component, in combination with R_E allows us to set the gain G of the amplifier while staying safely above the ' $\gg r_e$ ' limit. What is this 2nd component to be added?

Combine the answers to question 1 & 2 and draw a circuit fragment here of what goes between the Q4 – emitter and GND by adding these two components [TWO components are required to be added to Fig 1: you have to figure what they are, and how to connect them]

A resistor R_{E1} can be added in series with the above mentioned capacitor.

3. What are the design constraints that lead you to calculate the values of components you have chosen to add in answer to question 1 & 2 above?

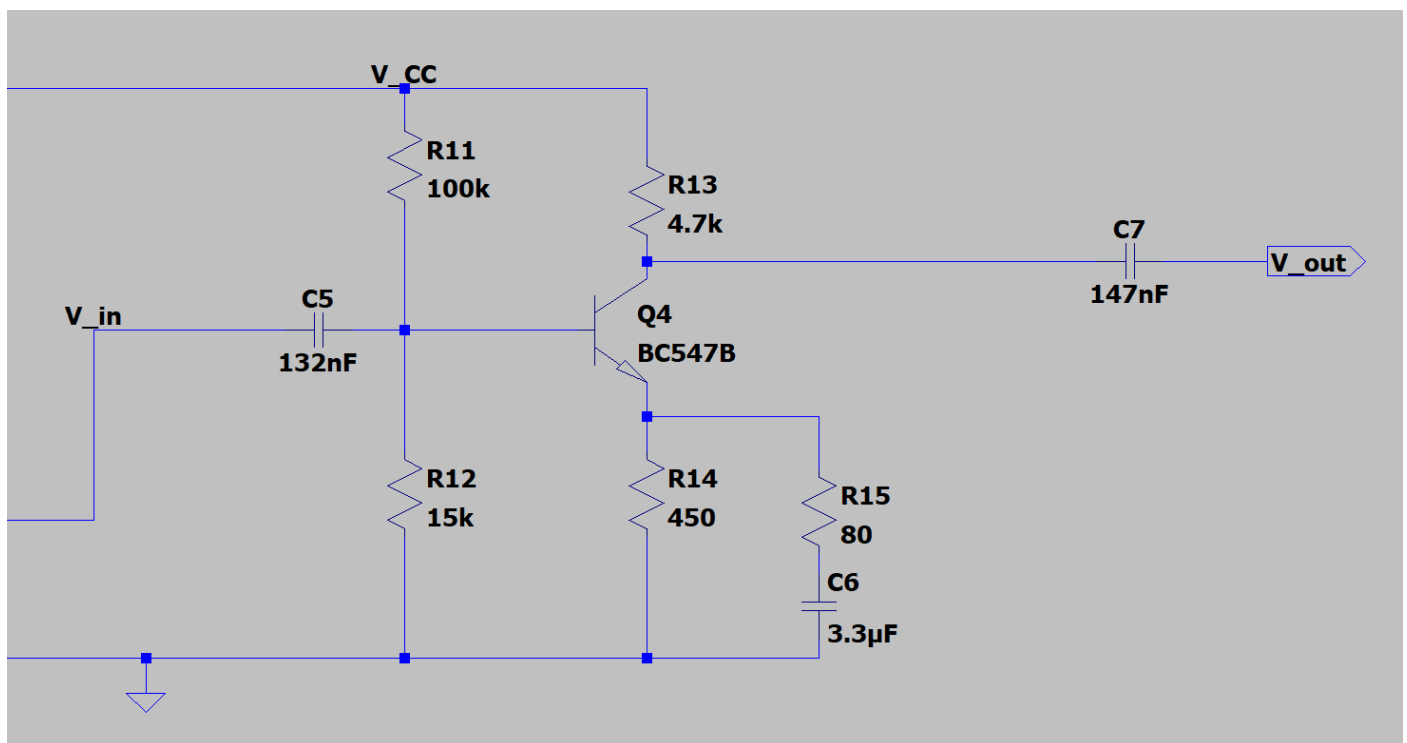
$$C_{new} = 1 / (2\pi f R) = 3.3 \mu F$$

$$R_E \parallel R_{E1} \gg r_e$$

Level 2.B Increase AC gain (design implementation) 5

Redesign the CE voltage amplifier of Fig 1 using the conceptual additions of Level 2.A to have a new set of design specifications:

1. Assume $V_{CC} = 9V$ constant,
and $Q4 \beta = 300$
2. Use $I_Q = 1mA$
3. Circuit gain $= -50 \rightarrow$ gain is $5\times$ higher!
4. high-pass $f_{3dB} = 100$ Hz



Level 3 High gain voltage amplifier

3.A) Circuit simulation

[5]

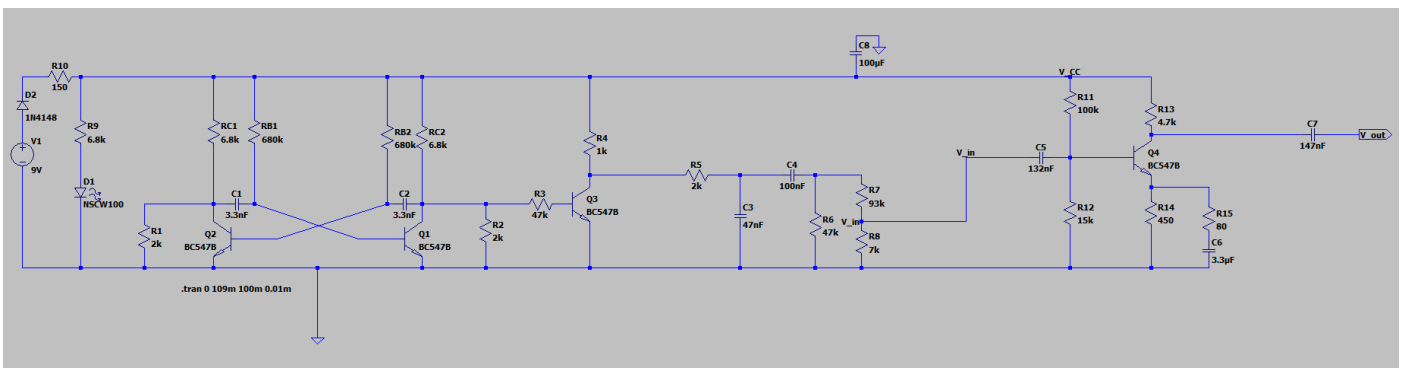
Make an LTSpice circuit simulation of your re-designed high voltage gain amplifier as per calculations of Level 2.B

- 1) Start with the standard FG simulation as published on Moodle.
- 2) Add the high voltage gain CE amplifier as a separate module, taking its v_{in} from the output of the FG potentiometer

Add a $100\mu\text{F}$ bypass capacitor between V_{CC} and GND as discussed in class, for both the FG and CE amplifier modules to reduce unwanted transients in V_{CC} supply.

Put your LTSpice circuit diagram here

1



Simulation results: (use the following LTSpice simulation parameters)

Stop time = 101m

Time to start saving data = 100m

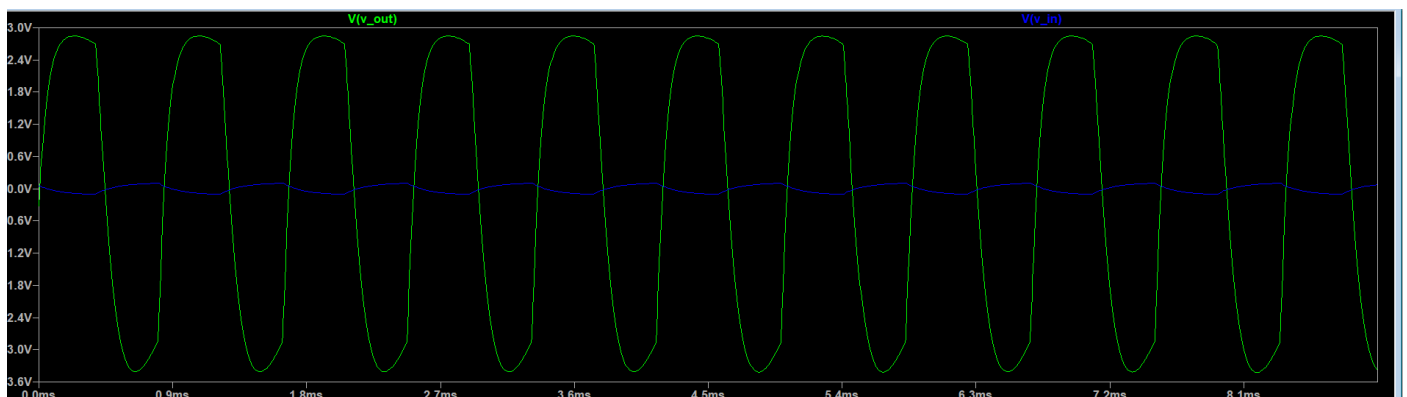
Maximum time step = 0.01m

Run the simulation and provide two output plots below:

Plot 1) $v_{in}(t)$ and $v_{out}(t)$ voltages (to be compared with experimental observations)

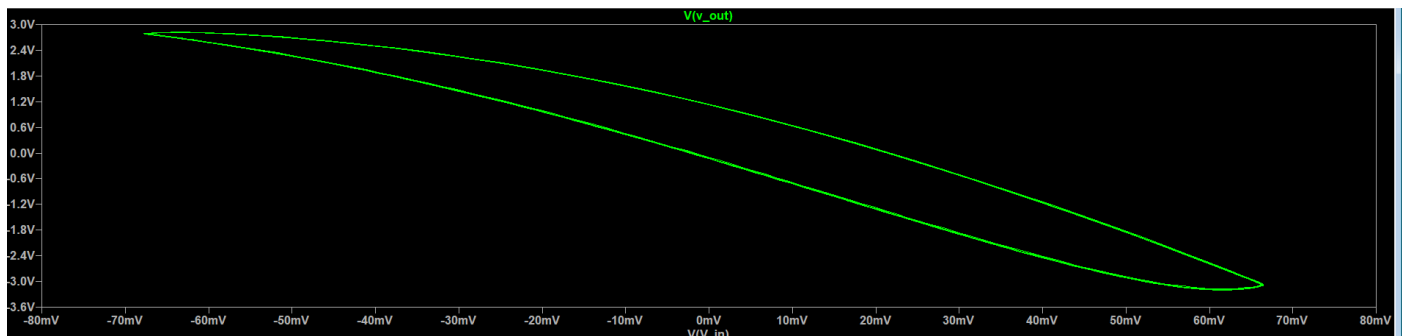
Typically you read off the peak values of the two voltages and decide the gain is the ratio of those voltages – this is not fully correct!

2



Plot 2) $v_{out}(t)$ v/s $v_{in}(t)$ demonstrating expected *linear* voltage gain. Plotting the ratio of $v_{out}(t)$ to $v_{in}(t)$ *throughout* the range of variation gives you a much clearer idea of the gain linearity (v_{in} and v_{out} are out of phase, so comparing just the peak values includes unwanted factors in the ratio)

2



3.B) Hardware demo:

[25]

Build the re-designed high gain CE voltage amplifier circuit of Level design on your breadboard. Adjust the FG output through the 100k potentiometer to obtain a desired range of v_{in} to your voltage amplifier.

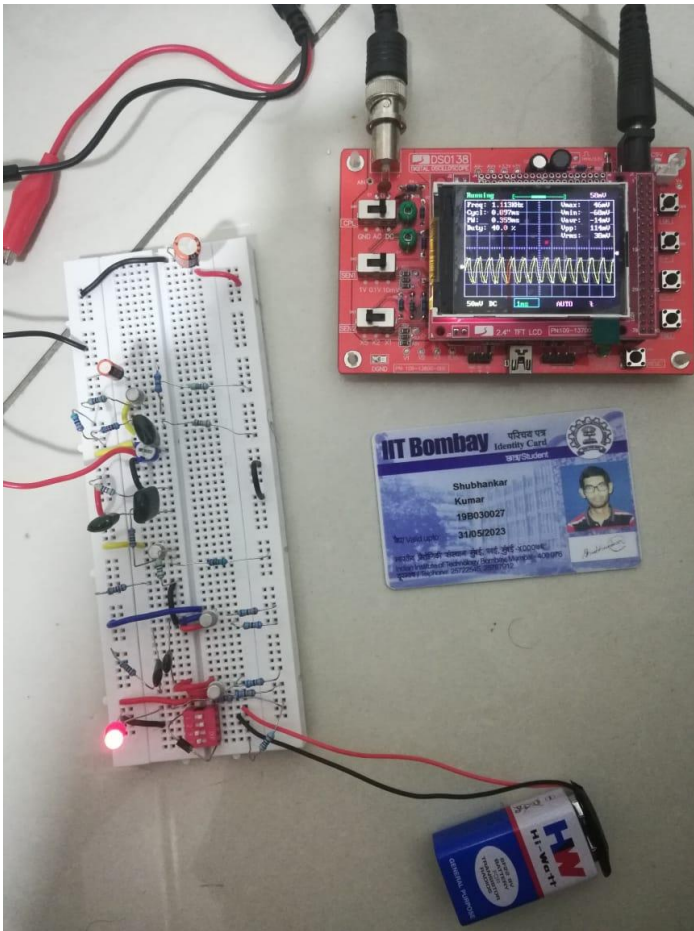
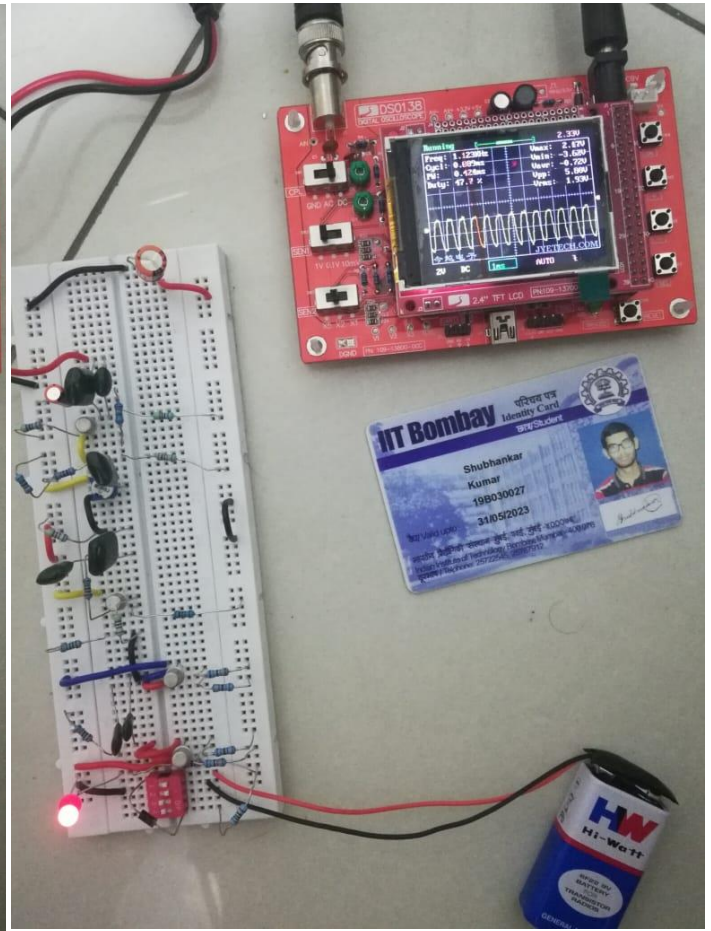
Put in photos of your successful demo below. Each photo must contain your circuit, the DSO trace measurement and your ID card:

Since the DSO has only one channel measurement, label each photo indicating which measurement is v_{in} and which one is v_{out}

1. v_{in} amplitude set to a (very small!) value such that you get $v_{out} \sim G \times v_{in}$ with $G \sim -50$

2 photos expected: 1 of v_{in} and 1 of v_{out}

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 V_{IN}

 V_{OUT}

2. v_{in} amplitude *increased* to a value such that v_{out} starts showing non-linearity similar to the type diagnosed in Level 1
- 2 photos expected: 1 of v_{in} and 1 of v_{out}
- use arrows and text labels overlaid on your photo indicating where the BJT goes into saturation or cutoff.

5

Square peaks
indicate
cutoff/saturation

