Lab 3: BJT as a current source: Emitter Follower

[80 + 20 advanced]

Prerequisite:

You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.

The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

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Stop time = 101m
Time to start saving data = 100m
Maximum time step = 0.01m
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This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ $f \sim 1kHz$

Grand goal:

Design a BJT based circuit that has no voltage gain, but is able to amplify a small input current to a large output current. In terms of impedance, it means that the final circuit design must have very high input impedance and very low output impedance. This is very attractive for practical applications, since most electro-mechanical devices are driven by current.

Note about terminology of 'current' used in this assignment:

1) We consider the traditional Kirchoff's Law current *I* in the circuit design and analysis. This current can be flowing in either direction across two nodes in a circuit. Though as explained in the introduction session, inside an NPN/PNP transistor, the current *I* flows exclusively from the Collector to the Emitter.
2) The term AC current used here refers to a time-varying current, and is denoted in small case *i*. In contrast, a DC current denoted by capital letter *I* is one whose value remains constant with time. Generalizing, a DC voltage is one which is constant in time (like the 9V supply to your circuit), and an AC voltage is one which varies as a function of time, like the output of your FG.
3) If V_{out} is supplying current to the load, we say the circuit is 'sourcing current'. Vice-versa, if current is being pulled *into* the circuit from the load, we say the circuit is 'sinking current'

Part 1 Circuit Design

Fig 1 shows the basic structure of a current amplifier circuit . In principle, since $I_C = \beta I_B$ this is all you need to crack this lab assignment! or… is it?

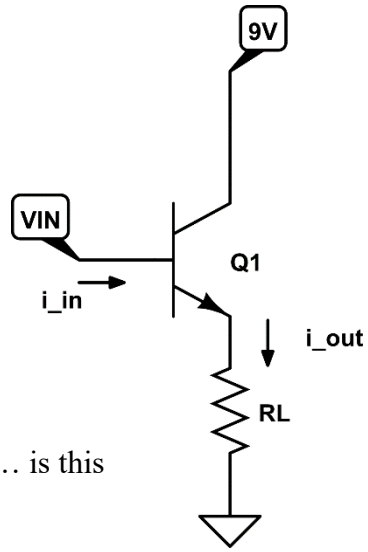


Fig 1:
The BJT current amplifier… is this all there is to it?

Level 0: The "crack" 5

If V_{in} is an AC voltage whose value can be both positive and negative,

0.1 What are the assumed conditions required for $i_{out} = \beta i_{in}$? List all: **1**

BJT must be in forward active mode ¼

BE junction must not go below reverse BE breakdown voltage of Q1 ¼

i_{CE} must never exceed maximum current rating Q1 ¼

R_L must remain constant, and be purely resistive ¼

0.2 What are the necessary absolute and relative voltage conditions required at the C, B, E terminals of Q1 to use it as a current amplifier? **1**

V_C is fixed at +9V, so $V_B < 8.3V$ always to keep CB reverse 1/3

$V_{BE} > 0.7V$ to keep BE forward biases 1/3

$V_E > 0V$ to make I_{RL} flow! 1/3

0.3 Including the load R_L as a part of your circuit is always a recipe for disaster. Will the circuit still work as a current amplifier as per design specifications if the following things happen? (explain your answers fully)

a) if R_L burns out due to excessive current? In electrical terms, $R_L \to \infty$? **1**

E left floating – V_{BE} and all the rest goes for a toss. Anyway, I_L=0, so no power to load!

Or

b) R_L short-circuits due to Q1-E accidently touching GND? **1**

Only $V_{in} > 0.7V$ allowed, negative cycle of V_{in} is rejected (this is hint for later analysis and Level 3!

Or

c) R_L is frequency dependent, i.e. $Z_L = f(\omega)$ where f is not known **1**

I_L delivery becomes frequency dependent, going from extremes of I_L=0 if Z_L=∞ to I_L clipped if Z_L=0 (other creative answers welcome!)

Level 1: Basic Design **15**

After having understood the limitations of the skeleton circuit of Fig 1 in Level 0

design a practical current amplifier using 1 NPN transistor with the following design parameters:

1. deliver PEAK power to load_____ = 5mW
2. Assume purely resistive load R_L_____ = 500Ω
3. V_{CC} _____ = 9V
4. Amplifier has a high-pass f_{3dB}_____ = 100 Hz
   (i.e. noise in V_{in} below 100Hz will be rejected)
5. Transistor β_____ = 300

Typical application scenario: an audio amplifier for headphones. The coil driving the speaker diaphragm in your headphones has $\mathcal{O}(500\Omega)$ resistance. Given the small size of the speaker in the headphone, 5mW peak power should drive it up to ear-splitting volume.

You will find that with the basic design, the amplifier circuit itself consumes power from V_{CC} *even if there is no* V_{in} applied. We will calculate this idle power dissipation, and ways to avoid it in Level 2 and Level 3

Here is the step-by-step design procedure:

From cracking Level 0, it is obvious that the BJT terminal voltages must be setup such that it always remains in the forward-active operation mode. Here are ways in which this can be accomplished, without too much complexity:

DC Design: Give your calculation steps for each of the questions below

1) Pick a value of I_C that must flow at the 'quiet' operating point. This is called the quiescent current I_{CQ}. Even when V_{in} is 0, the transistor must be ready to supply a range $I_{CQ} \pm \delta I$.

Choose I_{CQ} = 10mA

Since PEAK power delivery is specified, What δI do you expect to deliver to the load *if* the load were directly connected to E as in Fig 1? **1**

$$\delta I = \sqrt{\frac{(5m)^2}{500}} = 3.16mA$$

2) You *don't* want to include R_L in the core circuit of your amplifier! Yet you must use a resistor at the emitter to fix a DC value of V_E. Call this resistor R_E and calculate its value to set the DC value of V_E to be approximately half of V_{CC}. What is R_E? **1**

R_E = 4.5V/10mA = 450Ω (nearest standard values 470Ω/510Ω OK)

3) Use a resistor divider with resistors R_{B1} & R_{B2} to set the bias voltage V_B such that BE junction is always forward biased. There are three competing considerations in choosing suitable values of R_{B1} & R_{B2}

a. Base current I_B at DC must be kept very small ~ $\frac{I_Q}{\beta}$ When the BE junction is forward biased, it has an equivalent resistance of $r_e = \frac{25mV}{I_Q}$ The effective resistance 'looking into' the base is thus $R_B = \beta(r_e + R_E)$ R_{B1} in series with R_{B2} must provide a preferred current path to ground from V_{CC} than R_B. i.e. $(R_{B1}||R_{B2}) \ll R_B$

b. R_{B1} and R_{B2} are in series from V_{CC} to ground, hence this path will *always* pass DC current and contribute to the amplifier's idle power dissipation.

c. R_{B1} & R_{B2} will play a role in the f_{3dB} = 100Hz filter so you might have to iterate with the AC design below:

What is your choice of R_{B1} & R_{B2} ? **1**

R_{B1} = 22kΩ R_{B2} = 33kΩ (these are the nearest standard values, yet non-unique). Example: 12kΩ + 20kΩ also works. We just need to ensure $(R_{B1}||R_{B2}) \ll R_B$

AC Design:

We want the amplifier to have a high-pass filter at f_{3dB} = 100Hz. Keeping the core DC amplifier design as finalized above, we can add on high pass filters at the input and output.

4) It is easier to start at the output side. Add a single component high pass filter before R_L. What is the value of this component? **1**

$$C_{out} = \frac{1}{2\pi f_{3dB} R_L} = \frac{1}{2\pi * 100 * 500} = 3.18\,\mu F \quad (3.3\mu F \text{ OK!})$$

5) Now at the input side, we must take into account the entire input impedance of the amplifier circuit (*including R_L reflected through the amplifier)*
Take this input impedance to be $R_{inp} = (R_{B1}||R_{B2})||\beta(r_e + R_E||R_L)$

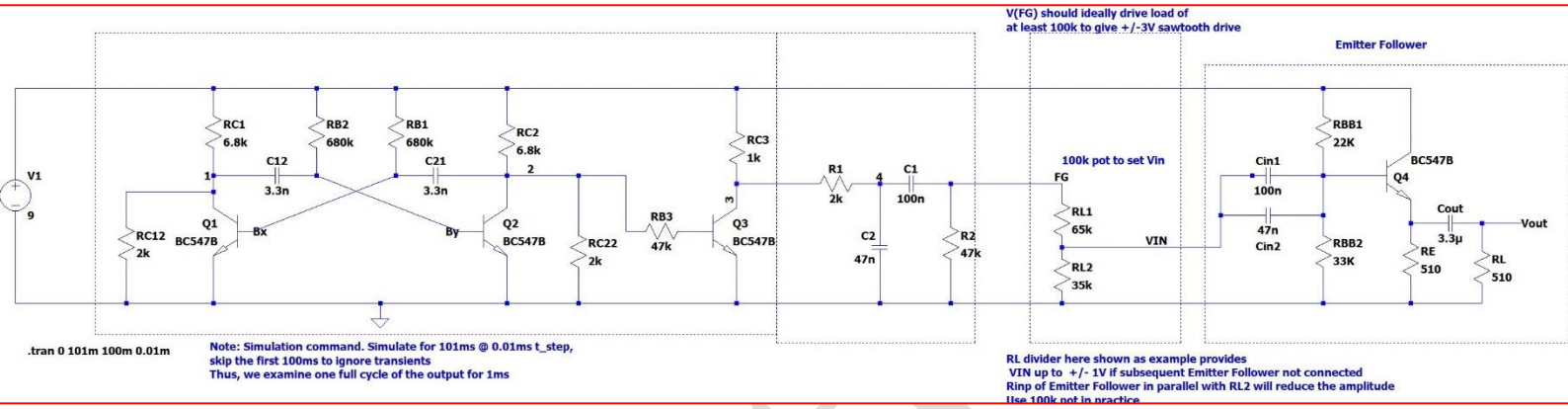
Calculate R_{inp} with the previously chosen component values

$R_{inp} = 11.5k\Omega$

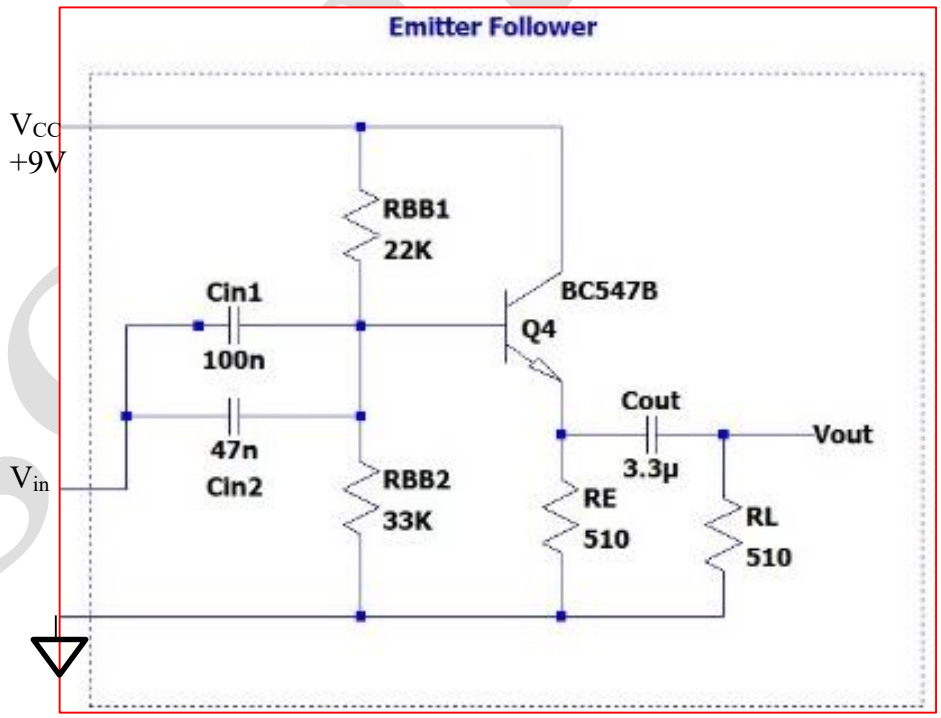
Accordingly add a single component series high pass filter for f_{3dB}=100Hz. What is the value of this component? **1**

$C_{in} = \frac{1}{2\pi f_{3dB} R_{inp}} = \frac{1}{2\pi * 100 * 11500} = 138nF$ (suitable parallel combo of standard values OK). We are going to test at a fixed $f = 1.17kHz$ so the exact high pass f_{3dB} is not very important, anything around a decade less than 1kHz is fine.

Paste a circuit diagram of the current amplifier created in LTSpice as per the above design calculations here. Provide the simulated test results: **10**



Ideally, provide a zoomed in view of the actual amplifier circuit (the FG is standard circuit)



5 marks for correct LTSpice circuit design

Simulations:

Use the FG simulation done earlier to provide V_{in} to your amplifier circuit. This will be a frequency $f \sim 1.17kHz$ so it should sail through the 100Hz high-pass cutoff frequency of your amplifier.

Specify V_{in} to have a pk-pk signal of 1V, centered around 0V. i.e. V_{in} should swing between +0.5V and –0.5V. Measure current delivered to the load R_L both as a current probe in LTSpice, and the voltage across R_L which you will measure in the circuit demo

Try a few higher values of V_{in} pk-pk: 1.5V, 2V, 2.5V. Do you observe a trend? Is there a reason for the circuit's (mis)behavior?

Put your simulation output plots here:

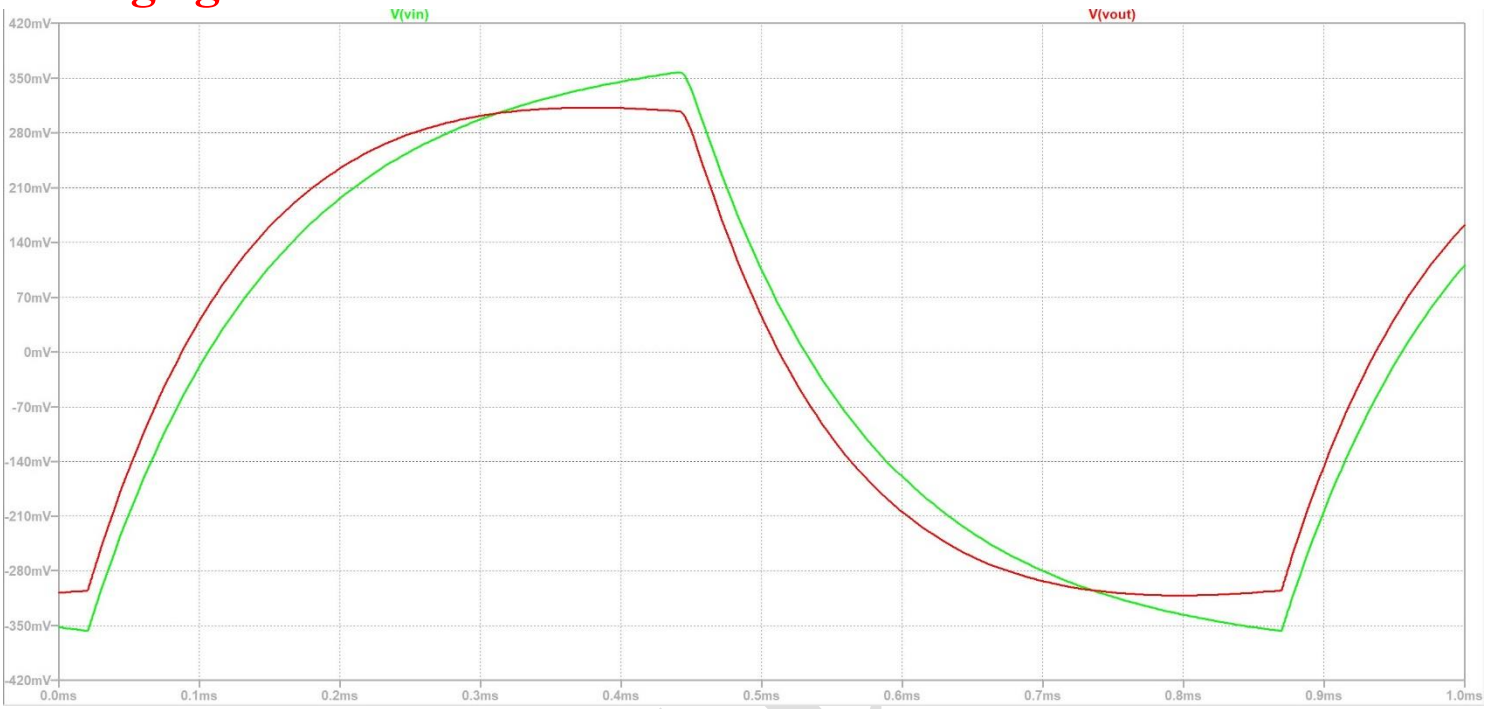
Note on solution and pk-pk values of V_{in} to be tried. Full marks if you checked with just the specified pk-pk V_{in} values (i.e. Set 100k voltage divider RL1,RL2 to get V_{in} = ±0.5V, ± 0.75V, ±1V, ±1.25V

However, it is interesting to see what happens when you get up to higher amplitudes of V_{in}: our FG can deliver up to close to ±3V even if $100k\Omega || R_{inp} < 100k\Omega$

Some sample plots given here:

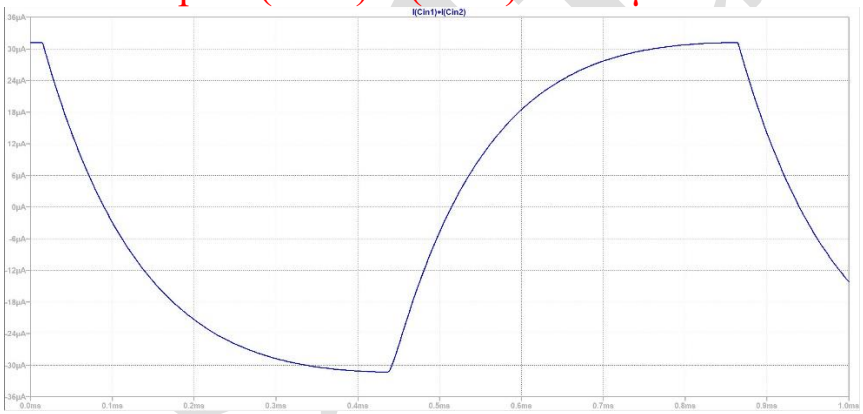
V_{in} = 1V pk-pk (±0.5V) RL1 = 65K, RL2 = 35k (loading by R_{inp} reduces V_{in} from expected $\frac{RL_1}{RL_1+RL_2}(\pm 3V)$ so you will have to tweak RL1&RL2 to get the desired V_{in} for testing your circuit simulation

Voltage gain:

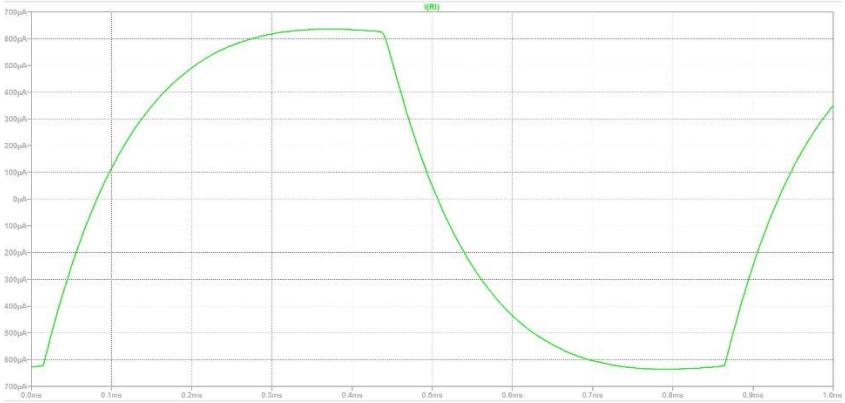


Current gain: $\mathcal{O}(10)$ expected (why?)

Current input I(Cin1)+I(Cin2) = ±30µA



Current output $I(R_L)$ = ±700µA → Actual gain = 700/30 = 23.33



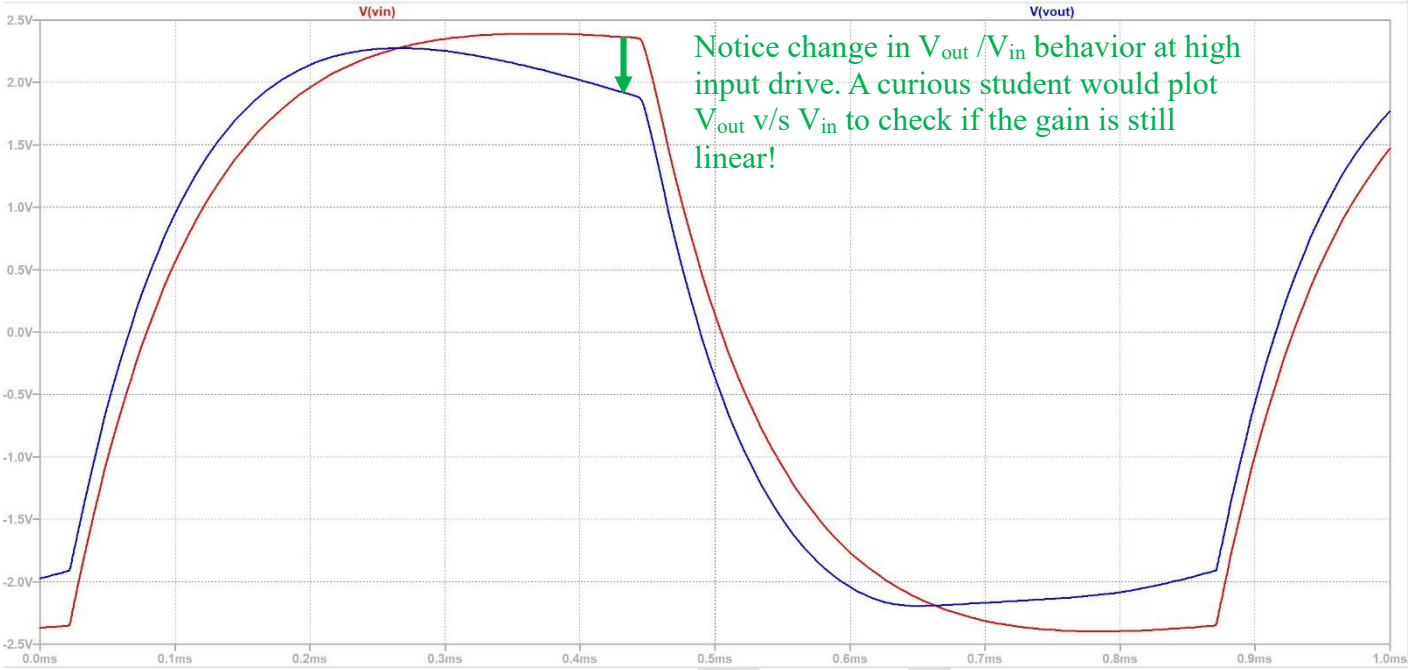
Notice that voltage amplification is in phase, but current amplification is phase reversed… why?
Possible explanation: During the positive half cycle of input, AC current direction in reality should be from Vin to base. But the LTSpice compiler assumes opposite direction. Compiler assumes load

current from Vout to Gnd as positive. Hence we see this phase difference in current amplification.

At the high end,

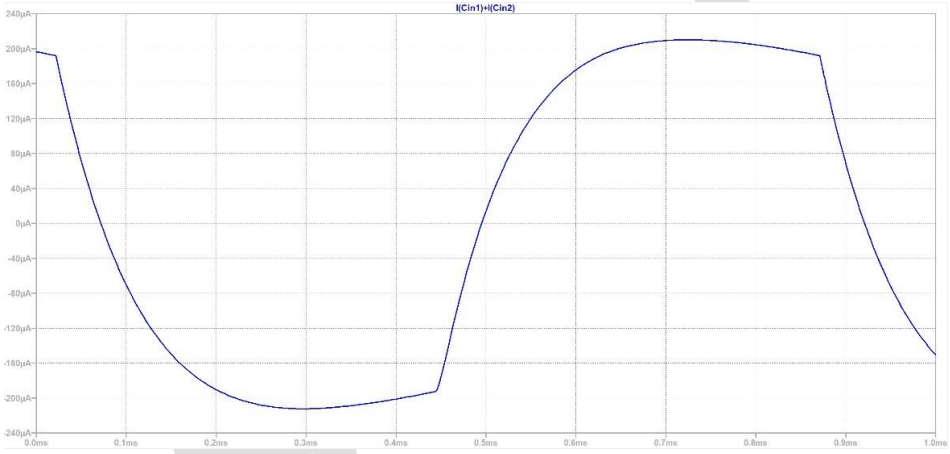
Setting RL1=0 and RL2=100kΩ we can drive V_{in} to close to ±3V

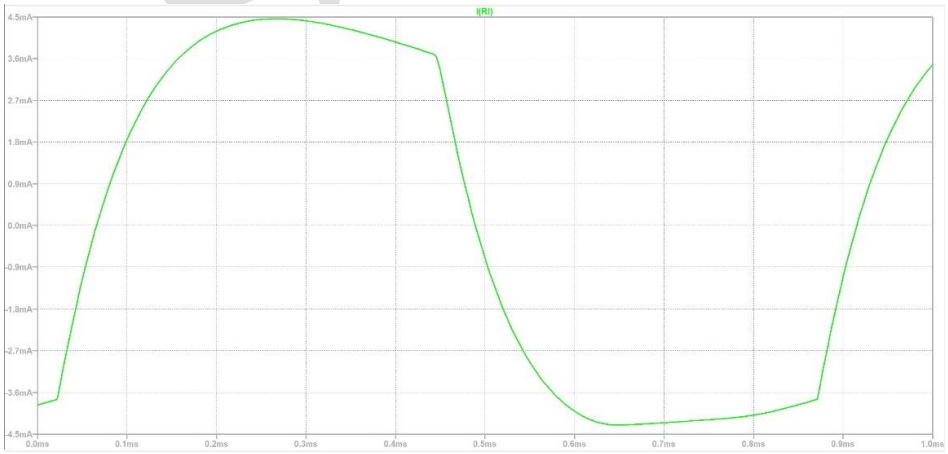
Voltage Gain with V_{in} swing to ± 2.5V



Current Gain:

Current input I(Cin1)+I(Cin2) = ±200μA, Current output $I(R_L)$ = ±4.5mA





→ Conclusion: we need to drive V_{in} to ~ ± 2.5V to get higher peak AC power delivery to R_L !

What is the amplitude of V_{in} required to drive peak power 5mW ($\delta I = 3.16mA$) into R_L?

Turns out we need V_{in} around $\pm 1.7V$ to drive peak power 5mW into R_L:

Power output can be directly plotted using the expression V(vout)*I(RL):