Lab 1: Design, simulate and analyze NPN transistor based oscillator

IMPORTANT UPDATES TO THIS Function Generator (FG) Model added in later labs:

Lab 2: RC, CR filter stages added to convert square wave output into smoothly varying sawtooth waveform

Transistors used in the FG slamming between saturation and cutoff cause significant purturbations in Vcc supply itself:
FIX: Apply a 100uF electrolytic bypass capacitor between Vcc - GND for this FG module, and every other active module built later in the semester: Emitter follower (Lab 3), CE voltage amplifier (Lab 4) + Endsemester exam

This FG can comfortably drive ~ O(50-100k) load without attenuation. Though some subtle effects have to fine tuned in Lab 3+4

4. In case of discrepancies in your measurements of 3.a, have a clear idea of what component values could be the cause of discrepancies. Figure out some ideas to get around potential problems caused by 3.b

Questions are given in the following pages. Put your answers in the space provided below each question. Be careful to adjust pagination while inserting circuit diagrams exported from LTSpice.

Edit the header above to insert your Rollnumber and Name.
Solution must be submitted on Moodle as a PDF file. Use 'File→Export'

Question 1: Design a circuit using two NPN transistors that produces a square wave output 0-9V, frequency 1kHz and 50% duty cycle

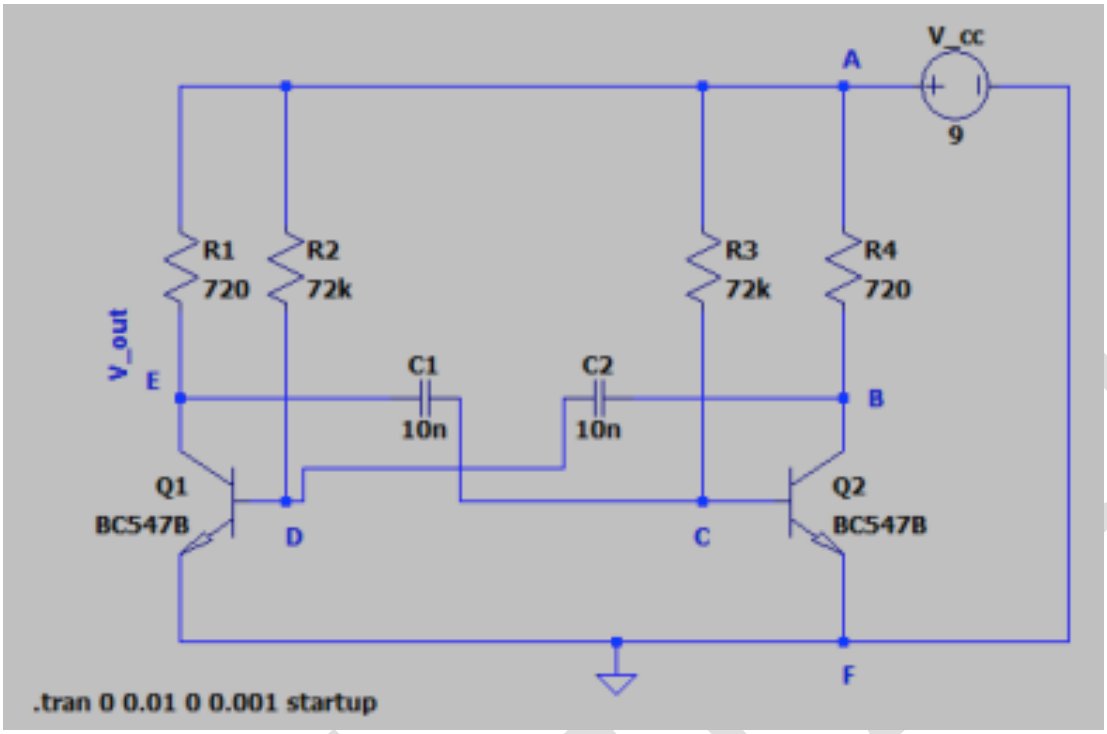
10

Your circuit design must obey the following design constraints:

1. It must use two NPN BJT's. You can assume initially that the BJT's are identical and use the ideal circuit model in LTSpice for the BJT BC547B
2. Work with a supply voltage V_{CC} = 9V and consume minimal current (few mA)
3. Use R, C as the only passive components.
4. The R values must set the BJT operating points. In conjunction with C, the circuit must produce the desired output voltage square waveform
5. Minimize the number of *different* values of R, C required – you may assume that each R and C is ideal

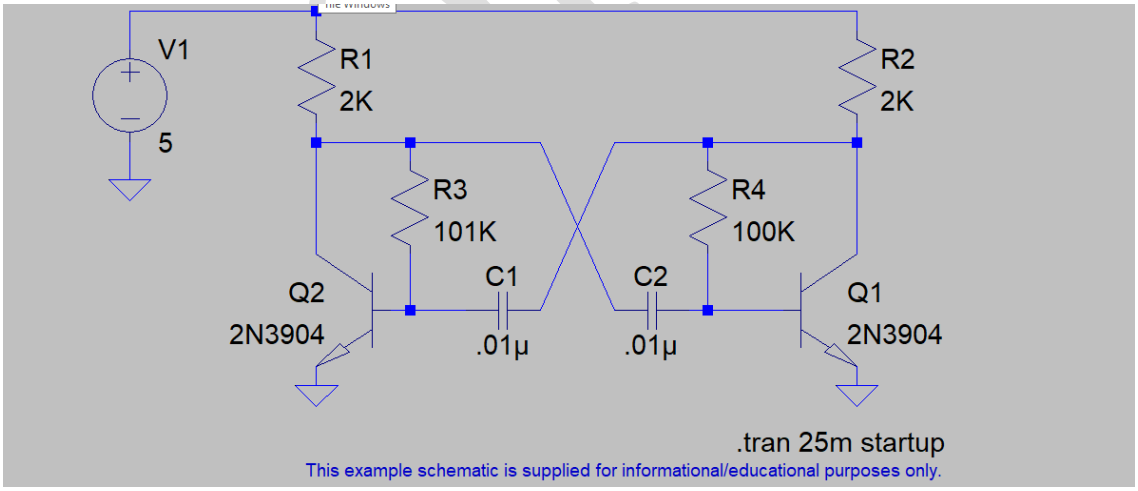
Space for Answer 1 (use 'Insert → picture' to insert your circuit design here)

10 marks for Standard circuit diagram, with typical component values (H.S)



Note: R_c ~ kΩ range is OK, because minimize power dissipation is specified.
Many students chose ≪ 1kΩ with correspondingly different C values, be lenient and don't cut marks – that's a separate trade-off issue between minimizing power dissipation and matching high load R_L to be discussed in post-lab wrap-up

Alternate diagram: 8 marks



Such a diagram is probably taken directly from the LTSpice examples directory! It is actually not straightforward to cross wires at 45° between C1 and C2 for a first-time user.

Question 2: What values to check after building the circuit? **20**

You have made a clever circuit design in Answer 1 – now suppose you build it on your breadboard using the actual transistors, resistors, capacitors and some wire. After turning on V_{cc} what, and where are the values of DC voltages you should check on your circuit as built, to ensure that all the connections are made properly and the circuit should be working?

Note that the designed circuit is expected to start oscillating when powered up – so ideally, there should be no stable DC voltages in the circuit! Yet, we usually build circuits a few components at a time. After the first few components are connected and V_{cc} is turned on, the circuit should demonstrate stable DC voltages at certain nodes. What are these nodes and what are values of their DC voltages?
Make a list of the voltages to be checked here:

Space for Answer 2:

20 marks:

C1 and C2 must be disconnected (physically) only then .op in LTSpice and DMM measurement on breadboard will give DC voltages at BJT terminals indicating bias on BJT terminals as below

BEST NODE VOLTAGE specification example (H.S)

1) The first step is to connect a voltage source of 9V, along with the 2 npn transistors, and the 4 resistances as given above with appropriate grounding. To check correctness of the circuit we first make sure that (Q1 fig for reference) –
   a) Node A gives 9V DC
   b) Node F is grounded and is showing 0V
   c) There is a voltage drop from 9V at nodes B,C,D,E (due to the resistances). B and E should be around 0.1V.
   d) C and D should show V<0.8V, indicating the two transistors are on (around 0.7V, the forward bias voltage in the saturation region).
   e) For an additional check, we can measure the base currents at both transistors (I_b) and make sure they are in the 100 μA range
2) The next step is to connect the 2 capacitors of values around 10 nF. After powering the circuit, only A (at 9V DC) and F (at 0V DC) will be the constant DC voltages, other nodes will have oscillatory solutions.
3) Checking these DC voltages in the 2 discrete steps guarantees the correctness of the circuit. We can also optimize the checking by just finding the voltages in D and E in steps (1c-1e), since the circuit is symmetrical. However to be thorough, all the nodes should be checked.

15 marks:

If circuit is fully connected including C1, C2, there should NOT be any DC voltages at any of the terminals! Except trivially V_{CC} fixed at 9V unless there is a dead short circuit and 9V battery drains to 0V

Question 3: What voltage waveform do you expect at the circuit output?

You are given a Digital Storage Oscilloscope (DSO) that allows you to probe the time-dependent voltage waveforms at various points in your circuit.

3.a) The DSO probe has effectively infinite impedance (like the LTSpice simulation "software probe") – what waveform do you expect to observe at the output of the circuit?

Insert a picture of your expected square wave output waveform here: **10**

Answer 3.a

1kHz nearly square waveform output of LTSpice simulation. Swings 0 to 9V

3.b) Suppose your oscillator circuit's output is sent to another circuit whose input is purely resistive. What waveform do you expect to observe at your oscillator's output if it is connected to ground through such a resistor load R_L?

3.b.1) Insert a picture of your expected circuit output when the output is connected to a load resistance R_L=1kΩ or 10kΩ **10**

7 marks – trivial addition to LTSpice circuit and re-run simulation

R_L = 1kΩ : If R_C was taken ~ 1kΩ, R_L loads circuit being in parallel with R_C and V_{out} drops by approximately half to ~ 5V (value depends on chosen value of R_C)
R_L = 10kΩ If R_C was in ~ 1kΩ range, R_L ~ 10*R_S will minimize loading and V_{out} amplitude should be only slightly smaller than 9V

3 marks – thought put into the answer:
Adding R_L which goes effectively in parallel with R_C changes the RC time constant of the circuit, hence expect the frequency and duty cycle of V_{out} to change

3.b.2) Think of ideas that reduce the effect of "loading" on your circuit output voltage, and think further about any *other* problems those ideas may cause on the design specifications.

(trade-off between source and load characteristics) **20**

Set $R_L \gg R_C$ so that $R_C \,||\, R_L \sim R_C$ and characteristics of the circuit are protected from load. 20 marks

Additional comment if student displays deeper understanding – (should have put extra marks for this!)
Setting R_L may not always be possible. Load specification is not part of the circuit design: usually we design the circuit to be as safe as possible from any loading, hence safest thing to do if driving a voltage output would be to put a high impedance voltage buffer at the output (to be treated in PH233 with opamps

Question 4: Unexpected, non-ideal measurements

Even with the effectively infinite input impedance of the DSO probe, suppose you measure the output of your circuit to be not a perfect square wave

a) The frequency of the output is not exactly 1kHz as expected.
b) The rise/fall times of each square pulse is rather large, i.e. the square pulse looks like it has 'rounded' edges
c) In extreme case, the rising edge may be so shallow that your output, instead of being a square waveform actually looks more like a 'saw-tooth' waveform.

Evaluate the effect of various components in your circuit design and determine which component is the likely culprit for each of the above deviations from expected results. Can it be?

1. Values of C, R used in the built circuit are different than expected due to component tolerances/component degradation over time/or mismatched?
2. The transistors are not exactly identical to each other.
3. Some important aspect of circuit operation was overlooked while calculating component values?

Remember that it could be a combination of factors, for a combination of deviations! Is there any factor that is the dominant cause of error?

You can use `.STEP` feature of LTSpice to vary component values and investigate their effect on the circuit output to get a rough idea. Then determine a quantitative expression which relates (say) a 5% difference in the value of R to measured output characteristics etc.

Give a summary of your circuit analysis and understanding here: **50**

Question is somewhat ill-framed – it asks student to give verbal description of circuit's operation. Whereas what we really wanted was a quantitative analysis of changes in component values by ~ 5% on the output performance. All components in the hardware kit are specified as 5% tolerance so there is bound to be variation by that much from the design value

45 marks: student describes sequence of Q1 and Q2 switching between saturation and cut-off as C1, C2 alternately charge/discharge

5 marks: (since not explicitly asked above :–(
Example of a thorough analysis: (H.S)

The DC Voltage determines the amplitude of the output. The frequency is determined by (R3C1) and (R2C2), and these must be equal for a 50% duty cycle. The sharpness of the pulse is determined by (R1C1 and R4C2).

Derivation -

Time period of wave depends only upon the discharge of capacitors C1 and C2. Initially, when C1 is fully charged, and C2 dischages.

$V(c) = V_{cc} - R3I_{R3}$

Also, since the capacitor C1 charged up to VCC, the initial discharge current will be -

$IR3 = (V_{cc} + V_{cc})/R3.$

Current will decay exponentially with a time constant of R3C1, hence -

$V(c) = V_{cc} - 2\ V_{cc}\ e^{-t/(R3C1)}$

The transistor will switch when V(c) will become the forward bias voltage, which is negligibly small compared to V_{cc}, and hence is approximated to 0, which helps us evaluate T1 (the on time for transistor Q1)

$2\ e^{-t/(R3C1)} = 1$

$T1 = R3C1\ln(2)$

Similarly, the on time for transistor Q2 is $T2 = R2C2\ln(2)$

Thus total time period $T = T1+T2 = R3C1\ln(2)+ R2C2\ln(2)$

In our specific case of R2 = R3 = R and C1 = C2 = C, this reduces to $T = 1.4RC$ and hence the frequency of oscillation is given by $f = 1/T = 0.7/RC$

From this, we can see that $\Delta R/R = \Delta T/T$, hence changing R by 5%, also changes the time period by 5%, and frequency of the wave also by 5% (increasing R decreases f and vice versa).

Question 5: (Advanced, BONUS questions)

1) What are the circuit modifications required to change the duty cycle of the waveform to less than or more than 50%? **20**

- **a.** How does the waveform performance change (with reference to non-idealities analyzed in question 4) as you change the parameters? It appears to be a large parameter space, but upon understanding the circuit's behavior you may find that only a few parameters really decide both the duty cycle and the waveform rise/fall times
- **b.** As an example, give circuit component values required for a 25% and 75% duty cycle waveform of 1kHz

Hardly anyone attempted these bonus questions, and among them the answers varied quite a bit (no unique answer possible really for such bonus 'open' questions now and in future labs.

For example, for 5.1.b we have specifically asked for 25% & 75% duty cycle variation. However, simply changing component values will compromise other aspects of the design, so alternative circuit designs may be better.

Hence 20 + 30 marks given to students who put in substantial answers to Question 5

2) It is, in principle, with a quick internet search, possible to make an oscillator circuit with a single BJT circuit. Analyze that circuit and determine what are its drawbacks. Why did we steer you away from a deceptively simpler single BJT oscillator?? **30**

This is a super advanced concept – it was a 'just fishing' question. Single transistor oscillators are prone to break out into unwanted oscillation. For example, if a BJT is biased close to the edge of FA, V_{BE} just barely above threshold, pick of stray EM field from the environment (eg cellphone radiation) can cause it to break out into ~ GHz uncontrolled oscillations..

---------- **End of Lab 1**