Lab 1: Design, simulate and analyze NPN transistor based oscillator

Objective: At the end of this lab assignment, you will:

1. Have a well-designed, ready to build square wave voltage waveform generator using two NPN transistors and a few selected R, C values
2. You will know what DC voltage values you must check after building the circuit to ensure that your circuit is correctly built and working
3. Know what to expect when you measure the square wave output of the oscillator with load set to:
    a. Infinity (open circuit direct probe)
    b. Terminated by a finite load resistor R_L
4. In case of discrepancies in your measurements of 3.a, have a clear idea of what component values could be the cause of discrepancies. Figure out some ideas to get around potential problems caused by 3.b

Questions are given in the following pages. Put your answers in the space provided below each question. Be careful to adjust pagination while inserting circuit diagrams exported from LTSpice.

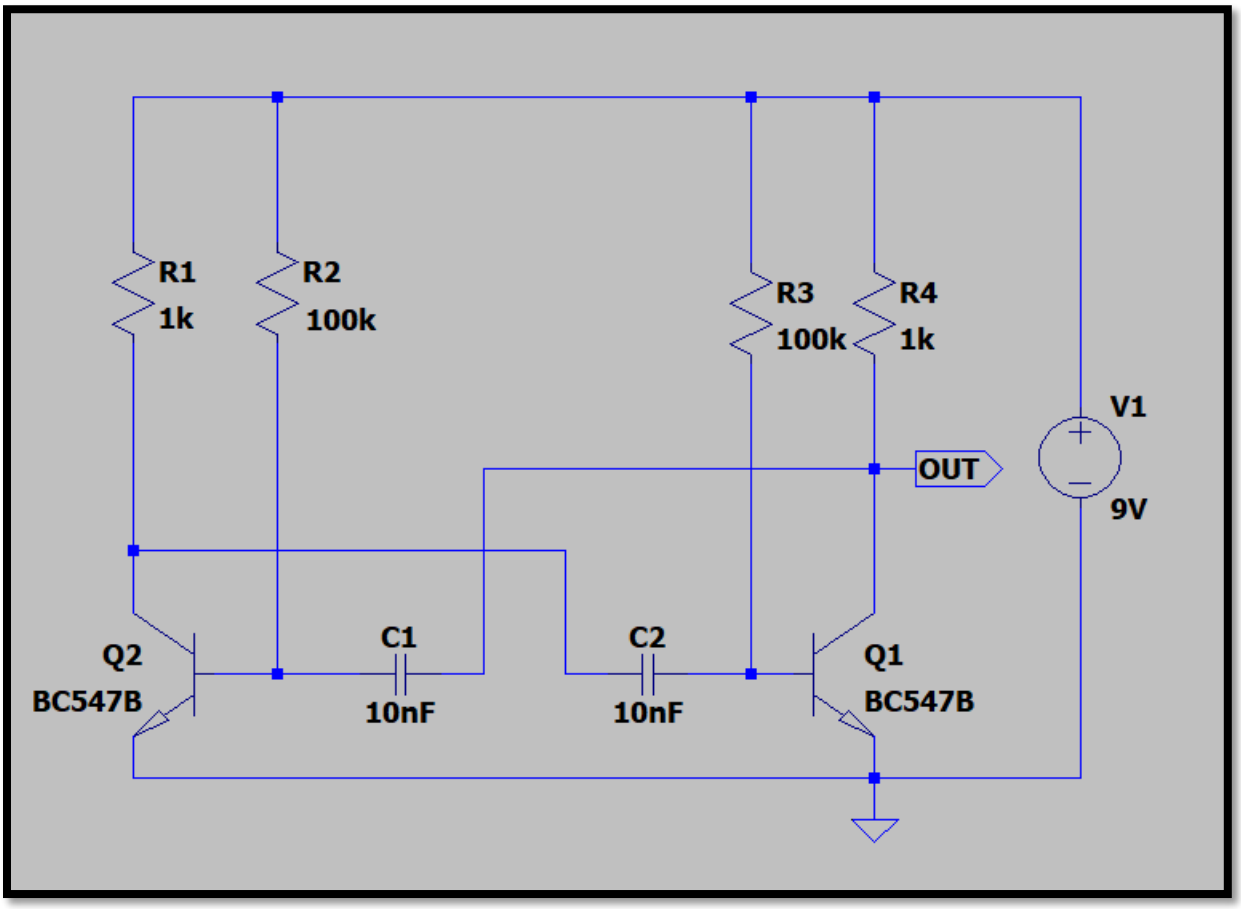
Edit the header above to insert your Rollnumber and Name.
Solution must be submitted on Moodle as a PDF file. Use 'File→Export'

Question 1: Design a circuit using two NPN transistors that produces a square wave output 0-9V, frequency 1kHz and 50% duty cycle **10**

Your circuit design must obey the following design constraints:

1. It must use two NPN BJT's. You can assume initially that the BJT's are identical and use the ideal circuit model in LTSpice for the BJT BC547B
2. Work with a supply voltage V_{CC} = 9V and consume minimal current (few mA)
3. Use R, C as the only passive components.
4. The R values must set the BJT operating points. In conjunction with C, the circuit must produce the desired output voltage square waveform
5. Minimize the number of *different* values of R, C required – you may assume that each R and C is ideal

Space for Answer 1 (use 'Insert → picture' to insert your circuit design here)



Question 2: What values to check after building the circuit? **20**

You have made a clever circuit design in Answer 1 – now suppose you build it on your breadboard using the actual transistors, resistors, capacitors and some wire. After turning on V_{cc} what, and where are the values of DC voltages you should check on your circuit as built, to ensure that all the connections are made properly and the circuit should be working?

Note that the designed circuit is expected to start oscillating when powered up – so ideally, there should be no stable DC voltages in the circuit! Yet, we usually build circuits a few components at a time. After the first few components are connected and V_{cc} is turned on, the circuit should demonstrate stable DC voltages at certain nodes. What are these nodes and what are values of their DC voltages?

Make a list of the voltages to be checked here:

Space for Answer 2:

We can check for DC voltages at the nodes before connecting the capacitors. When the transistor is on, the base will be at 0.7V. This will also happen to be the voltage at one end of R2/R3.

The other end of R2/R3 is connected to the source, i.e. 9V. Therefore, the potential difference across the resistor R2/R3 will be 9-0.7 = 8.3V.

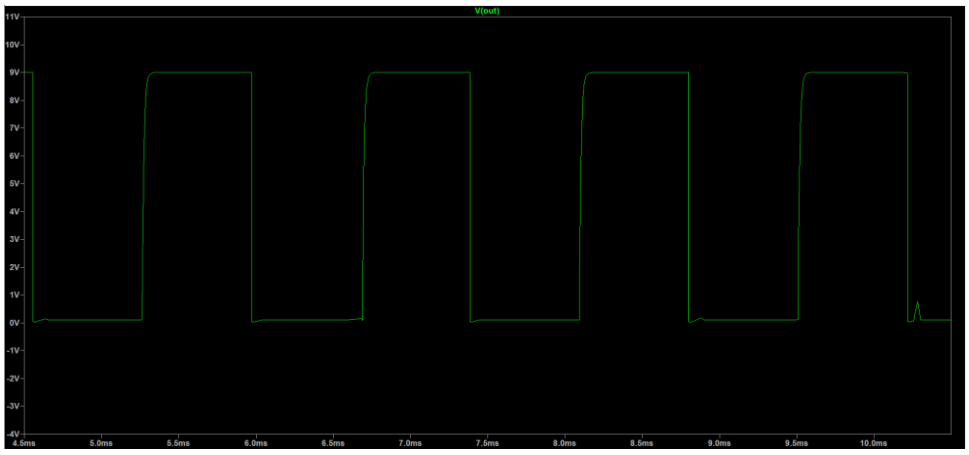
Question 3: What voltage waveform do you expect at the circuit output?

You are given a Digital Storage Oscilloscope (DSO) that allows you to probe the time-dependent voltage waveforms at various points in your circuit.

3.a) The DSO probe has effectively infinite impedance (like the LTSpice simulation "software probe") – what waveform do you expect to observe at the output of the circuit?

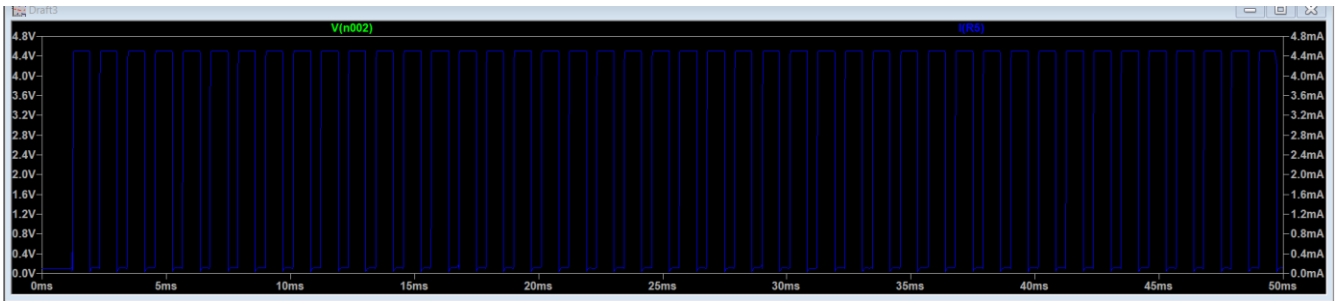
Insert a picture of your expected square wave output waveform here: **10**

Answer 3.a



3.b) Suppose your oscillator circuit's output is sent to another circuit whose input is purely resistive. What waveform do you expect to observe at your oscillator's output if it is connected to ground through such a resistor load R_L?

3.b.1) Insert a picture of your expected circuit output when the output is connected to a load resistance R_L=1kΩ or 10kΩ **10**



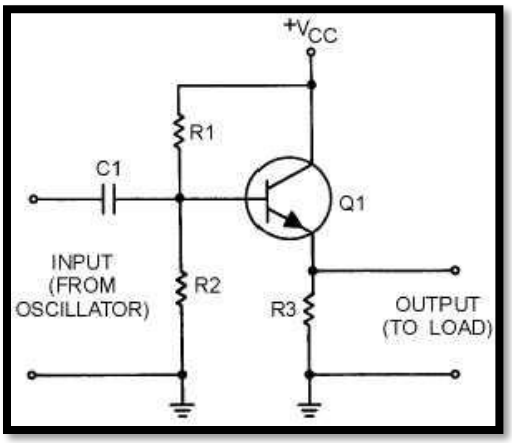
(Load used: 1kΩ)

3.b.2) Think of ideas that reduce the effect of "loading" on your circuit output voltage, and think further about any *other* problems those ideas may cause on the design specifications.

(trade-off between source and load characteristics) **20**

In general, a **buffer amplifier** should be used in between the output and the load resistance in order to reduce the effect of loading. In other words, the aim is to ensure that the load resistance is greater than the source resistance so as to avoid a large voltage drop in the supply circuit.

A buffer amplifier has a high input impedance and a low output impedance. Since the output of an oscillator is connected to the high impedance of the amplifier, the buffer has little effect on the operation of the oscillator. The output of the buffer is then connected to an external load; therefore, the changes in the output load cannot reflect back to the oscillator circuit. Thus, the buffer amplifier reduces interaction between the load and the oscillator.



A buffer amplifier

Question 4: Unexpected, non-ideal measurements

Even with the effectively infinite input impedance of the DSO probe, suppose you measure the output of your circuit to be not a perfect square wave

a) The frequency of the output is not exactly 1kHz as expected.
b) The rise/fall times of each square pulse is rather large, i.e. the square pulse looks like it has 'rounded' edges
c) In extreme case, the rising edge may be so shallow that your output, instead of being a square waveform actually looks more like a 'saw-tooth' waveform.

Evaluate the effect of various components in your circuit design and determine which component is the likely culprit for each of the above deviations from expected results. Can it be?

1. Values of C, R used in the built circuit are different than expected due to component tolerances/component degradation over time/or mismatched?
2. The transistors are not exactly identical to each other.
3. Some important aspect of circuit operation was overlooked while calculating component values?

Remember that it could be a combination of factors, for a combination of deviations!
Is there any factor that is the dominant cause of error?

You can use `.STEP` feature of LTSpice to vary component values and investigate their effect on the circuit output to get a rough idea. Then determine a quantitative expression which relates (say) a 5% difference in the value of R to measured output characteristics etc.

Give a summary of your circuit analysis and understanding here: **50**

(component labeling in accordance with circuit figure of question 1)

Assuming transistor, Q1 has just switched off (cut-off) and its collector voltage is rising towards Vcc, meanwhile transistor Q2 has just turned on. One side of capacitor C2 is also rising towards the 9V supply rail of Vcc as it is connected to the collector of Q1 which is now cut-off. Since Q1 is in cut-off, it conducts no current so there is no volt drop across

load resistor R4. The other side of the capacitor, C2, is connected to the base terminal of transistor Q2 and at 0.7V because transistor Q2 is conducting (saturation). Since Q2 is fully-on, capacitor C1 starts to charge up through resistor R3 towards Vcc. When the voltage across capacitor C1 rises to more than 0.7v, it biases transistor Q1 into saturation.

The instant that transistor, Q1 switches on, the side of the capacitor C2 which was originally at Vcc potential, immediately falls to 0.7 volts. This rapid fall of voltage causes an equal and instantaneous fall in voltage on the other side of the capacitor, therefore that side of C2 is pulled down to -5.3v and this negative voltage swing is applied the base of Q2 turning it off. This gives one unstable state.

Transistor Q2 is driven into cut-off so capacitor C2 now begins to charge in the opposite direction via resistor R2 which is also connected to the 9V supply rail, Vcc. Thus the base of transistor TR_2 is now moving upwards in a positive direction towards Vcc with a time constant equal to the C2 x R2 combination. However, it never reaches the value of Vcc because as soon as it gets to 0.7 volts positive, Q2 turns fully on into saturation. This action starts the whole process over again but now with capacitor C1 taking the base of transistor Q1 to -5.3v while charging up via resistor R3 and entering the second unstable state.

Thus, we can see that the circuit alternates between one unstable state in which transistor Q1 is off and transistor Q2 is on, and a second unstable in which Q1 is on and Q2 is off at a rate determined by the RC values. This process will repeat itself over and over again as long as the supply voltage is present.

The periodic time of the oscillator is given by:

$T = t_1 + t_2$,

Where $t_1 = 0.69*C_1*R_3$ and $t_2 = 0.69*C_2*R_2$

Question 5: (Advanced, BONUS questions)

1) What are the circuit modifications required to change the duty cycle of the waveform to less than or more than 50%? **20**

- **a.** How does the waveform performance change (with reference to non-idealities analyzed in question 4) as you change the parameters? It appears to be a large parameter space, but upon understanding the circuit's behavior you may find that only a few parameters really decide both the duty cycle and the waveform rise/fall times
- **b.** As an example, give circuit component values required for a 25% and 75% duty cycle waveform of 1kHz

2) It is, in principle, with a quick internet search, possible to make an oscillator circuit with a single BJT circuit. Analyze that circuit and determine what are its drawbacks. Why did we steer you away from a deceptively simpler single BJT oscillator?? **30**

It is possible to make an oscillator circuit with a single BJT. One such oscillator is the Hartley Oscillator. It basically works on the principle of the oscillating natures of LC circuits.

There are 2 major drawbacks of this Oscillator:

1. The harmonic content in the output is very large and hence, cannot be used in places where a pure sine wave is desired as output.
2. It cannot be used as a low frequency oscillator since the value and size of the inductors becomes quite large.

---------- End of Lab 1