

## **Lab 4: BJT as a Voltage Amplifier: Common Emitter Mode**

### **Part 2: the Demo**

#### **Prerequisite:**

You must have a working simulation and physical implementation of a waveform Function Generator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.

You must have solved Part 1 of this lab assignment – design of a BJT in Common Emitter mode as a voltage amplifier of Gain =  $-10$  and other design specifications as per Part 1. A working LTSpice simulation of the full circuit will be used in matching your measurements of the built-up circuit to the ones predicted from LTSpice.

The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

#### **Grand goal: Part 2**

Demonstrate a working circuit of a BJT configured as a voltage amplifier.

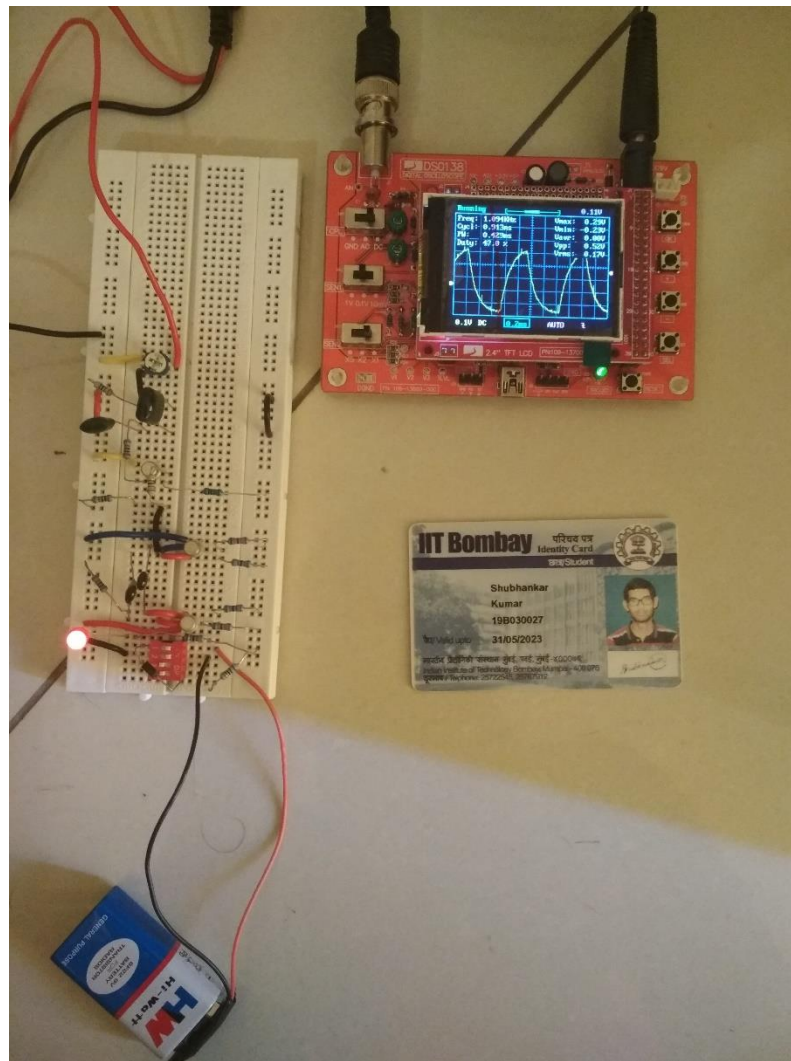
Input provided must be  $\pm 0.3\text{V}$  @  $f=1.17\text{kHz}$ . With the design specification of Gain =  $-10$ , we expect to see an output voltage swing of  $\mp 3\text{V}$  (negative sign is implicit in the design!)

To help you demonstrate your circuit building expertise and earn piece-wise marks, we have split up the circuit demo into separate parts

### **Level 0: Function generator (FG) is it still working?) 10**

Demonstrate that the FG built earlier and used several times in the past labs is still working! Include a photo of your built-up FG with **no load** connected at the output except the DSO probes. Set the output potentiometer to produce a sawtooth waveform of  $\pm 0.3\text{V}$  @  $f \sim 1.17\text{kHz}$

This will be your input for subsequent testing, so we make sure that FG is functioning correctly.



## Level 1: Voltage amplifier circuit build Sanity check 10

From LTSpice simulation of circuit as designed in Part 1, you should have a clear prediction of the node voltages at various points in your amplifier circuit with no  $v_{in}$  applied.

Build your amplifier with 1 BJT. Keep the FG disconnected completely from  $V_{CC}$  (since that seems to cause issues with  $V_{CC}$  fluctuation as the  $Q_i$  in the FG itself slam back and forth from saturation to cutoff). Also don't connect the output of the FG to the input of your amplifier yet.

Using a DMM, check the DC voltages at various nodes in your circuit:  $V_{CC}$ , and the BJT terminals C,B,E. Match the measured values to your expectations from design calculations and LTSpice simulation and list them here

This will give you confidence that your BJT voltage amplifier circuit is built correctly and BJT is biased into forward-active mode

$$V_C = 4.4V$$

$$V_B = 0.90V$$

$$V_E = 0.24V$$

## Level 2: Voltage amplifier working with $v_{in} = 0.3V$ 20

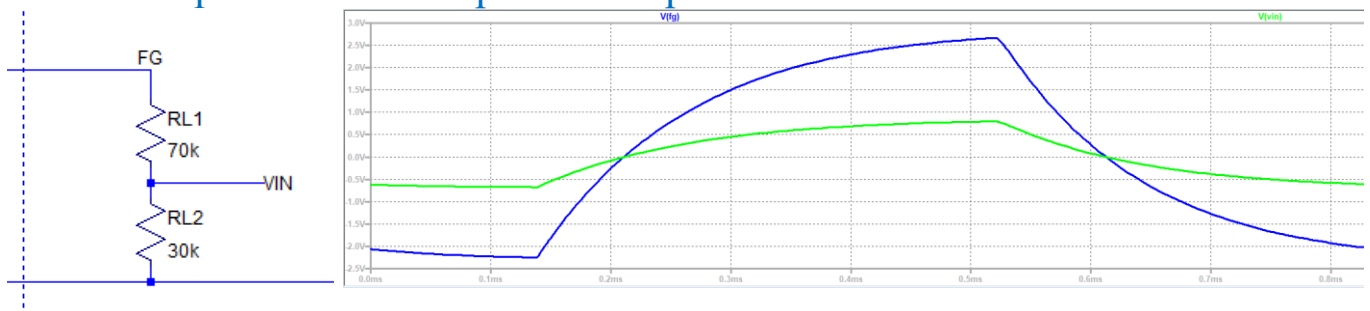
Connect the full end-to-end circuit together: FG  $\rightarrow$  RC-CR shaper  $\rightarrow$  newly built BJT voltage amplifier as per the full LTSpice simulation design of Lab 4, Part 1

Turn power ON and double check the power indicator light, that  $V_{CC}$  is indeed reaching your breadboard!

Now your FG *should* be putting out a  $\pm 0.3V$  sawtooth voltage waveform (checked in Level 0) and the newly built BJT common-emitter voltage amplifier should be ready to amplify that voltage (checked in Level 1)

Proceed to test the combination by connect output of your FG to  $v_{in}$  of your BJT amplifier. Answer the following questions by performing the hardware checks sequentially – this will help you characterize and understand the built circuit.

**2.1)** Does the input impedance  $R_{inp}$  of your BJT amplifier cause loading on your FG output, pulling down  $v_{in}$  amplitude? For example, V(FG) driving a 100k potentiometer load should be putting out a  $\pm 2.5V$  output. A 30k:70k split of the potentiometer should give you  $\pm 0.75V$  as  $v_{in}$  to your newly built BJT amplifier circuit as per the LTSpice simulation:



After connecting output of your FG to  $v_{in}$  of your BJT amplifier with a 30:70 split ratio of your potentiometer, do you in fact get  $\pm 0.75V$  swing of  $v_{in}$ ?

Explain quantitatively why not?

No, the output is not  $\pm 0.75V$ . This is due to the fact that the input impedance causes loading on the FG output.

The loading causes a drop in voltage.

## 2.1.A) Amplifier input $R_{in}$ loads the FG output. Explain how? 4

Use equations, calculate the effective impedance loading the FG. There is the resistor divider in the  $100\text{k}\Omega$  potentiometer and  $R_{in}$  of the amplifier to be taken into account!

$$R_{in} \text{ of Amplifier} = 1/(1/R_1 + 1/R_2 + 1/\beta \cdot r_e) = 3.3\text{k}\Omega$$

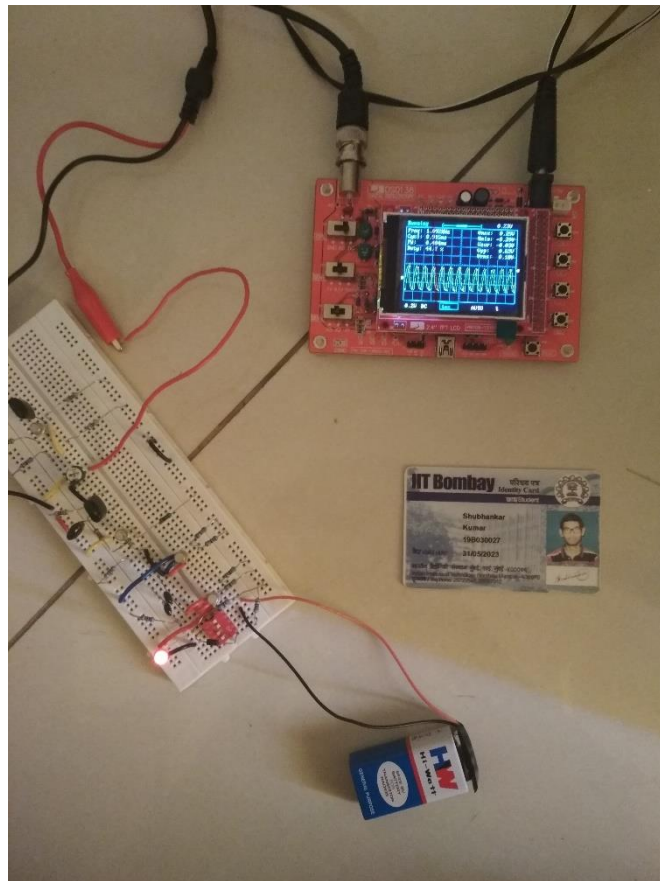
$$\text{Effective impedance} = 1/(1/R_{in} + 1/70\text{k} + 1/30\text{k}) = 2.8\text{ k}\Omega$$

## 2.1.B) INPUT DEMO 5

Instead of re-designing and re-building the whole circuit (big headache when you are likely within a few hours of the submission deadline!), simply adjust the potentiometer setting – you should be able to find some ratio of  $RL1:RL2$  that gets you

$$v_{in} \sim \pm 0.3\text{V at } f \sim 1\text{kHz}$$

Put a photo of your setup here with DSO measurement of  $v_{in}$



What is the value of  $RL1:RL2$  you ended up using to get  $\pm 0.3v_{in}$  swing? Does it match your calculation of Part 2.1.A? **1 mk bonus**

$$RL1:RL2 = 89k\Omega : 11k\Omega$$

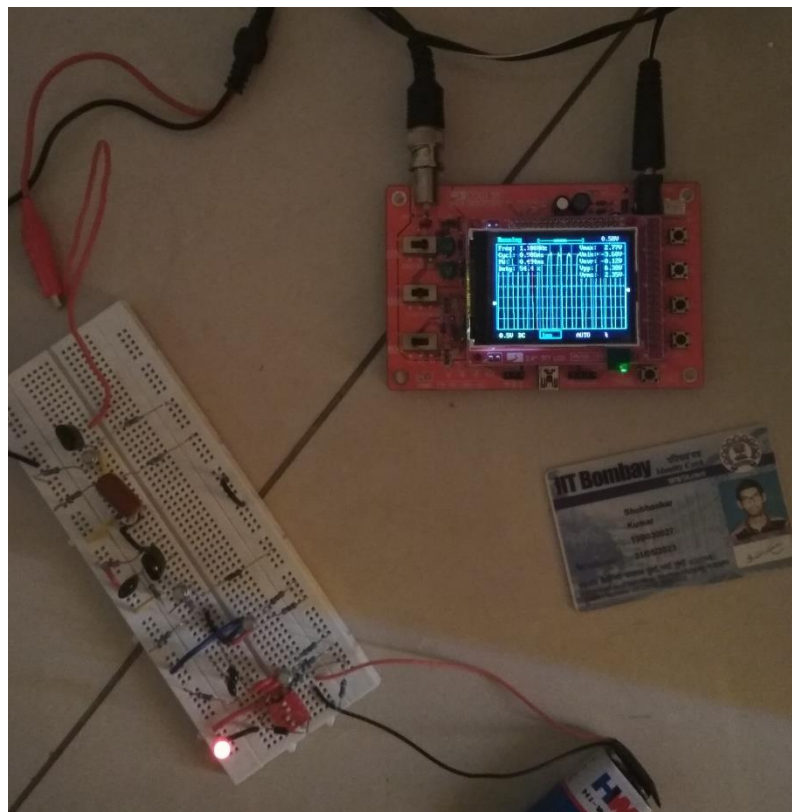
Note that it is incorrect to measure these resistors *while they are connected in the circuit*. You will have to apply some skill to take the potentiometer out of the circuit. Safest is to plug it into another blank area of your breadboard and use little probe wires to measure the resistor divider values. Of course, don't forget to put it back correctly in the circuit without changing the value!

This is a general principle of practical electronics – if you try to measure values of components like resistors with a DMM while they are connected in the circuit, you will end up measuring the value in parallel with all the other nearby (and sometimes far away) circuit nodes. You may find out later in life that this makes it very difficult to debug fully assembled complex PCB's with many components of which one or two may have malfunctioned.

## 2.1.C) OUTPUT DEMO

**10**

Probe  $v_{out}$  of your amplifier circuit. With effectively infinite impedance of your DSO probe, you should get close to the simulated voltage gain from  $v_{in} = \pm 0.3V$ . Put a photo of your circuit (with ID) and a DSO measurement of  $v_{out}$  highlighting the measured amplitude of  $v_{out}$  and hence the measured voltage gain





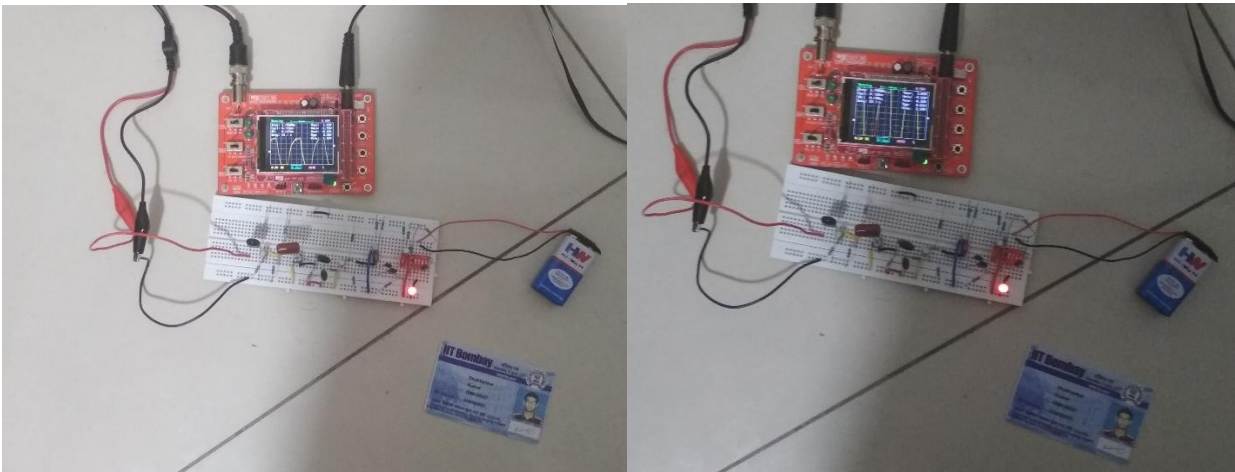
## Level 3: Explore limits of voltage amplification 10

With  $v_{in} = \pm 0.3V$  swing, you can see that the amplification is (mostly) linear and fixed except for some artifacts near the extremes. Thus the amplifier is able to amplify any  $v_{in}$  in the range  $0 - \pm 0.3V$

Increase  $v_{in}$  to higher values by adjusting the potentiometer of the FG. Put a photo of your measurements here when you see deviation from linear gain. Make a note of what is the value of  $v_{in}$  swing when  $v_{out}$  does not show a smooth amplified sawtooth waveform, but flattened edges near the extremities. Is the flattening present at both positive and negative extremities of  $v_{out}$ ? 5

Provide quantitative explanation of why you see a deviation from linear gain 5

When the value of  $v_{in}$  crossed approx.  $0.8V$ ,  $v_{out}$  didn't show a smooth amplified sawtooth waveform. As the potentiometer is being adjusted, first the flattening happens at the negative extremity and then gradually the positive extremity also gets flattened.



Reason: For a linear amplification to occur, we need the BJT to be in forward active mode. If the potentiometer value is disturbed from its optimum range (which gives forward active mode), then it causes the transistor to go either into saturation/cutoff.

We know that  $V_B = V_{CC} \cdot R_2 / (R_1 + R_2)$ . Changing the input voltage subsequently results in change of the voltage at the base junction, i.e.  $V_B$ . Thus,  $V_{BE}$  and  $V_{CB}$  change accordingly. This results in the possibility of the BJT going into cutoff/saturation.