Lab 4: BJT as a Voltage Amplifier: Common Emitter mode

Prerequisite:

You must have a working simulation and physical implementation of a waveform **F**unction **G**enerator that swings to both positive and negative voltages, as worked out in Lab 1 + 2. We call this the FG for short throughout the rest of this lab.
The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.
Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

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Stop time = 101m
Time to start saving data = 100m
Maximum time step = 0.01m
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This skips the initial transients in the first 10ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ $f \sim 1kHz$

Grand goal:

Design a BJT based circuit that is able to amplify a small AC input voltage to a large output Voltage. Current requirements are not very precisely defined, but the output must be able to function as a reasonably good AC voltage source (we will test in the end, how good is "reasonably" good)
By now, you must be familiar with the terms DC voltages and currents (constant in time, with capitals V,I); AC voltages and currents (v, i) and the concept of "sourcing" v/s "sinking" current at a circuit node.

Part 1) Circuit Design and Simulation [50]

Fig 1 shows the basic structure of a voltage amplifier circuit. In principle, since $I_c = \beta I_B \rightarrow V_{out} = V_{CC} - I_c R_C$ this is all you need to crack this lab assignment!
or… is it? NO! Some important extra components are needed to put Q1 operating mode as in earlier Lab, AND ensure non-linear effects at B-E junction are suppressed as given in the pre-lab reading notes.

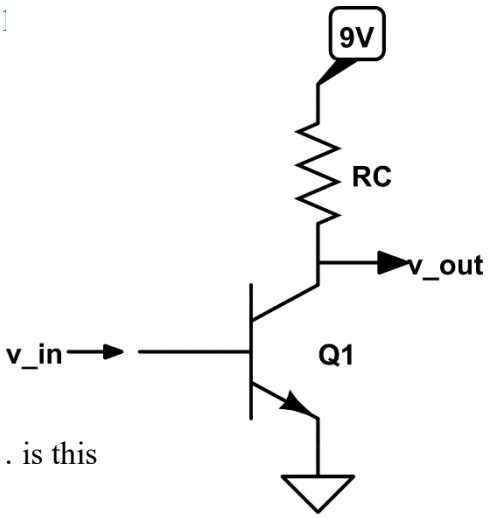

Fig 1:
The BJT voltage amplifier… is this all there is to it?

Level 0: The "crack"

If v_{in} is an AC voltage whose value can be both positive and negative,

0.1 What are the assumed conditions required for $i_c = \beta i_b$?
What are the necessary absolute and relative voltage conditions required at the C, B, E terminals of Q1 to use it as a voltage amplifier? **1**

a) BJT must be in forward active mode
b) $V_{BE} = V_B - V_E = 0.7V$ and $V_{CB} = V_C - V_B > 0V$

0.2 Input side: Our input signal is a voltage v_{in}, NOT i_{in}. Is it OK to send v_{in} directly into the base of Q1? Obviously not! List all the reasons why not: **1**

We wish to get the Q point current. Hence, an impedance needs to be added accordingly so that a DC Voltage is set up as a transistor bias.

Level 1: Basic Design

After cracking the problem concepts in Level 0, and with experience from previous circuit design, you should already have a rough idea how to proceed:

The design parameters we wish to achieve in this lab are:

1. Assume $V_{CC} = 9V$ constant, and Q1 $\beta = 300$
2. Use I_Q _____ = 1mA
3. Circuit gain _____ = **–10** (note '–' due to overall design)
4. Amplifier has a high-pass f_{3dB} _____ = 100 Hz
5. Test amplifier with $v_{in} = \pm 0.3V$ @ 1.17 kHz (our standard FG output)

Here is the step-by-step design procedure:
BJT terminal voltages must be setup such that it always remains in the forward-active operation mode. Here are ways in which this can be accomplished, without too much complexity:

DC Design:

1) Choice of $I_Q = 1mA$
Note that we have chosen I_Q much lower than the Q point of the emitter

follower current amplifier – we are mostly interested here in voltage amplification and not too bothered about delivering large current to the load. In the first approximation, we don't deliver *any* current to the DSO probe load. So a choice of low I_Q is OK as long as we can ensure the BJT remains forward-active at all times.

2) **Calculation of R_C** – we would like to allow v_{out} to have maximum possible range from 0 – V_{CC}. So, we would like to set V_C at about ½ V_{CC}. Fixing V_C and I_Q immediately determines R_C. What value of R_C do you choose? **1**

R_c = (4.5V)/(1mA) = 4500 Ω

3) **What should V_E be, if it is to be?** Is it OK to connect Q1-E terminal directly to GND as shown in Fig 1? Why not?

Hints:

1) There is an effective r_e across B-E whose value is very small, and non-linear, dependent on temperature and I_C: you don't want the Q-point of the circuit (or its overall operation) to be dependent on a small non-linear r_e

2) V_{BE} is ~ 0.7V in forward active mode. So V_E should be at least of comparable value at the Q-point to ensure thermal stability.

Explain what is the Q-point value of V_E required, and what is the component value required at E? [listed in pre-reading notes] **3**

No, we cannot connect Q1-E terminal directly to GND in order to avoid the transistor going into saturation or cutoff. Another reason is to avoid the non-linear effect of r_e, i.e. to avoid the increase in its resistance value cause by thermal heating.

We set $V_{EQ} = 0.1V_{cc}$. Hence in this case, V_E = 0.9V.

Finer points of choosing V_{EQ}: **2**

Setting V_E to be $0.1V_{CC}$ directly, you will find that you don't get to gain G= – 10 in step 5 below. So you can come back here to re-do the V_{EQ} setting to lower than $0.1V_{CC}$ (while still having $\frac{V_E}{I_E}$ dominate over r_e) – Design is an iterative process!

$V_{EQ} = 0.05V_{CC}$

4) Setting V_B: Once DC values of V_C and V_E are decided in steps above, choose the simplest method of setting V_B (similar considerations as used in earlier current amplifier lab apply, to make sure the biasing network provides a much lower impedance path to ground than R_B.

List the values of components used to set V_B here: **2**

$R_{B1} = 51k\Omega$ and $R_{B2} = 7.5k\Omega$

$V_B = V_{CC}R_{B2}/(R_{B1}+R_{B2})$

5) What AC voltage gain do you get?

Combining the answers to questions 2 & 3 gives you the AC voltage gain of the amplifier. Note: Though we are technically in the DC design phase, we are looking ahead and interested in the AC voltage gain. So turn all the capital letter quantities $V_{...}$, I… into small case and do a little bit of math with the AC terms $v_{in}=v_B$, $v_C=v_{out}$, i_C, i_E, i_B.

The main steps involve using the fact that

$v_{out} = v_C = -i_C R_C$ (V_{CC} is DC value drops out) &

$r_e \ll R_E$ by design

$v_B = v_E$ since $V_{BE} = 0.7V$ is fixed by the DC design.

You may find, surprisingly, that β is not involved in the final voltage gain of this circuit!

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$V_{out}/V_{in} = -R_C/(r_e+R_E)$

Now, $r_e = 25mV/I_Q = 25\Omega$

Therefore, $V_{out}/V_{in} = -4700/(495) = -9.5$

AC Design:

1) Input side: In general $V_{in} = V_{in|dc} + v_{in}$. We want to strictly reject $V_{in|dc}$ hence the 100Hz f_{3dB} high pass filter at the input is required. Calculate the value of the required component. The calculation is similar to the way we used R_{inp} of the amplifier as part of the CR high-pass filter in earlier lab **1**

Rin = 742 Ω

$C = 1/(2\pi f R_{in}) = 3.3\mu F$ (approx.)

2) Output side: $V_{out} = V_{CC} - I_C R_C$ we are interested in only amplifying the AC component of $I_C = I_Q + i_C$ In fact, we want to *block* any DC share of the current flowing through R_C getting diverted to the load – this will disturb our DC calculations above!
Calculate the filter components required at the output before connecting to v_{out} What is the corresponding R required for this filter calculation? Recall from the reading notes that looking back Q1's C, the CB junction is effectively open circuit (MΩ) and there is only one other resistor at that junction!

1

R_load = 75kΩ
C = 100nF

Go back and check: you may now realize that as long as you keep Q1 in forward-active mode, some I_Q and hence a DC $I_B = I_Q/\beta$ is required. Since I_Q has been set very low, corresponding DC I_B must be really small indeed! This means you must obey the constraint $(R_{B1}||R_{B2}) \ll R_B$ much more strictly to make sure most of the DC current in the biasing path is preferentially sent into the biasing network and *not* into the base of Q1. Re-check your answers to question 4) in the DC design above for the biasing network to set V_B to make sure your design is self-consistent in terms of all the DC values and the design gain G is achieved.

1

Level 3: Advanced Design check 2

Is the gain constant over the full span of $v_{in} = \pm 0.3V$?

We have designed for a gain of G= –10 at the Q-point. But as v_{in} varies i_C varies around I_{CQ} *and hence* r_e *also changes.* Have you chosen your component values conservatively enough that for the given design parameters, $G = -10$ is constant?

Yes, the gain is constant over the full span of $v_{in} = \pm 0.3V$.

Level 4: Simulate in LTSpice and plot 30

Simulate the complete circuit as designed above in LTSpice and check its performance as per the design parameters
(v_{in} = ±0.3V, f=1.17kHz, Gain = –10)
Put your LTSpice circuit diagram and simulation result plots below.
Make sure to plot voltages as a function of time (as you will check them after building the circuit). Also, plot voltages v_{out} v/s v_{in} to check the Gain linearity and any peculiar features.