Lab 3: BJT as a current source: Emitter Follower

Part 2: Circuit demo and analysis [60 + 20 bonus]

Prerequisite:

Completed Part 1 of this lab.
Full circuit design of FG + BJT configured as an emitter follower current amplifier. In case you are unsure of your design's correctness the model solution containing the full circuit design is posted on moodle – you can use that as a basis for your circuit building and demo.

Grand goal:

Demonstrate a working BJT current amplifier and measure its current gain.

Level 2.A: Circuit Demo 30

Build the circuit as designed and simulated in Level 1.
Use the FG as per standard design built earlier to provide V_{in} to your amplifier circuit..
Before connecting V_{in} and poking around with the DSO, follow the usual debugging steps: check DC voltage values at each significant node of the circuit to make sure they match the simulation and your circuit is wired up correctly. It's a good idea to explicitly write them down, since variations caused by component value tolerances may affect performance.
Connect V_{in} and probe the voltage across R_L. Provide photos of your full setup with ID card in the frame as usual.
Dividing by R_L allows you to re-calibrate the measured waveform V_{RL} into a current R_L

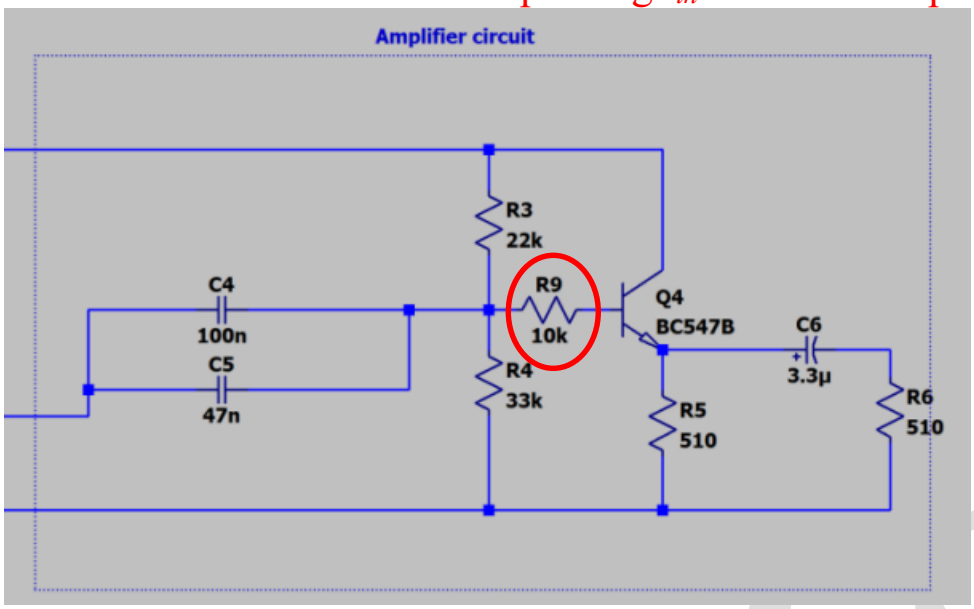
+15 marks: photo of fully connected breadboard, with DSO measurement and ID card

Based on your measurements, determine the current gain $\frac{I_L}{I_{in}}$ actually achieved in your circuit. Is it symmetrical for both polarities of V_{in}?

[+15 marks: Current gain: note that we are interested in the AC current gain]
+5 marks: Output current i_L → simply V_L scaled by R_L gives the peak current delivered to the load
+10 marks: you actually have to be rather clever to measure the input current i_{in} ! In LTSpice it was easy to plot $I(C_{in1})+I(C_{in2})$ as i_{in} In the real circuit, we usually need to put a small series resistor across two nodes and measure voltage drop across the resistor as a current probe. It's a like our Diode I/V characterization from back in Lab 2. But we have to be careful

that the black probe of the DSO is permanently at GND, so wherever we plug that in, should not affect the circuit operation

Here is one clever method of probing i_{in} in the built-up circuit: [Anish Bapat]:



Where are the red-blk crocodile clips connected? V(R9)/R9 gives i_B and V(R4) should provide a fixed DC offset

Level 2.B: Power analysis 30

For the following analysis, it is adequate to consider the peak power consumption. RMS power formulae are applied for sinusoidal waveforms, but our test waveform is *not* a sinusoid. So you may simply take V*I products at the peak values.

1) DC power consumption at idle. Disconnect V_{in} and V_{out}: Now your amplifier is ON and idling at DC. It is ready to amplify current, but there is no input to be amplified.

Measure the power consumed by the amplifier circuit from V_{CC} in idle condition at the Q-point

Find a clever method to do this without disturbing the circuit operation

Ammeter in series with V_{CC} to R_{B1} **5**

~ 50 mW

2) AC power consumption during amplification. Now apply a bipolar V_{in} input as earlier, and again measure the peak power consumed from V_{CC} (a suitable modification of the method used in 1.a) might be useful)

Keep the power consumed by the FG circuit and the load R_L as separate quantities. Power consumed by the FG can be measured independently and subtracted, *before* connecting it to the amplifier to get AC power measurement

during amplification. Power delivered to the load is measured separately below.

What is the power consumed by the amplifier circuit itself during AC operation? **10**

1Ω resistor in series at the central ground point will not disturb the circuit operation. V across this resistor would give $V^2/1\Omega$ power

As per the precise question phrasing, R_L should also be disconnected, or equivalently $I_L^2 R_L$ should be subtracted in stating the AC power consumption of the amplifier circuit.

Now due to addition of emitter follower and FG hanging from V_{CC} (even if the emitter follower is not driving anything) power consumed from V_{CC} into the two modules should increase. But it is noticed that due to V_{CC} itself misbehaving (falling) at the peaks when Q_i in the FG switch, the AC power consumption without load drive is about the same or slightly less ~ 47mW

3) What is the power delivered to the load? (re-verify the Level 2 result) Accordingly what is the ratio of power delivered to the load to the power consumed within the amplifier circuit itself?

5

Pk-to-pk voltage observed across final R_L is ~ 0.4V → a horrible, miserable 0.32W power delivery at the cost of ~ 50mW consumed by the circuit itself!

4) Provide a detailed analysis of why the current amplifier is unable to deliver the peak power specification to R_L.

> Did you go wrong somewhere in the step-by-step calculations?

> Was some operation assumption violated?

> Is there a fundamental limitation to this circuit design that will never let it the desired peak power delivery specification?

10

1) The single NPN emitter follower can only *source* current to the output (emitter cannot sink current). We have biased at a super high I_{CQ} (hence high power dissipation) to be able to source arbitrary amount of current to load. This is called 'Class A' operation.

So in principle, we should be getting only unipolar output to R_L . The bipolar output is provided by the output coupling capacitor C_{out} : in one half cycle, C_{out} sources current to load, and in the other half cycle, C_{out} provides a current path back from R_L to

GND. We are actually providing and taking back power from R_L in each half cycle and the net positive balance is marginal.

2) A full solution (Level 3 bonus design below) would use a complementary PNP transistor based emitter follower module below the NPN transistor – that has the complementary ability to actively *sink* current but not supply current.

Level 3: Optimize design to reduce power consumption 20 [Advanced bonus question]

3.1 Provide a rough circuit idea along the lines of Fig 1, to solve the main problem with power dissipation in amplifier v/s poor efficiency in delivering power to the load **5**

3.2 Fill out your circuit idea of (3.1) as a full-fledged LTSpice simulation. Use the same design parameters as Level 1. **5**
Insert your circuit design image and the LTSpice simulation results here.

3.3 Build a working circuit as per your full design of (3.2) and demonstrate that it achieves close to the desired power delivery to the load **10**
As usual, provide a photo of your working circuit with your ID card and the measured DSO waveforms highlighting what is better about your Level 3 design