PH231 Endsemester exam.B – Spring 2021 [60]

Prerequisite:

You must have a working LTSpice simulation and physical implementation of a waveform **F**unction **G**enerator (FG) that swings to both positive and negative voltages, as used in previous labs.
The official standardized design is published on moodle – use those component values to get a reliable output and test that your FG works as expected.

Add a 100µF (electrolytic) capacitor from V_{CC} to GND for the FG, and for the all other active modules involving BJT's, both in simulation and the built circuit. As discussed in lecture session, this prevents V_{CC} fluctuations caused by FG BJT's switching

Settings for LTSpice: Use the following timing parameters in LTSpice simulation command

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Stop time = 101m
Time to start saving data = 100m
Maximum time step = 0.01m
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This skips the initial transients in the first 100ms of simulation caused by calculation artefacts, capacitive charging etc and gives you a stable picture of one full cycle of V_{in} @ *f~ 1kHz*

Check and reduce dependence of voltage gain of a CE amplifier on load impedance

Level 0 10

Check how badly the load impedance affects voltage gain of the CE amplifier (to be done with LTSpice simulation of CE voltage amplifier)

1. What is the output resistance of the high gain CE voltage amplifier as designed and built in Endsem.A (also Lab 4)? **1**

   Note: at this level we are mostly interested in the 'resistive' output impedance.
   Though there is an output coupling capacitor, all our operational tests are done at a frequency 1 kHz ~ 10× f_{3dB} high-pass cutoff, so for practical purposes that coupling capacitor may be considered a short-circuit

   The output resistance will simply be R_C, i.e. 4.7kΩ.

2. So far, we have been probing the output v_{out} directly with the DSO probe (red+black crocodile clips) – what is the impedance of this probe? **1**

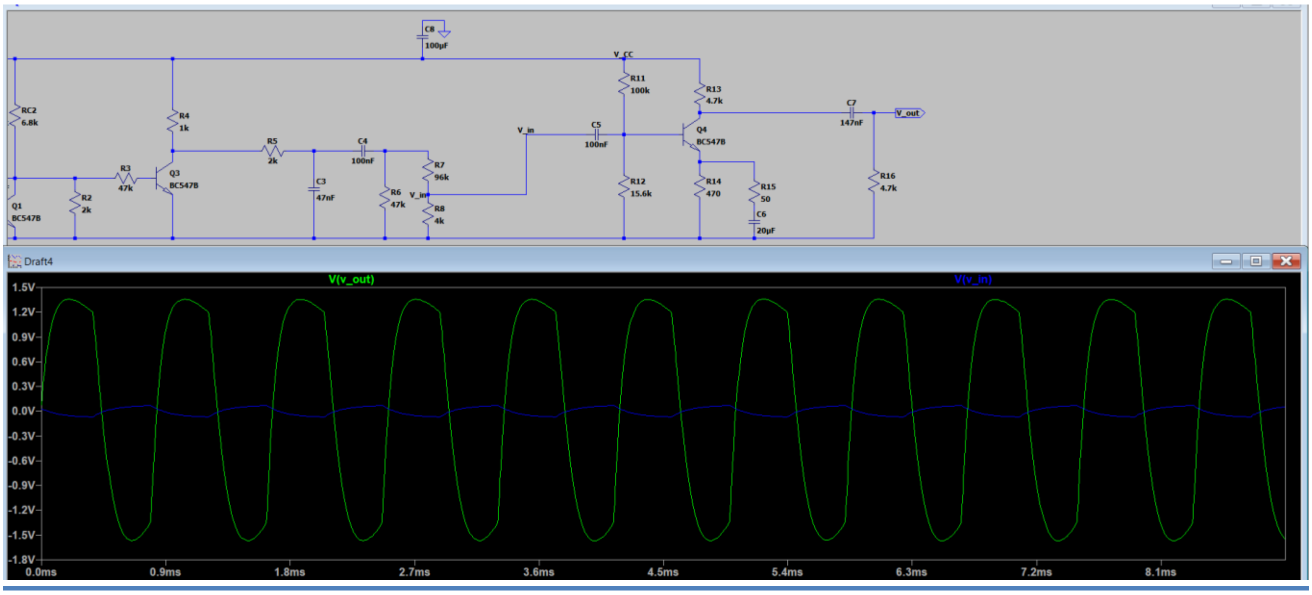
   The impedance is considered to be infinite.

3. If a finite load resistance R_L is connected to v_{out} do you expect the amplitude of v_{out} to be affected? If so, why and how much? **1**

   Yes, the amplitude of v_{out} will change as $v_{out}/v_{in} = -(R_C||R_L)/(r_e + R_E||R_{E1})$

4. Implement a finite $R_L = 4.7k\Omega$ between v_{out} and GND in your simulation to check if your calculation for question 3 is correct. **1**

Put photos of your simulation output with a finite $R_L = 4.7k\Omega$ here:



5. **CONCEPT CRACK:** From the above questions 1 – 4, it should be clear that the CE voltage amplifier really doesn't like to drive small load impedance. We would like to send this $v_{out} = G \times v_{in}$ into a node which always has a high input impedance, so that the amplitude of v_{out} is preserved.

a. What other circuits have you studied in the lab that have (a) high input impedance (b) preserve the voltage amplitude? **1**

Common Collector Amplifier (Emitter follower)

b. Can such a circuit (as solved earlier in the semester) be directly plugged in at v_{out} of the high gain voltage amplifier? Obviously not. Why not? **1**

No, because it will overload the amplifier.

c. What specific parameters of the desired circuit module must be re-done so that we can use it at v_{out} of the high gain voltage amplifier to provide the desired high load impedance? **4**

We add a coupling capacitor so that each transistor is separately biased and blocks the DC operating bias level of one stage from affecting the DC operating point of the next.

$C_{new} = 1/(2\pi f R_C)$

$C_{new} = 330nF$

Level 1 Fine-tune design of a high-impedance (active) load circuit so that it 'buffers' v_{out} of the voltage amplifier **15**

Solving questions 1 – **5** of Level 0, you have cracked the idea of the circuit module required to be connected at the output v_{out} such that the (high) input impedance of that circuit does not affect the amplitude of v_{out} –
we will call it a 'buffer circuit' in this assignment.

We have solved such a buffer circuit design earlier in the semester, though we called it by some other name then. The design parameters & constraints were different. Now that you are a beginner-expert in electronics, go back and re-write the design parameters of that circuit such that it is suitable for use in this context.

1. List the design parameters that are in your control, and features of the design of the earlier used circuit which you now need to re-do to be able use it today as a high input impedance buffer circuit **3**

We have,
1. $V_E = 0.5V_{CC}$
2. Beta = 300
3. $R_E = V_E/I_E$

2. Re-design the buffer circuit as per the above design requirements so that it can be applied as a high impedance buffer circuit after the CE voltage amplifier. Give all your calculation steps here: **6**

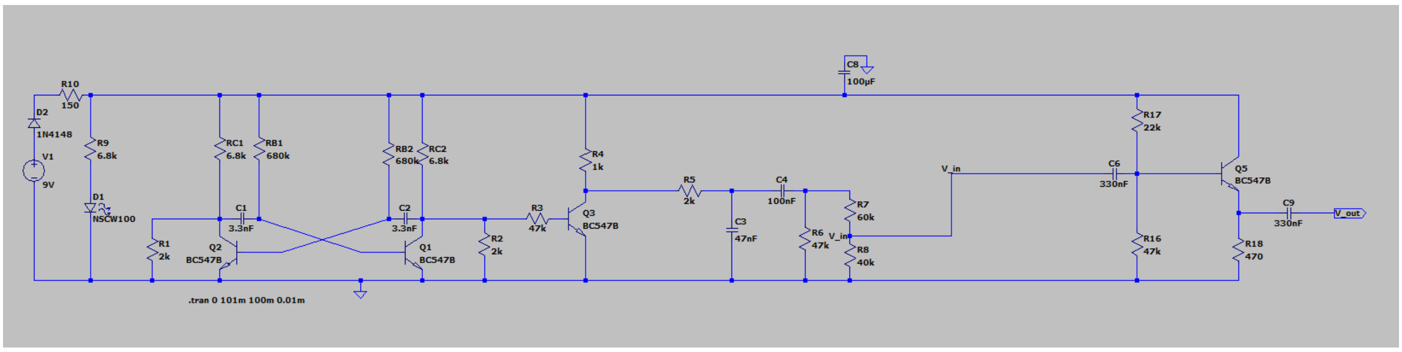
Taking $I_{CQ} = 10mA$, we design an emitter follower as done in Lab 3
Since $I_E \sim I_C$, $I_E = 10mA$. Therefore, $R_E = 470\Omega$.
Now, $R_B = \beta(r_e + R_E) = 148.5k\Omega$.
We now choose R_{B1} and R_{B2} such that $R_{B1} \,||\, R_{B2} << R_B$. Hence. $22k\Omega$ and $47k\Omega$ satisfy the given condition.

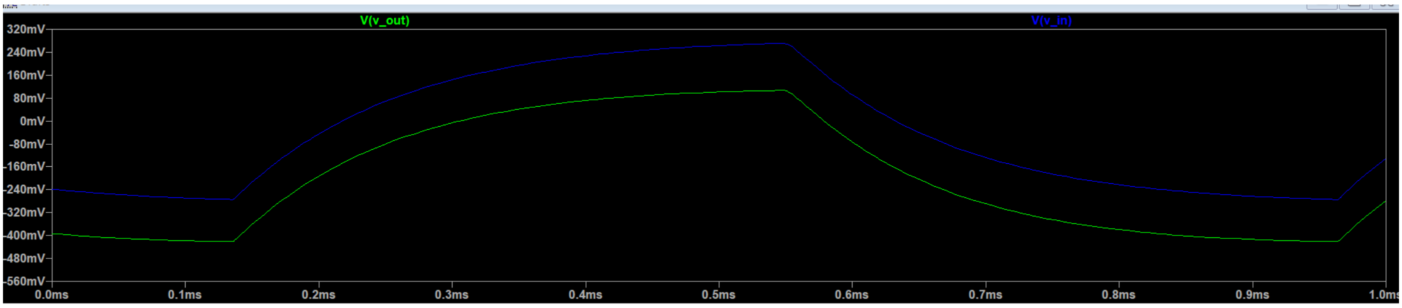
3. Put your LTSpice simulation circuit diagram and results for the buffer circuit here. **6**

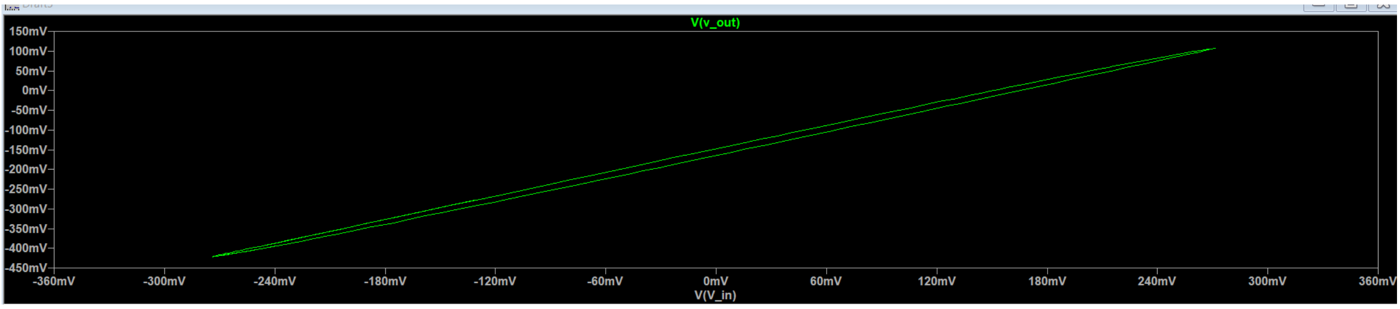
For this question just include the cracked and designed buffer circuit, driven by the FG (don't include the CE voltage amplifier of Endsem.A)
Label the nodes sensibly where you are measuring *I, V*
Result plots expected:

a. v_{in} *v/s* i_{in} (shows R_{inp} of your buffer, hope it is constant and high!) Measure the slope and record your simulated R_{inp} – does it match the value calculated for Question 2 above?

b. $v_{out}(t)$ and $v_{in}(t)$ → to be compared with experiment.







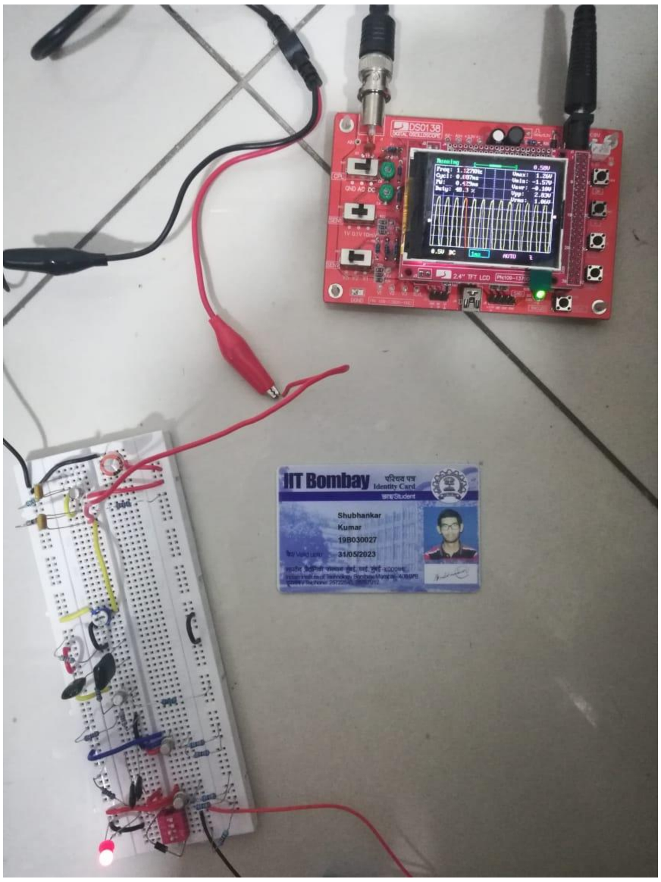
Level 2 Buffer circuit demo and grand end-to-end assembly demo

Level 2.A buffer circuit demo 20

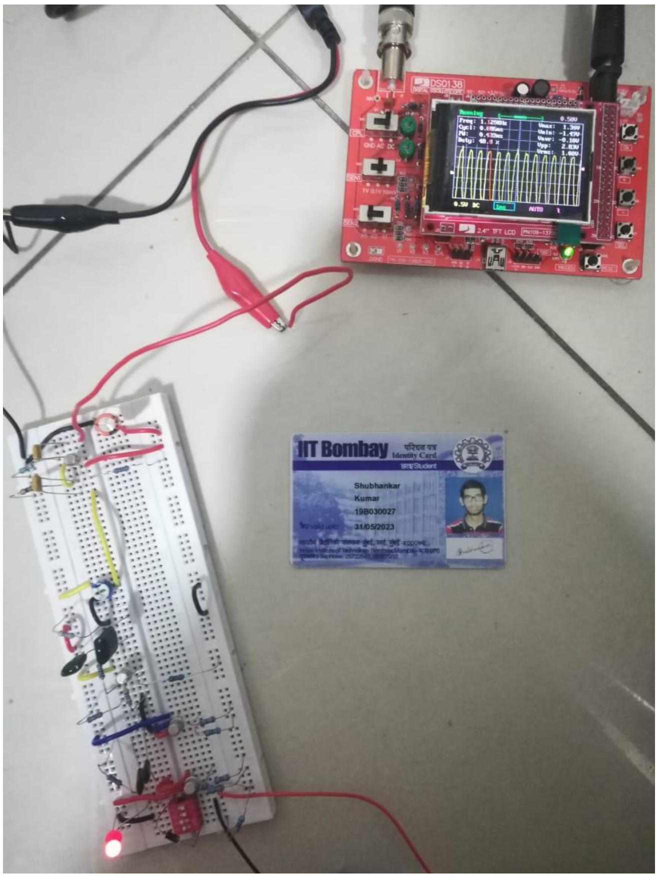
Build your high input impedance buffer circuit as designed at Level 1 on your breadboard. Provide it with input from your FG. Set the output $R_L = 4.7k\Omega$ Omit the intermediate high gain CE voltage amplifier (Endsem.A) at this stage to simplify debugging.

Set amplitude of FG output to a value you would expect to get from your high gain CE voltage amplifier.

Put photos of your circuit assembly and measurements (with DSO + ID) here. Label the photos indicating which trace is v_{in} and v_{out} to this buffer circuit



V_{IN}



V_{OUT}

From the two images, we see that the $v_{out}/v_{in} \sim 1$, i.e. voltage gain for the emitter follower is nearly constant, which is as expected.

Level 2.B end-to-end test 15

Do an end-to-end test of circuits from Endsem.A and Endsem.B together with a final load

$R_L = 4.7k\Omega$

Demonstrate linear behavior of the following chain:

FG
∟high gain voltage amplifier (Endsem.A)
∟ buffer circuit (Endsem.B)
∟**$R_L=4.7k\Omega$**

Put labelled photos below of the voltage as measured at each stage of the above chain.

Fallback option for those running out of time and ideas:

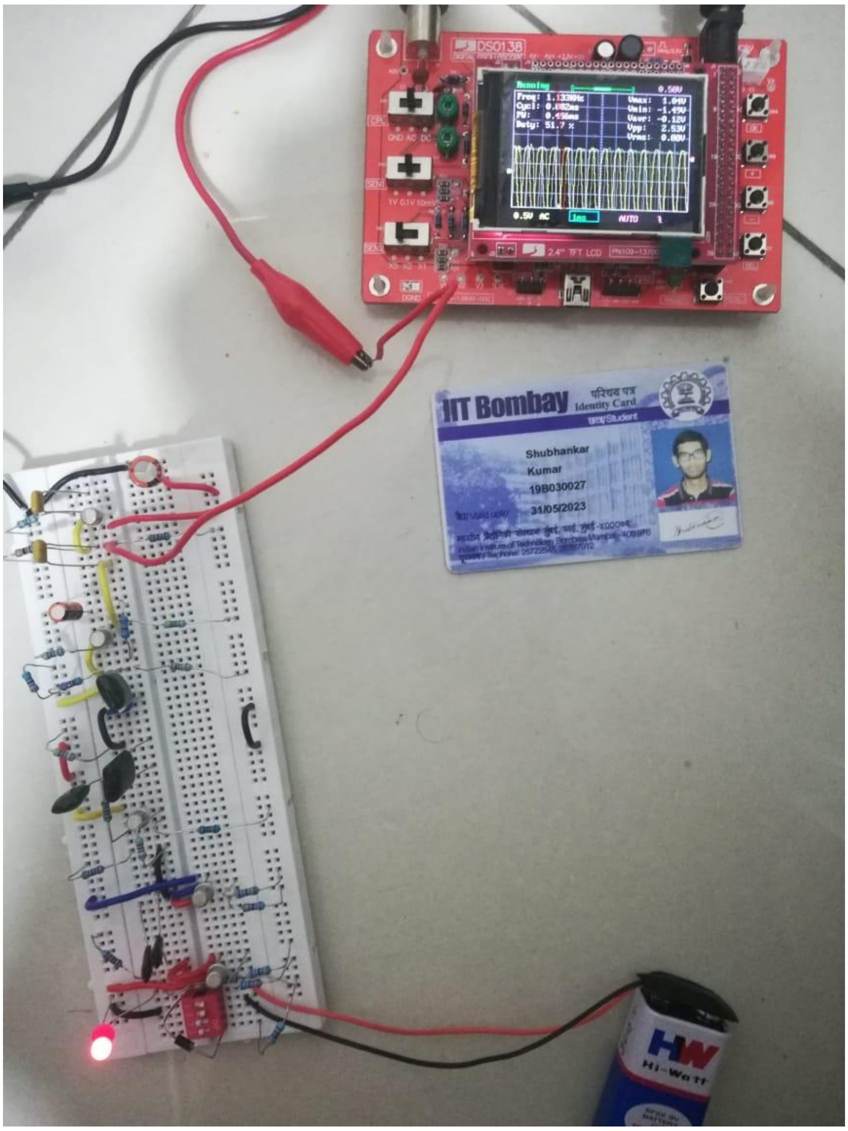
If: you were unable to solve Endsem.A problem,

Then: you can replace that stage with the pre-designed circuit from Fig 1 of

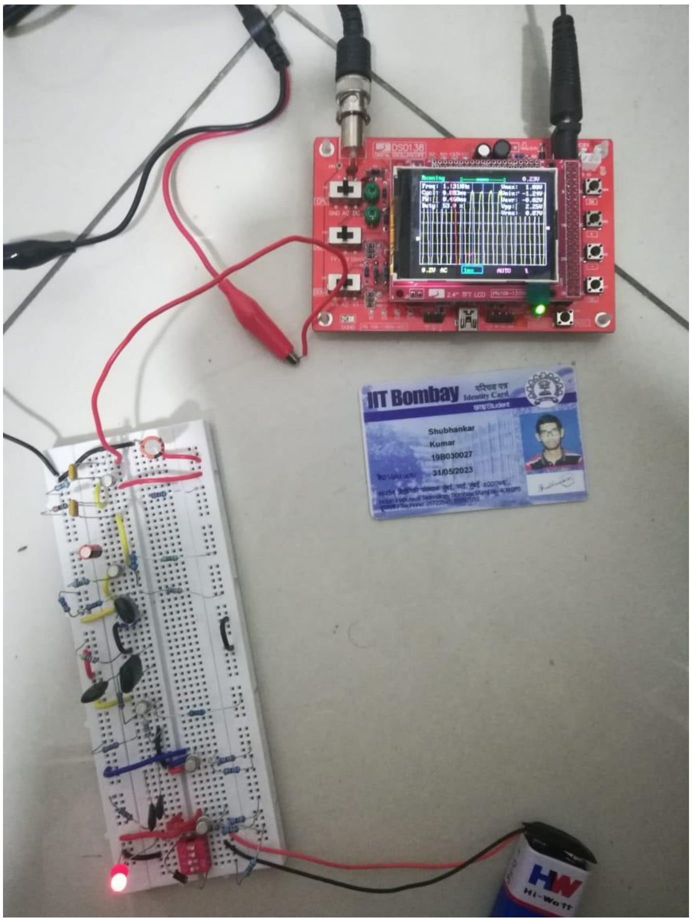
Endsem.A (i.e. CE voltage amplifier with voltage gain $G = -10$ like Lab 4).
Then: Test your solution to Endsem.B

i.e. it is acceptable to demonstrate for reduced marks, to demonstrate the following:

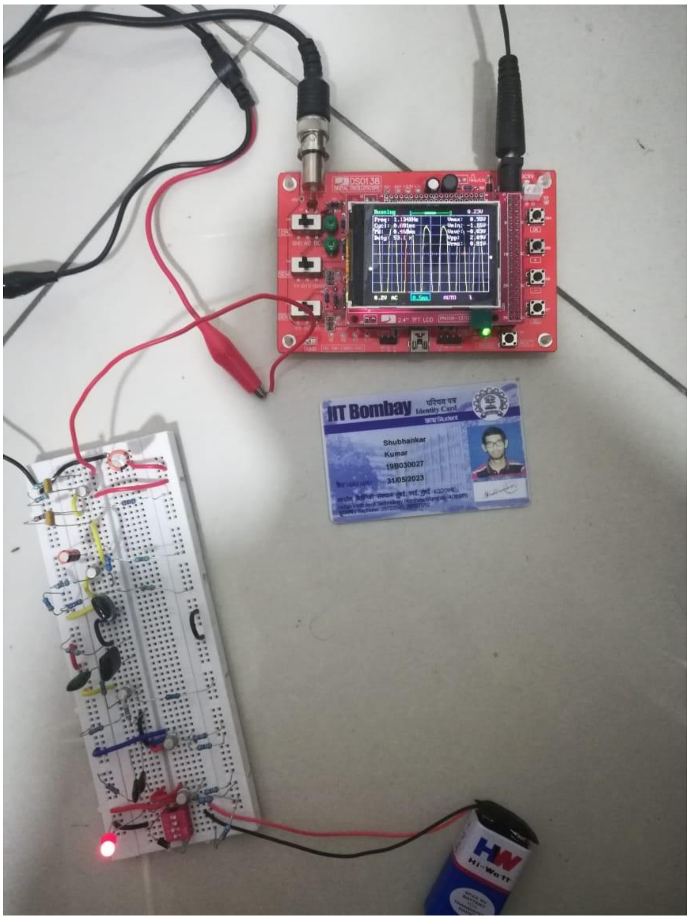
FG → CE voltage amplifier ($G = -10$) → driving Endsem.B buffer → final load $R_L = 4.7k\Omega$ maintaining net voltage $G \sim -10$



High gain Voltage Amplifier



High gain voltage amplifier with
Buffer circuit (Emitter follower)



High gain voltage amplifier +
Buffer circuit + Load resistance

--------------end of exam---------------