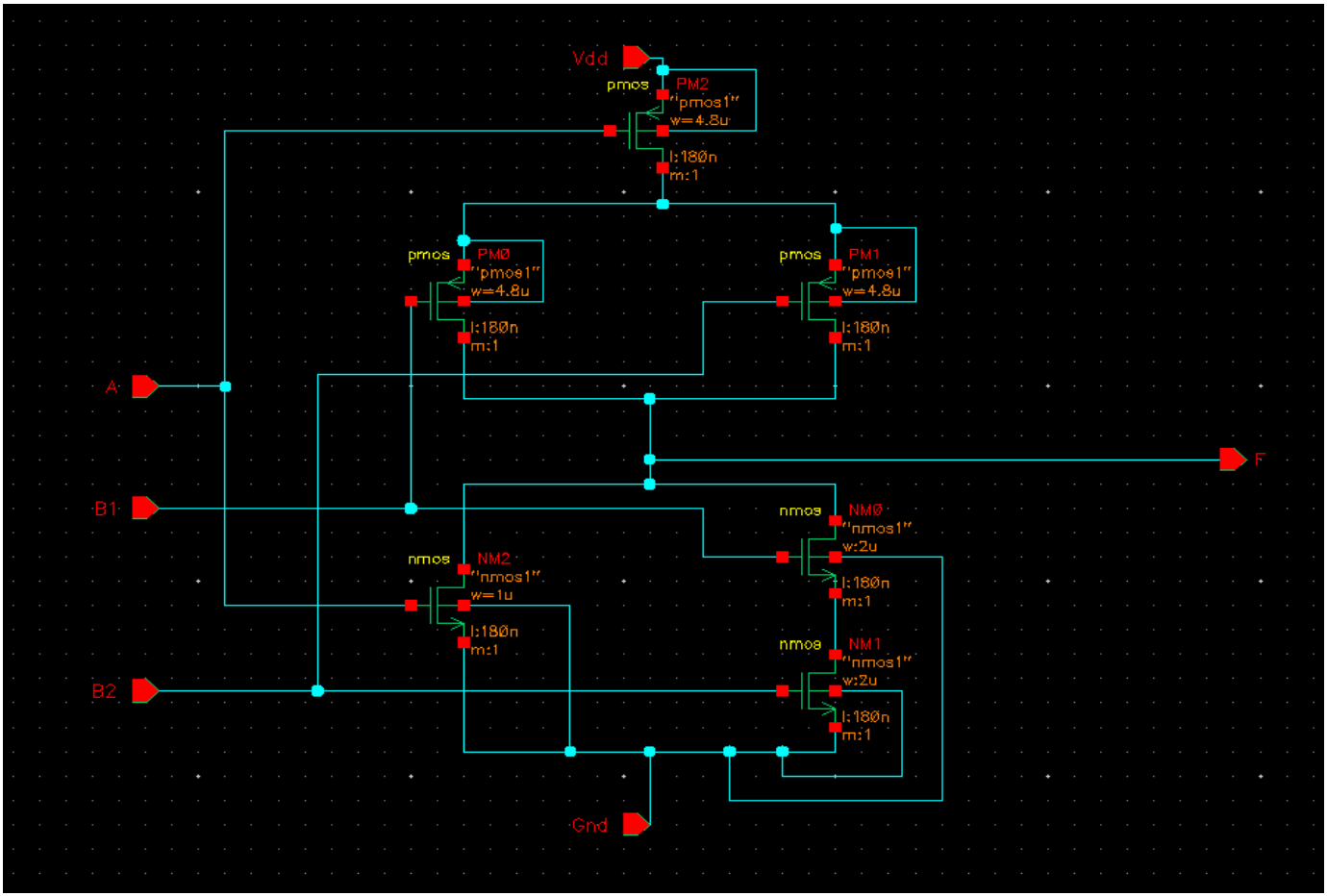
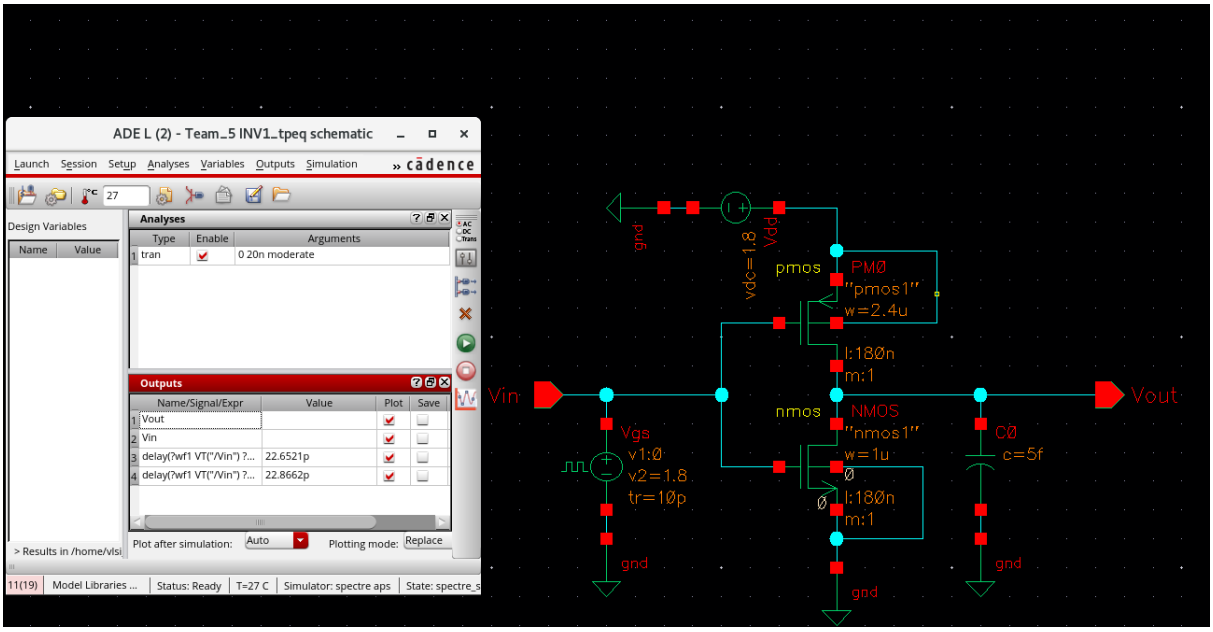
(a) SCHEMATIC


Vdd
pmos
PM2
"pmos1"
w=4.8u
l:180n
m:1
pmos
PM0
"pmos1"
w=4.8u
l:180n
m:1
pmos
PM1
"pmos1"
w=4.8u
l:180n
m:1
A
F
B1
nmos
NM0
"nmos1"
w:2u
l:180n
m:1
nmos
NM2
"nmos1"
w=1u
l:180n
m:1
nmos
NM1
"nmos1"
w:2u
l:180n
m:1
B2
Gnd

(b) HOW TO SIZE THE TRANSISTORS



Reference INV designed for $t_{plh} = t_{phl}$, as above.

Lengths / ~~widths~~ were kept same (180nm)

Width (NMOS) kept as 1 μm

Varied width (PMOS) to make delays equal.

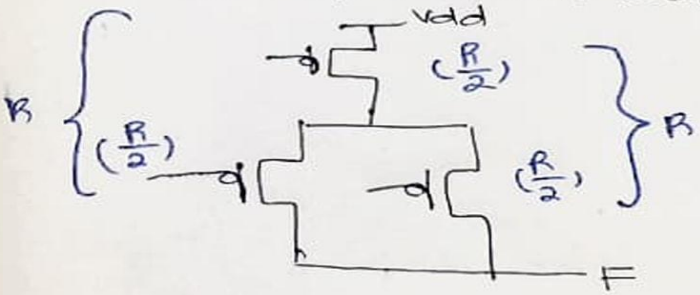
W (PMOS) = 2.4 μm

$t_{plh} = \ln 2 \, (R_{eq,p}) \, C_L$

$t_{phl} = \ln 2 \, (R_{eq,n}) \, C_L$.

$t_{plh} = t_{phl} \rightarrow R_{eq,n} = R_{eq,p} = R$

For t_{plh} → PUN design.



For keeping Req as R

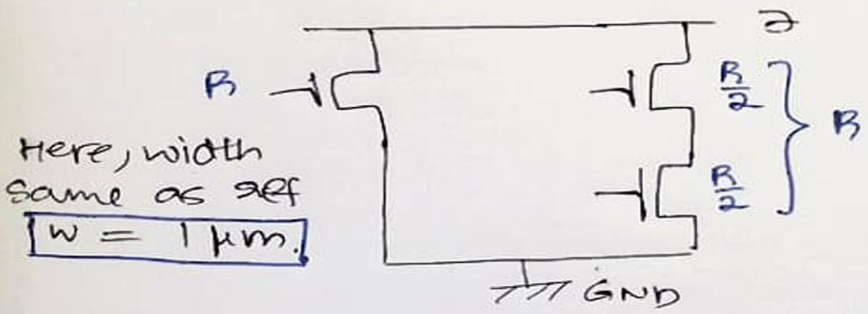
Each Tra has $\frac{R}{2}$

So size = 2β

ie. twice the width of PMOS (Ref Inv)

W = 4.8 μm

For t_{phl} → PDN Design.



Here, width same as ref

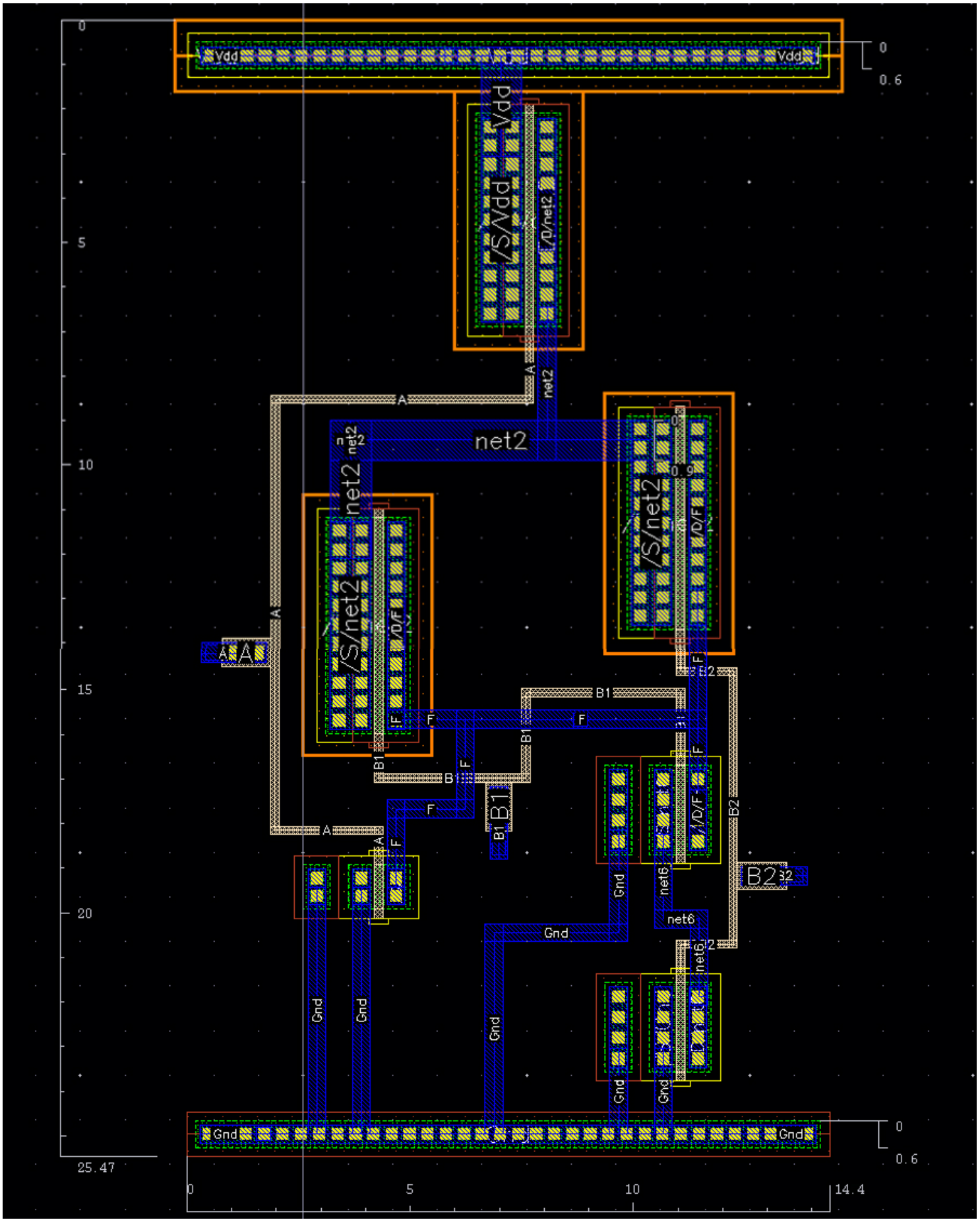
W = 1 μm.

Here size = twice width of NMOS (Ref Inv)

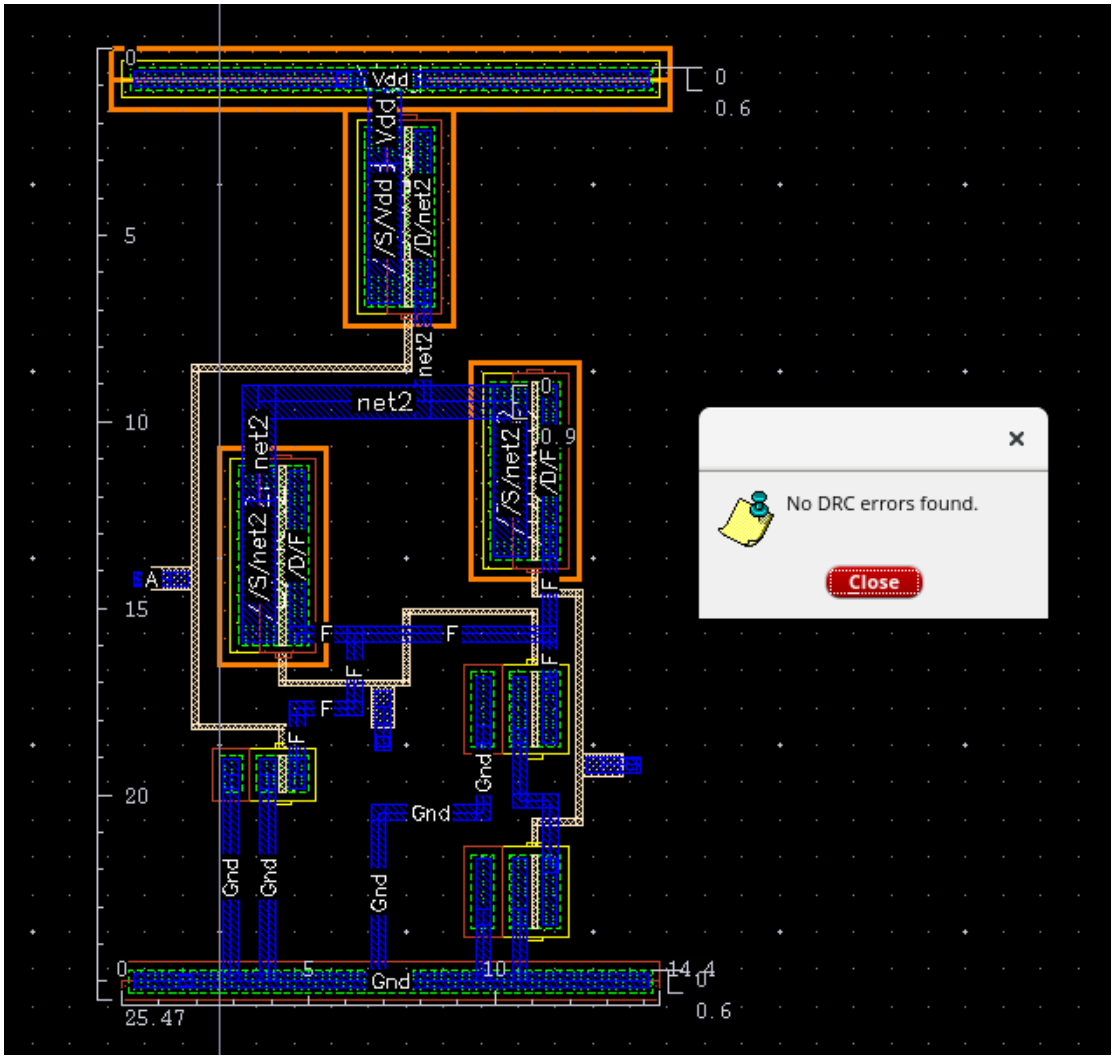
W = 2 μm

(c) LAYOUT WITH SIZES MARKED

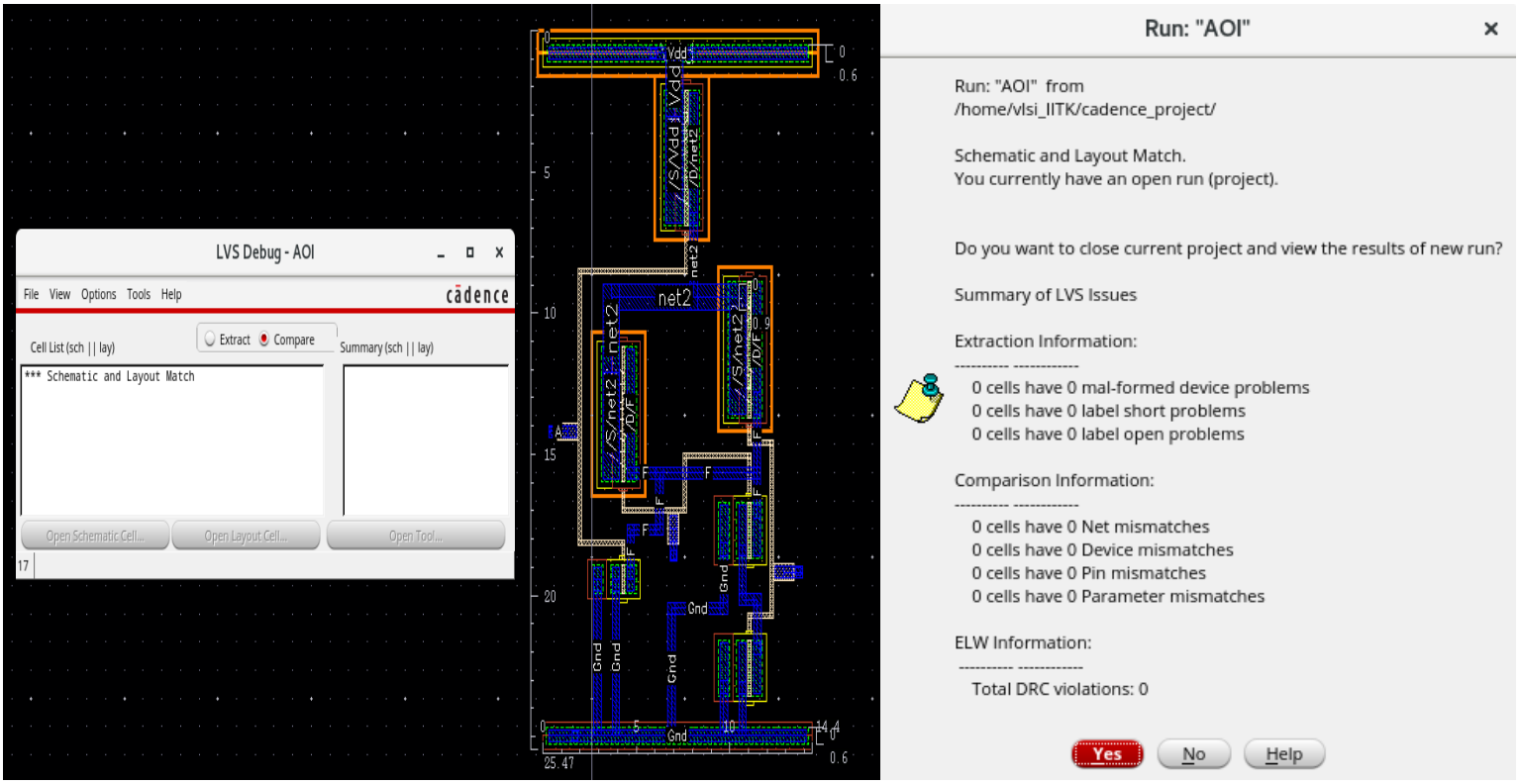
Width (VDD Rail) = Width (GND Rail) = 0.6. Length (Layout) = 14.4, Width (Layout) = 25.47.



(d) LAYOUT WITH DRC LOG



(e) LAYOUT WITH LVS LOG



(f) BEFORE SIMULATION

t_{pHL} from A to F (B_1 = 0, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	60.955	130.599
100 ps	73.818	143.258

t_{pLH} from A to F (B_1 = 0, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	38.118	91.682
100 ps	54.271	108.8

t_{pHL} from A to F (B_1 = 0, B_2 = 1)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	52.395	123.545
100 ps	65.068	135.942

t_{pLH} from A to F (B_1 = 0, B_2 = 1)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	44.567	114.66
100 ps	60.477	131.445

t_{pHL} from A to F (B_1 = 1, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	53.652	125.418
100 ps	66.266	137.505

t_{pLH} from A to F (B_1 = 1, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	57.424	128.079
100 ps	73.8141	144.866

(g) POST SIMULATION

t_{pHL} from A to F (B_1 = 0, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	70.318	140.586
100 ps	83.403	153.582

t_{pLH} from A to F (B_1 = 0, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	51.806	105.698
100 ps	66.909	121.871

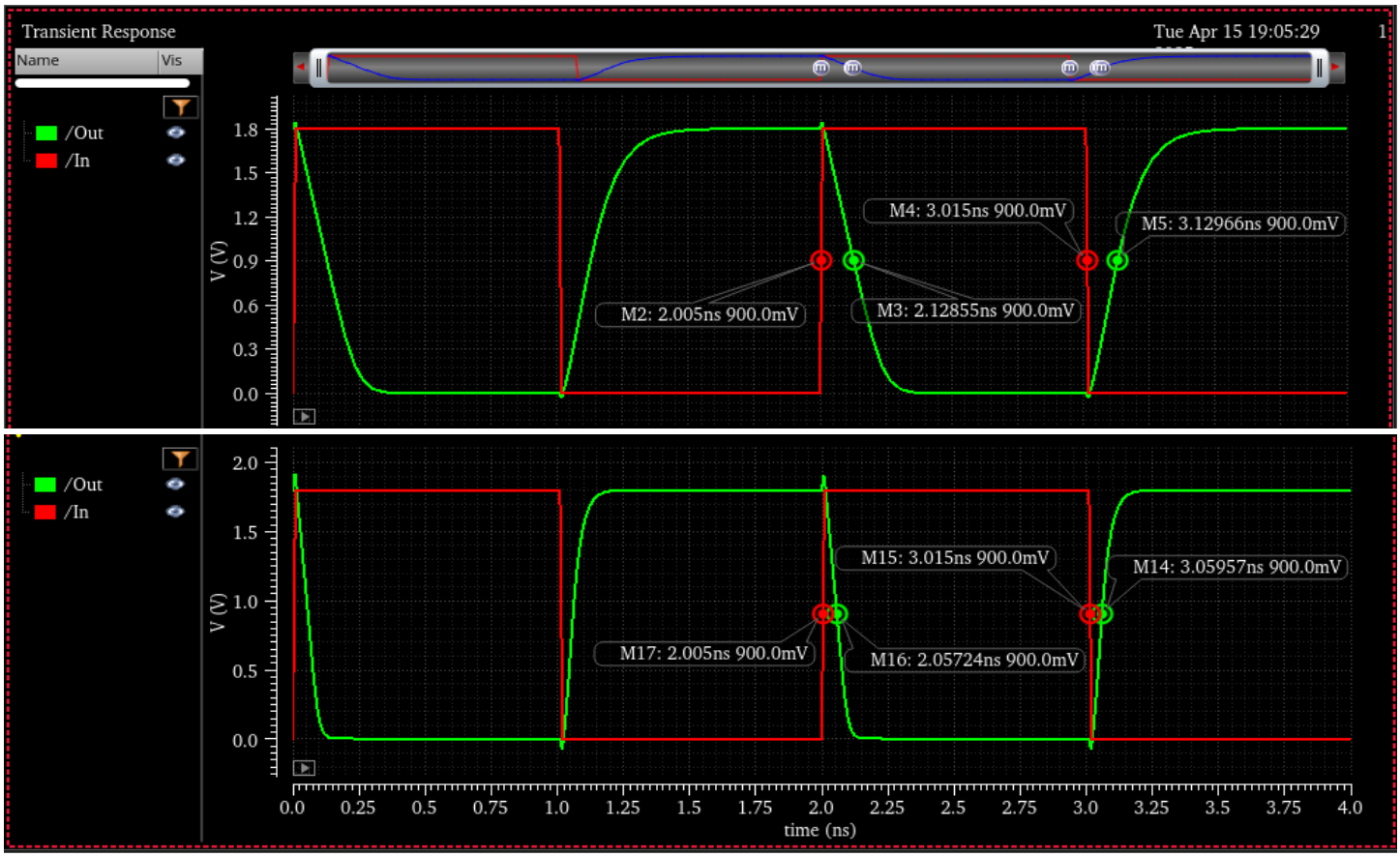
t_{pHL} from A to F (B_1 = 0, B_2 = 1)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	60.848	133.01
100 ps	74.168	145.852

t_{pLH} from A to F (B_1 = 0, B_2 = 1)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	59.664	130.574
100 ps	74.64	146.294

t_{pHL} from A to F (B_1 = 1, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	62.256	134.848
100 ps	75.434	147.705

t_{pLH} from A to F (B_1 = 1, B_2 = 0)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	74.638	145.701
100 ps	89.955	161.511

(h) Transient analysis waveforms of input and output from schematic, for **tr = tf = 10 ps, (B1= 0, B2 =1)**
(i) C = 50 fF (ii) C = 5 fF



(i) Transient analysis waveforms of input and output post layout, for **tr = tf = 10 ps, C = 50 fF , (B1= 0, B2 =1)**
(i) C = 5 fF (ii) C = 50 fF