Booth Multiplier

Robin Singh

August 2022

1 Introduction

Booth's Multiplication Algorithm is a commonly used algorithm for multiplication of two signed numbers. Let us see how to write a Verilog code for this algorithm in an FSM format.

2 Algorithm

Registers used: A, M, Q, Qres (Qres is the residual bit after a right shift of Q), n (counter)

Step 1: Load the initial values for the registers. A = 0 (Accumulator), Qres = 0, M = Multiplicand, Q = Multiplier and n is the count value which equals the number of bits of multiplier.
Step 2: Check the value of Q0,Qres. If 00 or 11, goto step 5. If 01, goto step 3. If 10, goto step 4.
Step 3: Perform A = A + M. Goto step 5.
Step 4: Perform A = A - M.
Step 5: Perform Arithmetic Shift Right of A, Q, Qres and decrement count.
Step 6: Check if counter value n is zero. If yes, goto next step. Else, goto step 2.
Step 7: Stop

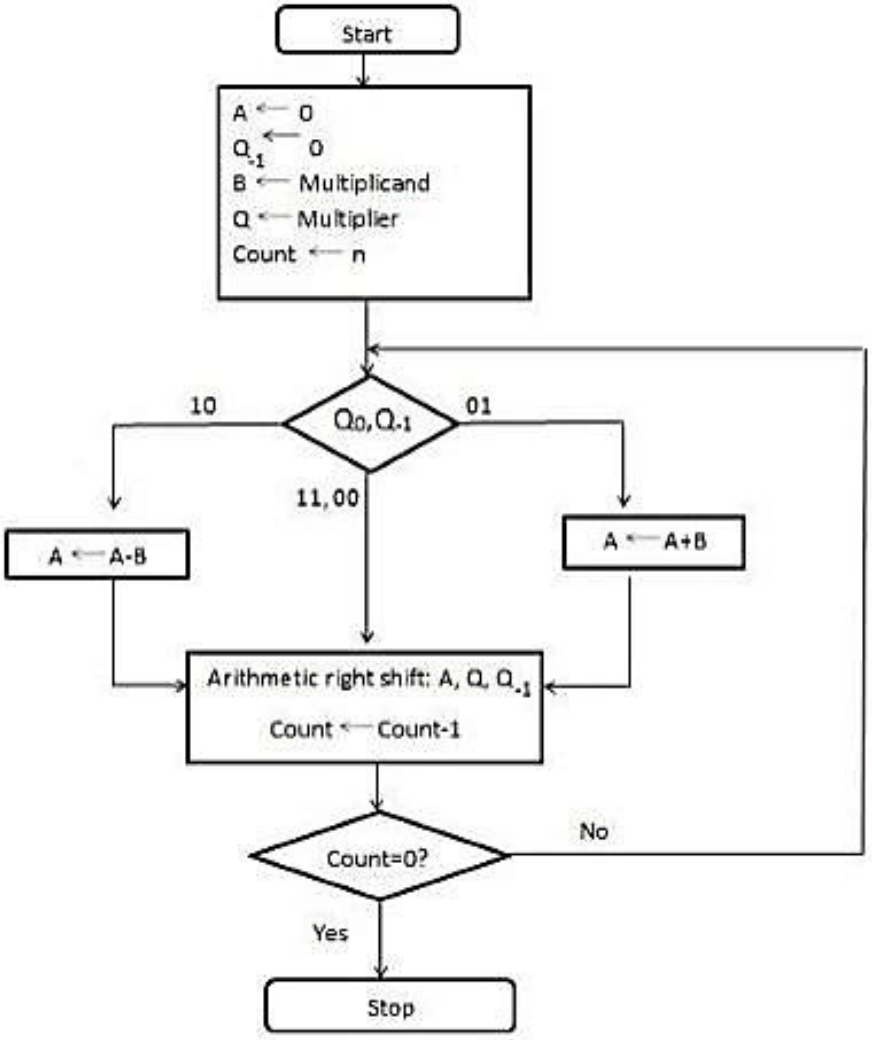
Start
A ← 0
Q-1 ← 0
B ← Multiplicand
Q ← Multiplier
Count ← n
Q0,Q-1
10
01
11, 00
A ← A-B
A ← A+B
Arithmetic right shift: A, Q, Q-1
Count ← Count-1
Count=0?
No
Yes
Stop

Figure 1:

3 Result

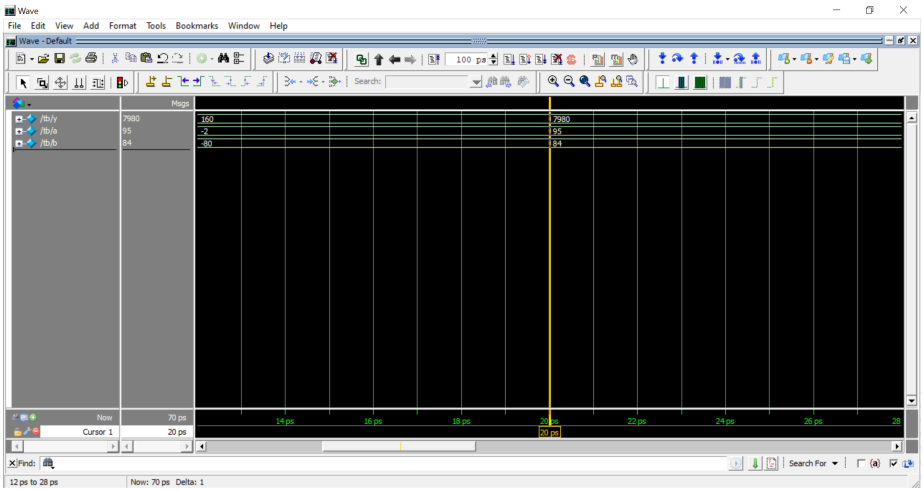

Figure 2: