ATIS WS 20/21 Assignment for Lecture 3

Team Members:

Ankit Agrawal (2581532)

Anika Fuchs (2580781)

Task 1:

a) False
There would be a **deadlock**. As XOR send only to one (A OR B) but AND will wait for both output A & B.

b) True
The first AND gate activates both A & B. but in XOR, let's say one time A is allowed and B disabled, similarly A is disabled, and B allowed. so, C will be executed only 2 times.

c) False
As after the conditional operator, both B & C can be activated, and if they are asynchronous, then both can individually go and activate D.

d) True
As we have OR gate so there are 4 possible combinations, i.e.

A(active) and B(active):	C(active)
A(active) and B(disabled):	C(active)
A(disabled) and B(active):	C(active)
A(disabled) and B(disabled):	C(disabled)

e) 1) True
Given starting XOR, any one of A & B will be definitely active, so after next XOR gate, C will also be definitely active, and as there is no end state, so it will keep on looping, and never end.
2) True
Same as above

f) True
Deadlock, as the initial AND waits for the output of second XOR which can never be executed as we do not have A.

g) True
As there is XOR in the starting, so A will be active. Then the AND gate sends the signal to end state and back to XOR, which will again active A, and keeps on executing it again and again.

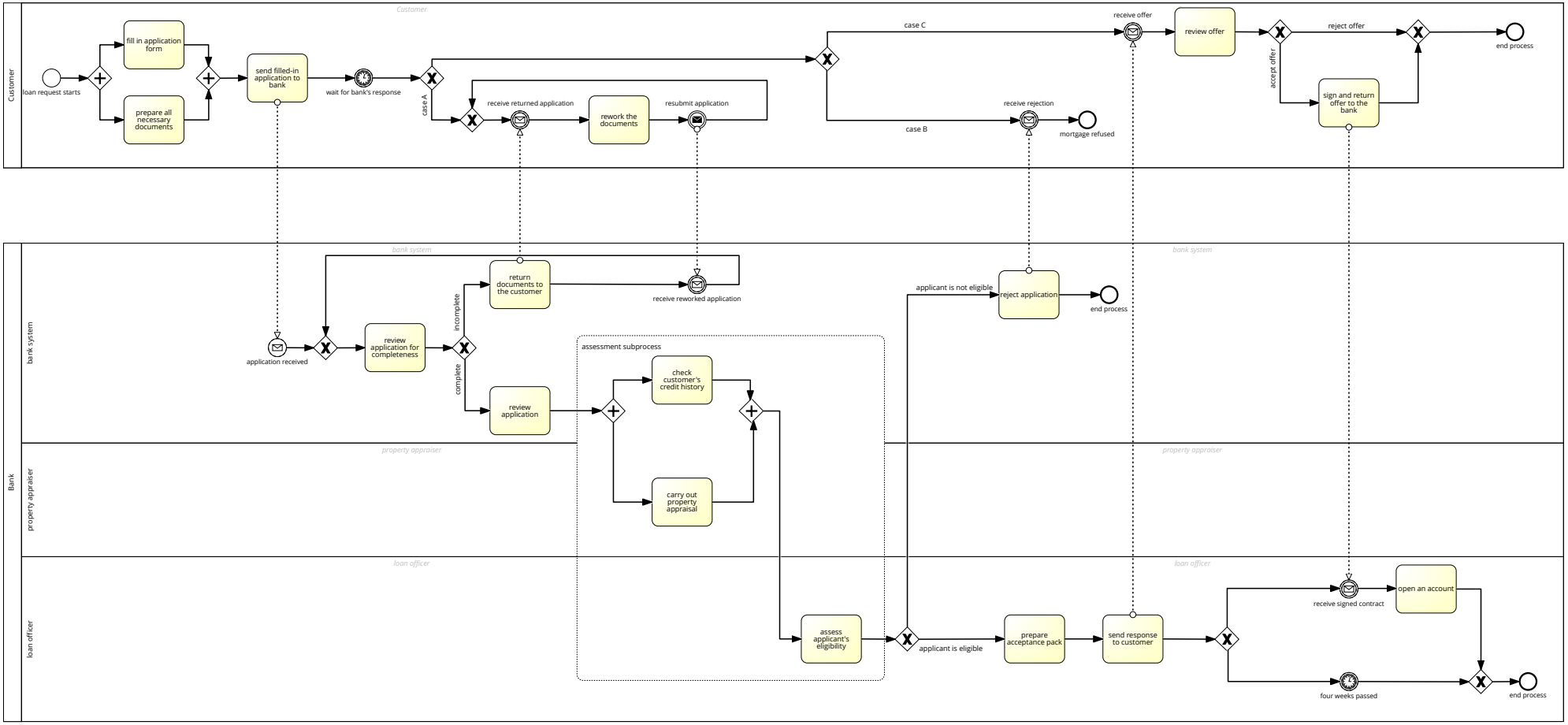
h) True

Yes, the diagram is sound. AND creates parallel paths, and while converging from the upstream it will still wait for both the signals to arrive, so it is synchronous, and also there is no loop, making the model sound.

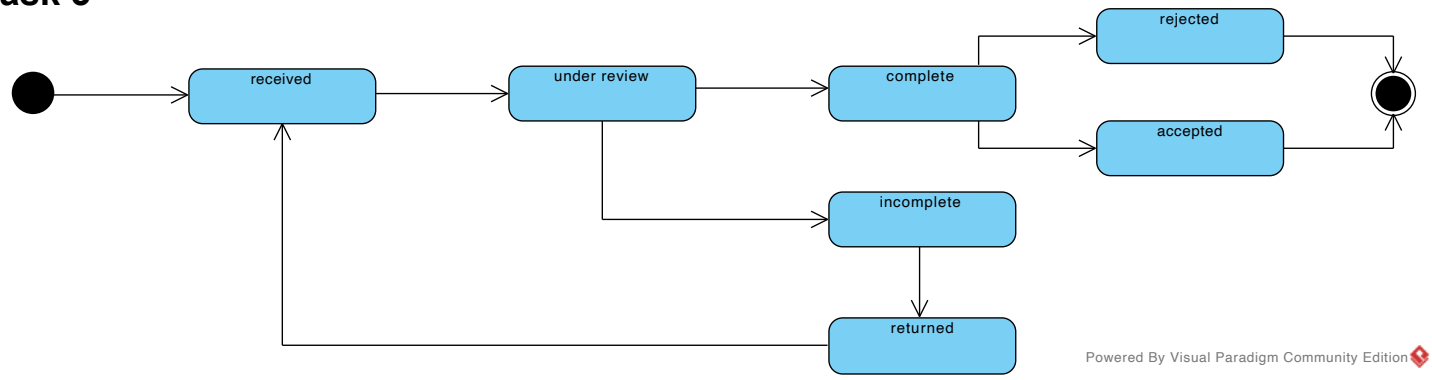
i) True
Lack of synchronization arises when any gate waits for 2 signals to arrive, whereas in XOR gate we never split the signal into parallel pathways, hence there is no problem of Lack of synchronization.

Task 2

Assignment for Lecture 3 - Mortgage Approval Process



Task 3


received
under review
complete
rejected
accepted
incomplete
returned
Powered By Visual Paradigm Community Edition