

# IC TESTER USING MICROPROCESSOR-8085

Under the guidance of Dr. Paritosh Peshwe

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## QUESTION:

Design a Microprocessor based Tester to test the logical functioning of the following chips:

(i) 7400

(ii) 7402

(iii) 7410

The IC to be tested will be inserted in a 14 pin ZIF socket. The IC number is to be entered via a keyboard. The results of the test along with the IC number are to be displayed. Design the necessary hardware and write the necessary ALP for implementing the above-mentioned task.

## SYSTEM DESCRIPTION:

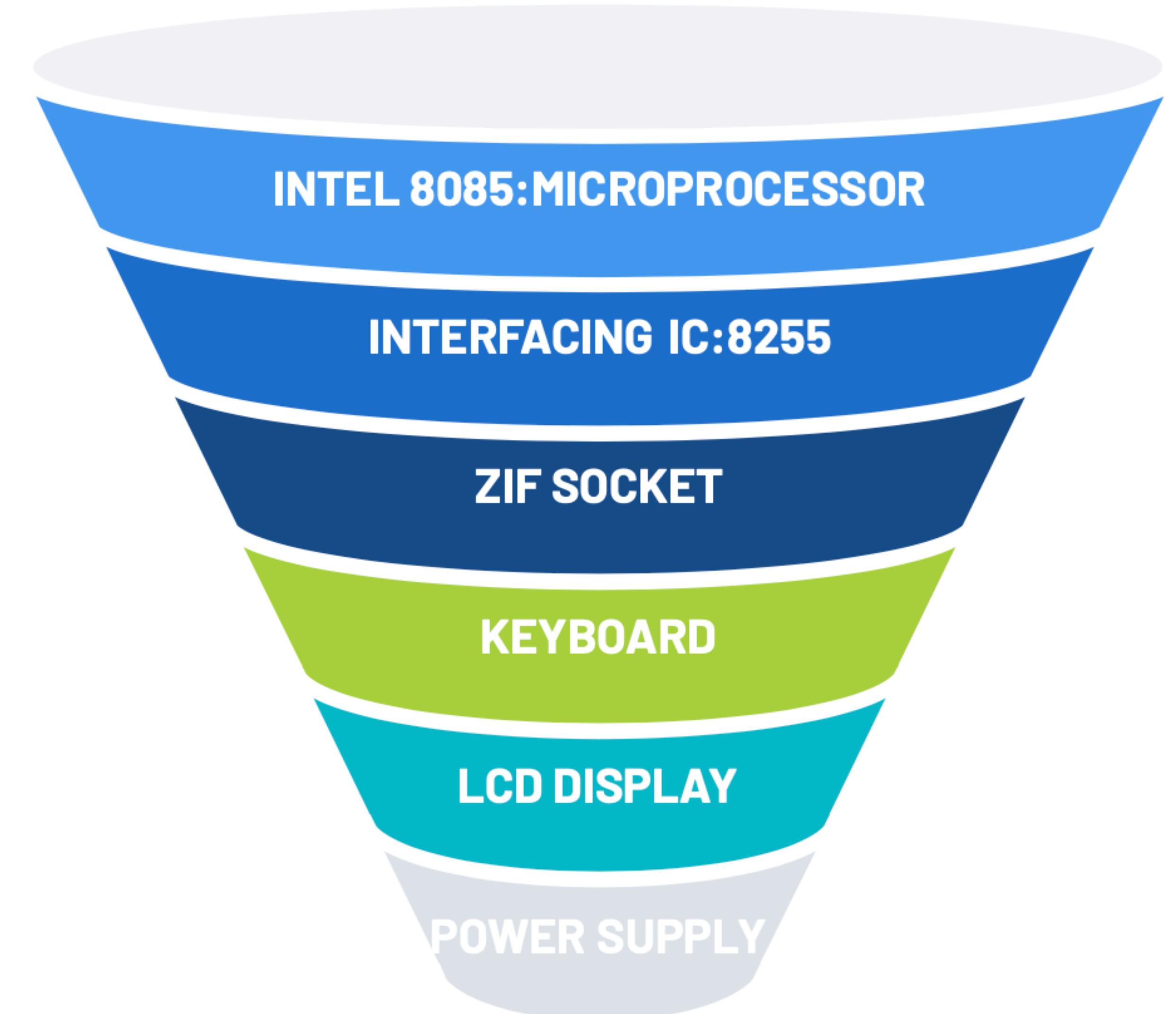
The **IC** tester is so designed ,such that user can check whether the **IC** is in working condition or not. User will enter **IC** number through keyboard and 8085 give result.If all the gate of **IC** are in working condition then LCD display will display good otherwise bad

The **IC** tester is built around 8085 and ZIF Socket are interface through 8255[PPL] **IC**.We need to do both read and write operations and display the result on LCD display.

## ASSUMPTIONS:

- 1.It is assumed that at any given instant only one Zif socket is used

## HARDWARE DEVICES:



# I/O MAP USING 8255:

1. 8255 :Interfacing the i/o devices

**Base Address:** 100H

Name of Ports of 8255	Address
PORT A	100H
PORT B	101H
PORT C	102H
CWR	103H

# Port Specification:

## a) For Checking NAND Gate

8255 in Mode 1

Port A: INPUT (PA<sub>0</sub>-PA<sub>7</sub>)

Port B: OUTPUT(PB<sub>0</sub>-PB<sub>3</sub>)

TRUTH TABLE

A (input)	C (input)	X (output)
0	0	1
0	1	1
1	0	1
1	1	0

CWR format for NAND Gate

1 0 1 1 0 1 0 0

## Port Specification:

### b) For Checking NOR Gate

8255 in Mode 1

Port A: INPUT (PA<sub>0</sub>-PA<sub>7</sub>)

Port B: OUTPUT(PB<sub>0</sub>-PB<sub>3</sub>)

TRUTH TABLE

A (input)	C (input)	X (output)
0	0	1
0	1	0
1	0	0
1	1	0

CWR format for NOR Gate

1	0	1	1	0	1	0	0
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## Port Specification:

### c) For Checking TRIPLE INPUT NAND Gate

8255 in Mode 0

Port A: INPUT (PA<sub>0</sub>-PA<sub>7</sub>)

Port B: INPUT(PB<sub>0</sub>-PB<sub>3</sub>)

Port C: OUTPUT(PB<sub>7</sub>-PB<sub>5</sub>)

TRUTH TABLE

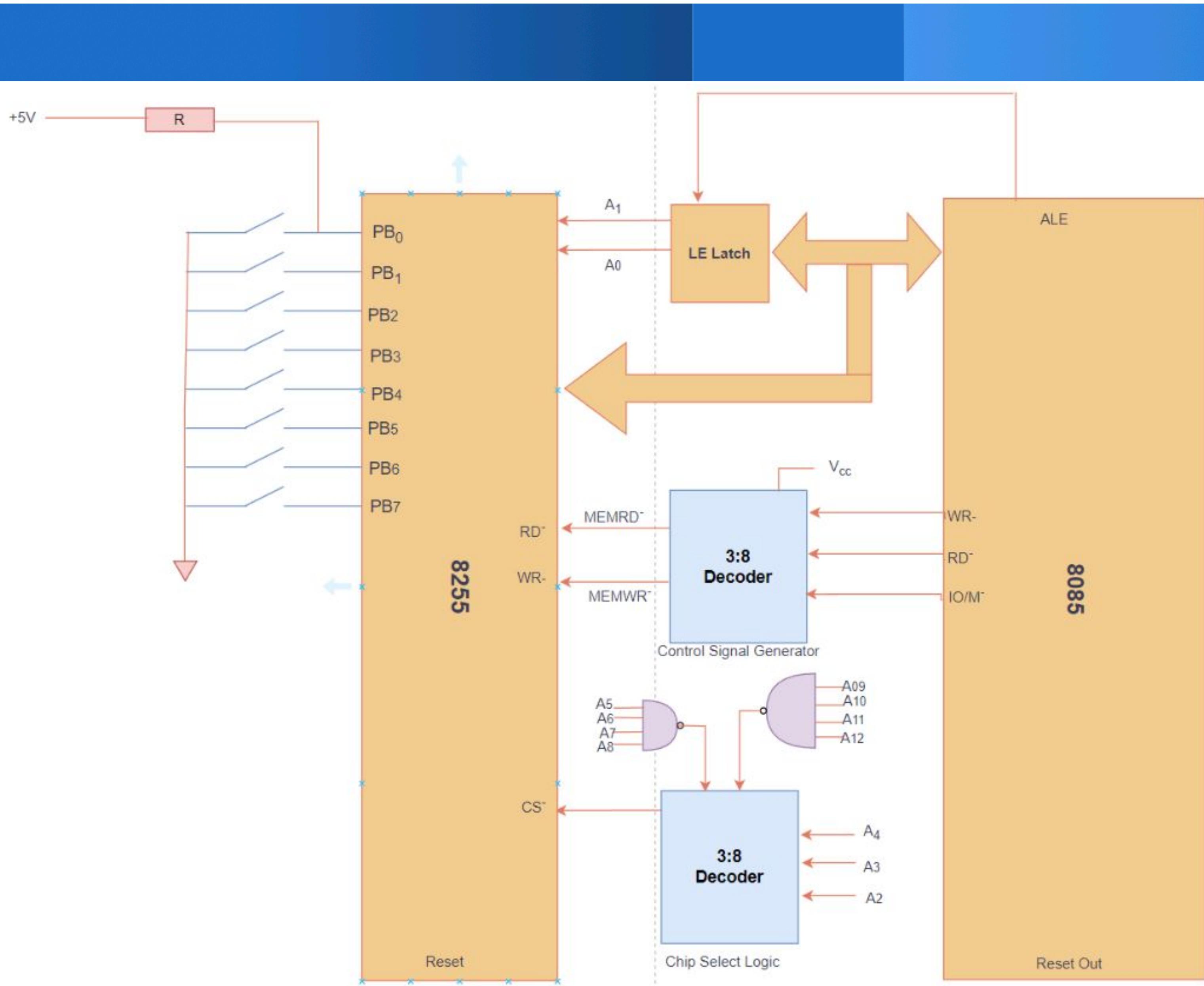
A (input)	B (input)	C (input)	X (output)
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

CWR format for Triple Input NAND Gate

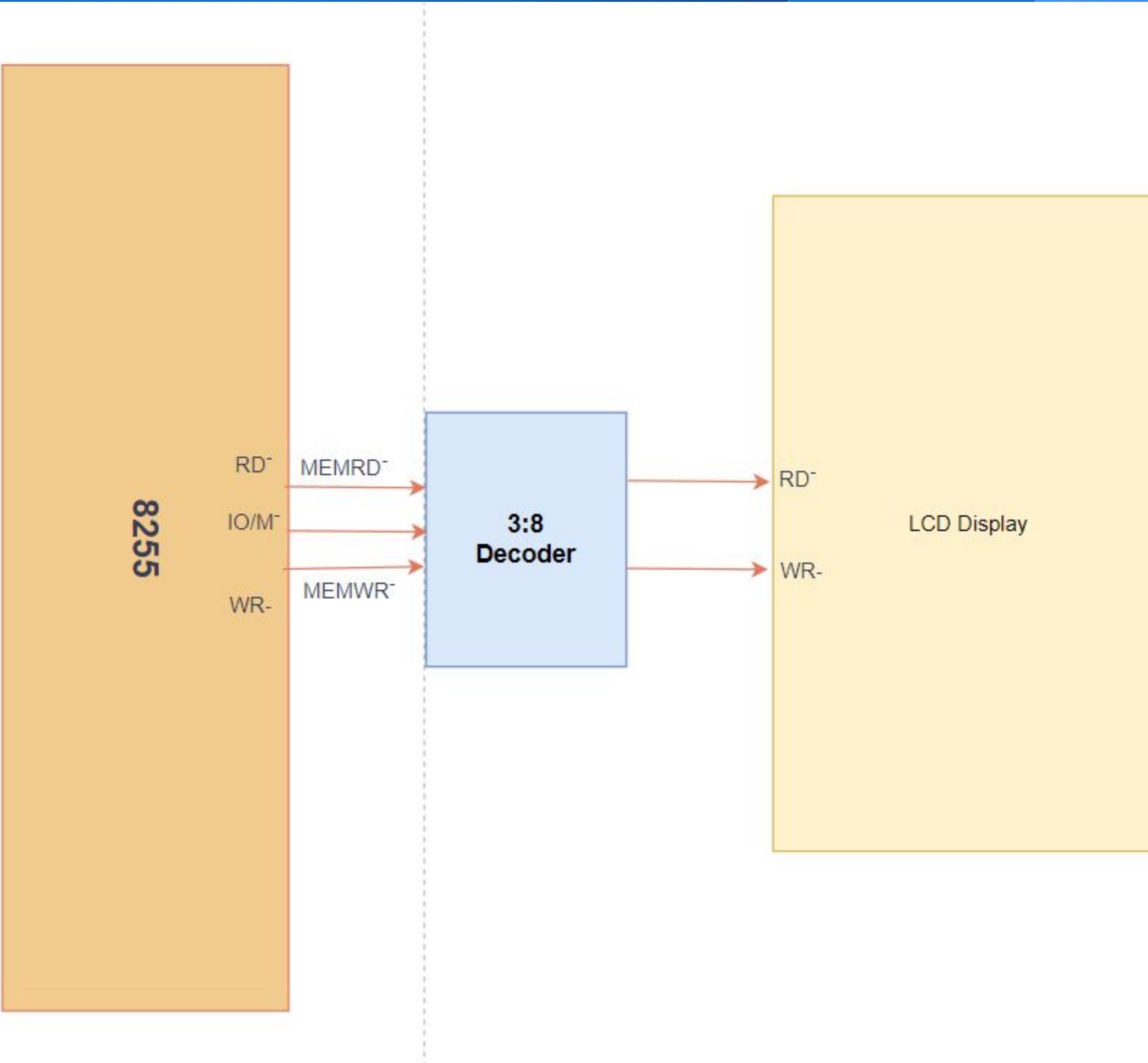
1 0 0 1 0 0 1 0

## INTERFACING OF HARWARE:

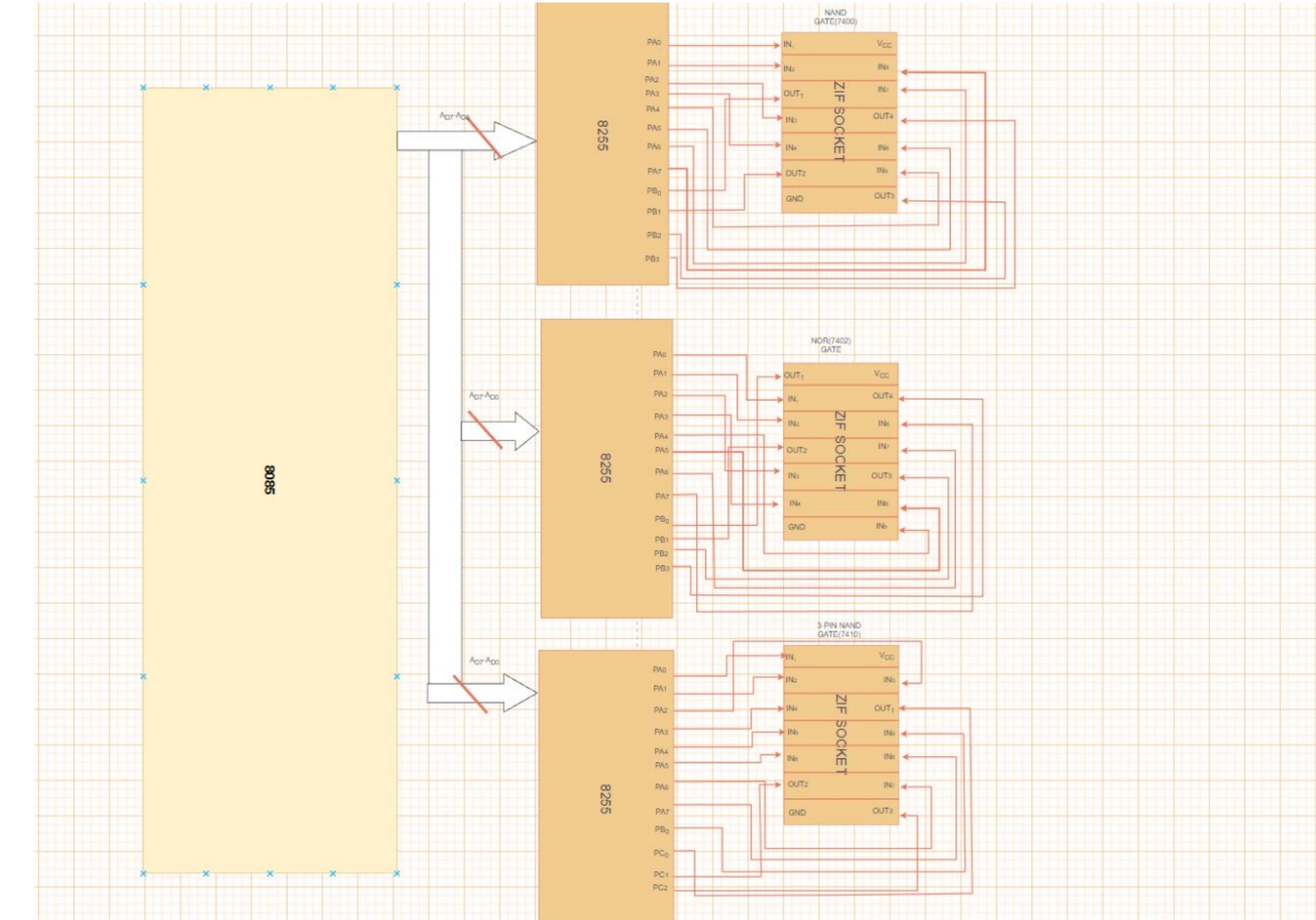
Interfacing of keyboard  
with 8085 with the help  
of 8255



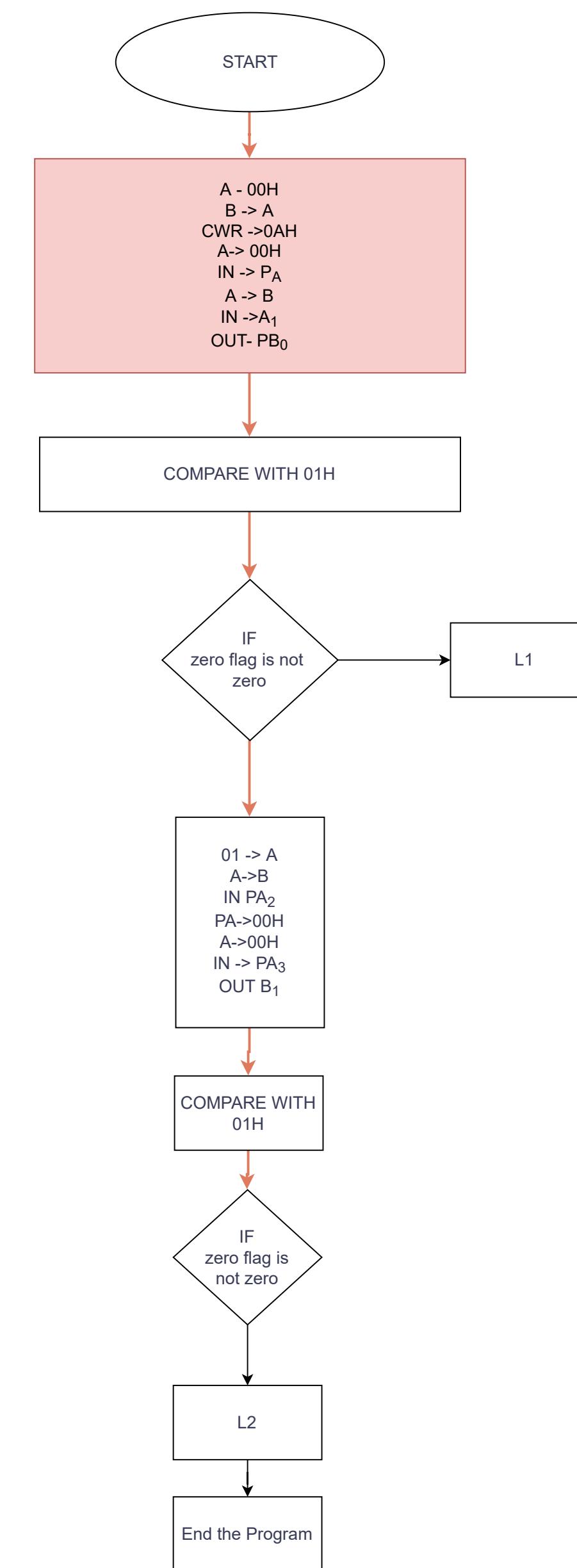
## Interfacing of LCD DISPLAY with 8085 with the help of 8255



## Interfacing of ZIF SOCKET with 8085 with the help of 8255



# FLOWCHART:



# CODES:

## Code to identify IC

OPCODE	OPERAND
MVI A	E8H
CPI	E8H
JZ	3050H
MVI A	EAH
CPI	E8H
JZ	4050H
MVI A	F2H
CPI	F2H
JZ	5050H

## SUBROUTINE CODE FOR NAND GATE:

3050:  
MVI A, B4H  
OUT CWR  
MVI A, 00  
IN PA0  
IN PA1  
IN PA2  
IN PA3  
IN PA4  
IN PA5  
IN PA6  
IN PA7  
OUT PB0  
CPI 01H  
JNZ L1 [BAD]  
OUT PB1  
CPI 01H  
JNZ L1[BAD]  
OUT PB2  
CPI 01H  
JNZ L1[BAD]

MVI A, 00H  
MOV B, A  
IN PA0  
IN PA2  
IN PA4  
IN PA6  
  
MVI A, 01H  
IN PA1  
IN PA3  
IN PA5  
IN PA7  
OUT PB0  
CPI 01H  
JNZ L1[BAD]  
OUT PB1  
CPI 01H  
JNZ L1  
OUT PB2  
CPI 01H  
JNZ L1[BAD]

MVI A, 01H  
MOV B, A  
IN PA0  
IN PA2  
IN PA4  
IN PA6  
MVI A, 00H  
MOV B, A  
IN PA1  
IN PA3  
IN PA5  
IN PA7  
OUT PB0  
CPI 01H  
JNZ L1[BAD]  
OUT PB2  
CPI 01H  
JNZ L1 [BAD]  
OUT PB4  
CPI 01H  
JNZ L1 [BAD]  
OUT PB6

CPI 01H  
JNZ L1 [BAD]  
MVI A, 01H  
IN PA0  
IN PA1  
IN PA2  
IN PA3  
IN PA4  
IN PA5  
IN PA6  
IN PA7  
OUT PB0  
CPI 00H  
JNZ L1 [BAD]  
OUT PB1  
CPI 00H  
JNZ L1  
CPI 00H  
JNZ L1[BAD]  
CALL DISPLAY [GOOD]

# SUBROUTINE CODE FOR NOR GATE:

```
4050:  
MVI A, B4H  
OUT CWR  
MVI A 00H  
IN PA0  
IN PA1  
IN PA2  
IN PA3  
IN PA4  
IN PA5  
IN PA6  
IN PA7  
OUT PB0  
CPI 01H  
JNZ L1[BAD]  
OUT PB1  
CPI 00H  
JNZ L1[BAD]  
OUT PB2  
CPI 00H  
JNZ L1[BAD]
```

```
MVI A, 00H  
MOV B, A  
IN PA0  
IN PA2  
IN PA4  
IN PA6  
  
MVI A, 01H  
IN PA1  
IN PA3  
IN PA5  
IN PA7  
OUT PB0  
CPI 01H  
JNZ L1[BAD]  
OUT PB1  
CPI 00H  
JNZ L1[BAD]  
OUT PB2  
CPI 00H  
JNZ L1[BAD]
```

```
MVI A, 01H  
MOV B, A  
IN PA0  
IN PA2  
IN PA4  
IN PA6  
MVI A, 00H  
MOV B, A  
IN PA1  
IN PA3  
IN PA5  
IN PA7  
OUT PB0  
CPI 00H  
JNZ L1[BAD]  
OUT PB2  
CPI 00H  
JNZ L1[BAD]  
OUT PB4  
CPI 00H  
JNZ L1[BAD]  
OUT PB6  
CPI 00H  
JNZ L1[BAD]
```

```
MVI A, 01H  
IN PA0  
IN PA1  
IN PA2  
IN PA3  
IN PA4  
IN PA5  
IN PA6  
IN PA7  
OUT PB0  
CPI 00H  
JNZ L1  
OUT PB1  
CPI 00H  
JNZ L1  
CPI 00H  
JNZ L1  
CALL DISPLAY
```

# SUBROUTINE CODE FOR TRIPLE INPUT NAND GATE:

5050: MVI A , 98  
OUT CWR  
MVI C, 01  
IN PA0  
MOV C,B  
INP A  
MVI A OO  
IN PA2  
OUT PC0  
CMI O1  
JNZ L1  
MVI B,OO  
IN PA3  
MOV C ,B  
IN PA4  
MOV C,A  
IN PA5  
OUT PC1  
CMI O1  
JNZ L1

MVI C,01  
IN PB1  
MVI B,01  
IN PB2  
MOV A,B  
IN PB3  
OUT PC4  
CMI OO  
JNZ L1

MVI B,OO  
IN PA6  
MVI B,01  
IN PA7  
MVI A 01  
IN PBO  
OUT PC2  
CMI O1  
JNZ L1

CALL DISPLAY

## DISPLAY CODES:

BAD:CALL 0F40  
MVI B 03H  
LXI H, 2030H  
CALL 1747  
HLT

GOOD:CALL 0F48  
MVI B 04H  
LXI H, 2030H  
CALL 1747  
HLT

## ASCII VALUE

BAD- 0F40: 42 41 44  
GOOD-0F48: 47 4F 4F 44