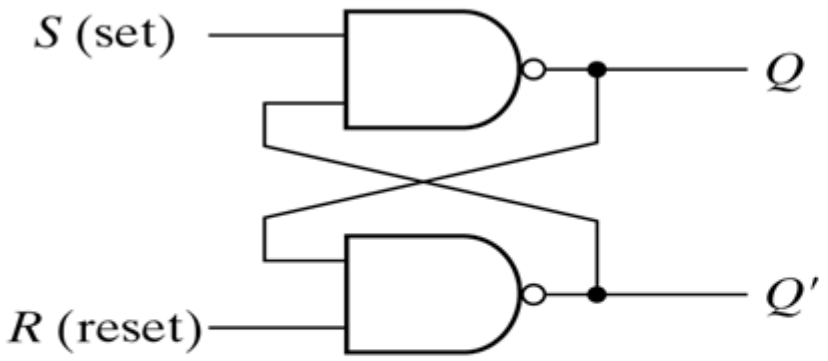
Digital Logic and Circuit
Paper Code: CS-102

Outline

- **Sequential Circuit**
- **Flip flops**
  - **JK Flip Flop**
  - **T Flip Flop**
  - **Master Slave JK Flip Flop**

SR Latch with NAND



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$) MEMORY
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$) MEMORY
0	0	1	1	NOT ACCEPTABLE

(b) Function table

SR Latch with NAND Gates

NAND TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

SR Latch with NAND

$S = set$

$R = reset$

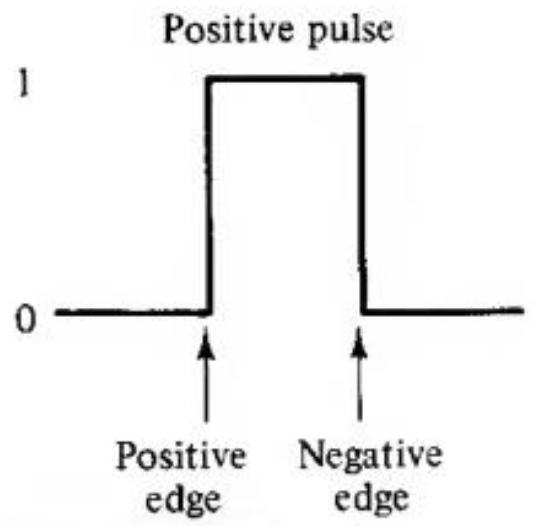
$Q = 0, \quad Q' = 1 \quad => \text{ set state}$

$Q = 1, \quad Q' = 0 \quad => \text{ reset state}$

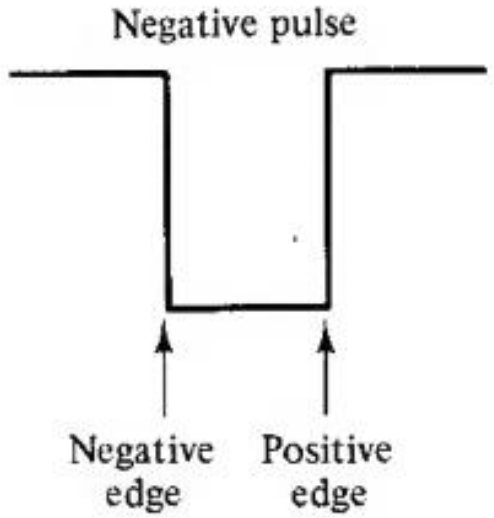
$S = 0, \quad R = 0 \quad => \text{ undefined, Q and Q' are set to 1}$

$\text{In normal conditions, avoid } S = 0, R = 0$

Triggering of Flip Flop



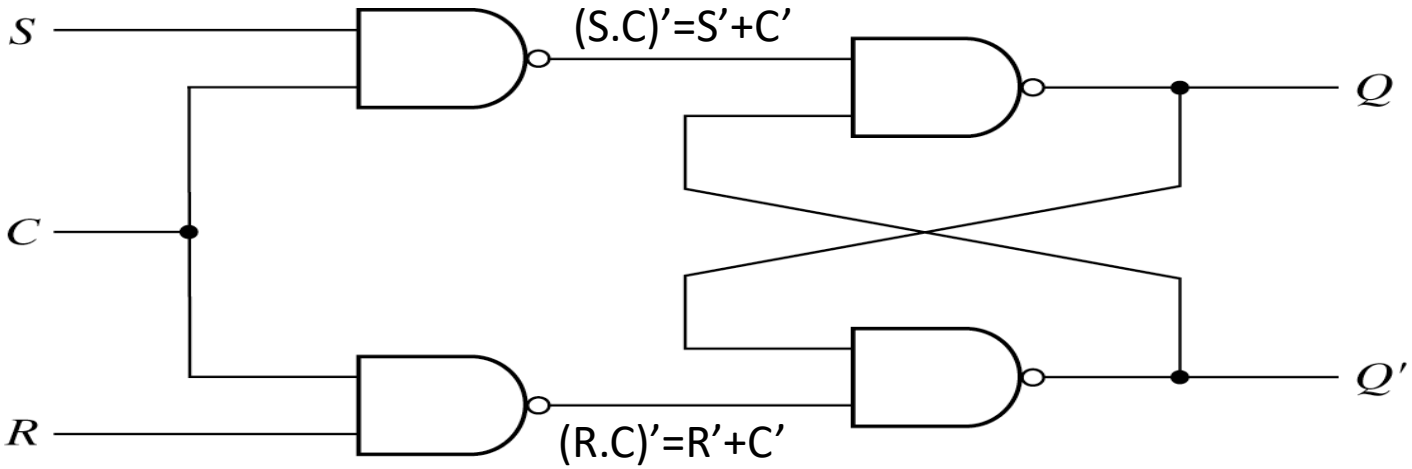
Definition of clock-pulse transition



NAND Latch

S	R	Q	Q′
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

SR Latch with Control Input



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

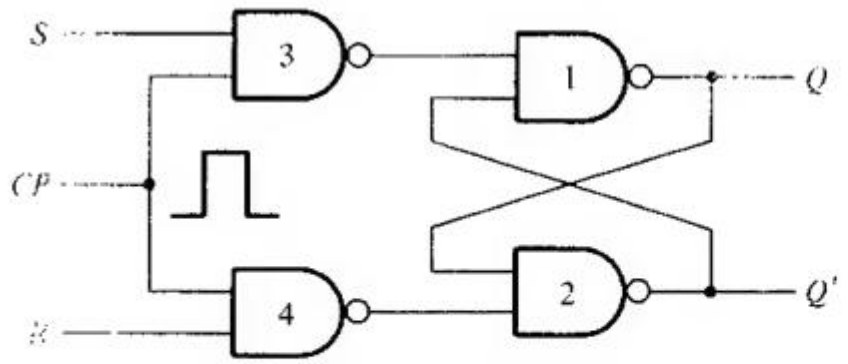
(b) Function table

Fig. 5-5 SR Latch with Control Input

We want to change the input when it is required

NAND TABLE

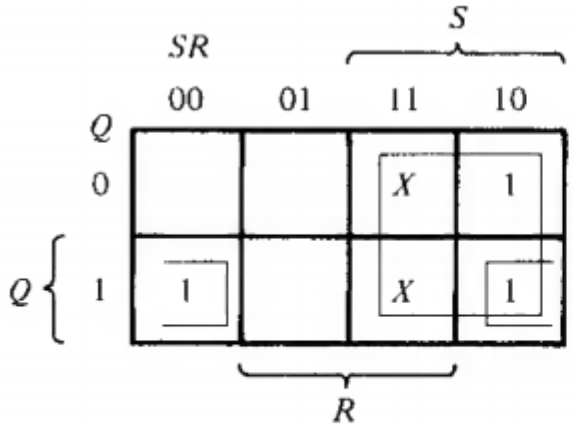
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



(a) Logic diagram

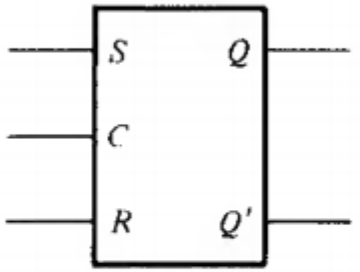
Q	S	R	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

(b) Characteristic table



$$Q(t+1) = S + R'Q$$
$$SR = 0$$

(c) Characteristic equation

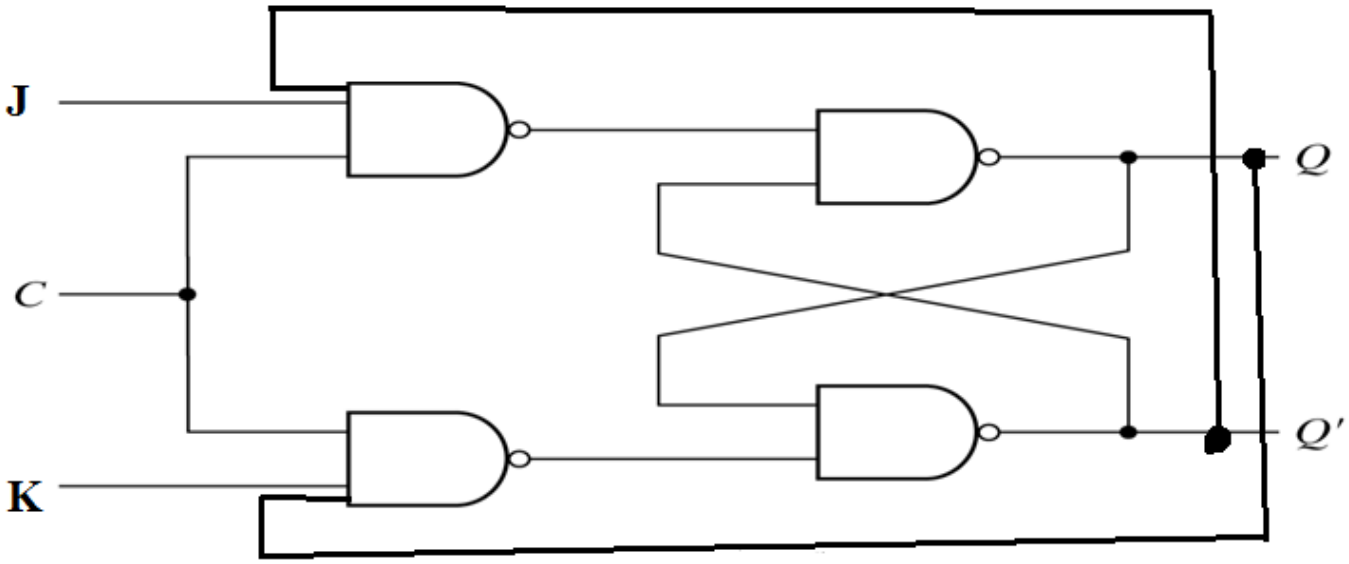


(d) Graphic symbol

NAND TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

JK Flip Flop



- When C=0, Memory
- When C=1, J=0, K=1, Q=0, Q'=1
- When C=1, J=1, K=0, Q=1, Q'=0
- When J=1, K=1, Assume Q=0 and Q'=1
- Q=0,1,0,1……
- Q'=1,0,1,0…….

NAND TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

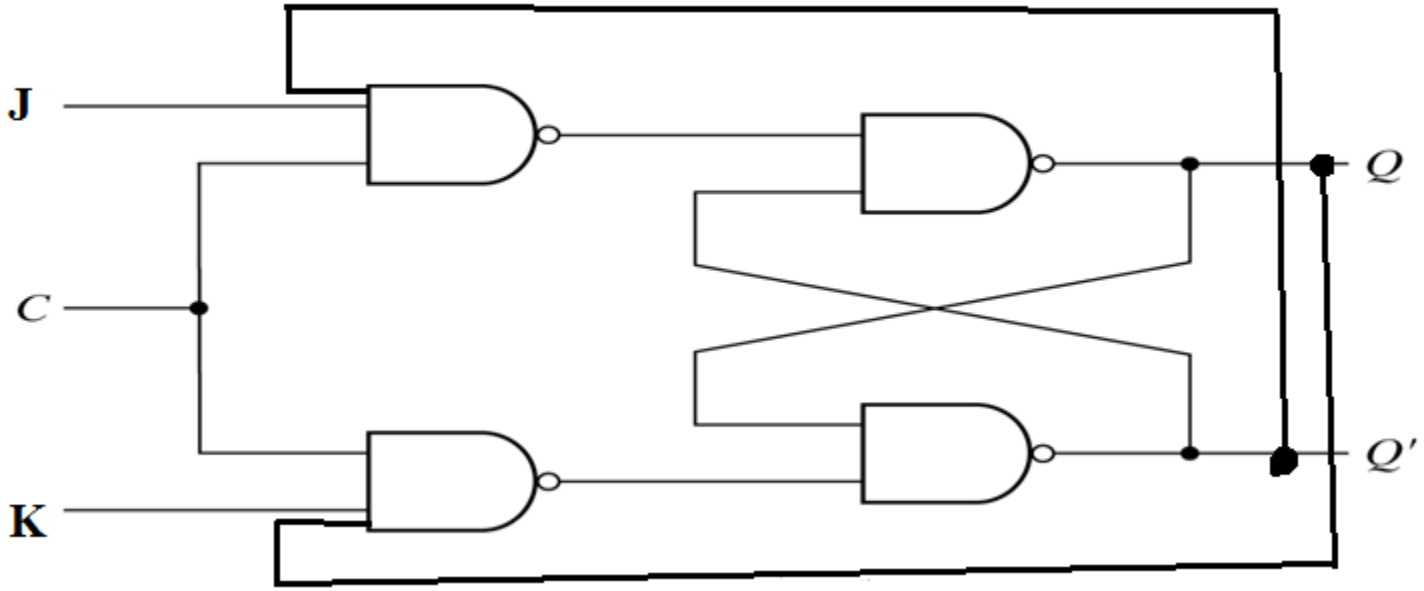
NAND Latch

S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

Clocked SR flip flop

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

JK Flip-flop



When C=0, Memory

When C=1, J=0, K=1, Q=0, Q'=1

When c=1, J=1, K=0, Q=1, Q'=0

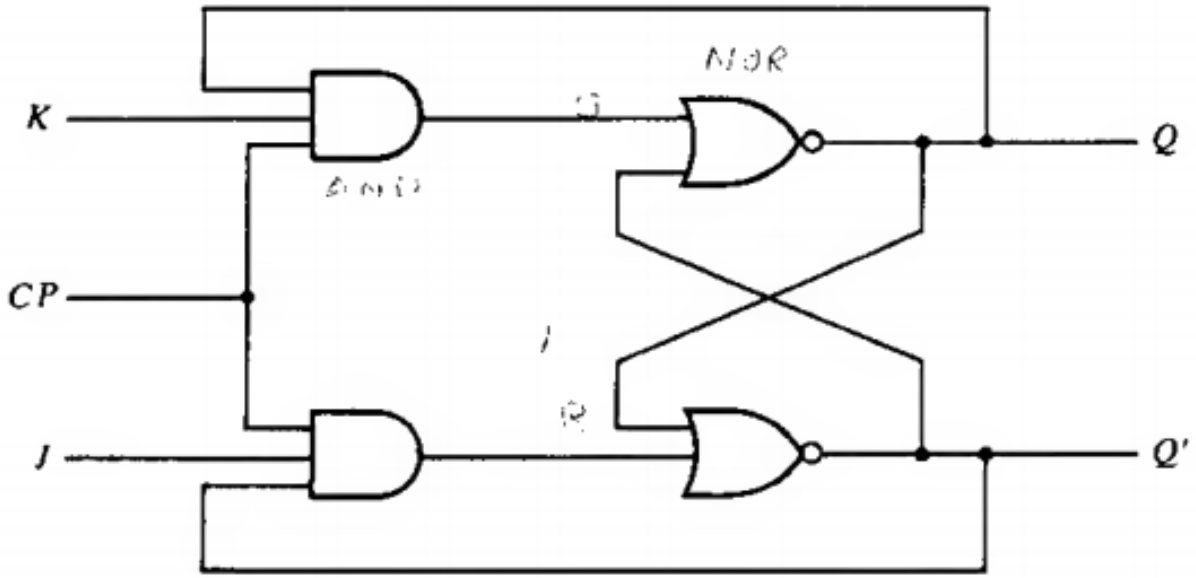
When J=1, K=1, Assume Q=0 and Q'=1

Q=0,1,0,1……

Q'=1,0,1,0……..

C	J	K	Next state of Q (Q_{n+1})
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	$\overline{Q}_n$

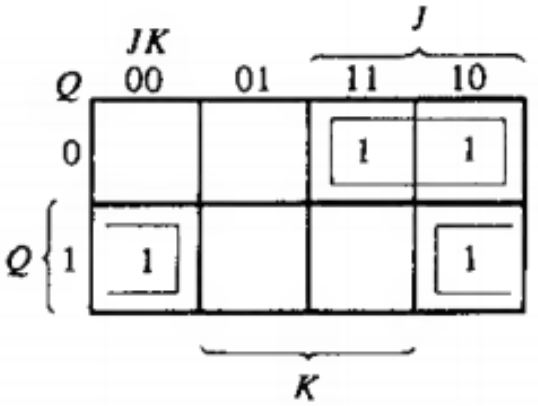
JK Flip Flop



(a) Logic diagram

Q	J	K	Q(t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Characteristic table

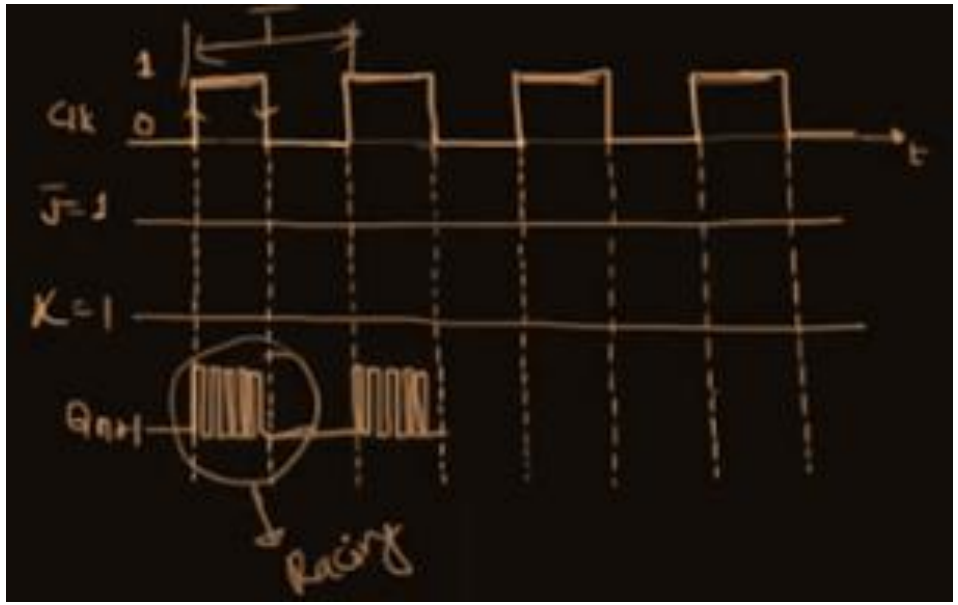


$$Q(t+1) = JQ' + K'Q$$

(c) Characteristic equation

JK Flip-flop

- The output of JK flip-flop keeps on toggling if J=K=1 and clock=1.
- When J=K=1, the output starts racing, which is called race around condition



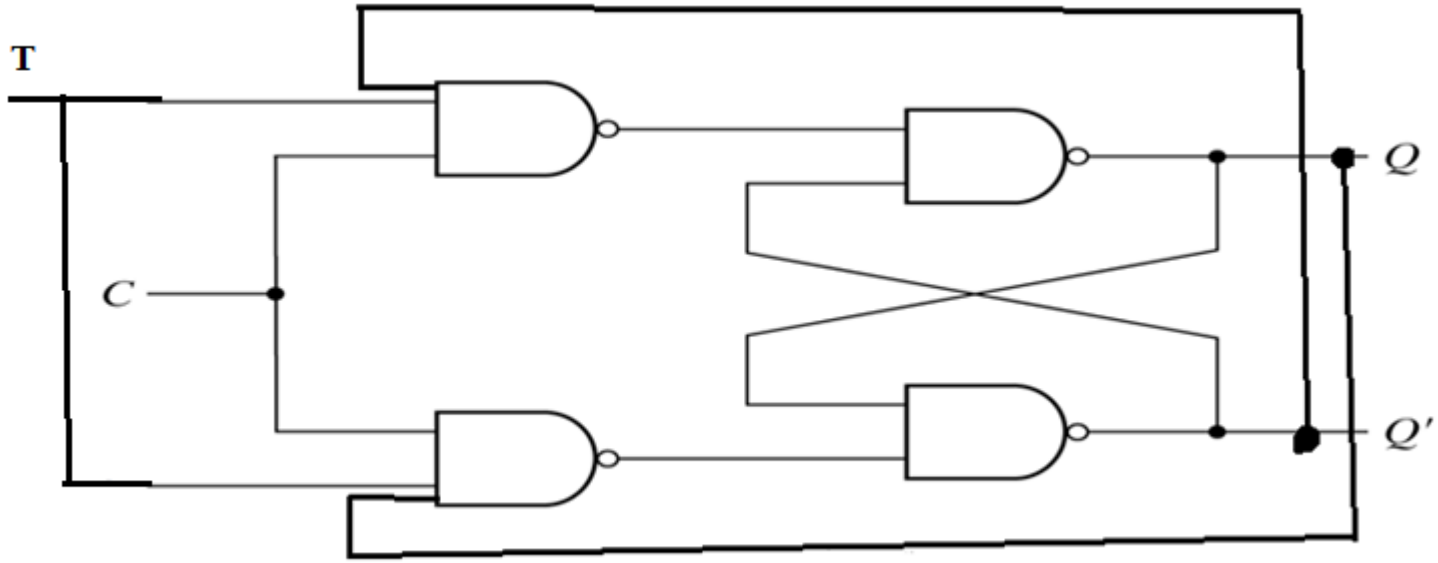
Conditions to overcome Race around condition

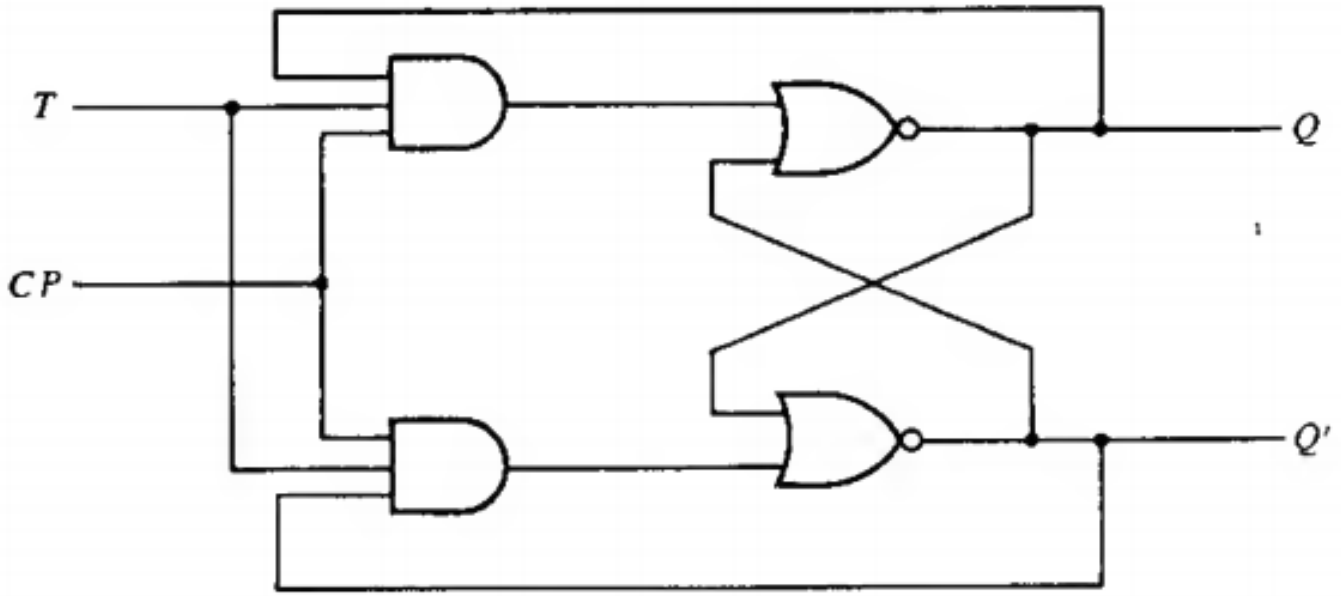
1. Instead of using level triggering use edge triggering

2. Master Slave JK flip flop

T Flip-Flop

If we want only Toggling operation then we call it T flip-flop, when J and K will always remain same .

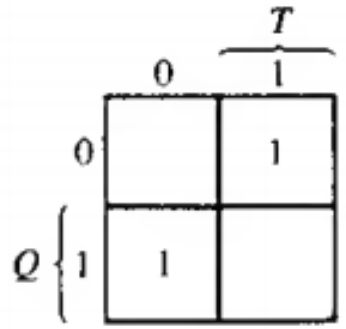




(a) Logic diagram

Q	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

(b) Characteristic table

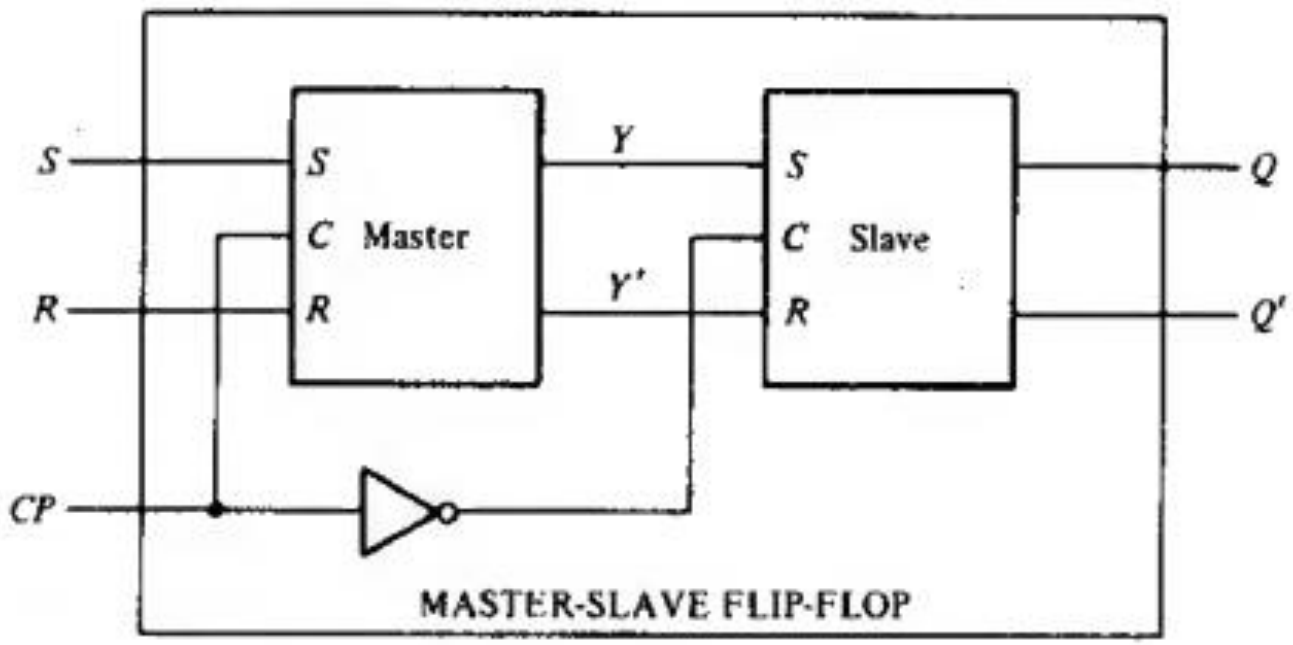


$Q(t+1) = TQ' + T'Q$

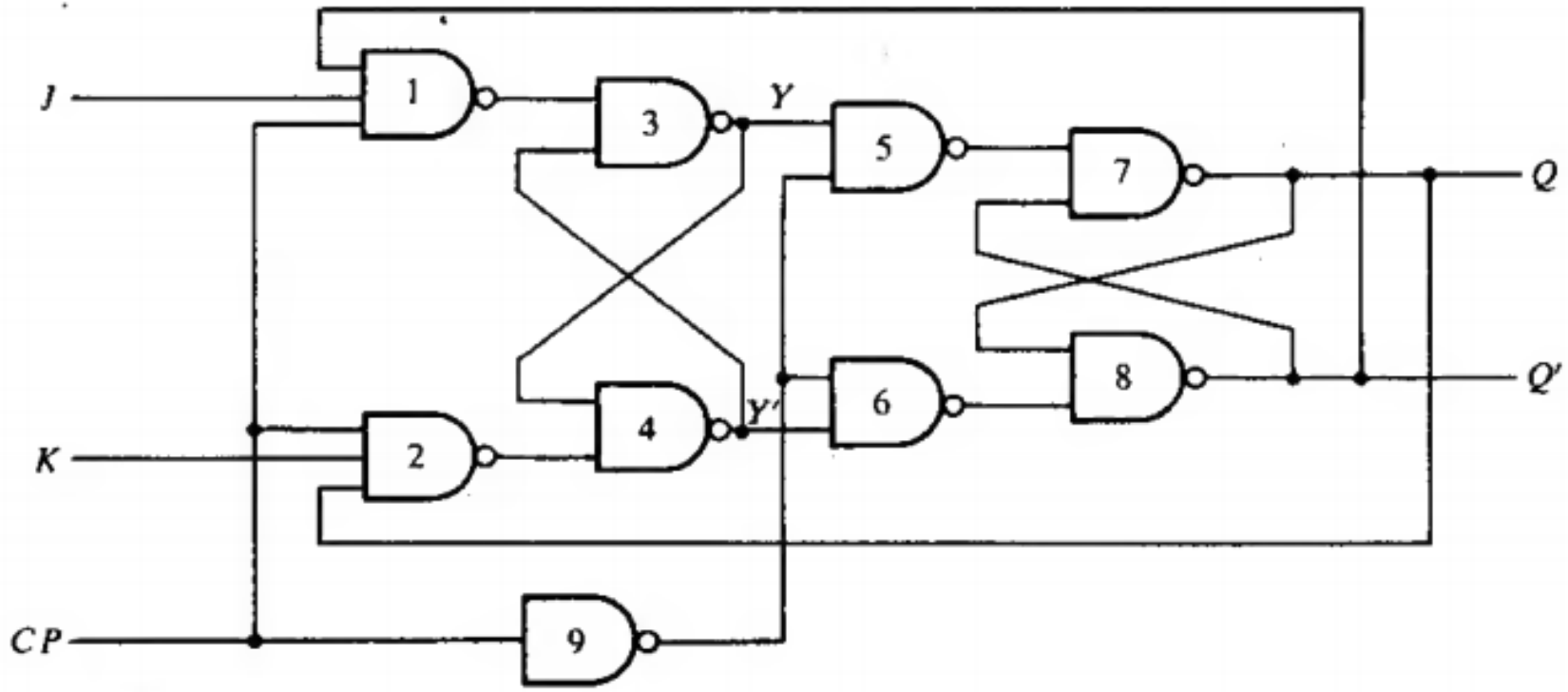
(c) Characteristic equation

Master- slave flip-flop

- A master- slave flip-flop is constructed from two separate flip-flops. One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a masterslave flip-flop.
- It consists of a master flip-flop, a slave flip-flop, and an inverter. When clock pulse CP is 0, the output of the inverter is 1 . Since the clock input of the slave is 1 , the flip-flop is enabled and output Q is equal to Y, while Q ’ is equal to Y‘ .
- The master flip-flop is disabled because CP = 0. When the pulse becomes 1, the information then at the external R and S inputs is transmitted to the master flip-flop.
- The slave flip-flop, however, is isolated as long as the pulse is at its 1 level, because the output of the inverter is 0.
  When the pulse returns to 0, the master flip-flop is isolated, which prevents the external inputs from affecting it.
- The slave flip-flop then goes to the same state as the master flip-flop.



Logic diagram of a master–slave flip-flop



Clocked master–slave *JK* flip-flop

- It is very important to realize that because of the feedback connection in the JK flipflop, a CP pulse that remains in the 1 state while both J and K are equal to 1 will cause the output to complement again and repeat complementing until the pulse goes back to 0.
- To avoid this undesirable operation, the clock pulse must have a time duration that is shorter than the propagation delay time of the flip-flop.
- This is a restrictive requirement, since the operation of the circuit depends on the width of the pulse.
- The restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.
- By removing the effect of feedback we can avoid racing. So output changes once in a clock cycle.

Suggested Reading

- M. Morris Mano, Digital Logic and Computer Design, PHI.

Thank you