Digital Logic and Circuit
Paper Code: CS-102

Outline

- **Sequential Circuit**
- **Latch**
- **Flip flops**

Cominational and Sequential Circuits

- Logic circuits for digital systems may be combinational or sequential .
- A combinational circuit consists of logic gates whose outputs at any time are determined directly from the present combination of inputs without regard to previous inputs.
- A combinational circuit performs a specific information-processing operation fully specified logically by a set of Boolean functions.
- Sequential circuits employ memory elements (binary cells) in addition to logic gates. Their outputs are a function of the inputs and the state of the memory elements.
- The state of memory elements, in turn, is a function of previous inputs. As a consequence, the outputs of a sequential circuit depend not only on present inputs, but also on past inputs, and the circuit behavior must be specified by a time sequence of inputs and internal states.

Block Diagram

Memory elements can store binary information

- This information at any given time determines the state of the circuit at that time

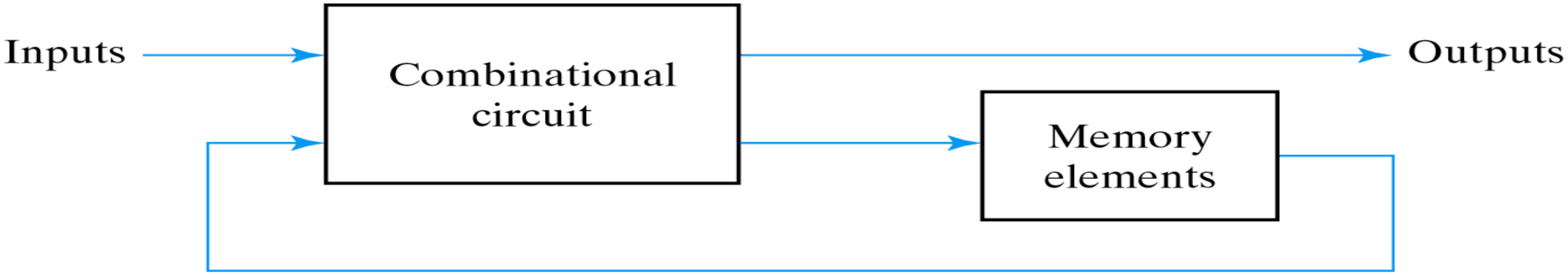


Fig. 5-1 Block Diagram of Sequential Circuit

- It consists of a combinational circuit to which memory elements are connected to form a feedback path.
- The memory elements are devices capable of storing binary information within them.
- The binary information stored in the memory elements at any given time defines the state of the sequential circuit.
- The sequential circuit receives binary information from external inputs.
- These inputs, together with the present state of the memory elements, determine the binary value at the output terminals. They also determine the condition for changing the state in the memory elements.

- The memory elements used in clocked sequential circuits are called flip-flops.
- These circuits are binary cells capable of storing one bit of information.
- A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the bit stored in it.
- Binary information can enter a flip-flop in a variety of ways, a feet that gives rise to different types of flip-flops.

Basic Flip-Flop Circuit

- a flip-flop circuit can be constructed from two NAND gates or two NOR gates.
- Each circuit forms a basic flip-flop upon which other more complicated types can be built.
- The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path.
- For this reason, the circuits are classified as asynchronous sequential circuits. Each flip-flop has two outputs, Q and Q', and two inputs, set and reset.
- This type of flip-flop is sometimes called a direct-coupled RS flip-flop, or SR latch. The R and S are the first letters of the two input names.

Flip-Flop

A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

The major differences among various types of flip-flops are in the number of inputs they possess and in the manner in which the inputs affect the binary state.

Types of Sequential circuit

There are two main types of sequential circuits: Synchronous and Asynchronous

Their classification depends on the timing of their signals.

Sequential Circuit Types

- Synchronous
  - The circuit behavior is determined by the signals at discrete instants of time
  - The memory elements are affected only at discrete instants of time
  - A clock is used for synchronization
    - Memory elements are affected only with the arrival of a clock pulse
    - If memory elements use clock pulses in their inputs, the circuit is called
      - Clocked sequential circuit

Sequential Circuit Types

ASynchronous

- The circuit behavior is determined by the signals at any instant of time
- It is also affected by the order the inputs change

Clock

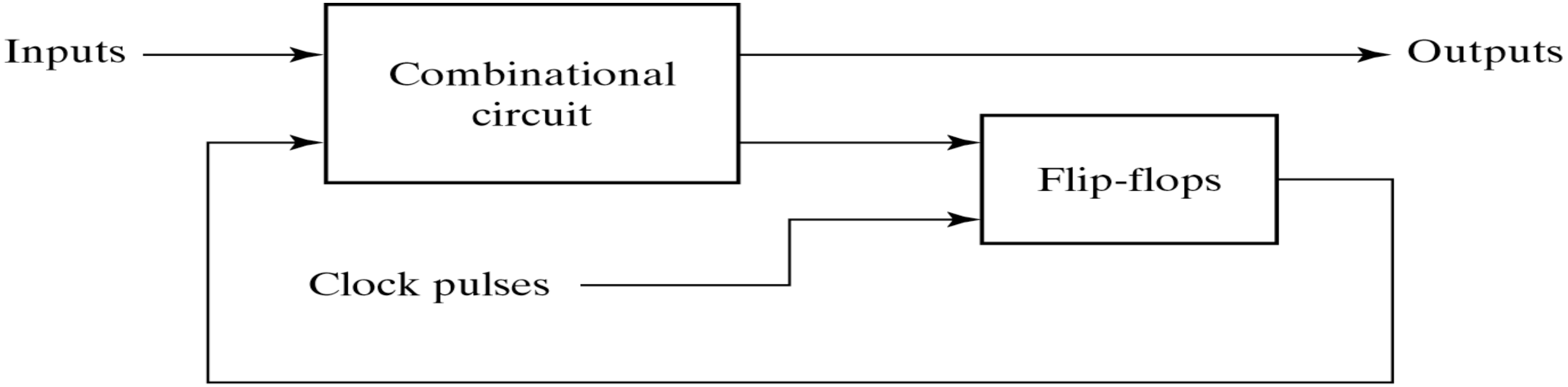
It emits a series of pulses with a precise pulse width and precise interval between consecutive pulses

Timing interval between the corresponding edges of two consecutive pulses is known as the clock cycle time, or period

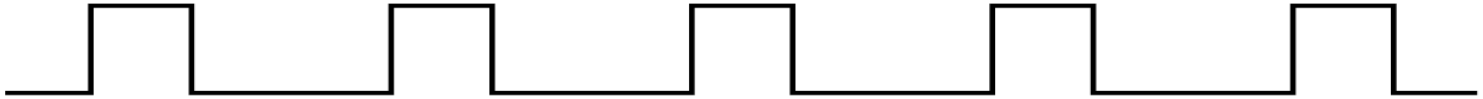
Flip-Flops

They are memory elements

They can store binary information



(a) Block diagram



(b) Timing diagram of clock pulses

Synchronous Clocked Sequential Circuit

Flip-Flops

Can keep a binary state until an input signal to switch the state is received

There are different types of flip-flops depending on the number of inputs and how the inputs affect the binary state

Latches

The basic storage element is called Latch. As the name suggests it latches ‘0’ or ‘1’.

The most basic flip-flops

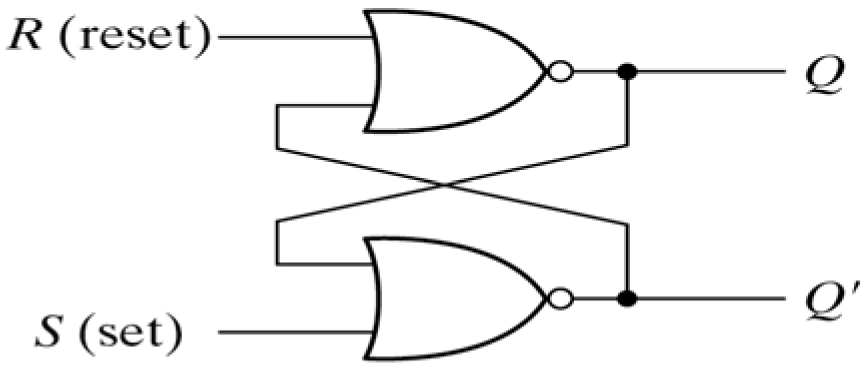
- They operate with signal levels (i/p)

The flip-flops are constructed from latches

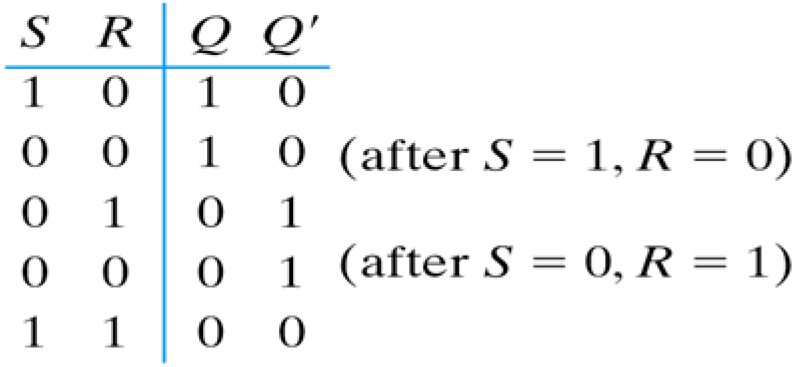
They are not useful for synchronous sequential circuits

They are useful for asynchronous sequential circuits

SR Latch with NOR



(a) Logic diagram



S	R	Q	Q'		
1	0	1	0		
0	0	1	0	(after $S = 1, R = 0$)	MEMORY
0	1	0	1		
0	0	0	1	(after $S = 0, R = 1$)	MEMORY
1	1	0	0		NOT ACCEPTABLE

(b) Function table

NOR TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

SR Latch with NOR

$S = set$

$R = reset$

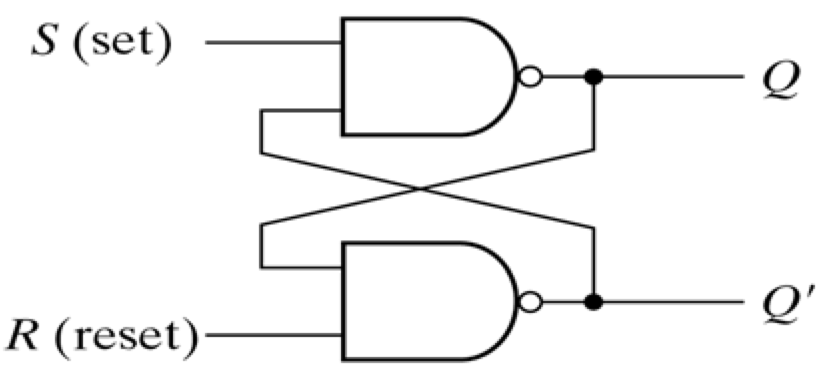
$Q = 1, \quad Q' = 0 \quad => \text{ set state}$

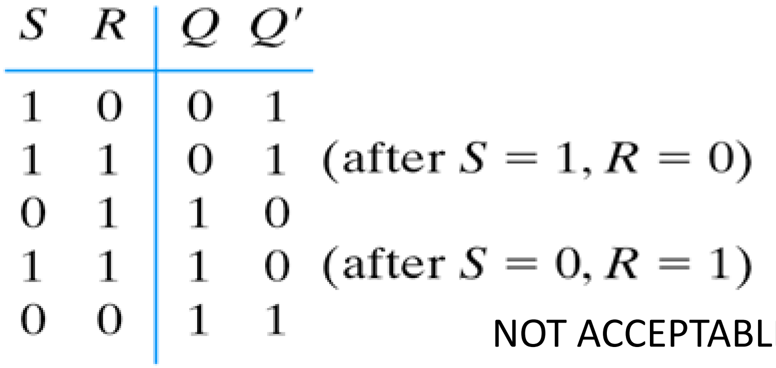
$Q = 0, \quad Q' = 1 \quad => \text{ reset state}$

$\mathrm{S} = 1, \quad \mathrm{R} = 1 \quad => \text{ undefined, Q and Q' are set to 0}$

$\text{In normal conditions, avoid S} = 1, \mathrm{R} = 1$

SR Latch with NAND





S	R	Q	Q'		
1	0	0	1		
1	1	0	1	(after $S = 1, R = 0$)	MEMORY
0	1	1	0		
1	1	1	0	(after $S = 0, R = 1$)	MEMORY
0	0	1	1		NOT ACCEPTABLE

(a) Logic diagram

(b) Function table

SR Latch with NAND Gates

NAND TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

SR Latch with NAND

$S = set$

$R = reset$

$Q = 0, \quad Q' = 1 \qquad => \text{ set state}$

$Q = 1, \quad Q' = 0 \qquad => \text{ reset state}$

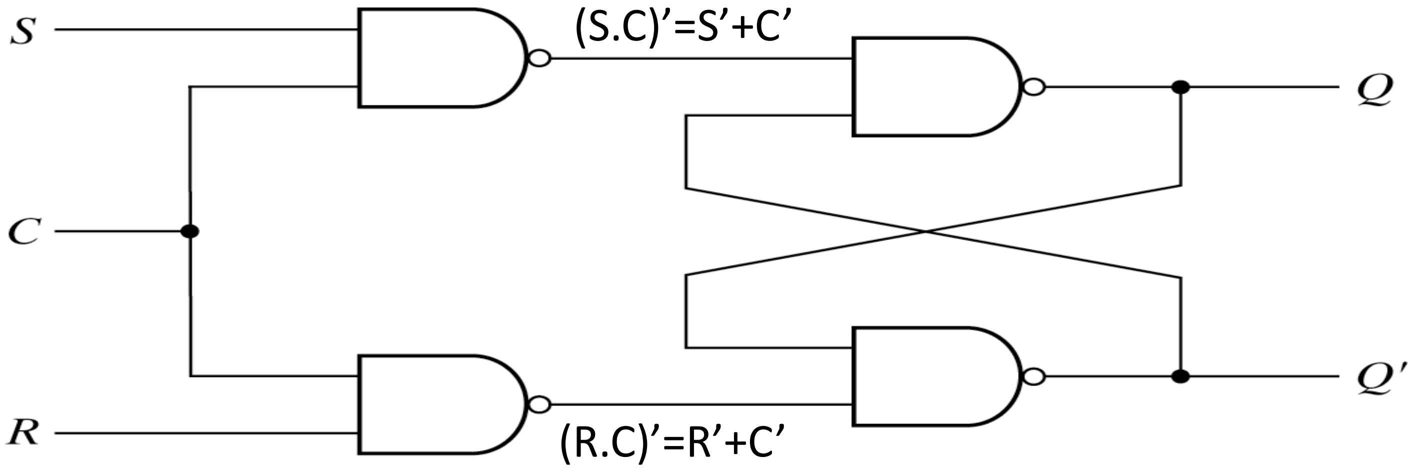
$\mathrm{S} = 0, \quad \mathrm{R} = 0 \qquad => \text{ undefined, Q and Q' are set to1}$

$\text{In normal conditions, avoid S} = 0\text{, R} = 0$

SR Latch with Control Input

NAND Latch

S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1



(S.C)'=S'+C'

(R.C)'=R'+C'

(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

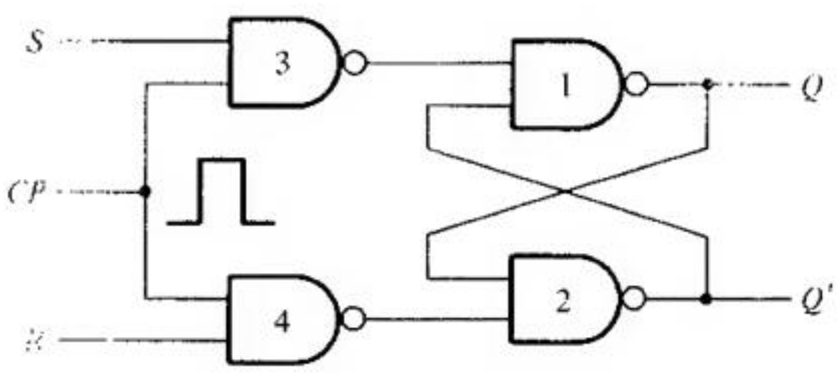
(b) Function table

SR Latch with Control Input

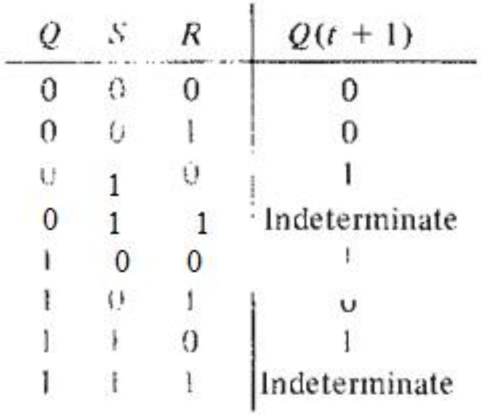
NAND TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

We want to change the input when it is required

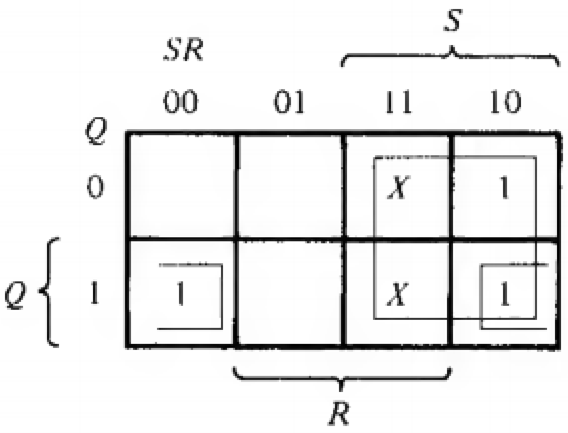


(a) Logic diagram



Q	S	R	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

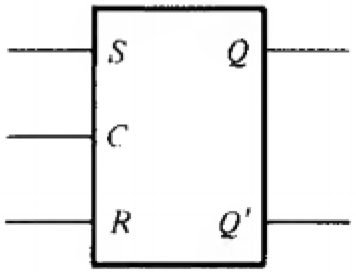
(b) Characteristic table



Q \ SR	00	01	11	10
0			X	1
1	1		X	1

$$Q(t+1) = S + R'Q$$
$$SR = 0$$

(c) Characteristic equation



(d) Graphic symbol

NAND TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

D Flip Flop

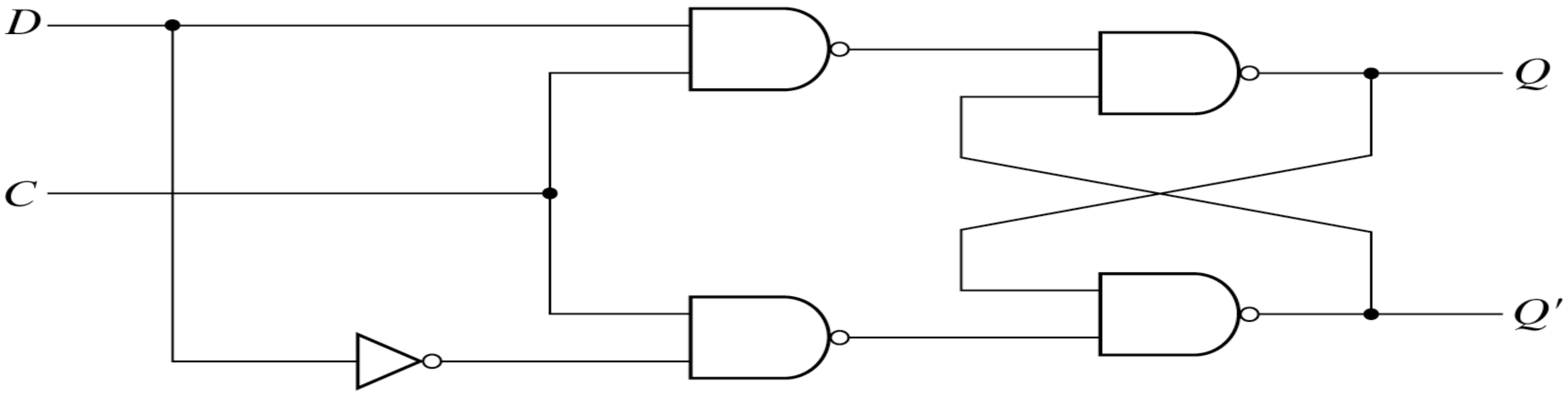
One way to eliminate the undesirable condition of the indeterminate state in the RS flipflop is to ensure that inputs S and R are never equal to 1 at the same time.

The D flip-flop has only two inputs: D and CP

.

The D input goes directly to the S input and its complement is applied to the R input.

D Flip Flop



(a) Logic diagram

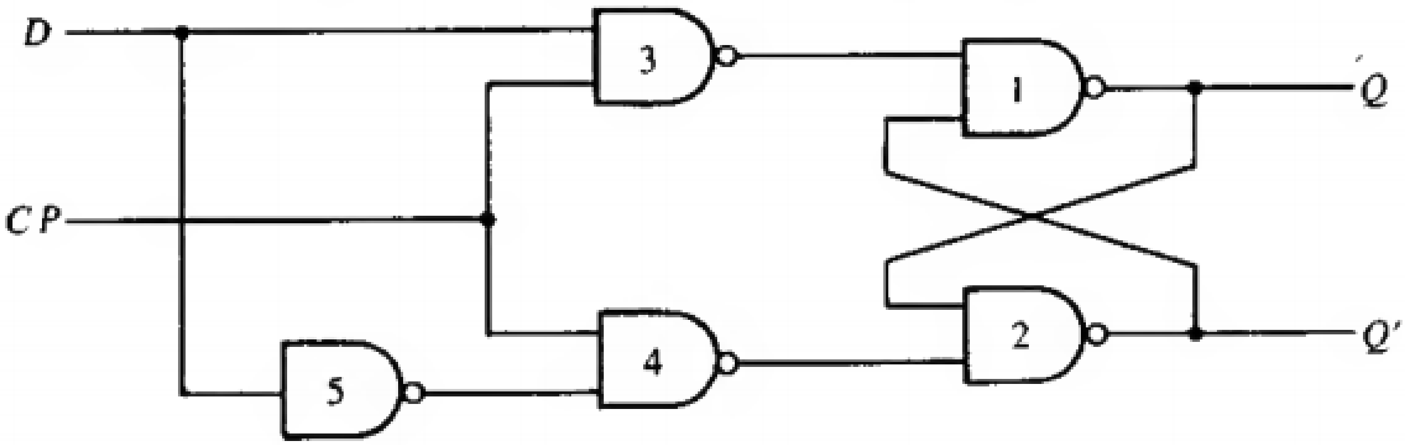
C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

(b) Function table

D Latch

NAND TABLE

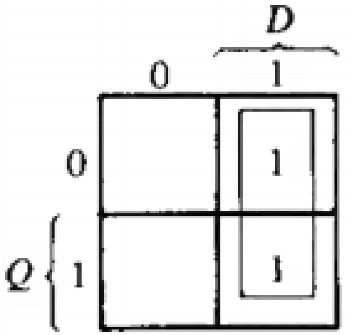
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



(a) Logic diagram

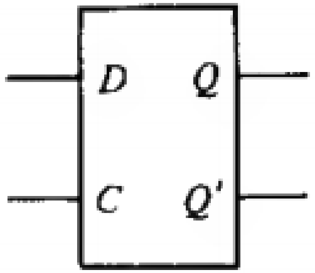
Q	D	$Q(t+1)$
0	0	0
0	1	1
1	0	0
1	1	1

(b) Characteristic table



$Q(t+1) = D$

(c) Characteristic equation



(d) Graphic symbol

Note

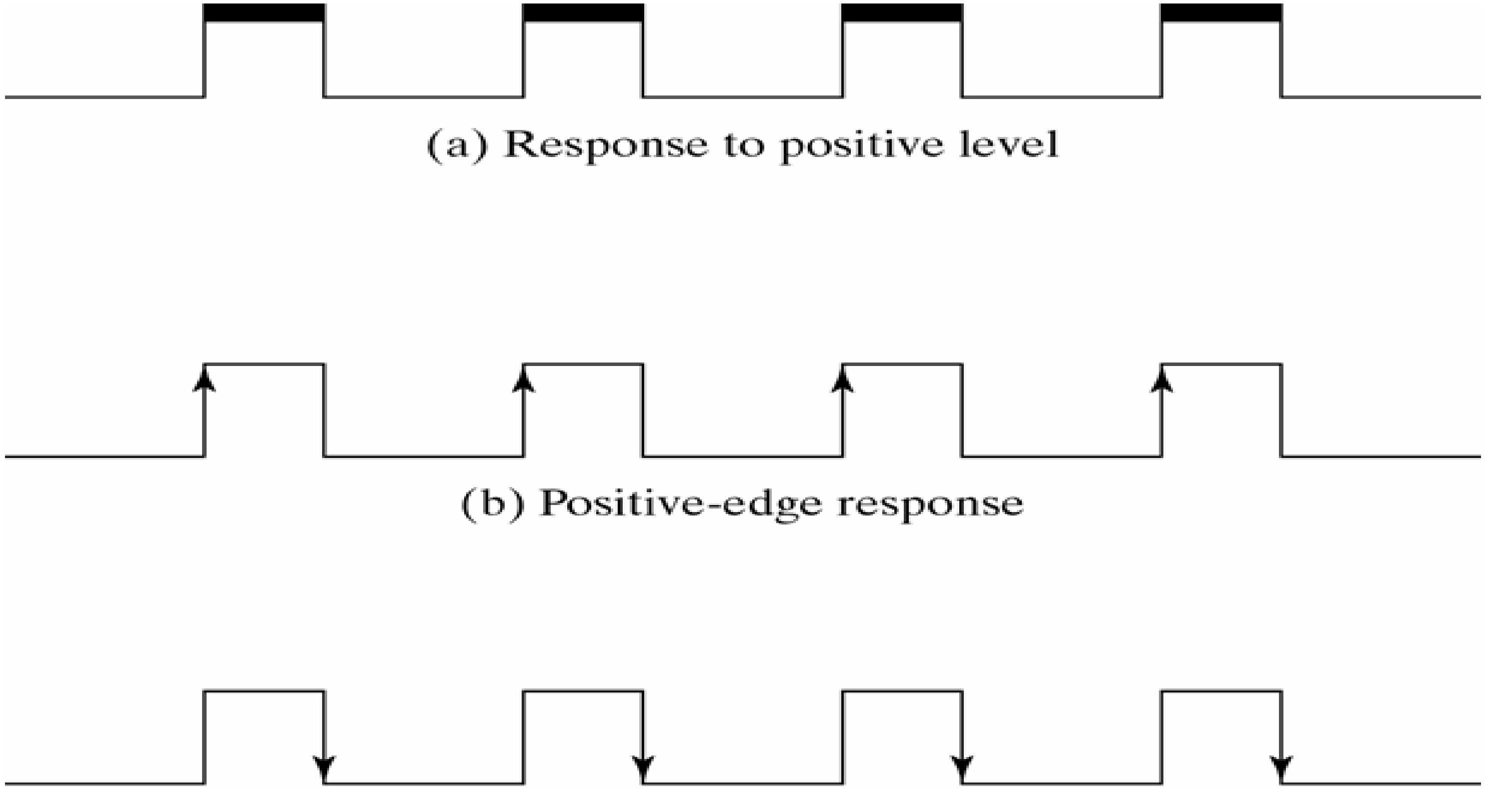
- The control input changes the state of a latch or flip-flop
- The momentary change is called a trigger

Example: D Latch

- It is triggered every time the pulse goes to the logic level 1
- As long as the pulse remains at the logic level 1, the change in the data (D) directly affects the output (Q)
- THIS MAY BE A BIG PROBLEM since the state of the latch may keep changing depending on the input (may be coming from a combinational logic network)

How to Solve?

Trigger the flip-flop only during a signal transition



(a) Response to positive level

(b) Positive-edge response

(c) Negative-edge response

Clock Response in Latch and Flip-Flop

Suggested Reading

❑ M. Morris Mano, Digital Logic and Computer Design, PHI.

Thank you