Digital Logic and Circuit
Paper Code: CS-102

Outline

Combinational circuit

- **Multiplexers & de-multiplexers**
- Combinational Logic Implementation

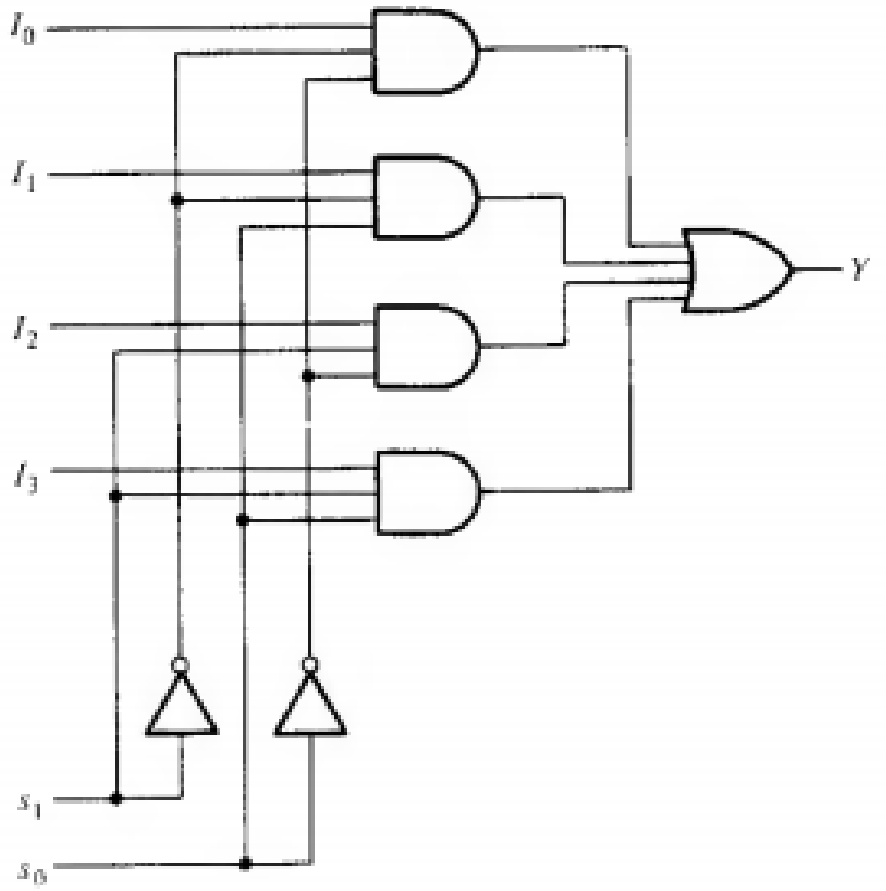
Multiplexer

- A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.

- The selection of a particular input line is controlled by a set of selection lines.

- Normally, there are 2" input lines and n selection lines whose bit combinations determine which input is selected.

- A 4-to- 1 -line multiplexer is shown in the Figure.
- Each of the four input lines, I_0 to I_3, is applied to one input of an AND gate.
- Selection lines S_1 and S_0 are decoded to select a particular AND gate.



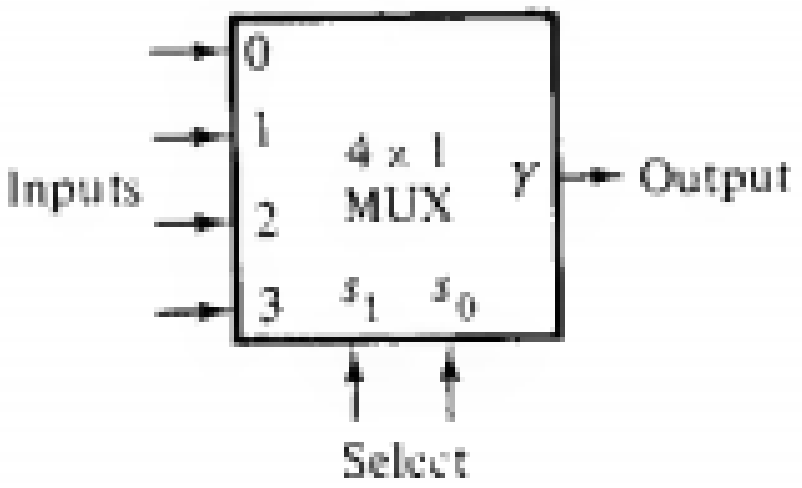
(a) Logic diagram

- The function table lists the input-to-output path for each possible bit combination of the selection lines.

s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

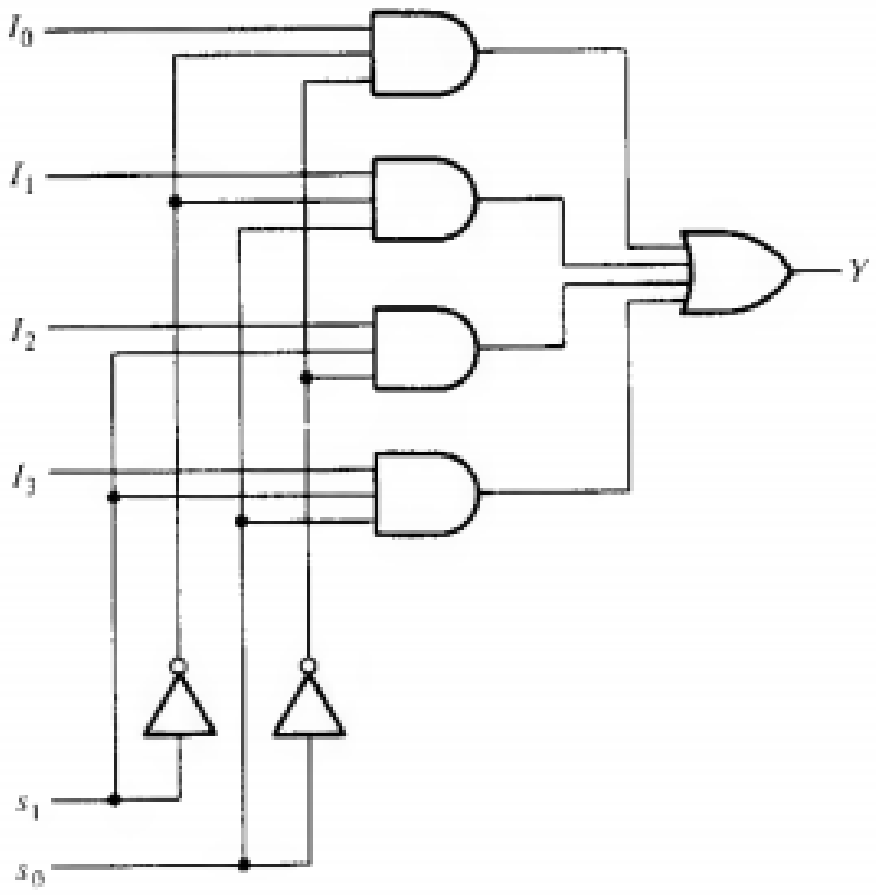
(b) Function table

- When this MSI function is used in the design of a digital system, it is represented in block diagram form, as shown in Figure (c)



(c) Block diagram

- To demonstrate the circuit operation, consider the case when $S_1S_0 = 10$.
- The AND gate associated with input I_2 has two of its inputs equal to 1 and the third input connected to I_2 .
- The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0.
- The OR gate output is now equal to the value of I_2 , thus providing a path from the selected input to the output.
- A multiplexer is also called a data selector, since it selects one of many inputs and steers the binary information to the output line. A multiplexer is often abbreviated as MUX.



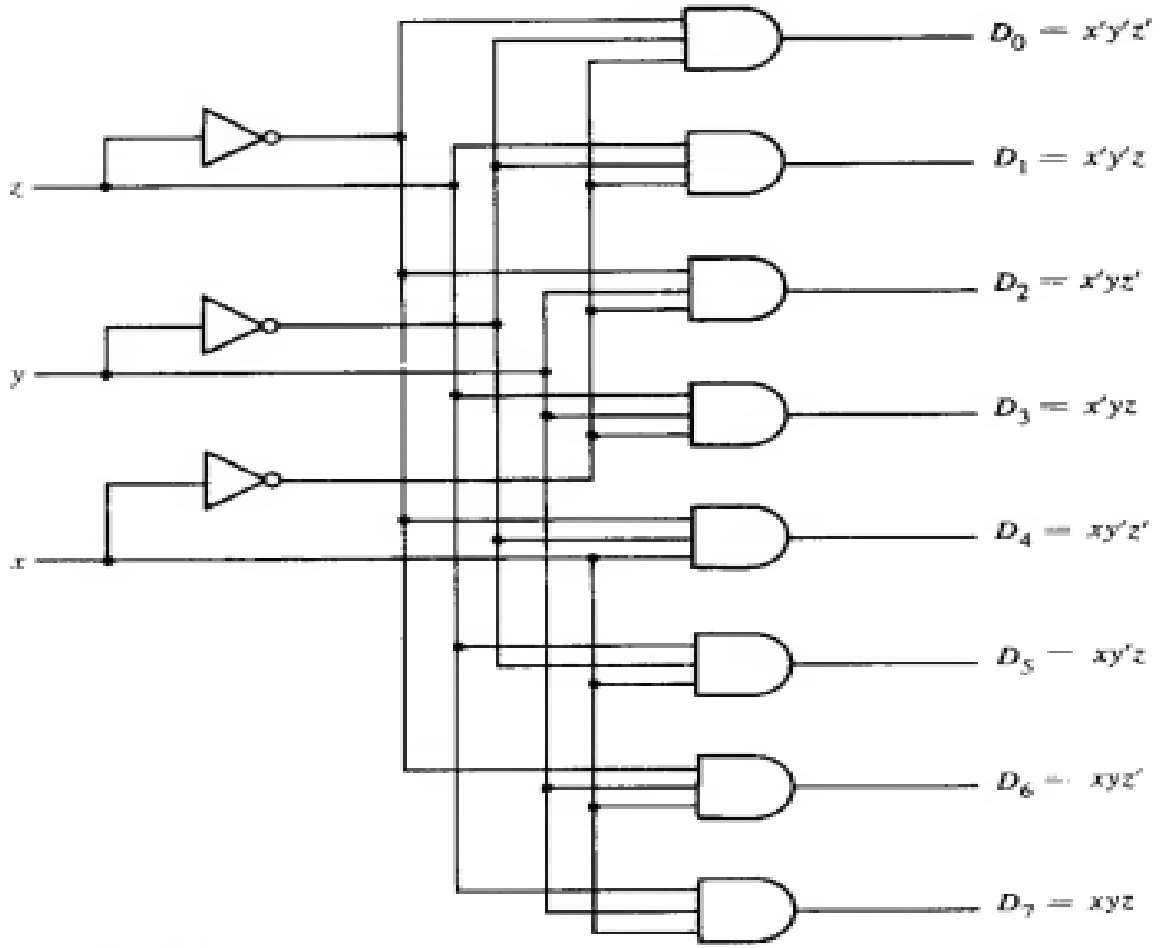
(a) Logic diagram

DECODERS

- A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.
- If the n-bit decoded information has unused or don't-care combinations, the decoder output will have fewer than 2^n outputs.
- The decoders presented here are called n-to-m-line decoders, where $m \leq 2^n$.
- Their purpose is to generate the 2^n (or fewer) minterms of n input variables.
- The name decoder is also used in conjunction with some code converters such as a BCD-to-seven segment decoder.

Truth Table of a 3-to-8-Llne Decoder

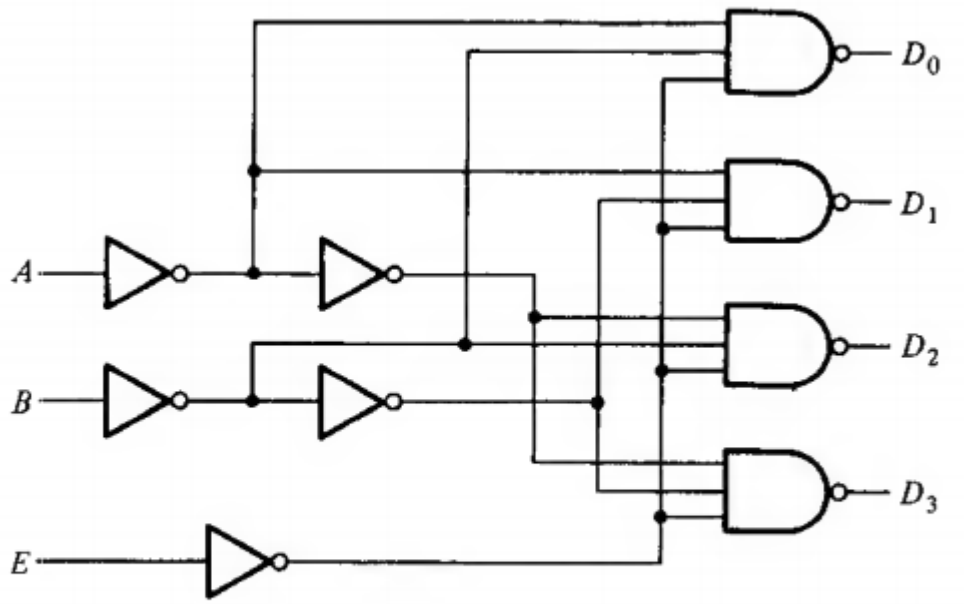
Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1


z
y
x
$D_0 = x'y'z'$
$D_1 = x'y'z$
$D_2 = x'yz'$
$D_3 = x'yz$
$D_4 = xy'z'$
$D_5 = xy'z$
$D_6 = xyz'$
$D_7 = xyz$

Decoder with enable input

- Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form.

- Most, if not all, IC decoders include one or more enable inputs to control the circuit operation.



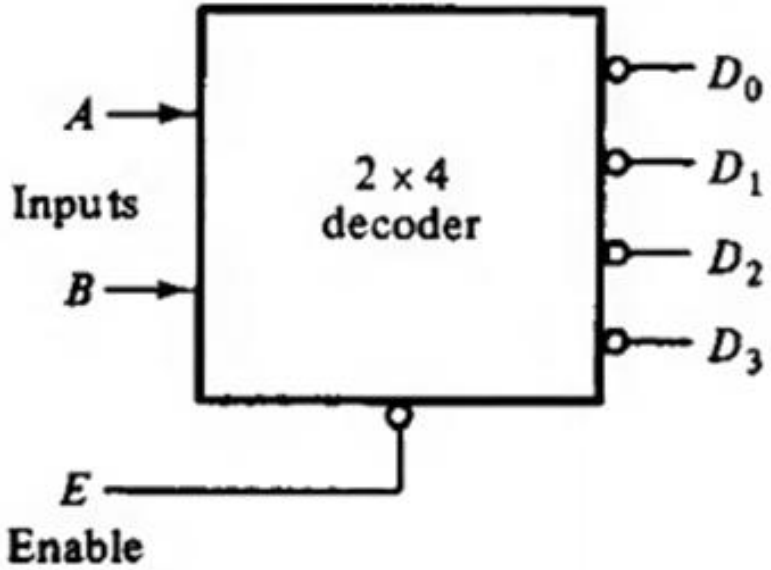
(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

A 2-to-4-line decoder with enable (E) input

Block diagram of decoder with Enable

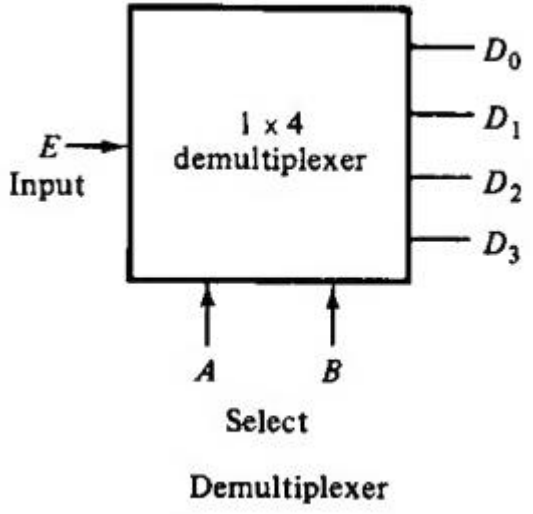


(a) Decoder with enable

- A 2-to-4-line decoder with an enable input constructed with NAND gates.
- All outputs are equal to 1 if enable input E is 1 , regardless of the values of inputs A and B. When the enable input is 0, the circuit operates as a decoder with complemented outputs.
- The truth table lists these conditions. The X's under A and B are don't-care conditions.
- Normal decoder operation occurs only with E = 0, and the outputs are selected when they are in the 0 state.

De-multiplexer

- A decoder with an enable input can function as a demultiplexer.
- A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2” possible output lines.
- The selection of a specific output line is controlled by the bit values of n selection lines.
- The decoder can function as a demultiplexer if the E line is taken as a data input line and lines A and B are taken as the selection lines.



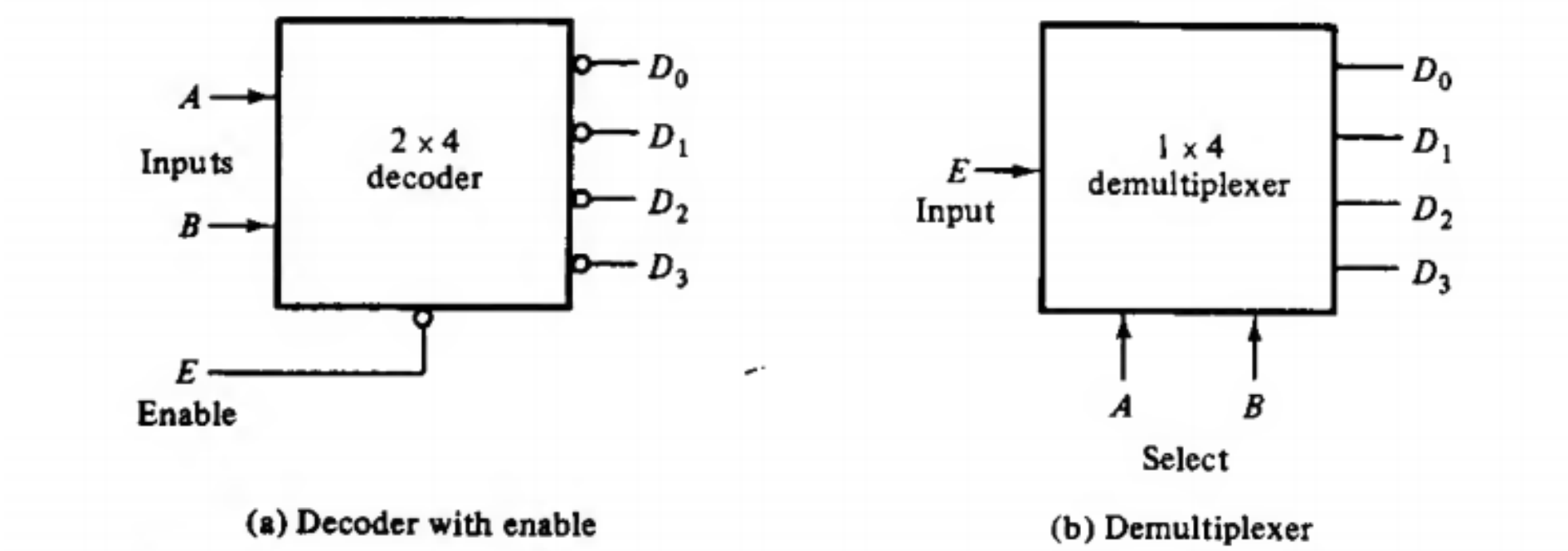
Demultiplexer

- The single input variable E has a path to all four outputs, but the input information is directed to only one of the output lines, as specified by the binary value of the two selection lines, A and B.
- This can be verified from the truth table of this circuit.
- For example, if the selection lines AB = 10, output D2 will be the same as the input value E, while all other outputs are maintained at 1 .
- Because decoder and demultiplexer operations are obtained from the same circuit, a decoder with an enable input is referred to as a decoder/demultiplexer.
- It is the enable input that makes the circuit a demultiplexer.

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

Block diagram of decoder with Enable

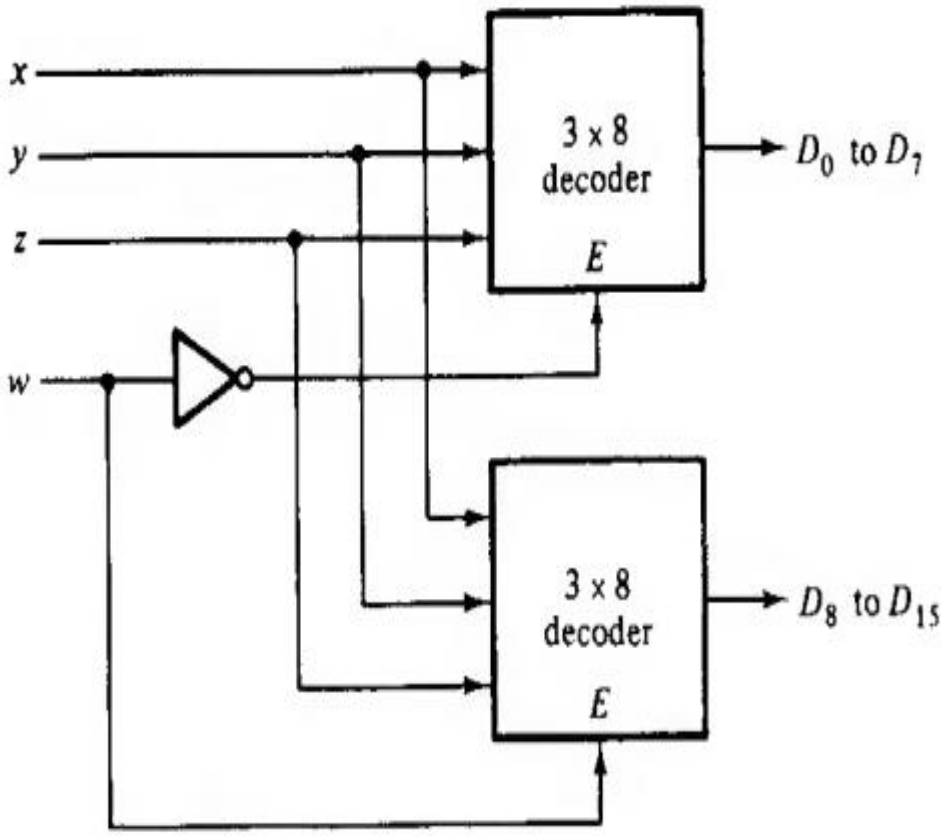


(a) Decoder with enable

(b) Demultiplexer

- Decoder/demultiplexer circuits can be connected together to form a larger decoder circuit.

- two 3x8 decoders with enable inputs connected to form a 4 x 16 decoder.
- When w = 0, the top decoder is enabled and the other is disabled.
- The bottom decoder outputs are all 0's, and the top eight outputs generate minterms 0000 to 0111.
- When w = 1, the enable conditions are reversed; the bottom decoder outputs generate minterms 1000 to 1111, while the outputs of the top decoder are all 0's.
- This example demonstrates the usefulness of enable inputs in ICs. In general, enable lines are a convenient feature for connecting two or more IC packages for the purpose of expanding the digital function into a similar function with more inputs and outputs.



A 4 × 16 decoder constructed with two 3 × 8 decoders

Combinational Logic Implementation

- A decoder provides the 2" minterm of n input variables.
- Since any Boolean function can be expressed in sum of minterms canonical form, one can use a decoder to generate the minterms and an external OR gate to form the sum.
- In this way, any combinational circuit with n inputs and m outputs can be implemented with an n-to-2"-line decoder and m OR gates.
- The procedure for implementing a combinational circuit by means of a decoder and OR gates requires that the Boolean functions for the circuit be expressed in sum of minterms.
- A decoder is then chosen that generates all the minterms of the n input variables.
- The inputs to each OR gate are selected from the decoder outputs according to the minterm list in each function.

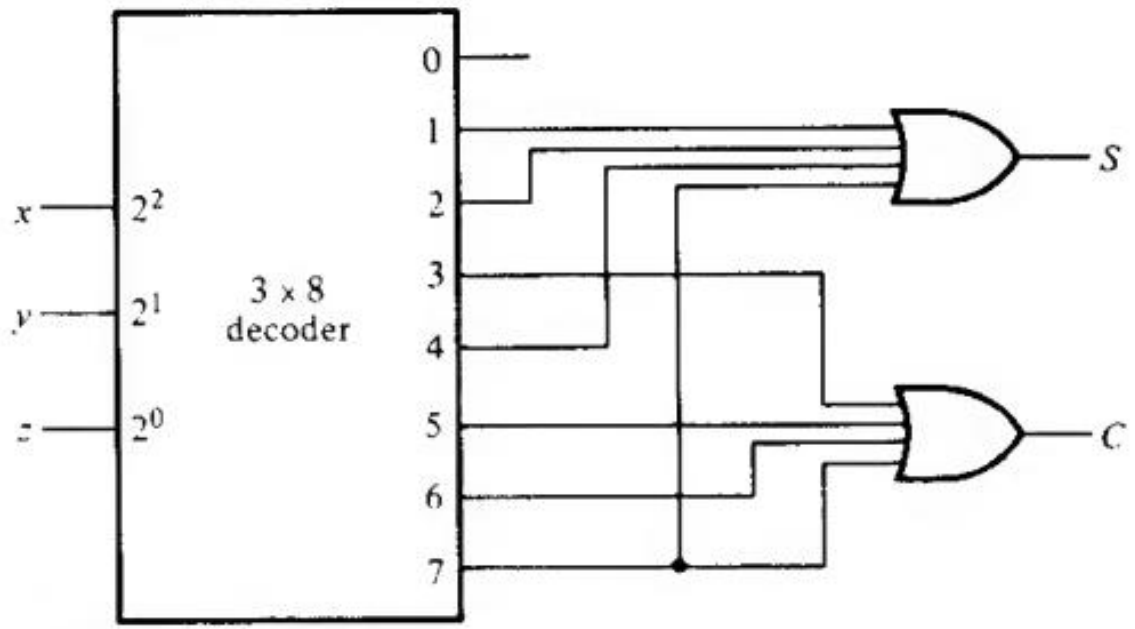
Implement a full-adder circuit with a decoder and two OR gates.

From the truth table of full-adder, we have,

$S(x, y, z) = \sum(1,2, 4, 7)$
$C(x, y, z) = \sum(3, 5, 6, 7)$

Since there are three inputs and a total of eight minterms, we need a 3-to-8-line decoder.

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Implementation of a full-adder with a decoder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Implement full subtractor using decoder

Suggested Reading

- M. Morris Mano, Digital Logic and Computer Design, PHI.

Thank you