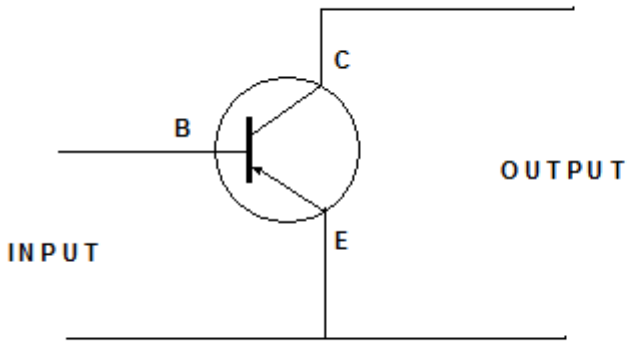
Transistor Biasing and bias stabilization

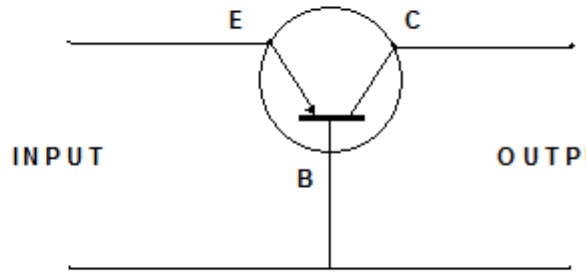
BPT: 401: Electronics and Modern Physics

Tutorial – 12

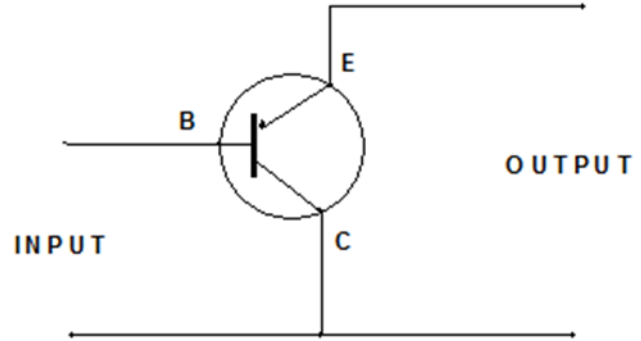
Comparison of BJT Configurations



COMMON EMITTER



COMMON BASE



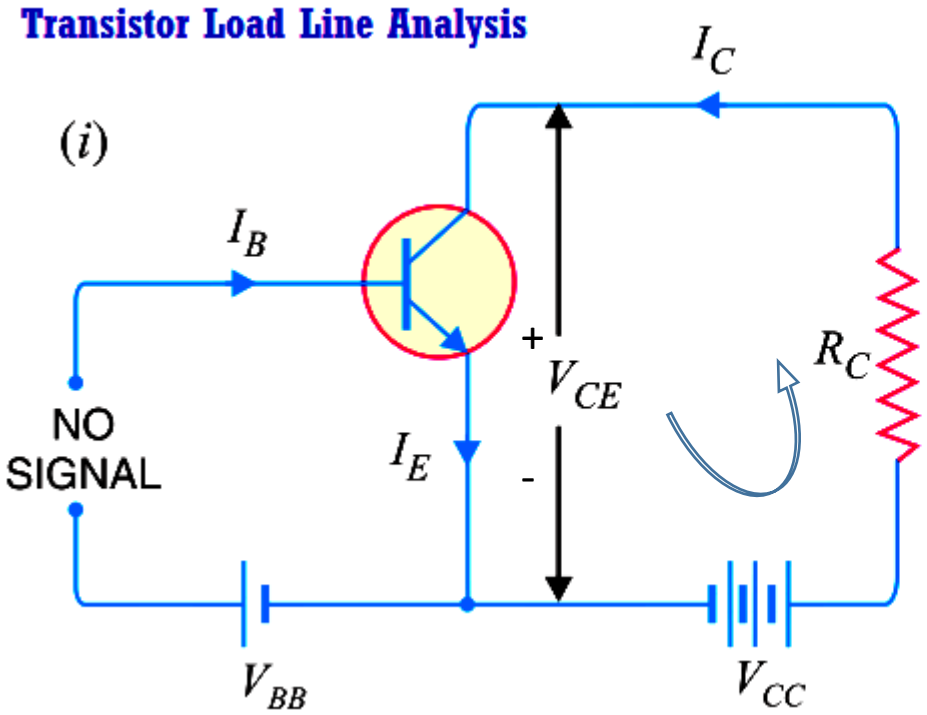
COMMON COLLECTOR

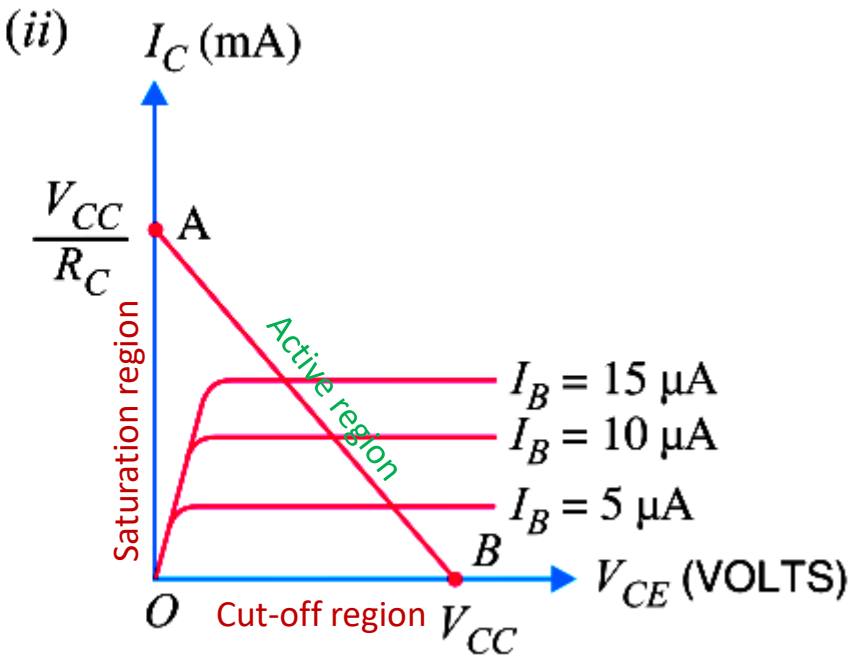
S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

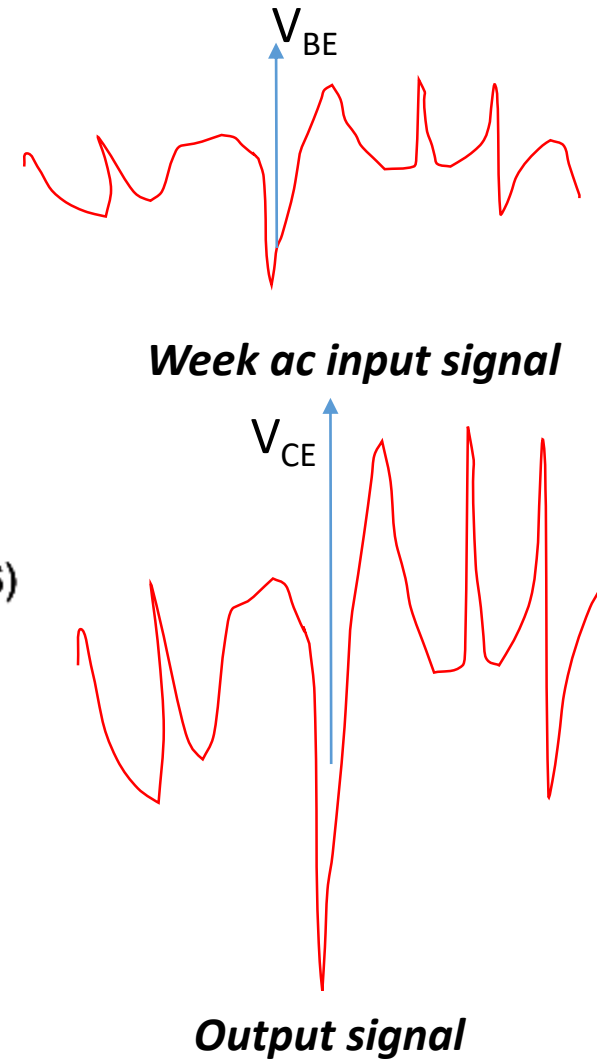
Sr. No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1KΩ)	High (500 KΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 KΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output cufrrent	I_C	I_C	I_E
5.	Input votage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Less than unity
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

DC load line of Transistor

DC load line of a transistor is a straight line joining cut-off & saturation points.







Using KVL in O/P loop **$V_{CC} - I_C R_C - V_{CE} = 0$**

Consider two cases:

Case (i): When $V_{CE} = 0$, then **$I_C = V_{CC}/R_C$ (Saturation point A)**

Case (ii): When $I_C = 0$, then **$V_{CE} = V_{CC}$ (Cut-off point B)**

The DC load line can be drawn if only V_{CC} and R_C are known. Slope of the load line AB = $-1/R_C$.

Operating regions and biasing conditions

Region of Operation	Emitter Base Junction	Collector Base Junction
Cut-off	Reverse biased	Reverse biased
Active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased

Bias Point (Q-Point)

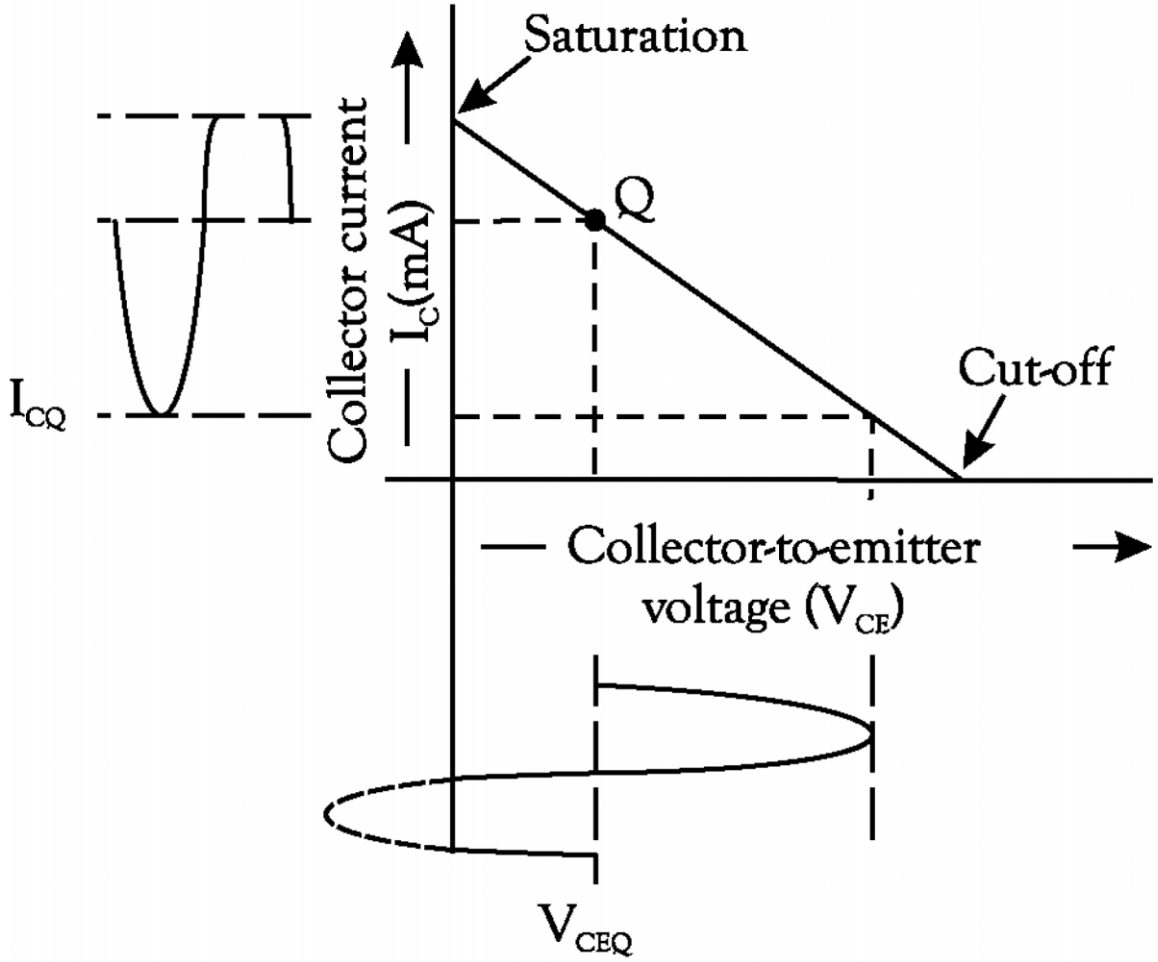
- It is a point on the DC load line, which represents the values of I_C and V_{CE} that exist in a transistor circuit when no input signal is applied. It is also known as the dc operating point or working point for faithful amplification of input ac signals.

- The best position for Q-point is mid-way between cut-off and saturation points where V_{CE} = ½ V_{CC}

- There are three cases for positioning Q-point:

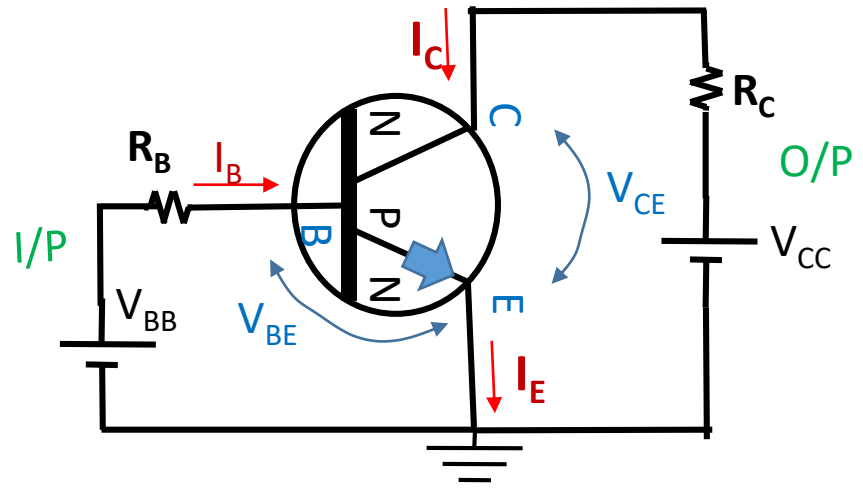
Bias Point (Q-Point)

Case (i): If the Q point is fixed near saturation point of the DC load line, then, during the negative half-cycle of the input signal, the transistor is driven into saturation. As a result, the negative peak of the input signal is clipped at output as shown in Fig.



Q-point is fixed near saturation point of the DC load line

The negative half-cycle of the
input signal causes the input junction, J1 in rever



$$V_{CC} - I_C R_C - V_{CE} = 0$$

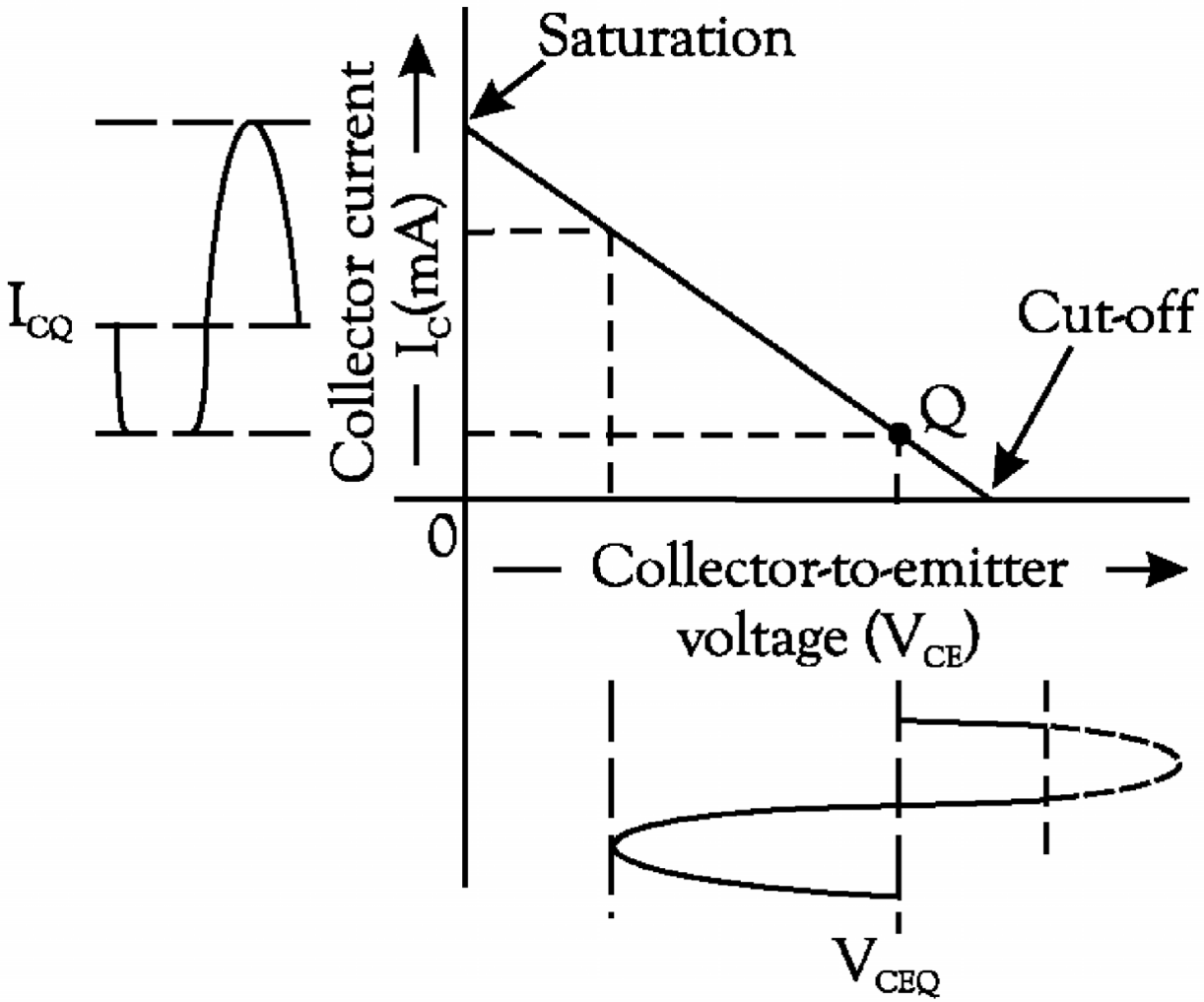
$$V_{CE} = V_{CC} - I_C R_C$$

V_{CC} → Reverse bias voltage (fixed) $I_C = \beta I_B$

The small increase in I_B causes a large increase in I_C as a result V_{CE} goes towards negative value

Bias Point (Q-Point)

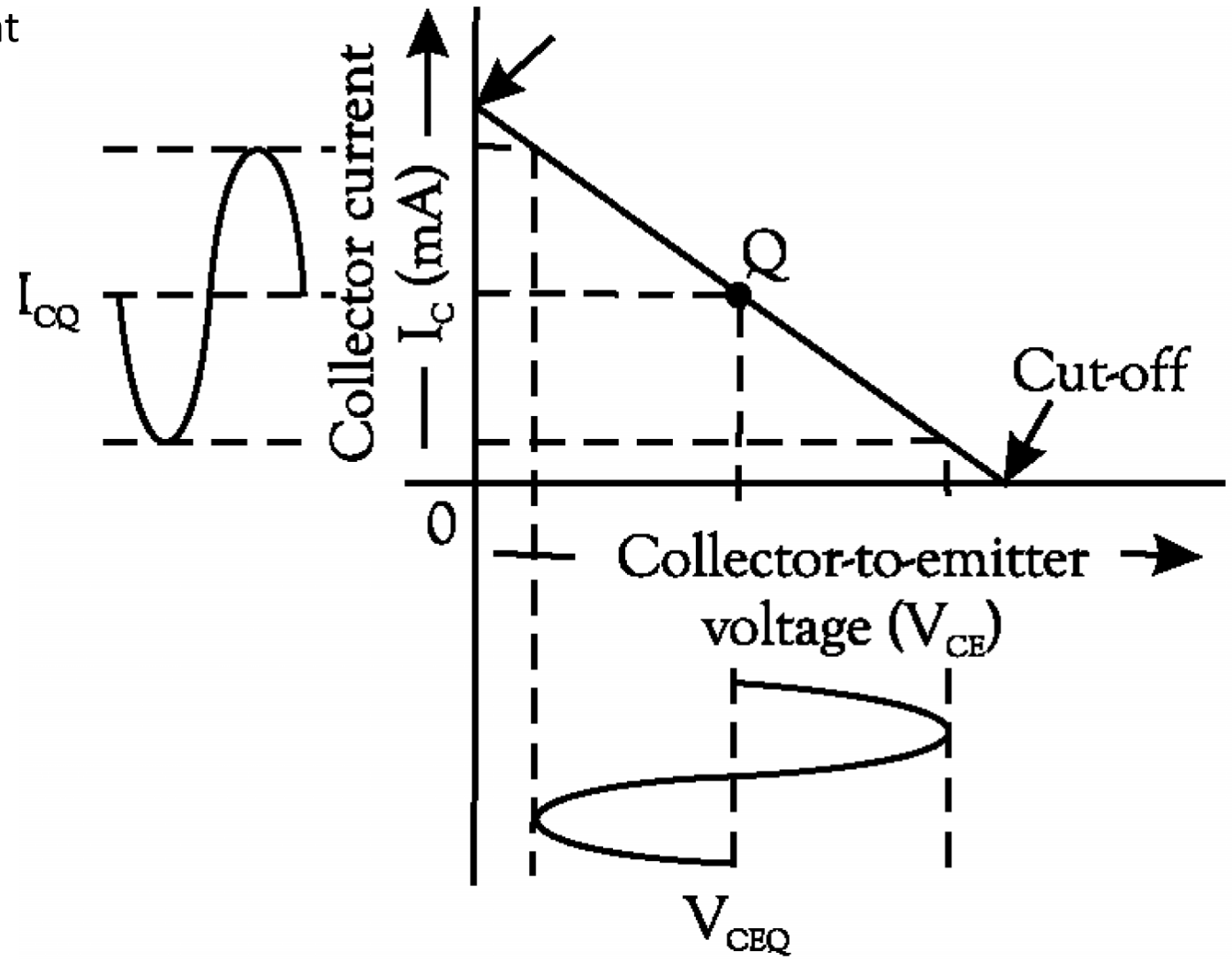
Case (ii): If the Q point is fixed near cut-off point of the DC load line, then, during the positive half-cycle of the input signal, the transistor is driven into cut-off. As a result, the negative peak of the input signal is clipped at output as shown in Fig.



Q-point is fixed near cut-off point of the DC load line

Bias Point (Q-Point)

Case (iii): If the Q-point is fixed at the centre of the DC load line by proper bias, as shown in Fig, we get undistorted signal at



Q-point is fixed at the centre of the DC load line

Factors Affecting Stability of Q-Point

It is found that even after the suitable selection of Q-point, it tends to shift from its position. It happens because of the following two reasons :

1. **Inherent variations of transistor parameters:**

   We know that the collector current for a common-emitter transistor amplifier is given by the relation,

$$I_C = \beta.I_B + (I + \beta).I_{CO}$$

   In the above equation the variables **β**, $\mathbf{I_B}$ and $\mathbf{I_{CO}}$ are found to be strongly dependent upon temperature. As the temperature increases, all the three variables also increase. This results in the increase of collector current and hence causes the operating point to shift towards the saturation point, resulting in clipping and bad distortion of the output. In some cases, a transistor may even burn out due to excessive collector current. But this problem can be solved by designing proper bias stabilization circuits.

2. **Variation in parameter values of transistors of the same type:**

   When the transistor is replaced by similar type due to aging, results fluctuation in specified parameters of the transistors provided by the manufacturer in the data sheet. This fluctuation gives rise to instability of the Q-point.

Stability Factor

The stability factor may be defined as the rate of change of collector current (I_C) with respect to the reverse saturation current (I_{CO}) keeping the common-emitter current gain (β) and base current (I_B) as constant.

Mathematically, the stability factor is given by the relation, $\mathbf{S = dI_C/dI_{CO}}$

The stability factor is a measure of bias stability of a transistor circuit. A higher value of stability factor indicates poor stability, whereas a lower value indicates good stability. If the rate of change of collector current (dI_C) is equal to the rate of change of reverse saturation current (I_{CO}), then the value of stability factor is unity (one). The unity is the lowest value of stability factor. If the value of stability factor is closer to the unity, the variation of collector current with the temperature will be less. Therefore, there will be less variation in the Q-point. The stability factor may also be expressed alternatively by using the relationship between base current (I_B), collector current (I_C) and reverse saturation current (I_{CO}). We know that the value of collector current in a transistor is given by the relation,

$$I_C = \beta . I_B + (1 + \beta) I_{CO}$$

Differentiating the above expression with respect to I_C,

$$1 = \frac{d(\beta I_B)}{dI_C} + \frac{d(1+\beta) I_{CO}}{dI_C}$$

$$= \beta \times \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{CO}}{dI_C} \quad \ldots \text{(Assuming } \beta \text{ as constant)}$$

$$= \beta \times \frac{dI_B}{dI_C} + (1+\beta)\frac{1}{S} \quad \ldots \left(\because \quad S = \frac{dI_C}{dI_{CO}}\right)$$

$$S = \frac{1+\beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

This expression can be used to determine the stability factor (S) of any biasing circuit

Stability Factor

(1) Stability Factor of Common Base Circuit

The collector current of a transistor in common base configuration, is given by the relation, $I_C = \alpha . I_E + I_{CO}$

Differentiating this equation with respect to I_{CO}, $\frac{dI_C}{dI_{CO}} = 0 + 1$

The value of stability factor indicates that the common base circuits are highly stable. Thus there is no need of bias stabilization in these circuits.

(2) Stability Factor of Common Emitter Circuit:

The collector current of a transistor in common emitter configuration is given by the relation,

$$I_C = \beta . I_B + (1 + \beta) I_{CO}$$

Differentiating this equation with respect to I_{CO}, $\frac{dI_C}{dI_{CO}} = 0 + (1 + \beta)$ or $S = 1 + \beta$

In CE circuit, if **β** = 100, then the value of S = 1 + 100 = 101. It means that the collector current changes 101 times the change in reverse saturation current. This means that the collector current is highly dependent upon the reverse saturation current and hence upon the temperature. Thus there is a strong need to provide bias stabilization in common emitter circuits to improve the stabilization factor.

Transistor Biasing

The process of energizing the transistor to amplify input a.c. signal such that the fluctuations in ac signal should not drive the transistor to either cut-off or saturation region is called **biasing**.
Biasing is setting up a Q-point of the transistor near the middle of the dc load line.

Need of Biasing

Proper biasing is required for providing following two conditions :

1. To keep the Emitter-Base junction forward biased and Collector-Base junction reverse biased during the entire cycle of input signal.
2. To stabilize the Q-point against the changes in temperature, variations in transistor parameters, aging of the components etc.

The first condition will ensure the linear operation of transistor and hence flow of proper collector current (I_C), proper value of V_{BE} (0.7 V for Si transistor and 0.3 V for Ge transistor), and proper value of V_{CE} (1 V for Si & 0.5 V for Ge transistor). The second condition will protect the transistor from thermal runaway.

Methods of Biasing

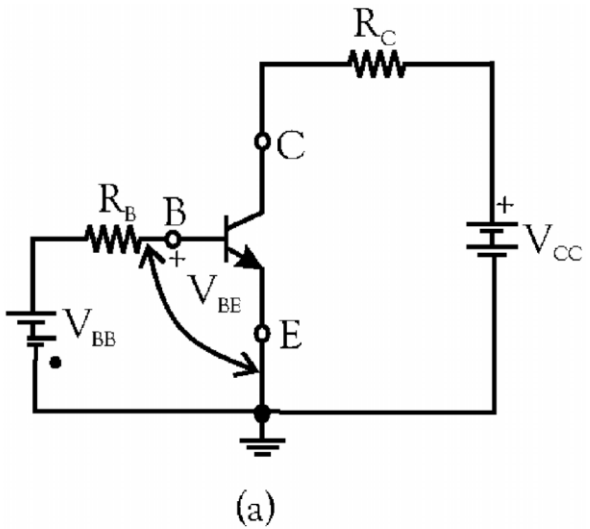
In the transistor amplifier circuits, the biasing can be done with two power supplies V_{BB} and V_{CC}. The V_{BB} supply is used for biasing of the emitter-base junction and V_{CC} supply is used for biasing the collector-base Junction. However, in practice, one power supply is used (only V_{CC}) for biasing both the junctions of a transistor. The most commonly used methods for biasing the transistors are:

(1) Base bias (also called fixed bias).
(2) Base bias with collector feedback (also called collector feedback bias).
(3) Voltage divider bias (also called self bias).

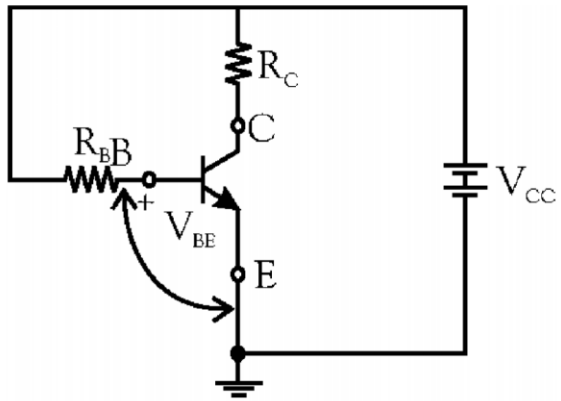
Base bias (Fixed bias)

Circuit Diagram

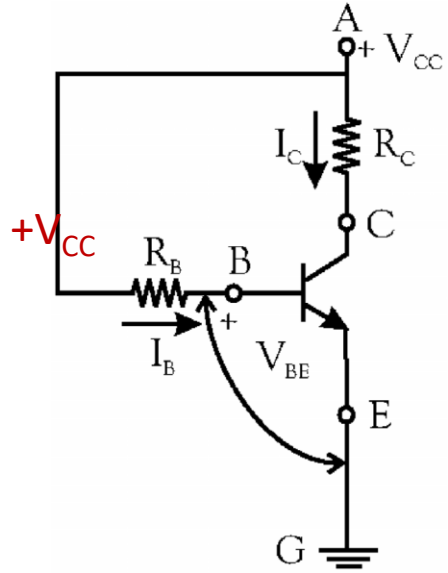
Base bias circuit for a NPN transistor is shown in Fig (a). The base bias circuit is also known as fixed bias circuit. In this case, the circuit uses two d.c. supplies namely VBB and V_{CC}. But a more practical method is to use only one d.c. supply (V_{CC}) as shown in Fig. (b). In this case, both the base and collector resistors are connected to the positive side of the V_{CC} supply. To simplify the
circuit diagram, we may replace the battery by a line termination with a voltage indicated as shown in Fig (c).



(a)



(b)



(c)

Circuit Analysis

Applying Kirchoff's Voltage Law for the E-B loop, **$+V_{CC} - I_B R_B - V_{BE} = 0$**

the base current, $$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since the supply voltage V_{CC} and the base-emitter voltage V_{BE} (0.7 V for Si) have fixed values of voltages, the selection of base bias resistor R_B fixes the value of I_B.

Applying Kirchoff's Voltage Law in C-E loop, **$+V_{CC} - I_C R_C - V_{CE} = 0$**

$V_{CE} = V_{CC} - I_C R_C$

$$I_B = V_{CC}/R_B$$

$V_{CC} >> V_{BE}$

In common emitter transistor configuration, **$I_C = \beta I_B = \beta (V_{CC}/R_B)$**

The above relation shows that the collector current I_C is β times greater than the base current I_B and is not at all dependent on the resistance of the collector circuit R_C.

Advantages and limitations of Base bias (Fixed bias)

Advantages:

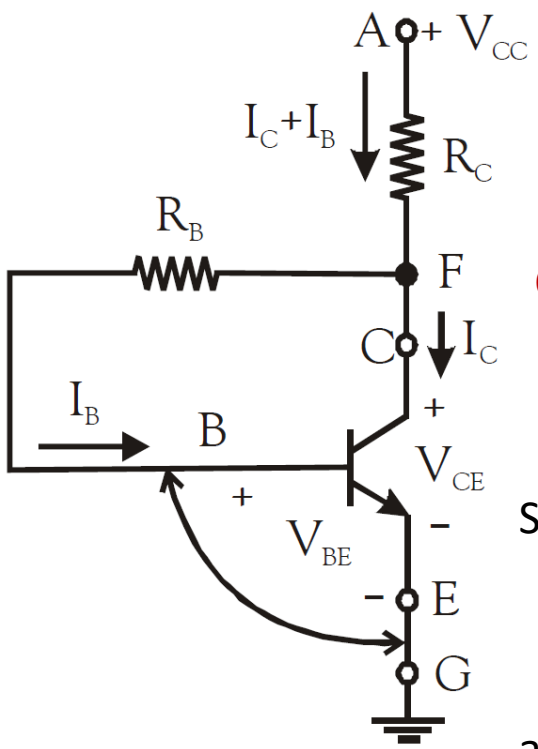
- This biasing circuit is very simple as only one resistance R_B is required.
- Biasing conditions can easily be set and the calculations are simple.
- There is no loading of the source by the biasing circuit since no external resistor is employed at emitter terminal.

Limitations:

- The values of collector current (I_C) and collector-to-emitter voltage (V_{CE}) are dependent on current gain $\boldsymbol{\beta}$. But we know that $\boldsymbol{\beta}$ is strongly dependent upon the temperature. It means that I_C and V_{CE} of a base bias circuit (which sets the Q-point of a transistor) will vary with the change in value of $\boldsymbol{\beta}$ due to variation in temperature. Hence, it is impossible to obtain a stable Q-point in a base-bias circuit. As a result the base bias is not used in amplifier circuits.
- The stability factor is very high (the base bias is CE transistor configuration. For this configuration stability factor S = $\boldsymbol{\beta}+1$). Therefore, there are large chances in I_C which leads thermal runaway. However, it is used in digital circuits, where the transistor is used as a switch between saturation and cut-off-regions.

Collector feedback bias (Base bias with collector feedback)

In order to decrease the stability factor further (ideally S = 1), collector to base bias is used. In collector to base bias, the collector voltage provides necessary bias voltage to Base-Emitter junction. This circuit tries to decrease thermal runaway problem.



In base bias collector feedback circuit, the base resistor (R_B) is connected to the collector terminal of a transistor rather than to the V_{CC} supply as in a base bias circuit. Here, the collector voltage provides the bias to base-emitter junction. The resistor R_B acts as a feedback resistor. It provides a very stable Q-point by reducing the effect of variations in current gain (**β**).

Circuit Analysis

Applying Kirchoff's Voltage Law to the base-emitter circuit loop.

$$+ V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

Substituting $I_C = \beta I_B$ in the above equation and solving for the base current,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_C} = \frac{V_{CC} - V_{BE}}{R_B + \beta . R_C} \quad \text{... (Taking } \beta + 1 = \beta)$$

and the collector current,

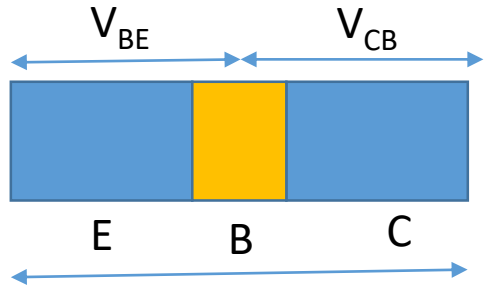
$$I_C = \beta . I_B = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta} = \frac{V_{CC}}{R_C + R_B / \beta} \quad (\because V_{CC} >> V_{BE})$$

Now applying Kirchoff's Voltage Law to the collector-emitter circuit loop, $+ V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$

$I_B << I_C$

Substituting $I_C + I_B = I_C$ in the above equation and solving it for collector-to-emitter voltage, $V_{CE} = V_{CC} - I_C R_C$

Advantages and limitations of Collector to Base Bias



Advantages:

It is a simple method as it requires only two resistors R_B & R_C.

This circuit provides some stabilization of the operating point as discussed below:

In general, $V_{CE} = V_{BE} + V_{CB}$

If there is an increase in collector leakage current due to increase in temperature, the total collector current tends to increase. As a result, V_{CE} tends to decreases due to greater drop across R_C ($V_{CE} = V_{CC} - I_C R_C$). This will decreases V_{CB} & hence I_B. Such decrease in I_B decreases I_C to original value compensating previous increase.

Limitations:

The circuit does not provide good stabilization and the stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and aging effects.

This circuit provides a negative feedback which reduces the gain of the amplifier. During the positive half-cycle of the input signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current. This will affect the stability of Q-point.

Stability of Collector to Base Bias

If we apply Kirchoff's Voltage Law to the base-emitter circuit, then we get

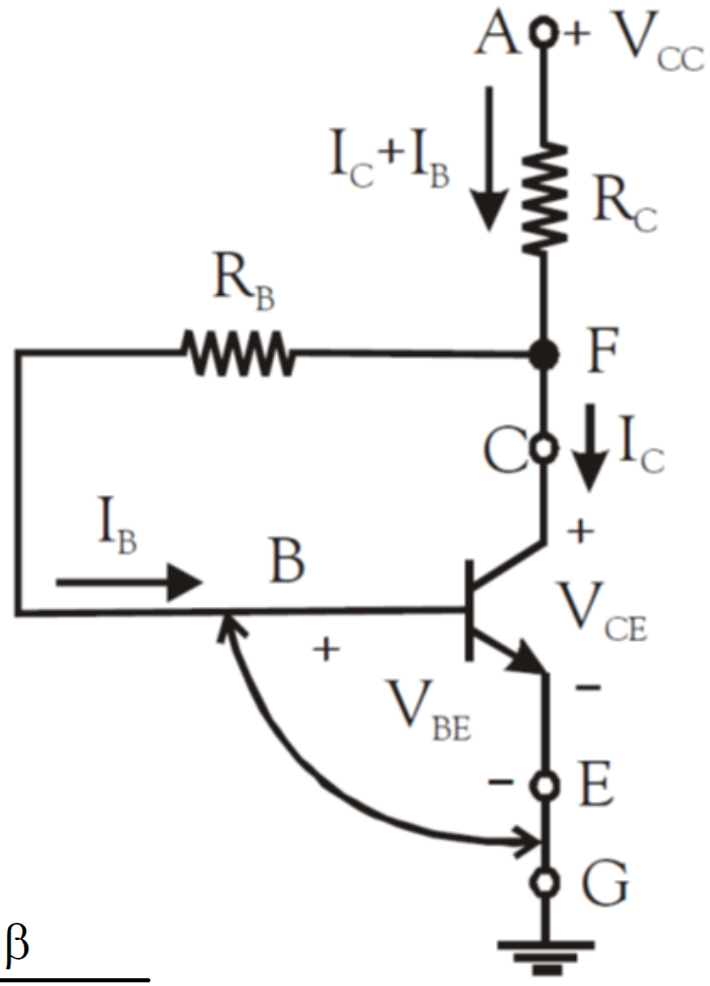
$$+ V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

Rearranging the above equation and solving for base current,

$$I_B = \frac{V_{CC} - V_{BE} - I_C.R_C}{R_C + R_B}$$

Differentiating the above expression with respect to I_C,

$$\frac{dI_B}{dI_C} = \frac{0 - 0 - 1.R_C}{R_C + R_B} = - \frac{R_C}{R_C + R_B}$$



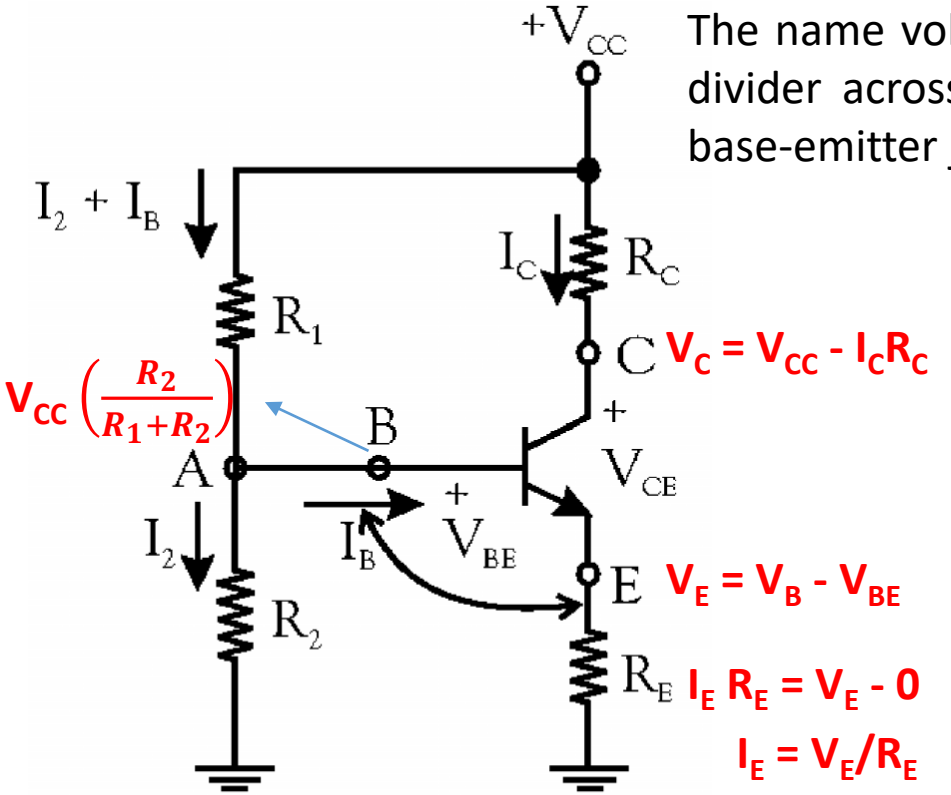
Substituting the value of dI_B/dI_C in the general expression for stability factor,

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_C+R_B}\right)} = \frac{1+\beta}{1+\beta\times\frac{R_C}{R_C+R_B}}$$

From the above expression it is evident that the stability factor (S) of a collector feedback bias is smaller than (1 + **β**). Therefore, the biasing arrangement of collector feedback resistor is certainly an improvement over the fixed bias circuit.

Voltage divider bias (self bias)

In base bias and Collector to base bias, the values of d.c. current (I_C) and voltage (V_{CE}) of the collector depends upon the current gain (β) of the transistor. But we know that the value of current gain (β) is temperature sensitive. Therefore it would be desirable to provide a d.c. bias circuit which is independent of the transistor current gain (β). The d.c. bias circuit shown in Fig meets this condition and is thus a very popular bias circuit. It is commonly known as voltage divider bias or self bias circuit.



(a) Voltage divide bias circuit

The name voltage divider is derived from the fact that resistors R_1 an R_2 form a voltage divider across the V_{CC} supply. The voltage drops across resistor R_2 forward biases the base-emitter junction of a transistor. The emitter resistor (R_E) provides the d.c. stability.

Circuit Analysis

Base voltage, $V_B = V_{CC}\left(\frac{R_2}{R_1+R_2}\right)$

Emitter current, $I_E = V_E/R_E$ (or)

$I_E = (I_2 R_2 + V_{BE})/R_E$

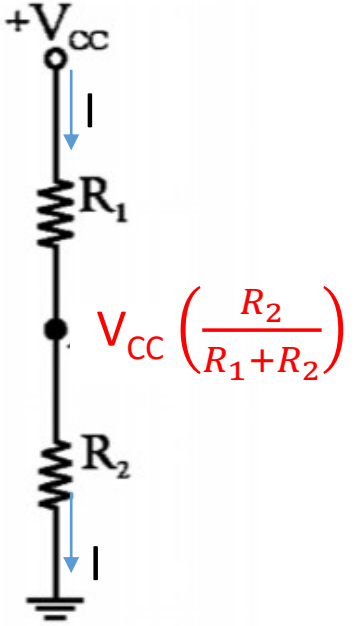
Collector current, $I_C = I_E$

$I_C = (I_2 R_2 + V_{BE})/R_E$

(or)

$I_C = (V_{CC} - V_C)R_C$

In voltage divider bias, I_C is independent on β.



(b) Voltage divider

Using KVL in B-E loop

$I_2 R_2 - V_{BE} - I_E R_E = 0$

$I_E = (I_2 R_2 + V_{BE})/R_E$

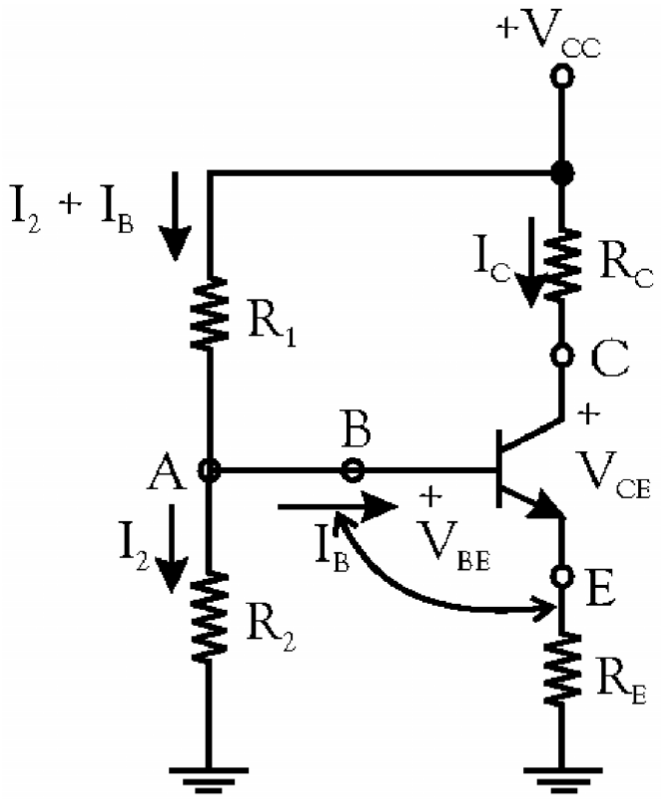
Collector-emitter voltage, $V_{CE} = V_C - V_E$

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

Since, $I_C = I_E$

Stability factor of Voltage divider bias (self bias)

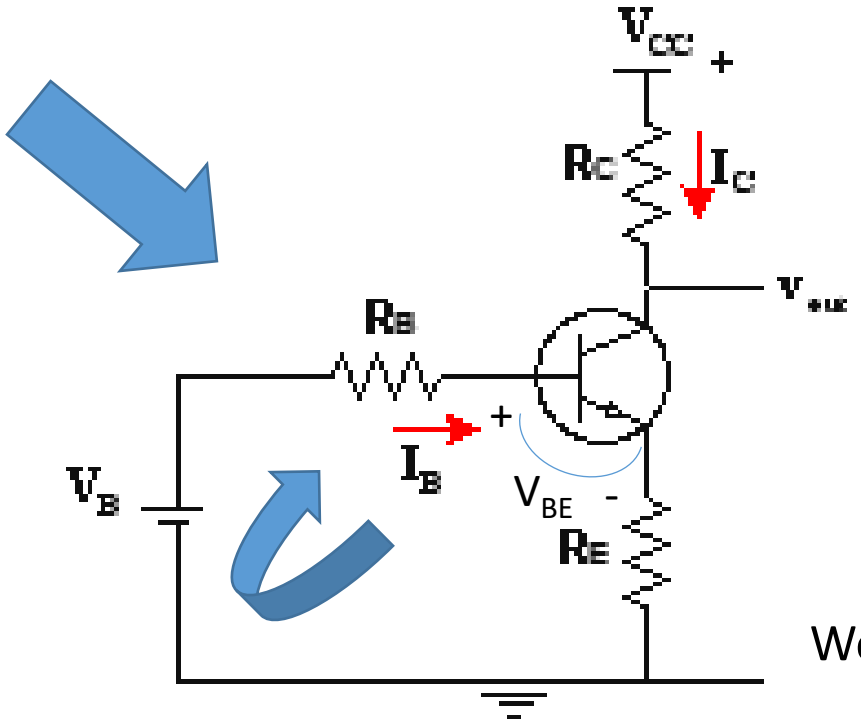


(a) Voltage divide bias circuit

In this circuit, excellent stabilization is provided by R_E.

$$I_2 R_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will increase the voltage drop across emitter resistance R_E. As voltage drop across R_2 (I_2R_2) is independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.



$$R_B = R_{Th} = R_1 \| R_2$$

$$V_B = V_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Using KVL in B-E loop

$$V_B - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (1+\beta) I_B R_E = 0$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

We know, $I_C = \beta I_B$

If $R_{Th} << (\beta+1)R_E$

Then I_C does not depend on β, as β in numerator and denominator cancels out

Using KVL in B-E loop

$$I_2 R_2 - V_{BE} - I_E R_E = 0$$

$$I_2 R_2 = V_{BE} + I_E R_E$$

Since, $I_E = I_C$

$$I_2 R_2 = V_{BE} + I_C R_E$$

$$I_C = I_E = (I_2 R_2 + V_{BE})/R_E$$