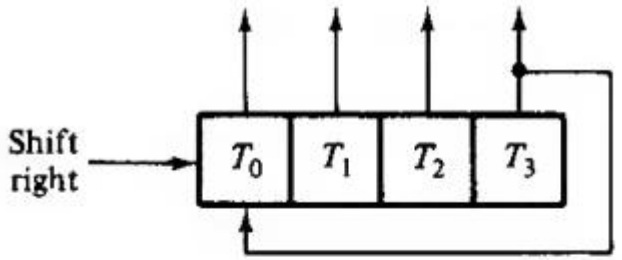
Digital Logic and Circuit
Paper Code: CS-102

Outline

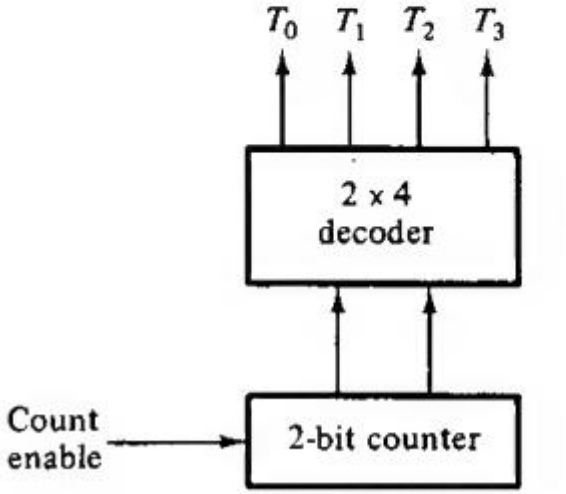
- **Sequential Circuit**
  - **Ring Counter**
  - **Johnson Counter**
  - **RAM**

Ring Counter

- A ring counter is a circular shift register with only one flip-flop being set at any particular time; all others are cleared.
- The single bit is shifted from one flip-flop to the other to produce the sequence of timing signals.
- Figure (a) shows a 4-bit shift register connected as a ring counter. The initial value of the register is 1000, which produces the variable T0 .
- The single bit is shifted right with every clock pulse and circulates back from T3 to T0 .
- Each flipflop is in the 1 state once every four clock pulses and produces one of the four timing signals shown in Fig. (c).
- Each output becomes a 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock pulse.

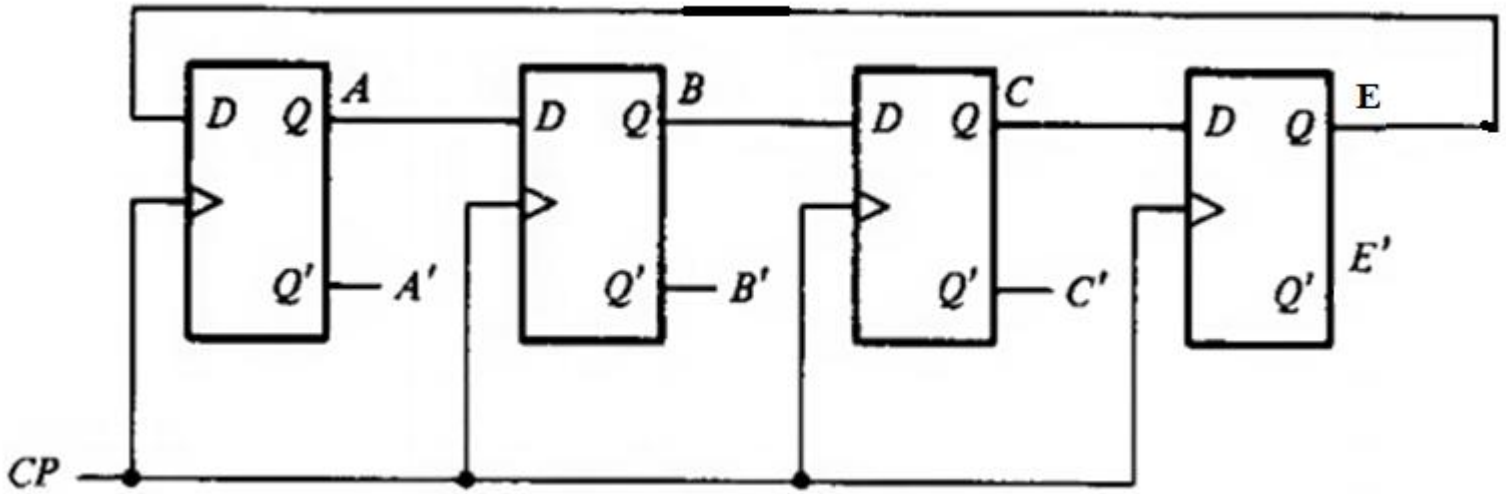


(a) Ringcounter (initial value = 1000)

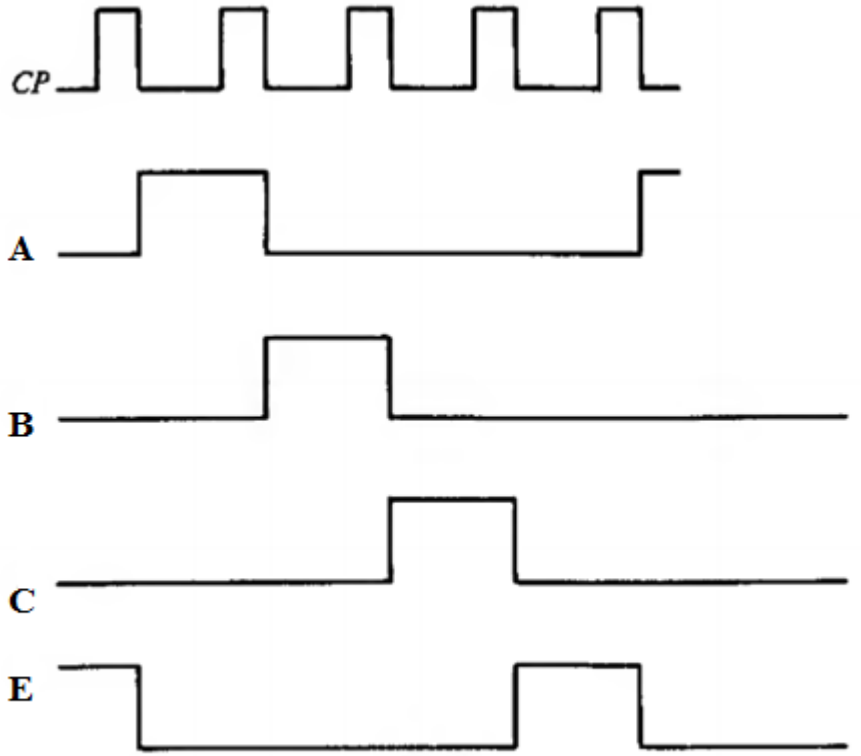


(b) Counter and decoder

CP4	0	0	0	1
CP3	0	0	1	0
CP2	0	1	0	0
CP1	1	0	0	0



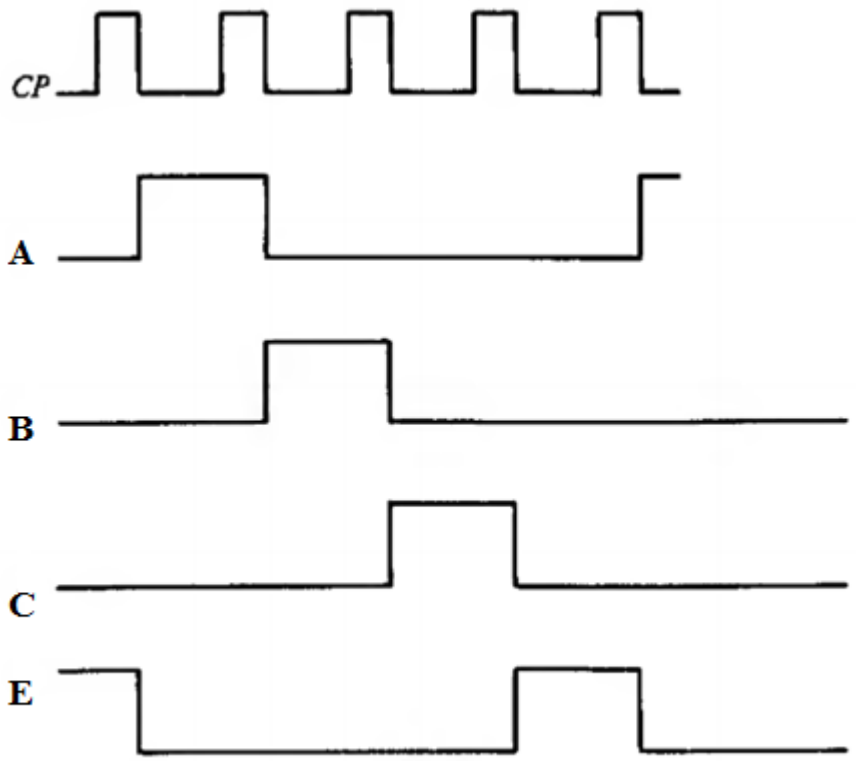
Initial value 1000



(c) Sequence of four timing signals

CP4	0	0	0	1
CP3	0	0	1	0
CP2	0	1	0	0
CP1	1	0	0	0

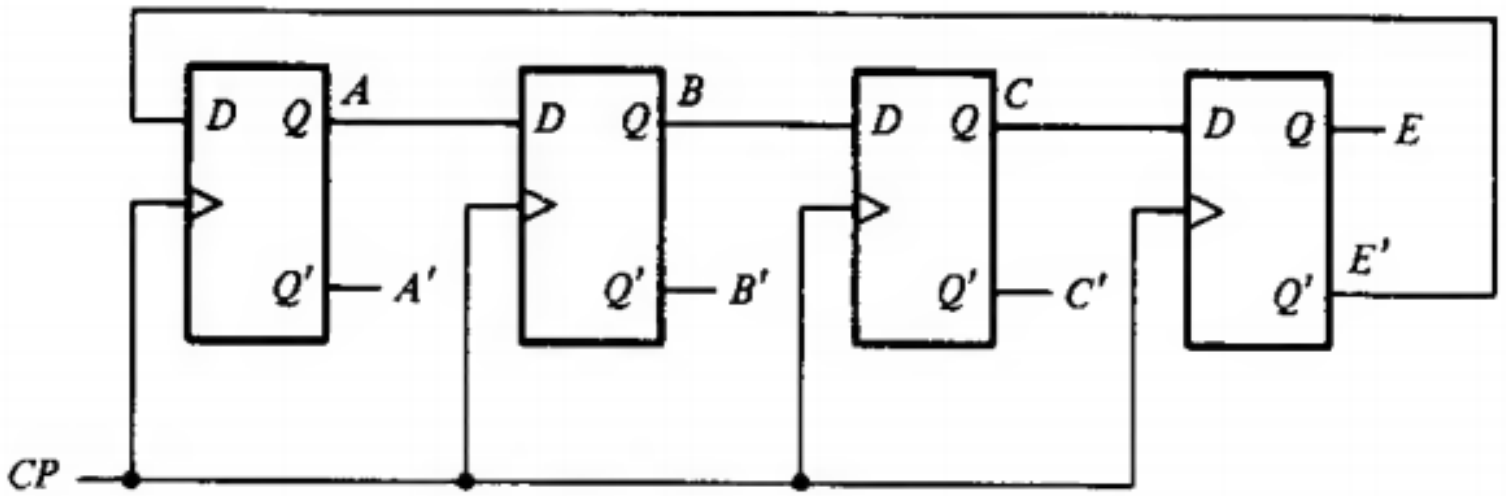
CP	A	B	C	E
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1



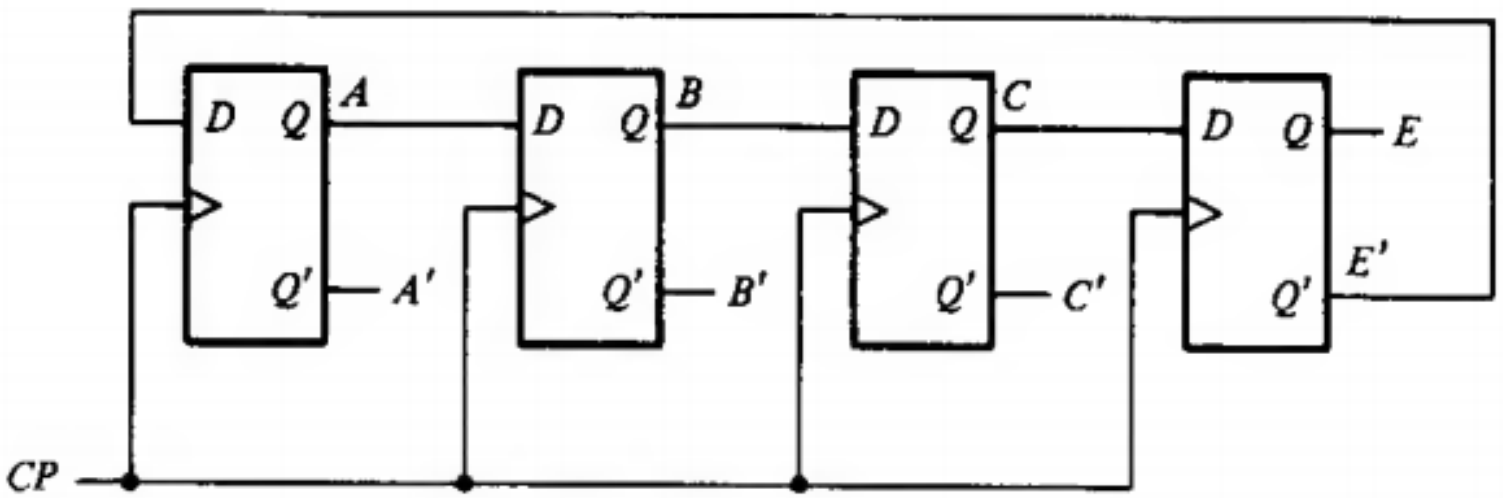
(c) Sequence of four timing signals

Johnson's Counter or switch-tail ring counter

- A k-bit ring counter circulates a single bit among the flip-flops to provide k distinguishable states.
- The number of states can be doubled if the shift register is connected as a switch- tail ring counter.
- A switch- tail ring counter is a circular shift register with the complement output of the last flip-flop connected to the input of the first flip-flop.
- The circular connection is made from the complement output of the rightmost flip-flop to the input of the leftmost flip-flop.
- The register shifts its contents once to the right with every clock pulse, and at the same time, the complement value of the E flip-flop is transferred into the A flip-flop.
- Starting from a cleared state, the switch- tail ring counter goes through a sequence of eight states, as listed in Fig. (b). In general, a A-bit switch-tail ring counter will go through a sequence of 2k states.



(a) Four-stage switch-tail ring counter



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs A	B	C	E
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

(b) Count sequence

RANDOM-ACCESS MEMORY (RAM)

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- A memory unit is a collection of storage cells together with associated circuits needed to transfer information in and out of the device.
- Memory cells can be accessed for information transfer to or from any desired random location and hence the name random access memory, abbreviated RAM.
  A memory unit stores binary information in groups of bits called words.
- A word in memory is an entity of bits that move in and out of storage as a unit.
- A group of eight bits is called a byte. Most computer memories use words that are multiples of 8 bits in length.
- Thus, a 16-bit word contains two bytes, and a 32-bit word is made up of four bytes.
- The capacity of a memory unit is usually stated as the total number of bytes that it can store.

- The communication between a memory and its environment is achieved through data input and output lines, address selection lines, and control lines that specify the direction of transfer.
- The memory unit is specified by the number of words it contains and the number of bits in each word.
- The address lines select one particular word. Each word in memory is assigned an identification number, called an address, starting from 0 and continuing with 1, 2, 3, up to $2^k - 1$, where k is the number of address lines.
- The selection of a specific word inside the memory is done by applying the k- bit binary address to the address lines.

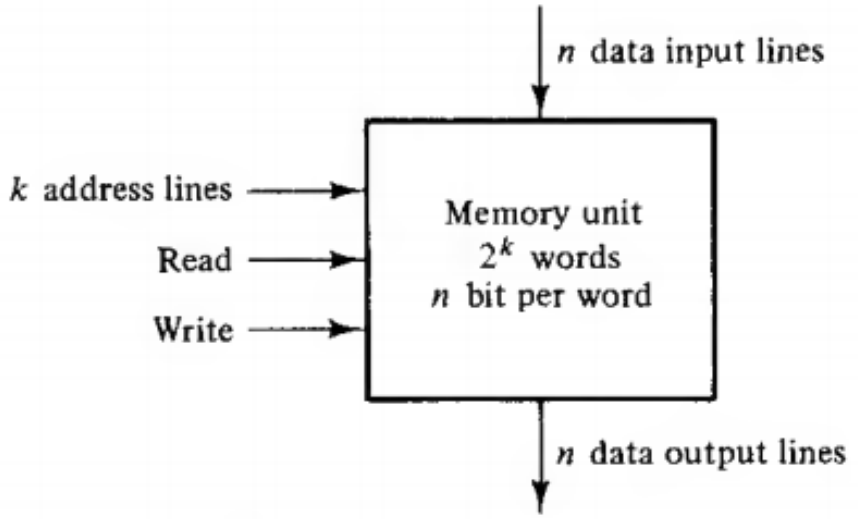
Computer memories may range from 1024 words, requiring an address of 10 bits, to 2^{32} words, requiring 32 address bits.

It is customary to refer to the number of words (or bytes) in a memory with one of the letters K (kilo), M (mega), or G (giga).

K is equal to 2^{10}, M is equal to 2^{20}, and G is equal to 2^{30}. Thus, $64K = 2^{16}$, $2M = 2^{21}$, and $4G = 2^{32}$.

Example:

Consider, for example, the memory unit with a capacity of IK words of 16 bits each. Since IK = 1024 = 2^{10} and 16 bits constitute two bytes, we can say that the memory can accommodate 2048 - 2K bytes.



Block diagram of a memory unit

Figure shows the possible content of the first three and the last three words of this memory.

Each word contains 16 bits, which can be divided into two bytes.

The words are recognized by their decimal address from 0 to 1023.

The equivalent binary address consists of 10 bits.

A word in memory is selected by its binary address. When a word is read or written, the memory operates on all 16 bits as a single unit.

Memory address		
Binary	decimal	Memory content
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Content of a 1024 × 16 memory

Write and Read Operations

The two operations that a random- access memory can perform are the write and read operations.

The write signal specifies a transfer-in operation and the read signal specifies a transfer-out operation.

On accepting one of these control signals, the internal circuits inside the memory provide the desired function.

The steps that must be taken for the purpose of transferring a new word to be stored into memory are as follows:

1. Transfer the binary address of the desired word to the address lines.

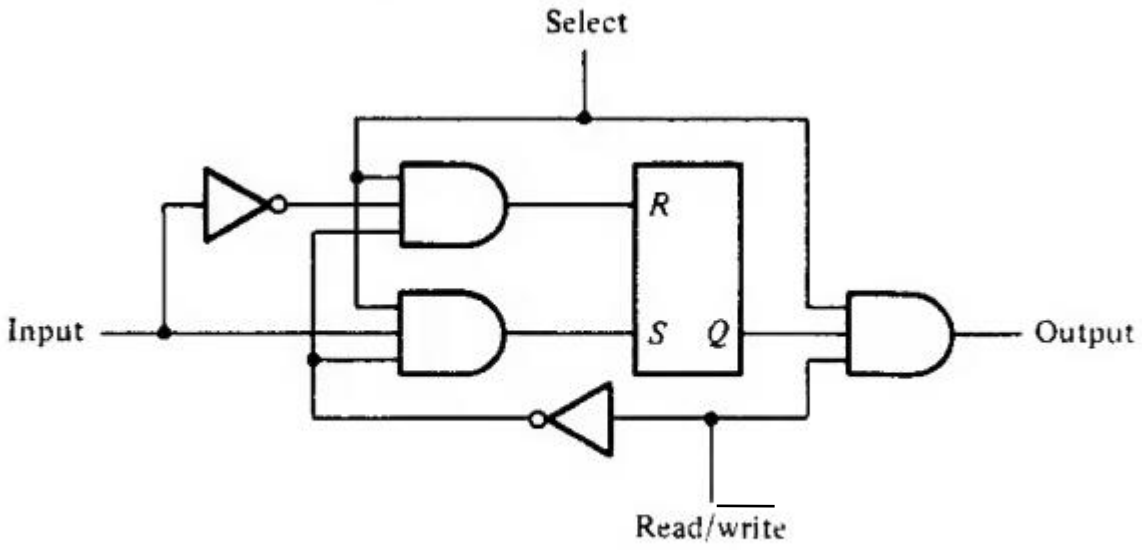
2. Transfer the data bits that must be stored in memory to the data input lines.

3. Activate the write input.

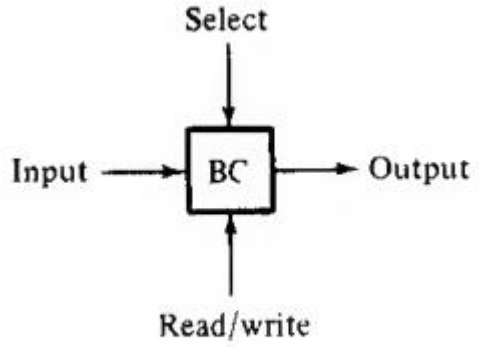
Internal Construction of RAM

The internal construction of a random-access memory of m words with n bits per word consists of m X n binary storage cells and associated decoding circuits for selecting individual words.

The binary storage cell is the basic building block of a memory unit.



(a) Logic diagram

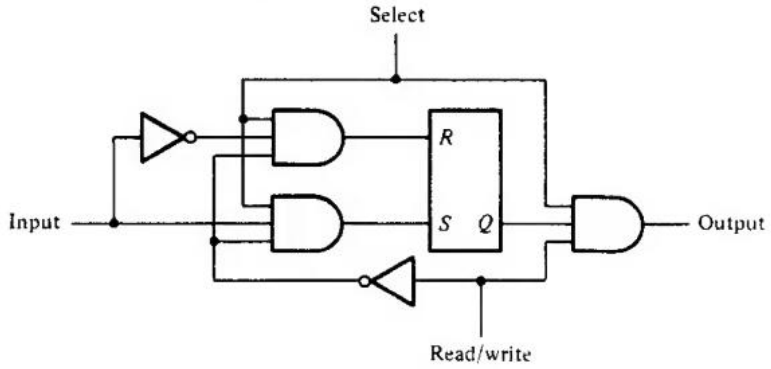


(b) Block diagram

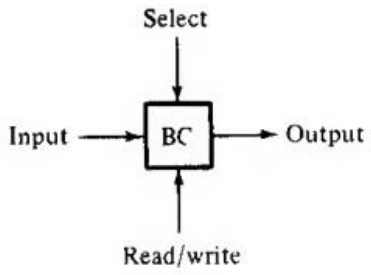
Read=1
Write=0

The logical construction of a small RAM is shown in Figure.

It consists of 4 words of 3 bits each and has a total of 12 binary cells.

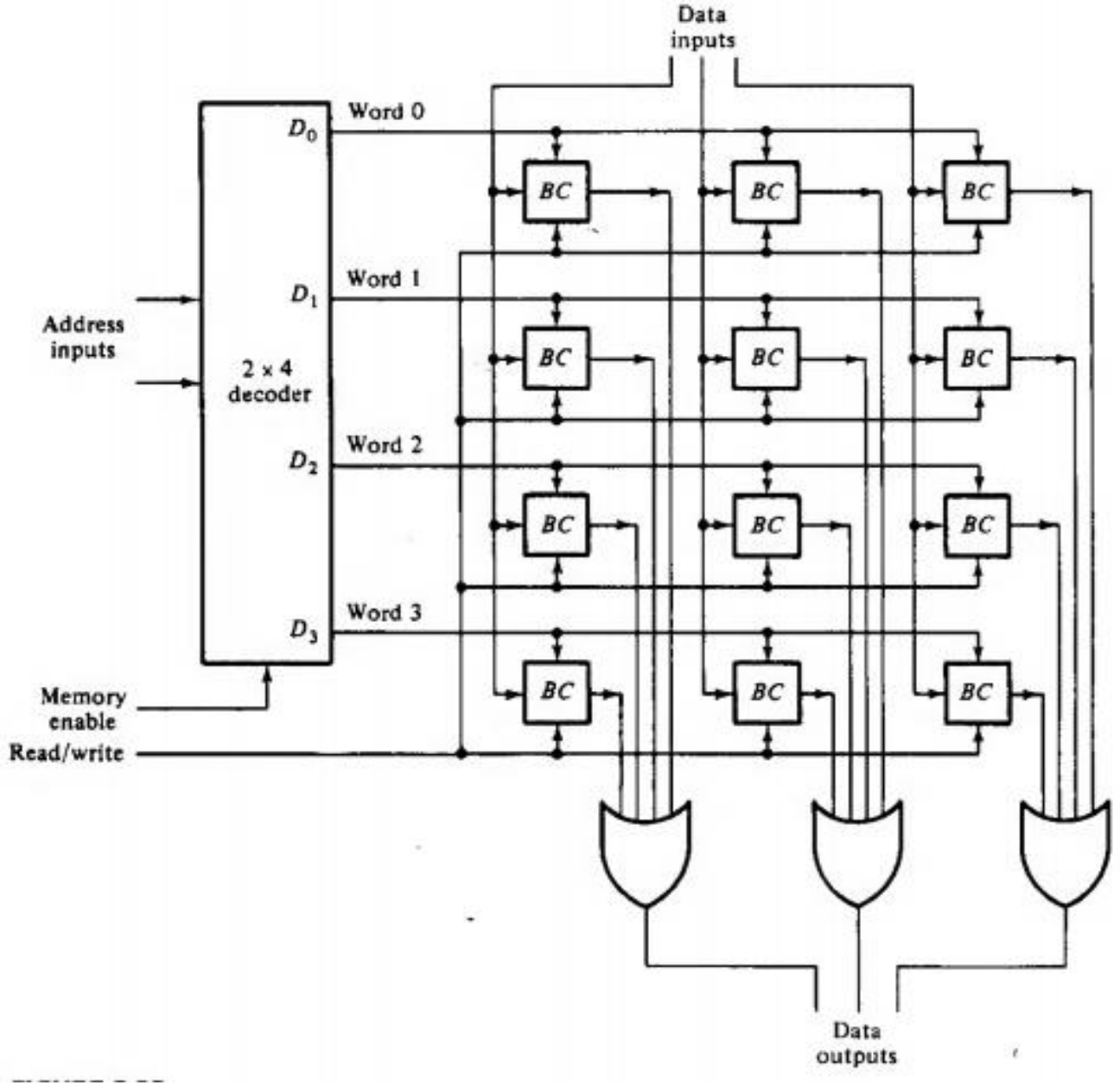


(a) Logic diagram



(b) Block diagram

Read=1
Write=0



Logical construction of a 4 x 3 RAM

- Commercial random-access memories may have a capacity of thousands of words and each word may range from 1 to 64 bits .
- The logical construction of a large capacity memory would be a direct extension of the configuration shown here.
- A memory with 2^k words of n bits per word requires k address lines that go into a k x 2^K decoder.
- Each one of the decoder outputs selects one word of n bits for reading or writing.

Suggested Reading

- M. Morris Mano, Digital Logic and Computer Design, PHI.

Thank you