Digital Logic and Circuit
Paper Code: CS-102

Outline

Combinational circuit

- Programmable Logic Array
- Programmable Array Logic

Sequential Circuit

PROGRAMMABLE LOGIC ARRAY (PLA)

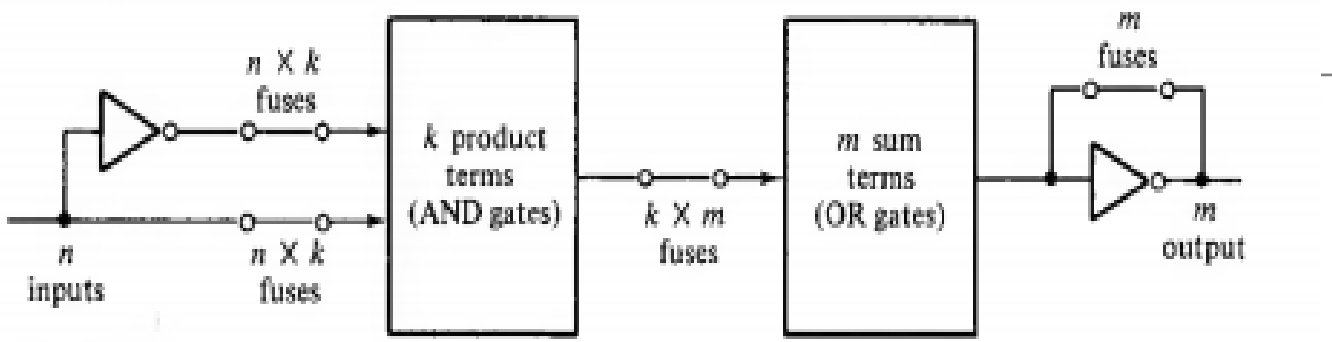
- A PLA is similar to a ROM in concept; however, the PLA does not provide full decoding of the variables and does not generate all the minterms as in the ROM.

- In the PLA, the decoder is replaced by a group of AND gates, each of which can be programmed to generate a product term of the input variables.

- The AND and OR gates inside the PLA are initially fabricated with fuses among them.

- The specific Boolean functions are implemented in sum of products form by blowing appropriate fuses and leaving the desired connections.

Block diagram of PLA



- It consists of n inputs, m outputs, k product terms, and m sum terms.
- The product terms constitute a group of **k** AND gates and the sum terms constitute a group of **m** OR gates.
- Fuses are inserted between all n inputs and their complement values to each of the AND gates.
- Fuses are also provided between the outputs of the AND gates and the inputs of the OR gates.
- Another set of fuses in the output inverters allows the output function to be generated either in the AND-OR form or in the AND-OR-INVERT form.
- With the inverter fuse in place, the inverter is bypassed, giving an AND-OR implementation.
- With the fuse blown, the inverter becomes part of the circuit and the function is implemented in the AND-OR-INVERT form.

- The use of a PLA must be considered for combinational circuits that have a large number of inputs and outputs.

- It is superior to a ROM for circuits that have a large number of don’t-care conditions.

Example

Consider the truth table of the combinational circuit.

A	B	C	F_1	F_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

(a) Truth table

- Although a ROM implements a combinational circuit in its sum of minterms form, a PLA implements the functions in their sum of products form.

- Each product term in the expression requires an AND gate.

- Since the number of AND gates in a PLA is finite, it is necessary to simplify the function to a minimum number of product terms in order to minimize the number of AND gates used.

Example:

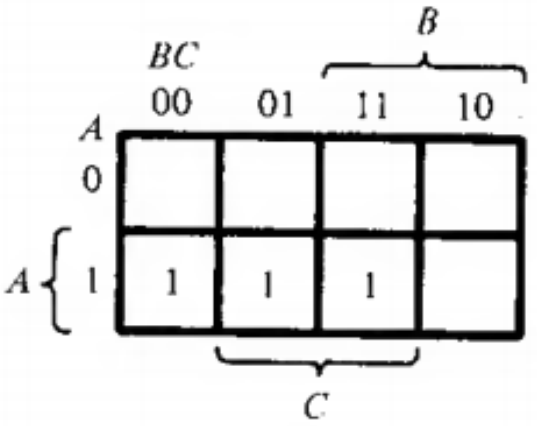
- The simplified functions in sum of products are obtained using k-Map

- F_1=AB'+AC

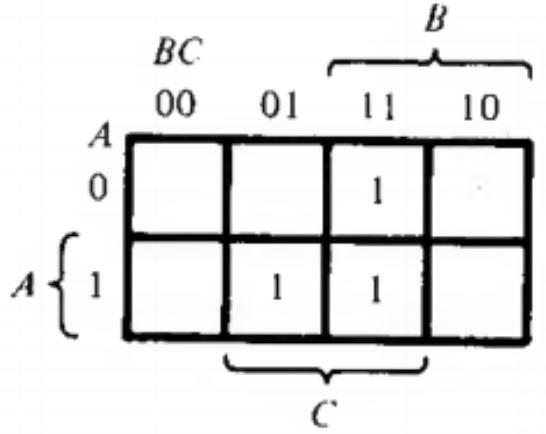
- F_2=AC+BC
- There are three distinct product terms in this combinational circuit: AB', AC, and BC. The circuit has three inputs and two outputs
- No. of input buffer=no. of input variable
- No. of AND gate=no. of product term
- No. of OR gate=No. of Output function

A	B	C	F_1	F_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

(a) Truth table



$F_1 = AB' + AC$



$F_2 = AC + BC$

(b) Map simplification

- For each product term, the inputs are marked with 1 , 0, or - (dash).
- If a variable in the product term appears in its normal form (unprimed), the corresponding input variable is marked with a 1.

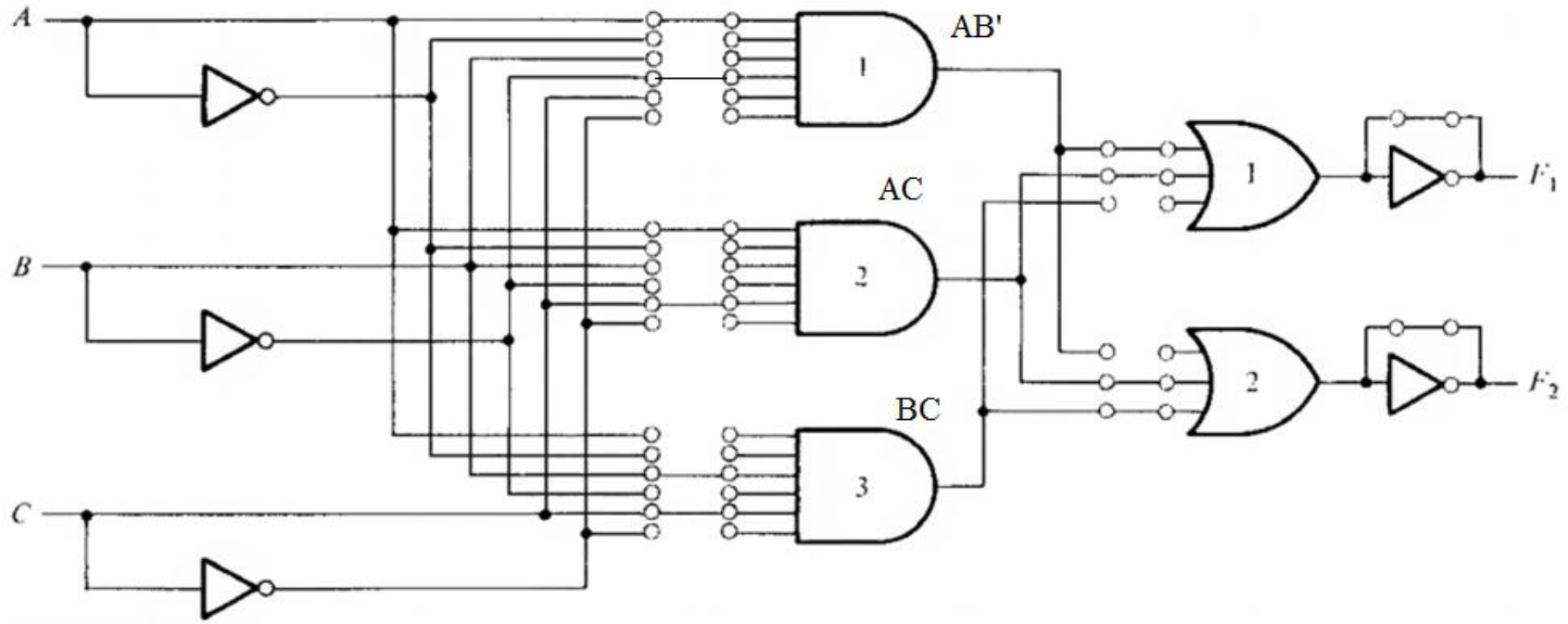
- If it appears complemented (primed), the corresponding input variable is marked with a 0.
- If the variable is absent in the product term, it is marked with a dash.

	Product term	Inputs A	B	C	Outputs F_1	F_2
AB'	1	1	0	–	1	–
AC	2	1	–	1	1	1
BC	3	–	1	1	–	1

- so F1 is marked with 1's for product terms 1 and 2 and with a dash for product term 3.
  Each product term that has a 1 in the output column requires a path from the corresponding AND gate to the output OR gate.

- Those marked with a dash specify no connection.

PLA with three Inputs, three product terms, and two outputs;



The example to be presented demonstrates how a PLA is programmed.

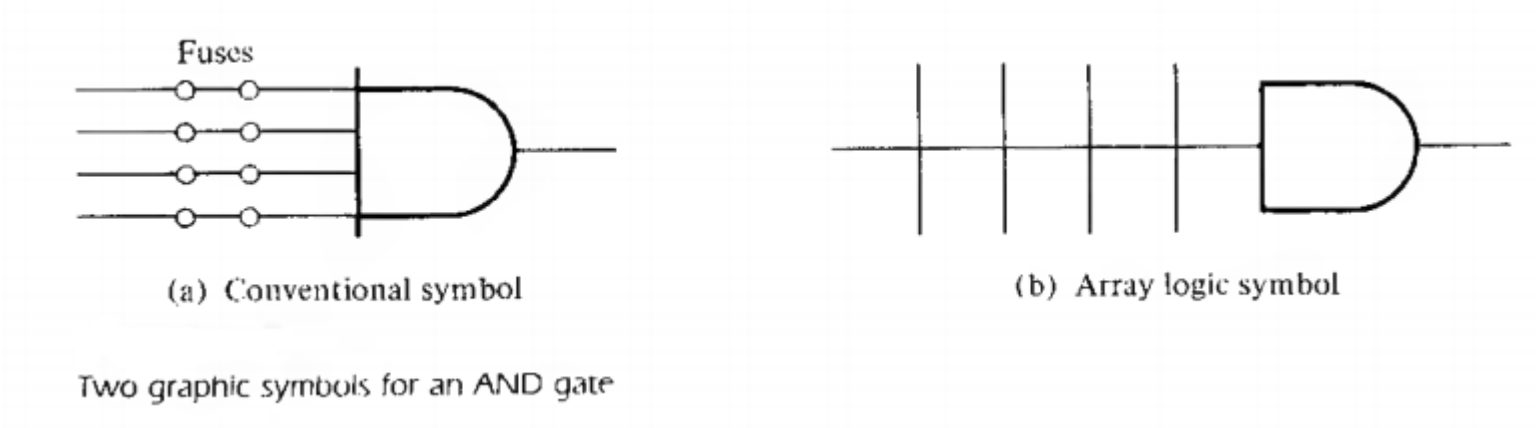
Bear in mind when going through the example that such a simple circuit will not require a PLA because it can be implemented more economically with SSI gates.

PROGRAMMABLE ARRAY LOGIC

PROGRAMMABLE ARRAY LOGIC (PAL)

The programmable array logic (PAL) is a programmable logic device with a fixed OR array and a programmable AND array.

Because only the AND gates are programmable, the PAL is easier to program, but is not as flexible as the PLA.



Two graphic symbols for an AND gate

Example: Consider the following Boolean functions given in sum of minterms:

$w(A,B,C,D) = \sum(2, 12, 13)$
$x\{A, B, C, D) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$
$y(A, B, C, D) = \sum(0, 2, 3. 4, 5, 6, 7, 8, 10, 11, 15)$
$z(A, B, C, D) = \sum(1, 2, 8, 12, 13)$

Simplifying the four functions to a minimum number of terms results in the following Boolean functions:

$w = ABC' + A'B'CD'$
$x = A + BCD$
$y = A'B + CD + B'D'$
$z = ABC' + A'B'CD' + AC'D' + A'B'C'D$
$z = w + AC'D' + A'B'CD$

Note that the function for z has four product terms. The logical sum of two of these terms is equal to w. By using w, it is possible to reduce the number of terms for z from four to three.

The PAL programming table is similar to the one used for the PLA except that only the inputs of the AND gates need to be programmed.

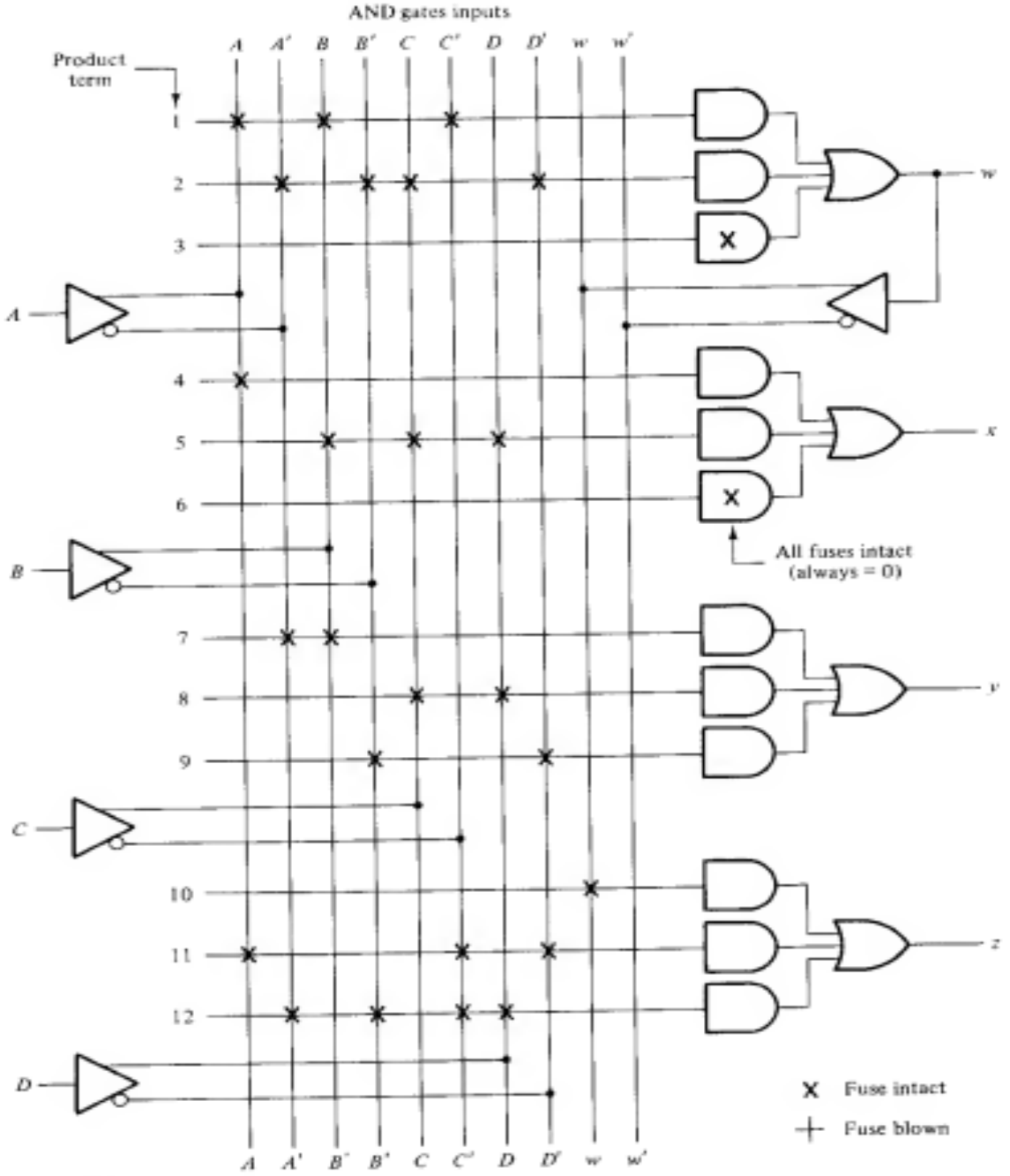
PAL Programming Table

Product Term	AND Inputs A	B	C	D	W	Outputs
1	1	1	0	–	–	$w = ABC'$
2	0	0	1	0	–	$+ A'B'CD'$
3	–	–	–	–	–	
4	1	–	–	–	–	$x = A$
5	–	1	1	1	–	$+ BCD$
6	–	–	–	–	–	
7	0	1	–	–	–	$y = A'B$
8	–	–	1	1	–	$+ CD$
9	–	0	–	0	–	$+ B'D'$
10	–	–	–	–	1	$z = w$
11	1	–	0	0	–	$+ AC'D'$
12	0	0	0	1	–	$+ A'B'C'D$

Input buffer=no. of input varaible

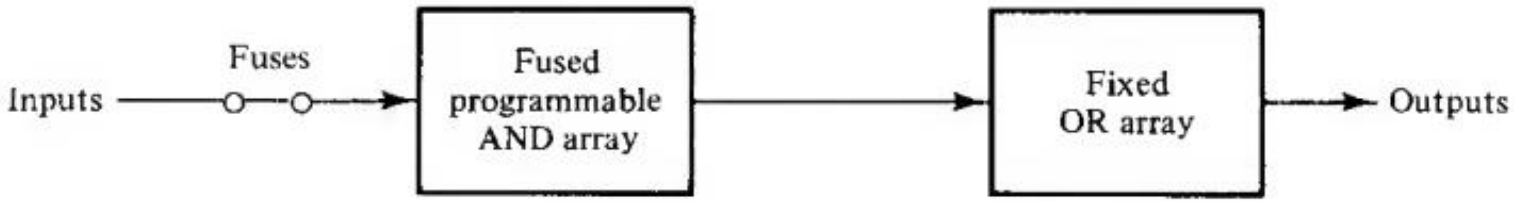
No. of AND gate= Highest number of product term present in any Boolean expression

No. of OR gate=number of output.

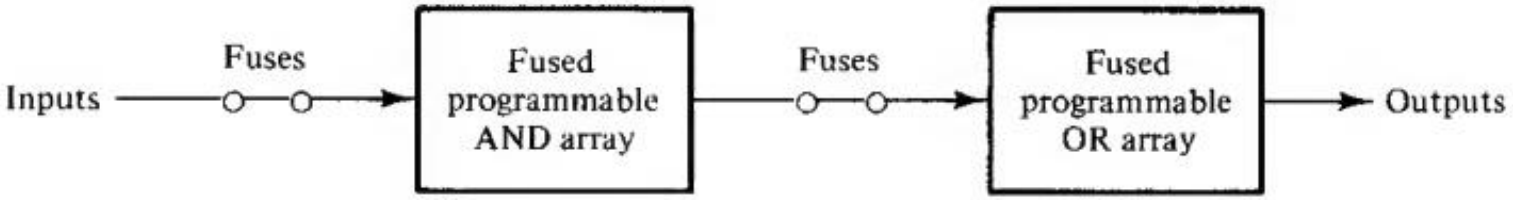


- PAL has four inputs and four out puts. Each input has a buffer and an inverter gate. Note that the two gates are shown with one composite graphic symbol with normal and complement outputs.
- There are four sections in the unit, each being composed of a threewide AND-OR array.
- This is the term used to indicate that there are three programmable AND gates in each section and one fixed OR gate. Each AND gate has 10 fused programmable inputs.
- This is shown in the diagram by 10 vertical lines intersecting each horizontal line.
- The horizontal line symbolizes the multiple -input configuration of the AND gate.
- One of the outputs is connected to a buffer-inverter gate and then fed back into the inputs of the AND gates through fuses.

Basic Configuration of PAL and PLA



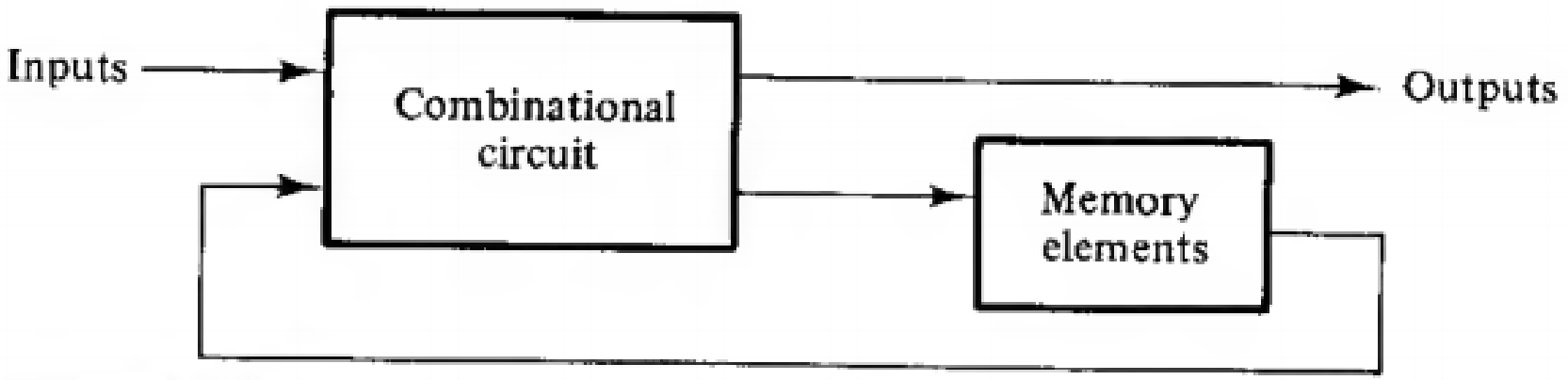
(b) Programmable array logic (PAL)



(c) Programmable logic array (PLA)

The digital circuits considered thus far have been combinational, i.e., the outputs at any instant of time are entirely dependent upon the inputs present at that time.

Although every digital system is likely to have combinational circuits, most systems encountered in practice also include memory elements , which require that the system be described in terms of sequential logic.



Block diagram of a sequential circuit

Suggested Reading

- M. Morris Mano, Digital Logic and Computer Design, PHI.

Thank you