EXPERIMENT ON LOGIC GATES

OBJECT:

To assemble the logic gates AND, OR, NOT, NAND and NOR using diodes, resistances and a transistor, and to verify their truth tables by measuring voltages at inputs and output.

APPARATUS REQUIRED:

Experimental kit fitted with 5V power supply, 3 diodes (OA 79), one transistor (SL 100), three resistances (820 Ohm, 2.8K Ohm and 73K Ohm) a voltmeter (0-5V range) and a light emitting diode (LED).

THEORY:

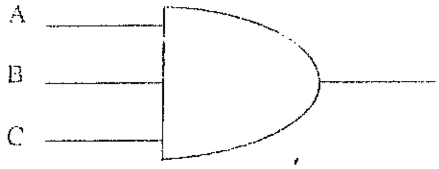
Logic gates are basic circuits that are used to implement the different logical operations of Boolean algebra. In Boolean algebra there are three basic operations (i) AND, (ii) OR (iii) and NOT. By combining these we get additional logical operations like NAND, NOR, XOR and XNOR.

A logical statement can be true or false, so any Boolean variable can have only two values. These values are represented as 0 (false) and 1 (true), respectively. These two values of Boolean variables can be implemented experimentally in terms of two clearly distinguishable voltage levels. Exact magnitudes of these voltage levels are unimportant so long as the levels are clearly distinguishable. If the more positive (higher) voltage is regarded level 1 and the other is treated as level 0, then the system is said to employ positive logic. On the other hand a negative logic system is one which designates more negative (lower) voltage state as level 1 and the more positive (higher) as level 0. It should be noted that the 0 level need not represent zero voltage level. Normally in positive logic 0 level is represented by 0.3 ± 0.3 V and 1 level is represented by 4.0 ± 1.0 V, while in negative logic 0 level is represented by 4.0 ± 1.0 V and 1 level is represented by 0.3 ± 0.3 V.

A digital system also functions in a binary manner. It employs devices that exist only in two possible states 0 and 1, so digital systems can also be designed using basic logic gates described below.

1. AND Gate

An AND gate is a logic gate which has two or more inputs and one output. The output assumes state 1 if and only if all the inputs are in state 1. A symbol for the 3-input AND gate is given in Fig.1 together with the Boolean expression for it. This equation is to be read as "Y equals A and B and C". The dot (.) between the symbols denotes AND operation. Table 1 summarizes the relationship between inputs and the output for this gate and is known as its truth table.



$Y = A.B.C$

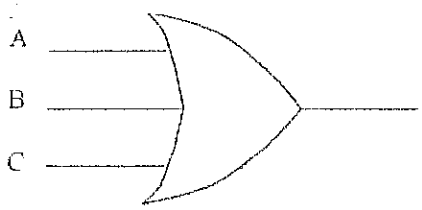
Fig. 1

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 1

2. OR Gate

An OR gate is a circuit which has two or more inputs and one output. The output assumes state 1 if one or more inputs assume state 1. A symbol for 3-input OR gate together with the Boolean expression for this gate is given Fig 2. The equation is to be read as "Y equals A or B or C". Table 2 gives the truth table for the 3-input OR gate.



$Y = A+B+C$

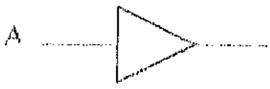
Fig. 2

A	B	C	Y
0	0	0	0
0	0	[illegible]	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 2

3. NOT Gate

A NOT gate, also known as an inverter, has one input and one output and performs the operation of logic negation. The output of a NOT gate is in state 1, if the input is in state 0 and the output is in state 0 if the input is in state 1. The symbol for the NOT gate and the Boolean expression for negation are given in Fig.3. The equation is to be read as "Y equals NOT A" or "Y is the complement of A". The truth table is given in Table3. The logic symbol and the Boolean expression for NOT gae is given in Fig.3.



$$Y = \overline{A}$$

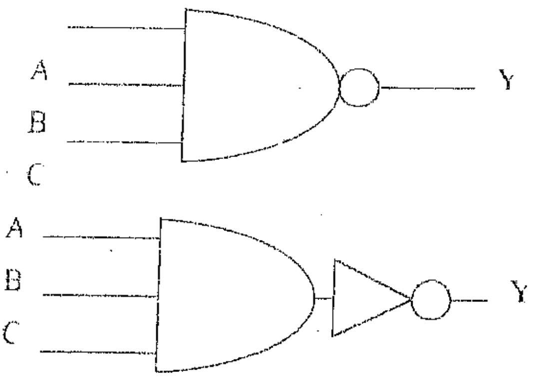
Fig. 3

A	Y
0	1
1	0

Table 3

4. NAND Gate

The term NAND is a contraction of NOT-AND and implies an AND operation th a complemented (inverted) output. It is equivalent to AND gate followed by a OT gate. The logic symbol for a 3-input NAND gate, its equivalence to an AND te followed by a NOT gate and its Boolean expression are given in Fig. 4. The truth ble for a 3-input NAND gate is summarized in Table 4.



$$Y = \overline{A.B.C}$$

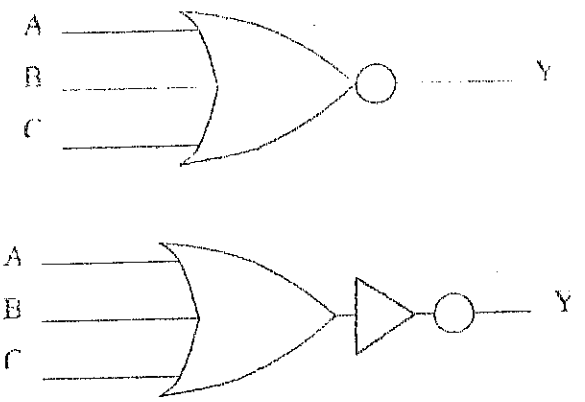
Fig. 4

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 4

5. NOR Gate

The term NOR is a contraction of NOT-OR and implies an OR function with verted output. Thus a NOR gate is equivalent to an OR gate followed by a NOT The logic symbol for a 3-input NOR gate, its equivalence to an OR gate wed by a NOT gate and its Boolean expression are given in Fig. 5. The truth for a 3-input NOR gate is given in Table 5.



0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

$$Y = \overline{A+B+C}$$

Fig.5

Table 5

EXPERIMENTAL PROCEDURE:

1. AND Gate

1. Assemble the circuit for 3-input AND gate as shown in Fig. 6

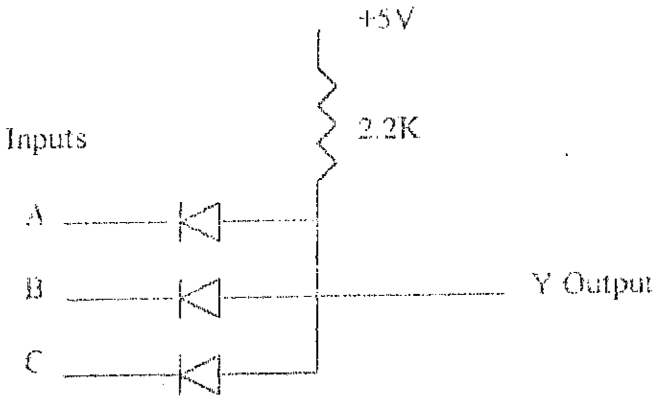


Fig. 6.

2. Apply various combinations of inputs at A, B and C as given in Table 1 and note the corresponding output. The inputs A, B and C can be set to be 0 or 1 by changing the position of respective switches. When the switch is in position 1 the input is connected to +5V internally and when the switch is in position 0 the input is connected to ground internally through the switch. Measure the voltages at the inputs and output for various combinations of inputs and record them in the table. It should be noted that all voltages are measured with respect to ground, so the negative

rminal of voltmeter should always be connected to ground while the positive rminal of the voltmeter should be connected to the point where the voltage is to be easured. We are using positive logic therefore if the voltage is 4.0 ± 1.0 V then it ould be considered in state 1 and if the voltage is 0.3 ± 0.3 V then it should be nsidered in state 0. States 1 and 0 of the inputs and the output can also be studied by nnecting an LED (light emitting diode) at the appropriate points. For this purpose e LED is provided in the kit. The LED indicates state 1 when it glows and it dicates state 0 when it is off. The negative terminal of the LED is already grounded ly the positive terminal is to be connected to the point where the state is to be ecked. By recording the states of various inputs and corresponding outputs verify e truth Table 1.

Prepare the table by considering 4.0 + 0.1 as 0 state and 0.3 + 0.3 V as state 1 in negative logic and show that the circuit follows the truth table of 3-input OR e (Table 2).

2. OR Gate

Assemble the circuit of 3-input OR gate as shown in Fig. 7

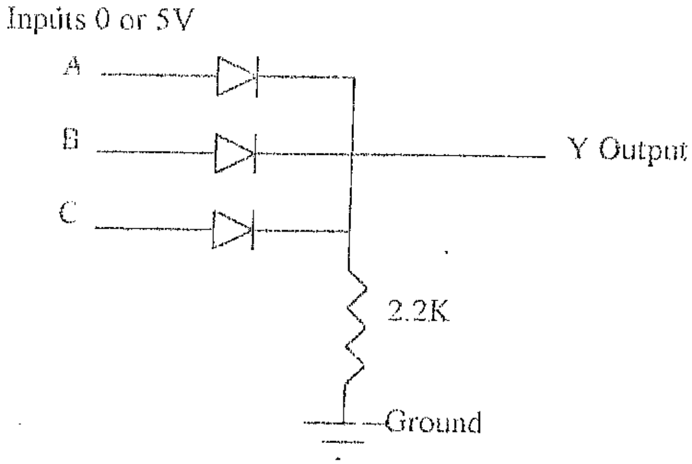


Fig. 7

Measure the Voltage levels at the inputs and the output for various oinations of inputs A, B and C, arrange them as in Table 2 and verify it. Inputs 0 are to be applied and voltages are measured as in Part A.

From the study of voltage levels show that the above circuit behaves as an gate for negative logic.

3. NOT Gate

Assemble the circuit for NOT gate as shown in Fig. 8

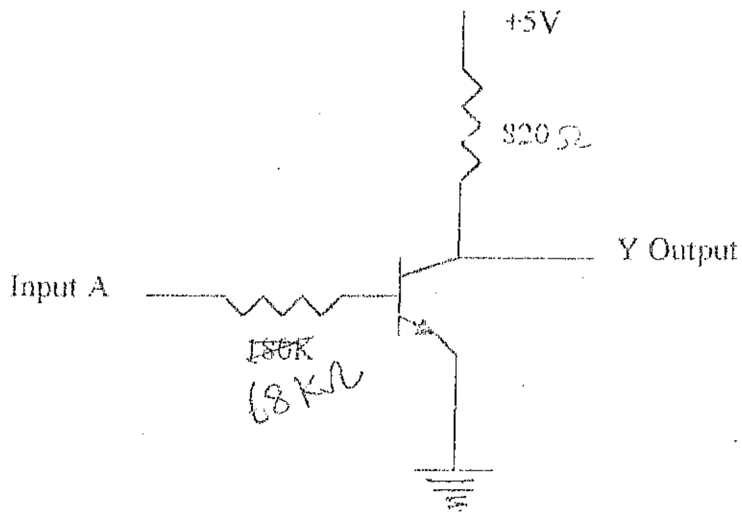


Fig 8

2. By changing the position of switch set the input A in state 0 or 1 and record the input and the output voltages of the gate.

3. From these voltages verify the truth Table 3.

4. NAND Gate

1. Assemble the circuit for 3-input NAND gate as shown in Fig. 9

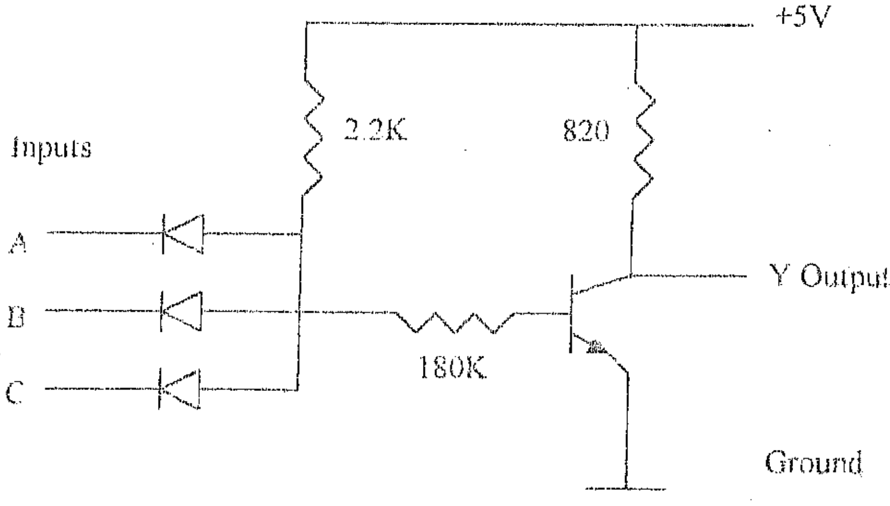


Fig. 9

2. Verify the truth Table 4 for various combinations of the inputs A, B, and C by measuring the various voltage levels at inputs and output as in part A and B

5. NOR Gate

1. Assemble the circuit for 3-input NOR gate as a own in Fig. 10

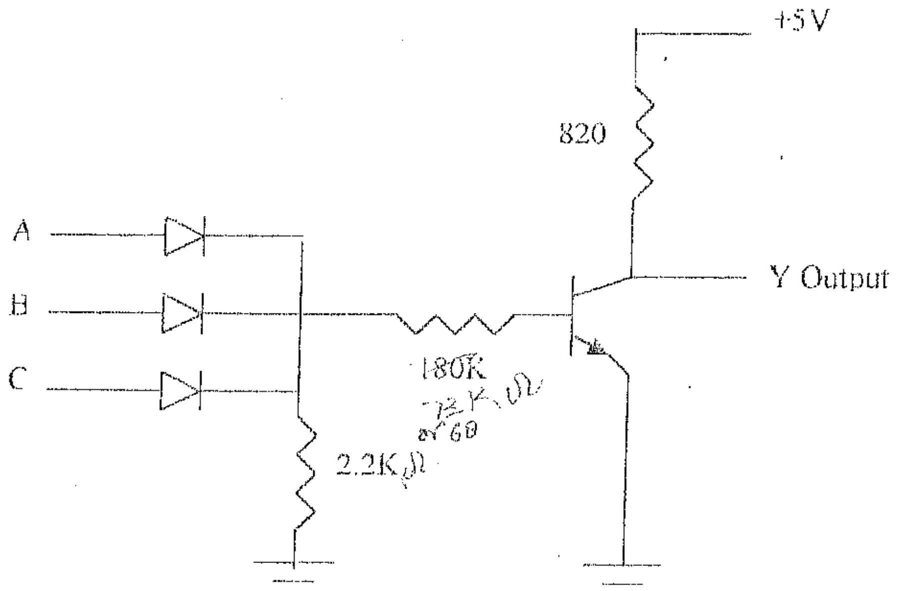


Fig. 10

Verify the truth Table 5 for various combinations of the inputs A, B and C by asuring the various voltage levels at inputs and output as in part A and B.

FERENCES:

Integrated Electronics - Millman and Halkias
Digital Fundamentals - Floyd
Principles of Digital Electronics - Malvino and Leach
Pulse, Digital and Switching Wave Farms - Millman and Taub

ESTIONS:

Voltages measured at different points are often found not to be 0 or 5 V (depending on the case). What could be the reason?
Discuss the importance of the voltmeter impedance in the measurements involved.
n the NOT gate circuit, how will the results change, if the base side or the ollector side resistance, respectively, is taken relatively large or small?
Diode-based logic gates are generally not used in practice. Can you give any eason?
How can you modify the NOT gate circuit without using diodes so that it becomes quivalent to a 3-input NAND gate?