Problem 1

Answer) $-0.8_{10} = \left(\frac{-8}{10}\right)_{10} = -[(8)_{10} \times (0.1)_{10}]$ $\cancel{= -[(1000)_2 \times (0.5)_{10} + (0.5)_{10}]}$

$\cancel{= -[(1000)_2 \times \{(0.1)_2 + (0.1)_2\}]}$

$= -[(1000)_2 \times (0.\overline{0011})_2]$

$= (-1)^1[1.0 \times 2^3]$

$F_1 = 1.0 \times 2^3 = 1.0 \times 2^{130-127}$

$F_2 = (-1)^1 \times 1.1\overline{0011} \times 2^{-4} = (-1)^1 \times 1.10011 \times 2^{123-127}$

$\Rightarrow F_3 = F_1 \times F_2 = (-1)^1 \times (1.0 \times 1.1\overline{0011}) \times 2^{(130-127+123)-127}$

$= (-1)^1 \times 1.1\overline{0011} \times 2^{126-127}$

$\therefore$ IEEE 64-bit representation that consists of sign, ~~magnitude~~ exponent & significand is as follows:

$s = 1$

$e = 1111\ 1110$

$f = 1001100110011001100110011001100$

---

Problem 2

Answer) $y = \lceil x \rceil$ ; $x = x_1 x_0 . x_{-1} x_{-2}$ ; $y = y_2 y_1 y_0$

| $x_1$ | $x_0$ | $x_{-1}$ | $x_{-2}$ | $y$ $\{y_2\, y_1\, y_0\}$ | Error = $y - x$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 000 | +0 |
| 0 | 0 | 0 | 1 | 001 | +3/4 |
| 0 | 0 | 1 | 0 | 001 | +1/2 |
| 0 | 0 | 1 | 1 | 001 | +1/4 |
| 0 | 1 | 0 | 0 | 001 | +0 |
| 0 | 1 | 0 | 1 | 010 | +3/4 |
| 0 | 1 | 1 | 0 | 010 | +1/2 |
| 0 | 1 | 1 | 1 | 010 | +1/4 |
| 1 | 0 | 0 | 0 | 010 | +0 |
| 1 | 0 | 0 | 1 | 011 | +3/4 |
| 1 | 0 | 1 | 0 | 011 | +1/2 |

Mohit Sharma, ID-110031631



| $x_1$ | $x_0$ | $x_{-1}$ | $x_{-2}$ | $y$ $\{y_2\, y_1\, y_0\}$ | Error $= y - x$ |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 011 | $+1/4$ |
| 1 | 1 | 0 | 0 | 011 | $+0$ |
| 1 | 1 | 0 | 1 | 100 | $+3/4$ |
| 1 | 1 | 1 | 0 | 100 | $+1/2$ |
| 1 | 1 | 1 | 1 | 100 | $+1/4$ |

$\therefore$, Maximal errors, $e^{+}_{max} = +3/4$

$$\text{Bias} = \frac{1}{16}\left[4\left(+\tfrac{1}{4}+\tfrac{1}{2}+\tfrac{3}{4}\right)\right] = \frac{3/2}{4} = +\frac{3}{8}$$

For $y_0$

| $x_1x_0 \backslash x_{-1}x_{-2}$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 1 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 1 | 0 | 0 | 0 |
| 10 | 0 | 1 | 1 | 1 |

For $y_1$

| $x_1x_0 \backslash x_{-1}x_{-2}$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | 1 | 0 | 0 | 0 |
| 10 | 1 | 1 | 1 | 1 |

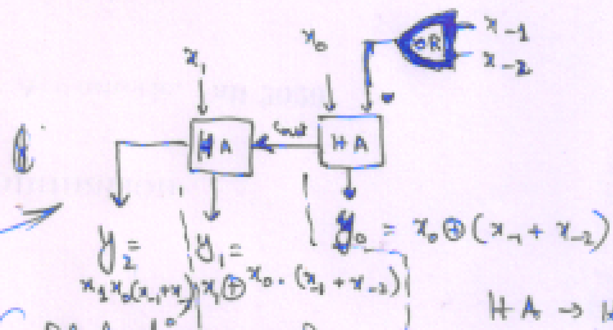
$$\Rightarrow y_0 = \bar{x}_0 x_{-2} + \bar{x}_0 x_{-1} + x_0 \bar{x}_{-1}\bar{x}_{-2}$$
$$= \bar{x}_0 (x_{-1} + x_{-2}) + x_0 (\bar{x}_{-1} . \bar{x}_{-2})$$
$$= \bar{x}_0 (x_{-1} + x_{-2}) + x_0 (\overline{x_{-1} + x_{-2}})$$
$$= x_0 \oplus (\overline{x_{-1} + x_{-2}})$$

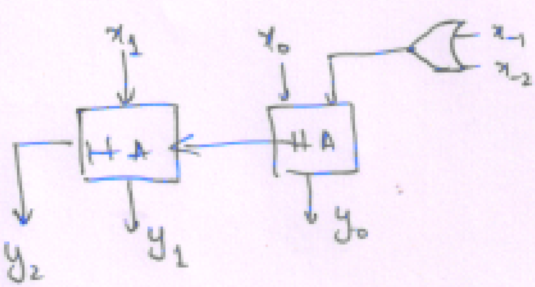
$$y_1 = x_1 \bar{x}_0 + x_1 . (\bar{x}_{-1} . \bar{x}_{-2}) + \bar{x}_1 x_0 . x_{-2} + \bar{x}_1 x_0 x_{-1}$$
$$= x_1 (\bar{x}_0 + \bar{x}_{-1} . \bar{x}_{-2}) + \bar{x}_1 x_0 (x_{-2} + x_{-1})$$
$$= x_1 (\overline{x_0 . (x_{-1} + x_{-2})}) + \bar{x}_1 . (x_0 . (x_{-2} + x_{-1}))$$
$$= x_1 \oplus (x_0 . (x_{-1} + x_{-2}))$$

For $y_2$

| $x_1x_0 \backslash x_{-1}x_{-2}$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 0 | 1 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

$$y_2 = x_1 x_0 (x_{-1} + x_{-2})$$



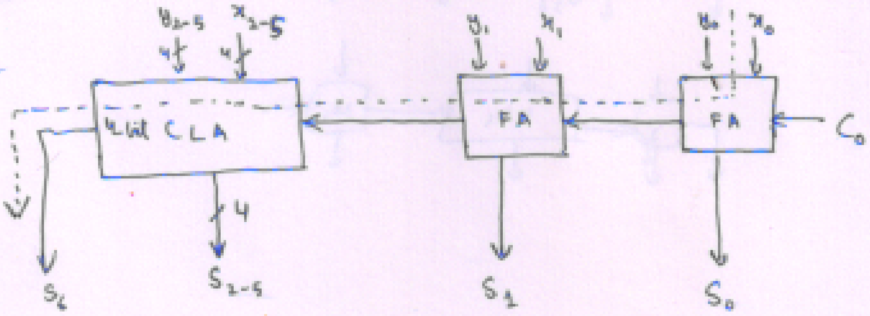

Block diagram of rounding scheme given as ceiling function

HA → Half adder
OR → OR gate

Problem 3)

Answer) For the following configuration of the CLA and the two Full Adder's, the critical path delay will be minimal

Config 1



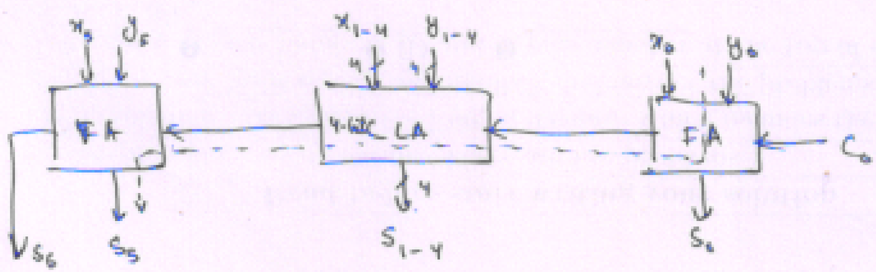

Critical path delay of 6-bit adder $= T^{FA}_{x/y \to C_{out}} + T^{FA}_{C_{in} \to C_{out}} + T^{CLA}_{C_0 \to C_4}$

$= 2\Delta_G + 2\Delta_G + 4\Delta_G$

Minimal critical path delay $= \boxed{8\Delta_G}$

Other configurations that are possible are

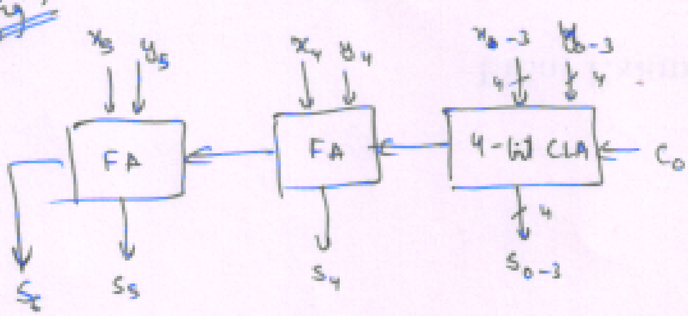
Config 2




$T_{critical} = T^{FA}_{x/y \to C_{out}} + T^{CLA}_{C_0 \to C_4} + T^{FA}_{C_{in} \to S_6}$

$= 2\Delta_G + 4\Delta_G + 3\Delta_G = 9\Delta_G$

Config 3




$T_{critical} = T^{CLA}_{x/y \to C_4} + T^{FA}_{C_{in} \to C_{out}} + T^{FA}_{C_{in} \to S}$

$= 4\Delta_G + 2\Delta_G + 3\Delta_G = 9\Delta_G$

$\therefore$ Minimal critical path delay $= 8\Delta_G$ for config. 1

Problem 4) Designing the 26 bit carry - select adder

$\Rightarrow$ Let 26 - bit carry select adder be divided into $l$ groups of length $k_1, k_2, \dots, k_l$

$\Rightarrow (l-1)\,2\Delta_G = 2k_l\,\Delta_g$ (For FA's for addition & assuming i/p's to MUX are available at exactly same time

$k_l = l - 1$ $\Rightarrow$ Group sizes are 1, 1, 2, 3, 4, ....

Also, $1 + \frac{l(l-1)}{2} \geq n \Rightarrow l(l-1) \geq 2n + 1$ $(n = 26)$

$\Rightarrow l(l-1) \geq 53$

$\therefore, l = 8$

And group size are, $k_1 = 1, k_2 = 1, k_3 = 2, k_4 = 3, k_5 = 4, k_6 = 5,$
$k_7 = 6, k_8 = 4$

$\therefore, C_{select} =$ 50 FA's + 1 HA

$T_{select} = 1\Delta_g + 2 \times 7\,\Delta_G = 15\,\Delta_G$

* Designing the 26 - bit carry - skip adder

$\Rightarrow$ Let 26 - bit adder be divided into $k$ groups of equal sizes

$\Rightarrow T_{carry} = (k-1)t_n + t_b + \left(\frac{n}{k} - 2\right)(t_s + t_b) + (k-1)t_n$

$= \left(4k + \frac{2n}{k} - 7\right)\Delta_G$ $(t_n = 2\Delta_G,\ t_s = t_B = \Delta_G)$

$\Rightarrow \frac{dT_{carry}}{dk} = 4 - \frac{2n}{k^2} = 0 \Rightarrow k = \sqrt{\frac{n}{2}} \Rightarrow k = \sqrt{\frac{26}{2}} = \sqrt{13}$

$T_{opt} = \left(4\sqrt{13} + \frac{2(26)}{\sqrt{13}} - 7\right)\Delta_G = \left(\frac{52 + 52 - 7\sqrt{13}}{\sqrt{13}}\right)\Delta_G = \left(\frac{104 - 7\sqrt{13}}{\sqrt{13}}\right)\Delta_G$

$= 21.8\,\Delta_G$

$\therefore C_{skip} =$ 26 FA's

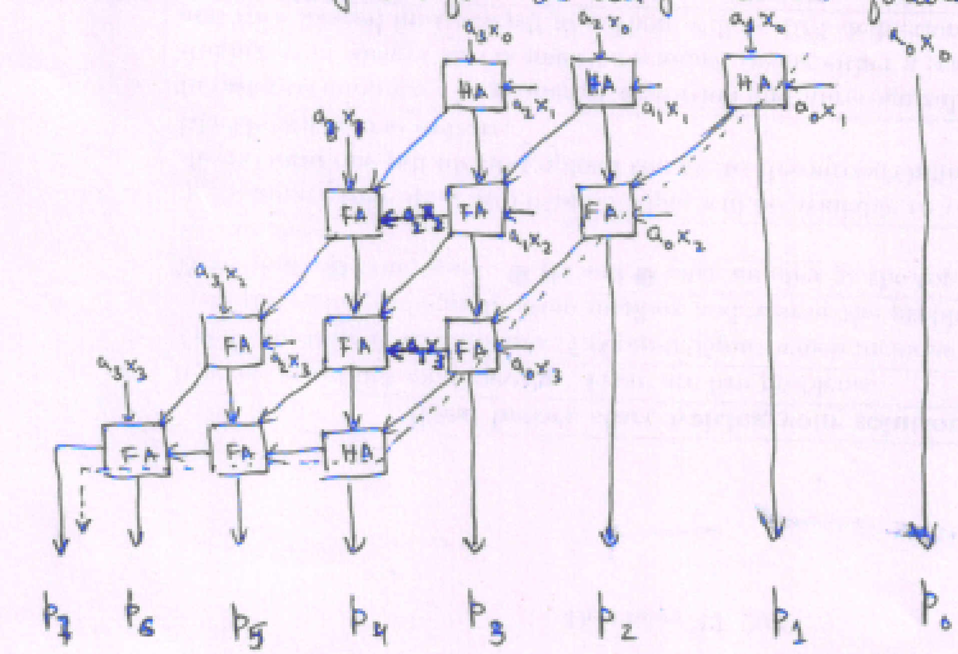
$T_{skip} = 21.8\,\Delta_G$

Hence, $C_{select} > C_{skip}$ & $T_{skip} > T_{select}$ $\Rightarrow$ (B)

Problem 5) $A = (a_3\ a_2\ a_1\ a_0)$ ; $X = (x_3\ x_2\ x_1\ x_0)$ then the seven product bits $P = (p_6\ p_5\ p_4\ p_3\ p_2\ p_1\ p_0)$ can be obtained as follows:

$$
\begin{array}{cccccccc}
 & & & & a_3 & a_2 & a_1 & a_0 \\
 & & & & x_3 & x_2 & x_1 & x_0 \\
\hline
 & & & & a_3x_0 & a_2x_0 & a_1x_0 & a_0x_0 \\
 & & & a_3x_1 & a_2x_1 & a_1x_1 & a_0x_1 & \\
 & & a_3x_2 & a_2x_2 & a_1x_2 & a_0x_2 & & \\
 & a_3x_3 & a_2x_3 & a_1x_3 & a_0x_3 & & & \\
\hline
p_7 & p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0
\end{array}
$$

The block diagram for the design is as follows.




No. of FA's required = 8

No. of HA's required = 4

Time delay of multiplier = Time delay to generate partial products + Time delay for the ~~array multiplier~~ partial products addition

$$= 1\Delta_G + (1\Delta_G + 2\Delta_G + 2\Delta_G + 1\Delta_G + 2\Delta_G + 2\Delta_G)$$

$$= 11\Delta_G$$