Assignment – 4

1. (20 marks) Build a 18-bit carry-select adder. Decide the number of groups and the size of each group. Estimate the time delay of your design.

Ans.) 18-bit carry-select adder => n = 18

Let the 18-bit carry select adder be divided into L groups, each group of length k_1, k_2,...k_L, then, the following inequality holds:

=> $1 + (L\,(L-1)) / 2 \geq 18$ => $L(L - 1) \geq 34$

Since, L is an integer, the minimum value of L that satisfies the above relation is L = 7. Hence, the number of groups in the carry-select adder are 7.

The group size of each group would then be $k_1 = 1$, $k_2 = 1$, $k_3 = 2$, $k_4 = 3$, $k_5 = 4$, $k_6 = 5$, $k_7 = 2$

For a group l of length k_l it takes $(l-1)\times 2\,\Delta_G$ for its carry-in c_j signal to be available. And the latency of k_l-bit RCA is $2k_l\,\Delta_G$

Hence, time delay of this design would be = $1\Delta_G + (7 - 1)2\Delta_G = 13\,\Delta_G$

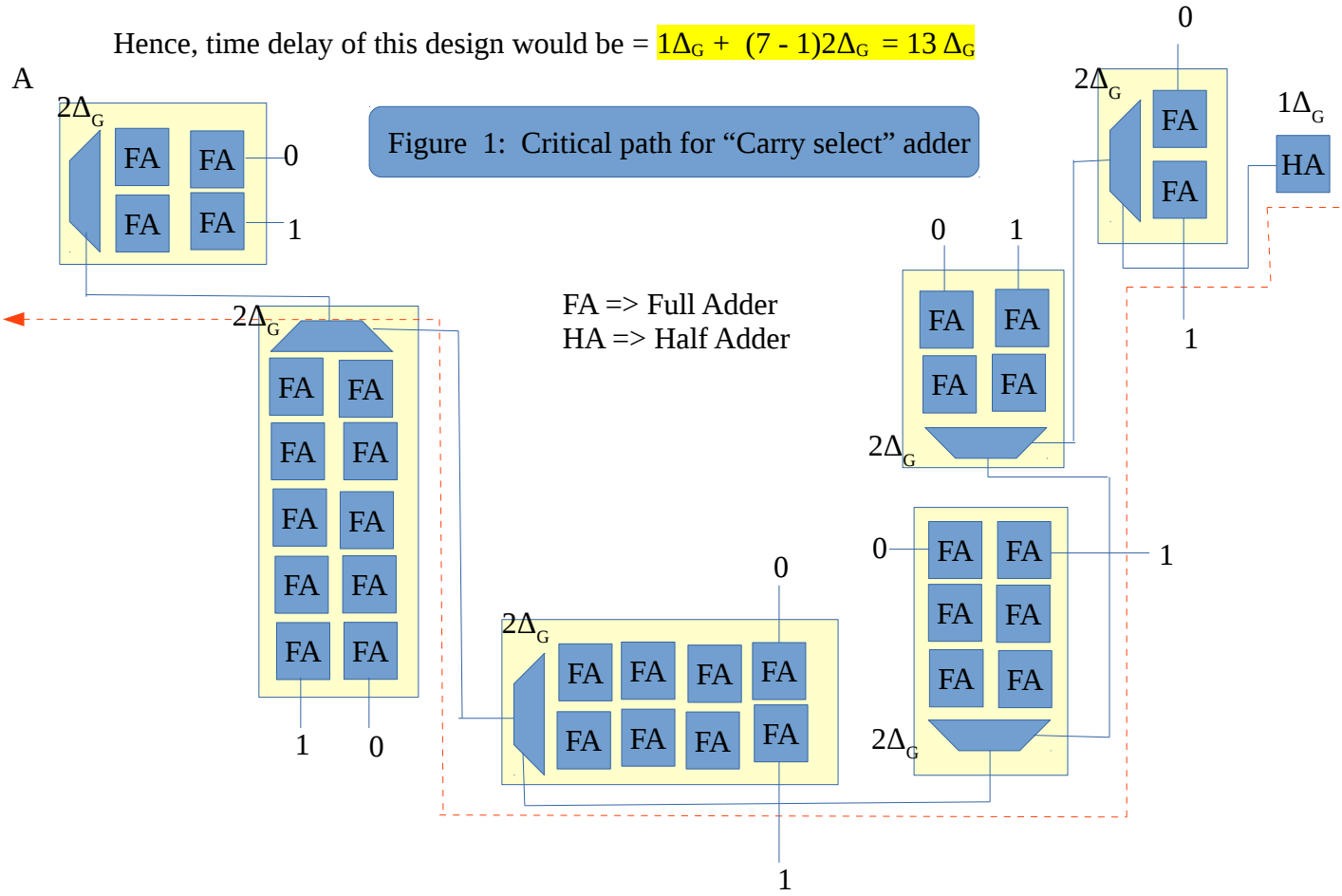


Figure 1: Critical path for "Carry select" adder

2. (20 marks) Build a 18-bit carry-skip adder. Decide the number of groups and the size of a group. Estimate the time delay of your design.

Ans.) Let the following three time delays be defined:

t_r denote carry ripple time through one bit
$t_s(k)$ denote the time to skip on group
t_b denote the time delay of an OR gate

For a n-bit carry-skip adder, of n/k groups where k is the size of the group,

$$T_{carry} = (k-1)\,t_r + t_b + (n/k - 2)(t_s + t_b) + (k-1)\,t_r$$
$$= (4k + 2n/k - 7)\,\Delta_G$$

where $t_r = 2\Delta_G$ and $t_b = t_s = \Delta_G$

Optimal size of k => $k_{opt} = \sqrt{\frac{n}{2}}$

Hence, for n = 18, $k_{opt} = 3$ => Number of groups = $n / k_{opt} = 18 / 3 = 6$

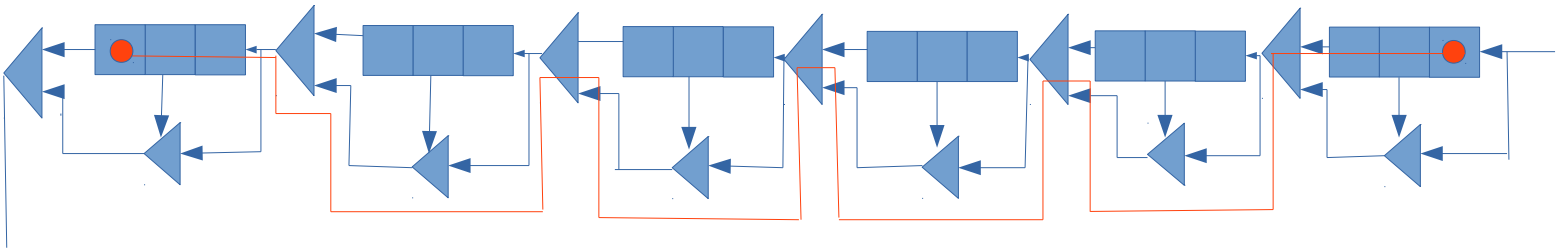


Figure 2 : Showing the critical path for "Carry Skip Adder"

=> Size of the group = $k_{opt} = 3$

=> Optimal time delay of the design, $T_{opt} = (4\,k_{opt} + 2n/k_{opt} - 7)\,\Delta_g$
$= (4*3 + (2*18)/3 - 7)\,\Delta_g = 17\Delta_g$

3. (20 marks) Build a carry-save adder that performs X = A + B + C + D + E, where each of operands A, B, C, D, and E has 4 bits. Draw a full diagram for the carry-save adder and estimate the complexities using both (3, 2) and (2, 2) counters as building blocks. Explicitly show a critical path.

Ans.) Since, A, B, C, D and E are 4 bit operands => A, B, C, D, E $\in$ [0, 2^4 - 1] = [0-15]
Hence, the sum of four such numbers will have no more than (5 x [0-15]) $\subset$ [0, 2^{7-} 1] i.e. 7 bits

=> Organize the architecture diagram in at most 7 columns.

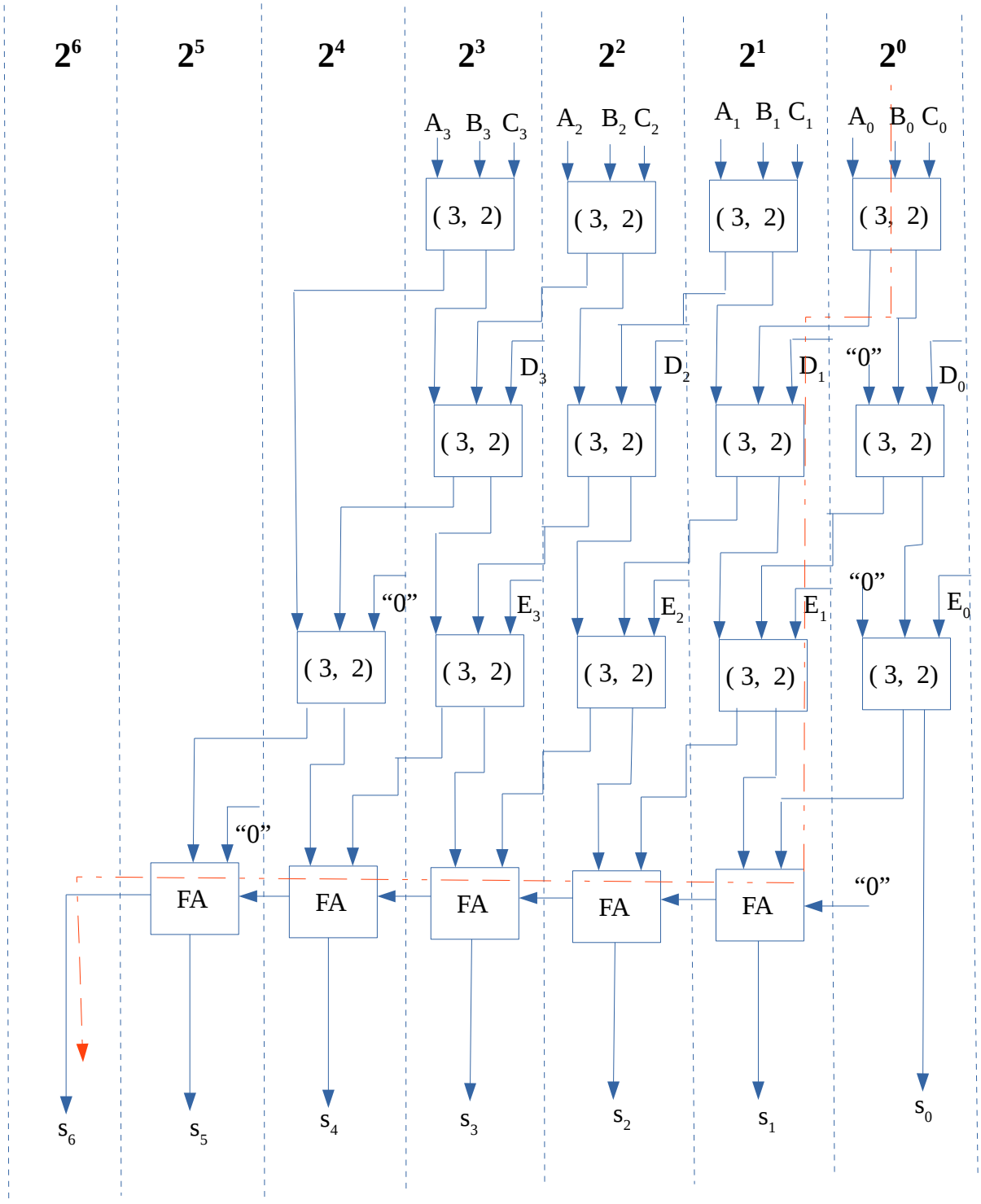


Figure 3: "Carry Save Adder" using (3,2) as building blocks

The architecture complexities using only (3,2) or FA as building blocks are:

* Circuit complexity: C = 18(3,2)'s = 18 FA
* Critical path delay: T = 8 * ($2\Delta_G$) = 16 Δ_G

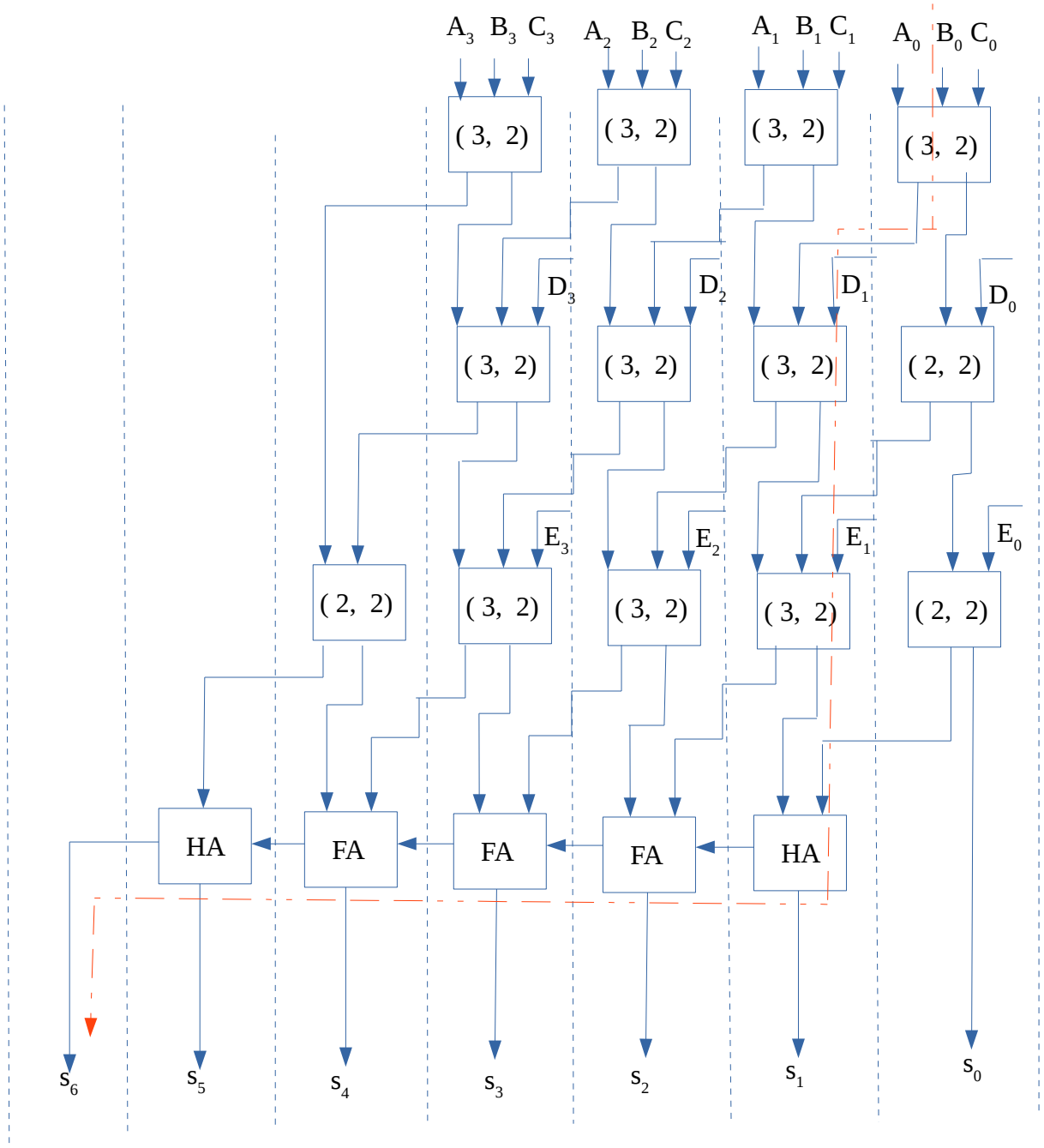


Figure 4: "Carry Save Adder" using (2,2) as building blocks

The architecture complexities using both (3,2) or FA and (2,2) or HA as building blocks are:

* Circuit complexity: C = 13(3,2)'s + 5(2,2)'s = 13 FAs + 5HAs
* Critical path delay: T = 6 ($2\Delta_G$) + 2($1\Delta_G$) = 14 Δ_G

4. (20 marks) Consider multiplication of a 5-bit multiplicand A and a 4-bit multiplier X. Design a high-speed multiplier realizing this multiplication operation. Assume that (3, 2) and (2, 2) counters are used for carry save addition and carry-propagate addition. Show the steps in dot diagram or draw a block diagram for your design. How many (3, 2) and (2, 2) counters are required? Assume that Δ (3,2) = 2Δ G and Δ (2,2) = Δ G . What is time delay of your multiplier?

Ans.) Let A = $(a_4a_3a_2a_1a_0)$ and X = $(x_3x_2x_1x_0)$ then the product bits P = $(p_8p_7p_6p_5p_4p_3p_2p_1p_0)$ can be obtained as follows:

				a_4	a_3	a_2	a_1	a_0
					x_3	x_2	x_1	x_0
				a_4x_0	a_3x_0	a_2x_0	a_1x_0	a_0x_0
			a_4x_1	a_3x_1	a_2x_1	a_1x_1	a_0x_1	
		a_4x_2	a_3x_2	a_2x_2	a_1x_2	a_0x_2		
	a_4x_3	a_3x_3	a_2x_3	a_1x_3	a_0x_3			
p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

* The 20 partial product bits can be generated using 20 two-input AND gates and hence requires one gate delay

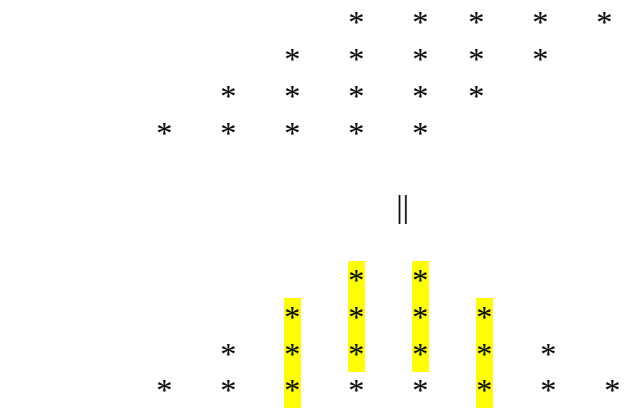
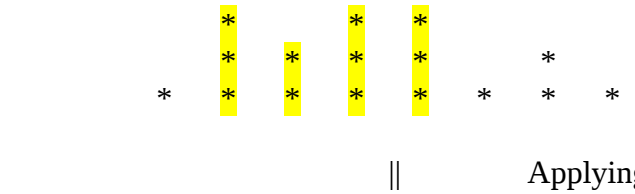


Figure 5: Dot diagram depicting the usage of (3,2)'s and (2,2)'s for adding the partial product terms

Applying 4 (3,2)'s (1-level CSA)



Applying 3 (3,2)'s and 1 (2,2) (1-level CSA)

(CPA: 4 (3,2)'s and 3 (2,2)'s)

* Let the partial product bit be denoted with a *. Then, the CSA tree of 20 partial product bits forms an isoceles trapezoid with 4 rows and base consisting of 8 asterisk's. Since, the height of the trapezoid is 4, it requires 2 levels of CSA before the final CPA.

* Number of (3,2) counter's required = 11
* Number of (2,2) counter's required = 4

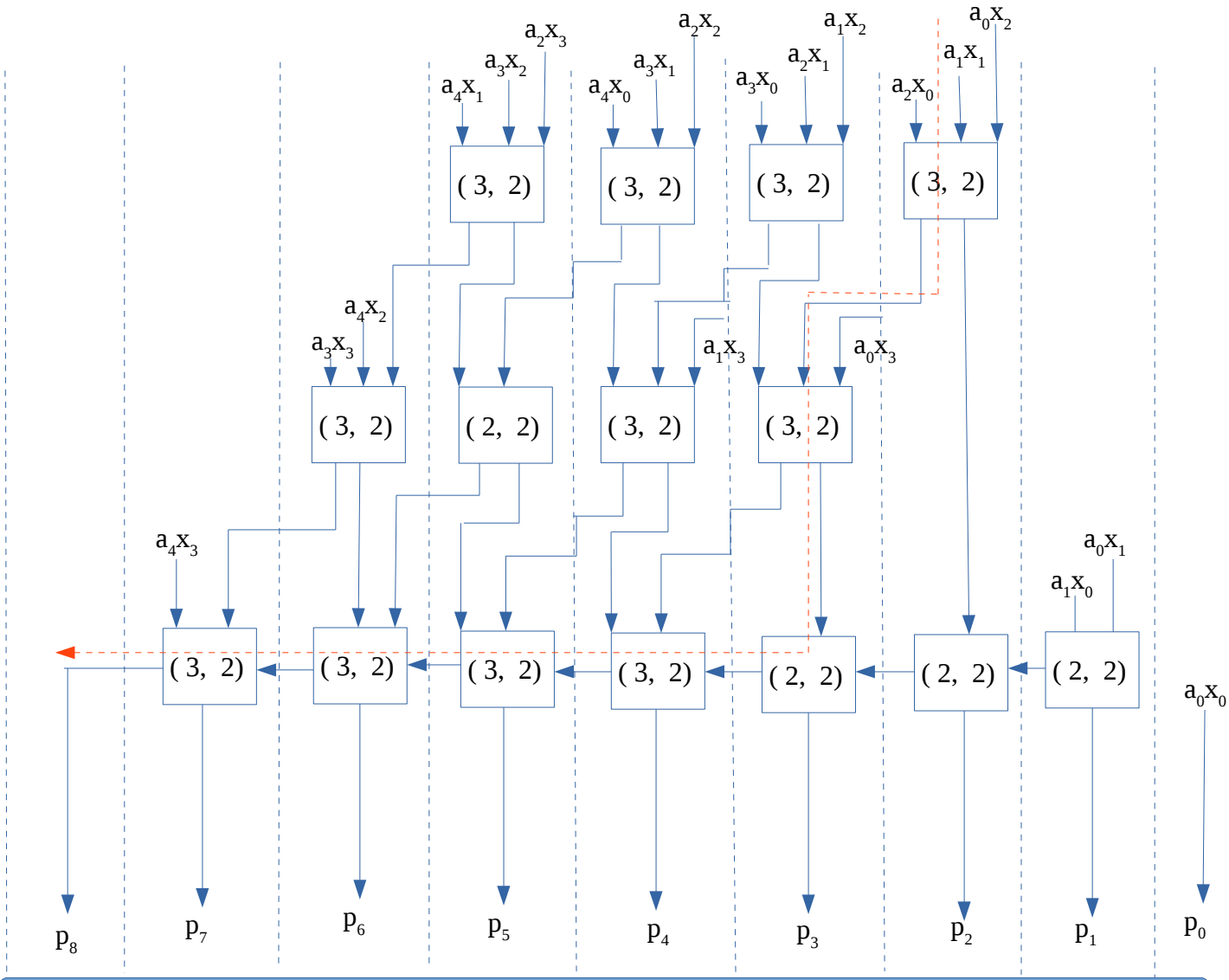


Figure 6 : Block diagram depicting the usage of (3,2)'s and (2,2)'s for adding the partial product terms

* Time delay of the multiplier = Time to form the partial product terms (1 gate delay for the 2 input AND gates) + Time for CSA to give actual product bits (Critical path highlighted in red in Figure 6)

= $1\,\Delta_G$ + $(2 + 2 + 1 + 2 + 2 + 2 + 2)\,\Delta_G$
= $14\Delta_G$

5. (20 marks) Consider multiplication of a 5-bit multiplicand A and a 4-bit multiplier X. Design an array multiplier realizing this multiplication operation. Assume that FA and HA are used as building cells. Draw a block diagram for your design. How many FAs and HAs are required? Assume that Δ FA = 2Δ G and Δ HA = Δ G . What is time delay of your design?

Ans.)

Let A = ($a_4a_3a_2a_1a_0$) and X = ($x_3x_2x_1x_0$) then the product bits P = ($p_8p_7p_6p_5p_4p_3p_2p_1p_0$) can be obtained as follows:

				a_4	a_3	a_2	a_1	a_0
			*		x_3	x_2	x_1	x_0
				a_4x_0	a_3x_0	a_2x_0	a_1x_0	a_0x_0
			a_4x_1	a_3x_1	a_2x_1	a_1x_1	a_0x_1	
		a_4x_2	a_3x_2	a_2x_2	a_1x_2	a_0x_2		
+	a_4x_3	a_3x_3	a_2x_3	a_1x_3	a_0x_3			
p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

Assuming that the partial product bits $a_i x_j$, i = 0,...,4 and j = 0,...,3, have been generated, an array multiplier realizing the multiplication operation can be designed using FA's and HA's as follows:

HA => Half Adder
FA => Full Adder

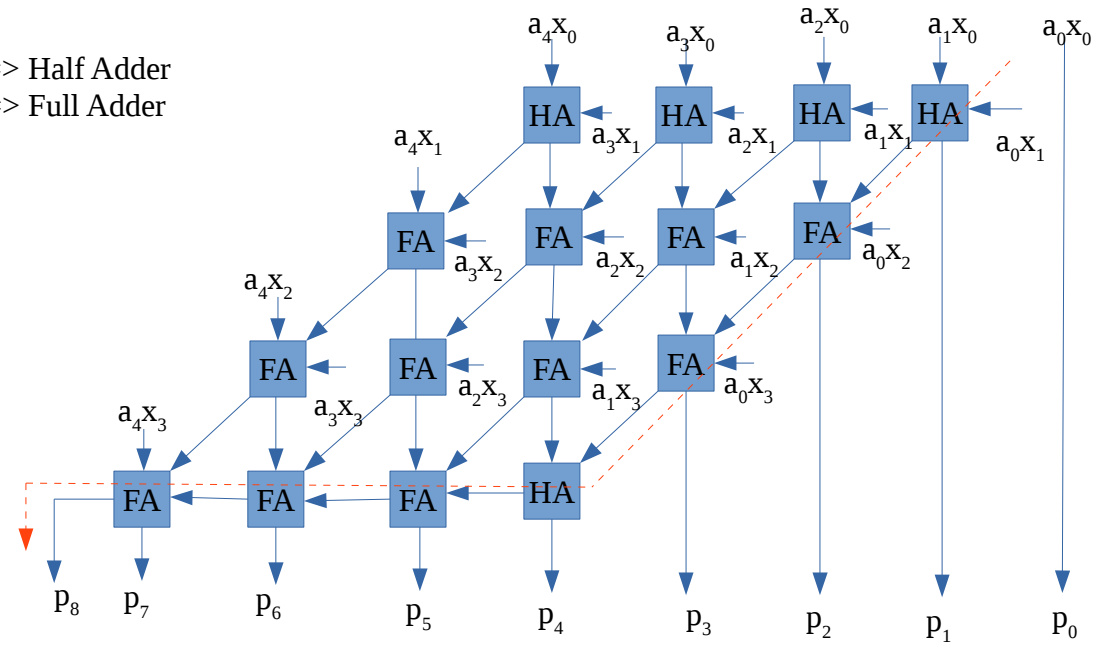


Figure 7 : Block diagram for multiplication of 5-bit multiplicand A and a 4-bit multiplier X

* Number of Full Adder's required = 11
* Number of Half Adder's required = 5

* Time delay for the design = Time to form the partial product terms (1 gate delay for the 2 input AND gates) + Time to get actual product bits (Critical path highlighted in red in Figure 7)

$= 1\,\Delta_G + (1 + 2 + 2 + 1 + 2 + 2 + 2)\Delta_G$

$= 13\Delta_G$

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6. (no marks) Let a residue number system (RNS) be given by $(m_2, m_1, m_0) = (15, 14, 13)$.
(a) Solve dynamic range for the RNS.
(b) Find the RNS representations for $A = 19_{10}$ and $B = 22_{10}$. Perform $C = A \times B$ in the RNS.
(c) How many bits are required to represent a number with respect to this RNS?

Ans.)

a) Dynamic range for the RNS(15,14,13), M = 15 * 14 * 13 = 15 * 182 = 2730
=> Range = [0, 2729]

b) RNS representation for $A = 19_{10}$ is (19 % 15, 19 % 14, 19 % 13) = (4, 5, 6)
RNS representation for $B = 22_{10}$ is (22 % 15, 22 % 14, 22 % 13) = (7, 8, 9)
C = A x B => C = (4*7, 5*8, 6*9)
= (28, 40, 54)
= (13, 12, 2) RNS (15,14,13)

c) Bits required to represent a number w.r.t this RNS = 4 + 4 + 4 = 12
