Chapter 5. Fast Addition (Part 1)

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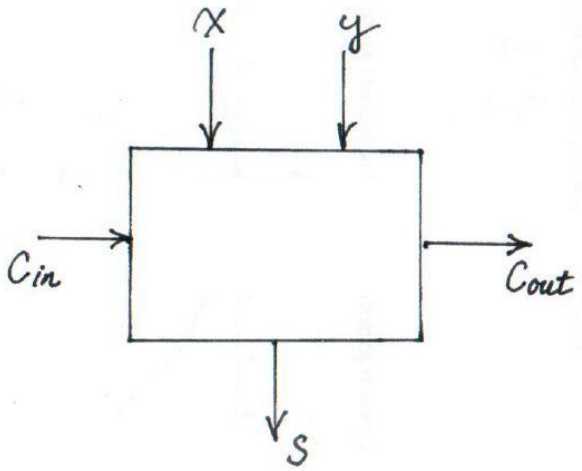
Single-digit Adder

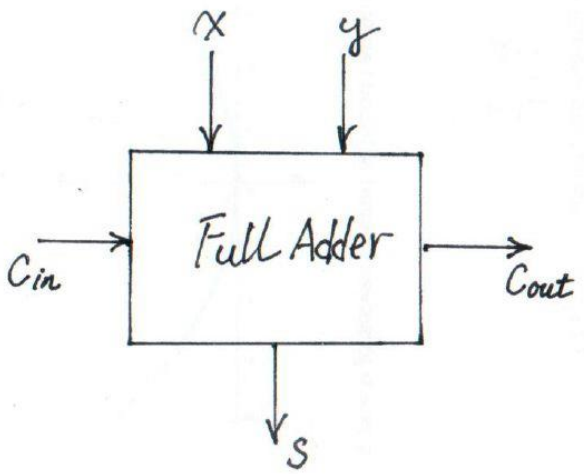
1. Consider adding two decimal digits
   - s = x + y, where x, y, and s are single digit numbers.
   - There is also a carry-in c_{in} and a carry-out c_{out}.



2. Can you write s and c_{out} as functions of x, y, and c_{in}?

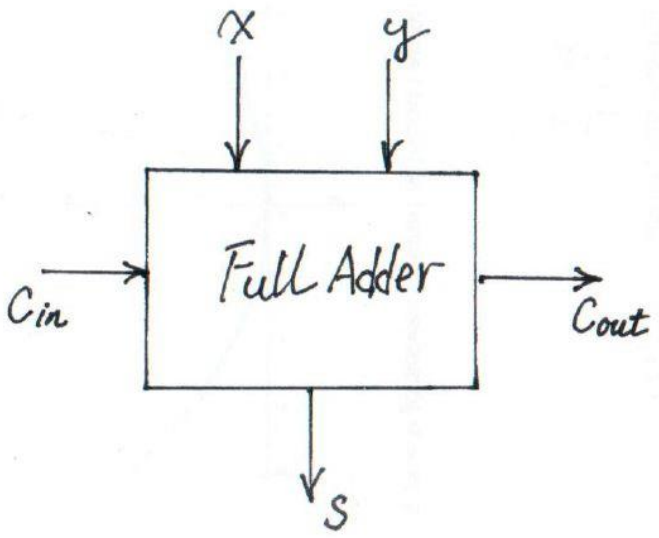
Full Adder

1. Now consider designing a one-bit adder (full adder):
   - S = x + y, where x and y are one-bit operands, s one-bit sum.
   - There is also one-bit carry-in c_{in} and one-bit carry-out c_{out}.



Full Adder

2. Arithmetic equations for one-bit adder:
   - $s = (x + y + c_{in}) \bmod 2$, and $c_{out} = [(x + y + c_{in}) / 2]$.



3. What are the logic equations for the full adder?

Full Adder

4. Recall how to design a circuit for this as a digital logic design problem:
   1) create a truth table
   2) write Karnaugh map
   3) optimise Karnaugh map
   4) obtain logic equation
   5) draw the circuit

Full Adder

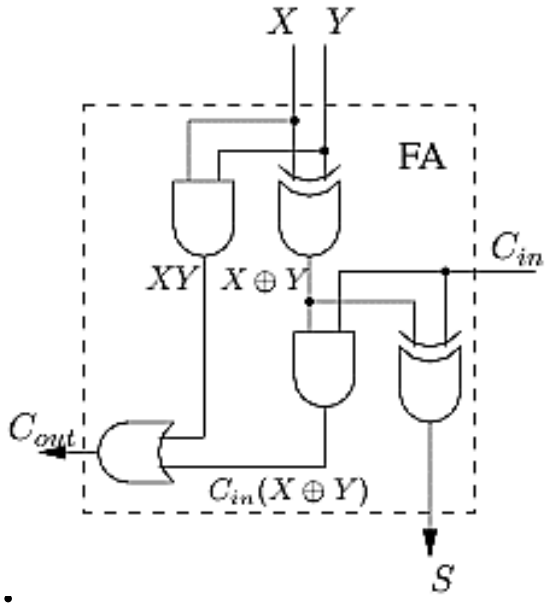
- Arithmetic equations:
  - $S = (X + Y + C_{in}) \bmod 2$, and $C_{out} = [(X + Y + C_{in}) / 2]$.
- Truth table:

X	Y	Cin	S	Cout
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

- Logic equations: (Karnaugh map step omitted)
  - $S = X \oplus Y \oplus C_{in}$, $C_{out} = XY + C_{in}(X \oplus Y)$

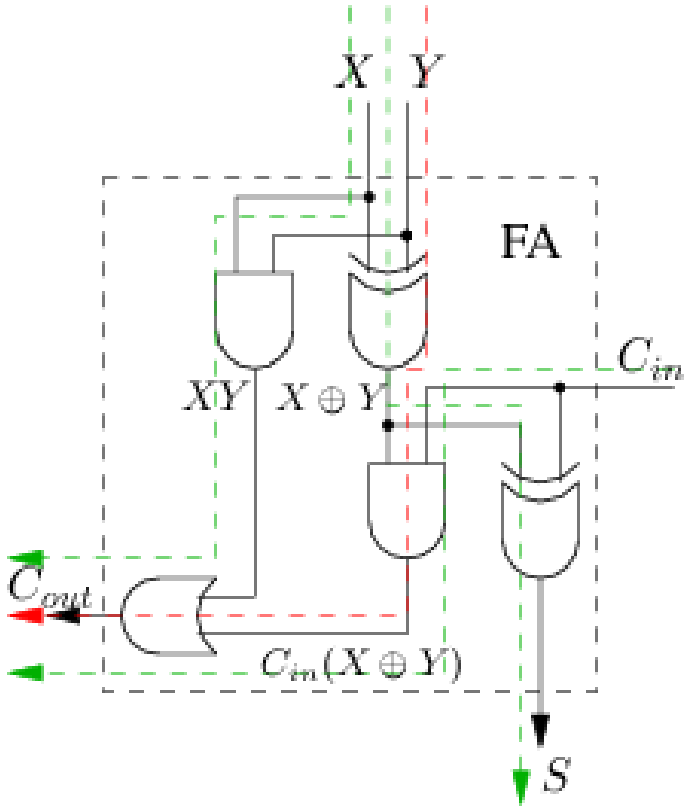
Full Adder

1. Representation of the inputs and outputs:
   - Input: X, Y, C_{in} and Output: S, C_{out}
   - All are one-bit binary numbers
2. Output logic functions:
   - $S = X \oplus Y \oplus C_{in}$, $C_{out} = XY + C_{in}(X \oplus Y)$
   - S is the sum bit, and C_{out} is the carry-out bit.
3. Circuit diagram for the 1-bit adder shown:
4. Space complexity (C) and critical path delay (T):
   - C = 2 AND + 1 OR + 2 XOR
     - 5 gates in total.
   - Critical path delay?



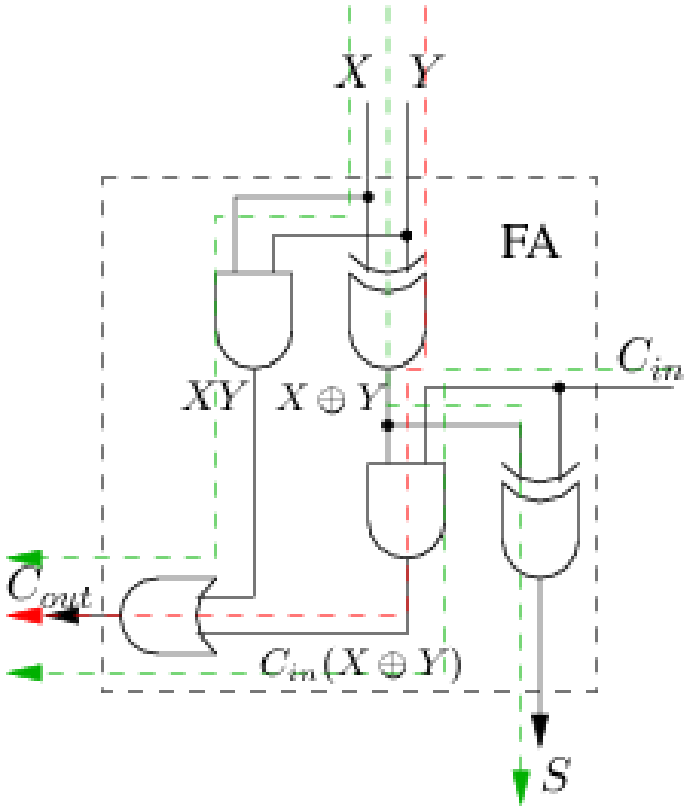
Critical Path Delay for Full Adder

- First to find the critical path:
  - X/Y → (red dashed line) →C_{out}
- Then find its delay
  - $T = 3 \Delta_G$



Finding Critical Path (cp)

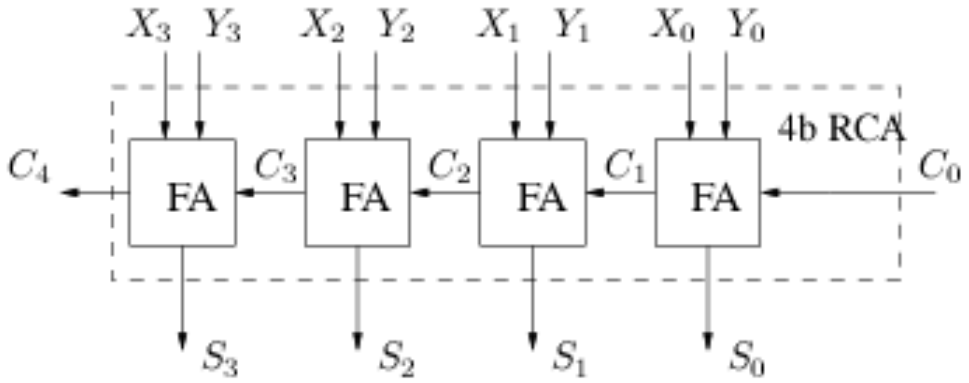
Input	Output	Delay
X/Y	S	$2\Delta_G$
X/Y	C_{out}	$3\Delta_G$ → cp
C_{in}	S	Δ_G
C_{in}	C_{out}	$2\Delta_G$



- Next we will show how to use FA as building blocks to make ripple-carry adder.

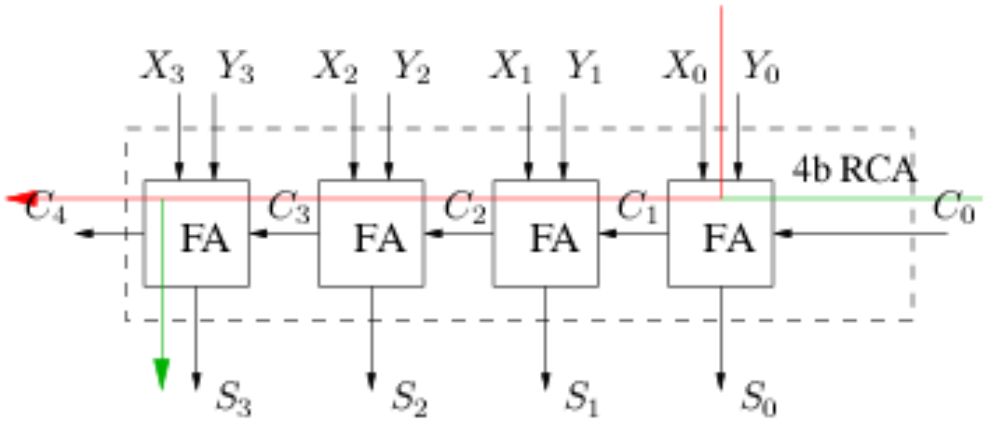
Ripple Carry Adder: 4-bit RCA

1. Algorithm for 1-bit addition:
   - $S_i = X_i \oplus Y_i \oplus C_i$, $C_{i+1} = X_iY_i + C_i(X_i \oplus Y_i)$, i=0,1,2,3.
2. Circuit for the 4-bit ripple carry adder:



3. Complexities:
   - C = 4 FA = 8AND + 4OR + 8XOR
   - What is its critical path delay?

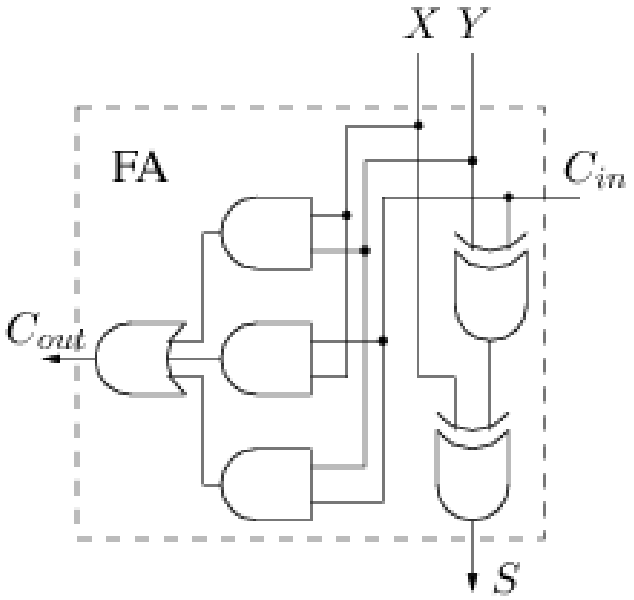
Ripple Carry Adder: 4-bit RCA



- Critical path (depending on the delay table for FA)
  - $X_0/Y_0 \rightarrow C_1 \rightarrow C_2 \rightarrow C_3 \rightarrow C_4$
- Critical path delay
  - $T = 3\Delta_G + 2\Delta_G + 2\Delta_G + 2\Delta_G = 9\Delta_G$
  - Or, $T = 4\Delta_{FA} = 8\Delta_G$ (as in textbook)
  - why different?

FA and RCA: alternate design

1. Algorithm for FA:
   - $S = X \oplus Y \oplus C_{in}$, $C_{out} = XY + C_{in}X + C_{in}Y$
2. Circuit complexity and critical path delay for FA:
   - C = 3 AND + 1 OR + 2 XOR
     - 6 gates in total.
   - $T = 2\Delta_G$
3. A 4-bit RCA built with this FA:
   - C = 4 FA = 12AND + 4OR + 8XOR
   - $T = 8\Delta_G$

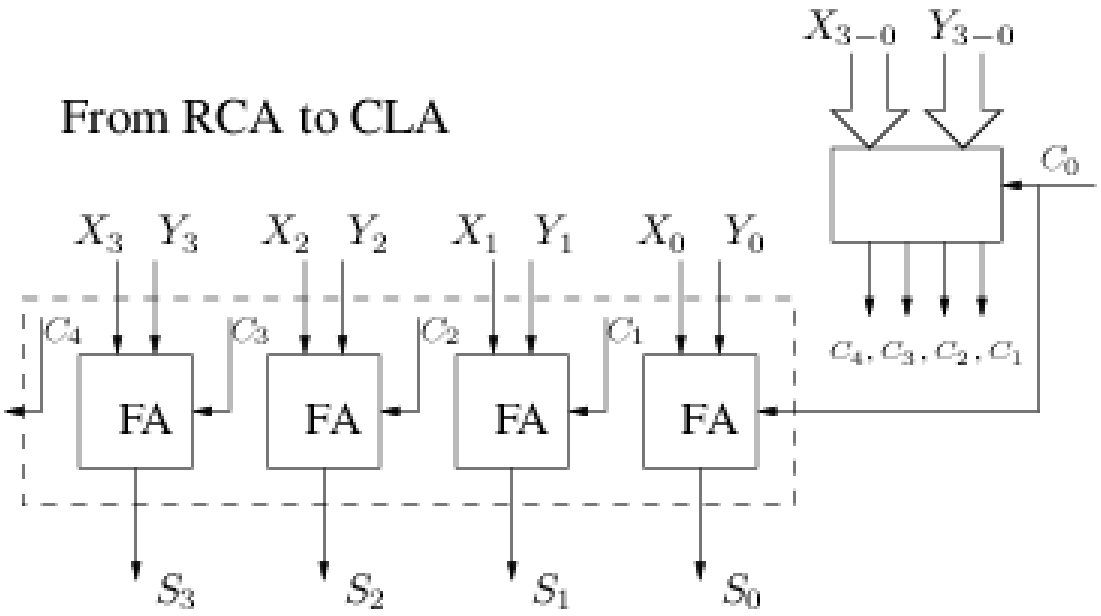


Ripple Carry Adder Complexities

- 4-bit RCA:
  - Circuit complexity
    - 4 FA:
  - Critical path delay:
    - $4\Delta_{FA} = 8\Delta_G$
- *n*-bit RCA:
  - Circuit complexity
    - *n* FA:
  - Critical path delay:
    - $n\Delta_{FA} = 2n\Delta_G \rightarrow O(n)$
- RCA is the simplest and also the slowest adder.

To Speed up RCA

- Idea:
  - In order to cut off the carry chain, the carries c_i are generated separately.



Carry-Lookahead Addition

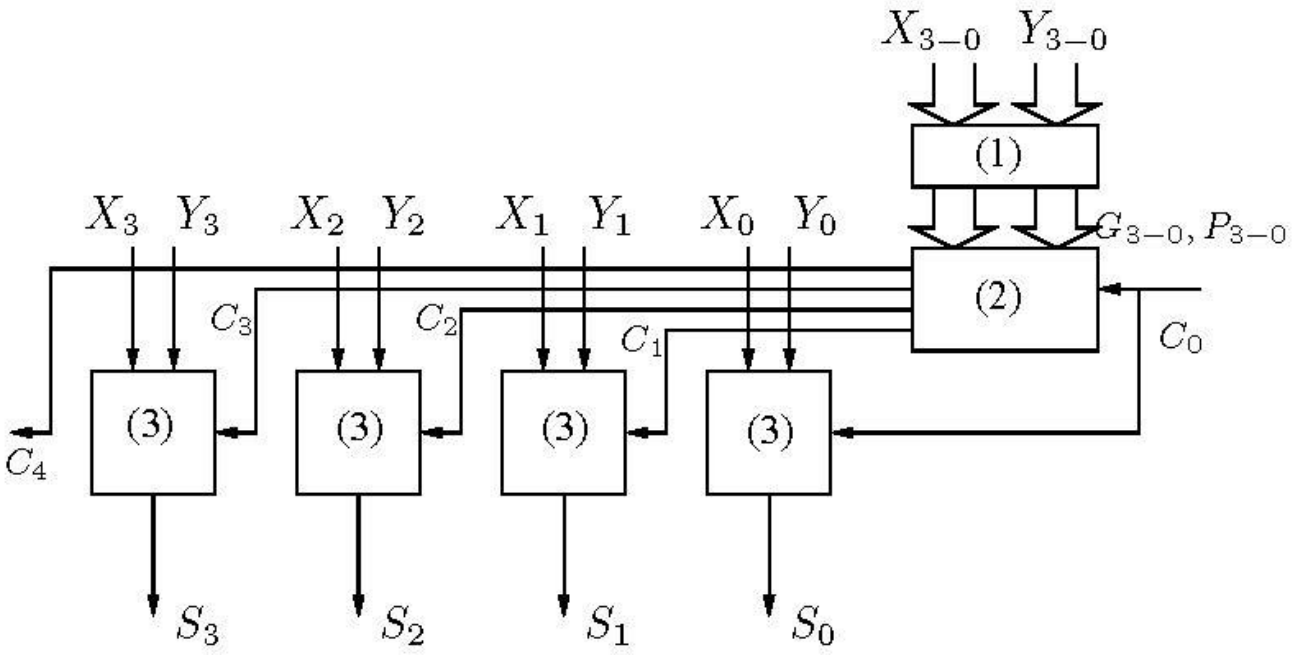
- Let $\begin{cases} G_i = x_i y_i \\ P_i = x_i \oplus y_i \end{cases}$ for $i = 0, 1, 2, 3.$ (1)

- Then $\begin{cases} c_1 = G_0 + c_0 P_0 \\ c_2 = G_1 + c_1 P_1 = G_1 + G_0 P_1 + c_0 P_0 P_1 \\ c_3 = G_2 + G_1 P_2 + G_0 P_1 P_2 + c_0 P_0 P_1 P_2 \\ c_4 = G_3 + G_2 P_3 + G_1 P_2 P_3 + G_0 P_1 P_2 P_3 + c_0 P_0 P_1 P_2 P_3 \end{cases}$ (2)

- And $S_i = x_i \oplus y_i \oplus c_i$ for $i = 0, 1, 2, 3.$ (3)

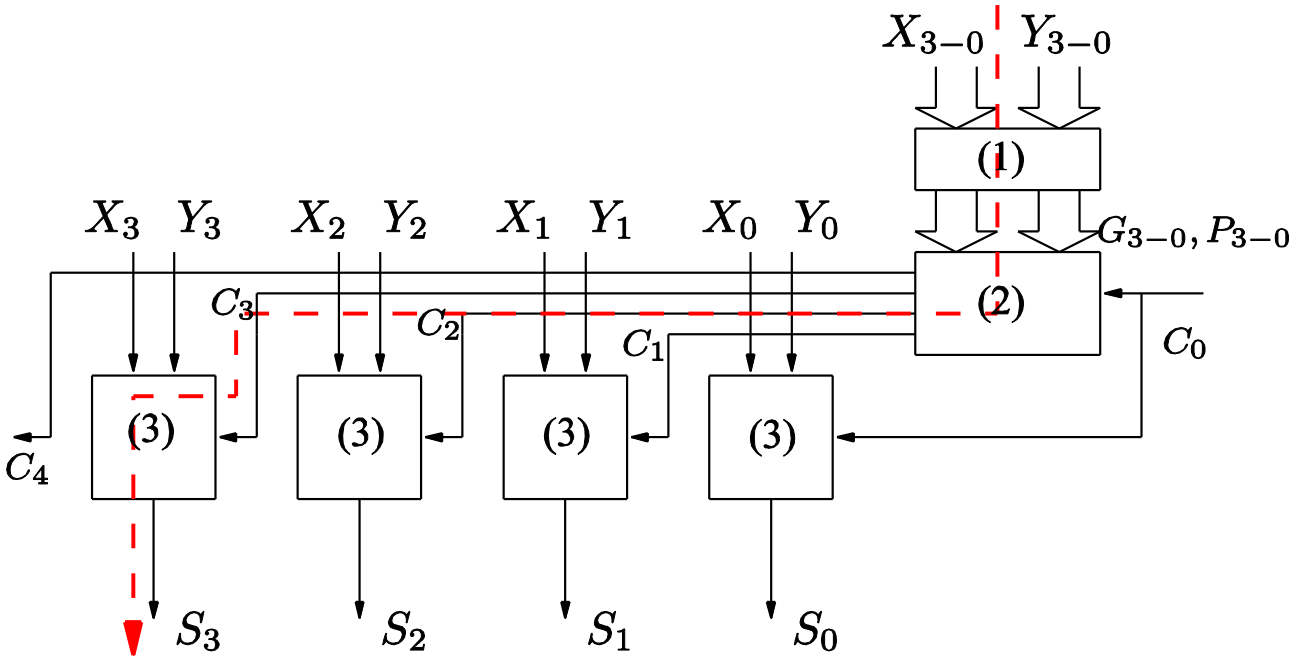
Carry-Lookahead Adder

- Circuit Diagram



Carry-Lookahead Adder: Delay

- Critical Path Delay:



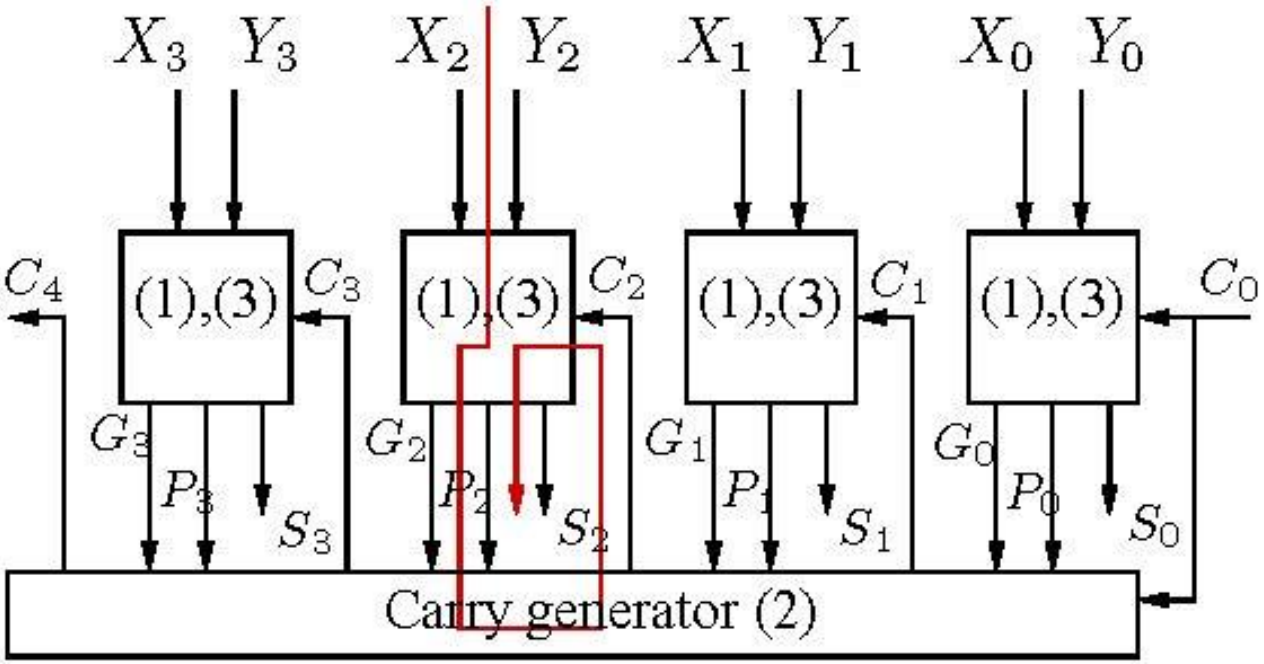
- $T = 1\Delta_G + 2\Delta_G + 1\Delta_G = 4\Delta_G$ √
- $T = 1\Delta_G + 2\Delta_G + 2\Delta_G = 5\Delta_G$ (textbook)

Construction of n-bit CLA

- Change equation (3) into

  And $S_i = P_i \oplus c_i$ for $i = 0, 1, 2, 3$. (3)

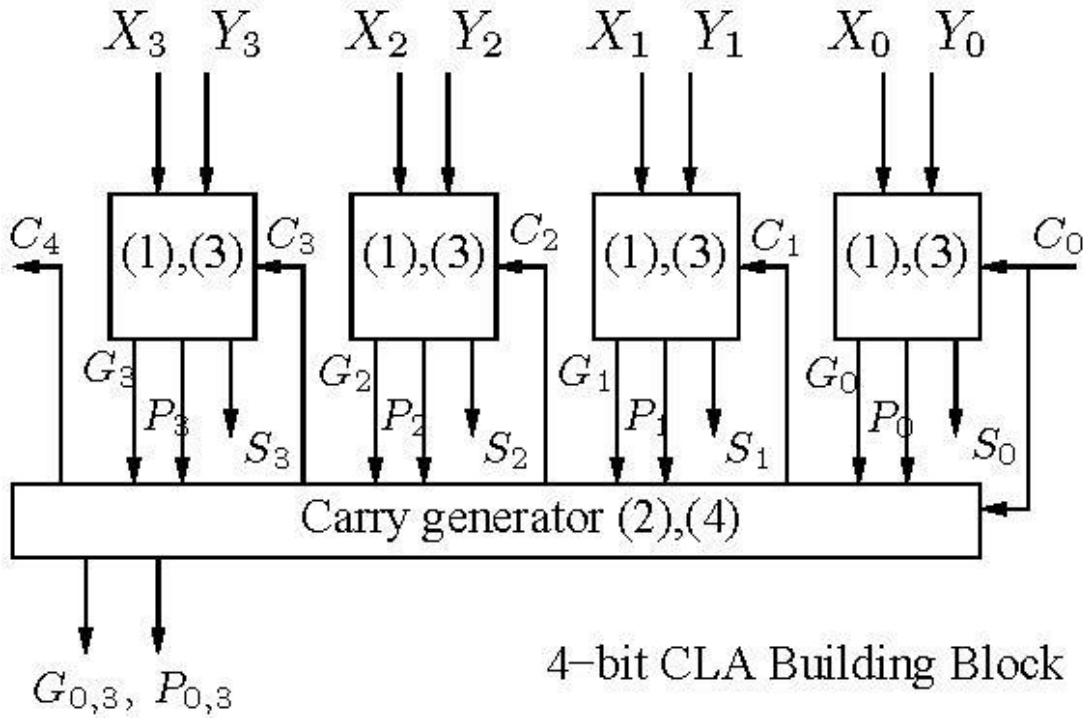
- 4-bit CLA diagram can be shown as



4-bit CLA Building Block

- Let $\begin{cases} G_{0,3} = G_3 + G_2P_3 + G_1P_2P_3 + G_0P_1P_2P_3 \\ P_{0,3} = P_0P_1P_2P_3 \end{cases}$ (4)

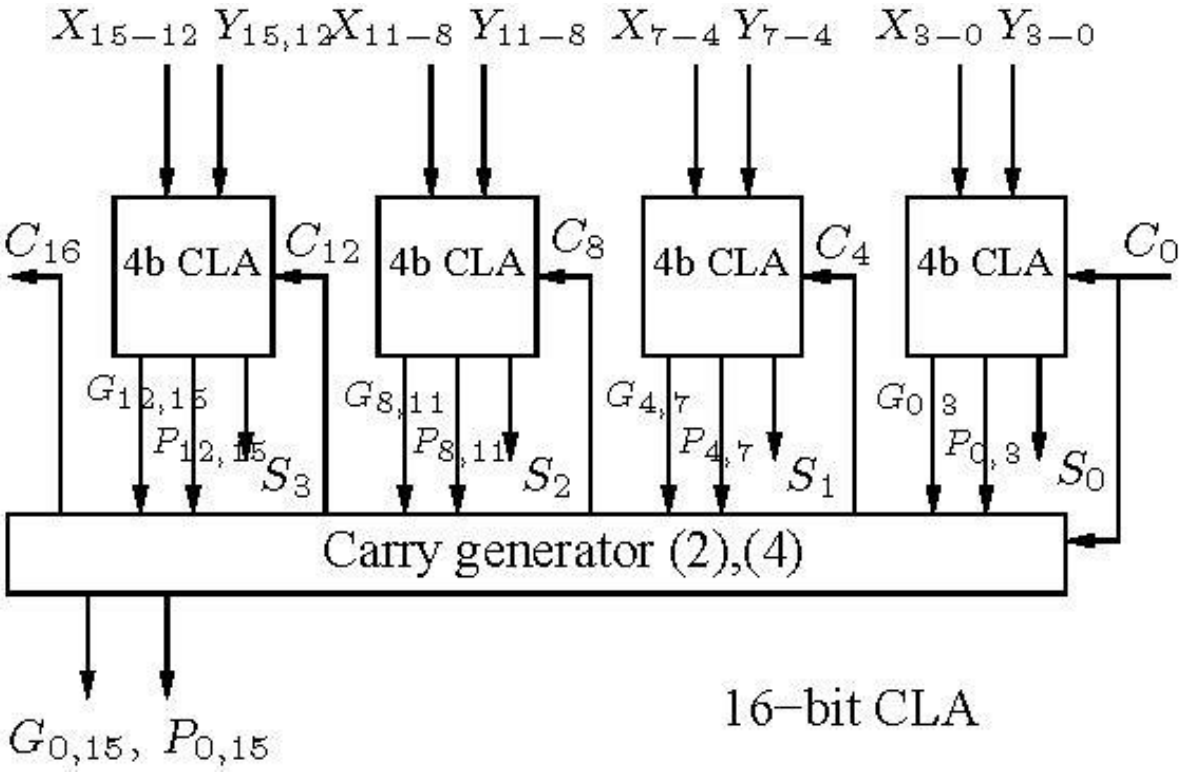
- Then a 4-bit CLA building block can be shown as



4–bit CLA Building Block

16-bit CLA Using 4-bit CLA Blocks

- Circuit diagram for 16-bit CLA built with 4-bit CLA blocks
  - (Two-level carry lookahead structure)



16-bit CLA Using 4-bit CLA Blocks

- The carry generator module is the same as that in 4-bit CLA,
- where equation (2) becomes

$$\begin{cases} c_4 = G_{0,3} + c_0 P_{0,3} \\ c_8 = G_{4,7} + c_4 P_{4,7} = G_{4,7} + G_{0,3} P_{4,7} + c_0 P_{0,3} P_{4,7} \\ c_{12} = G_{8,11} + G_{4,7} P_{8,11} + G_{0,3} P_{4,7} P_{8,11} + c_0 P_{0,3} P_{4,7} P_{8,11} \\ c_{16} = G_{12,15} + G_{8,11} P_{12,15} + G_{4,7} P_{8,11} P_{12,15} + G_{0,3} P_{4,7} P_{8,11} P_{12,15} + c_0 P_{0,3} P_{4,7} P_{8,11} P_{12,15} \end{cases} \quad (5)$$

- And equation (4) becomes

$$\begin{cases} G_{0,15} = G_{12,15} + G_{8,11} P_{12,15} + G_{4,7} P_{8,11} P_{12,15} + G_{0,3} P_{4,7} P_{8.11} P_{12,15} \\ P_{0,15} = P_{0,3} P_{4,7} P_{8.11} P_{12,15} \end{cases} \quad (6)$$

- Note that eqn (5) can be realized using the same logic for eqn (2), Page 10.
- And eqn (6) can be realized using the same logic as for eqn (4), Page 14.

16-bit CLA

- Circuit complexity:
  - Four 4-bit CLA plus a carry generator module.
- Critical Path Delay:
  - $T = 8\Delta_G$, or $T = 9\Delta_G$ as given in the textbook
  - Both the above results are considered as correct.

n-bit CLA

- 64-bit CLA
  - Circuit complexity: four 16-bit CLA plus a carry generator
  - Critical path delay: 12 Δ_G
- Delay for n-bit CLA built in this way:
  - $T = 4 \log_4 n \, \Delta_G$
  - or $T = (4 \log_4 n + 1)\Delta_G$ as given in the textbook