**Assignment – 4**

**1. (20 marks) Build a 18-bit carry-select adder. Decide the number of groups and the size of**

**each group. Estimate the time delay of your design.**

Ans.) 18-bit carry-select adder => n = 18

Let the 18-bit carry select adder be divided into L groups, each group of length k1, k2,...kL,

then, the following inequality holds:

=> 1 + (L (L-1)) / 2 ≥ 18 => L(L - 1) ≥ 34

Since, L is an integer, the minimum value of L that satisfies the above relation is L = 7.

Hence, the number of groups in the carry-select adder are 7.

The group size of each group would then be k1 = 1, k2  = 1, k3  = 2, k4 = 3, k5  = 4, k6 = 5,

k7 = 2

For a group l of length kl it takes for its carry-in cj signal to be available.

And the latency of kl-bit RCA is 2kl ΔG

0

Hence, time delay of this design would be = 1ΔG + (7 - 1)2ΔG = 13 ΔG

A

FA

2ΔG

1ΔG

2ΔG

Figure 1: Critical path for “Carry select” adder

HA

FA

FA

FA

0

FA

FA

1

0

1

FA

FA

2ΔG

FA => Full Adder

HA => Half Adder

1

FA

FA

FA

FA

FA

FA

2ΔG

FA

FA

FA

FA

1

0

FA

FA

0

FA

FA

2ΔG

FA

FA

FA

FA

FA

FA

FA

FA

FA

FA

FA

FA

2ΔG

0

1

1

**2. (20 marks) Build a 18-bit carry-skip adder. Decide the number of groups and the size of a**

**group. Estimate the time delay of your design.**

Ans.) Let the following three time delays be defined:

tr denote carry ripple time through one bit

ts(k) denote the time to skip on group

tb denote the time delay of an OR gate

For a n-bit carry-skip adder, of n/k groups where k is the size of the group,

Tcarry  = (k – 1) tr + tb  + ( n/k - 2 ) ( ts + tb ) + (k – 1) tr

= ( 4k + 2n / k - 7) ΔG

where tr = 2ΔG and tb = ts = ΔG

Optimal size of k => kopt  =

Hence, for n = 18, kopt  = 3 => Number of groups = n /kopt  = 18 / 3 = 6

Figure 2 : Showing the critical path for “Carry Skip Adder”

=> Size of the group = kopt  = 3

=> Optimal time delay of the design, Topt  = ( 4 kopt + 2n / kopt  - 7) Δg

= ( 4\*3 + (2 \* 18) / 3 - 7) Δg  = 17Δg

**3. (20 marks) Build a carry-save adder that performs X = A + B + C + D + E, where each**

**of operands A, B, C, D, and E has 4 bits. Draw a full diagram for the carry-save adder and**

**estimate the complexities using both (3, 2) and (2, 2) counters as building blocks. Explicitly**

**show a critical path.**

Ans.) Since, A, B, C, D and E are 4 bit operands => A, B, C, D, E ∈ [0, 24 - 1] = [0-15]

Hence, the sum of four such numbers will have no more than ( 5 x [0-15]) ⊂ [0, 27 – 1] i.e. 7 bits

=> Organize the architecture diagram in at most 7 columns.

**26 25 24 23 22 21 20**

A0 B0 C0

A1 B1 C1

A2 B2 C2

A3 B3 C3

( 3, 2)

( 3, 2)

( 3, 2)

( 3, 2)

( 3, 2)

( 3, 2)

FA

FA

FA

FA

“0”

FA

“0”

“0”

s0

D0

( 3, 2)

( 3, 2)

( 3, 2)

( 3, 2)

D2

( 3, 2)

( 3, 2)

( 3, 2)

E3

E2

D3

E1

E0

“0”

“0”

D1

s1

s2

s3

s4

s5

s6

Figure 3: “Carry Save Adder” using (3,2) as building blocks

The architecture complexities using only (3,2) or FA as building blocks are:

\* Circuit complexity: C = 18(3,2)'s = 18 FA

\* Critical path delay: T = 8 \* (2ΔG) = 16 ΔG

A1 B1 C1

A3 B3 C3

A0 B0 C0

A2 B2 C2

( 3, 2)

( 3, 2)

( 3, 2)

( 3, 2)

D2

D1

D3

D0

( 3, 2)

( 3, 2)

( 2, 2)

( 3, 2)

E3

E2

E1

E0

( 2, 2)

( 3, 2)

( 3, 2)

( 3, 2)

( 2, 2)

Figure 4: “Carry Save Adder” using (2,2) as building blocks

s6

s5

s4

s3

s2

s1

s0

HA

HA

FA

FA

FA

The architecture complexities using both (3,2) or FA and (2,2) or HA as building blocks are:

\* Circuit complexity: C = 13(3,2)'s + 5(2,2)'s = 13 FAs + 5HAs

\* Critical path delay: T = 6 (2ΔG) + 2(1ΔG ) = 14 ΔG

**4. (20 marks) Consider multiplication of a 5-bit multiplicand A and a 4-bit multiplier X. Design a high-speed multiplier realizing this multiplication operation. Assume that (3, 2) and (2, 2) counters are used for carry save addition and carry-propagate addition. Show the steps in dot diagram or draw a block diagram for your design. How many (3, 2) and (2, 2) counters are required? Assume that ∆ (3,2) = 2∆ G and ∆ (2,2) = ∆ G . What is time delay of your multiplier?**

Ans.) Let A = (a4a3a2a1a0) and X = (x3x2x1x0) then the product bits P = (p8p7p6p5p4p3p2p1p0) can be

obtained as follows:

a4 a3 a2 a1 a**0**

x3 x2 x1 x0

---------------------------------------------------------------------

a4x0 a3x0 a2x0 a1x0 a0x0

a4x1 a3x1 a2x1 a1x1 a0x1

a4x2 a3x2 a2x2 a1x2 a0x2

a4x3 a3x3 a2x3 a1x3 a0x3

----------------------------------------------------------------------------------------------------------------------------

p8 p7 p6 p5 p4 p3 p2 p1 p0

\* The 20 partial product bits can be generated using 20 two-input AND gates and hence

requires one gate delay

\* \* \* \* \*

\* \* \* \* \*

\* \* \* \* \*

\* \* \* \* \*

Figure 5: Dot diagram depicting the

usage of (3,2)'s and (2,2)'s for

adding the partial product terms

||

\* \*

\* \* \* \*

\* \* \* \* \* \*

\* \* \* \* \* \* \* \*

|| Applying 4 (3,2)'s (1-level CSA)

\* \* \*

\* \* \* \* \*

\* \* \* \* \* \* \* \*

|| Applying 3 (3,2)'s and 1 (2,2) (1-level CSA)

\* \* \* \* \*

\* \* \* \* \* \* \* \*

|| (CPA: 4 (3,2)'s and 3 (2,2)'s)

\* \* \* \* \* \* \* \* \*

\* Let the partial product bit be denoted with a \*. Then, the CSA tree of 20 partial product bits forms an isoceles trapezoid with 4 rows and base consisting of 8 asterisk's. Since, the height of the trapezoid is 4, it requires 2 levels of CSA before the final CPA.

\* Number of (3,2) counter's required = 11

\* Number of (2,2) counter's required = 4

a0x2

a1x2

a2x2

a1x1

a2x3

a2x0

a3x0

a2x1

a3x1

a3x2

a4x0

a4x1

( 3, 2)

( 3, 2)

( 3, 2)

( 3, 2)

( 2, 2)

( 2, 2)

( 2, 2)

( 3, 2)

( 3, 2)

( 3, 2)

a4x2

a3x3

( 3, 2)

a4x3

( 2, 2)

a1x0

a0x1

p1

p0

a0x0

Figure 6 : Block diagram depicting the usage of (3,2)'s and (2,2)'s for adding the partial product terms

( 3, 2)

a1x3

a0x3

( 3, 2)

p2

p3

p4

p5

p6

p7

p8

( 3, 2)

\* Time delay of the multiplier = Time to form the partial + Time for CSA to give actual product

product terms (1 gate bits ( Critical path highlighted in red

delay for the 2 input in Figure 6)

AND gates)

= 1 ΔG + (2 + 2 + 1 + 2 + 2 + 2 + 2) ΔG

= 14ΔG

5. (20 marks) Consider multiplication of a 5-bit multiplicand A and a 4-bit multiplier X. Design

an array multiplier realizing this multiplication operation. Assume that FA and HA are used as

building cells. Draw a block diagram for your design. How many FAs and HAs are required?

Assume that ∆ FA = 2∆ G and ∆ HA = ∆ G . What is time delay of your design?

Ans.)

Let A = (a4a3a2a1a0) and X = (x3x2x1x0) then the product bits P = (p8p7p6p5p4p3p2p1p0) can be

obtained as follows:

a4 a3 a2 a1 a**0**

\* x3 x2 x1 x0

---------------------------------------------------------------------

a4x0 a3x0 a2x0 a1x0 a0x0

a4x1 a3x1 a2x1 a1x1 a0x1

a4x2 a3x2 a2x2 a1x2 a0x2

+a4x3 a3x3 a2x3 a1x3 a0x3

----------------------------------------------------------------------------------------------------------------------------

p8 p7 p6 p5 p4 p3 p2 p1 p0

Assuming that the partial product bits ai xj , i = 0,...,4 and j = 0,...,3, have been generated, an array multiplier realizing the multiplication operation can be designed using FA's and HA's as follows:

a1x0

a2x0

a3x0

a4x0

a0x0

HA => Half Adder

a0x2

a1x1

a0x1

a2x1

a3x2

a4x3

a3x3

a4x2

a2x3

a4x1

a1x3

a2x2

a3x1

a1x2

FA

FA

FA

FA

HA

HA

FA

FA

FA

FA

FA

FA

HA

HA

FA

HA

FA => Full Adder

a0x3

p0

p1

p2

p3

p4

p5

p6

p7

p8

Figure 7 : Block diagram for multiplication of 5-bit multiplicand A and a 4-bit multiplier X

\* Number of Full Adder's required = 11

\* Number of Half Adder's required = 5

\* Time delay for the design = Time to form the partial + Time to get actual product

product terms (1 gate bits ( Critical path highlighted in red

delay for the 2 input in Figure 7)

AND gates)

= 1 ΔG  + (1 + 2 + 2 + 1 + 2 + 2 + 2)ΔG

= 13ΔG

**6. (no marks) Let a residue number system (RNS) be given by (m2 , m1 , m0 ) = (15, 14, 13).**

**(a) Solve dynamic range for the RNS.**

**(b) Find the RNS representations for A = 1910 and B = 2210 . Perform C = A × B in the**

**RNS.**

**(c) How many bits are required to represent a number with respect to this RNS?**

Ans.)

a) Dynamic range for the RNS(15,14,13), M = 15 \* 14 \* 13 = 15 \* 182 = 2730

=> Range = [0, 2729]

b) RNS representation for A = 1910 is (19 % 15, 19 % 14, 19 % 13) = (4, 5, 6)

RNS representation for B = 2210 is (22 % 15, 22 % 14, 22 % 13) = (7, 8, 9)

C = A x B => C = (4\*7, 5\*8, 6\*9)

= (28, 40, 54)

= (13, 12, 2) RNS (15,14,13)

c) Bits required to represent a number w.r.t this RNS = 4 + 4 + 4 = 12