ELEC 8590
Physical Design Automation for VLSI and FPGAs

Lecture 1:
Introduction to EDA, VLSI and FPGAs

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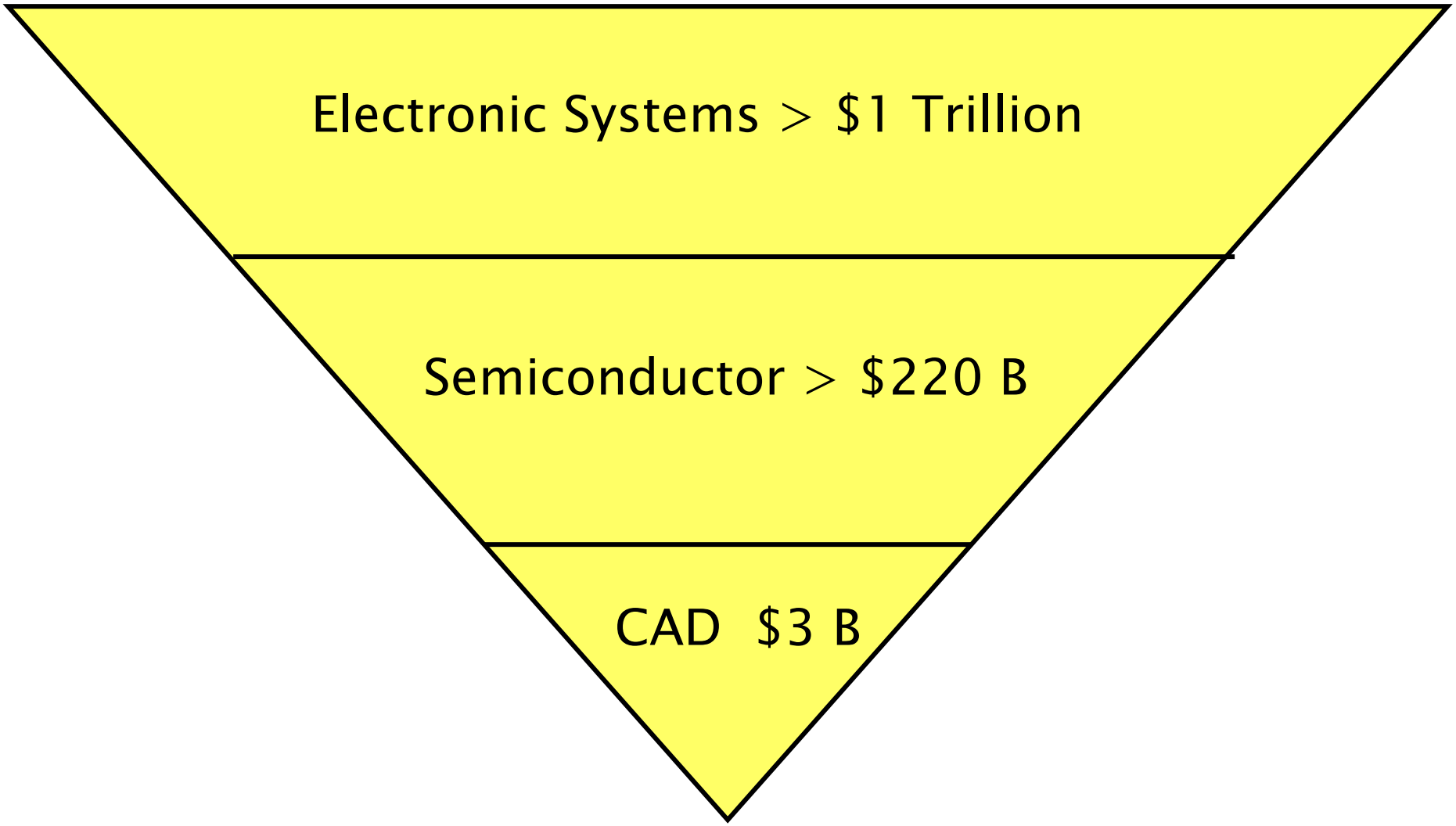
References and Copyright

- Slide sources:
  - Kia Bazargan, University of Minnesota
  - Kurt Keutzer, UC Berkeley
  - Mike Butts, Former Cadence Fellow, well known researcher currently a co-founder of a start-up company.
  - Naveed Sherwani (Companion slides with textbook)

The Inverted Pyramid

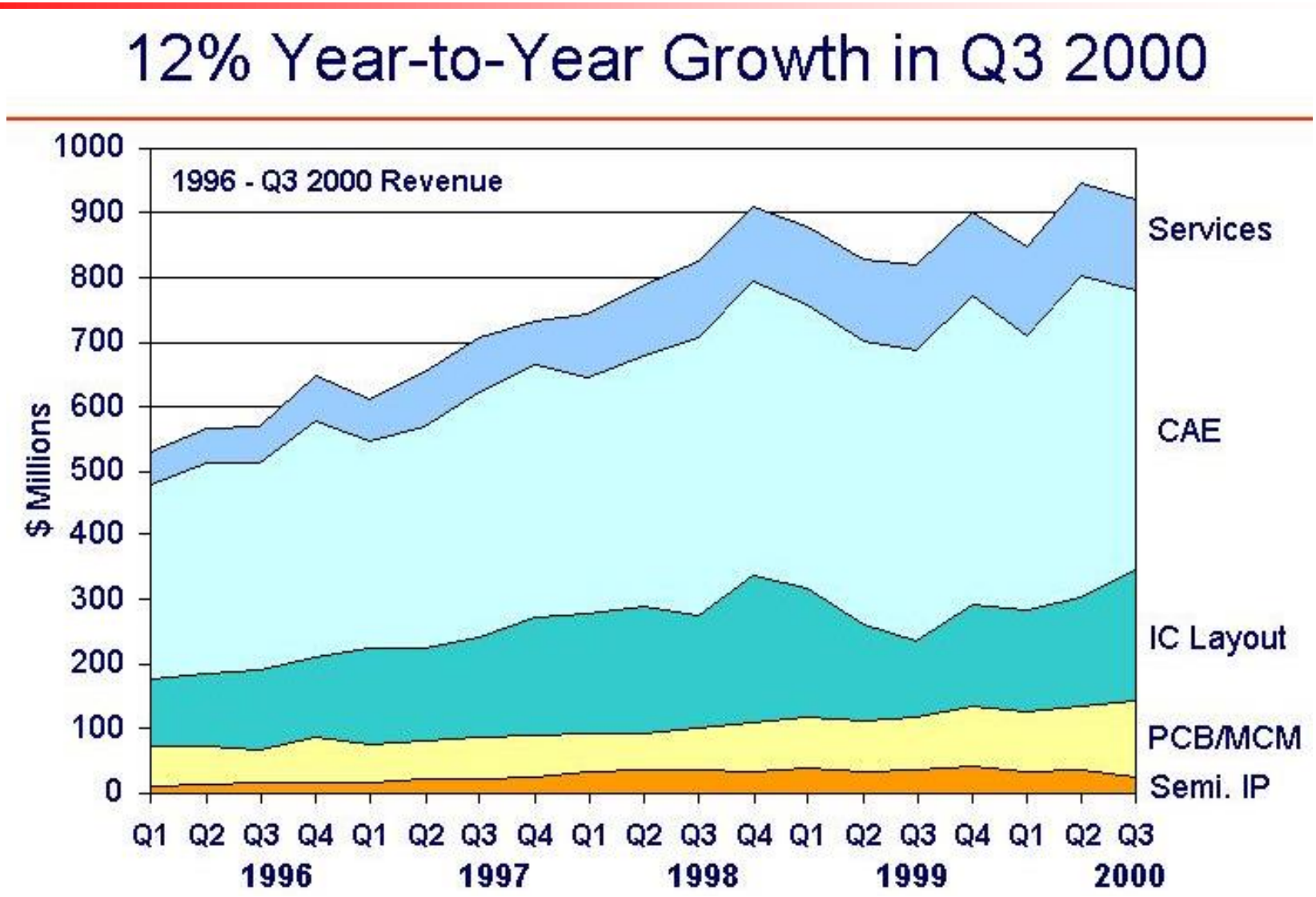


IC Products

- Processors
  - CPU, DSP, Controllers
- Memory chips
  - RAM, ROM, EEPROM
- Analog
  - Mobile communication, audio/video processing
- Programmable
  - PLA, FPGA
- Embedded systems
  - Used in cars, factories
  - Network cards
- System-on-chip (SoC)

Images: amazon.com

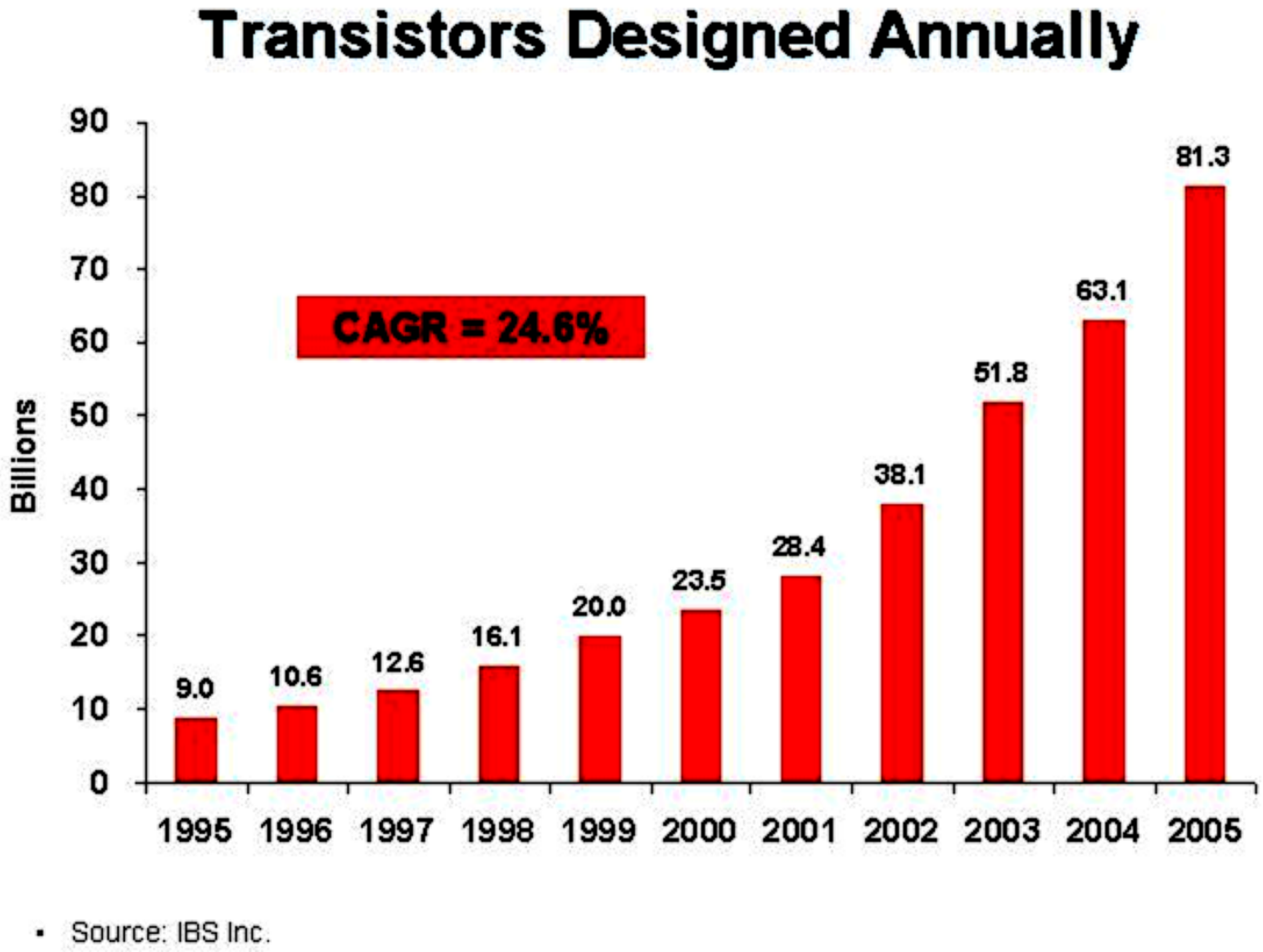
More Demand for EDA



Source: http://www.edat.com/edac

CAE = Computer Aided Engineering

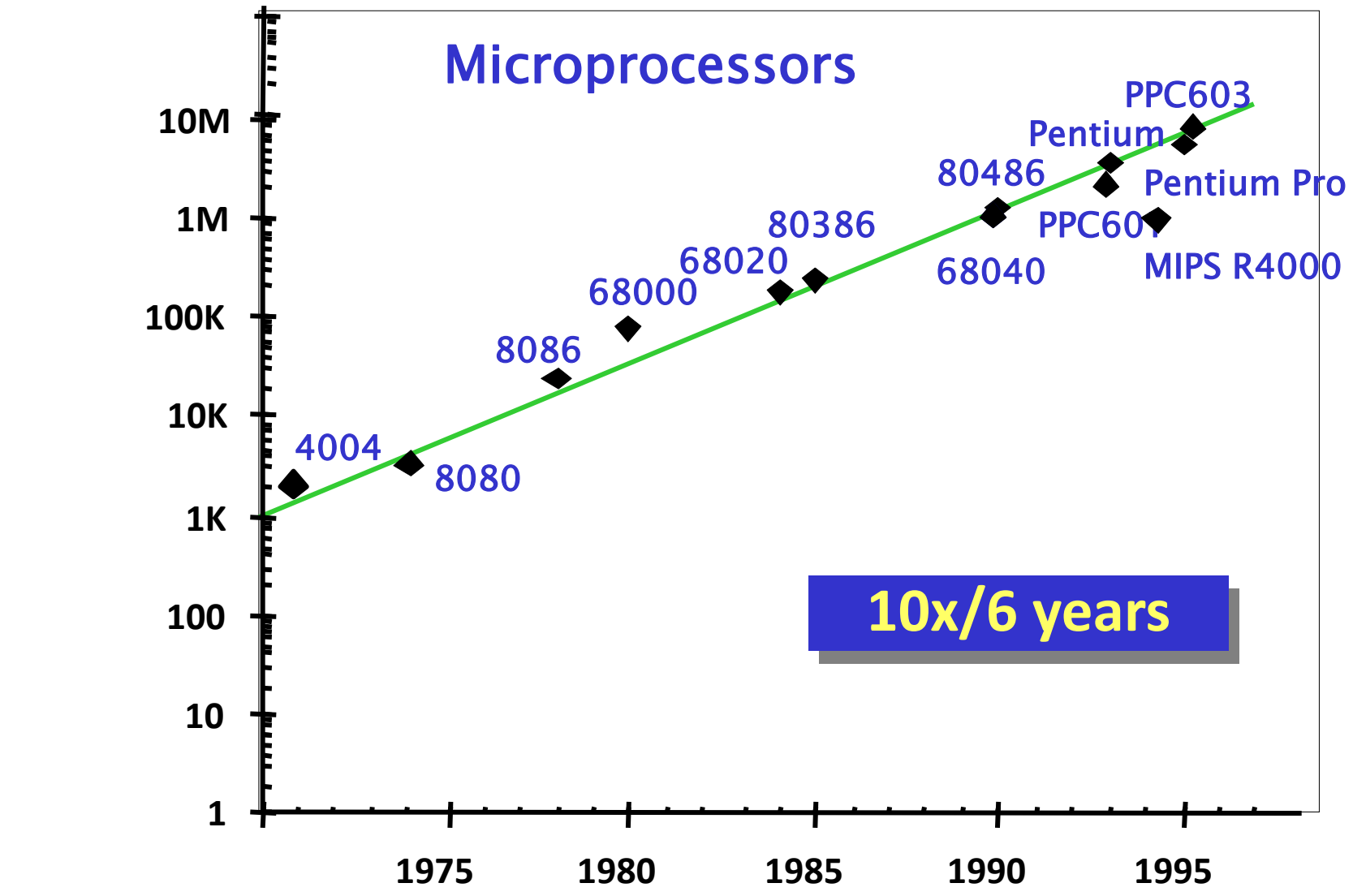
Growth in System Size



CAGR = Compound Annual Growth Rate

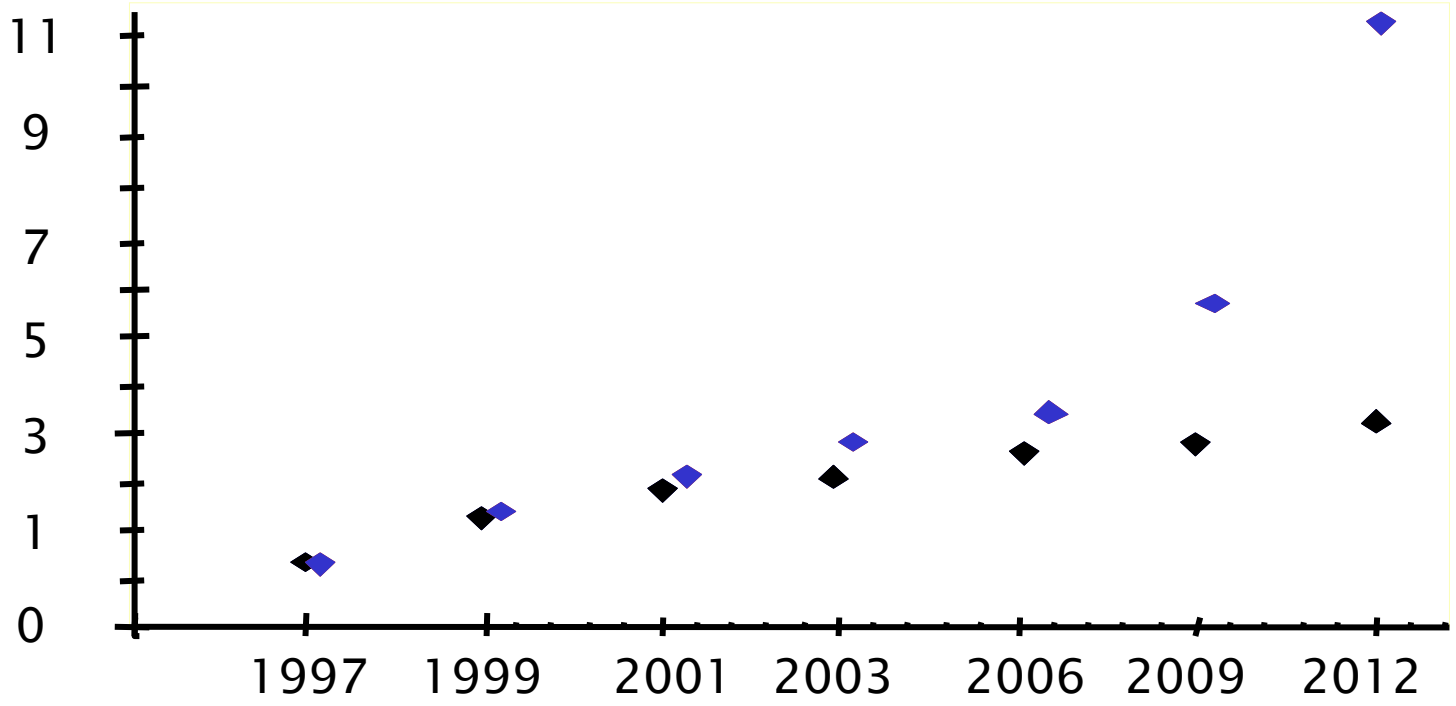
Source: http://www.edat.com/edac

Moore's Law


Transistors
Microprocessors
10M
1M
100K
10K
1K
100
10
1
1975
1980
1985
1990
1995
4004
8080
8086
68000
68020
80386
80486
68040
Pentium
PPC603
Pentium Pro
PPC601
MIPS R4000
10x/6 years

NRTS: Chip Frequencies

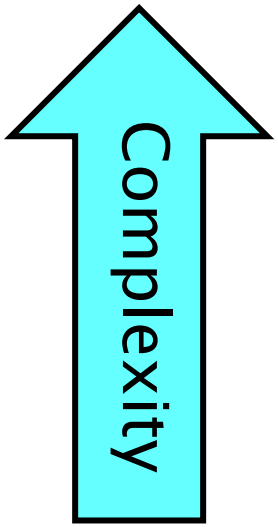
Clock speed GHz



- On-chip, local clock, high performance
- On-chip, global clock, high performance

Increasing Device and Context Complexity

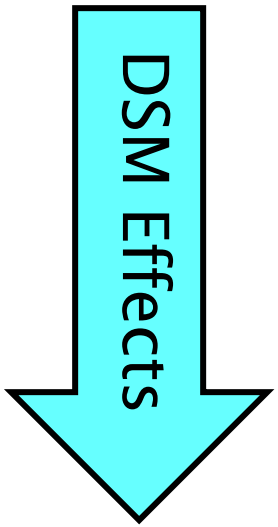
- Exponential increase in device complexity
  - Increasing with Moore's law (or faster)!
- More complex system contexts
  - System contexts in which devices are deployed (e.g. cellular radio) are increasing in complexity
- Require exponential increases in design productivity



We have exponentially more transistors!

Deep Submicron Effects

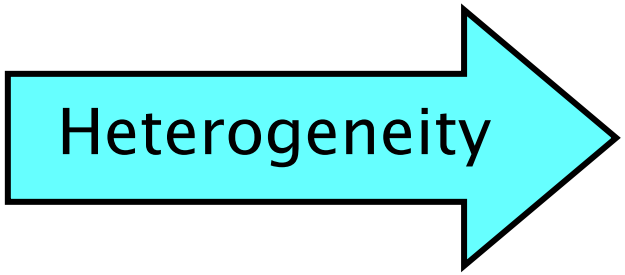
- Smaller geometries are causing a wide variety of effects that we have largely ignored in the past:
  - Crosscoupled capacitances
  - Signal integrity
  - Resistance
  - Inductance



Design of each transistor is getting more difficult!

Heterogeneity on Chip

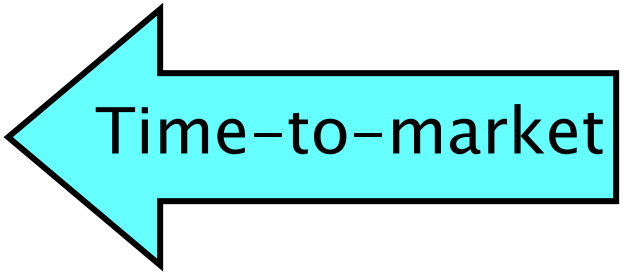
- Greater diversity of onchip elements
  - Processors
  - Software
  - Memory
  - Analog



More transistors doing different things!

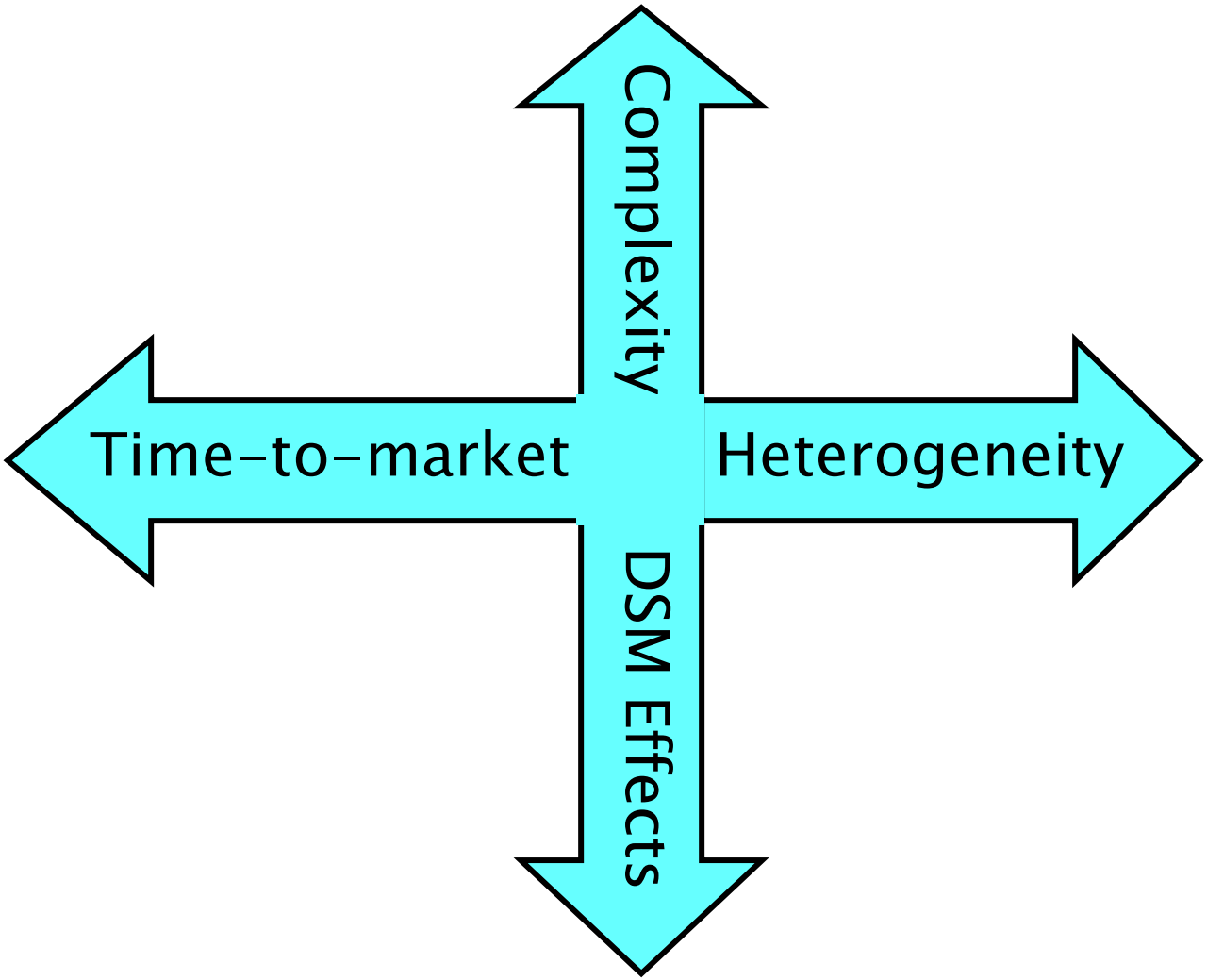
Stronger Market Pressures

- Decreasing design window
- Less tolerance for design revisions

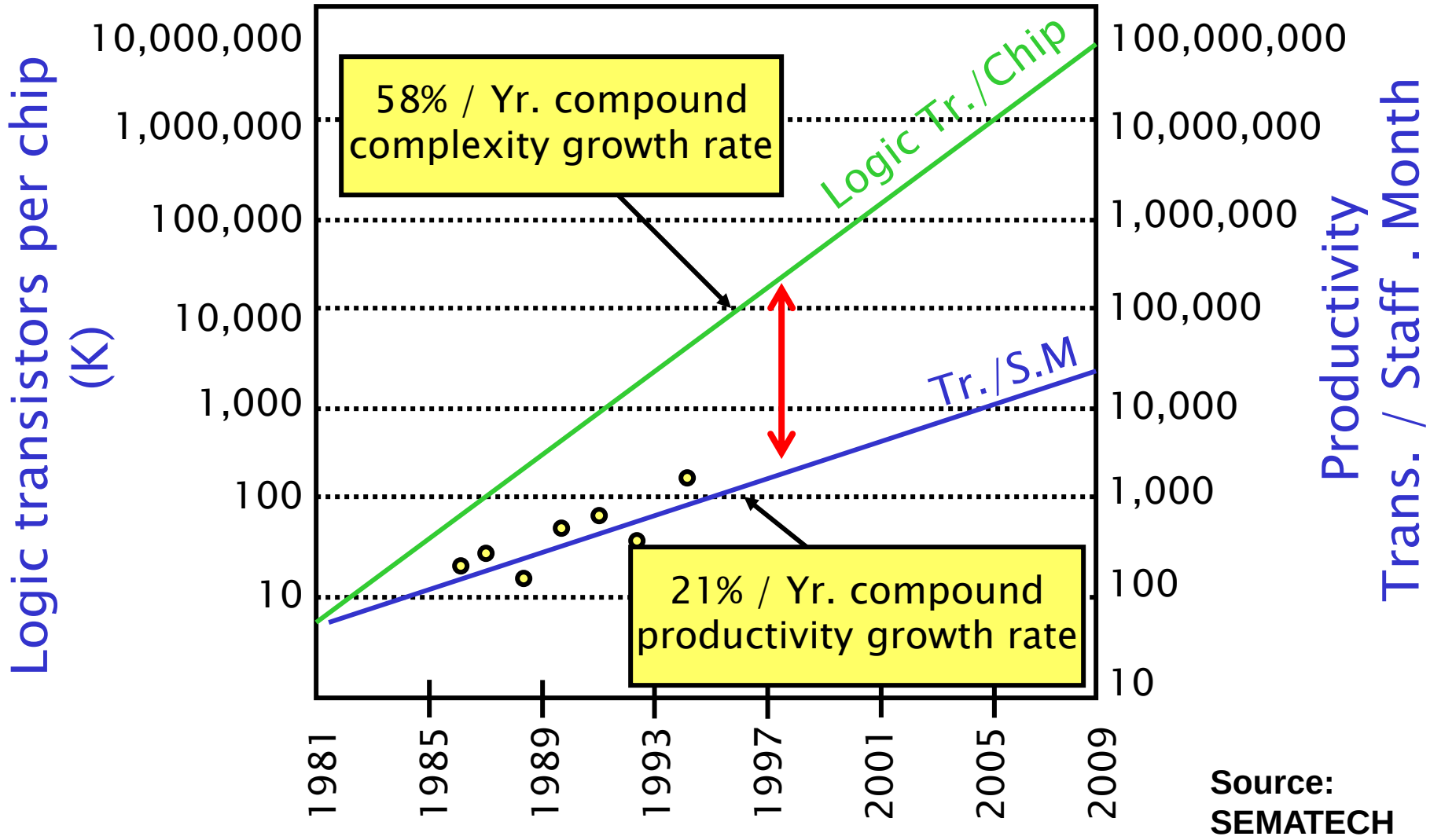


Exponentially more complex, greater design risk, greater variety, and a smaller design window!

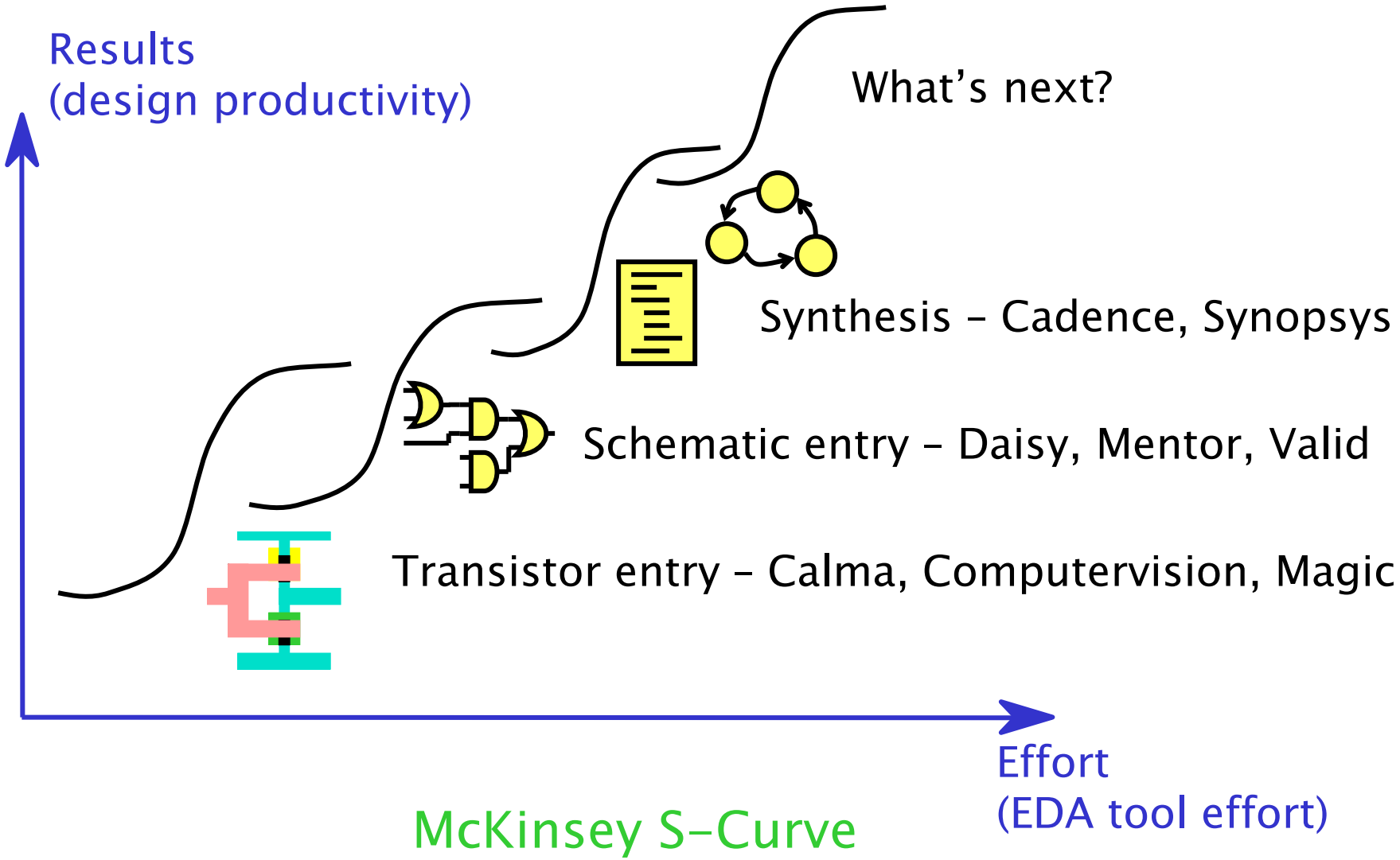
A QuadrupleWhammy



Design Productivity Gap



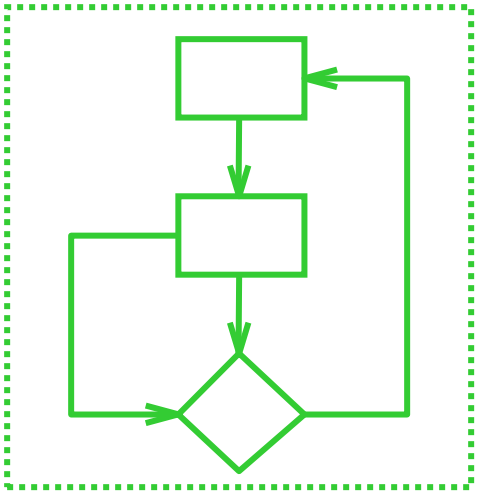
Evolution of the EDA Industry



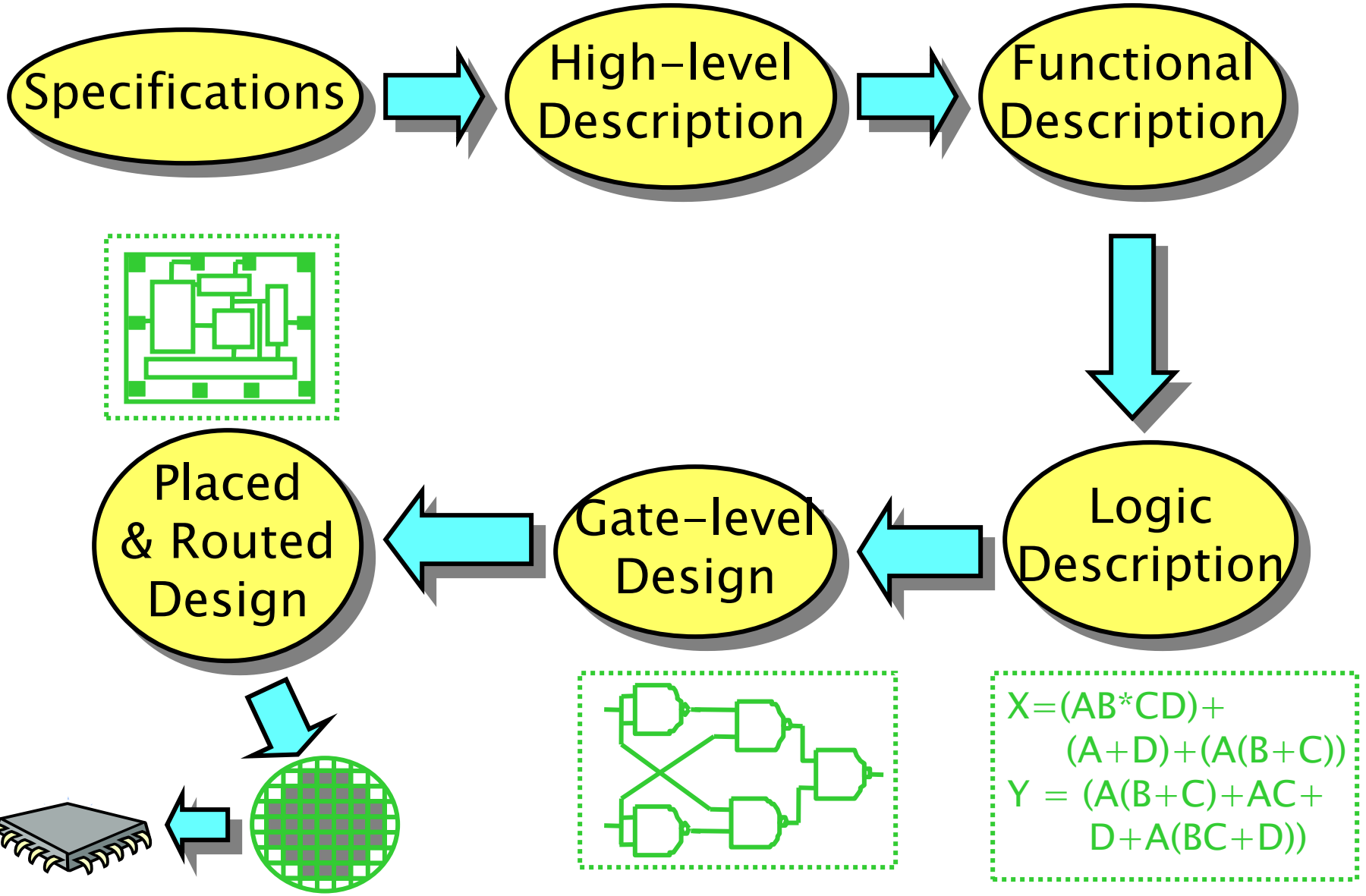
IC Design Steps (cont.)

Behavioral
VHDL, C

Structural
VHDL

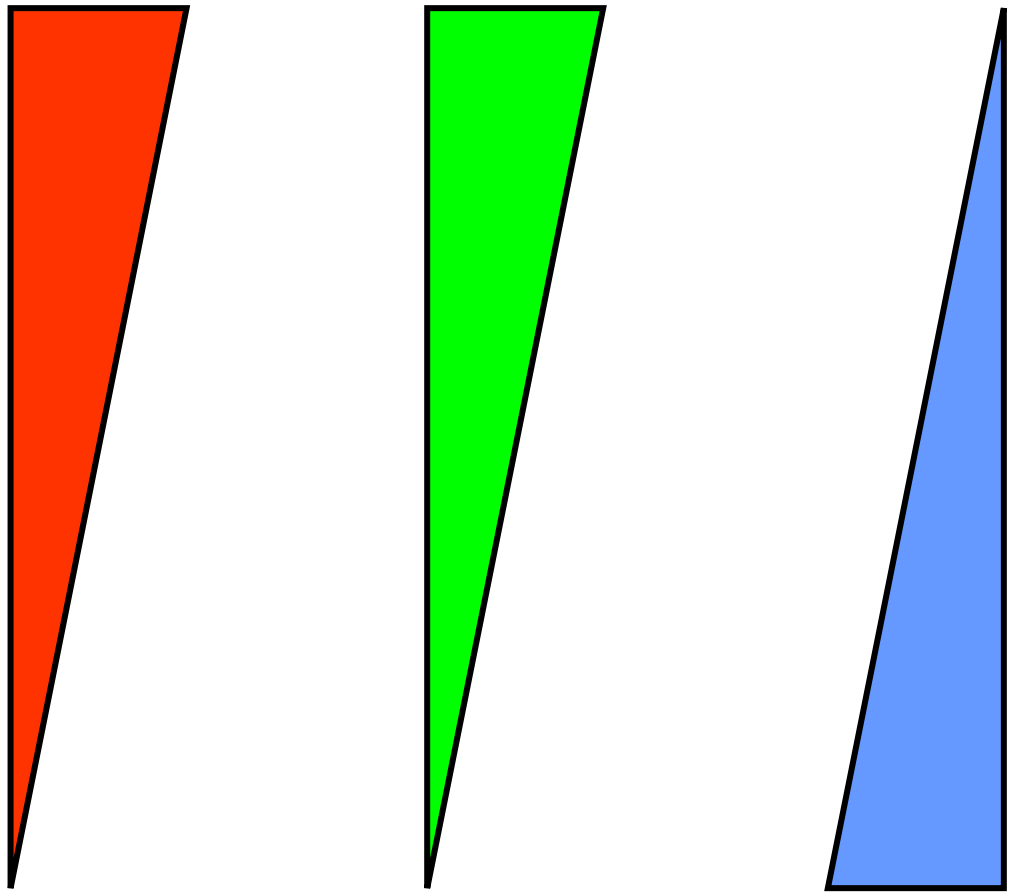


IC Design Steps (cont.)

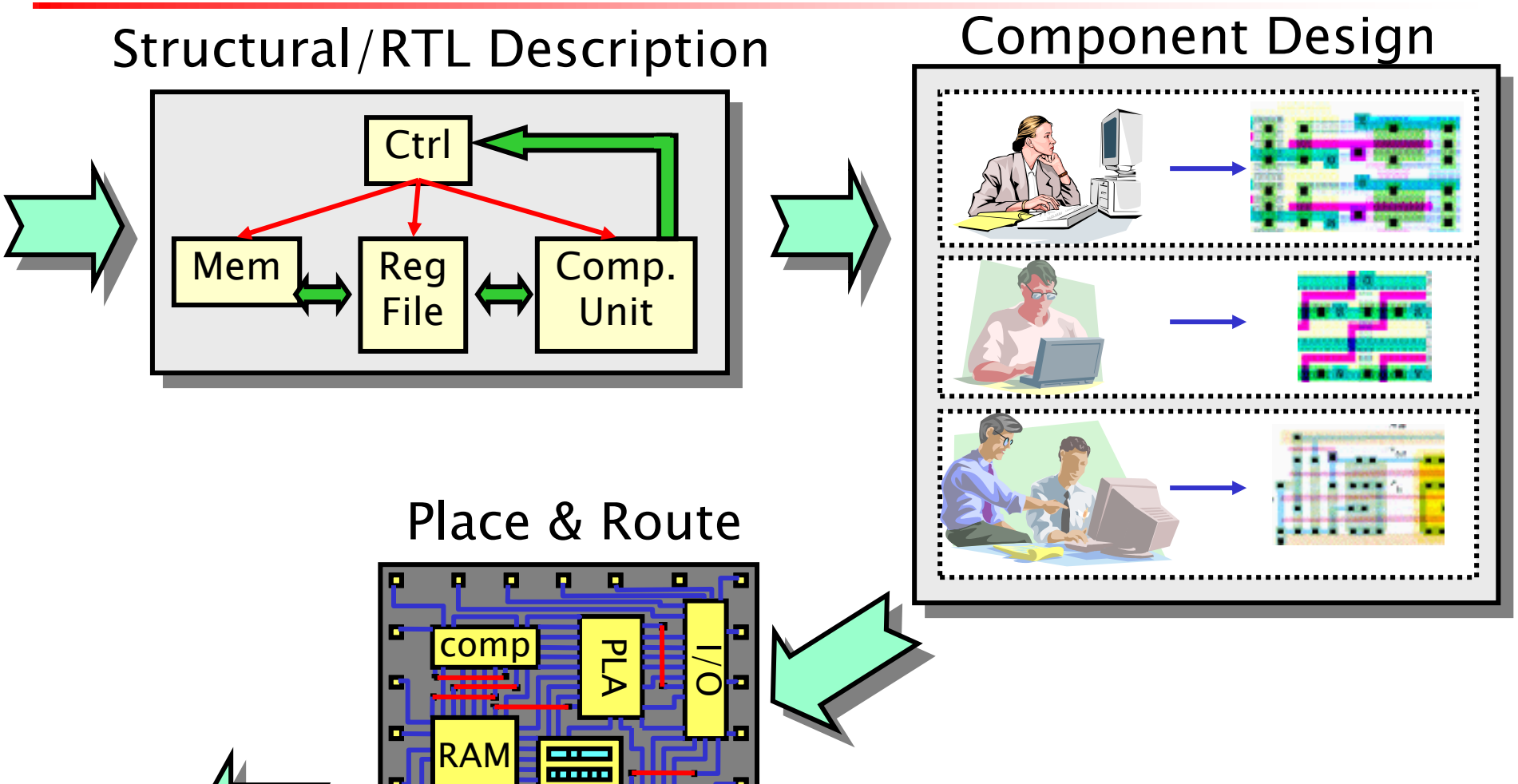


The Big Picture: IC Design Methods

Design Methods	Cost / Development Time	Quality	# Companies involved
Full Custom			
Standard Cell Library Design			
ASIC – Standard Cell Design			
RTL-Level Design			

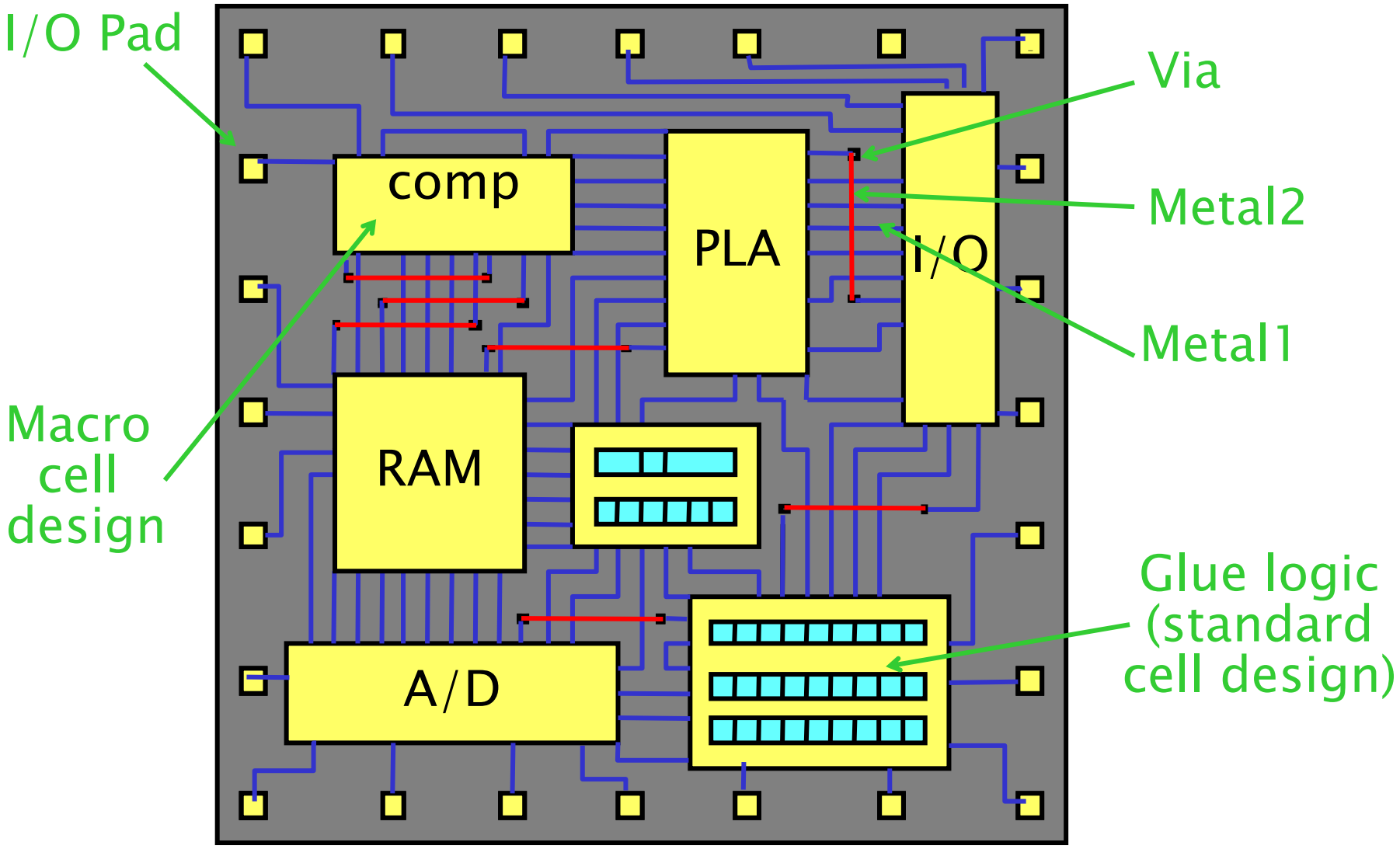


Full Custom Design



Floorplan [©Sherwani]
Layouts [© Prentice Hall]

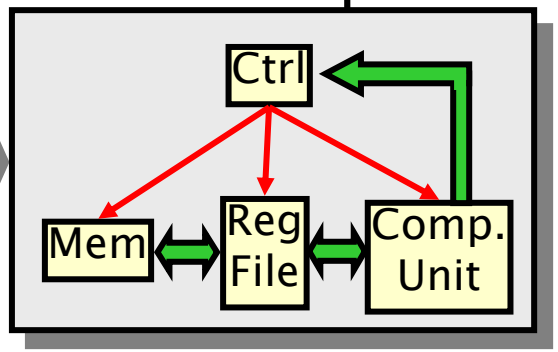
Full Custom Design Example (30+ Mgates per chip today , 200K in 1994, 150X!)



[©Sherwani]

ASIC Design

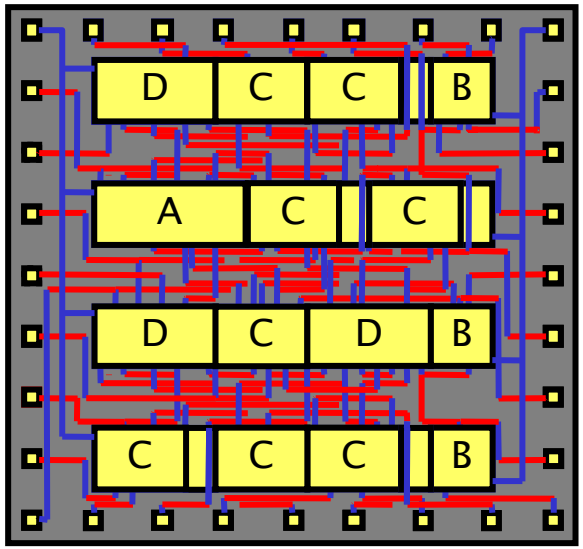
Structural / RTL Description



HDL Programming

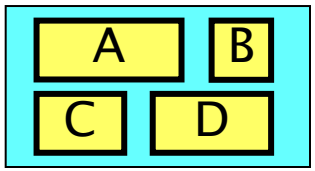
```
P_Inp: process (Reset, Clock)
  begin
    if (Reset = '1') then
      sum <= ( others => '0' );
      input_nums_read <= '0';
      sum_ready <= '0';
```

```
add82 : kadd8 port map (
    a => add_i1, b => add_i2,
    ci => carry, s => sum_o);
Mult_i1 <= sum_o(7 downto 0);
```



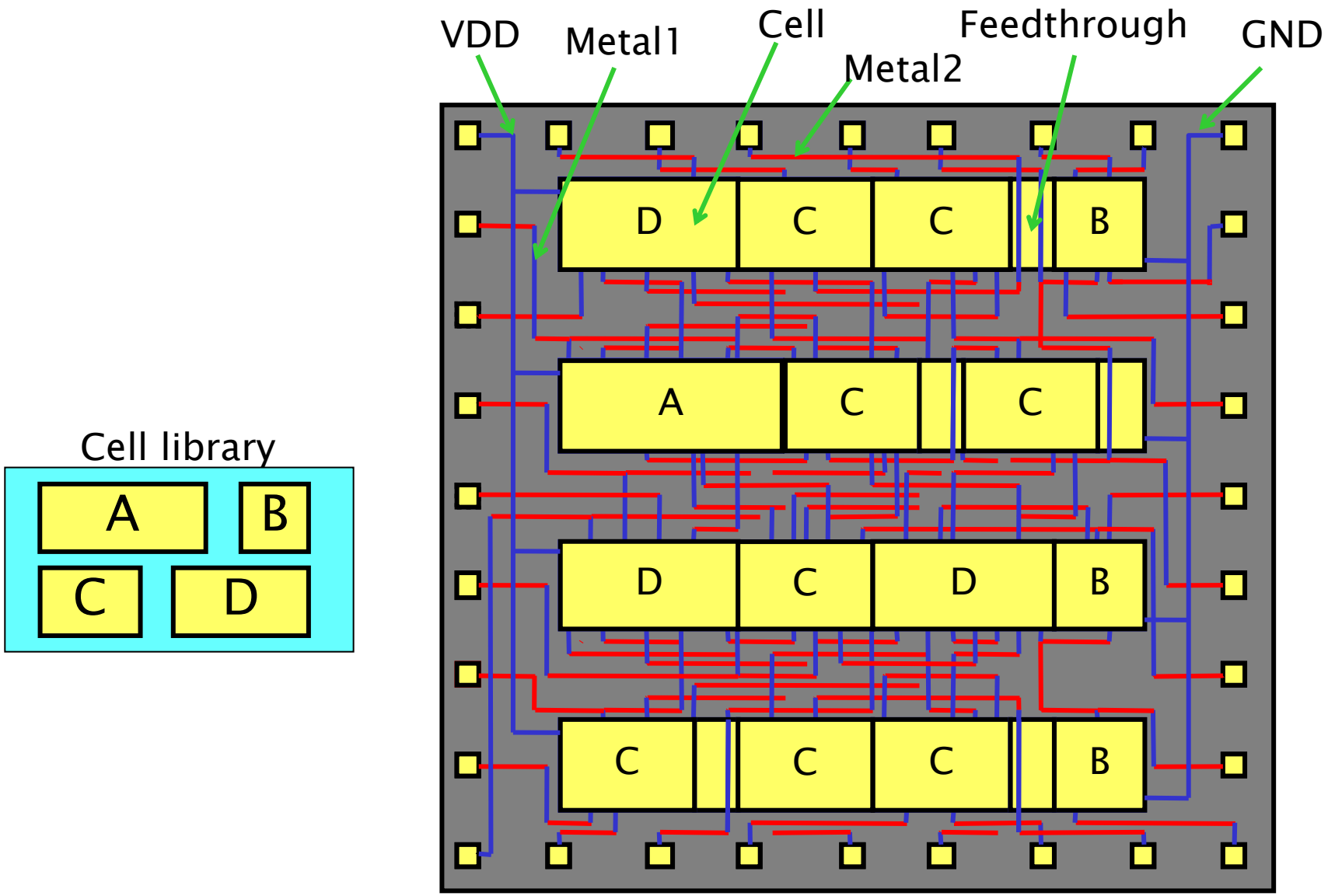
...

Cell library



Floorplan [©Sherwani]

ASIC (Standard Cell) Design Example

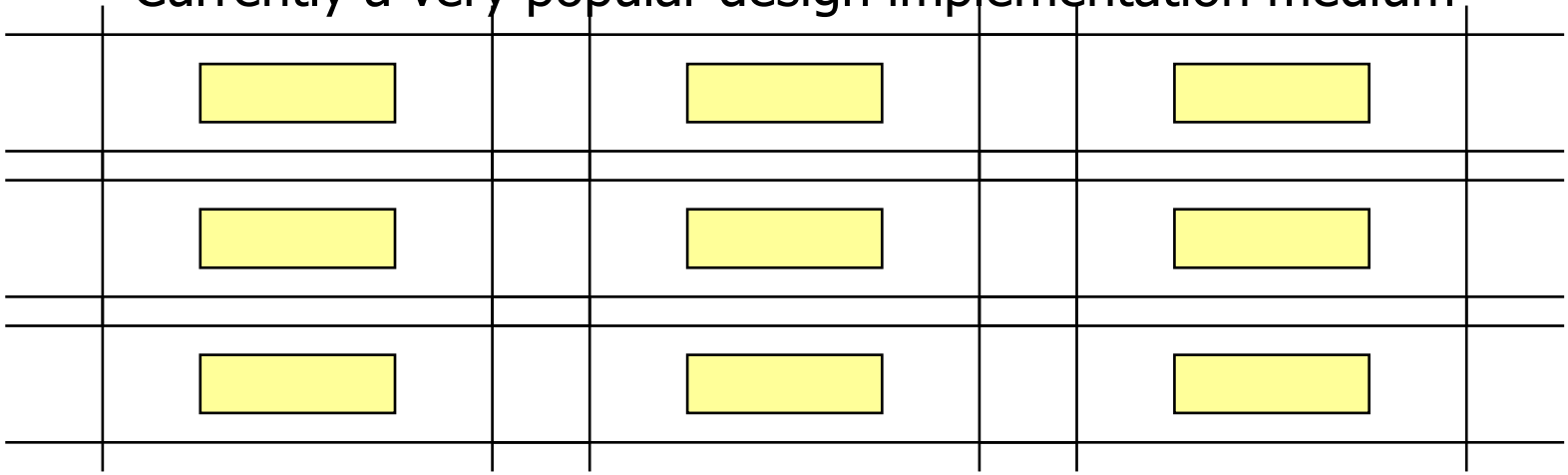


References and Web links

- IEEE Trans. on CAD of ICs and Systems, Special Issue on EDA, vol. 19, no. 12, December 2000 - particularly the following:
  - D. MacMillen et al, An Industrial View of EDA
  - M. A. Breuer et al, Fundamental CAD Algorithms
- S. Hauck, *The Roles of FPGAs in Reprogrammable Systems*, Proc. Of IEEE, vol. 86, no. 4, pp. 615-638, April 1998.
- www.cadence.com, www.synopsys.com
  - Leading EDA tool vendors
- Leading FPGA vendors
  - Altera, acquired by Altera
  - Xilinx, acquired by AMD

Field Programmable Gate Arrays (FPGAs)

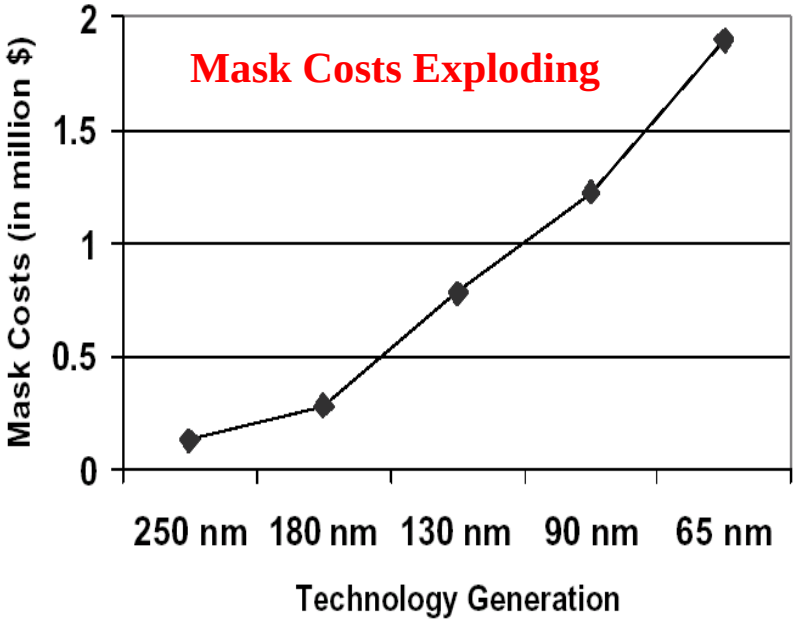
- A digital IC chip with programmable logic and programmable routing
  - Can implement almost any digital design within its logic capacity
- Very flexible compared to custom ICs or ASICs but much larger and slower (programmability overhead)
  - Currently a very popular design implementation medium



Nanometer Silicon implications: Why FPGAs?

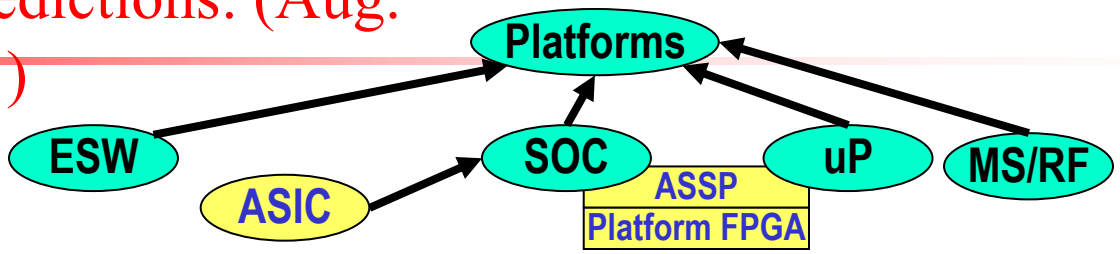
- Chips getting Bigger, Harder, More Expensive to Build
  - Fewer, bigger more expensive fabs, masks, NREs
- Applications are changing and proliferating ever faster
  - Protocols, customer-specific and user-specific features

- Each tapeout must cover more sockets (volume)
- But sockets are getting more individual (custom)
- Implies: Chips must get more programmable



Ref: Zuchowski, et al, Hybrid ASIC and FPGA Architecture, ICCAD 2002

GSRC* "Nano" Predictions: (Aug. 2001)

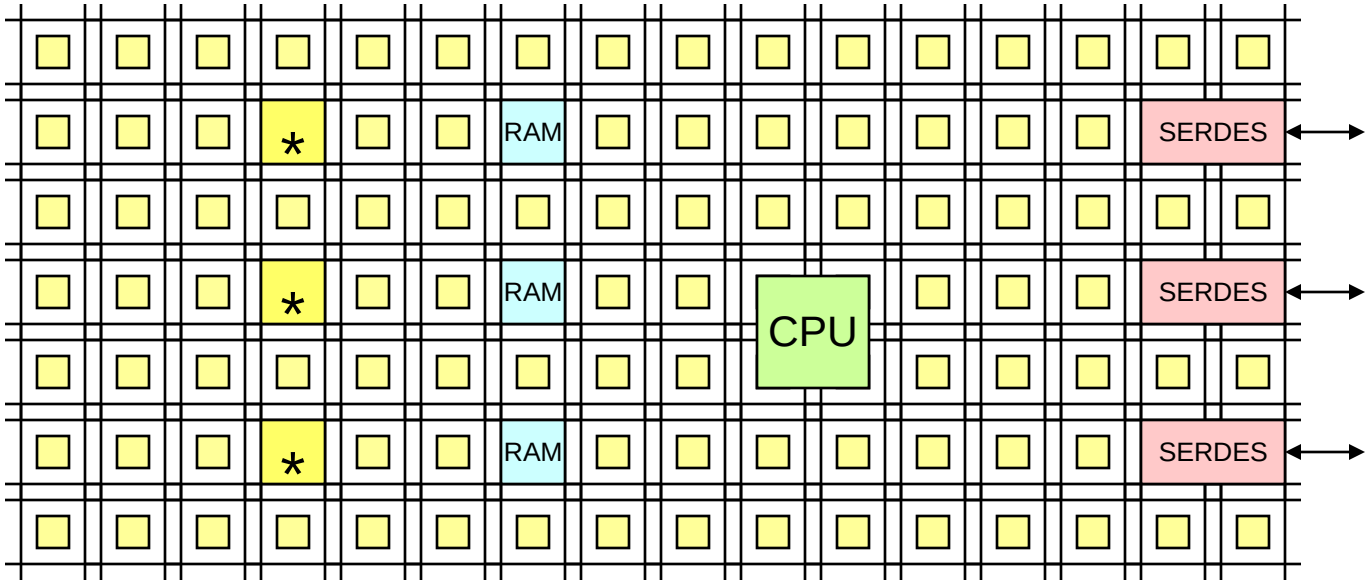


- **The Nature of IC's**
  - Traditional ASIC design starts will diminish from 2001 forward and will be replaced by platform-based designs.
  - By 2005 the majority (60%) of IC designs will have one or more software (e.g. embedded microprocessor) and/or electrically programmable (e.g. FPGA) components on the chip.
- **Programmable Systems (Platform FPGAs)**
  - From 2001 onward, a growing percentage of high-performance electronic systems will be fielded without any ASIC components whatsoever, but built entirely from programmable application-specific standard parts.
  - This will account for 30% of all electronic systems by 2008.

* GSRC = Gigascale Silicon Research Center (www.gigascale.org)

Current Capabilities: Platform FPGA

- An off-the-shelf chip and CAD toolset which combines:
  - A substantial amount of FPGA programmable logic
  - One or more CPUs in hard or soft cores
  - Additional hard cores such as RAMs, multipliers, comm ports, etc.



Platform FPGAs are Here

- Xilinx Virtex-II Pro shipping today:
  - 1M real ASIC gates, 2.5 Mbits SRAM, 144 multipliers
  - Up to four 300 MHz IBM PowerPC CPUs, IBM 0.12 μ process
  - Wind River RTOS, IDE
  - Up to twenty 2.5 Gb/s SERDES cores
  - 200+ soft IP cores: DRAM ctlrs, etc.
  - In 2003: 1 GHz CPUs, 10 Gb/s SERDES
- Likewise from Altera (100 MHz ARM)

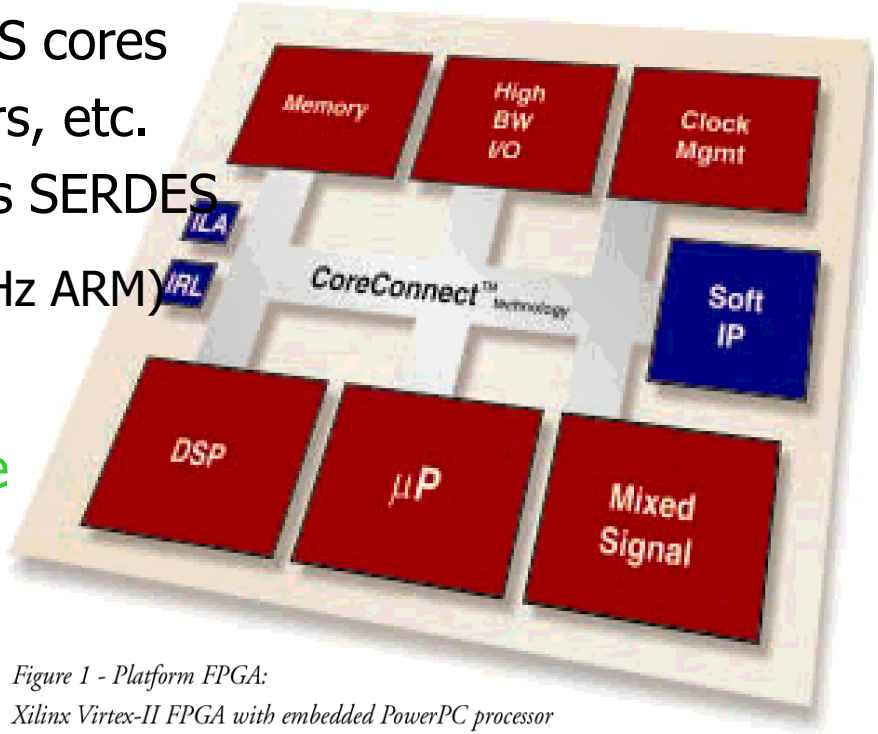


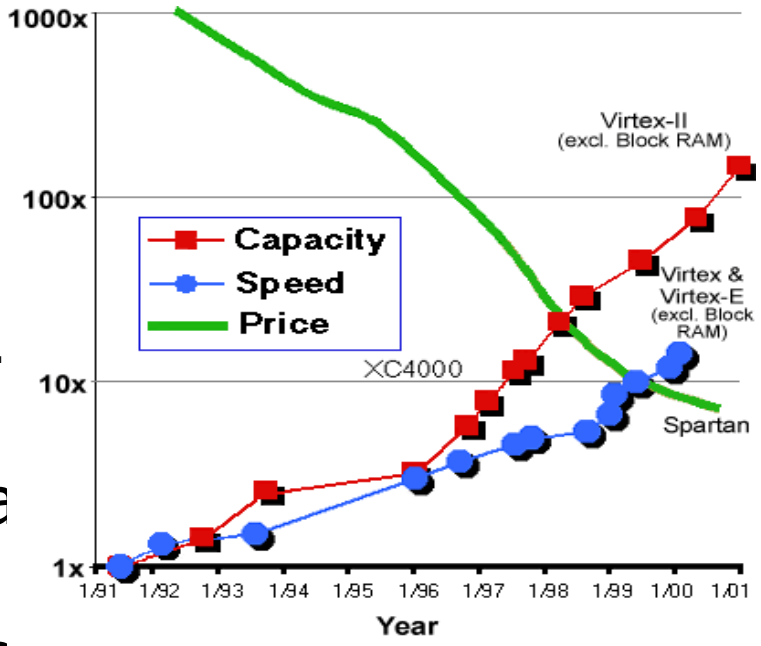
Figure 1 - Platform FPGA:
Xilinx Virtex-II FPGA with embedded PowerPC processor

✳ This is a complete SoC, available off the shelf

- No tapeout, No NRE
- Potentially instant time-to-market

Platform FPGAs Will Be Cheap

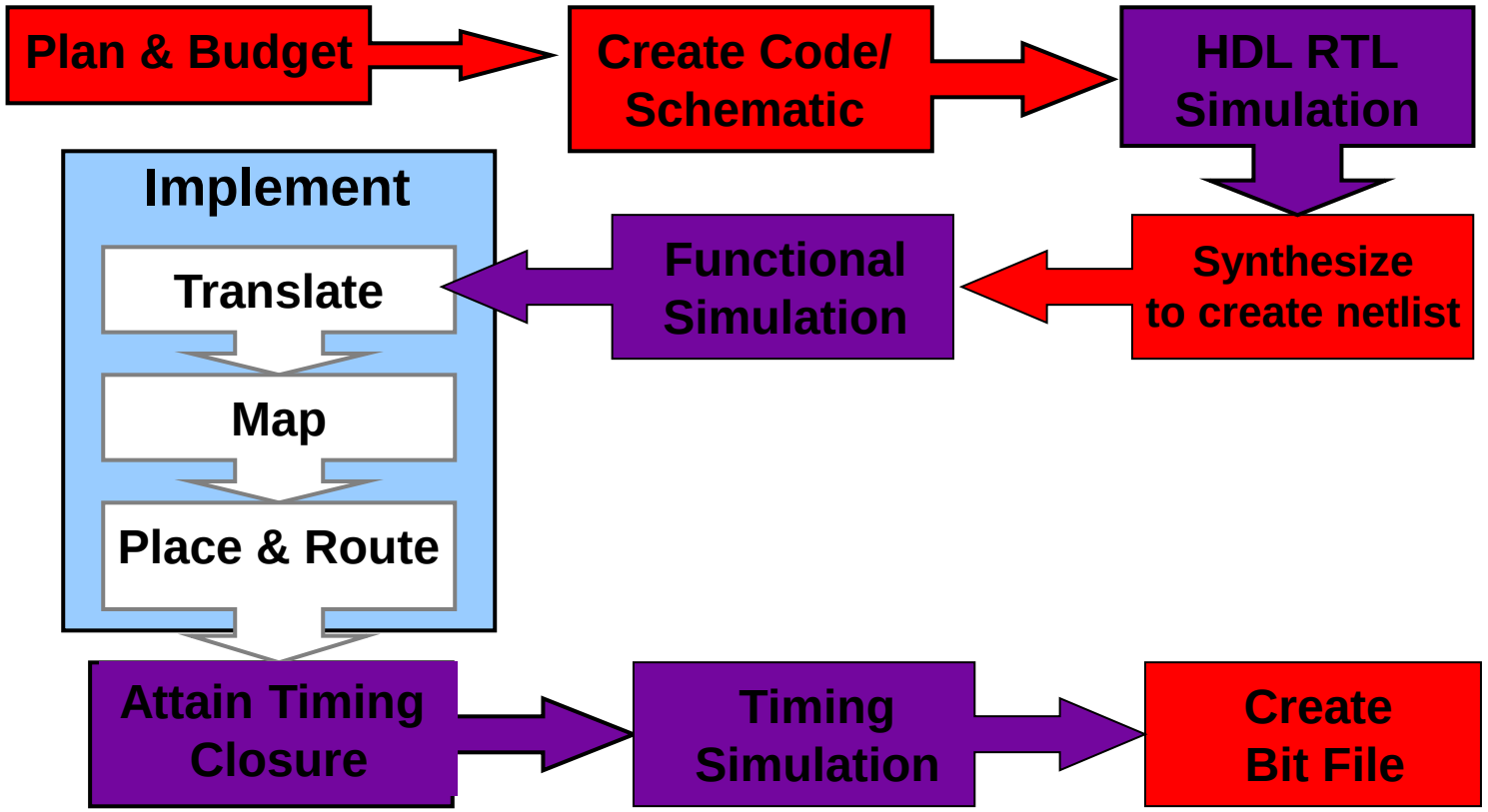
- Today:
  - Top end: Virtex-II 6000
    - 1M real ASIC gates + RAM, etc.
  - High volume: Spartan-IIE 300:
    - 100K real ASIC gates + RAM, etc.
    - "$18 in volume, 2H2002"
- Apply Five Years of Moore's La
  - Top end: 10M ASIC gates + CPU,
  - High volume: 1M ASIC gates + CPU, RAM, etc.
- Future's high volume = today's top end
  - **Platform FPGAs for < $20 in 2004-5**



FPGA Applications

- Complex building blocks (ASIC replacement) in cellular base stations, telecom switches, computer peripherals, high speed servers, instrumentation, etc.
- **Any application in which cost, speed and power requirements are met!**

Mapping CAD Tools: Xilinx ISE Design Flow



Mapping CAD Tools

- Fully automatic (push button) compilation in most cases
  - manual intervention for dense and fast implementations
- Front end synthesis tool vendors: Mentor, Synopsys
- Back end tools provided by FPGA vendors, e.g. Xilinx ISE and Altera Quartus.
- Optimized and synthesizable "IP cores" provided for many applications such as filtering, binary arithmetic, etc.