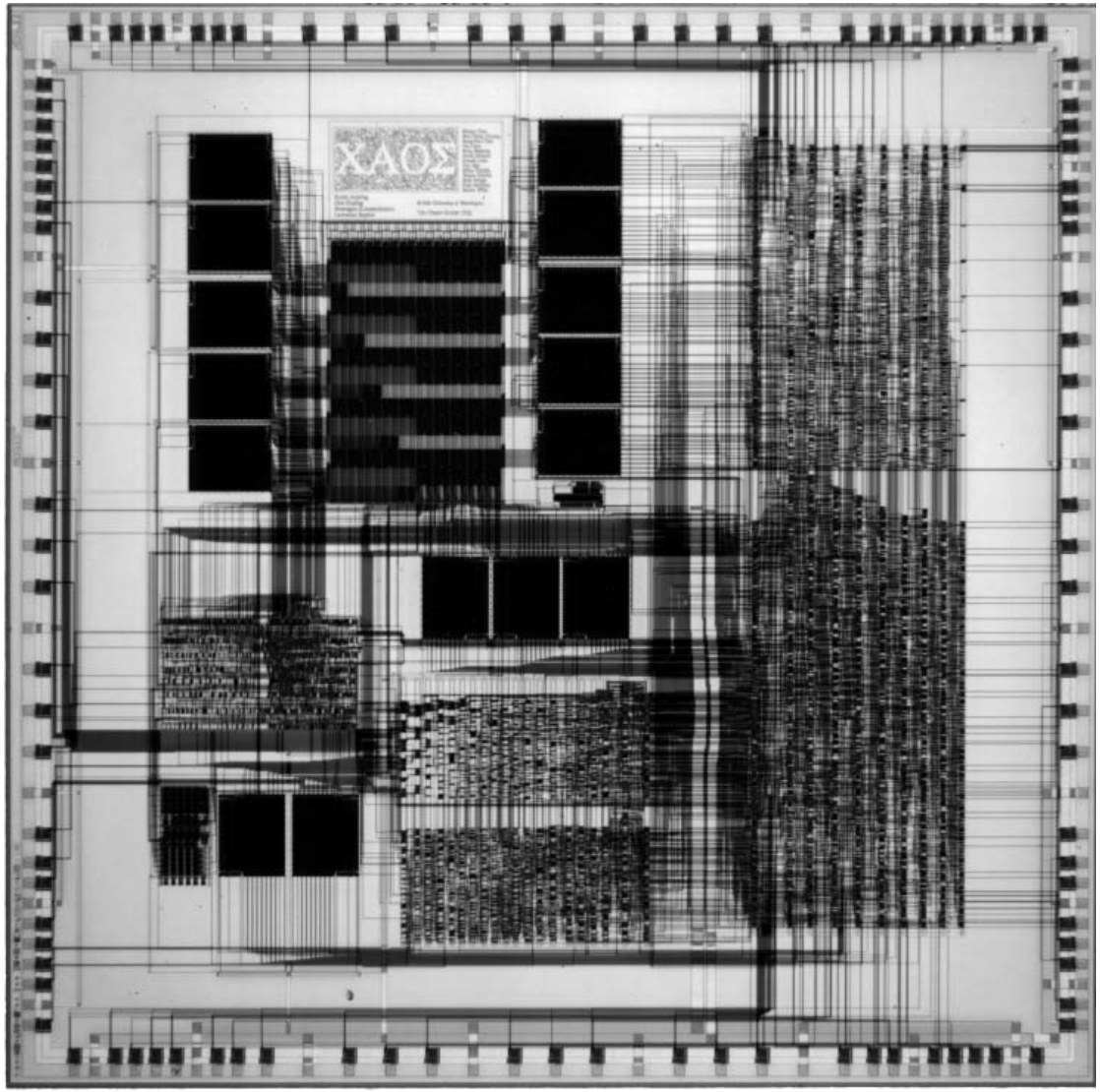
VLSI: Very Large-Scale Integration



CAD & Physical Design

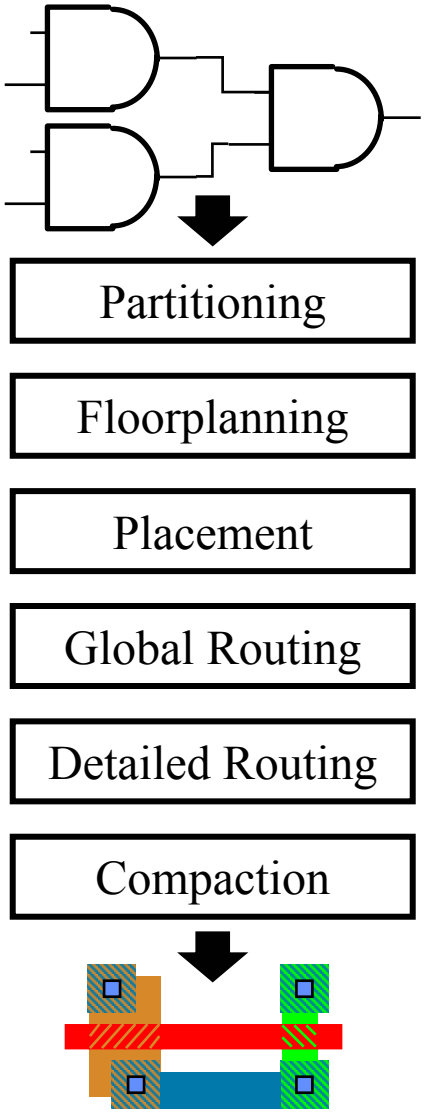
CAD = Computer Aided Design

Complexity of today's circuits requires computer support for most design tasks

CAD split into Synthesis, Physical Design

Synthesis = translating designer requirements into a circuit graph

PD = translating circuit graph into layout ("blueprint") for fabrication

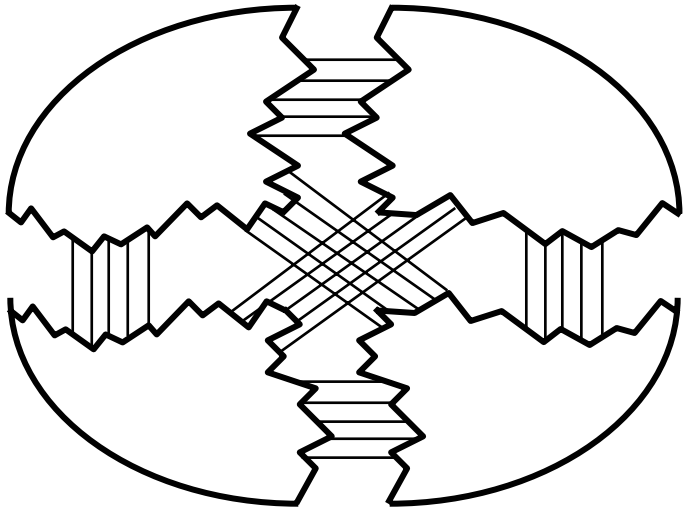


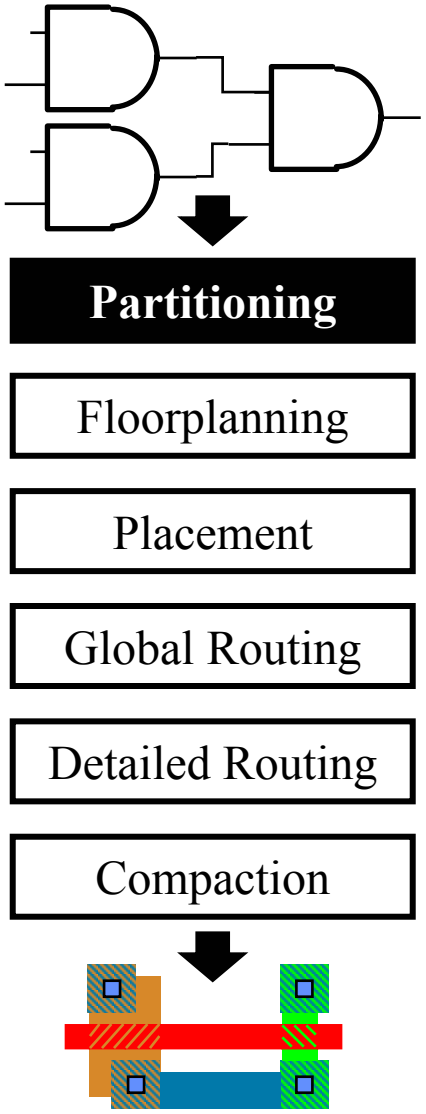
Partitioning

Circuits can exceed chip capacity

Split circuits into chip-sized subcircuits

- Meet capacity constraints
- Reduce interconnect demand
- Meet performance requirements



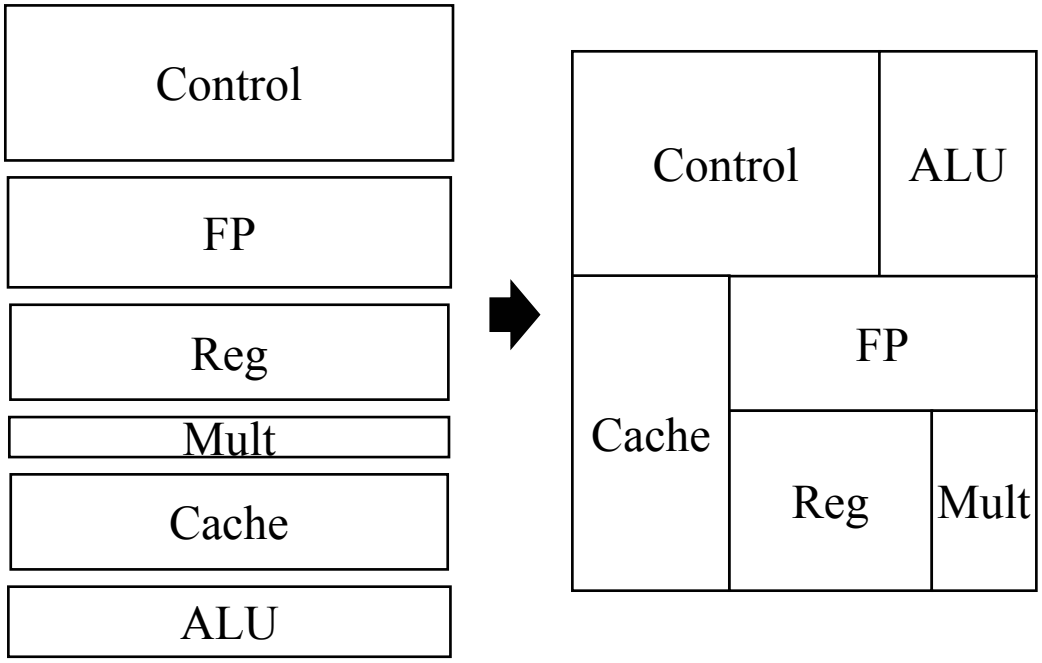


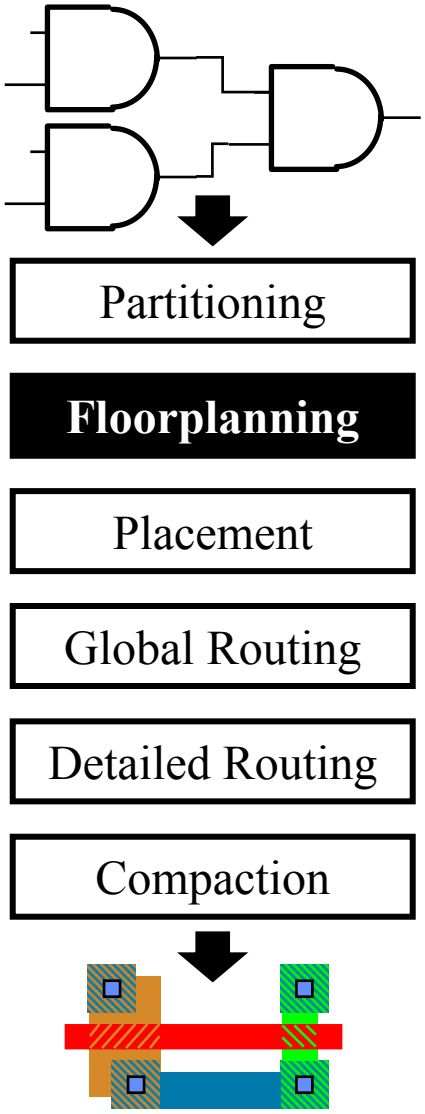
Floorplanning

Assign portions of a design to regions of the chip area

Blocks have adjustable sizes

Seek to reduce routing delay & area





Placement

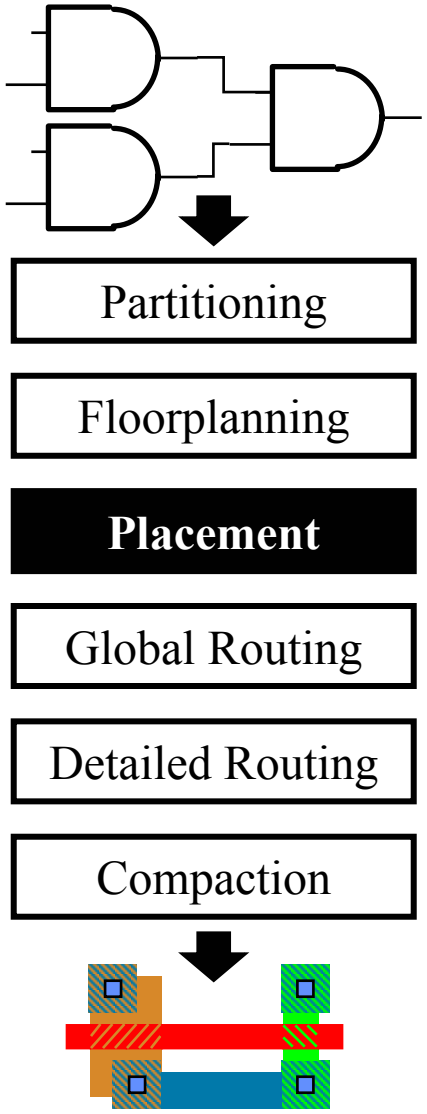
Pick relative location for each gate

Seek to improve routeability, limit delay, reduce overall area

NAND	AOI

DFF	INV	NOR

DFF	NOR	DFF

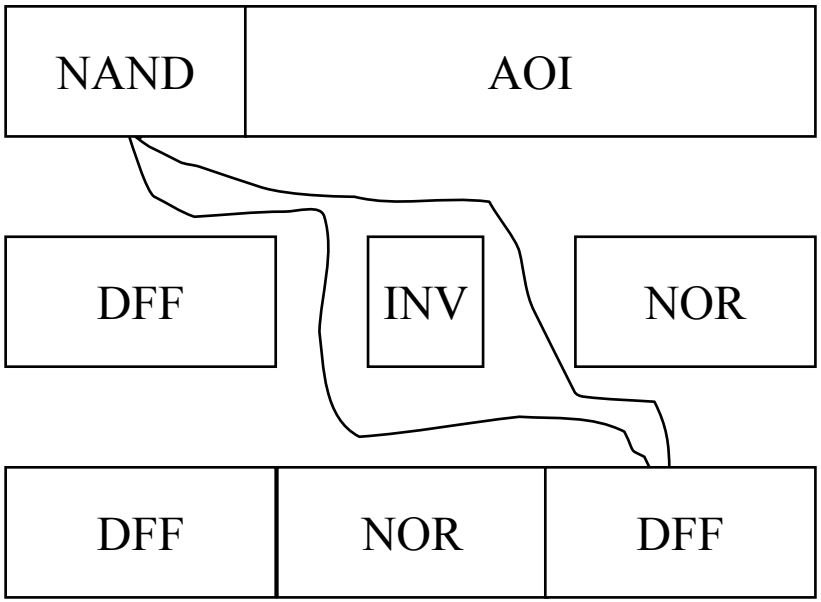


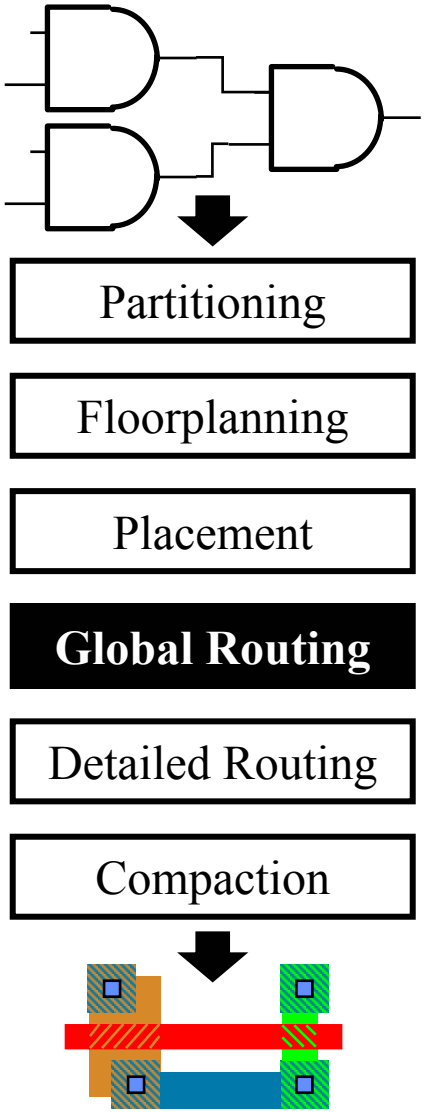
Global Routing

Determine overall path of all routes

Pick channels to route through

Seeks to reduce delay, channel widths

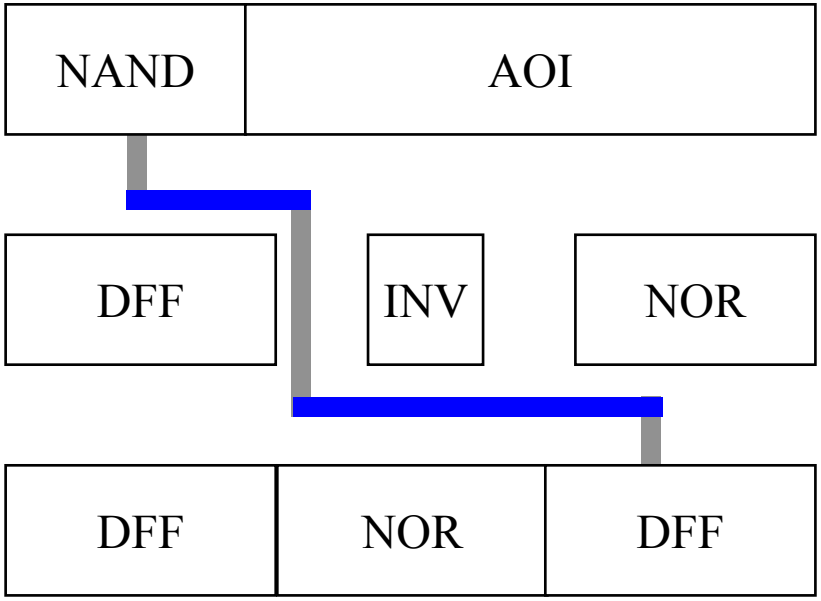


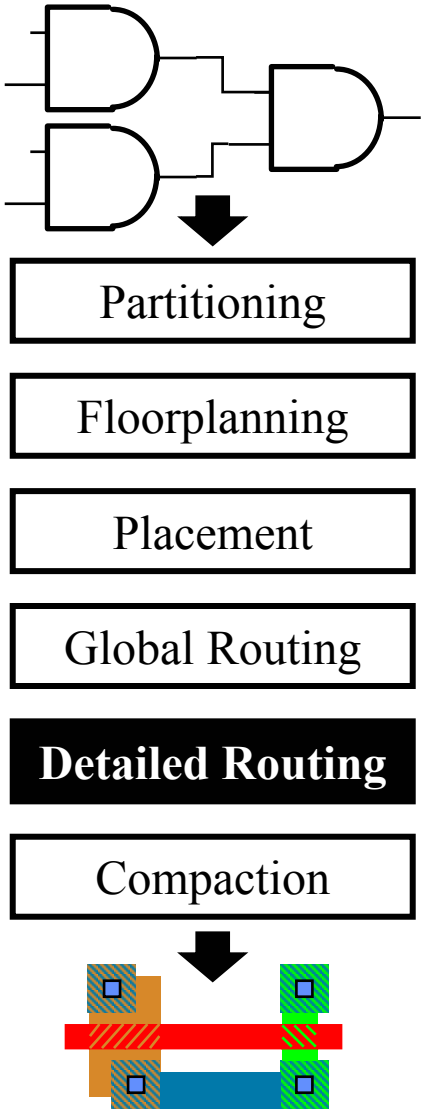


Detailed Routing

Determine exactly how each signal is routed through each region

Seeks to reduce routing area





Compaction

Squeeze layout to reduce chip area

- Helps eliminate inefficiencies caused by other steps