



Collect essential information from the job posting to create a customized cover letter on this worksheet. **Use your answers on this worksheet to create your cover letter.** You will be evaluated on how well you followed instructions and completed this worksheet. Provide this worksheet and your finished cover letter, at a virtual meeting during the dates given on your professional development timeline.

## INSTRUCTIONS

### Part 1: Preparation

1. Choose a job posting from the *Cover Letter Assignment Job Postings Resource* that suits your skills and abilities or chose another job\* that you have found on your own (\*cannot be your VIP role, must have a detailed job description, and you must provide a copy of the full job description).
2. Read the job posting carefully and cut and paste the following information into this worksheet from the posting (use as much space as you need):
  - a. Transferable Skills (can be used in many different jobs): Teamwork, Leadership skills, Communication skills, Interpersonal skills
  - b. Specific Skills (are only used in this type of job): ASIC design, DFT techniques, Verilog simulator and waveform debugging tools, Logic design, STA, Synthesis, Equivalency checking, UNIX/Linux, Scripting (TCL, c-shell, Perl), C++, ATE, Digital IC manufacturing, Emulator for ATPG pattern verification
  - c. Knowledge and/or Educational Requirements: Minimum B.Sc in Electrical or Computer Engineering (or equivalent)
  - d. Other requirements: DFT design skills, Project execution experience, Verbal/Written communication skills, Self-driven, Disciplined, Time management, Work independently/collaboratively
3. To whom are you sending the letter? For this exercise, we have provided you with this information within the job posting. If it is not listed directly on the job posting you found on your own, find the name and address of your contact by either calling the company directly or researching online.
  - a. Company Contact Full Name: Don Sweet
  - b. Organization Name: Advanced Micro Devices, Inc. (AMD)
  - c. Street Address: 7171 Southwest Pkwy
  - d. City, Province, Postal Code: Austin, TX 78735

### Part 2: First Paragraph

**Use your answers to these 3 questions to create your first paragraph**

1. What is the exact title of the job? Is there a reference number for this job? If so, include both.  
Design for Test Engineer - Central DFT -- Requisition Number: 96162

2. How did you learn about the position and company? If you have a contact at the company, who are they?  
Linkedin Job posting
3. Why are you interested in this specific job and company? (e.g., type of work, reputation, opportunities).  
Avoid stating what the position can do for you.  
AMD is a well-known company that develops computer processors and related technologies for business and consumer markets. Also, I have ~6 years of experience in DFT(ATPG) software testing

### Part 3: Second Paragraph

What are your most significant accomplishments, abilities, and experiences that are **directly relevant** to the specific job requirements? Do not include anything that the employer is not asking for in their job description. Use this chart to show how your experience matches up with exactly what the employer is looking for. (Use as much space as you need)

Job Requirement (cut and paste from job description)	Your related accomplishment, experience, or ability (include evidence of how/where)
<b><u>TECHNICAL SKILL REQUIREMENTS</u></b>	
<ul style="list-style-type: none"> <li>• Demonstrated DFT design skills and project execution experience :: Demonstrated ASIC design experience</li> <li>• Experience in complex ASIC design (multi-million gates) in DFT/DFD techniques such as JTAG/IEEE standards, scan and ATPG, on-chip test pattern compression and at-speed testing using PLL, memory BIST, and repair, logic BIST, power-gating, on-chip debug logic, testing of high-speed SerDes IO and analog design</li> <li>• Understanding various technologies that must work with DFT/DFD technology such as CPUs, graphics engines, high-speed digital design, memory, I/O controllers, ... etc.</li> <li>• Expertise in scan compression architecture, scan insertion, and ATPG methodologies are essential</li> <li>• Experience in solving logic design or timing issues with integration, synthesis, and PD teams</li> <li>• Knowledge in EDA tools/methodology, such as synthesis, equivalency checking, static timing analysis</li> <li>• Knowledge of ATE and digital IC manufacturing tests is a plus</li> <li>• Knowledge of using emulators for ATPG pattern verification is a plus</li> </ul>	<ul style="list-style-type: none"> <li>• Approximately 6 years of work experience in the DFT EDA domain at Cadence design systems.</li> <li>• Worked on several <b>DFT synthesis</b> (Cadence Genus tool) and <b>ATPG pattern generation</b> (Cadence Modus tool) features as a product validation engineer.</li> <li>• <b>DFT scan insertion</b> including <b>LBIST, MBIST, and JTAG</b> performed for several designs as part of feature testing of Genus/Modus.</li> <li>• Performed <b>IJTAG feature reporting</b> bugs to RnD.</li> <li><b>Scan insertion and ATPG pattern generation</b> were undertaken for several large designs from TI, IBM, GF, TSMC, etc., with millions of gates and flops.</li> <li>• <b>ASIC design experience</b> working as an intern at Aarish technologies. Specifically, knowledge about <b>physical design (PD)</b> i.e., placement and routing using genus and Innovus.</li> <li>• <b>Placement-driven (PD) synthesis</b> performed in Makefile-based environment on Linux operating system. Beginner in logic equivalence checking resolving some LEC issues.</li> <li>• <b>Basic knowledge about Automatic Test Equipment (ATE).</b></li> <li>• <b>Strong fundamentals in digital IC manufacturing.</b></li> </ul>

<p>Working knowledge and experience in Verilog simulator and waveform debugging tools, proficiency in debugging both RTL and gate level simulations</p>	<ul style="list-style-type: none"> <li>• Experienced in using both ModelSim (Mentor Graphics simulator) and Xcelium (Cadence simulator) tools</li> <li>• <b>RTL simulations and gate-level simulations executed</b> for many designs at Cadence designs systems as part of feature testing of Genus/Modus software.</li> <li>• <b>Debugging Verilog design for issues using waveform debugging tool.</b> Wrote wrapper Verilog for memories generated using GlobalFoundries memory compilers and did Verilog simulation and waveform debugging while working as an intern at Aarish technologies.</li> </ul>
<p style="text-align: center;"><b><u>ADDITIONAL QUALIFICATIONS</u></b></p>	
<ul style="list-style-type: none"> <li>• Good working knowledge of UNIX/Linux and scripting languages (e.g., TCL, c-shell, Perl), C++ programming</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Excellent scripting skills</b> (in <b>TCL, c-shell, Perl, Python</b>) learned at Cadence Design Systems as part of daily tasks working on several Linux operating systems like RHEL, SLES, CentOS, and LOP.</li> <li>• I have <b>developed several projects</b> both professionally and personally (Some project links on GitHub: <a href="#">Minesweeper in Tcl</a>, <a href="#">Virtual Machine Translator in Tcl</a>, <a href="#">Software Foundation Course on using Linux tools like sed/awk/bash</a> )</li> <li>• Intermediate level <b>programming experience in C++</b> demonstrated by projects developed during High school, B.Tech. at JMI and MASc. at UWindsor (Project link on GitHub: <a href="#">ELEC-8590</a> )</li> <li>• Have <b>completed several courses and received certifications for scripting and programming</b> (both offline and online) – Refer to resume/LinkedIn profile</li> </ul>
<p style="text-align: center;"><b>TRANSFERABLE SKILL REQUIREMENTS</b></p>	
<ul style="list-style-type: none"> <li>• Demonstrated technical leadership and works well with cross-functional teams</li> <li>• Excellent communication and interpersonal skills</li> <li>• Excellent verbal and written communication and interpersonal skills</li> <li>• Self-starter, driven and disciplined with a dedication to meeting deadlines</li> <li>• Has an aptitude to thrive in a fast-paced multi-tasking environment</li> <li>• Used to working independently, and yet can work collaboratively with various levels and organization functions.</li> </ul>	<ul style="list-style-type: none"> <li>• Approximately 6 years of work experience at Cadence Design Systems, managing and maintaining thousands of test cases and improving turn time from days to hours by scripting/automating. <b>Demonstrated abilities to communicate, do critical thinking and solve problems.</b></li> <li>• <b>Time management, project planning and management, writing skills, teamwork, and communication skills</b> applied and exercised as part of volunteering activity for various organizations.</li> <li>• As a Mitacs research intern, my role involved <b>teamwork in an online environment</b> owing to COVID where I <b>worked independently</b> and used my <b>communication skills to effectively convey my ideas</b> to complete the <b>assigned work on time.</b></li> <li>• <b>Teaching experience and time management skills</b> gained as part of a graduate assistantship at the</li> </ul>

	University of Windsor, all this while doing thesis work and internship at Aarish Technologies. • A <b>lifelong, and quick learner</b> with a passion to learn exemplified by learning interests and good skills in Maths/Science since high school.
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**Using the chart above**, now create three sentences that include keywords from the job description to describe how you have what they want. Use action words. Include real examples from your experiences to demonstrate your suitability for the position **from the chart above**. These statements describe what abilities or experiences you have that are directly relevant to the position and they show how you gained the ability or experience. **Include these statements in the second paragraph of your cover letter**. If you already crafted sentences within the chart above that meet these requirements, then you can cut and paste them below.

1. DFT scan insertion including LBIST, MBIST, and JTAG performed for several designs as part of feature testing of Genus/Modus. Worked on IJTAG feature, reporting bugs to RnD. Scan insertion and ATPG pattern generation were carried out for several large designs from TI, IBM, GF, TSMC, etc., with millions of gates and flops.
2. Excellent scripting skills (in TCL, c-shell, Perl, Python) learned at Cadence Design Systems as part of daily tasks working on several Linux operating systems like RHEL, SLES, CentOS, and LOP. I have developed several projects both professionally and personally (Some project links on GitHub: [Minesweeper in Tcl](#), [Virtual Machine Translator in Tcl](#), [Software Foundation Course on using Linux tools like sed/awk/bash](#) )  
Intermediate level programming experience in C++ demonstrated by projects developed during High school, B.Tech. at JMI and MASc. at UWindsor (Project link on GitHub: [ELEC-8590](#) )  
Have finished several courses and received certifications for scripting and programming (both offline and online) – Refer to resume/LinkedIn profile
3. Demonstrated abilities to communicate, do critical thinking and solve problems. Teamwork and professionalism skills gained as part of volunteering experience while working with different organizations. Teaching experience and time management skills gained as part of a graduate assistantship at the University of Windsor, all this while doing thesis work and internship at Aarish Technologies. A Lifelong learner with a passion to learn exemplified by learning interests and good skills in Maths/Science since high school.

#### Part 4: Final Paragraph

The information in the last paragraph can vary according to each job description. Use this checklist to determine what you need to include:

- ☒ Have you thanked the employer for considering your resume?
- ☒ Have you indicated that you are confidently seeking an interview?
- ☒ Have you told the employer you are willing to relocate, work flexible hours, or have a car (if the job asked for such things)?
- ☒ Have you included your phone number and UWindsor email address?

#### Part 5: Putting It All Together

Now that you have filled out everything above, you have what you need to write a customized cover letter for the specific job posting you chose. Create your cover letter in paragraph format **using your answers from this worksheet**. It should look like this:

*Your Name*

*Your Address*

*Your City, Province, Postal Code*

*Date*

*Company Contact's Name*

*Organization*

*Street Address*

*City, Province, Postal Code*

*Dear [Contact Full Name],*

*[First Paragraph]*

*[Second Paragraph]*

*[Third/Final Paragraph]*

*Sincerely,*

*[Full name and signature]*

Your cover letter should be 1 page in length and consist of three paragraphs. Speak of what you can do for the company, NOT what you can gain from the company. Your letter should not be a summary of your resume; it should draw interest and attention to your resume. It is alright if you cannot fit all of your related skills and abilities into your cover letter, choose the most relevant.

This document is adapted from:

“Cover Letter Checklist.” *Brigham Young University Career Services*.

<https://ucs.byu.edu/sites/default/files/handouts/HUMCoverLetterChecklist.pdf>.