Hardware Characteristics:8086 (REVISITED)

27/11/12

The Pin-Out

- packaged in 40-pin **dual in-line** packages (DIPs)
- 8086 is a 16-bit microprocessor with a 16-bit data bus
  - 8086 has pin connections AD_0–AD_{15}

Power Supply Requirements

- Require +5.0 V with a supply voltage tolerance of ±10 percent.
- 8086 uses a maximum supply current of 360 mA
- Operate in ambient temperatures of between 32° F and 180° F.
- 80C86 is CMOS versions that require only 10 mA of power supply current.
  - and function in temperature extremes of –40° F through +225° F

DC Characteristics

- It is impossible to connect anything to a microprocessor without knowing input current requirement for an input pin.
  - and the output current drive capability for an output pin
- This knowledge allows to select proper interface components for use with the microprocessor
  - without the fear of damaging anything

Input Characteristics

- Input characteristics compatible with all the standard logic components available today.
- The input current levels are very small because the inputs are the gate connections of MOSFETs and represent only leakage currents.

Output Characteristics

- The logic 1 voltage level of the 8086 is compatible with most standard logic families.
  - logic 0 level is not
- Standard logic circuits have a maximum logic 0 voltage of 0.4 V; 8086 has a maximum of 0.45 V.
  - a difference of 0.05 V
- This difference reduces the noise immunity from 400 mV (0.8 V – 0.45 V) to 350 mV.
- Reduction in noise immunity may result in problems with long wire connections or too many loads.
- No more than 10 loads of any type should be connected to an output pin without buffering

BUS BUFFERING AND LATCHING

- Before 8086 can be used with memory or I/O interfaces, their multiplexed buses must be demultiplexed.
- Because the maximum fan-out is 10, the system must be buffered if it contains more than 10 other components

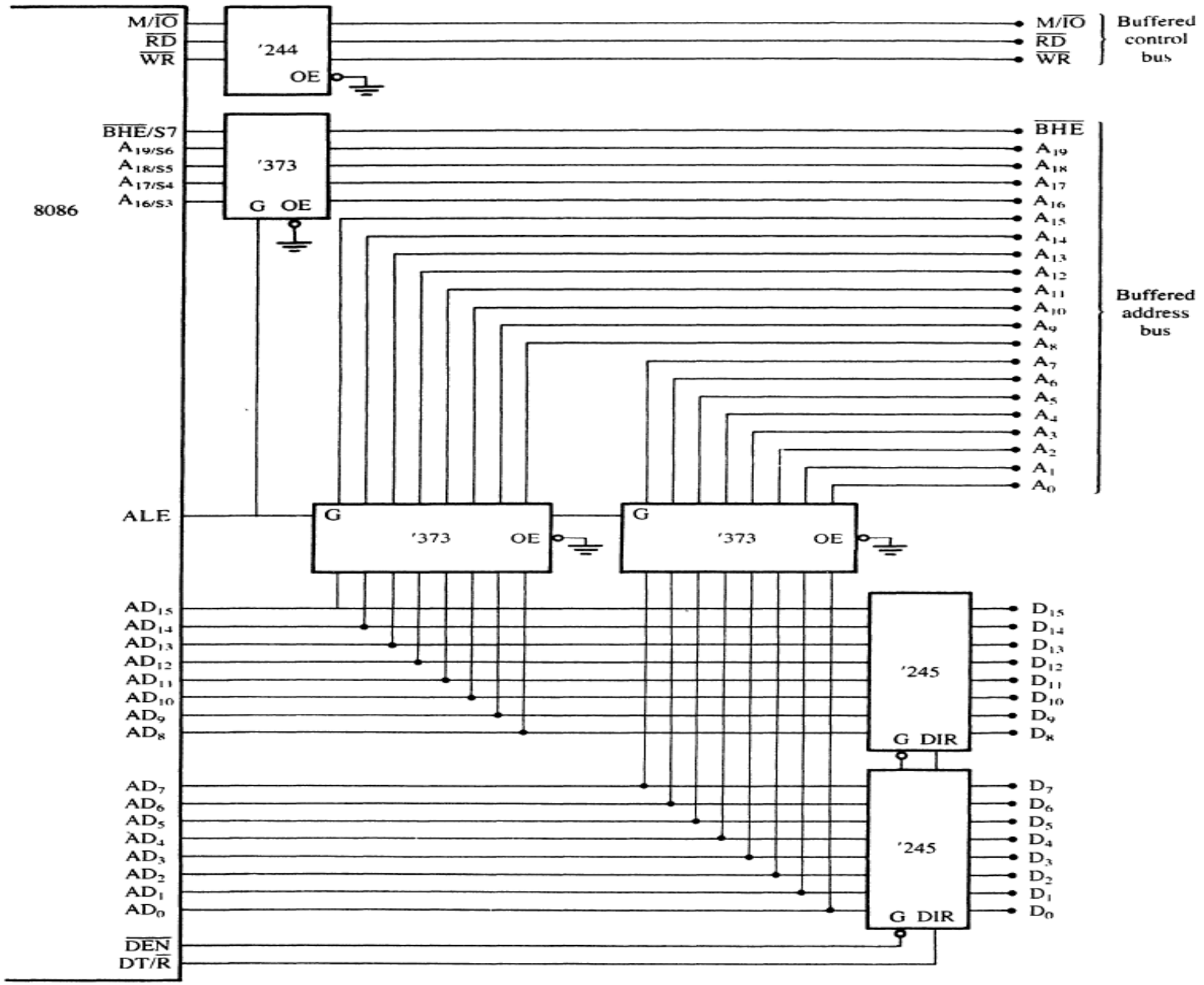
The Buffered System

- If more than 10 unit loads are attached to any bus pin, the entire system must be buffered.
- Buffer output currents have been increased so that more TTL unit loads may be driven.
- A fully buffered signal will introduce a timing delay to the system.
- No difficulty unless memory or I/O devices are used which function at near maximum bus speed.

The Fully Buffered 8086

- Figure illustrates a fully buffered 8086.
  - a fully buffered 8086 system requires one 74LS244, two 74LS245s, and three 74LS373s
- 8086 requires one more buffer than 8088 because of the extra eight data bus connections, D_{15}–D_8.
- It also has a $\overline{\text{BHE}}$ signal that is buffered for memory-bank selection.

Figure /
8086 m



- All computer systems have three buses:
  - an address bus that provides memory and I/O with the memory address or the I/O port number
  - a data bus that transfers data between the microprocessor and the memory and I/O
  - a control bus that provides control signals to the memory and I/O
- These buses must be present in order to interface to memory and I/O.

Pin Connections AD_7 - AD_0

- **Address/data bus** lines are multiplexed
  - ALE=logic1,Address on the bus
    - contain the rightmost 8 bits of the memory address or I/O port number
  - ALE=logic0,Data on the bus
- These pins are at their high-impedance state during a hold acknowledge.

Pin Connections A_{15} - A_8

- **address bus** provides the upper-half memory address bits that are present throughout a bus cycle.
- These address connections go to their high-impedance state during a hold acknowledge.

Pin Connections AD_{15} - AD_8

- 8086 **address/data bus** lines compose upper multiplexed address/data bus on the 8086.
- These lines contain address bits A_{15}–A_8 whenever ALE is a logic 1, and data bus connections D_{15}–D_8 when ALE is a logic 0.
- These pins enter a high-impedance state when a hold acknowledge occurs.

BHE S_7

- The **bus high enable** pin is used in 8086 to enable the most-significant data bus bits (D_{15}–D_8) during a read or a write operation.
- The state of S_7 is always a logic 1.

Pin Connections A_{19}/S_6 - A_{16}/S_3

- **Address/status bus** bits are multiplexed to provide address signals A_{19}–A_{16} and status bits S_6–S_3.
  - high-impedance state during hold acknowledge
  - status bit S_6 is always logic 0,
  - bit S_5 indicates the condition of the IF flag bit
- S_4 and S_3 show which segment is accessed during the current bus cycle.

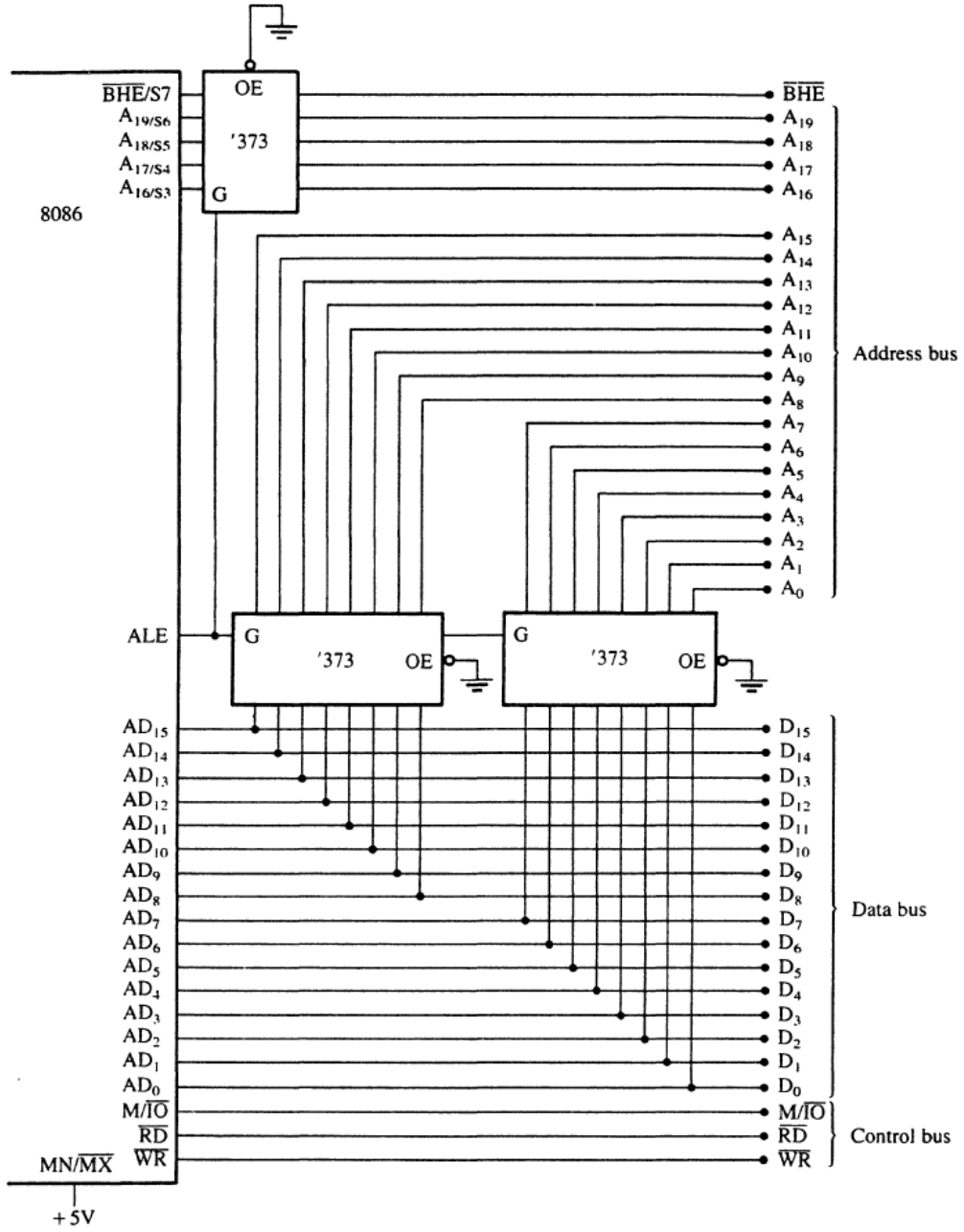
Demultiplexing the Buses

- The address/data bus of the 8086 is multiplexed (shared) to reduce the number of pins required for the integrated circuit
  - the hardware designer must extract or demultiplex information from these pins
- Memory & I/O require the address remain valid and stable throughout a read/write cycle.
- If buses are multiplexed, the address changes at the memory and I/O, causing them to read or write data in the wrong locations

Demultiplexing the 8086

- Figure illustrates a demultiplexed 8086 with all three buses:
- address (A_{19}–A_0 and $\overline{BHE}$)
- data (D_{15}–D_0), $\overline{\quad}$ $\overline{\quad}$
- control (M/$\overline{IO}$,$\overline{RD}$, and $\overline{WR}$)
- Here, the memory and I/O system see the 8086 as a device with:
  - a 20-bit address bus;16-bit data bus
  - and a three-line control bus

Figure : The 8086 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8086-based systems.



Pin Connections $\overline{RD}$

- When **read signal** is logic 0, the data bus is receptive to data from memory or I/O devices
  - pin floats high-impedance state during a hold acknowledge

Ready

- Inserts wait states into the timing.
  - if placed at a logic 0, the microprocessor enters into wait states and remains idle
  - if logic 1, no effect on the operation

Pin Connections INTR

- **Interrupt request** is used to request a hardware interrupt.
  - If INTR is held high when IF = 1, 8086 enters an interrupt acknowledge cycle after the current instruction has completed execution

NMI

- The **non-maskable interrupt** input is similar to INTR.
  - does not check IF flag bit for logic 1
  - if activated, uses interrupt vector 2

Pin Connections $\overline{\text{TEST}}$

- The **Test** pin is an input that is tested by the WAIT instruction.
- If $\overline{\textbf{TEST}}$ is a logic 0, the WAIT instruction functions as an NOP.
- If $\overline{\textbf{TEST}}$ is a logic 1, the WAIT instruction waits for $\overline{\textbf{TEST}}$ to become a logic 0.
- The $\overline{\textbf{TEST}}$ pin is most often connected to the 8087 numeric coprocessor.

Pin Connections RESET

- Causes the microprocessor to reset itself if held high a minimum of four clocking periods.
  - when 8086 is reset, it executes instructions at memory location FFFFOH
  - also disables future interrupts by clearing IF flag

CLK

- The **clock** pin provides the basic timing signal.
  - must have a duty cycle of 33 % (high for one third of clocking period, low for two thirds) to provide proper internal timing

Pin Connections VCC

- This **power supply** input provides a +5.0 V, ±10 % signal to the microprocessor.

GND

- The **ground** connection is the return for the power supply.
  - 8086 microprocessors have two pins labeled GND—both must be connected to ground for proper operation

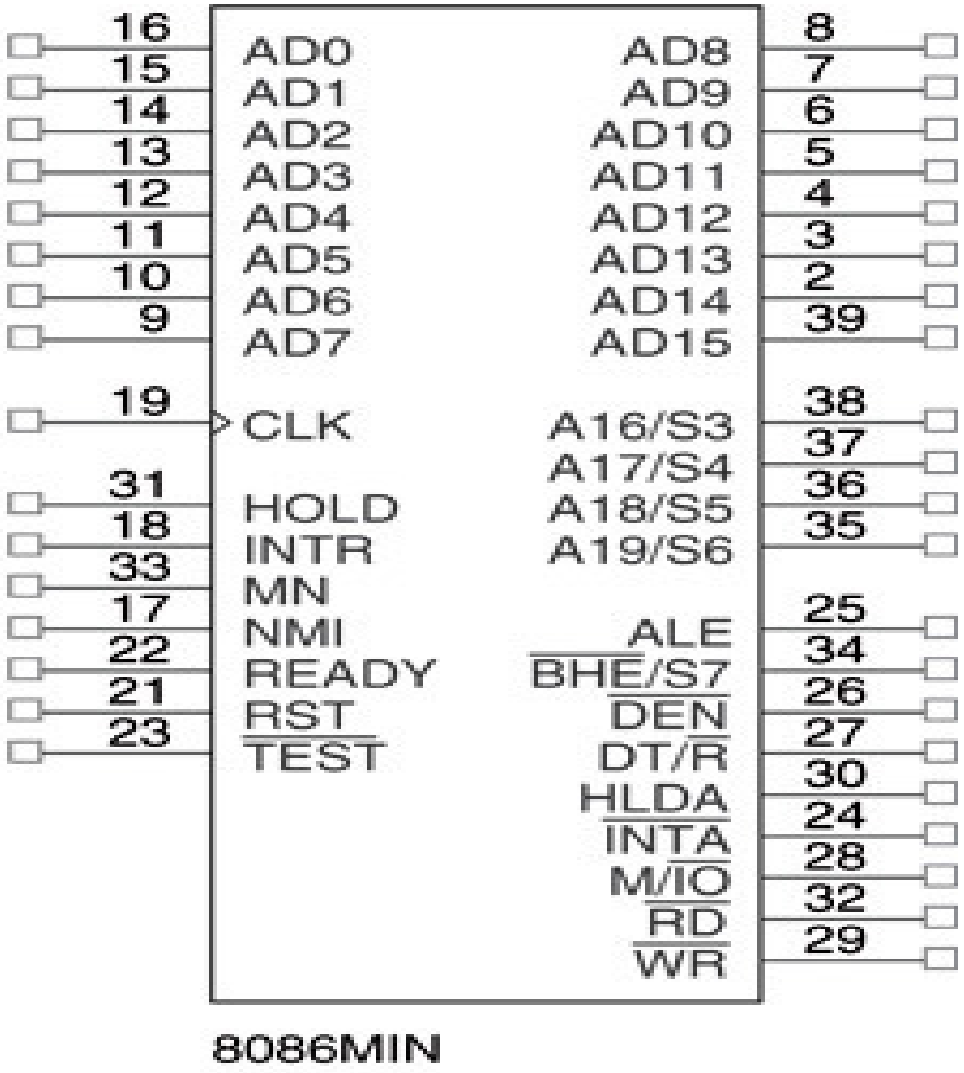
Pin Connections MN/$\overline{MX}$

- **Minimum/maximum** mode pin selects either minimum or maximum mode operation.
  - if minimum mode selected, the MN/$\overline{MX}$ pin must be connected directly to +5.0 V

MINIMUM VS MAXIMUM MODE

- Minimum mode is obtained by connecting the mode selection MN/$\overline{MX}$ pin to +5.0 V,
  - maximum mode selected by grounding the pin
- The mode of operation provided by minimum mode is similar to that of the 8085A
  - the most recent Intel 8-bit microprocessor
- Maximum mode is designed to be used whenever a coprocessor exists in a system.

Figure the pin-out of the 8086 in minimum mode.



(b)

Minimum Mode Pins

- Minimum mode operation is obtained by connecting the MN/$\overline{\text{MX}}$ pin directly to +5.0 V.

M/$\overline{\text{IO}}$

- The **M/$\overline{\text{IO}}$** (8086) pin selects memory or I/O.
  - indicates the address bus contains either a memory address or an I/O port address.
  - high-impedance state during hold acknowledge

Minimum Mode Pins WR

- **Write line** indicates 8086 is outputting data to a memory or I/O device.
  - during the time $\overline{WR}$ is a logic 0, the data bus contains valid data for memory or I/O
  - high-impedance during a hold acknowledge

$\overline{INTA}$

- The **interrupt acknowledge** signal is a response to the INTR input pin.
  - normally used to gate the interrupt vector number onto the data bus in response to an interrupt

Minimum Mode Pins ALE

- **Address latch enable** shows the 8086 address/data bus contains an address.
  - can be a memory address or an I/O port number
  - ALE signal doesn't float during hold acknowledge

$\mathbf{DT/\overline{R}}$

- The **data transmit/receive** signal shows that the microprocessor data bus is transmitting (**$DT/\overline{R} = 1$**) or receiving (**$DT/\overline{R} = 0$**) data.
  - used to enable external data bus buffers

Minimum Mode Pins HLDA

- **Hold acknowledge** indicates the 8086 has entered the hold state.

$\overline{SS0}$

- The $\overline{SS0}$ status line is equivalent to the S_0 pin in maximum mode operation.
- Signal is combined with **$\overline{IO}$/M** and **DT/$\overline{R}$** to decode the function of the current bus cycle.

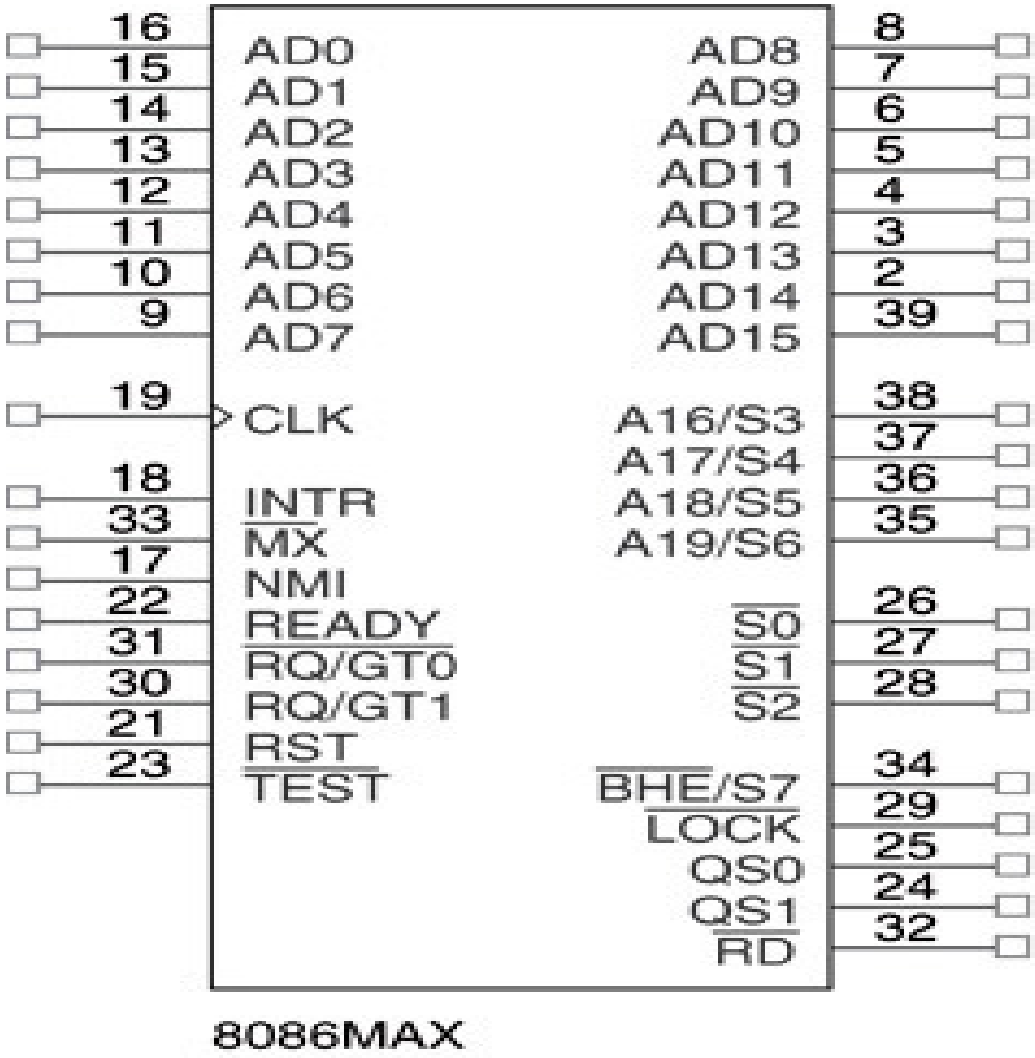
Minimum Mode Pins DEN

- **Data bus enable** activates external data bus buffers.

HOLD

- **Hold input** requests a direct memory access (DMA).
  - if HOLD signal is a logic 1, the microprocessor stops executing software and places address, data, and control bus at high-impedance
  - if a logic 0, software executes normally

Figure (a) The pin-out of the 8086 in maximum mode;



(a)

Maximum Mode Pins

- In order to achieve maximum mode for use with external coprocessors, connect the MN/$\overline{MX}$ pin to ground.

$\overline{S2}$, $\overline{S1}$, and $\overline{S0}$

- **Status bits** indicate function of the current bus cycle.
  - normally decoded by the 8288 bus controller

Maximum Mode Pins $\overline{\text{RQ}}/\overline{\text{GT1}}$

- The **request/grant** pins request direct memory accesses (DMA) during maximum mode operation.
  - bidirectional; used to request and grant a DMA operation

$\overline{\text{LOCK}}$

- The **lock** output is used to lock peripherals off the system. This pin is activated by using the LOCK: prefix on any instruction.

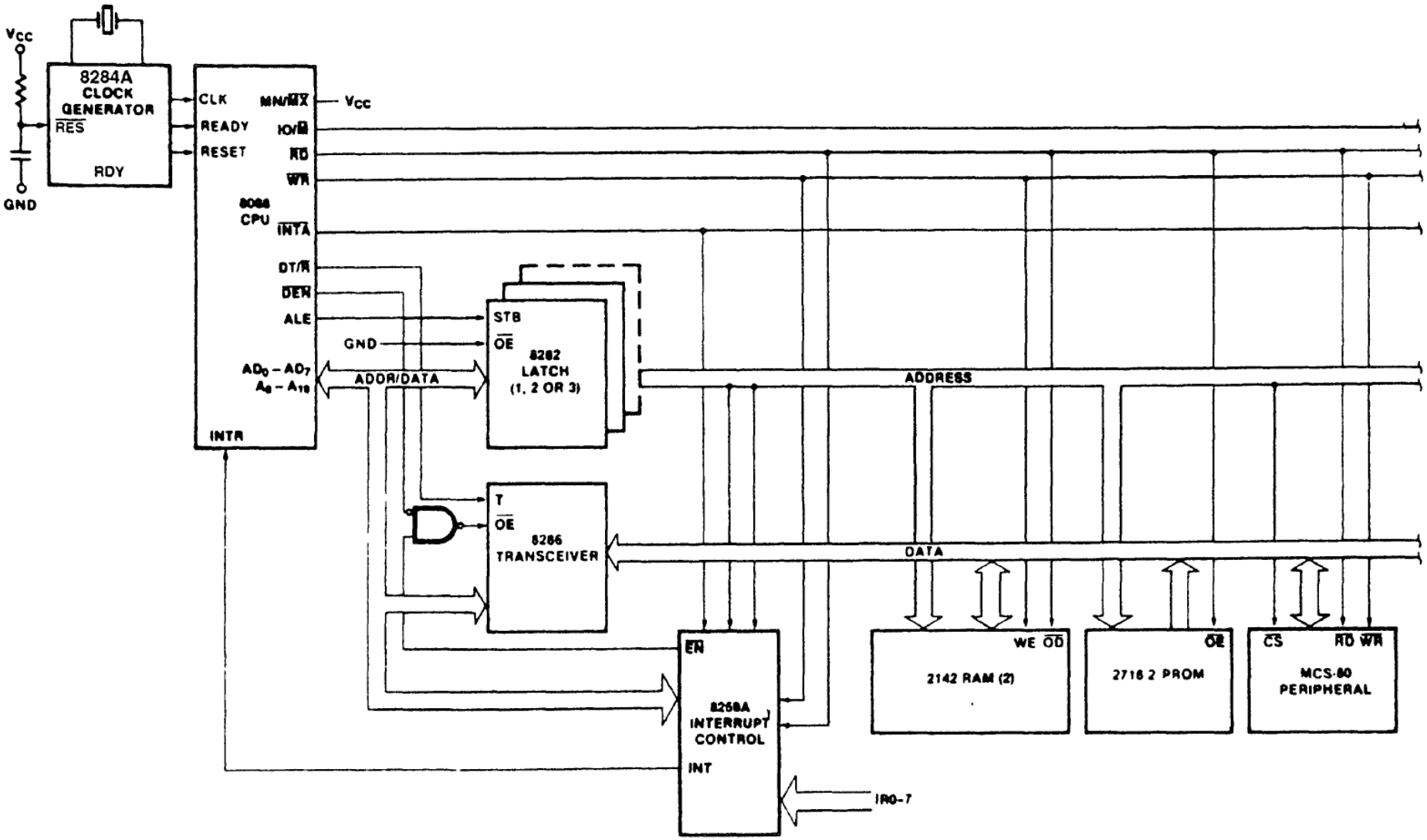
Maximum Mode Pins QS_1 and QS_0

- The **queue status** bits show the status of the internal instruction queue.
  - provided for access by the 8087 coprocessor

Minimum Mode Operation

- Least expensive way to operate 8086.
  - because all control signals for the memory & I/O are generated by the microprocessor
- Control signals are identical to Intel 8085A.
- The minimum mode allows 8085A 8-bit peripherals to be used with the 8086 without any special considerations.

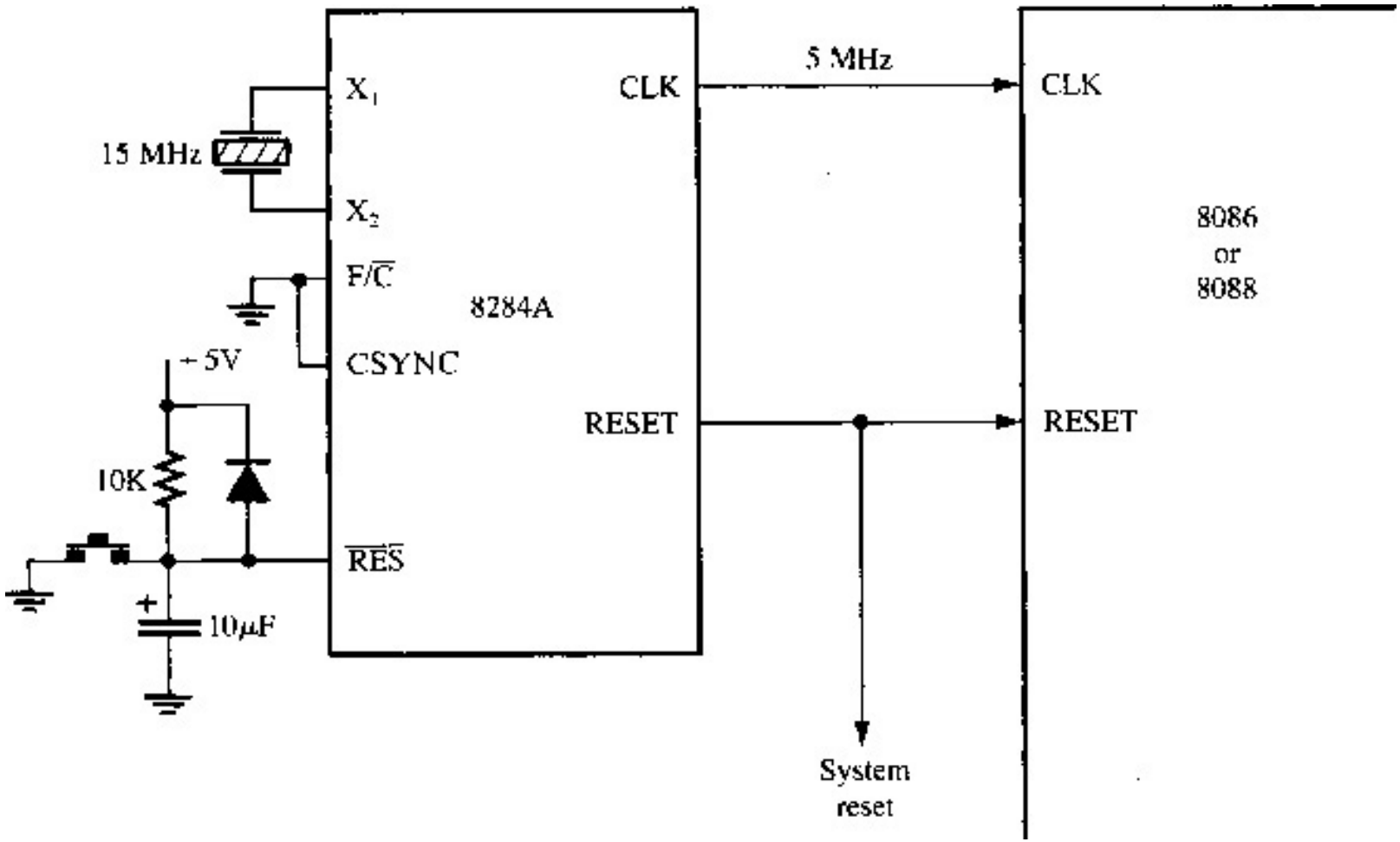
Figure Minimum mode 8088 system.



Maximum Mode Operation

- Differs from minimum mode in that some control signals must be externally generated.
  - requires addition of the 8288 bus controller
- There are not enough pins on the 8086 for bus control during maximum mode
  - new pins and features replaced some of them
- Maximum mode used only when the system contains external coprocessors such as 8087.

Figure The clock generator (8284A) and the 8086 microprocessor illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor.



Basic Bus Operation

- The three buses of 8086 function the same way as any other microprocessor.
- If data are written to memory the processor:
  - outputs the memory address on the address bus
  - outputs the data to be written on the data bus
  - issues a write $\overline{(WR)}$ to memory
  - $\overline{IO}/M$ = 1 for 8086

Figure Simplified 8086 write bus cycle.

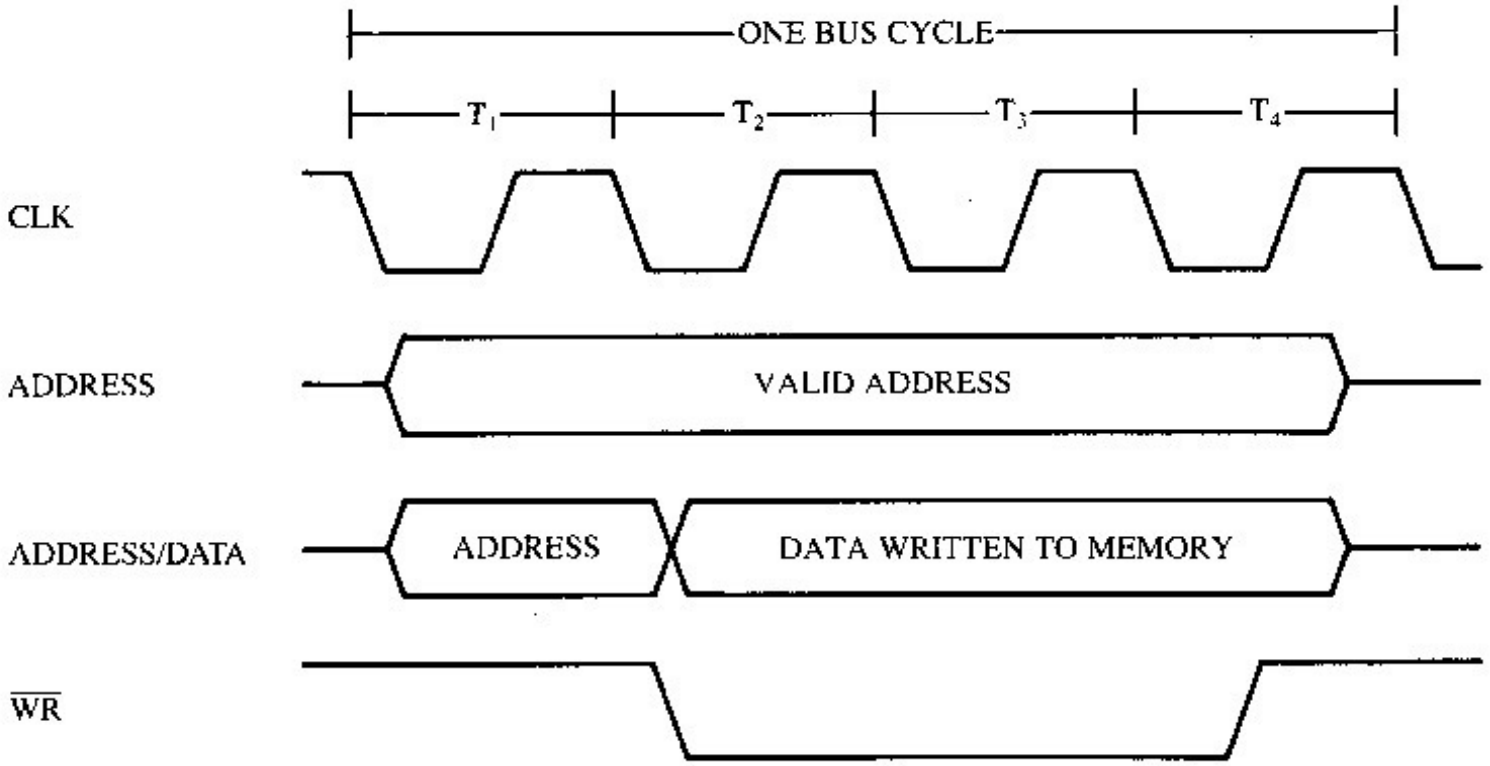
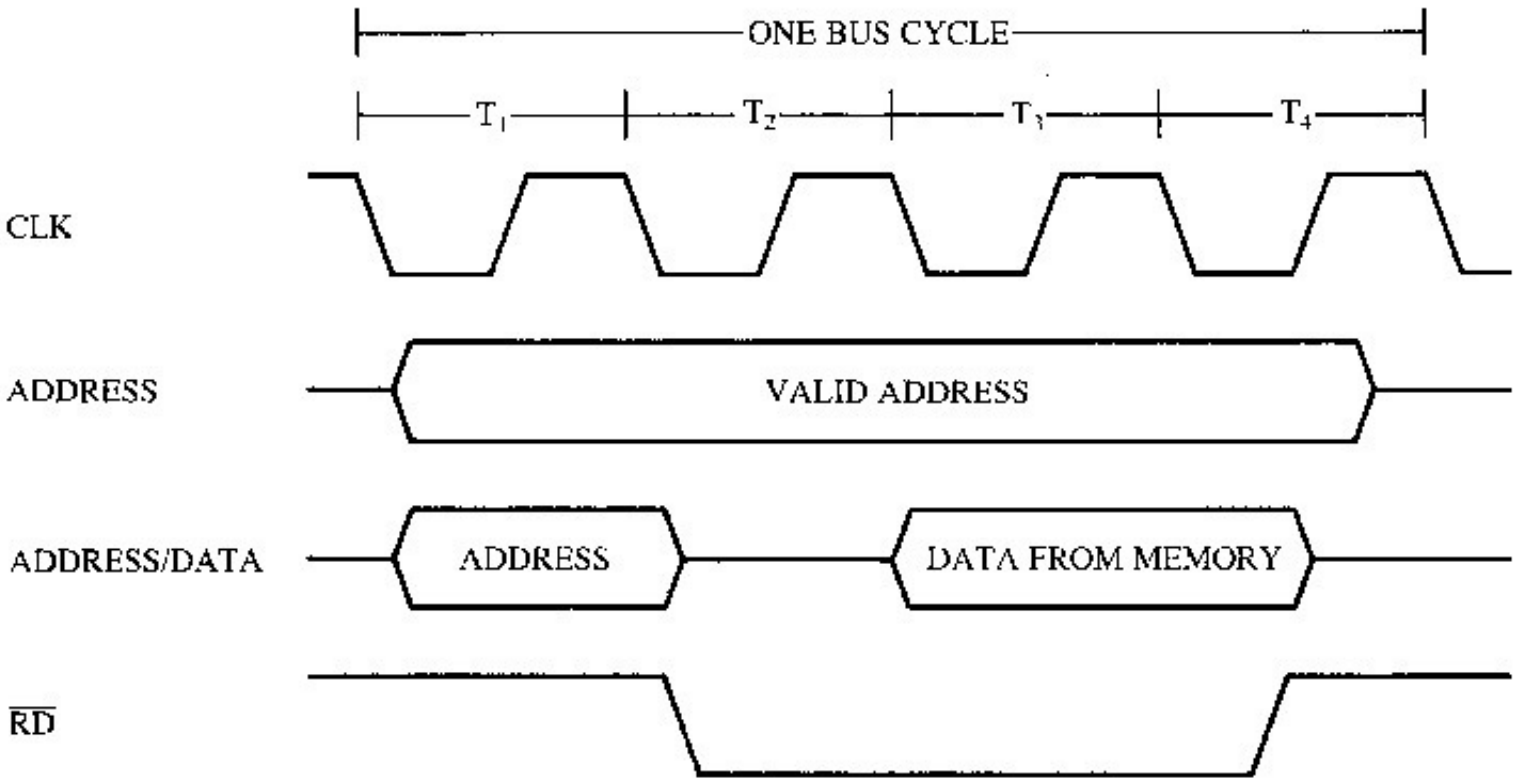


Figure Simplified 8086 read bus cycle.



- The DRAM controller in the chip set for the microprocessor times refresh cycles and inserts refresh cycles into the timing.
- The memory refresh is transparent to the microprocessor, because it really does not control refreshing.
- For Pentium II, III, and P4, DRAM control is built in the chip set provided by Intel or AMD.
- In the future, even the chip set will undoubtedly be built into the microprocessor.