

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74LS76A

Dual J-K Flip-Flops (with Preset and Clear)

REJ03D0417-0300

Rev.3.00

Jul.22.2005

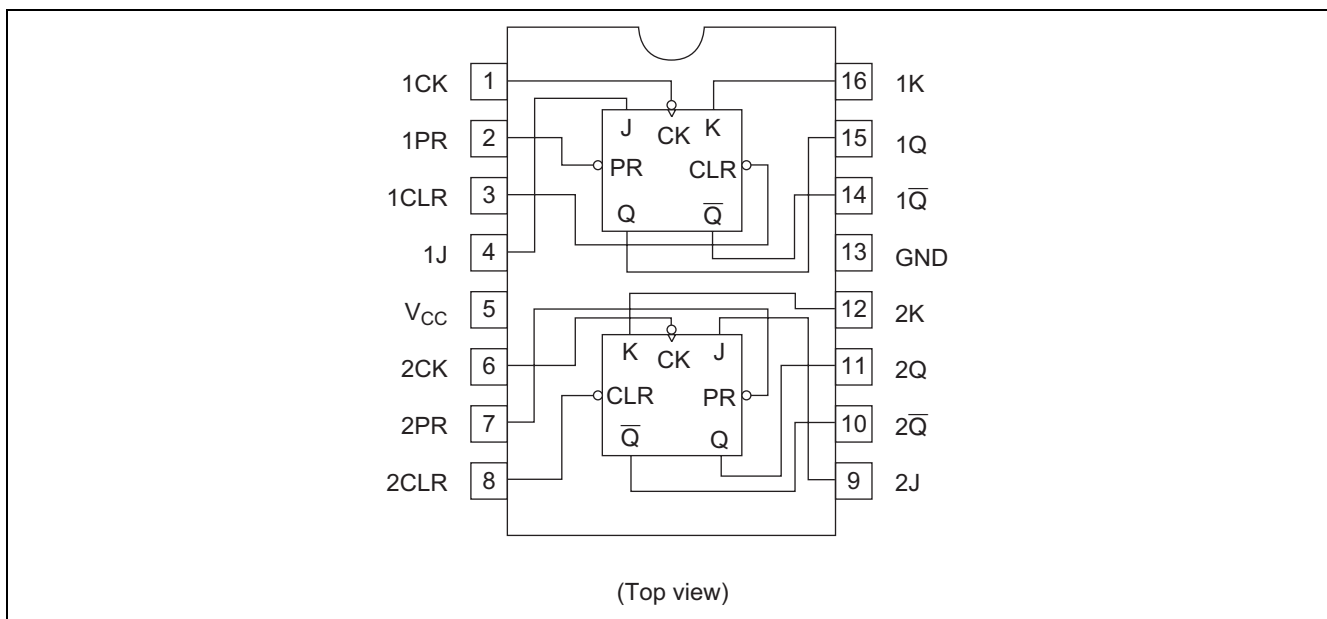
## Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS76AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS76ARPEL	SOP-16 pin(JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL(2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

## Pin Arrangement



## Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

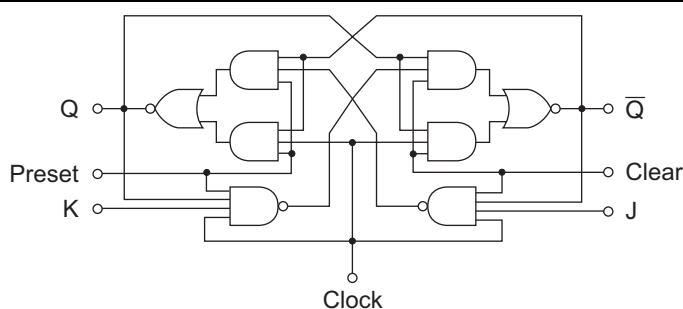
$Q_0$ ; level of Q before the indicated steady-state input conditions were established.

$\bar{Q}_0$ ; complement of  $\bar{Q}_0$  or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

\* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## Block Diagram (1/2)



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	μA
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C
Clock frequency	$f_{clock}$	0	—	30	MHz
Pulse width	Clock High	$t_w$	20	—	ns
	Clear Preset Low	$t_w$	25	—	
Setup time	"H" Data	$t_{su}$	20↓	—	ns
	"L" Data	$t_{su}$	20↓	—	
Hold time	$t_h$	0↓	—	—	ns

## Electrical Characteristics

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V <sub>IH</sub>	2.0	—	—	V	
		V <sub>IL</sub>	—	—	0.8	V	
Output voltage		V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
		V <sub>OL</sub>	—	—	0.5	V	I <sub>OL</sub> = 8 mA
			—	—	0.4		V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 4 mA
Input current	J, K	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	Clear		—	—	60		
	Preset		—	—	60		
	Clock		—	—	80		
	J, K	I <sub>IL</sub> **	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	Clear		—	—	-0.8		
	Preset		—	—	-0.8		
	Clock		—	—	-0.8		
	J, K	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
	Clear		—	—	0.3		
	Preset		—	—	0.3		
	Clock		—	—	0.4		
Short-circuit output current		I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current***		I <sub>CC</sub>	—	4	6	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage		V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C\*\* I<sub>IL</sub> should not be measured when preset and clear inputs are low at same time.\*\*\* With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn.

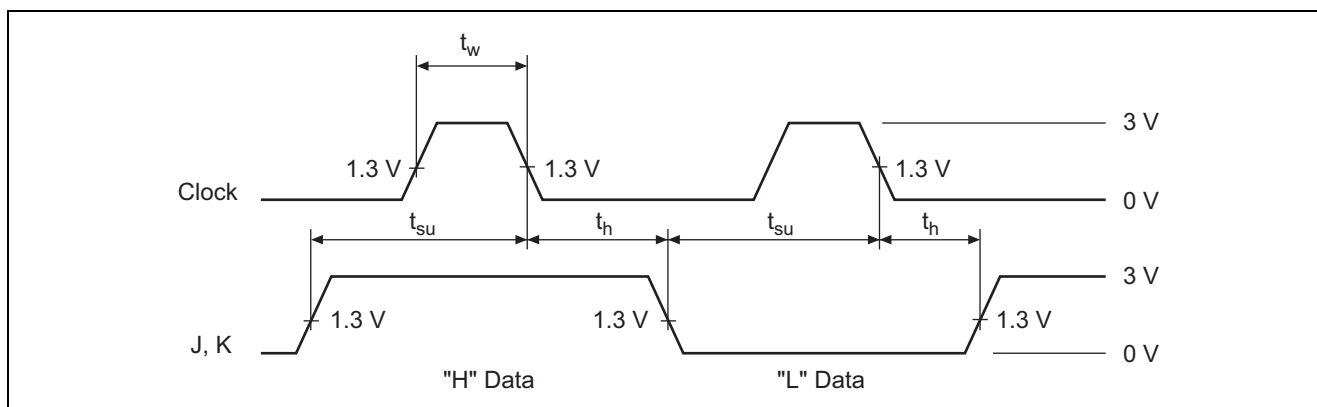
At the time of measurement, the clock input is grounded.

## Switching Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>			30	45		MHz	
Propagation delay time	t <sub>PLH</sub>	Clear Preset Clock	Q, $\bar{Q}$	—	15	20	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
	t <sub>PHL</sub>			—	15	20	ns	

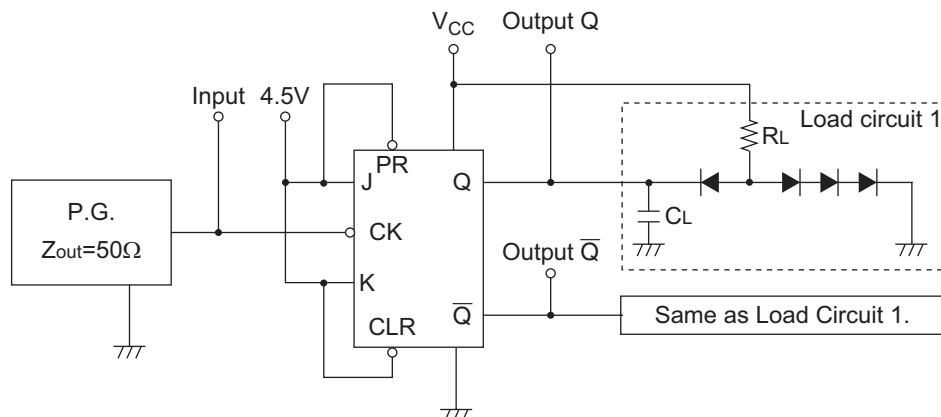
## Timing Definition



## Testing Method

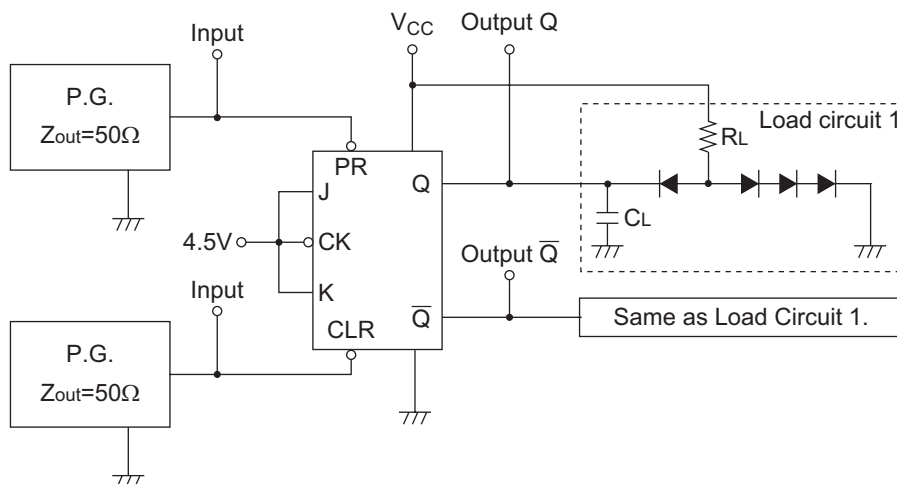
### Test Circuit

1.  $f_{\max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Clock  $\rightarrow$  Q,  $\bar{Q}$ )



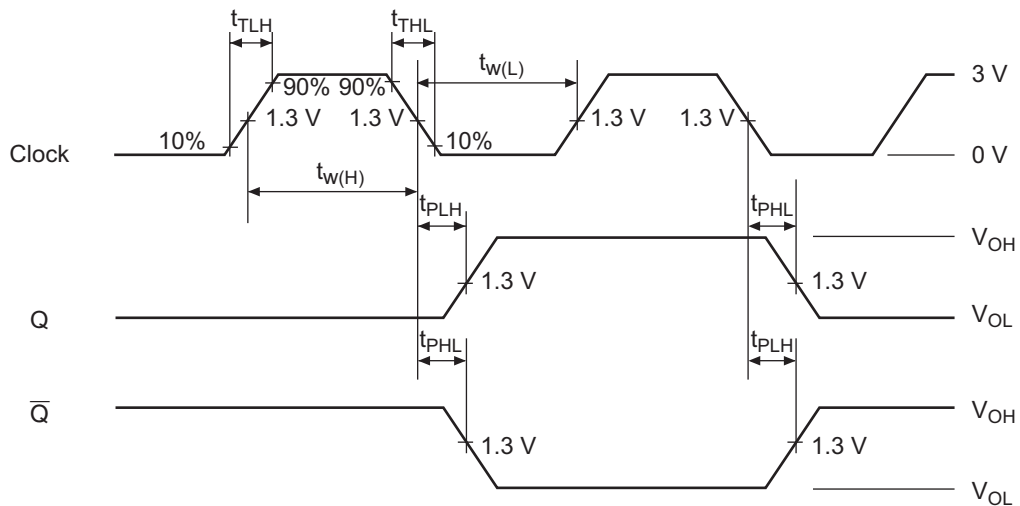
- Notes:
1. Test is put into the each flip-flop.
  2.  $C_L$  includes probe and jig capacitance.
  3. All diodes are 1S2074(H).

2.  $t_{PHL}$ ,  $t_{PLH}$  (Clear, Preset  $\rightarrow$  Q,  $\bar{Q}$ )



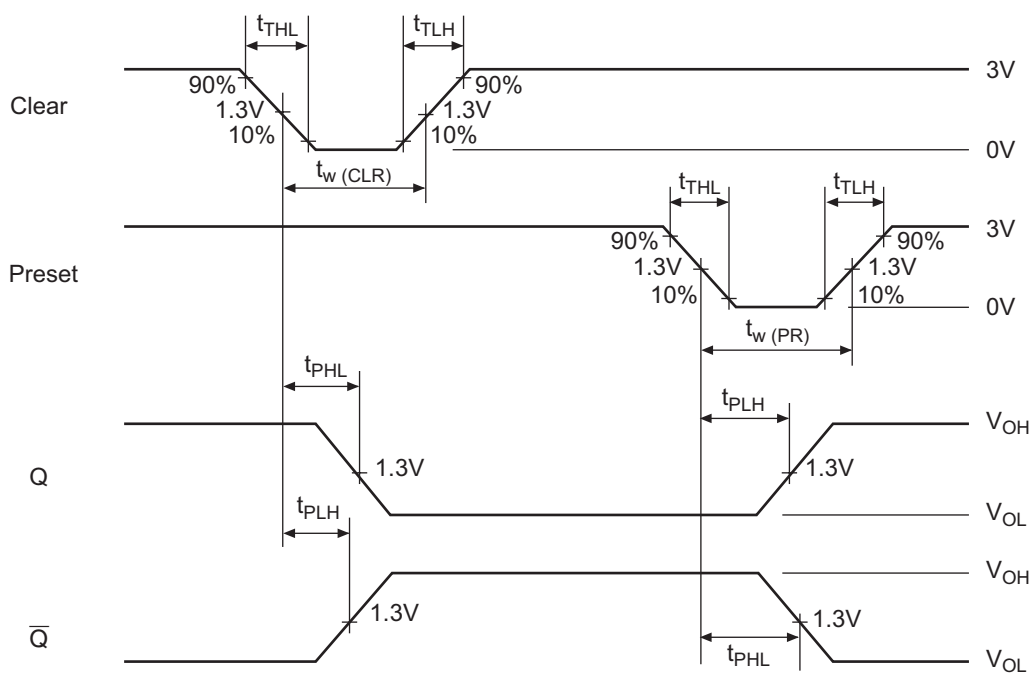
- Notes:
1. Test is put into the each flip-flop.
  2.  $C_L$  includes probe and jig capacitance.
  3. All diodes are 1S2074(H).

## Waveforms 1



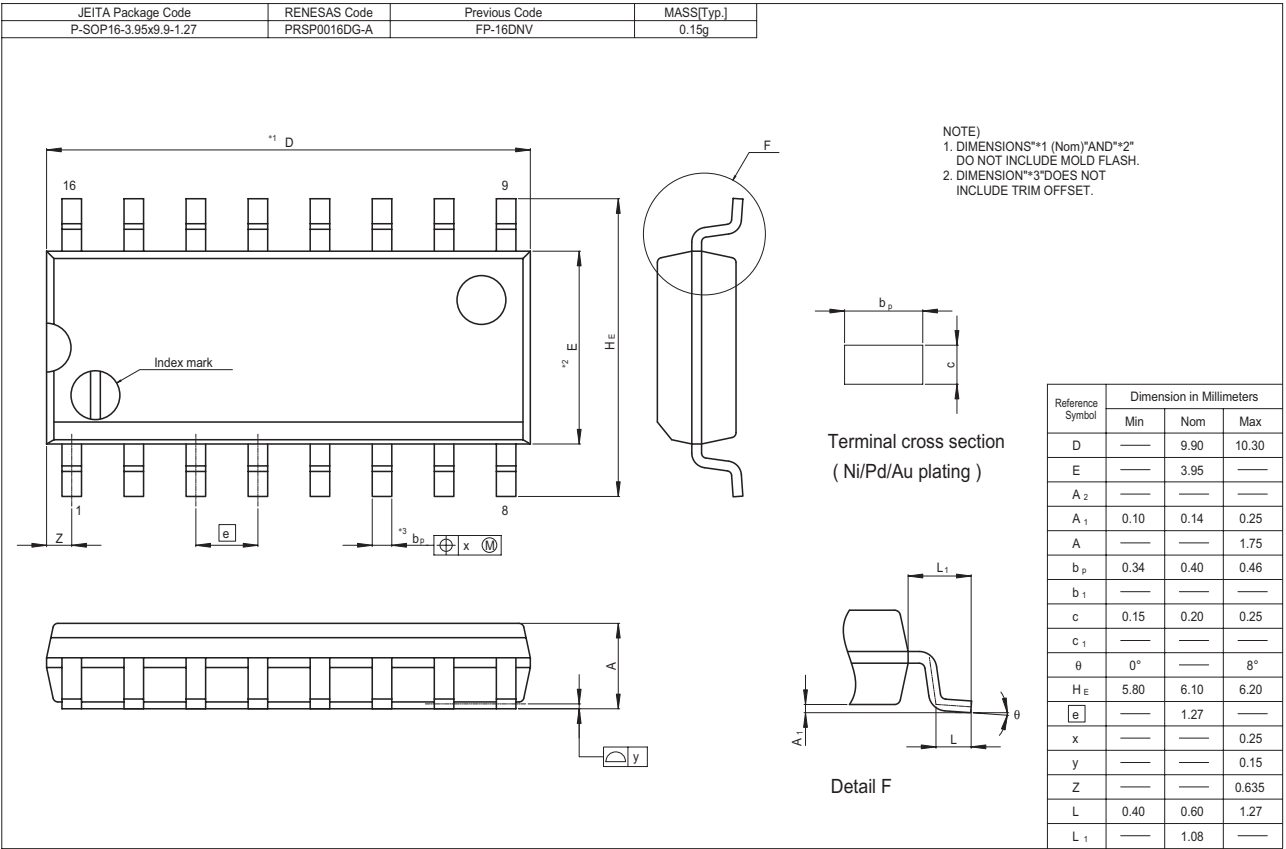
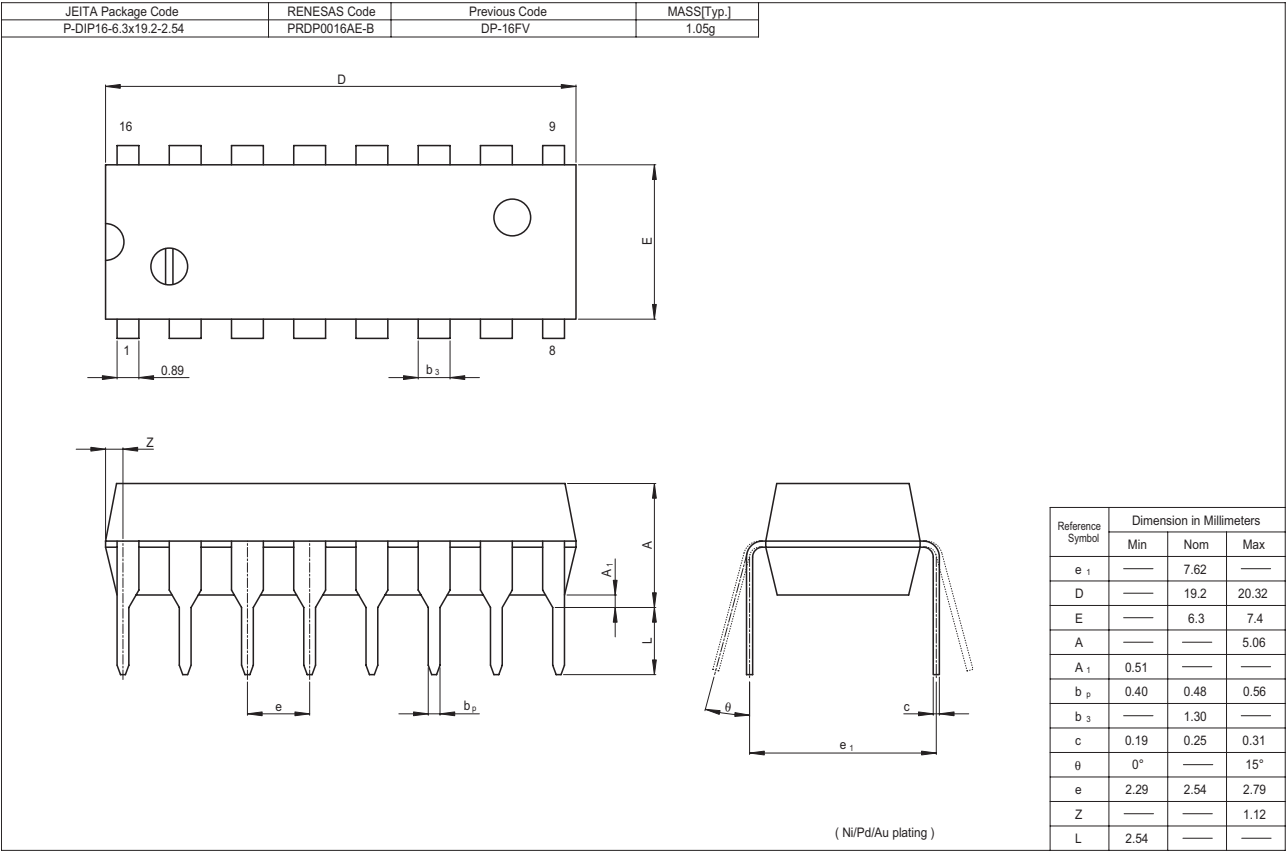
Note: Clock input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, duty cycle = 50% and for  $f_{max}$ ,  $t_{TLH} = t_{THL} \leq 2.5$  ns

## Waveforms 2



Note: Clear and preset input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz,

Package Dimensions





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