BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
K. K. BIRLA Goa Campus
Second Semester 2012-2013
IS F242 Computer Organization
Lab – 4, 14th March 2013

Design and implement the following using verilog HDL in **Xilinx software** with the following specifications.

D_FF(d_1b, q_1b, Write_1b, clk);
Mux4to1(Din0_1b,D in1_1b, Din2_1b, Din3_1b, Dout_1b,Addr_2b);
Mux2to1(Dout_3b, Zero_3b,Qout_3b,Read_1b);
Decoder2to4(Addr_2b,Loc_4b);
Memory(Din_3b,Addr_2b,WE_1b,Read_1b,Qout_3b,clk);
Testbench;