Digital Electronics and Microprocessors

Class 17

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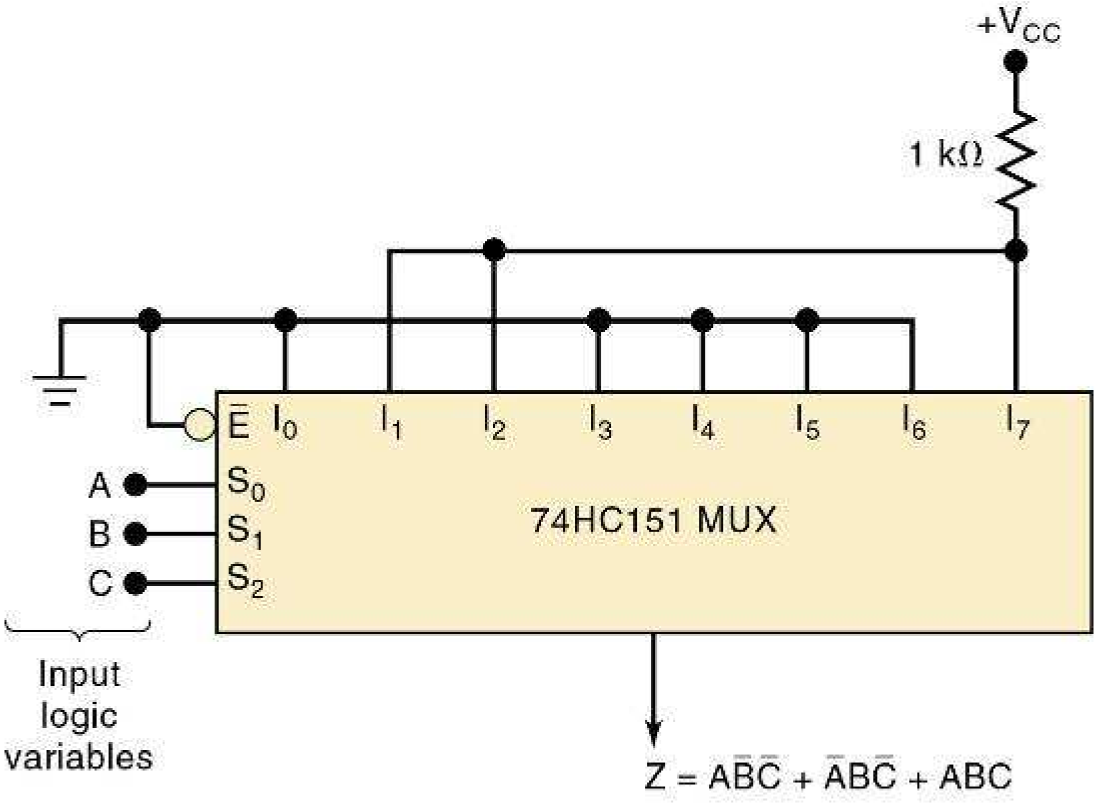
MSI logic circuits(Chapter 9 of T1)

- Digital systems obtain data and information continuously operated on in some manner:
  - *Decoding/encoding.*
  - *Multiplexing/demultiplexing,.*
  - *Comparison; Code conversion;*
- These and other operations have been facilitated by the availability of numerous ICs in the MSI (medium-scale-integration) category.

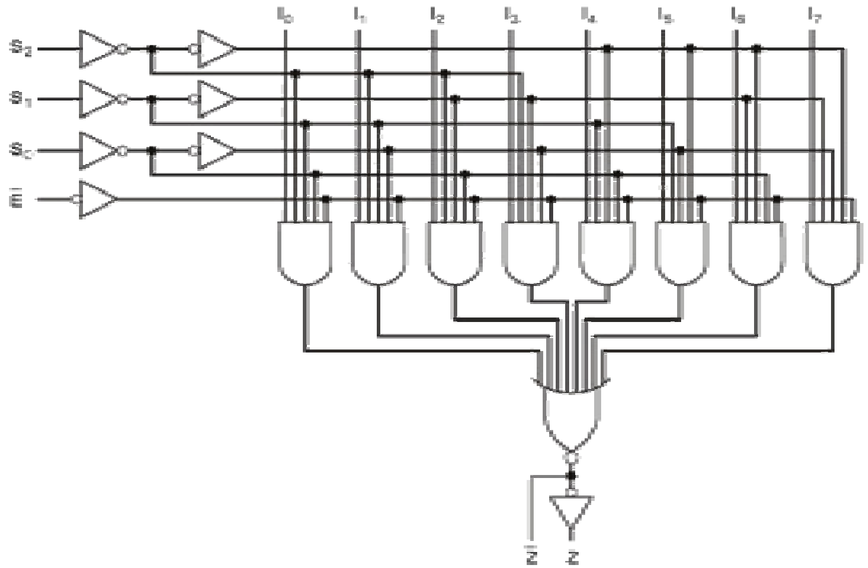
Multiplexer Applications

Multiplexer used to implement a logic function described by the truth table.



C	B	A	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

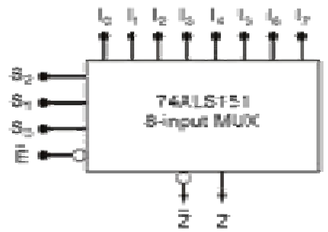
Multiplexers (Data Selectors)



(a)

Inputs				Outputs	
$\bar{E}$	S_2	S_1	S_0	$\bar{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\bar{I}_0$	I_0
L	L	L	H	$\bar{I}_1$	I_1
L	L	H	L	$\bar{I}_2$	I_2
L	L	H	H	$\bar{I}_3$	I_3
L	H	L	L	$\bar{I}_4$	I_4
L	H	L	H	$\bar{I}_5$	I_5
L	H	H	L	$\bar{I}_6$	I_6
L	H	H	H	$\bar{I}_7$	I_7

(b)

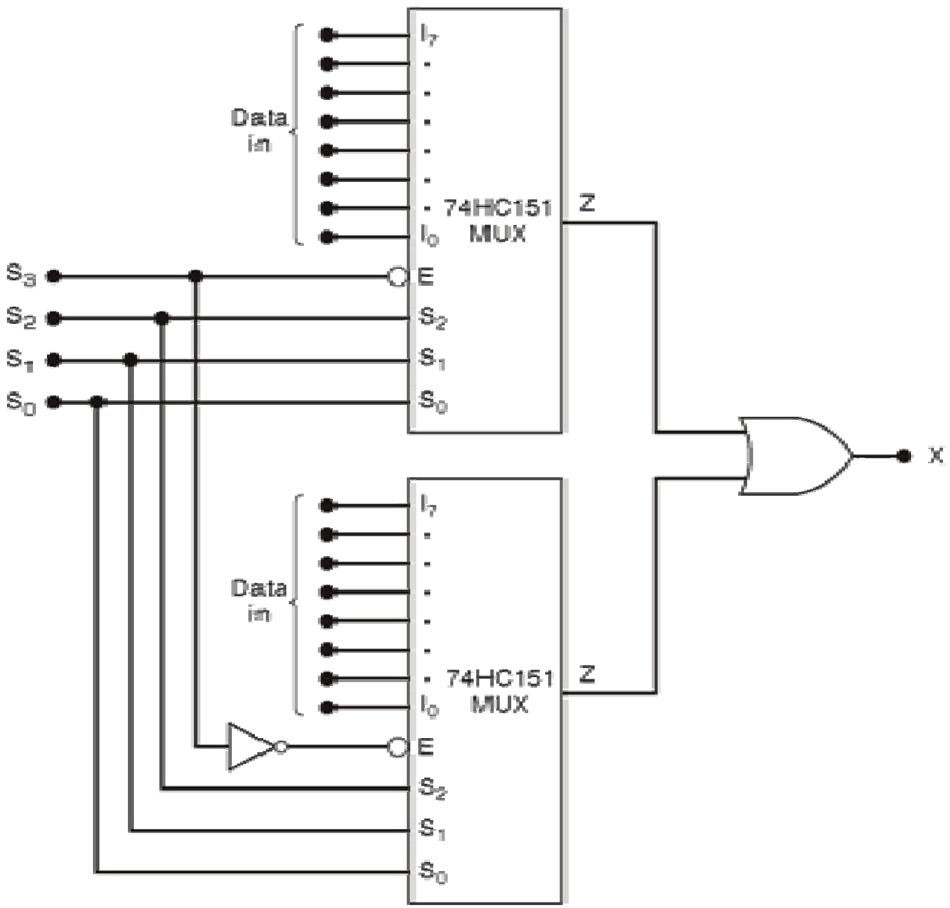


(c)

(a) Logic diagram for the 74ALS151 multiplexer; (b) truth table; (c) logic symbol

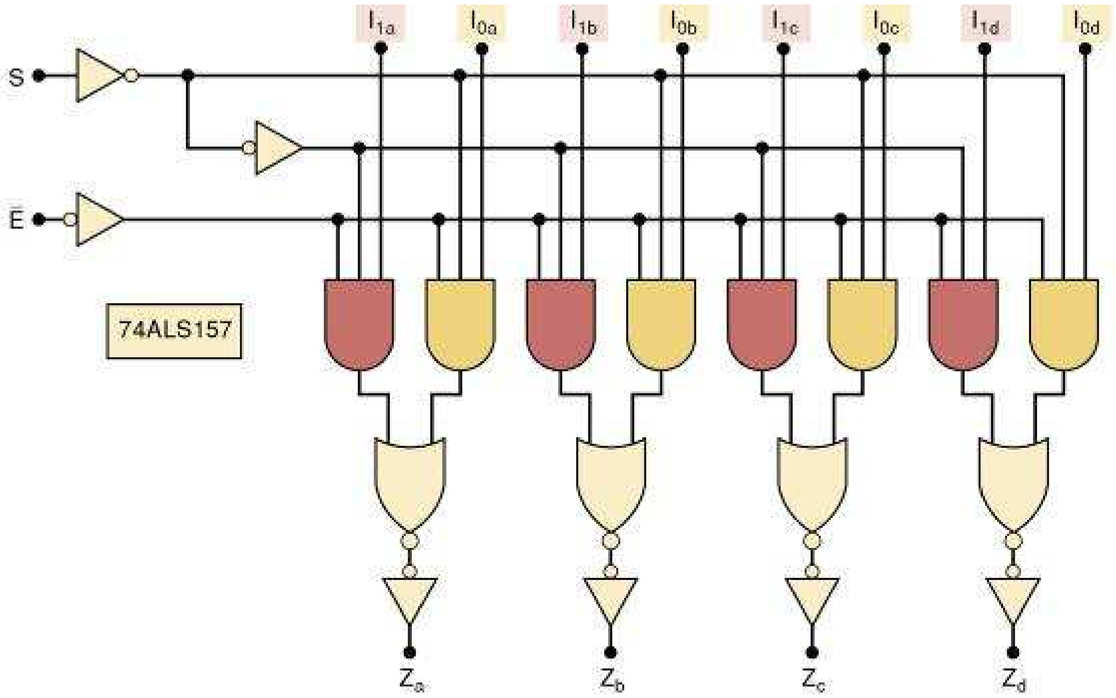
Multiplexers (Data Selectors)

two 74HC151s combined to form a 16-input multiplexer.

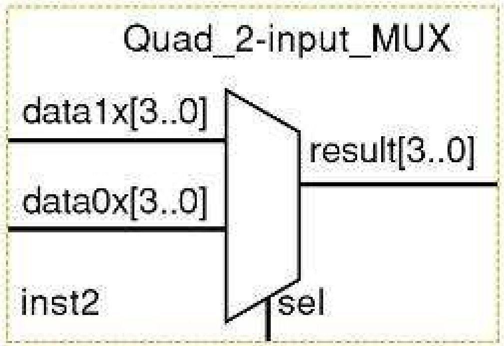


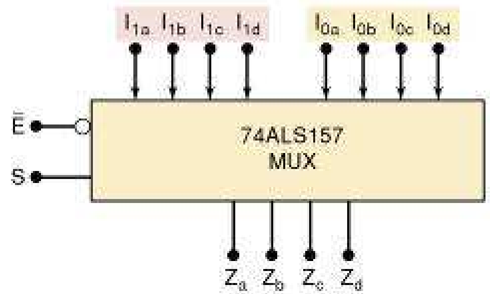
Multiplexers (Data Selectors)

The 74ALS157 contains four two-input multiplexers



$\bar{E}$	S	Z_a	Z_b	Z_c	Z_d
H	X	L	L	L	L
L	L	I_{0a}	I_{0b}	I_{0c}	I_{0d}
L	H	I_{1a}	I_{1b}	I_{1c}	I_{1d}

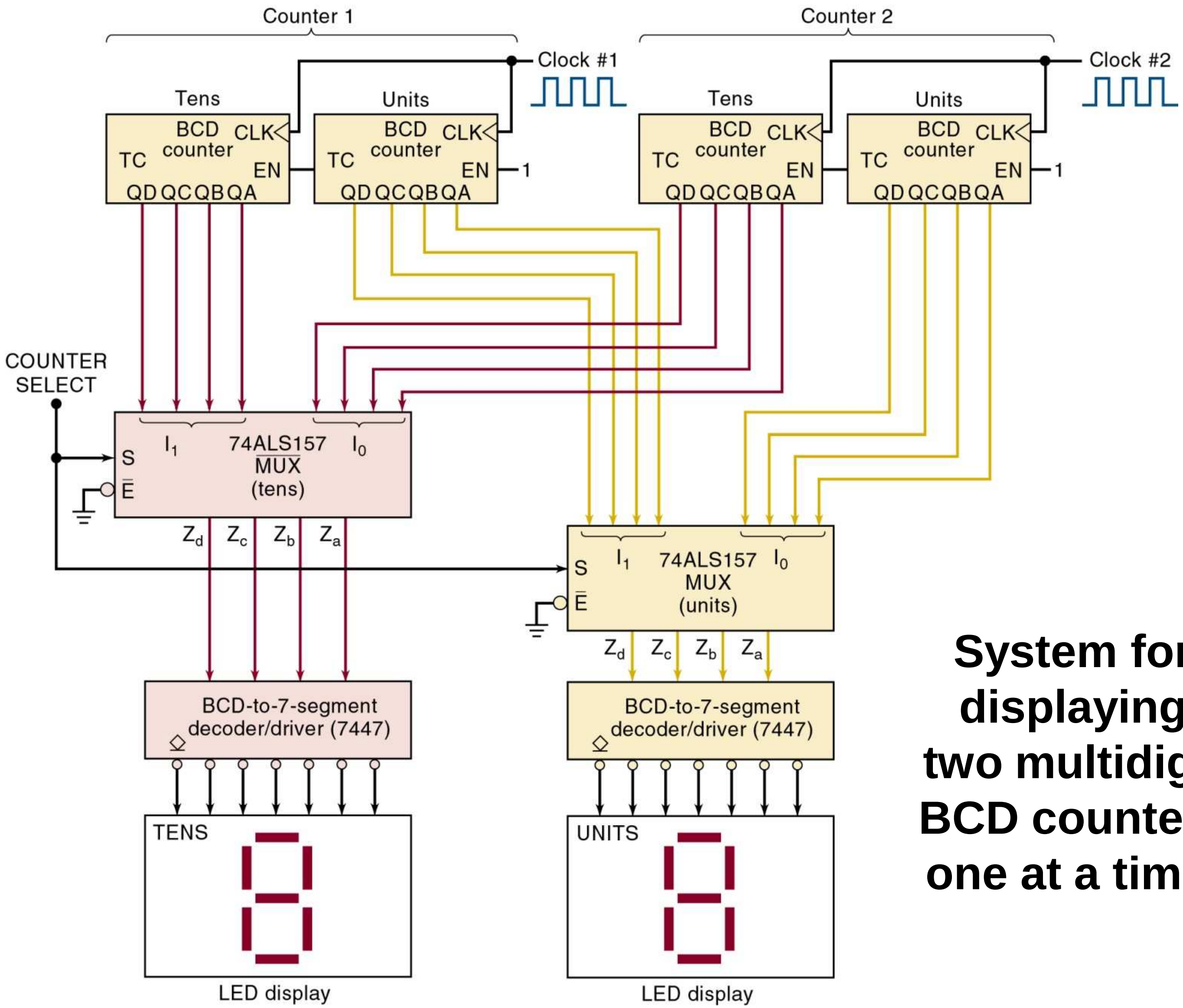




Multiplexer Applications

- Multiplexer circuits find numerous and varied applications in digital systems of all types.
  - Data selection/routing, parallel-to-serial conversion.
  - Operation sequencing.
  - Waveform/logic-function generation.

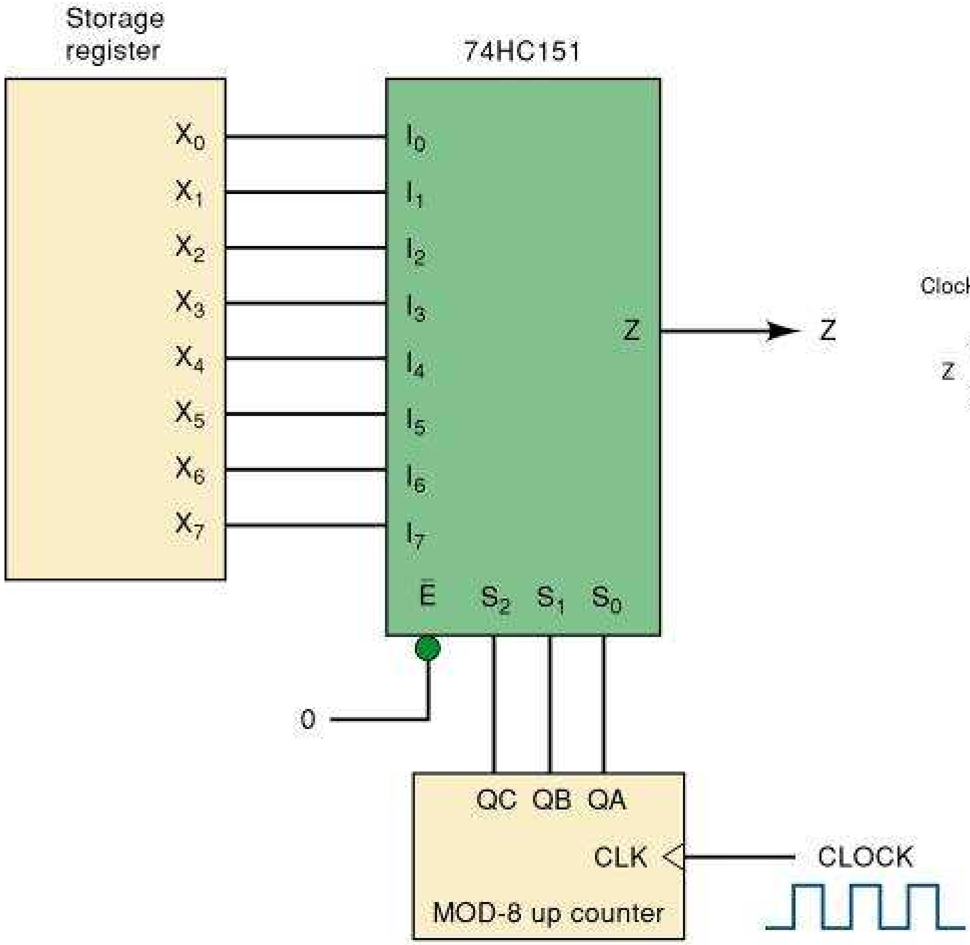
Multiplexer Applications

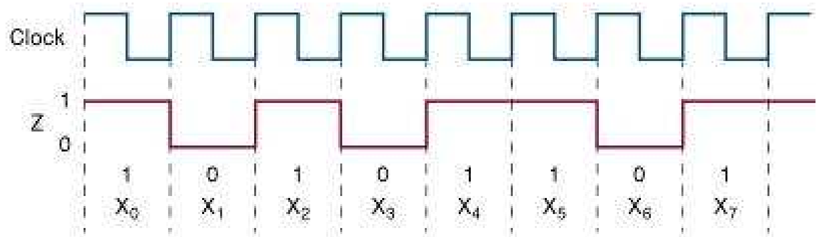


System for displaying two multidigit BCD counters one at a time.

Multiplexer Applications

Parallel-to-serial converter.



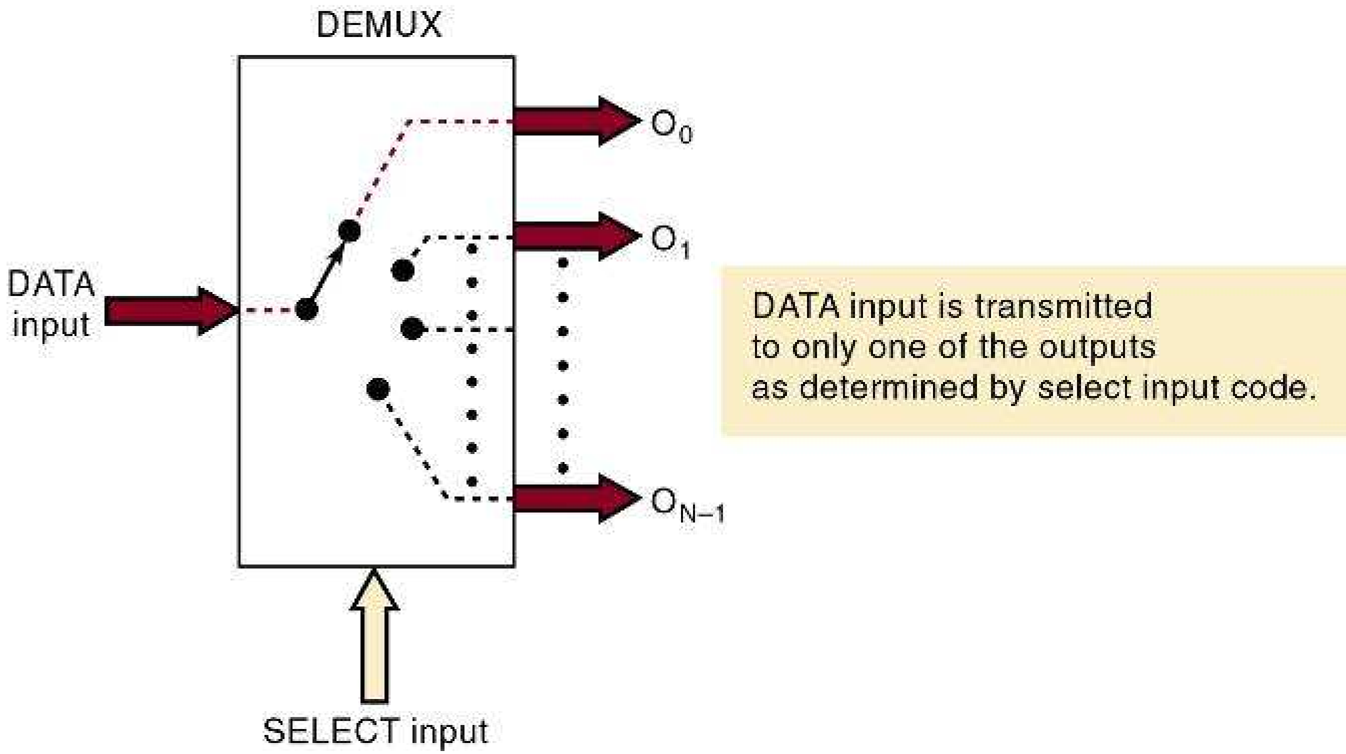


Waveforms for X7X6X5X4X3X2X1X0

10110101

Demultiplexers (Data Distributors)

- A **demultiplexer (DEMUX)** takes a single input and distributes it over several outputs.
  - The select input code determines to which output the DATA input will be transmitted.

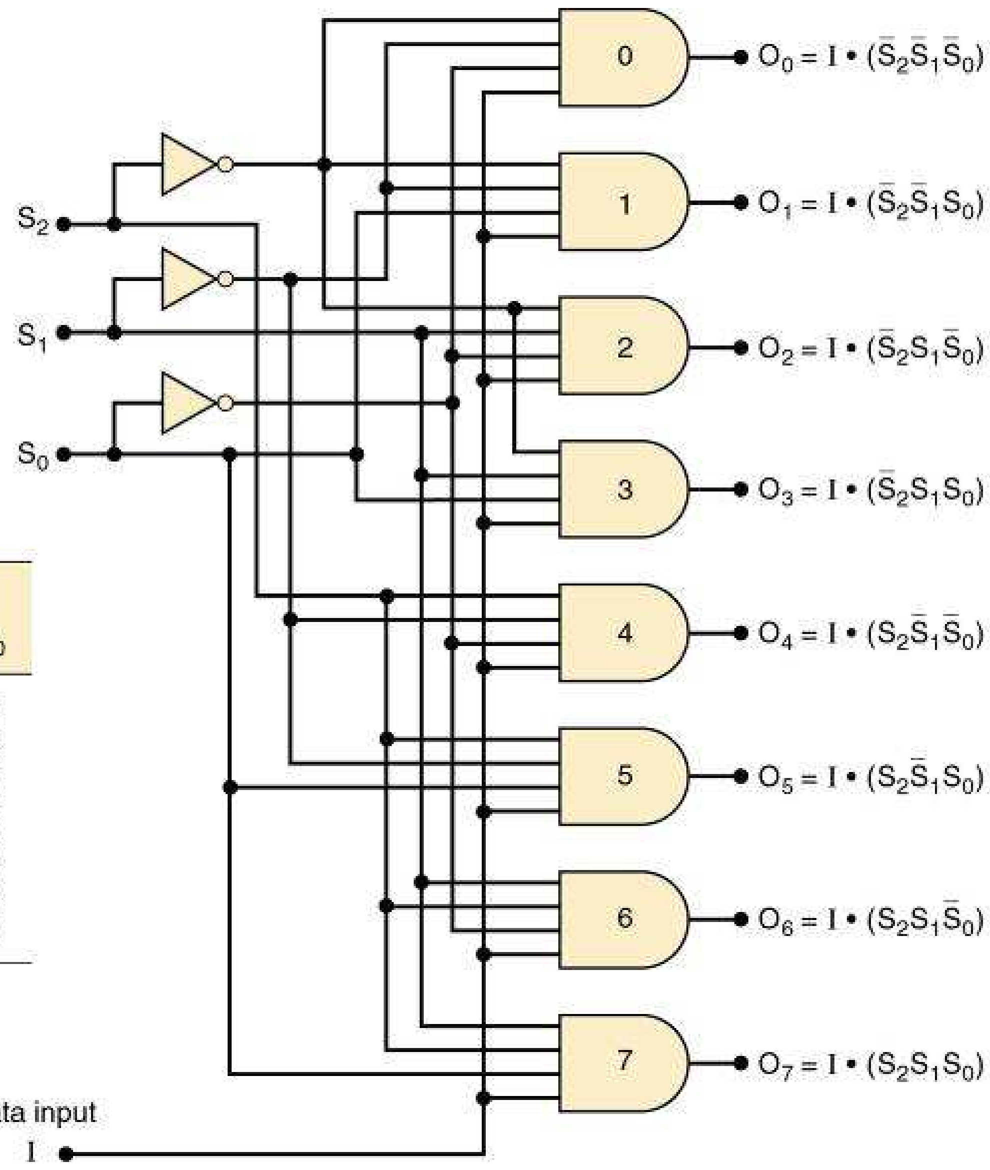


Demultiplexers (Data Distributors)

A 1 line to 8 line demultiplexer.

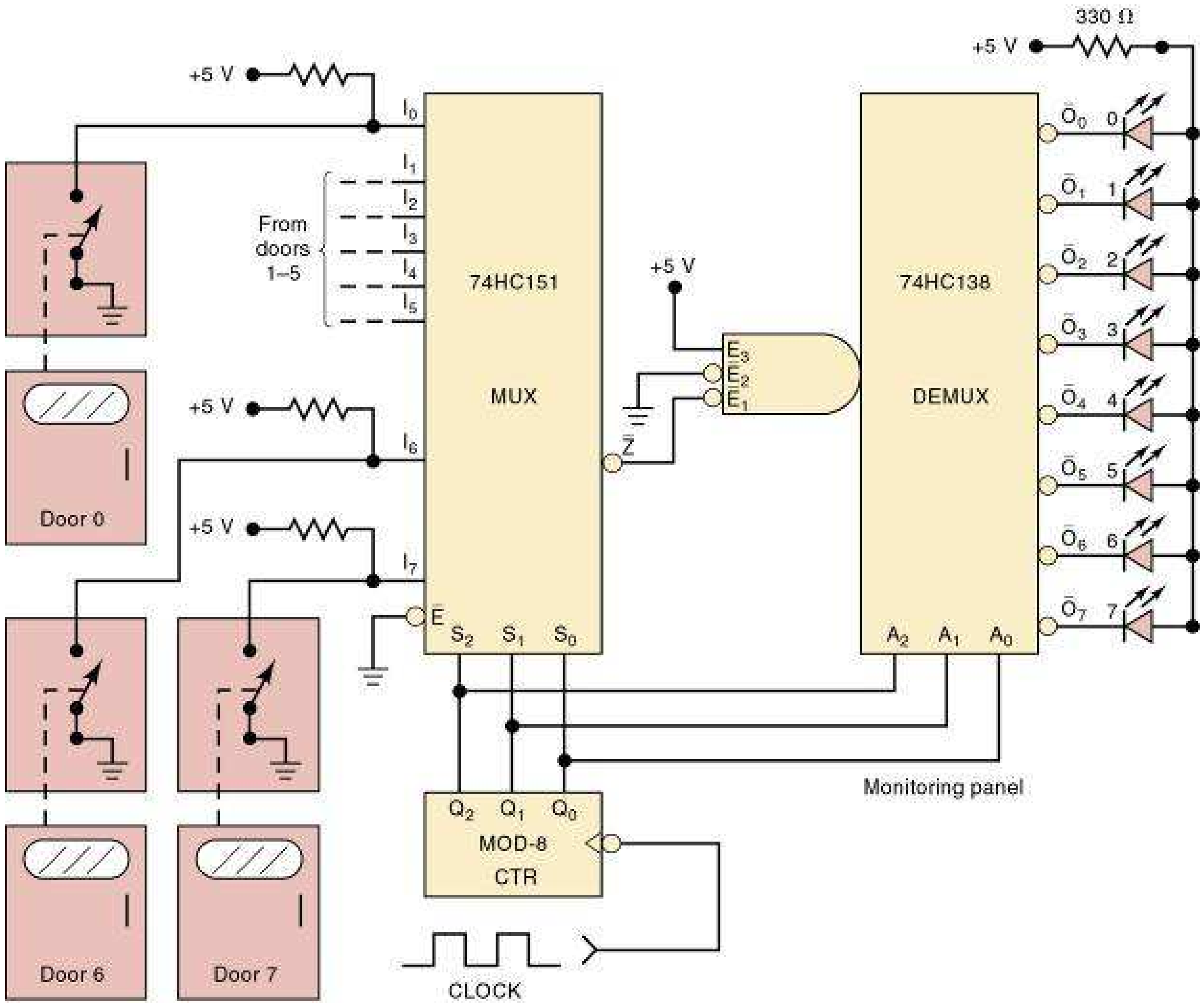
Select Code			Outputs							
S_2	S_1	S_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	1	0	0	0	0	0	0	I	0	0
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	I	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0

Note: I is the data input



Demultiplexers (Data Distributors)

Security monitoring system using the 74ALS138.



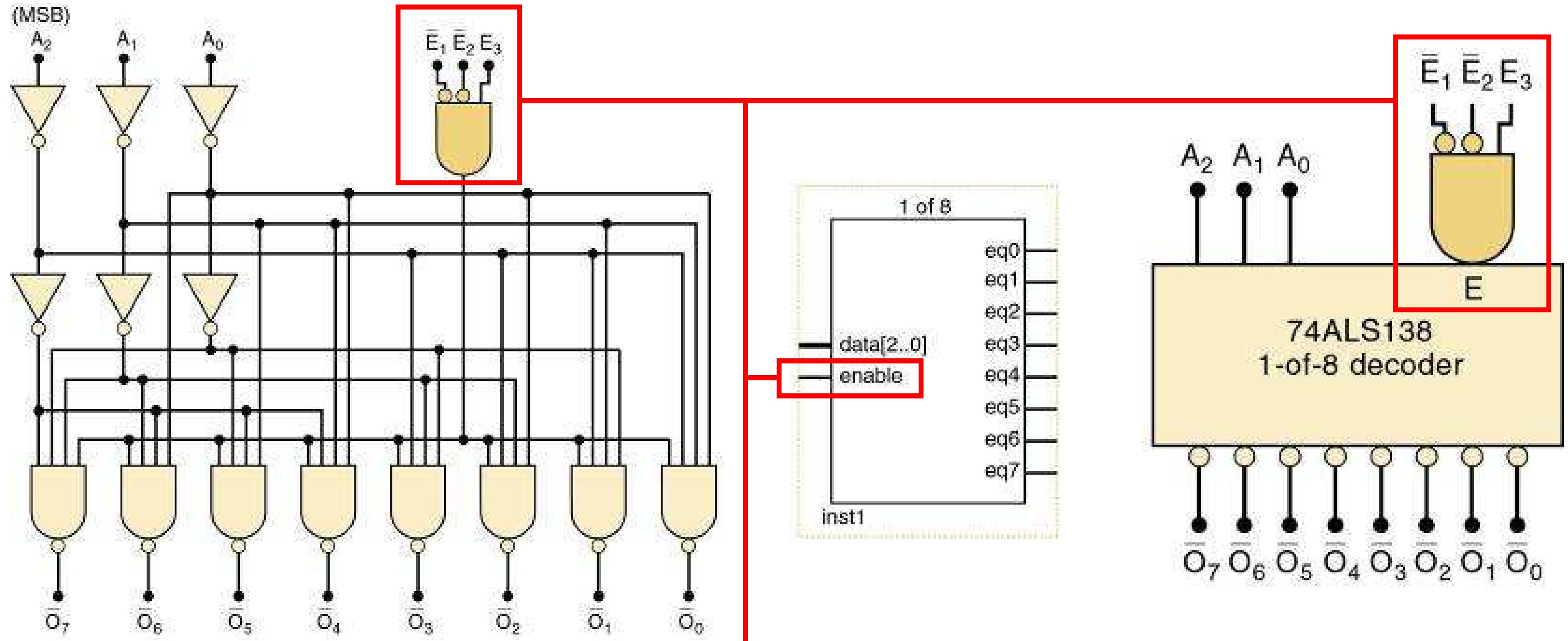
The system shown can handle eight doors, but can be expanded to any number.

The door switches are data inputs to the MUX.

They produce a HIGH when a door is open and a LOW when it is closed.

Decoders

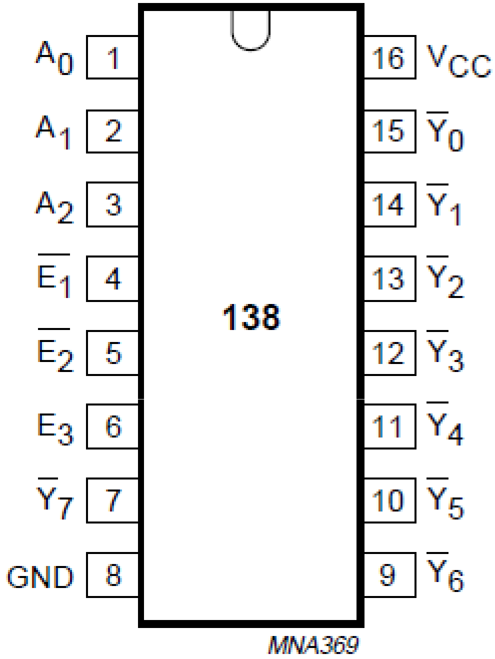
The 74ALS138 decoder.

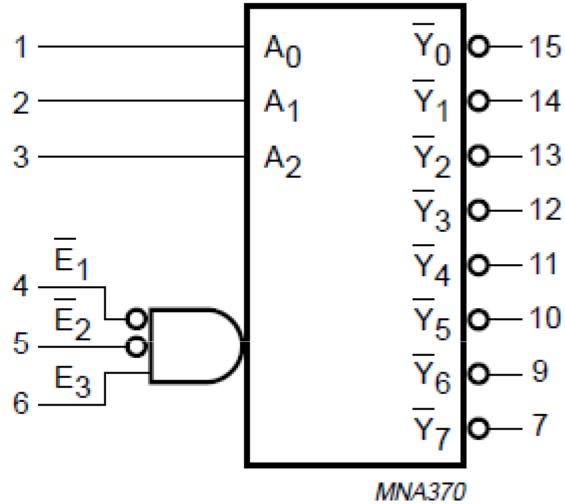


ENABLE inputs

$\bar{E}_1$	$\bar{E}_2$	E_3	Outputs
0	0	1	Respond to input code $A_2A_1A_0$
1	X	X	Disabled – all HIGH
X	1	X	Disabled – all HIGH
X	X	0	Disabled – all HIGH

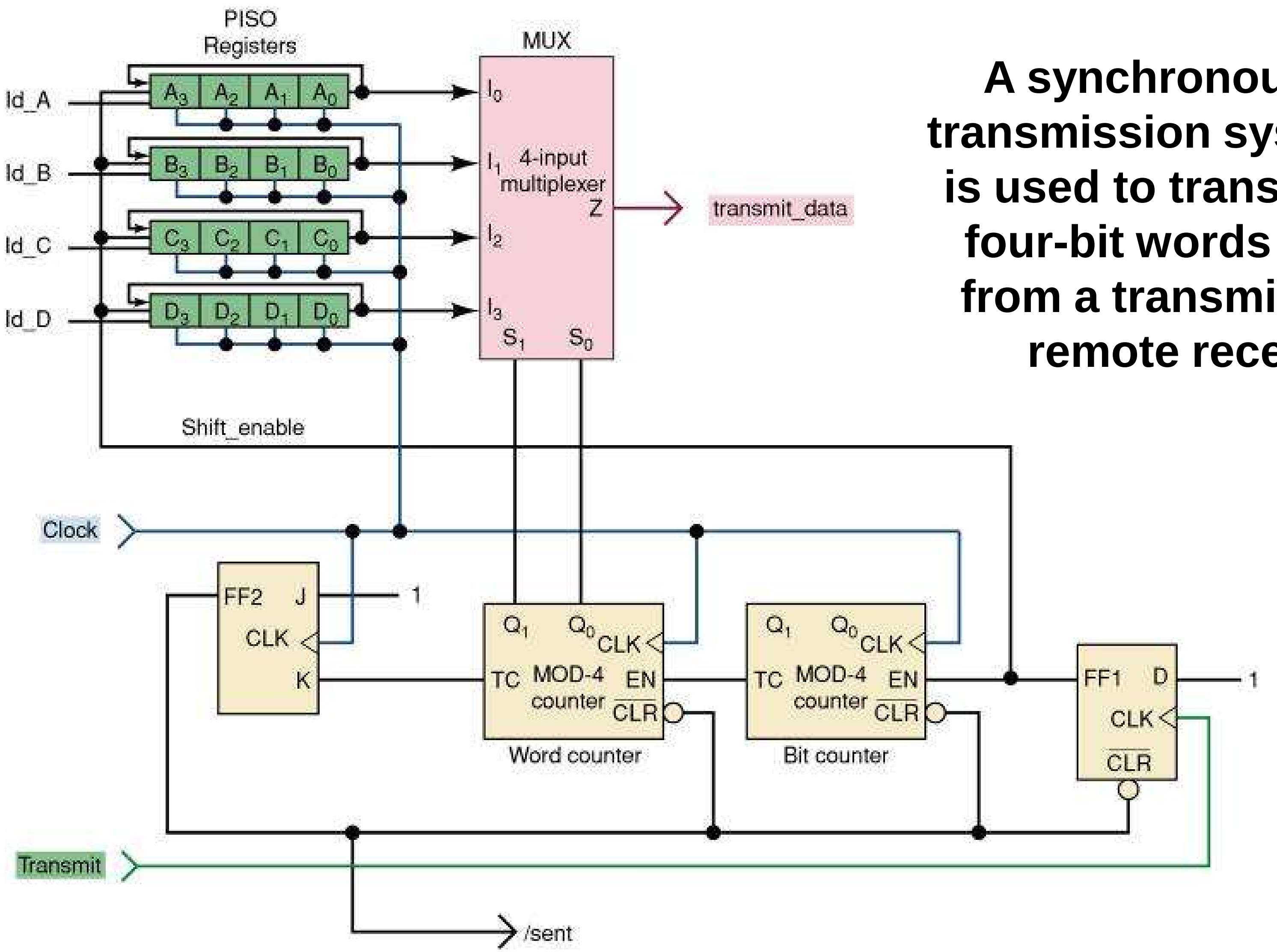
Pin diagram and logic symbol





INPUT						OUTPUT							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

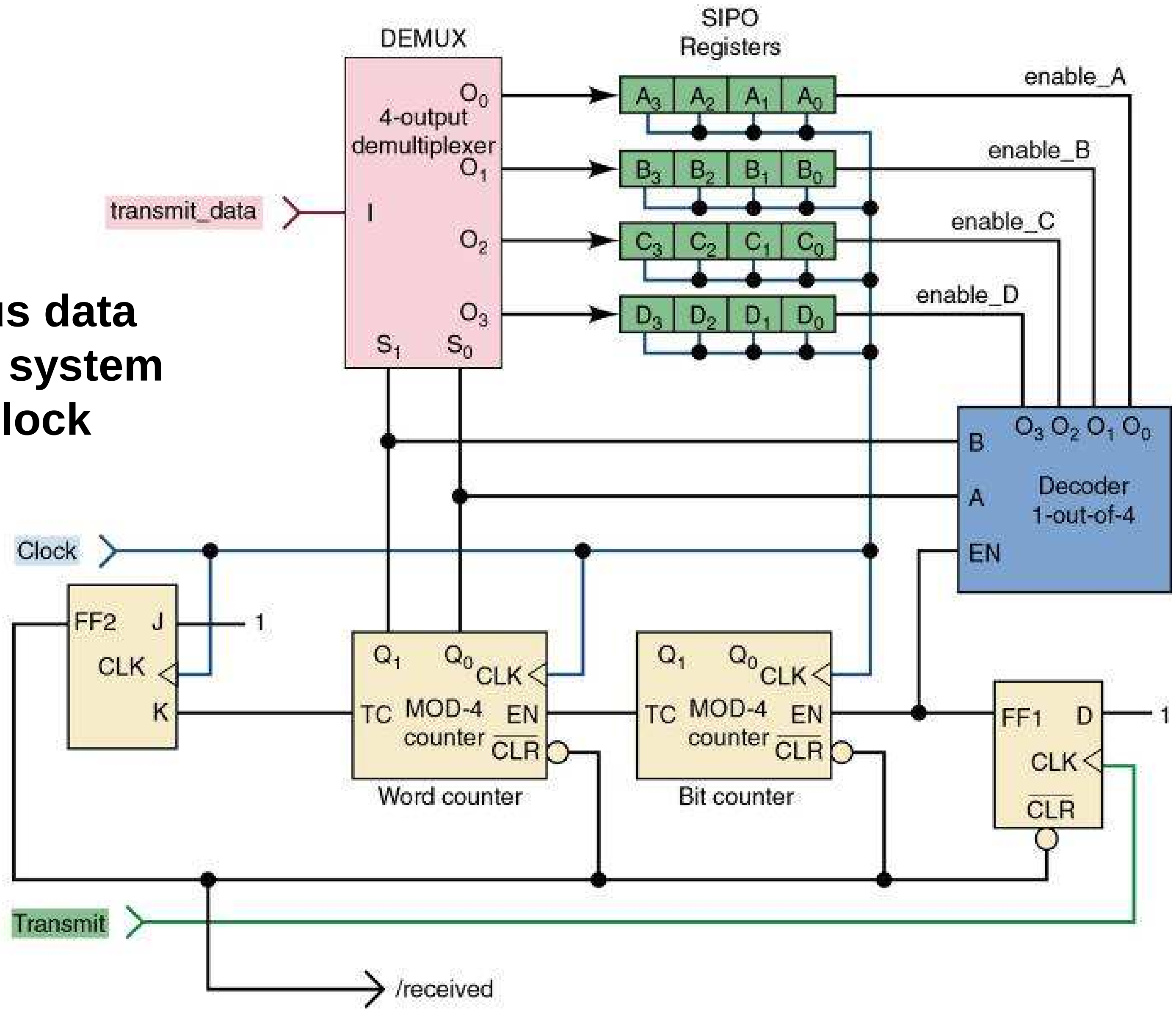
Demultiplexers (Data Distributors)



A synchronous data transmission system that is used to transmit four, four-bit words serially from a transmitter to a remote receiver.

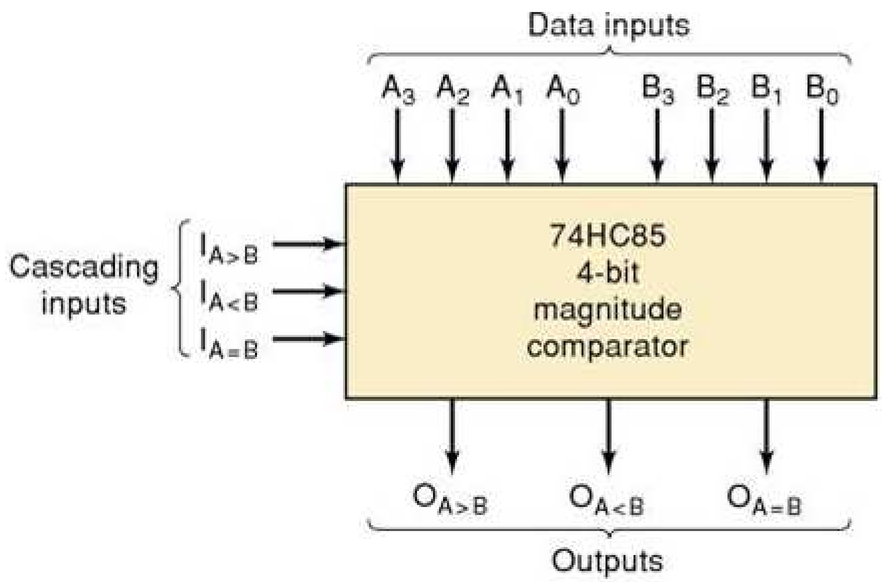
Demultiplexers (Data Distributors)

Synchronous data transmission system receiver block



Magnitude Comparator

- Another useful MSI is a **magnitude comparator**.
  - A combinational logic circuit that compares two input binary quantities and generates outputs to indicate which one has the greater magnitude.

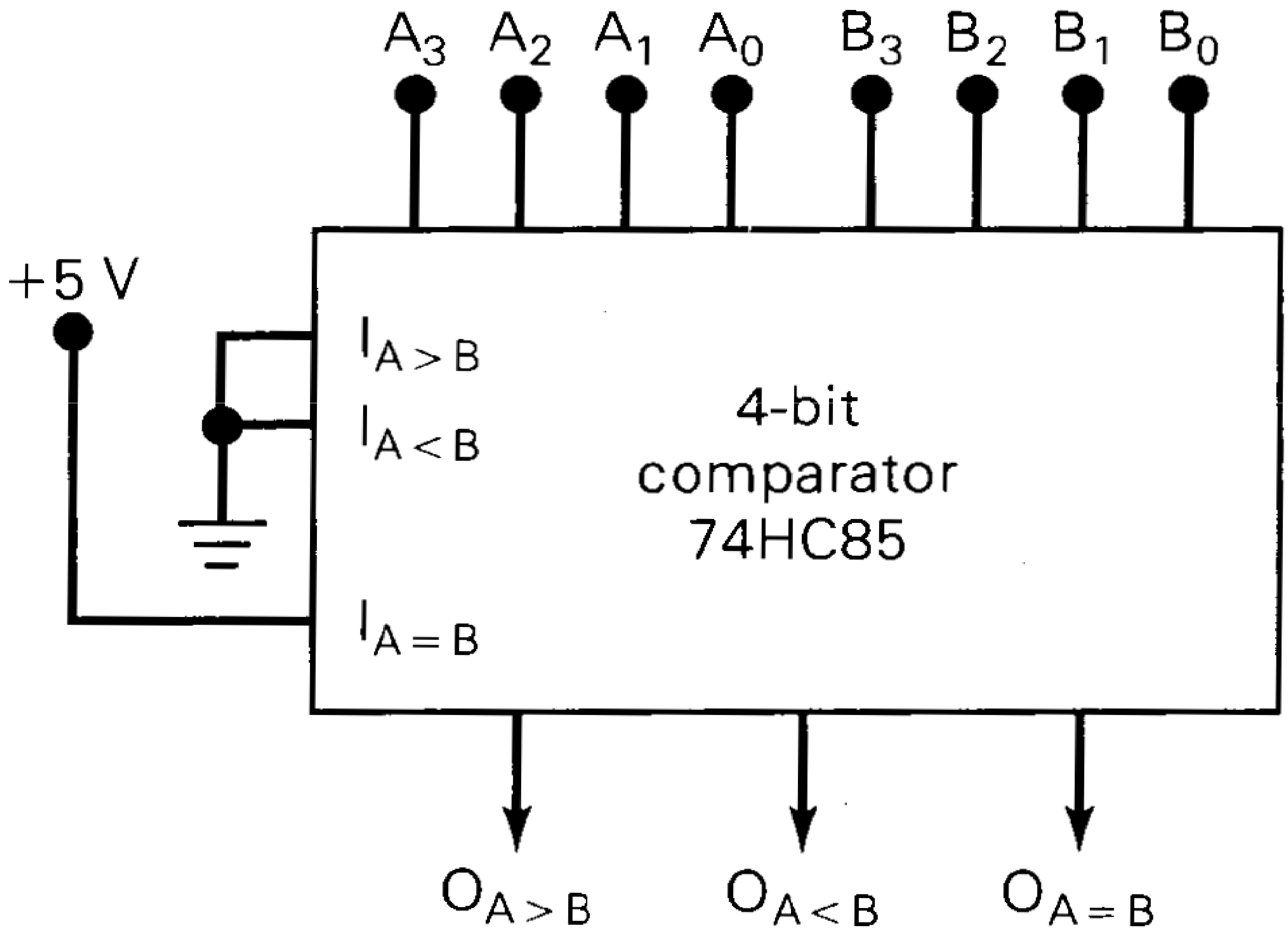


Magnitude Comparator

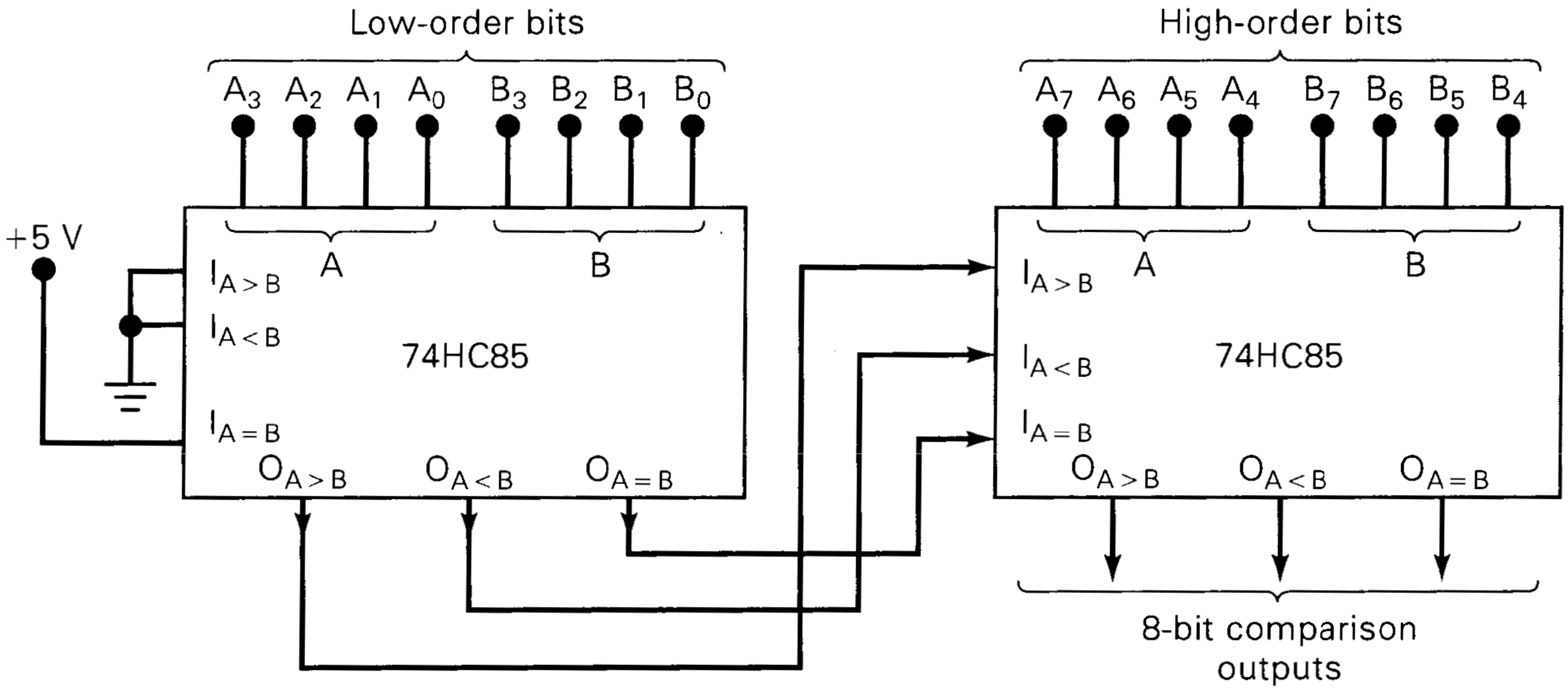
TRUTH TABLE

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L



A3 A2 A1 A0 B3 B2 B1 B0
+5 V
IA>B
IA<B
IA=B
4-bit
comparator
74HC85
OA>B OA<B OA=B



$A_7A_6A_5A_4A_3A_2A_1A_0 = 10101111$; $B_7B_6B_5B_4B_3B_2B_1B_0 = 10110001$

The high-order comparator compares its inputs $A_7A_6A_5A_4 = 1010$ and $B_7B_6B_5B_4 = 1011$ and produces $O_{A<B} = 1$ regardless of what levels are applied to its

Cascaded inputs

Magnitude Comparator

Magnitude comparator used in a digital thermostat.