# Digital Electronics and Microprocessors

Class 11

CHHAYADEVI BHAMARE

# Some important terms

- Modulus of a counter (Divide-by-*N* counter ):-the number of states trough which a counter sequences before repeating.
- Full sequence counter.

Example:- mod 4 (Divide-by-4), mod 8 (Divide-By-8), mod 16(Divide-by-16), mod32(Divide-by-32)

- Truncated sequence counter.

Example:-mod 3 (Divide-by 3)(0,1,2,0,1,2....)

mod 10(Divide-by 10) (0,1,2,3,4,5,6,7,8,9,0,1,2....)

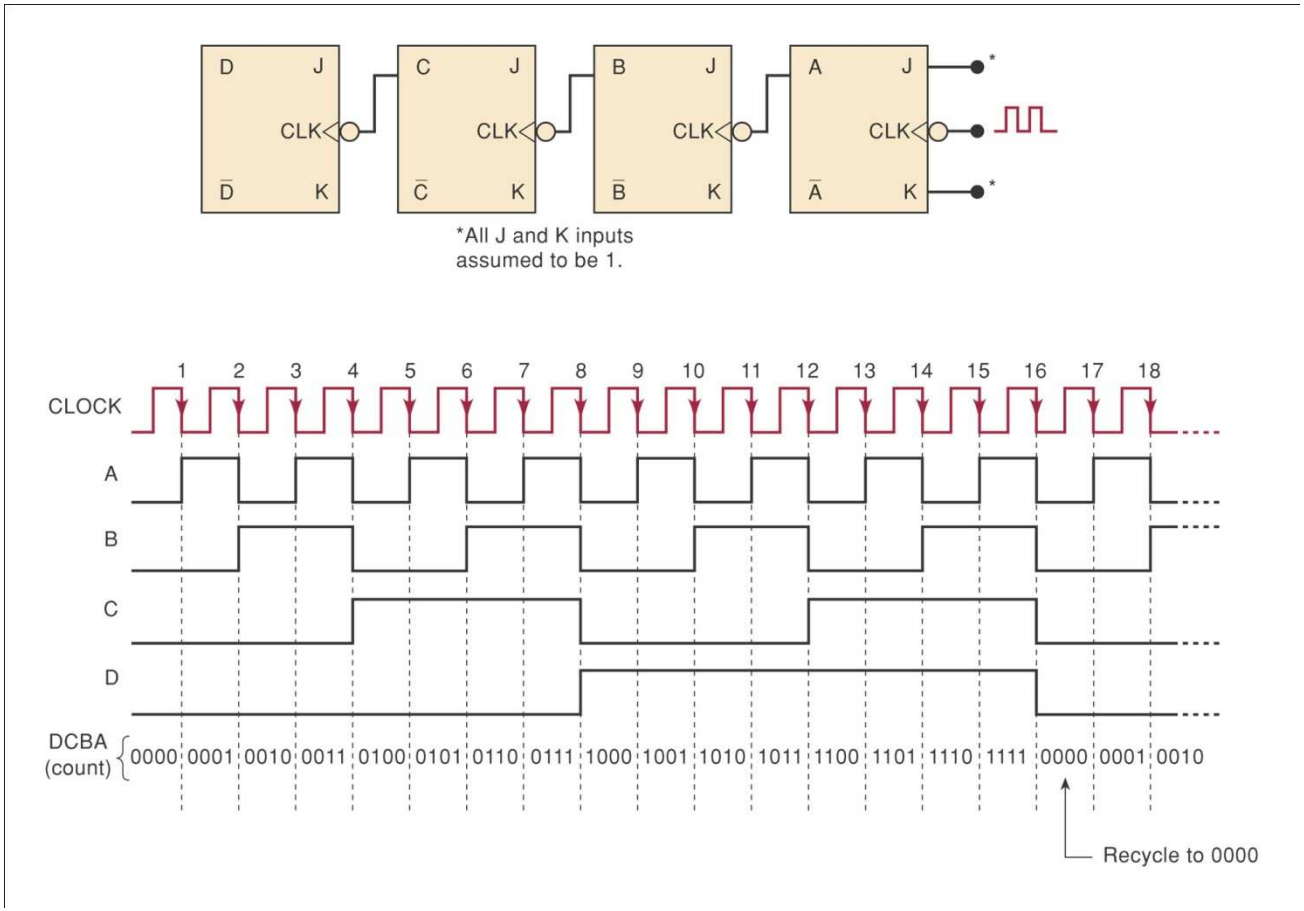
# Counters

- Asynchronous (Ripple)
- Synchronous

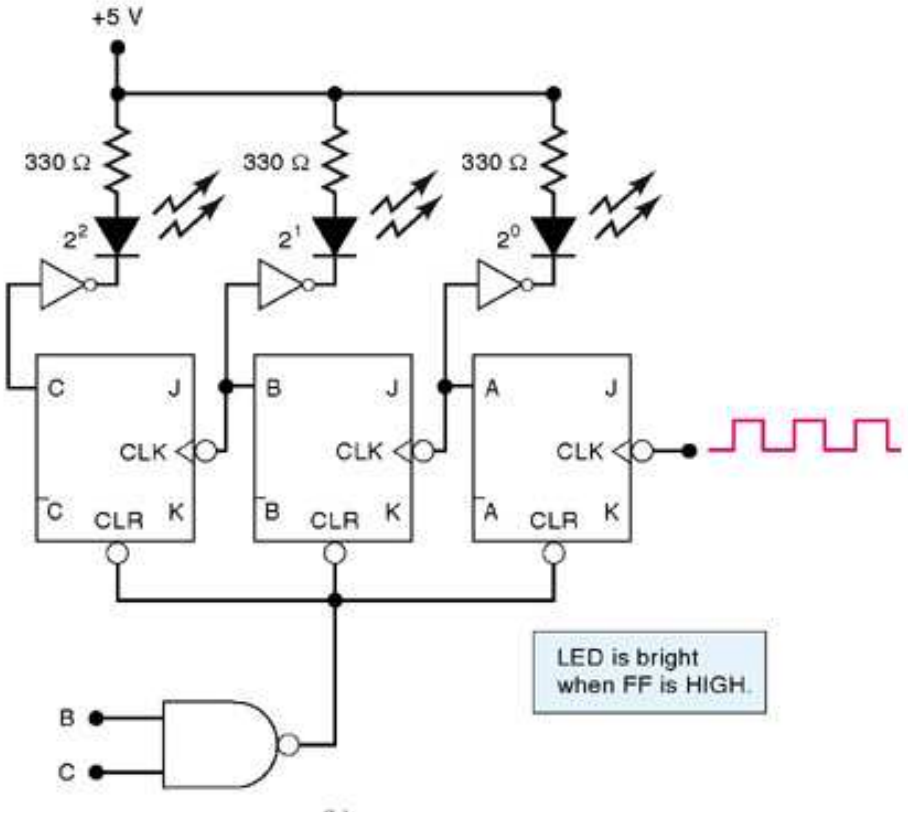
# Counters

- Analysis of counter:-counter circuit is given analyzing its count sequence.
- Design of a counter:-counter behavior will be given,  then designing a circuit accordingly to get expected counter behavior.

# Four-bit asynchronous (ripple) up counter.



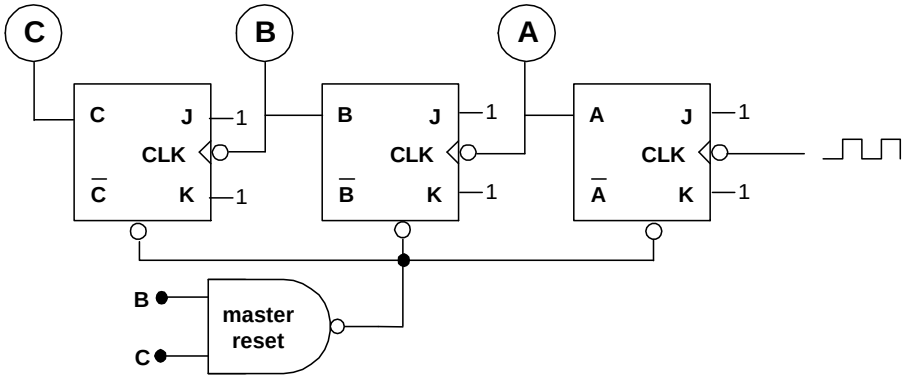
# Counters with MOD Number $<2^N$



# PROGRAMMING A RIPPLE COUNTER

- **Counters may be made to recycle after any desired count by using a gate to reset the counter.**

CONVERT MOD 8 TO MOD6




| INPUT CLK | | | |
|---|---|---|---|
| | C | B | A |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | | | |

UNSTABLE STATE

3 *FLIP FLOPS*

$2^3 = MOD\ 8$

$HIGHEST\ COUNT = 2^3 - 1 = 7$

# HOW TO BUILD A COUNTER TO GO FROM ZERO TO MOD NUMBER X

**1. Determine smallest number of FF's such that** $2^N \geq X$

$IF\ 2^N = X\ ,\ SKIP\ STEPS\ 2\ AND\ 3$

**2. Connect a NAND gate output to asynchronous clears of all FF's**

**3. Determine which FF's will be high at count = X**
**Connect the Q outputs of these FF's to NAND gate inputs**

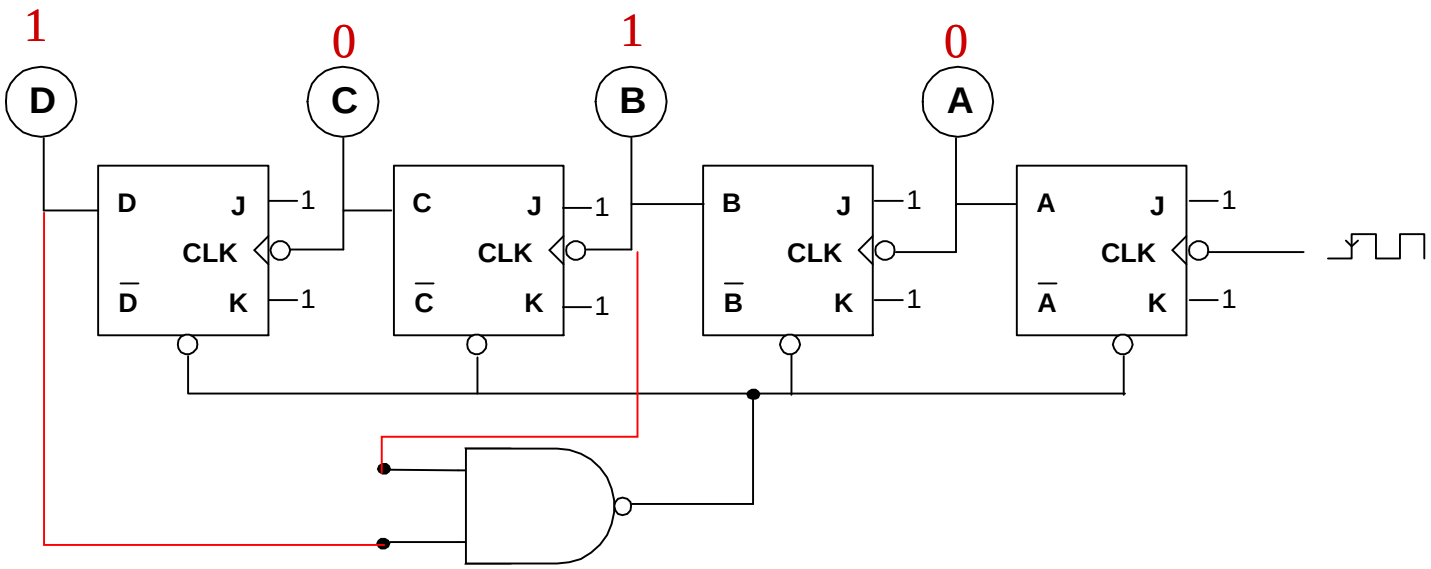
# BUILD A COUNTER THAT COUNTS FROM ZERO TO NINE (X=MOD 10)

**1. Determine smallest number of FF's such that** $2^N \geq X$

$2^3 = 8 \; and \; 2^4 = 16$ **thus 4 FF's are required**

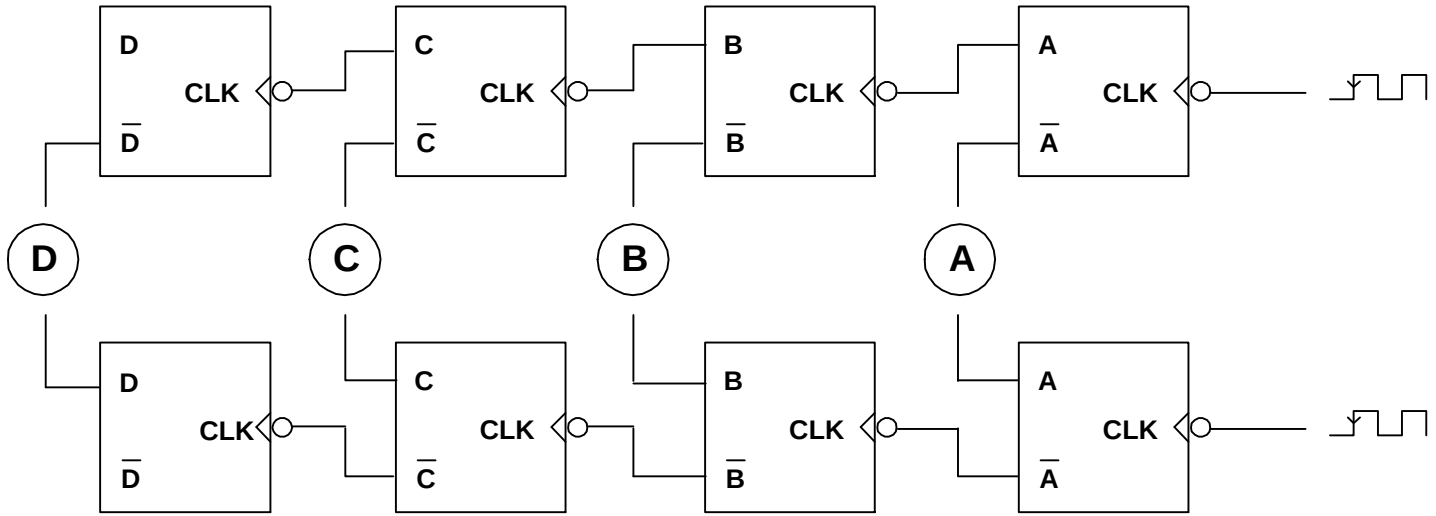
**2. Connect a NAND gate to asynchronous clears of all FF's**

**3. Determine which FF's will be high at count = X**
**Connect the Q outputs of these FF's to NAND gate inputs**



# ASYNCHRONOUS DOWN COUNTER

- Direction of count can be reversed by
  - (a) complementing each FF's output or
  - (b) complementing each FF's input



# COUNTER PROBLEM

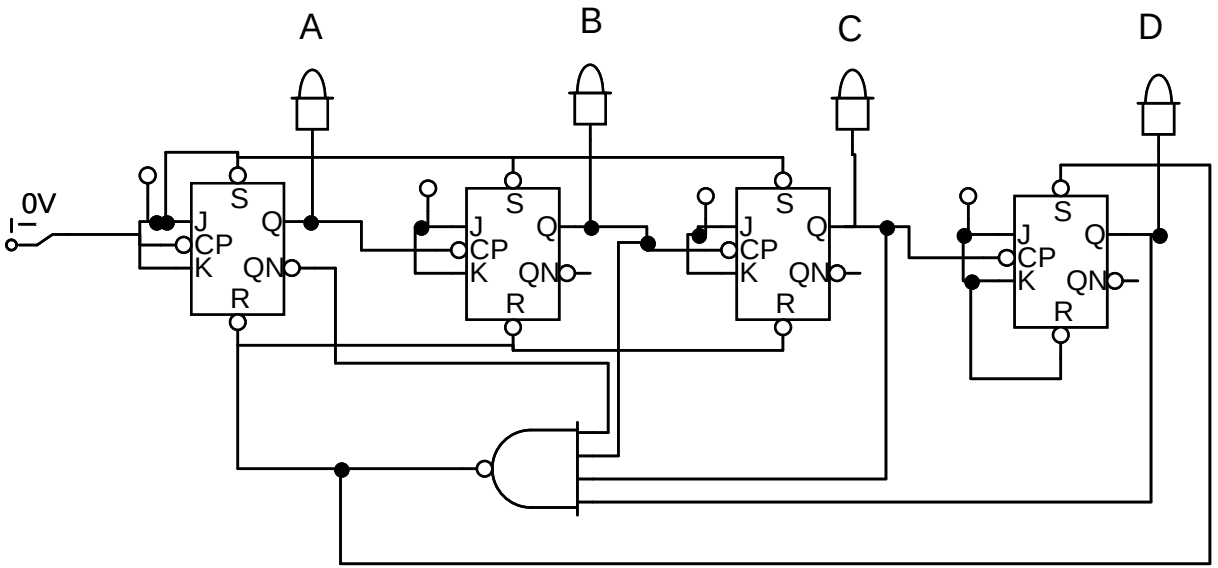
1. What is the value of the last usable state before the NAND gate resets the circuitry? $1101_2 = 13_{10}$

2. What value does the NAND gate reset the value to? $1000_2 = 8_{10}$

3. What is the modulus of this counter? 6

4. If count starts at decimal 11 and receives seven clock pulses, what is the new value on the counter? $12_{10}$

5. What is the unstable state of the counter? $1110_2 = 14_{10}$

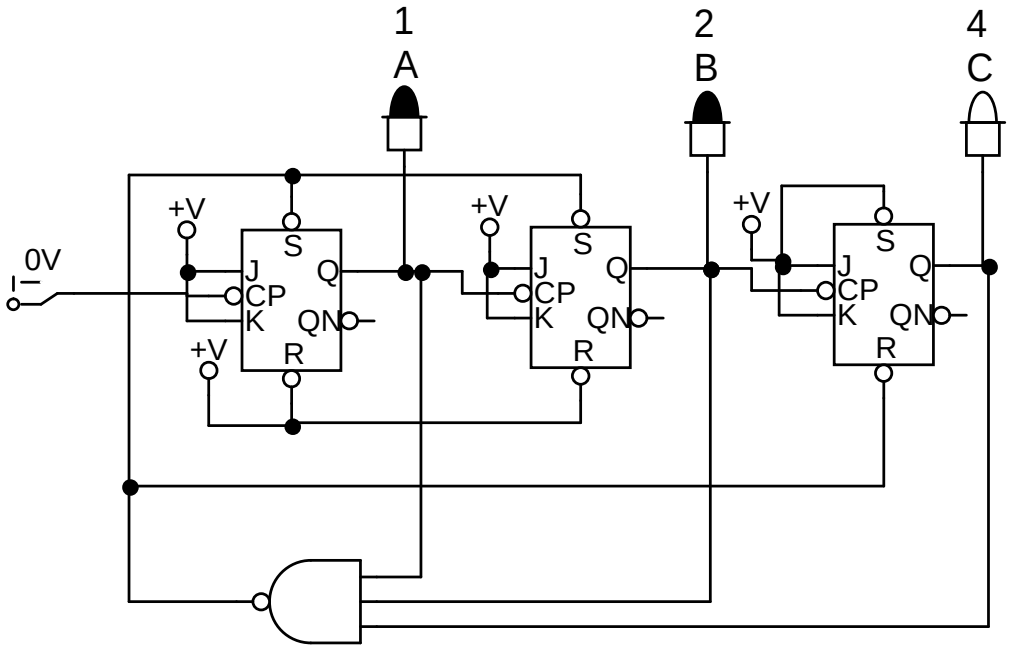


# COUNTER PROBLEM

1. What is the value of the unstable state, in decimal? $111_2 = 7_{10}$
2. At what value does the NAND gate set the counter to? $011_2 = 3_{10}$
3. If QA=1, QB=1, and QC=0, and 5 clock pulses are applied:

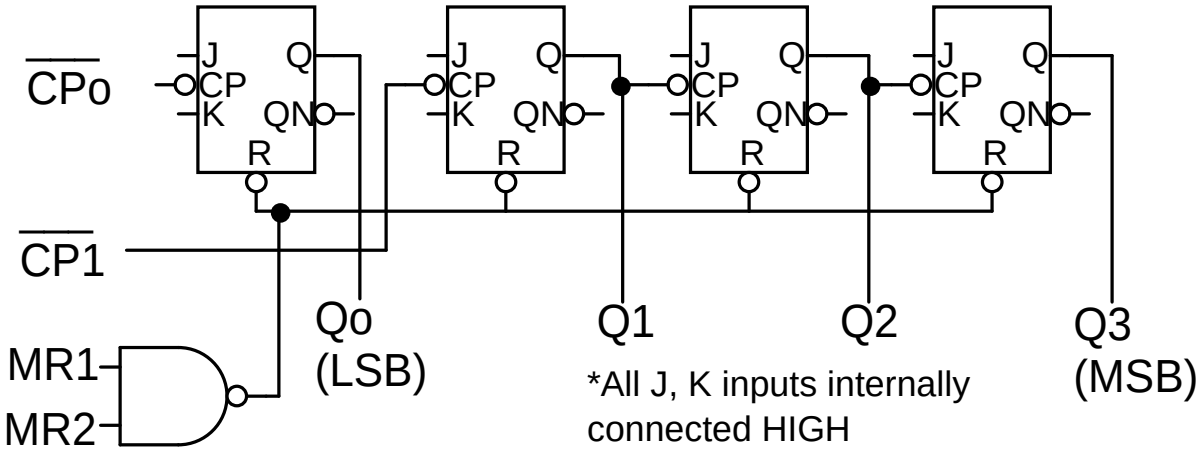
QC= QB= 1 QA= 0 0

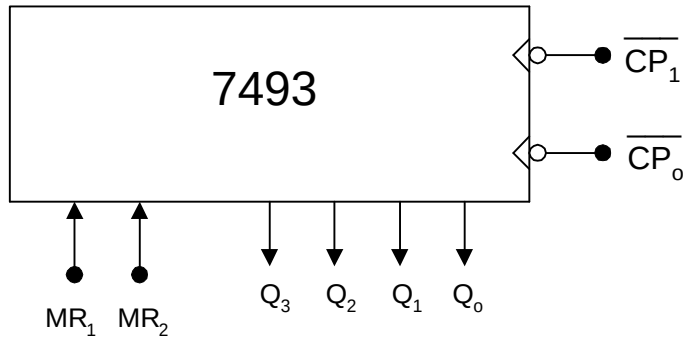
4. What is the modulus of this counter? 4



# IC ASYNCHRONOUS COUNTERS

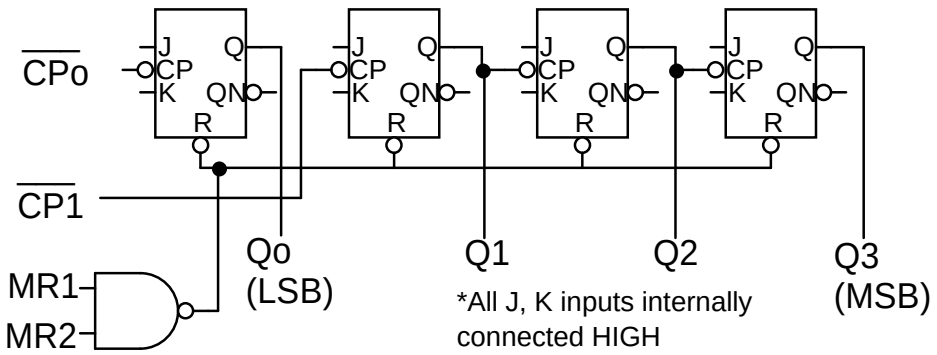
Logic Diagram for 7493

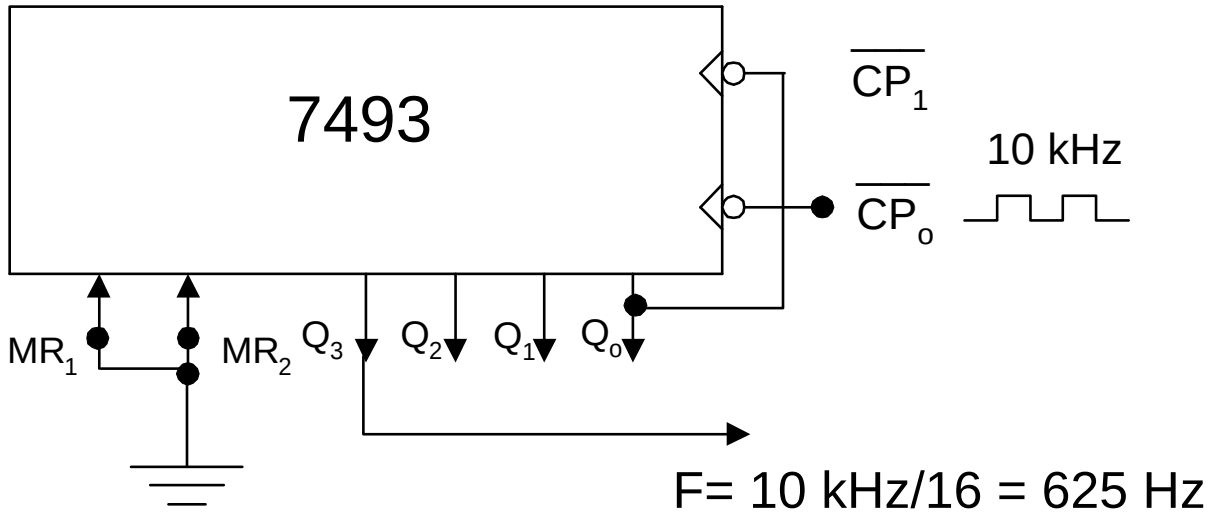


# 7493 AS A MOD-16 COUNTER

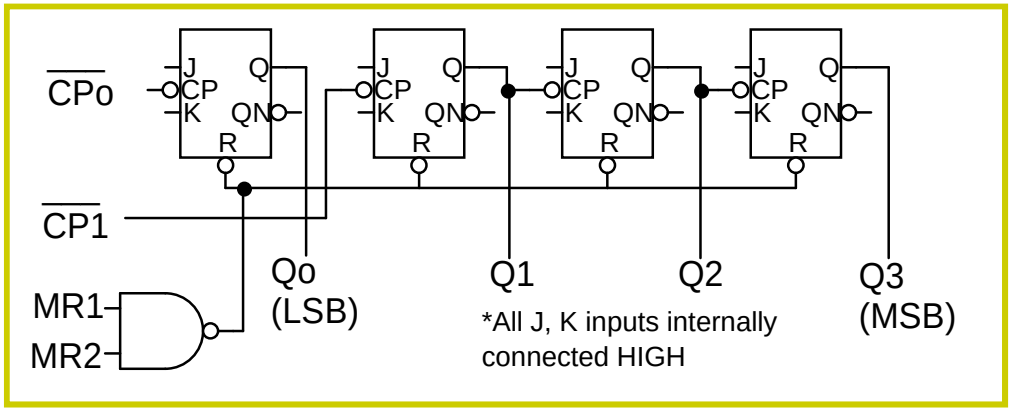
Logic Diagram for 7493

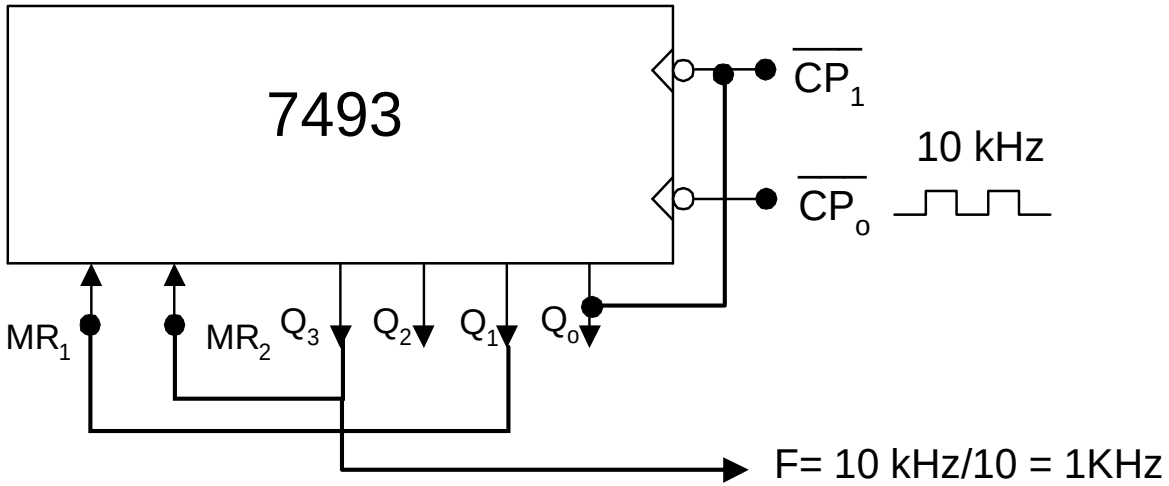



F= 10 kHz/16 = 625 Hz

# Build a MOD 10 counter with a 7493



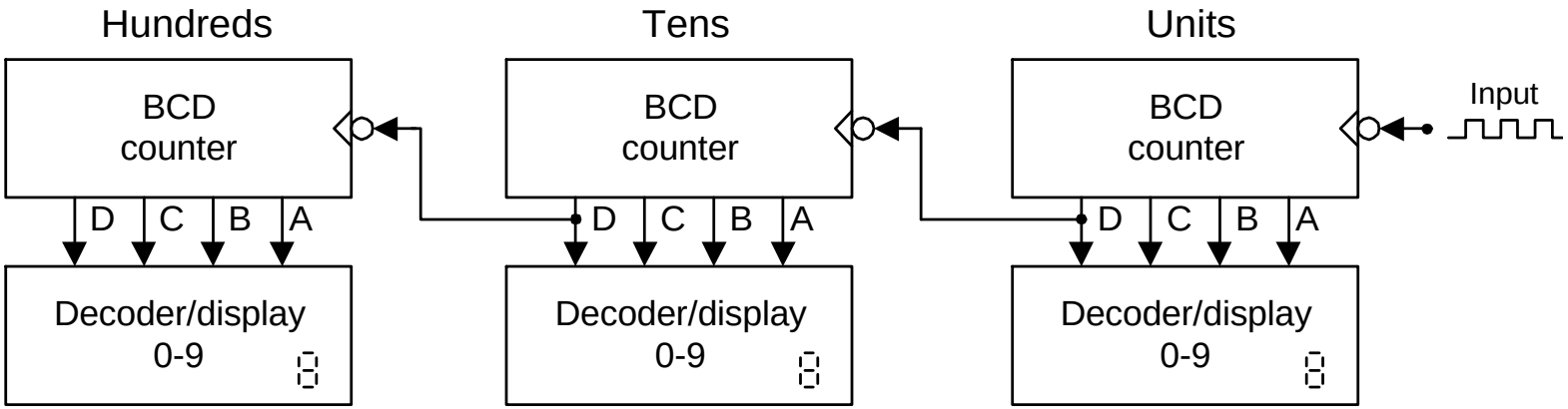



# BCD COUNTER

•Binary counter that counts from 0000 to 1001 before it recycles (MOD-10).

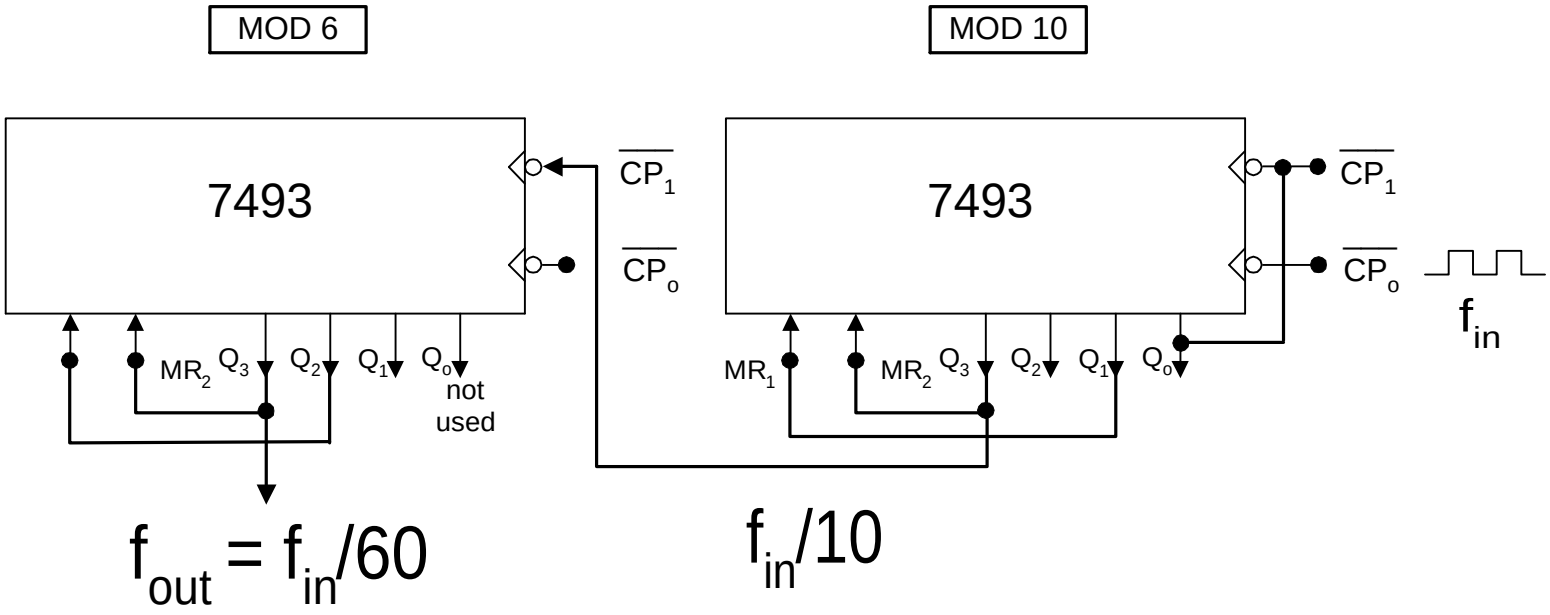
•Widespread applications where pulses or events are to be counted and the results displayed on a decimal numerical read-out.

•Also used for dividing a pulse frequency *exactly* by 10.




Cascading BCD counters to count and display from 000 to 999.

# MOD-60 COUNTER




Two 7493s can be combined to produce a MOD-60 Counter

# Design of a counter(Synchronous)

# Design of a synchronous 2 bit up/down counter using D flip flops

- Determine the number of flip-flops
- Draw state diagram
- Get excitation table
- Obtain the minimal expressions for inputs
- Draw the logic diagram

| Present State | Next State | F.F. Input |
|---|---|---|
| *Q*(*t*) | *Q*(*t*+1) | *D* |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| Present State | Next State | F.F. Input | |
|---|---|---|---|
| *Q*(*t*) | *Q*(*t*+1) | *J* | *K* |
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |

0 0 (No change)
0 1 (Reset)

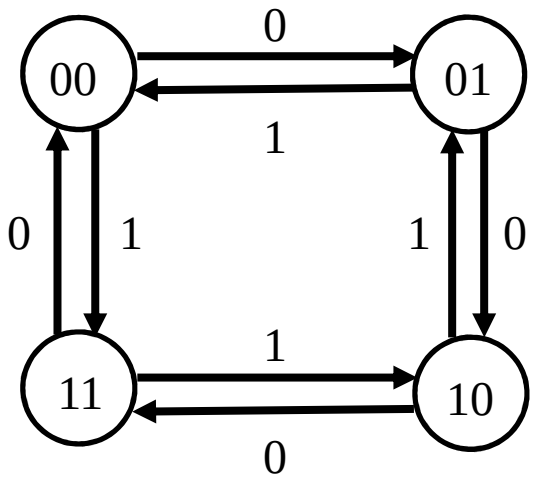
1 0 (Set)
1 1 (Toggle)

0 1 (Reset)
1 1 (Toggle)

0 0 (No change)
1 0 (Set)

| *Q*(*t*) | *Q*(*t*+1) | *T* |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# The complete state diagram and table




| Present State $Q_1$ | Present State $Q_0$ | Inputs X | Next State $Q_1$ | Next State $Q_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

# D flip-flop inputs

- If we use D flip-flops, then the D inputs will just be the same as the desired next states.
- Equations for the D flip-flop inputs are shown at the right.

| Present State | | Inputs | Next State | |
|---|---|---|---|---|
| $Q_1$ | $Q_0$ | X | $Q_1$ | $Q_0$ |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

| | $Q_0$ | | | |
|---|---|---|---|---|
| | 0 | 1 | 0 | 1 |
| $Q_1$ | 1 | 0 | 1 | 0 |
| | | X | | |

$D_1 = Q_1 \oplus Q_0 \oplus X$

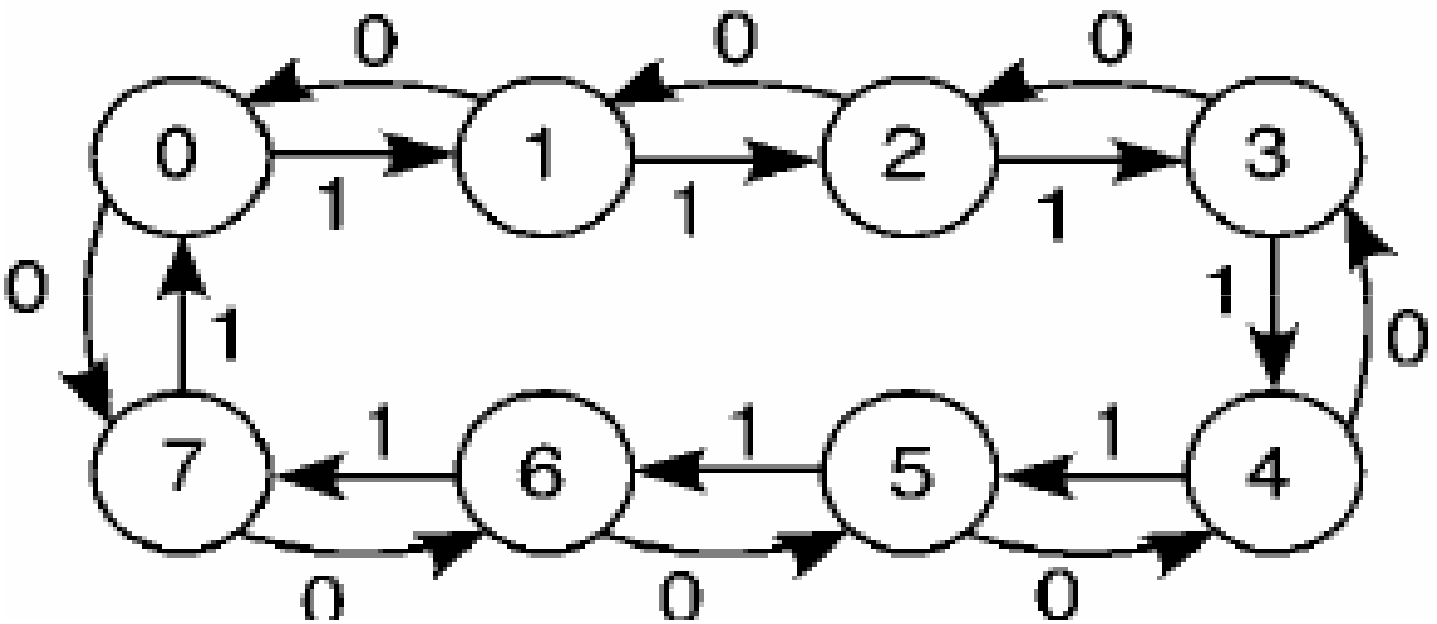
| | $Q_0$ | | | |
|---|---|---|---|---|
| | 1 | 1 | 0 | 0 |
| $Q_1$ | 1 | 1 | 0 | 0 |
| | | X | | |

$D_0 = Q_0'$

# Design of a synchronous 3 bit up/down counter using JK flip flops

- Determine the number of flip-flops
- Draw state diagram
- Get excitaion table
- Obtain the minimal expressions for inputs
- Draw the logic diagram

- State diagram



# Excitation table

| Present state | | | Mode | Next state | | | Required inputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Q3 | Q2 | Q1 | M | Q3 | Q2 | Q1 | J3 | K3 | J2 | K2 | J1 | K1 |
| **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **X** | **1** | **X** | **1** | **X** |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | 0 | X | 1 | X |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | 0 | X | X | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | X | 1 | X | X | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | X | X | 1 | 1 | X |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | X | X | 0 | 1 | X |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | X | X | 0 | X | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | X | X | 1 | X | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | X | 1 | 1 | X | 1 | X |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | X | 0 | 0 | X | 1 | X |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | X | 0 | 0 | X | X | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | X | 0 | 1 | X | X | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | X | 0 | X | 1 | 1 | X |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | X | 0 | X | 0 | 1 | X |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | X | 0 | X | 0 | X | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | X | 1 | X | 1 | X | 1 |

* PS=Present state *NS= Next state

| Present State | Next State | F.F. Input | |
|---|---|---|---|
| *Q*(*t*) | *Q*(*t*+1) | *J* | *K* |
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |

Q3(PS)Q3(NS) = 01 then from excitation table of JK flip flop J3K3 should be 1X( J3=1 K3=X)
Q2(PS)Q2(NS)= 01 then from excitation table of JK flip flop J2K2 should be 1X( J2=1 K2=X)
Similarly fill all the rows of excitation inputs for all states of counter

# K-maps for excitations of synchronous 3 bit U/D counter

Q1M

| Q3Q2 | | | | |
|---|---|---|---|---|
| | 1 | | | |
| | | | 1 | |
| | X | X | X | X |
| | X | X | X | X |

J3=Q2’Q1’M’+Q2Q1M

Q1M

| Q3Q2 | | | | |
|---|---|---|---|---|
| | X | X | X | X |
| | X | X | X | X |
| | | | 1 | |
| | 1 | | | |

K3=Q2’Q1’M’+Q2Q1M

Q1M

| Q3Q2 | | | | |
|---|---|---|---|---|
| | 1 | | 1 | |
| | X | X | X | X |
| | X | X | X | X |
| | 1 | | 1 | |

J2=Q1’M’+Q1M

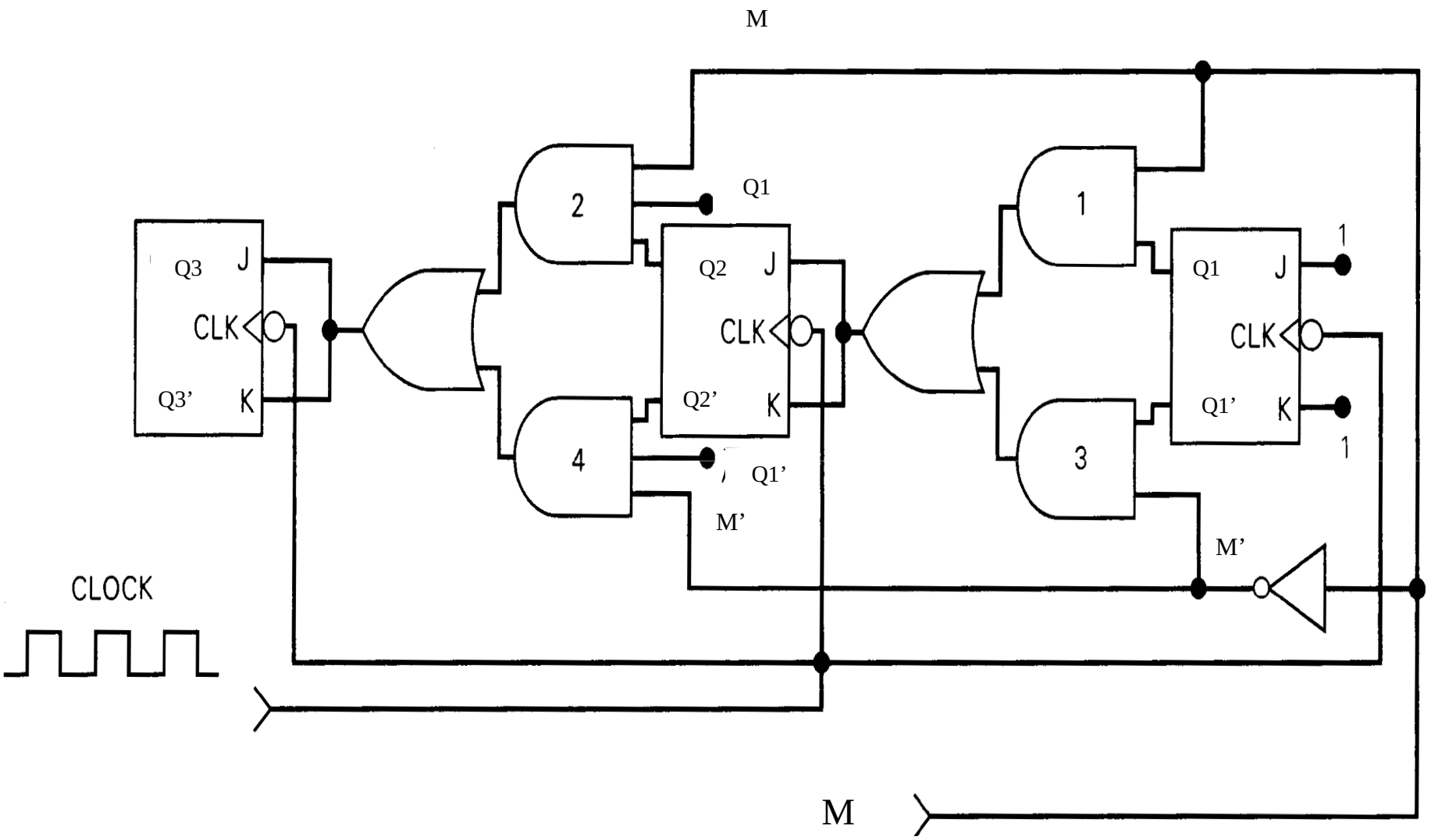
J1=1

Q1M

| Q3Q2 | | | | |
|---|---|---|---|---|
| | X | X | X | X |
| | 1 | | 1 | |
| | 1 | | 1 | |
| | X | X | X | X |

K2=Q1’M’+Q1M

k1=1


M
Q3
J
CLK
Q3'
K
2
Q1
Q2
J
CLK
Q2'
K
4
Q1'
M'
1
Q1
J
CLK
Q1'
K
1
1
3
M'
CLOCK
M

Draw the final circuit of 3bit UP/DOWN counter using D and T flip flop

- Work for you

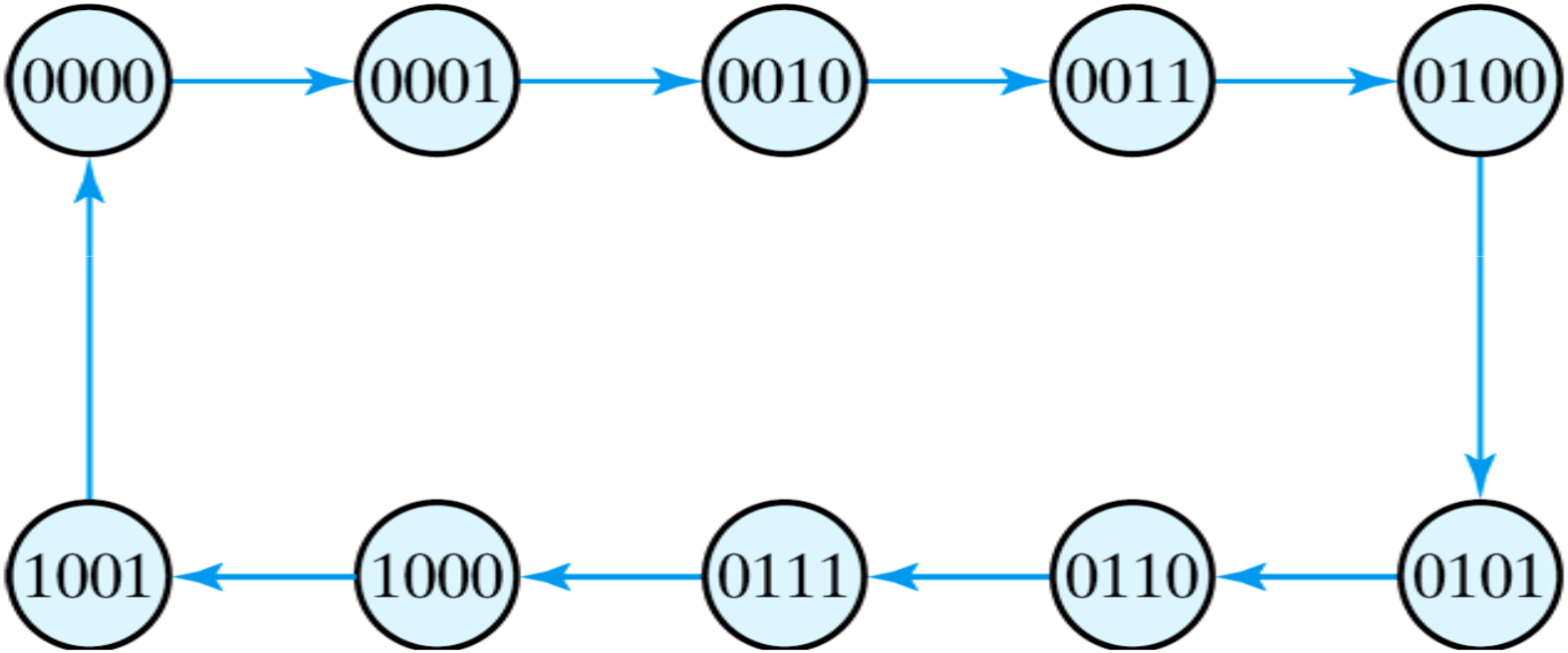
# Design of a BCD (mod10) or decade counter using JK and T flip flops

- Determine the number of flip-flops
- Draw state diagram
- Get excitation table
- Obtain the minimal expressions for inputs
- Draw the logic diagram

# Determine the number of flip-flops

- 3 will not be sufficient (0 to 7)
- We will require 4(JK or D)

# Draw state diagram



Write Excitation table (Present state Next State Excitation Inputs for JK FF and T FF).
Obtain the Equations for J1K1 J2K2 J3K3 and J4K4
Draw the final circuit of BCD counter using JK flip flop .
Obtain the Equations for T1, T2,T3 and T4.
Draw the final circuit of BCD counter using T flip flop .

- Work for you