Asynchronous Counter

Asynchronous Counter

This presentation will

- Define *asynchronous counters*.
- Define the terms *states* and *modulus*.
- Provide multiple examples of asynchronous counters designed with D & J/K flip-flops.
- Explain an asynchronous counter's ripple effect.
- Summarize the asynchronous counter design steps.

Asynchronous Counters

- Only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop.
- Asynchronous counters are slower than synchronous counters (discussed later) because of the delay in the transmission of the pulses from flip-flop to flip-flop.
- Asynchronous counters are also called ripple counters because of the way the clock pulses, or ripples, its way through the flip-flops.

States / Modulus / Flip-Flops

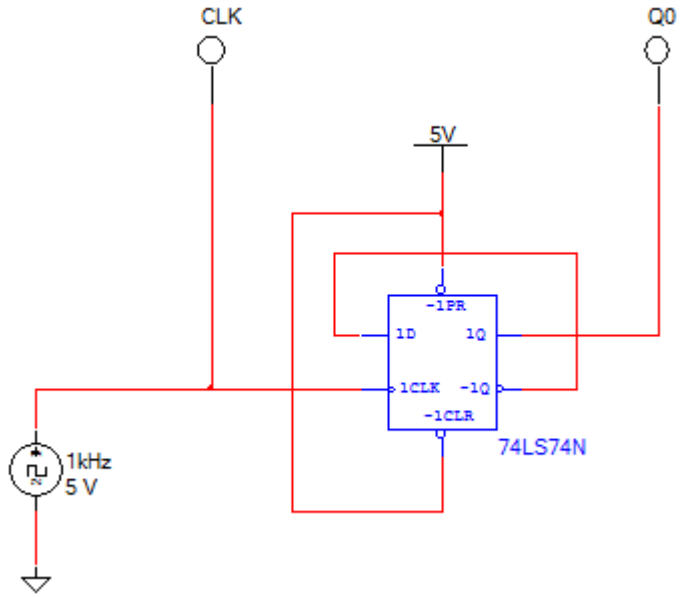
- The number of flip-flops determines the count limit or number of states:

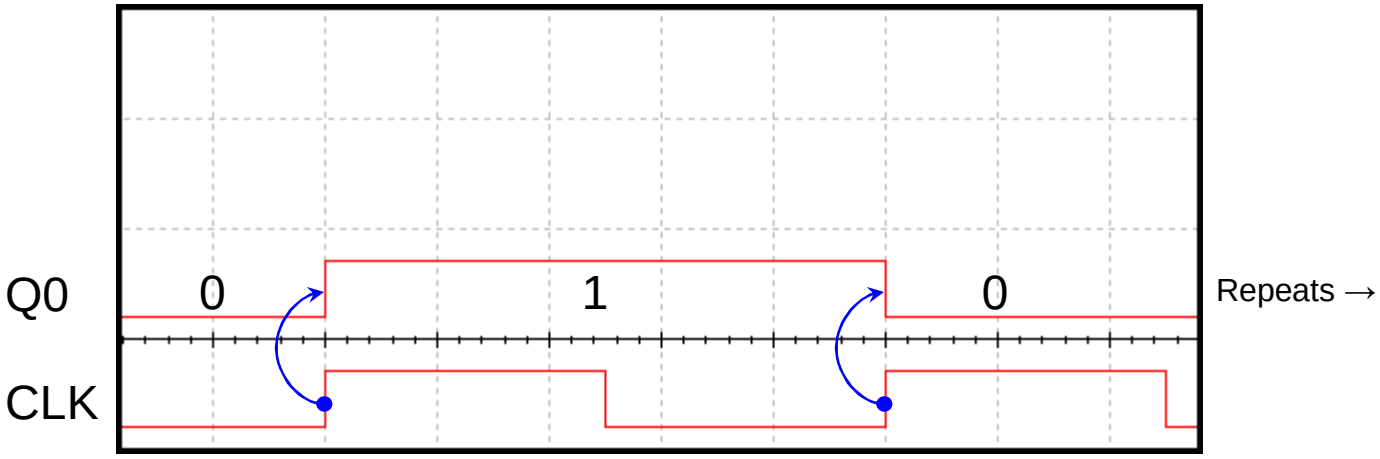
$$\text{States} = 2^{(\#\text{ of flip-flops})}$$

- The number of states used is called the MODULUS.
- For example, a Modulus-12 counter (Mod-12) would count from 0 (0000) to 11 (1011) and would require four flip-flops ($2^4 = 16$ states; 12 are used)

Asynchronous Counter

D-Flip Flop – 1 Bit

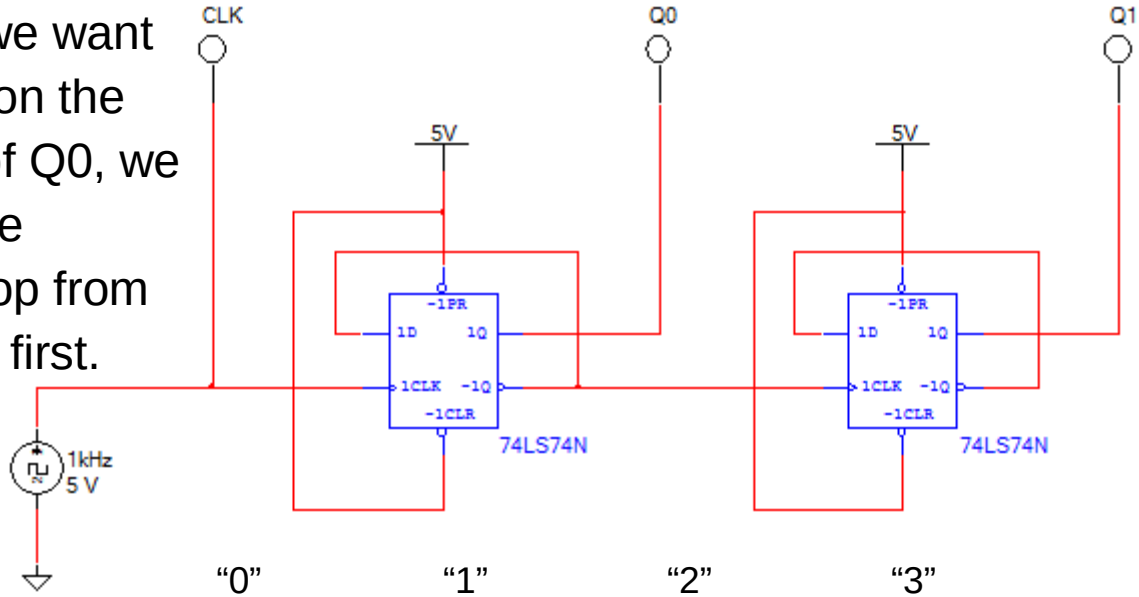


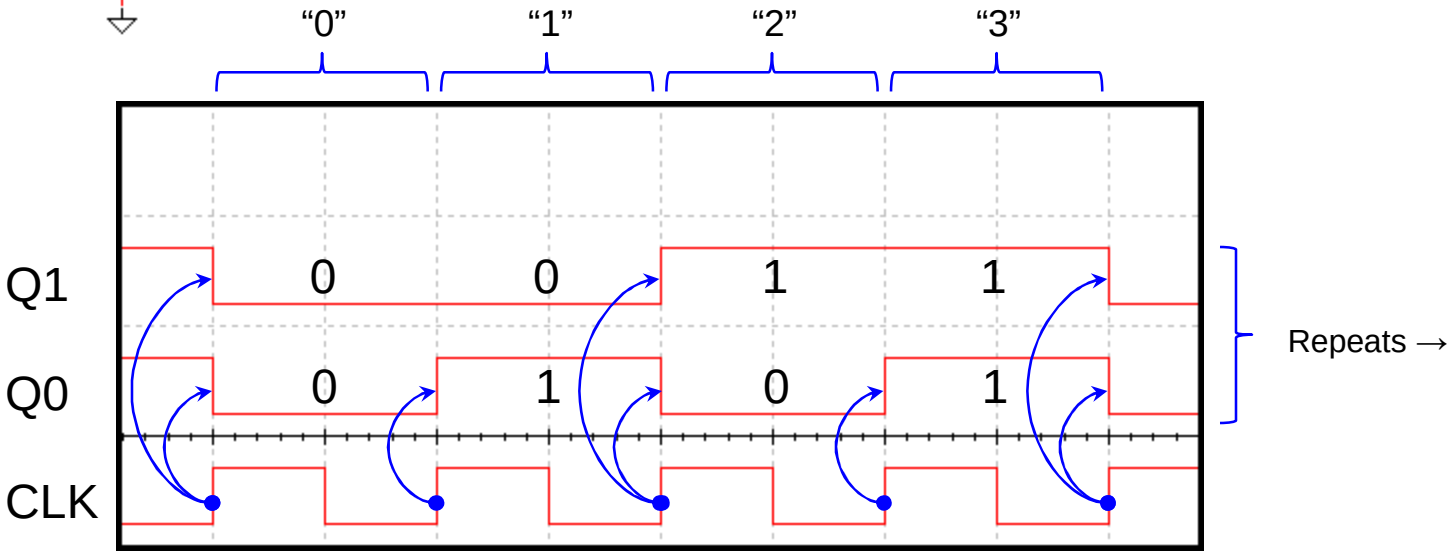


Asynchronous Counter

Up Counter – D-Flip Flops – 2 Bit

Note: Since we want Q1 to toggle on the falling edge of Q0, we must clock the second flip-flop from the $\overline{Q0}$ of the first.

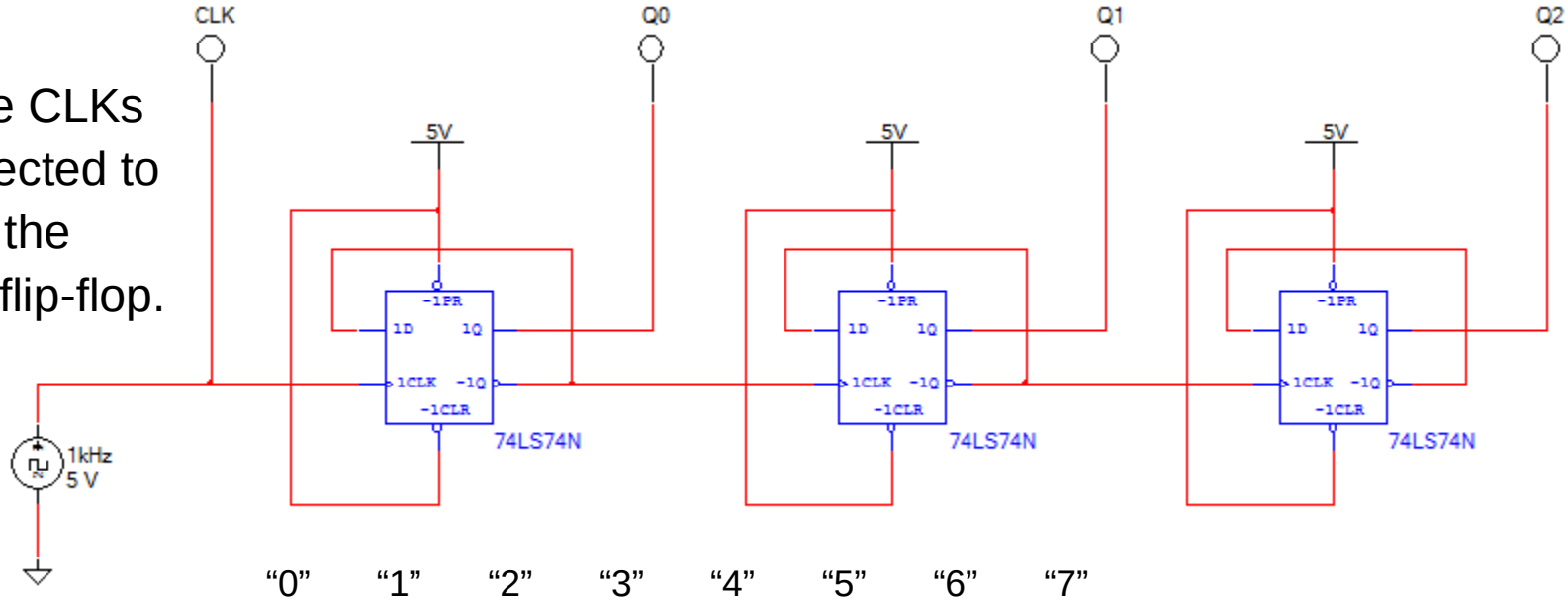


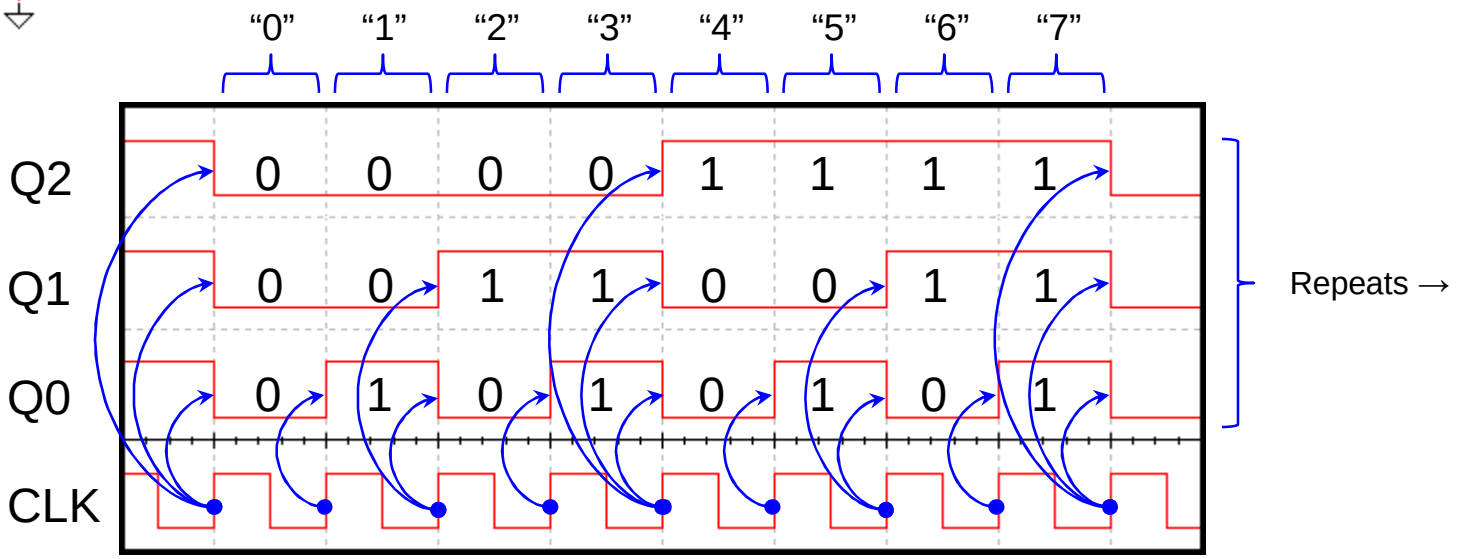


Asynchronous Counter

Up Counter – D-Flip Flops – 3 Bit

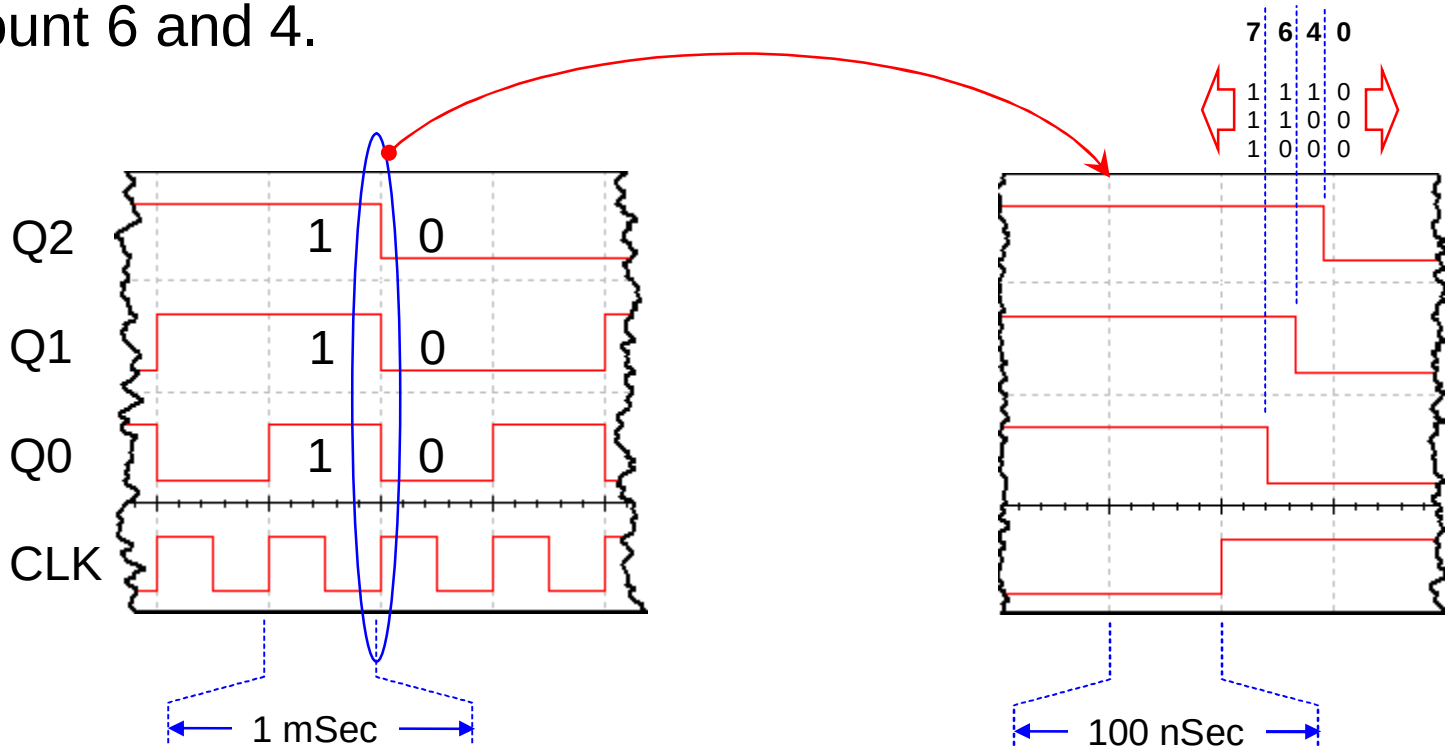
Note: The CLKs are connected to the $\overline{Q}$ of the previous flip-flop.





The Ripple Effect

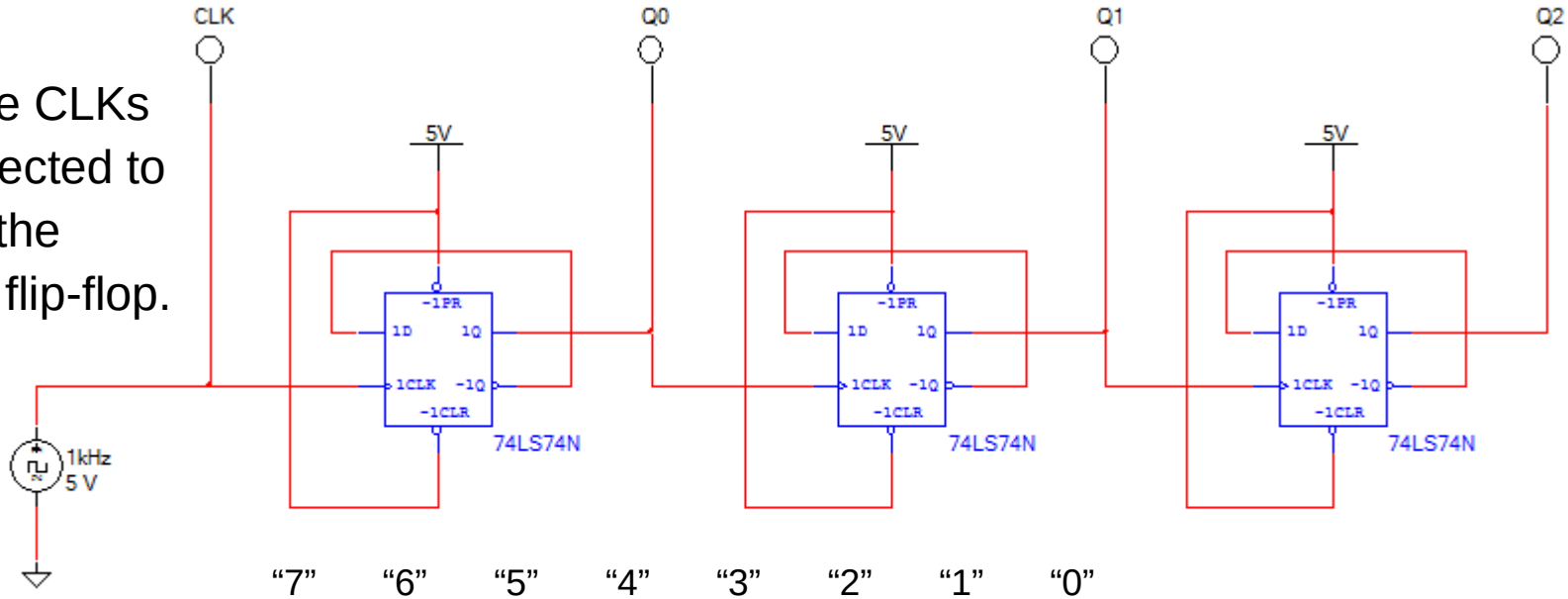
As the clock input “ripples” from the first flip-flop to the last, the propagation delays from the flip-flops accumulate. This causes the Q outputs to change at different times, resulting in the counter briefly producing incorrect counts. For example, as a 3 bit ripple counter counts from 7 to 0, it will briefly output the count 6 and 4.

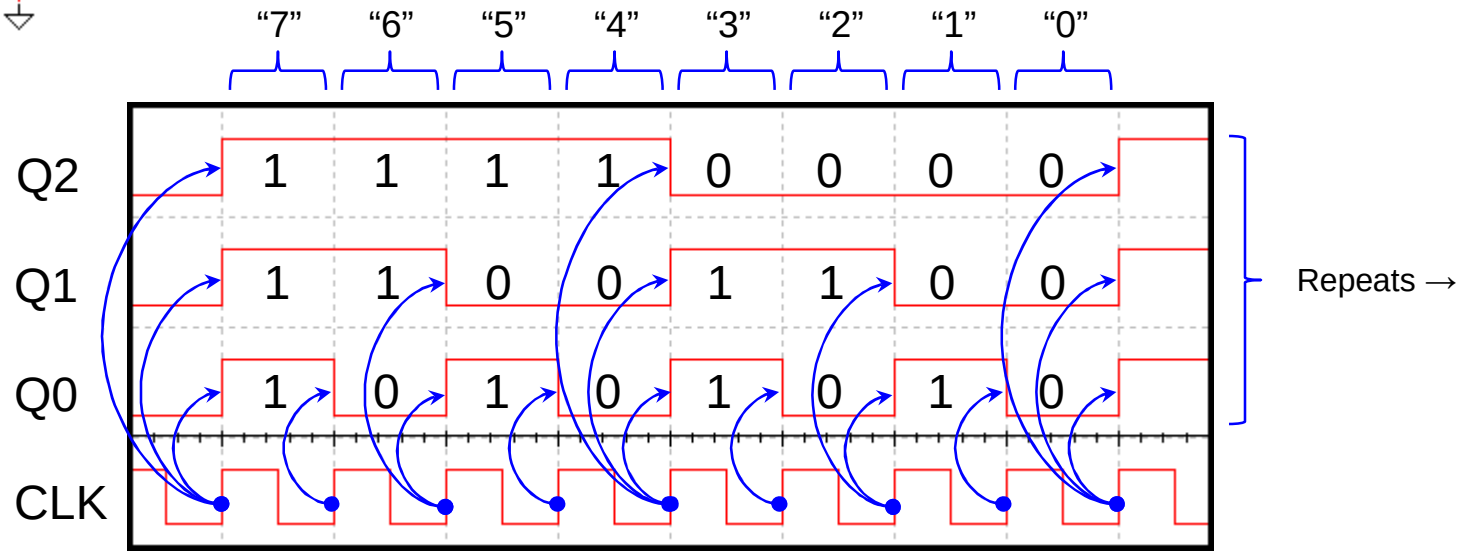


Asynchronous Counter

Down Counter – D-Flip Flops – 3 Bit

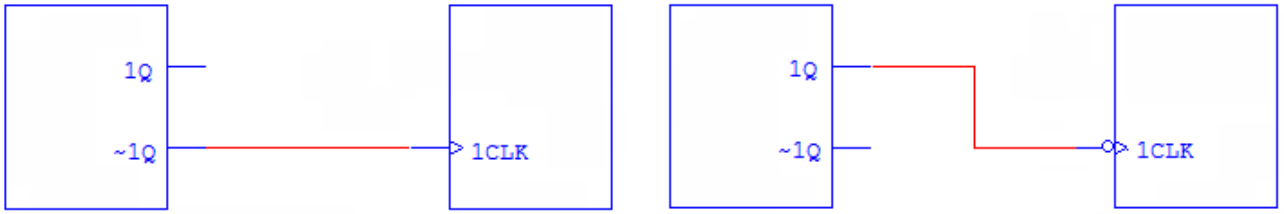
Note: The CLKs are connected to the Q of the previous flip-flop.



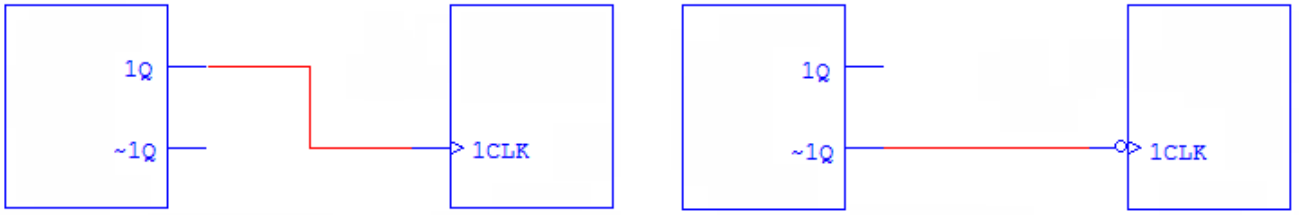


Asynchronous Counter Summary

- Up Counters
  - Connect the CLK input to the Q output with the opposite polarity



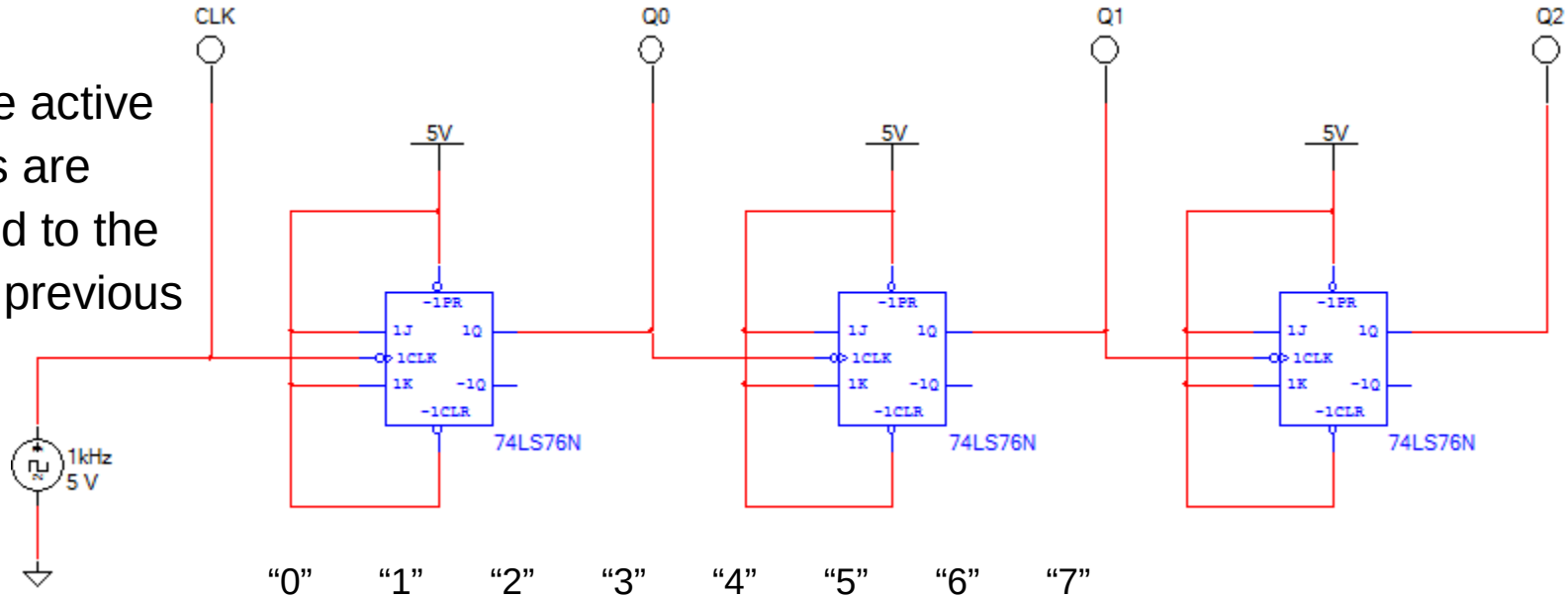
- Down Counters
  - Connect the CLK input to the Q output with the same polarity

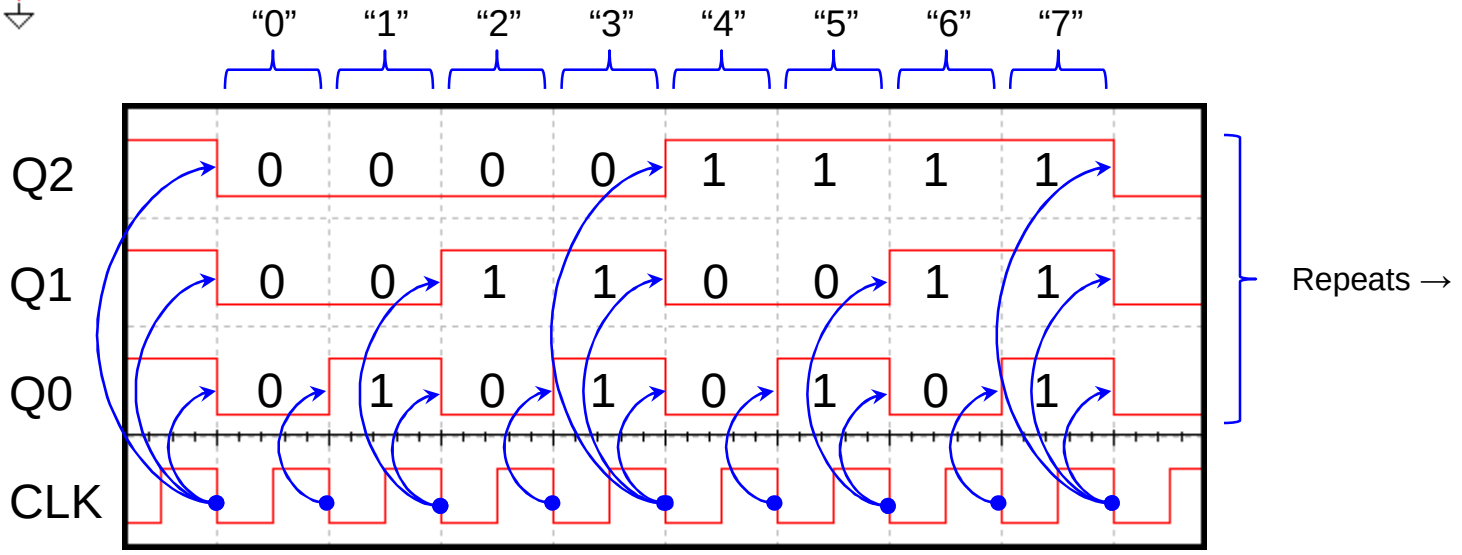


Asynchronous Counter

Up Counter – JK-Flip Flops – 3 Bit

Note: The active low CLKs are connected to the Q of the previous flip-flop.

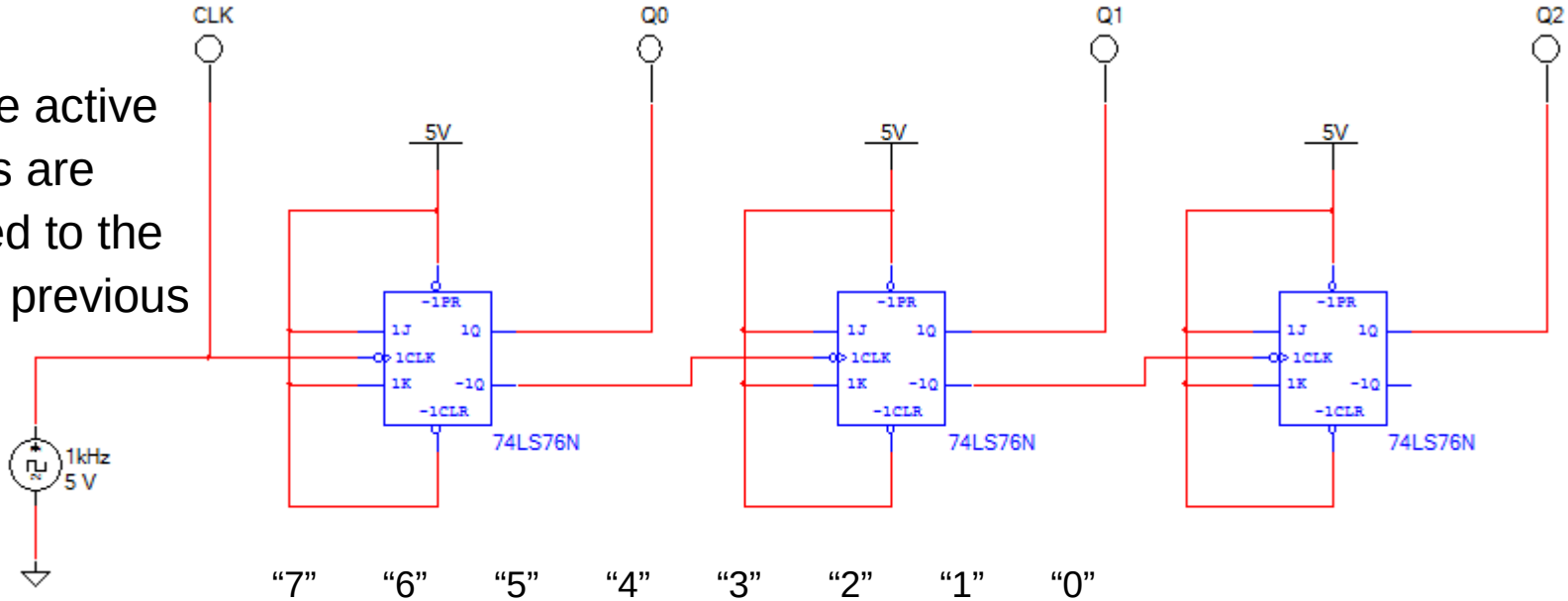


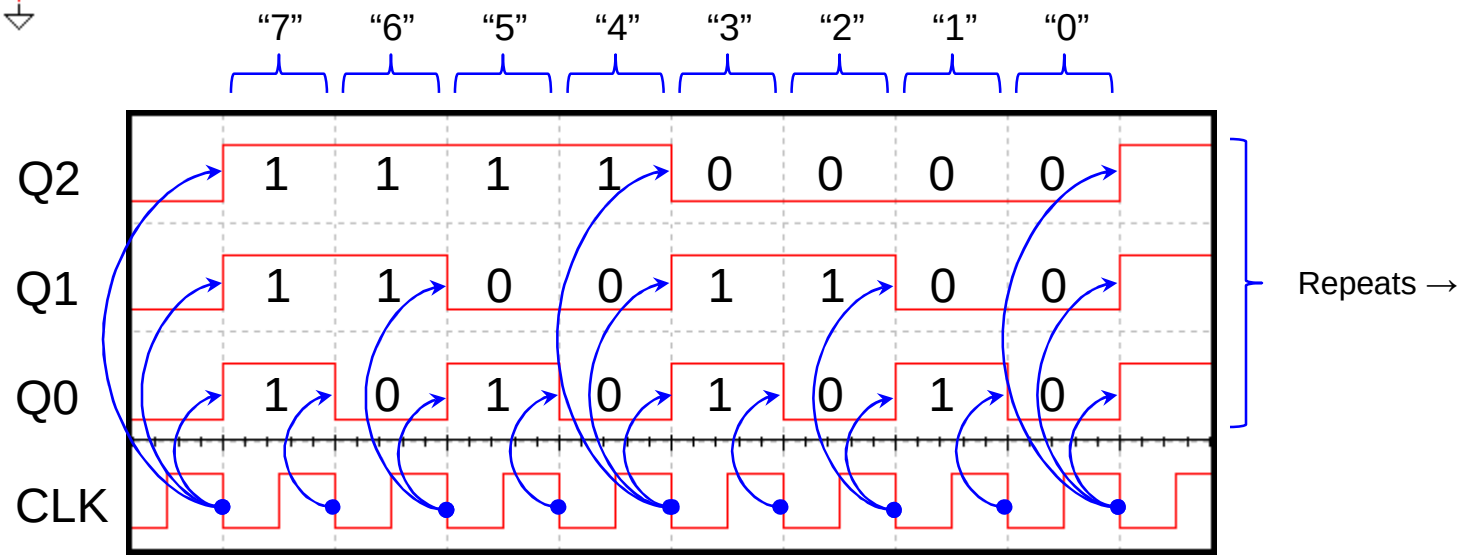


Asynchronous Counter

Down Counter – JK-Flip Flops – 3 Bit

Note: The active low CLKs are connected to the $\overline{Q}$ of the previous flip-flop.

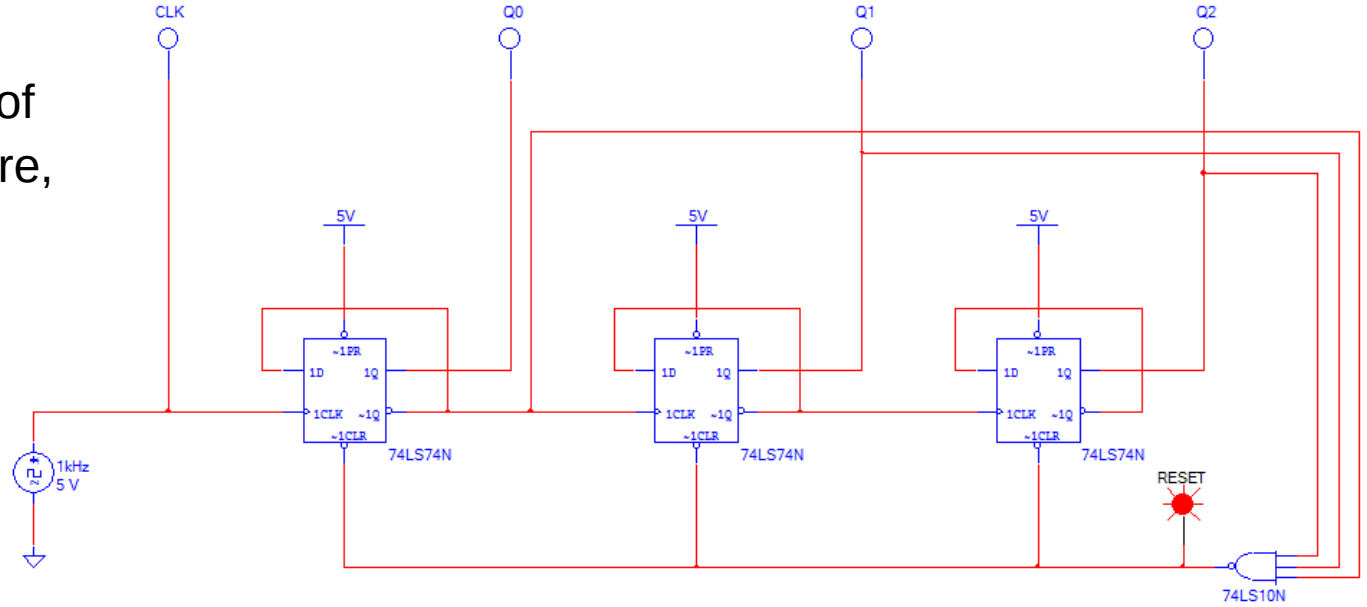


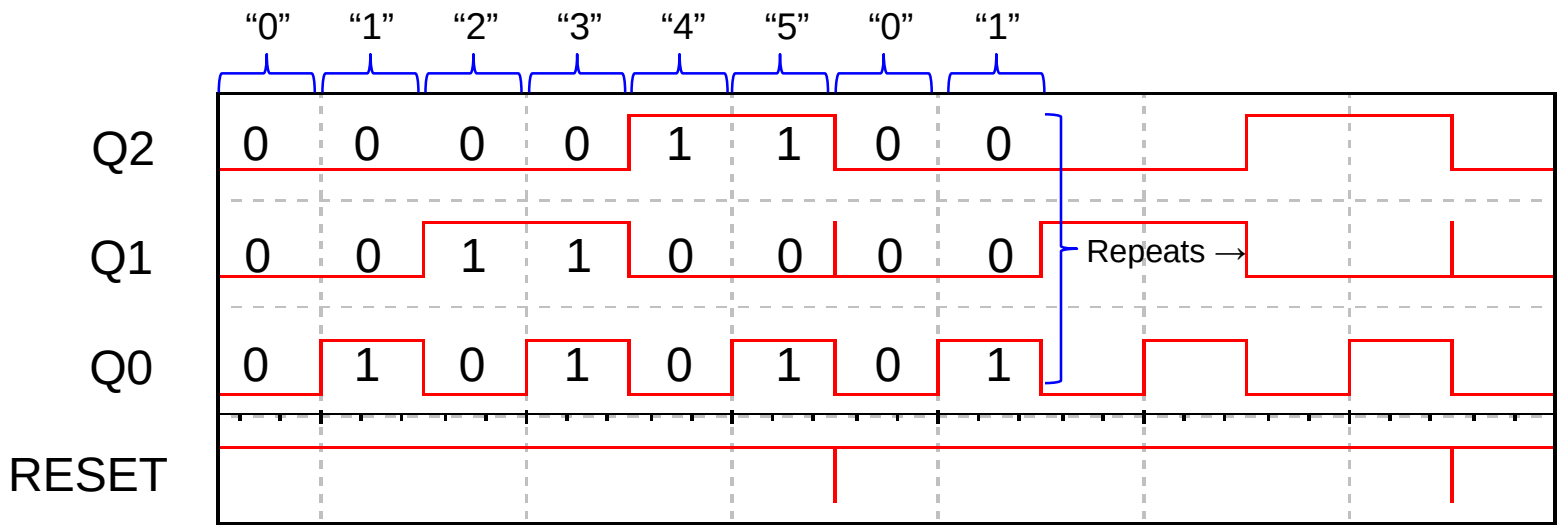


Modulus Asynchronous Counter

Up Counter – D Flip Flops – 3 Bit / Mod-6 (0-5)

Note: The upper limit of the count is 5; therefore, the reset circuit must detect a 6 (count +1).





Asynchronous Counter Design Steps

1) Select Counter Type
   - Up or Down
   - Modules
2) Select Flip-Flop Type
   - D (74LS74)
   - J/K (74LS76)
3) Determine Number of Flip-Flops
   - $2^{\#\text{ Flip-Flops}} \geq$ Modules
4) Design Count Limit Logic
   - Input to reset logic circuit is count limit plus one for up counters (minus one for down counters)