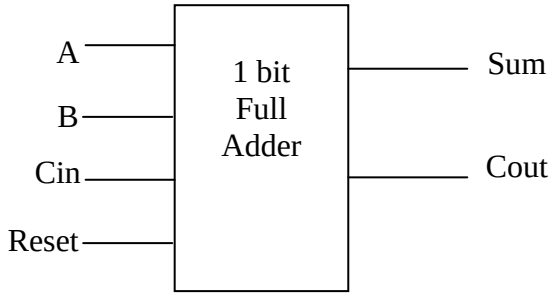
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
Second Semester 2012-2013
IS F242 Computer Organization
Lab Handout - 1, 29th January 2013

Lab Question:

1. Given below the truth table of a 1 bit adder.

A	B	Cin	Reset	Sum	Cout
X	X	X	0	0	0
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	1	1



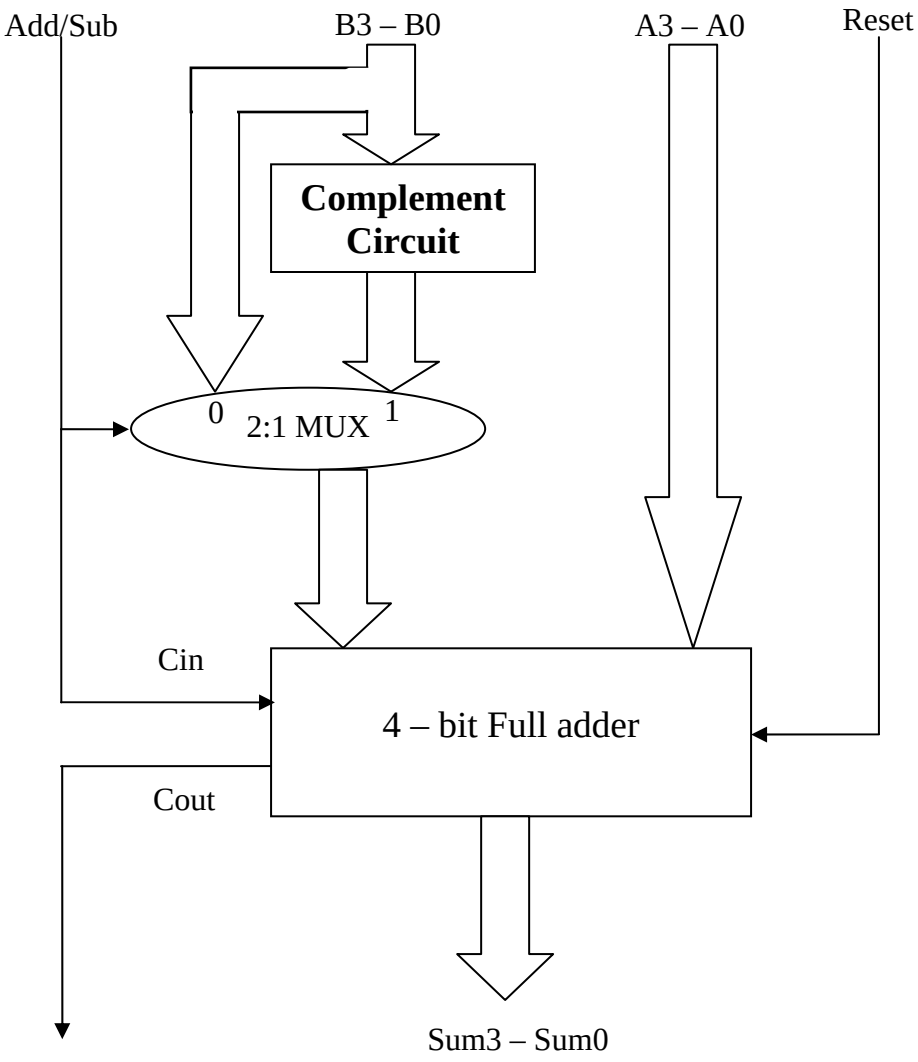
1. Implement a 1-bit full adder as given in the truth table
(A) Gate level model
(B) Data flow model and
(C) Behavioral model
2. Run the code in veriwell simulator with a test bench which includes all cases and checks the correctness of the design.
3. Design a 4 – bit Added / Subtractor as shown in figure below. Run the code in veriwell simulator with a test bench and check the correctness of the design.

module Adder1b(A, B, Cin, Reset, Sum, Cout); // 1 bit adder

module Adder4b(A4b, B4b, Cin, Reset, Sum4b, Cout); // 4 bit adder using 1 bit adder

module AddSub4b(A4b, B4b, AddSub, Reset, Sum4b, Cout); // Complement circuit,
// 2:1 mux, and 4 bit adder

module testbench;


Add/Sub
B3 – B0
A3 – A0
Reset
Complement Circuit
0
2:1 MUX
1
Cin
4 – bit Full adder
Cout
Sum3 – Sum0