BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
Second Semester 2012-2013
IS F242 Computer Organization
Homework for Lab – 2, 5th February 2013

Design and implement the following using verilog HDL in **Xilinx software** with the following specifications.

1. **module D_FF(D, Q, Clk,WE);**
   //A D flip flop has 3 input and 1 output ports. The inputs are – 1 bit input D, 1 bit clock Clk and 1 bit write enable WE. The clock is neg edge triggered (not level triggered). The output is – 1 bit Q. The truth table of a D flip flop is given below.

Clk	WE	D	Q
Non – neg edge	X	X	Q
Neg edge	0	X	Q
Neg edge	1	0	0
Neg edge	1	1	1

2. **module Register(in_Reg, out_Reg, reg_Write, Clk);**
   // A 16 – bit register is made of 16 D_FFs. The register has 3 input and 1 output ports. The inputs are – 16 bit in_Reg, 1 bit clock Clk and 1 bit reg_Write. The clock is neg edge triggered (not level triggered). The output is – 16 – bit out_Reg. The working of Register is as follows:
   All the non- neg edge clock time, the register will preserve its previous value.
   In neg edge clock time, if the reg_Write is 0 then the register will preserve its previous value. i.e. out_Reg will be the same value as previous.
   In neg edge clock time, if the reg_Write is 1 then the register will store the 16 – bit in_Reg value to the register and the out_Reg will be same as in_Reg value.

3. **Testbench;**

Solve this problem and take it to the lab. We will be using these modules in next lab.

From next lab on we are going to use Xilinx. So solve this using Xilinx (installed in all Zone 2 and Zone 3 machines in CC)