Digital Electronics and Microprocessors

Class 13

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Synthesis of a sequential circuits(Design Procedure)

- Design Procedure for sequential circuit
  - The word description of the circuit behavior to get a state diagram;
  - State reduction if necessary;
  - Assign binary values to the states;
  - Obtain the binary-coded state table;
  - Choose the type of flip-flops;
  - Derive the simplified flip-flop input equations and output equations;
  - Draw the logic diagram;

SHIFT REGISTER VOCABULARY

REGISTER- group of flip flops capable of storing data.

SERIAL DATA TRANSMISSION- transfer of data from one place to another one bit at a time.

PARALLEL DATA TRANSMISSION- simultaneous transfer of all bits of a data word from one place to another.

SISO- SERIAL IN/SERIAL OUT- type of register that can be loaded with data serially and has only one serial output.

SIPO- SERIAL IN/PARALLEL OUT- type of register that can be loaded with data serially and has parallel outputs available.

PISO- PARALLEL IN/SERIAL OUT- type of register that can be loaded with parallel data and has only one serial output.

PIPO- PARALLEL IN/PARALLEL OUT- type of register that can be loaded with parallel data and has parallel outputs available.

OVERVIEW OF SHIFT REGISTERS

- A shift register is a sequential logic device made up of flip-flops that allows parallel or serial loading and serial or parallel outputs as well as shifting bit by bit.
- Common tasks of shift registers:
  - Serial/parallel data conversion
  - UART (an example)
  - Time delay
  - Ring counter
  - Twisted-ring counter or Johnson counter
  - Memory device

CHARACTERISTICS OF SHIFT REGISTERS

- Number of bits (4-bit, 8-bit, etc.)
- Loading
  - Serial
  - Parallel (asynchronous or synchronous)
- Common modes of operation.
  - Parallel load
  - Shift right-serial load
  - Shift left-serial load
  - Hold
  - Clear
- Recirculating or non-recirculating

Integrated-Circuit Registers

- Registers can be classified by the way data is entered for storage, and by the way data is outputted from the register.
  - Parallel in/parallel out (PIPO)
  - Serial in/serial out (SISO)
  - Parallel in/serial out (PISO)
  - Serial in/parallel out (SIPO)

PIPO – The 74ALS174/74HC174

- Refer to Figure 7-47
  - Six bit register
  - Parallel inputs D_5 through D_0
  - Parallel outputs Q_5 through Q_0
- Parallel data loaded to the register on the PGT of CP
- Master reset can reset all FFs asynchronously

SISO – 74ALS166/74HC166

- Refer to Figure 7-49
  - The chip contains an 8-bit shift register
  - The serial input is labeled SER
  - Only the Q_H output is accessible.
  - Clock input responds to PGT
- Inputs A-H provide the means for parallel data entry into register FFs

PISO – The 74ALS165/74HC165

- Refer to figure 7-51
  - 8 bit register
  - Serial data entry via D_S
  - Asynchronous parallel data entry P_0 through P_7
  - Only the outputs of Q_7 are accessible
- CP is clock input for shifting
- Clock inhibit input
- Shift load input

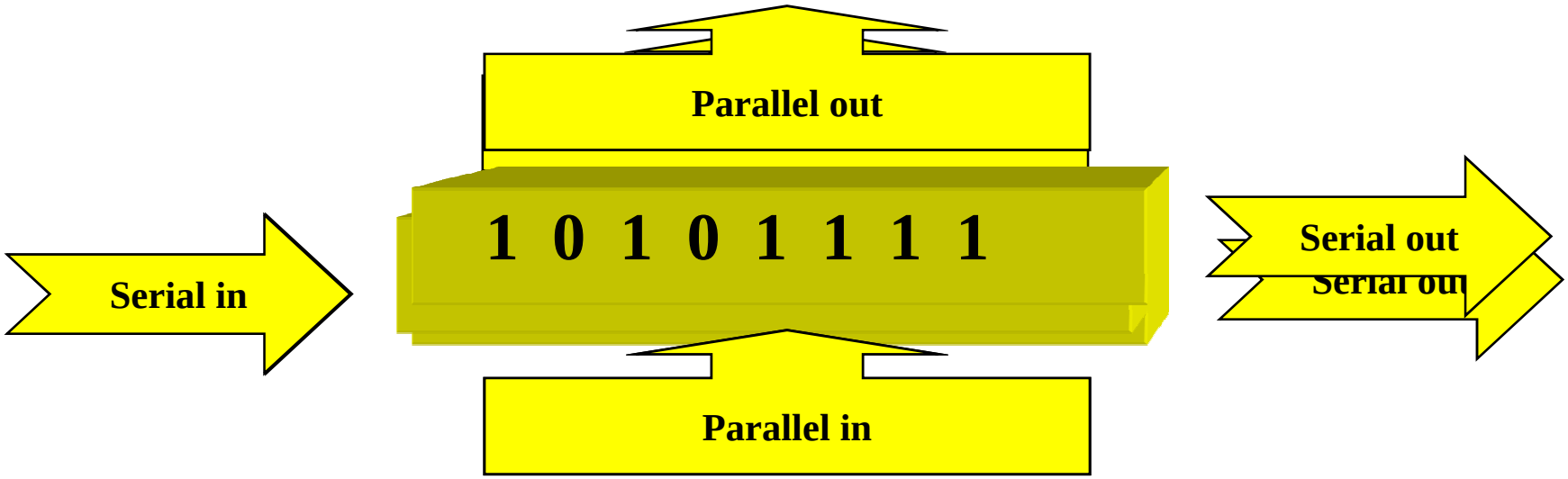
SIPO – The 74ALS164/74HC164

- Refer to Figure 7-53
  - 8 bit shift register
  - Each FF output is externally accessible
- Shift occurs on NGT of the clock input.

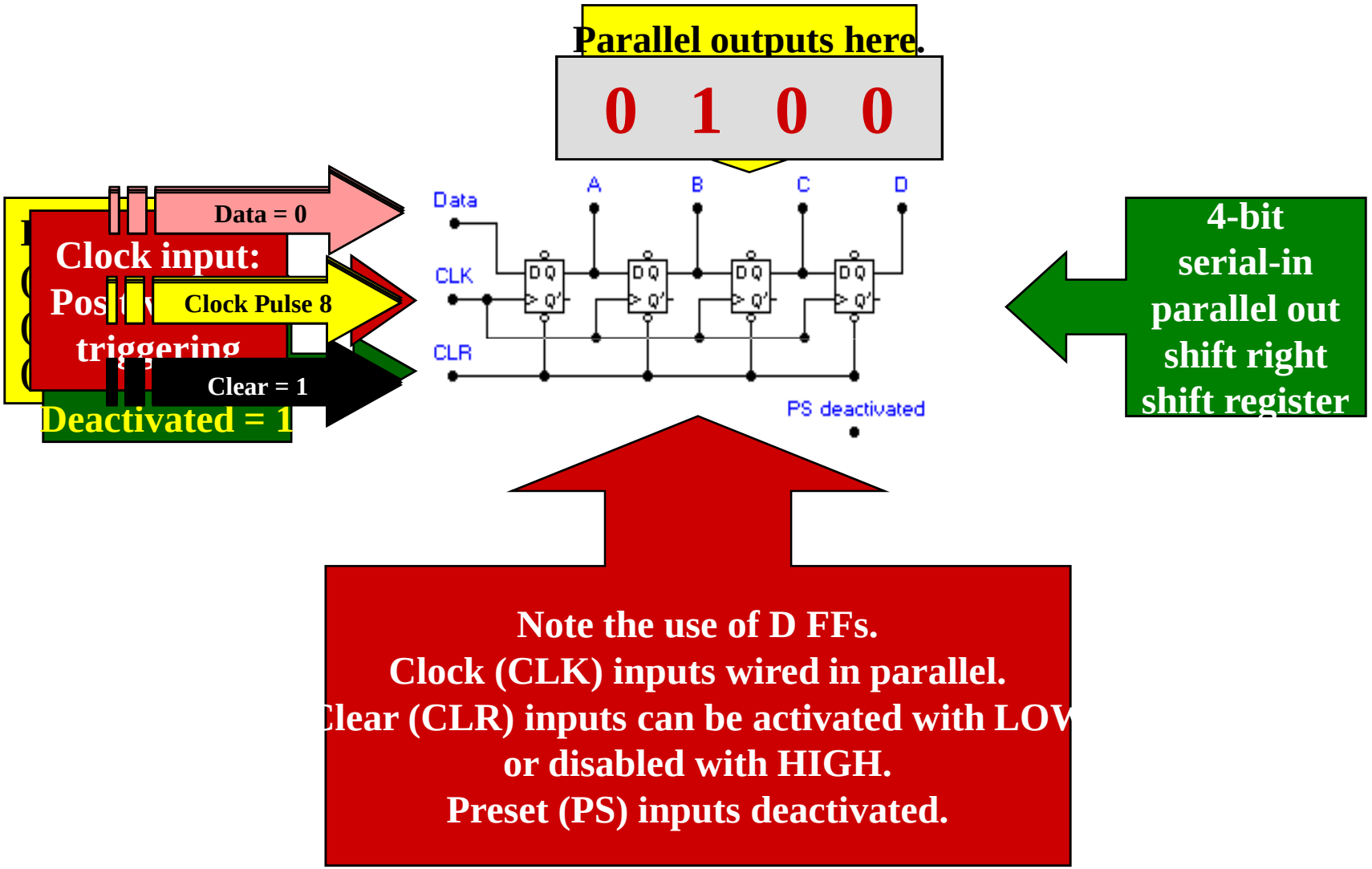
- Other similar devices
  - 74194/ASL194/HC194
    - 4 bit bi-directional universal shift register
    - Performs shift left, shift right, parallel in and parallel out.
  - 74373/ALS373/HC373/HCT373
    - 8 bit PIPO with 8 D latches
    - Tristate outputs
  - 74374/ALS374/HC374
    - 8 bit PIPO with 8 edge triggered D FFs
    - Tristate outputs

SERIAL/PARALLEL DATA CONVERSION

Shift registers can be used to convert from serial-to-parallel or the reverse from parallel-to-serial.



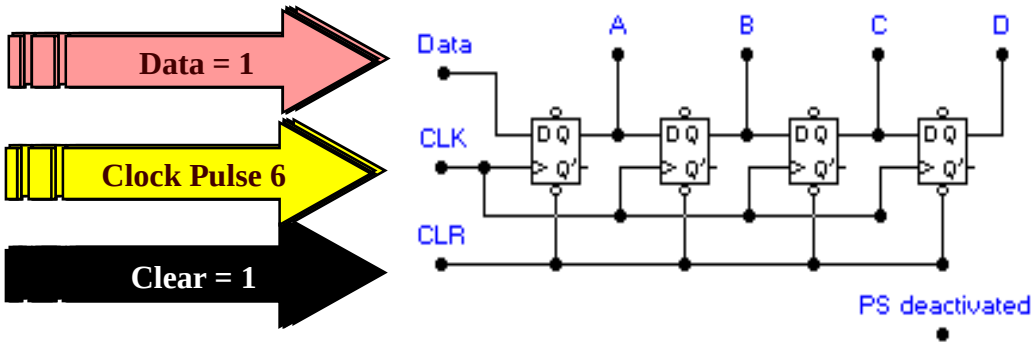
SERIAL LOAD SHIFT REGISTER



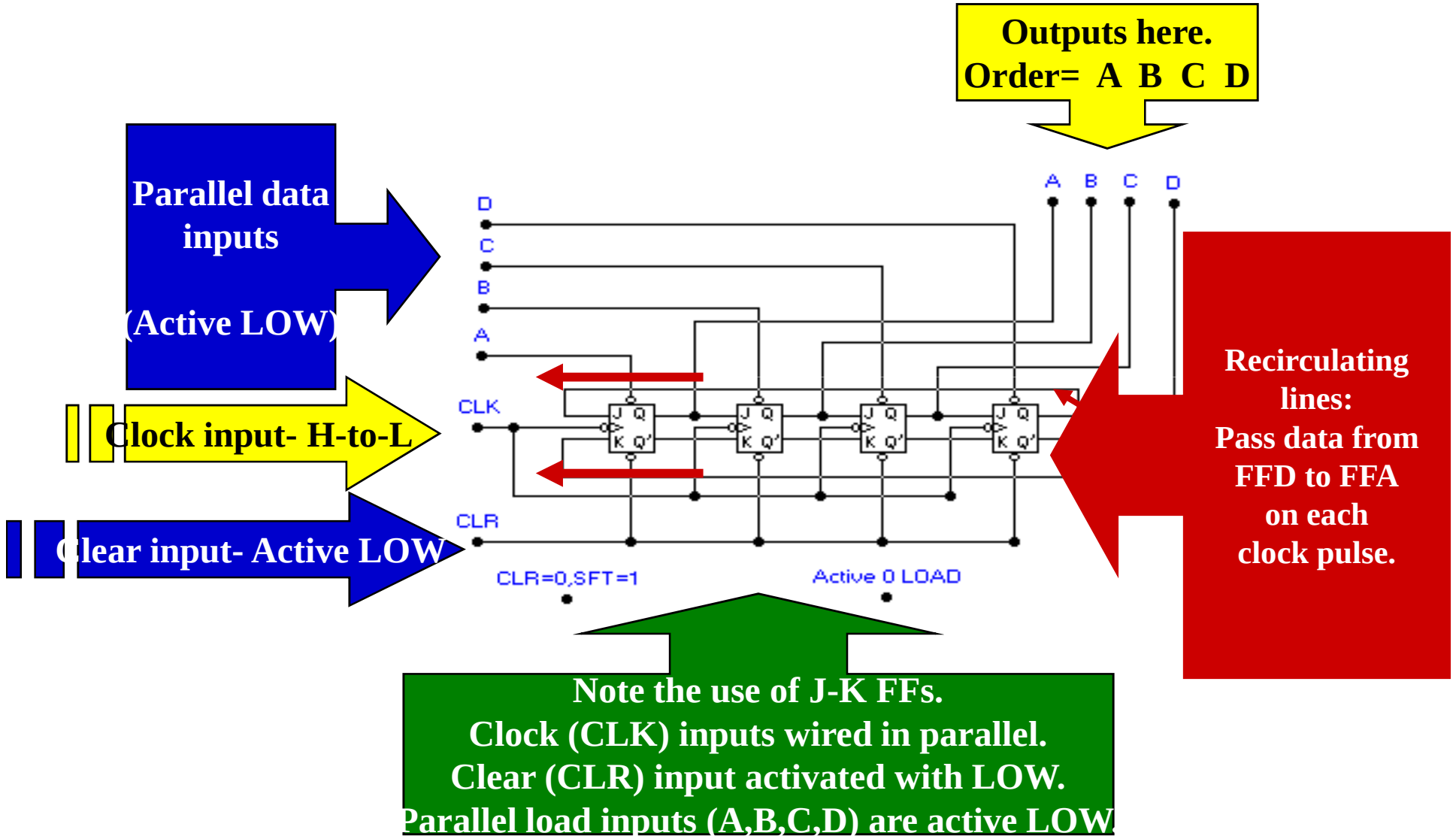
QUESTION #7

What is the 4-bit output (bit A on left, D on right) after pulse 6?

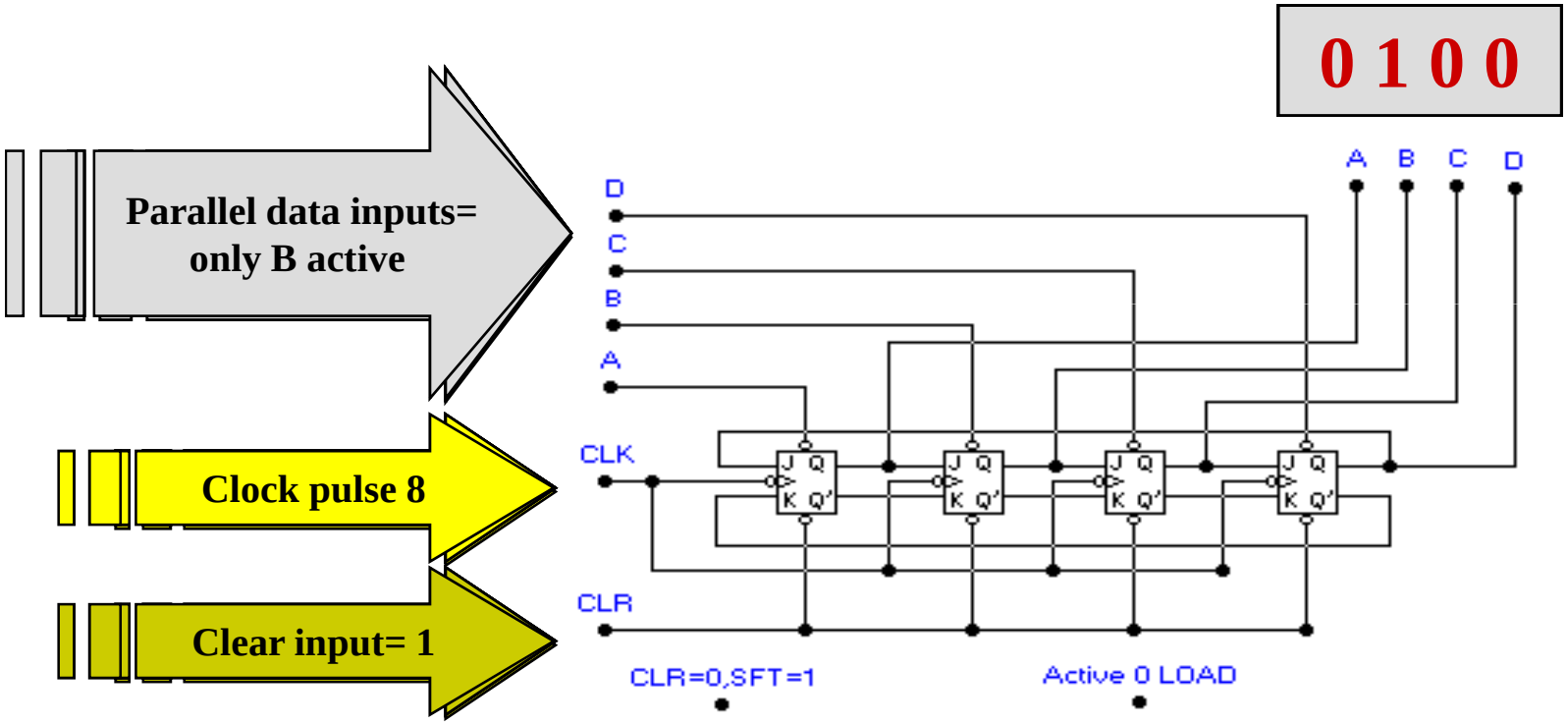
A: 1100



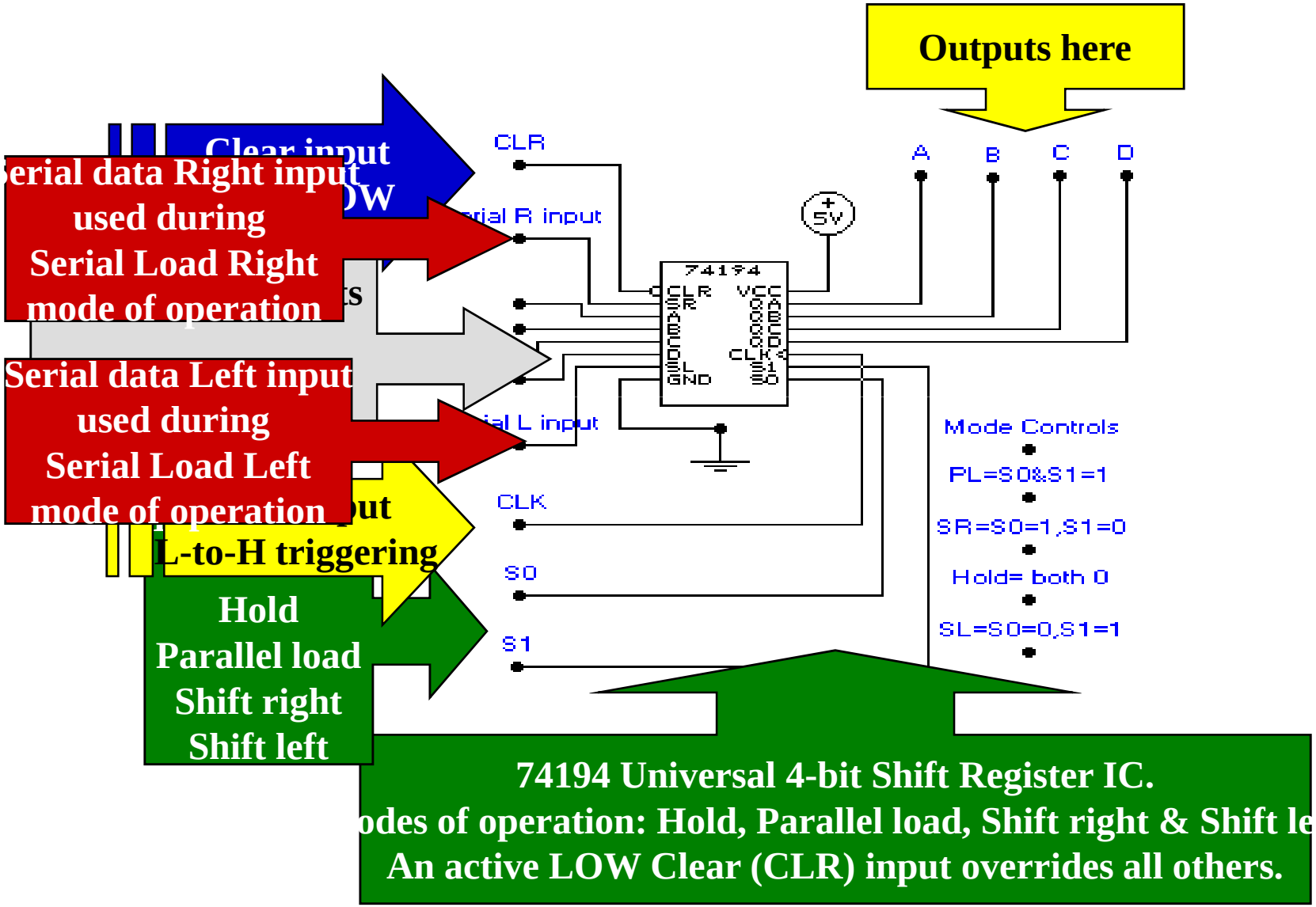
PARALLEL LOAD SHIFT REGISTER



RECIRCULATING SHIFT REGISTER



UNIVERSAL SHIFT REGISTER IC



USING THE 74194 SHIFT REGISTER IC

CLR = 1

Serial R = X

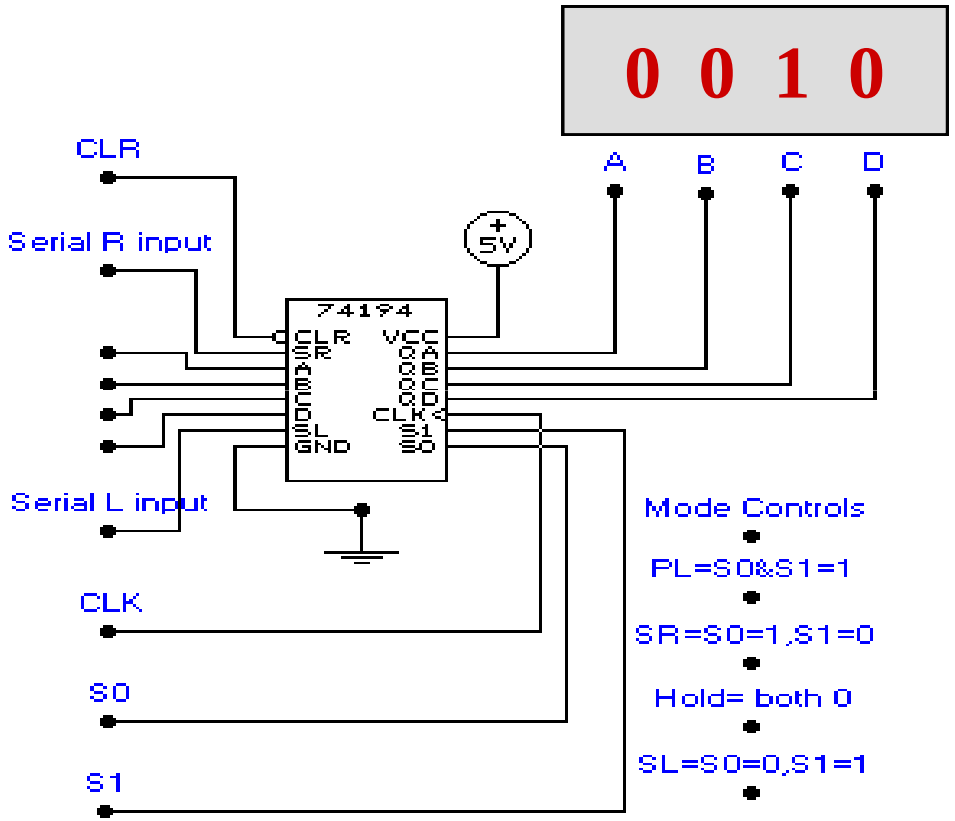
Parallel Load= 0 1 0 0

Serial L = 0

Clock pulse 8 (L-to-H)

S0= 0

S1= 1



X = Irrelevant

Homework

7-67 of T1(10th edition)

QUESTION #7

What is the mode of operation during and the output of the shift register after pulse 6?

A: Shift left, 1 0 1 1

CLR = 1

Serial R = X

Parallel Load= 0 1 0 0

Serial L = 1

Clock pulse 6 (L-to-H)

S0= 0

S1= 1