BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus

Second Semester 2012-2013

IS F242 Computer Organization

Lab – 3, 26th February 2013

Design and implement the following using verilog HDL in **Xilinx software** with the following specifications.

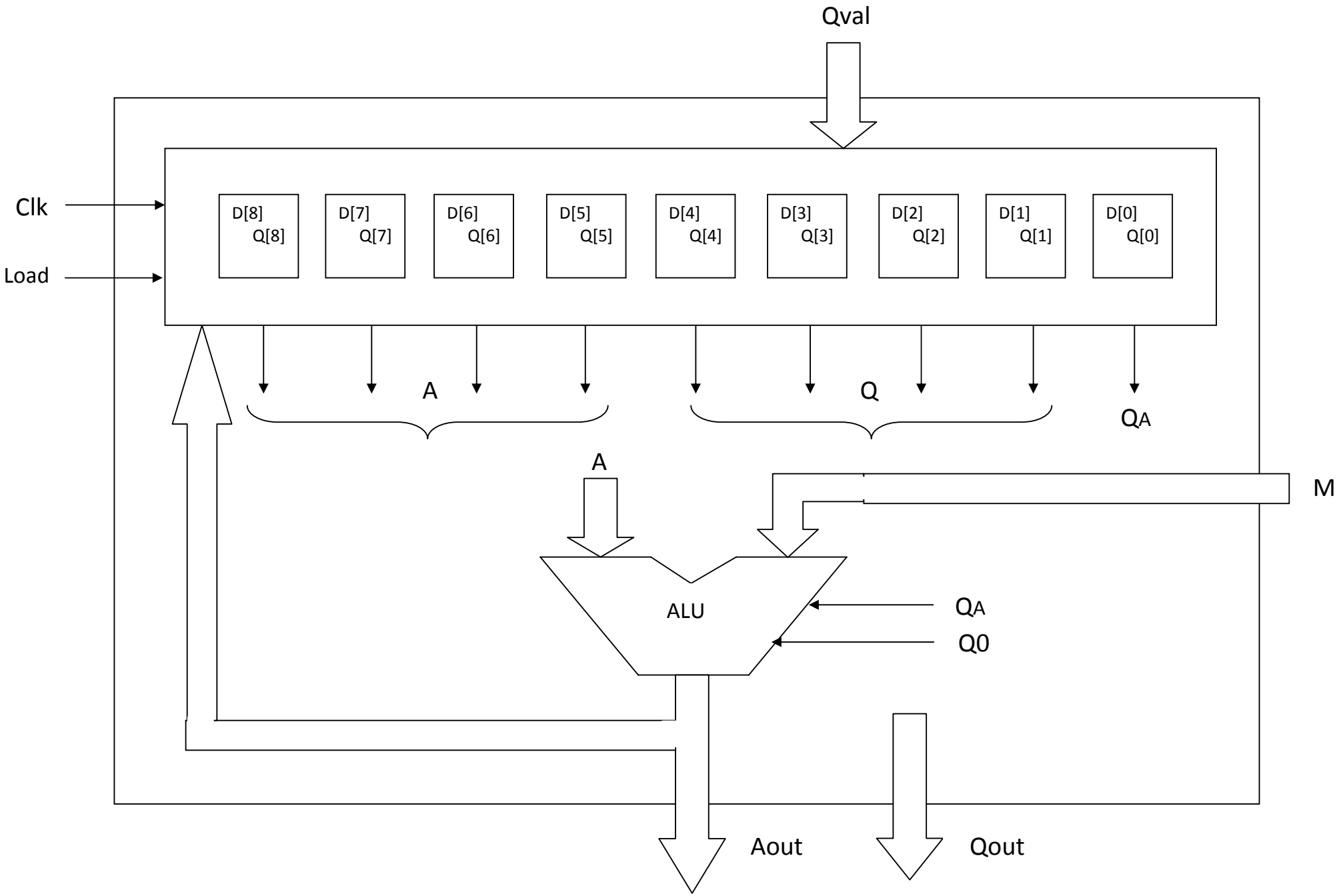
module DFF(input D, output reg Q);

module RShiftReg(input Clk, input Load, input [3:0] Qval, input [3:0] Res, output [8:0] Q);

module Adder(input Ctrl0, input Ctrl1, input [3:0] A, input [3:0] M, output reg [3:0] Out);

module BoothMul(input Clk, input Load, input [3:0] Qval, input [3:0] M, output reg [3:0] Qout, output reg [3:0] Aout);

module testben;


Qval
Clk
Load
D[8]
Q[8]
D[7]
Q[7]
D[6]
Q[6]
D[5]
Q[5]
D[4]
Q[4]
D[3]
Q[3]
D[2]
Q[2]
D[1]
Q[1]
D[0]
Q[0]
A
Q
QA
A
M
ALU
QA
Q0
Aout
Qout