Digital Electronics and Microprocessors

Class 14

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Overview of sequential circuits

- Chapter 5
- ✓ NAND gate Latch, NOR gate latch
- ✓ Digital pulses , clock signals, clocked f/f(SR,JK,D,T) Gated latches (D,SR,JK)
- ✓ Asynchronous inputs
- ✓ **Flip-Flop Timing Consideration, potential timing problems in FF ckts**
- ✓ Master/slave ff
- ✓ Analyzing Sequential Circuits
- ✓ Flip-Flop Applications (Data storage and transfer, serial data transfer: shift registers, frequency division and counting) Flip-Flop synchronization reading assignment for you

Overview of sequential circuits

- **Chapter 7**
- **Part-I**

✓ Asynchronous(Ripple Counters), IC asynchronous counters (74LS293, 7493(used in lab),mod16, mod 10 ripple and any other lower mod counter by giving ff outputs to master reset, and higher mod counter by cascading of these IC.

✓ Asynchronous down counter (by giving complement o/p of previous f/f to clock input of next flip flop)

✓ Synchronous (Parallel) counters:- analysis of counters, counters with mod number $< 2^N$ (Using Nand Gate whose o/p is used to clear all flip/flops at certain count) ,design of a counter (full sequence counter, up down full sequence counter, irregular sequence counter, truncated counters, gray code counters)using design procedures. Unused states in counters other than full sequence counters can have next state as Don't care or can be any other valid state(self correcting).

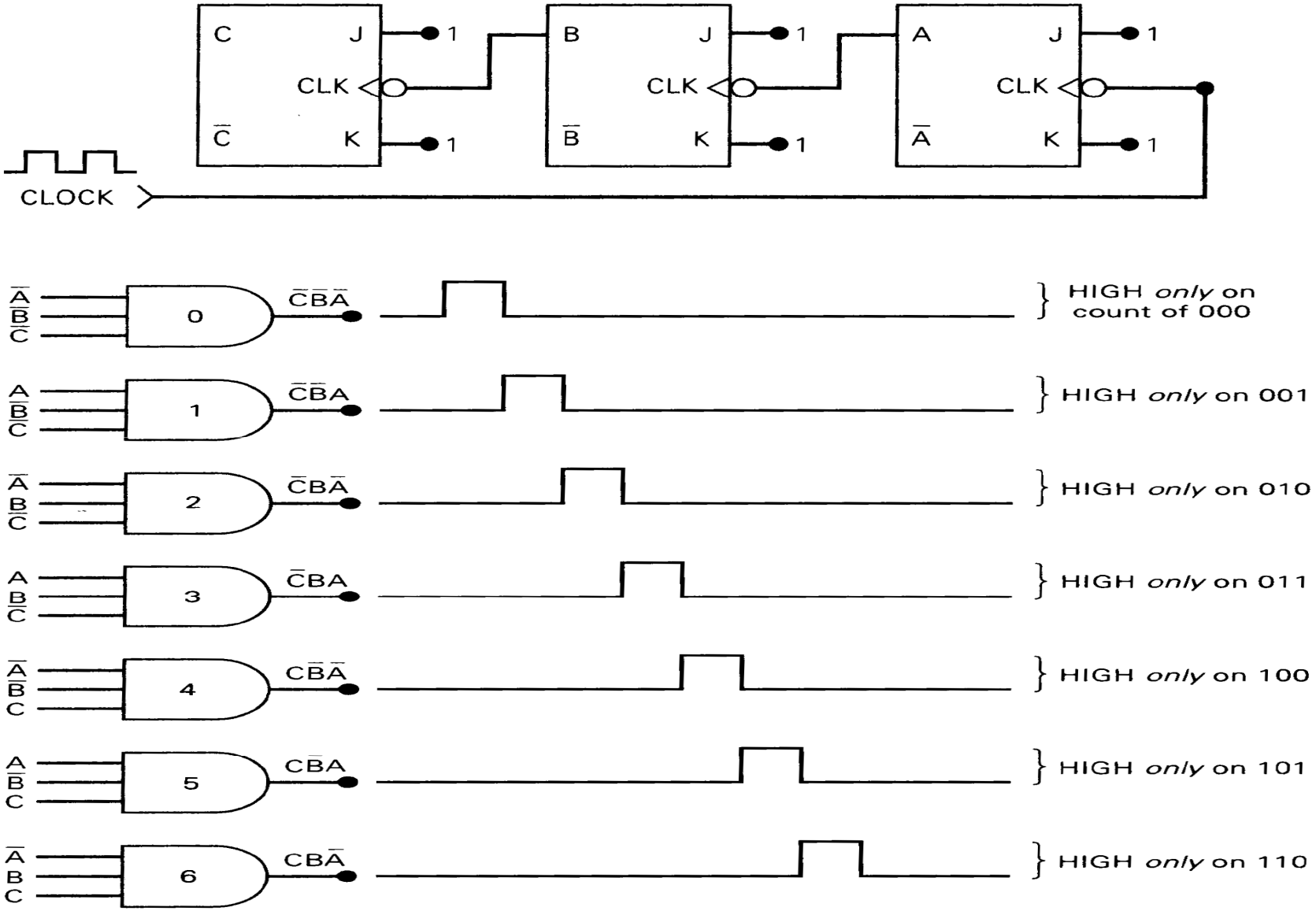
✓ 7-9 ofT1 10th edition IC synchronous counters (Don't read)

✓ Decoding of a counter (will be covered in next slides)

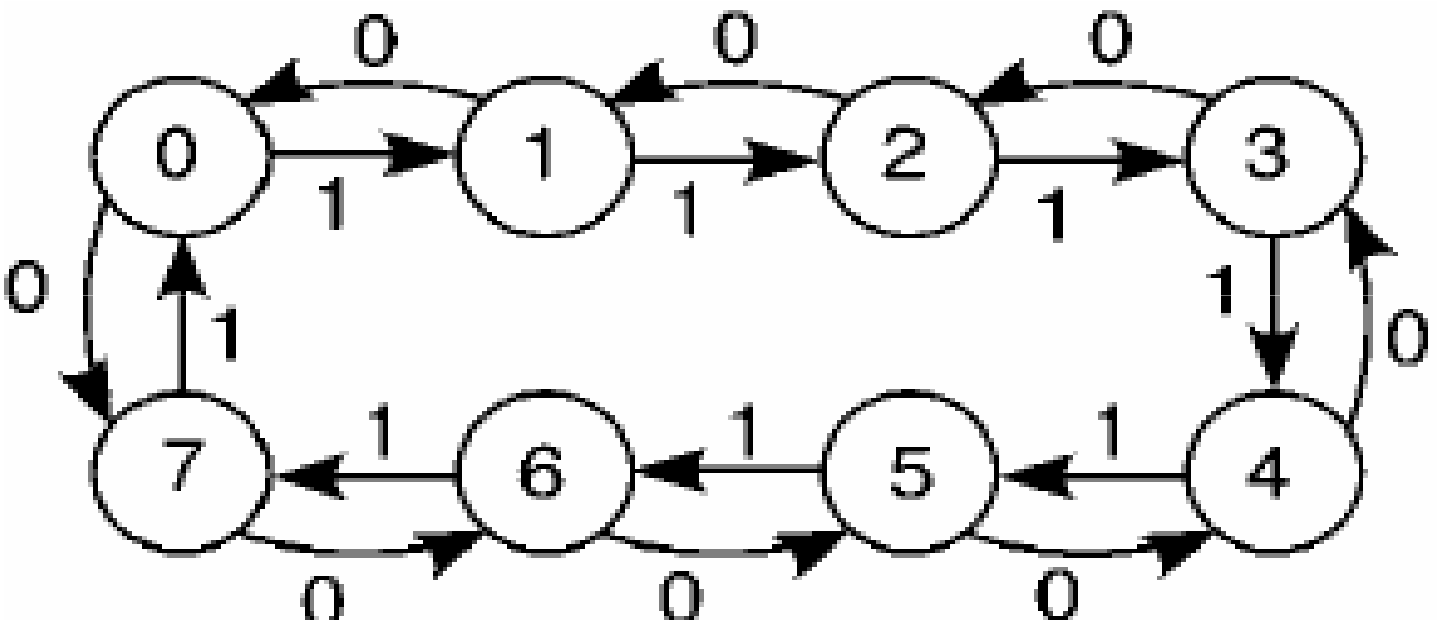
Overview of sequential circuits

- **Chapter 7**
- **Part-II** IC registers
- ✓ (understanding the concept of serial loading and parallel loading of a register)
- ✓ IC registers (PIPO 74ALS174,SISO 74ALS166,PISO 74ALS165, SIPO 74ALS164, Universal shift register of type PIPO 74194)
- ✓ Shift register counters (Ring and Johnsan), design these using design procedure (state table, state diagram , excitation table, Input equations, final circuit diagram)
- ✓ Ring and Johnsan counter using shift registers

Decoding of a counter



- State diagram



Present State	Next State	F.F. Input
Q(*t*)	*Q*(*t*+1)	*D*
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	F.F. Input	
Q(*t*)	*Q*(*t*+1)	*J*	*K*
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

0 0 (No change)
0 1 (Reset)

1 0 (Set)
1 1 (Toggle)

0 1 (Reset)
1 1 (Toggle)

0 0 (No change)
1 0 (Set)

Q(*t*)	*Q*(*t*+1)	*T*
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table

Present state			Mode	Next state			Required inputs					
Q3	Q2	Q1	M	Q3	Q2	Q1	J3	K3	J2	K2	J1	K1
0	**0**	**0**	**0**	**1**	1	1	**1**	**X**	1	X	1	X
0	0	0	1	0	0	1	0	X	0	X	1	X
0	0	1	0	0	0	0	0	X	0	X	X	1
0	0	1	1	0	1	0	0	X	1	X	X	1
0	1	0	0	0	0	1	0	X	X	1	1	X
0	1	0	1	0	1	1	0	X	X	0	1	X
0	1	1	0	0	1	0	0	X	X	0	X	1
0	1	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	1	1	X	1	1	X	1	X
1	0	0	1	1	0	1	X	0	0	X	1	X
1	0	1	0	1	0	0	X	0	0	X	X	1
1	0	1	1	1	1	0	X	0	1	X	X	1
1	1	0	0	1	0	1	X	0	X	1	1	X
1	1	0	1	1	1	1	X	0	X	0	1	X
1	1	1	0	1	1	0	X	0	X	0	X	1
1	1	1	1	0	0	0	X	1	X	1	X	1

* PS=Present state *NS= Next state

Present State	Next State	F.F. Input	
Q(*t*)	*Q*(*t*+1)	*J*	*K*
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Q3(PS)Q3(NS) = 01 then from excitation table of JK flip flop J3K3 should be 1X(J3=1 K3=X)
Q2(PS)Q2(NS)= 01 then from excitation table of JK flip flop J2K2 should be 1X(J2=1 K2=X)
Similarly fill all the rows of excitation inputs for all states of counter

K-maps for excitations of synchronous 3 bit U/D counter

Q1M

Q3Q2				
	1			
			1	
	X	X	X	X
	X	X	X	X

J3=Q2’Q1’M’+Q2Q1M

Q1M

Q3Q2				
	X	X	X	X
	X	X	X	X
			1	
	1			

K3=Q2’Q1’M’+Q2Q1M

Q1M

Q3Q2				
	1		1	
	X	X	X	X
	X	X	X	X
	1		1	

J2=Q1’M’+Q1M

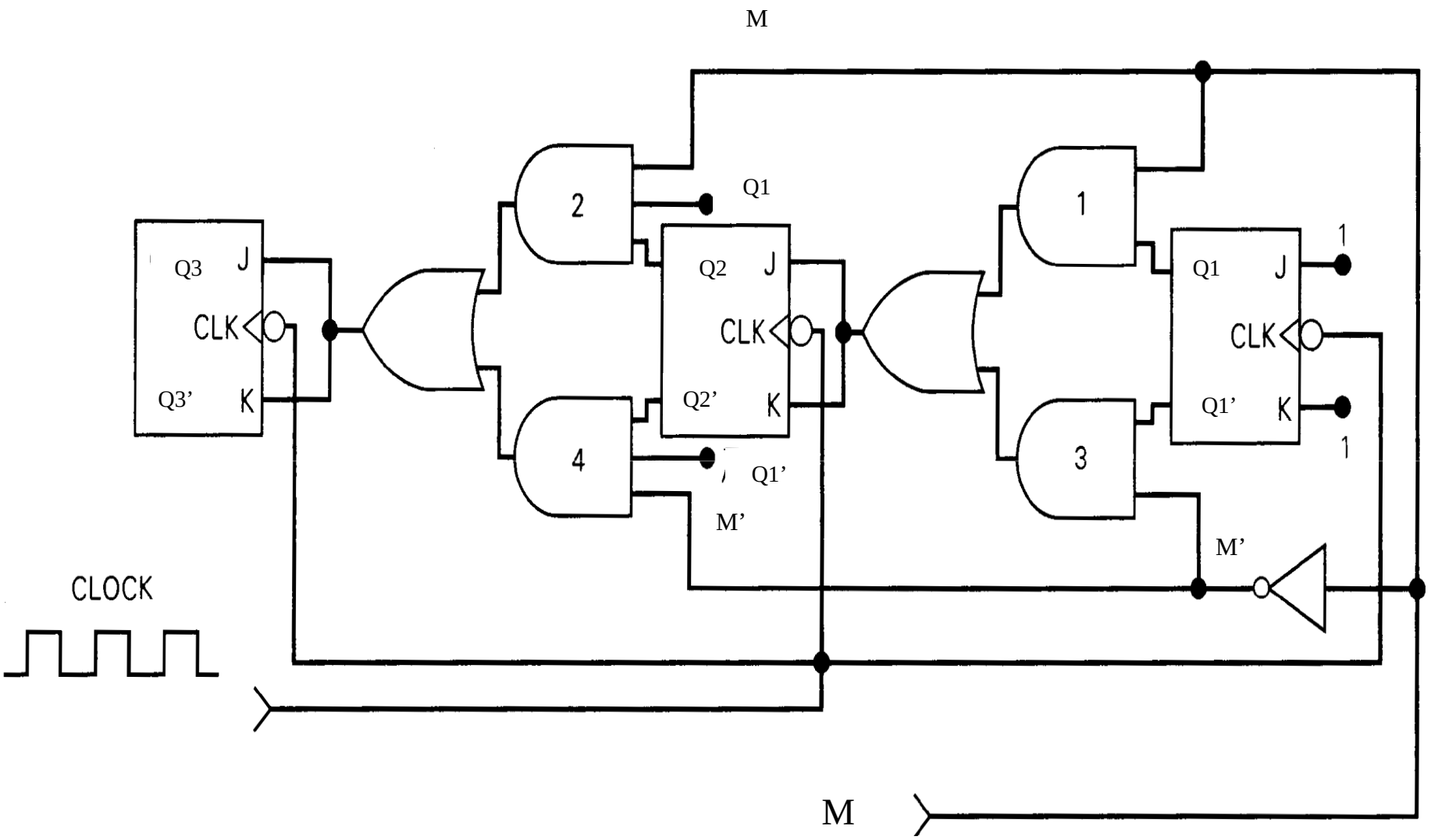
J1=1

Q1M

Q3Q2				
	X	X	X	X
	1		1	
	1		1	
	X	X	X	X

K2=Q1’M’+Q1M

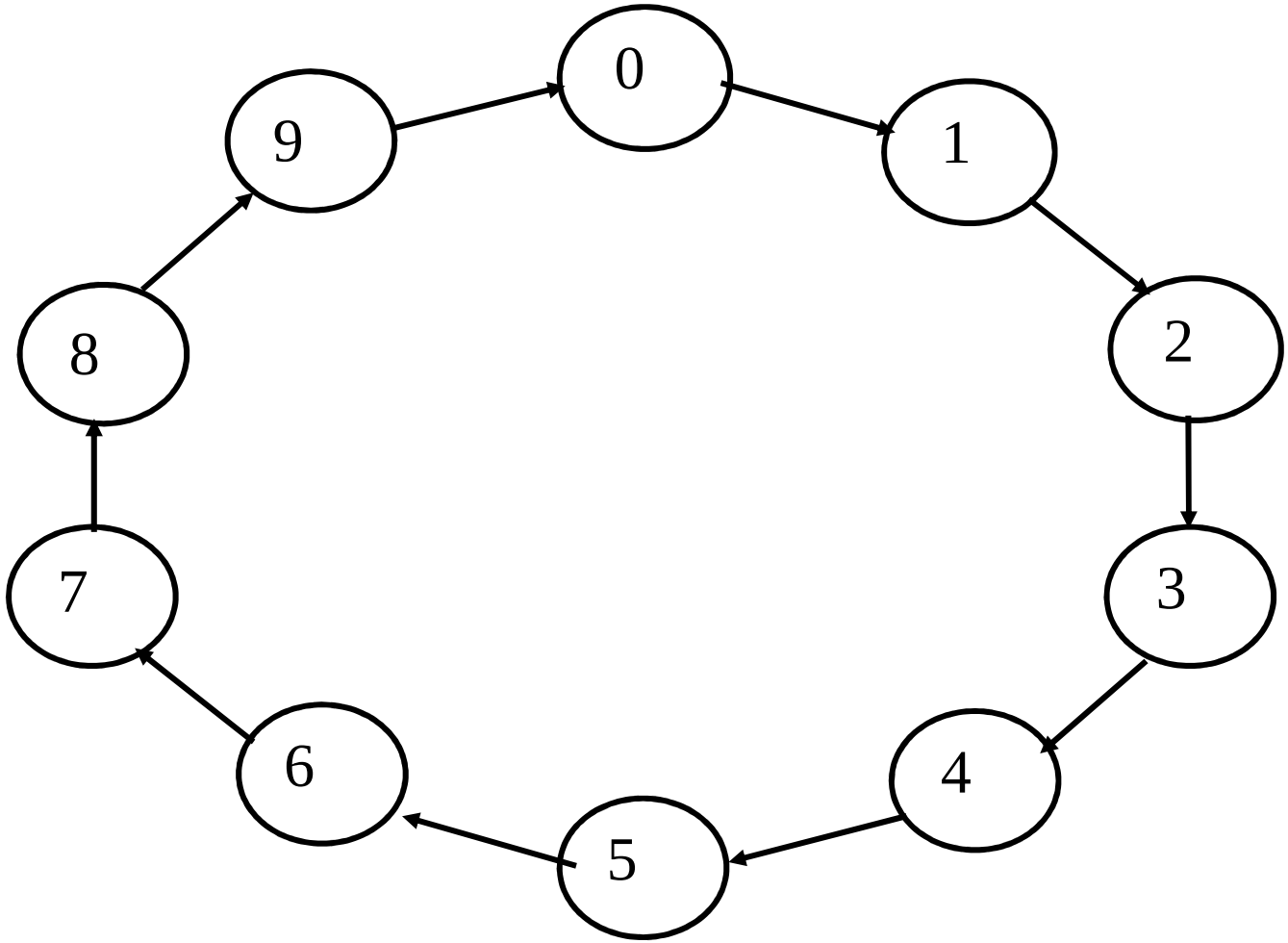
k1=1


M
Q3
J
CLK
Q3'
K
2
Q1
Q2
J
CLK
Q2'
K
4
Q1'
M'
1
Q1
J
CLK
Q1'
K
1
1
3
M'
CLOCK
M

Design of a synchronous BCD counter using JK flip-flops

- Number of flip flops
- State diagram
- Type of flip flop and excitation table
- Minimal expression
- Logic diagram

State diagram



Excitation table

Present state				Next state				Required inputs							
Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1	J4	K4	J3	K3	J2	K2	J1	K1
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Present states	Next States				Required Inputs							
1010	X	X	X	X	X	X	X	X	X	X	X	X
1011	X	X	X	X	X	X	X	X	X	X	X	X
1100	X	X	X	X	X	X	X	X	X	X	X	X
1101	X	X	X	X	X	X	X	X	X	X	X	X
1110	X	X	X	X	X	X	X	X	X	X	X	X
1111	X	X	X	X	X	X	X	X	X	X	X	X

K-maps for excitations of synchronous BCD counter

Q4Q3 \ Q2Q1				
			1	
	X	X	X	X
	X	X	X	X

J4=Q3Q2Q1

Q4Q3 \ Q2Q1				
	X	X	X	X
	X	X	X	X
	X	X	X	X
		1	X	X

K4=Q1

Q4Q3 \ Q2Q1			1	
	X	X	X	X
	X	X	X	X
			X	X

J3=Q2Q1

Q4Q3 \ Q2Q1				
	X	X	X	X
			1	
	X	X	X	X
	X	X	X	X

K3=Q2Q1

K-maps for excitations of synchronous 3 bit U/D counter

Q2Q1

Q4Q3				
	1	X	X
	1	X	X
X	X	X	X
		X	X

J2=Q4’Q1

J1=1

Q2Q1

Q4Q3				
	X	X	X	X
	X	X	X	X
	X	X	X	X
		1	X	X

K2=Q1

k1=1

Homework

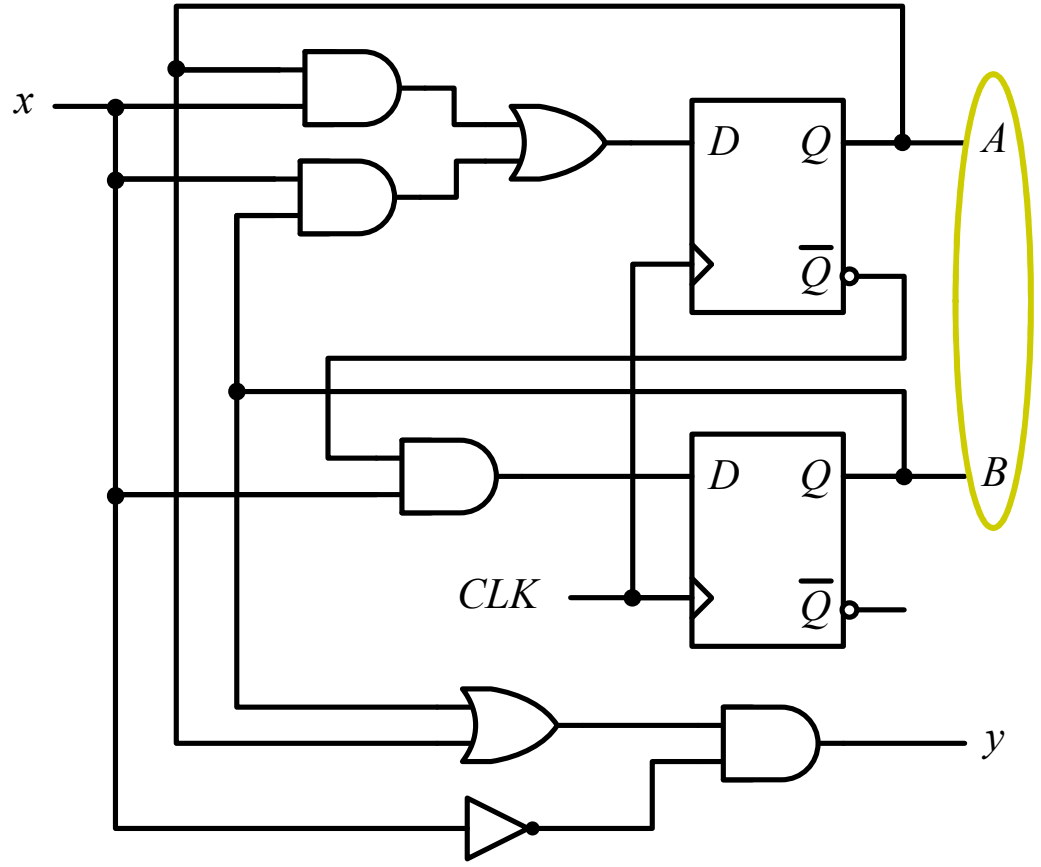
Design a counter(using JK and D) that goes to states 0,1,2,4,0,1,2,4----- the undesired state must always go to 0

Analysis of Clocked Sequential Circuits

- The State
  - State = Values of all Flip-Flops

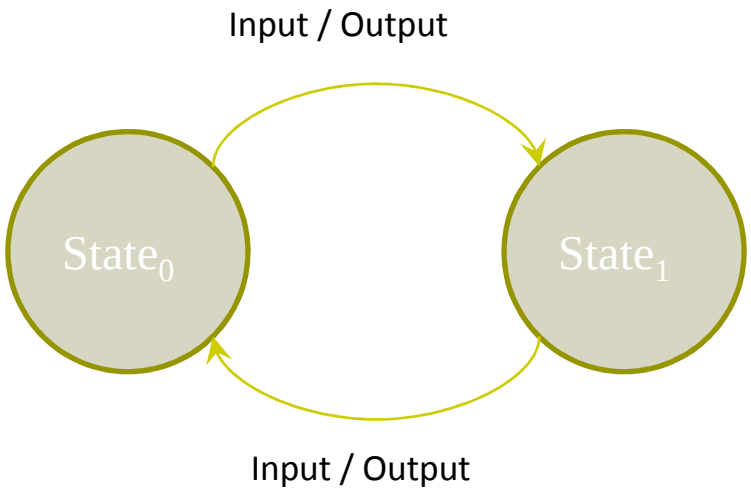
Example

$A\ B = 0\ 0$

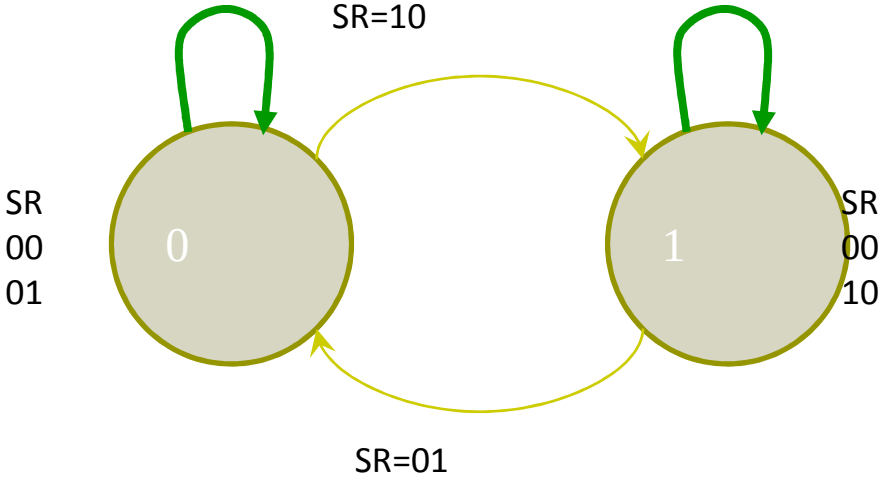


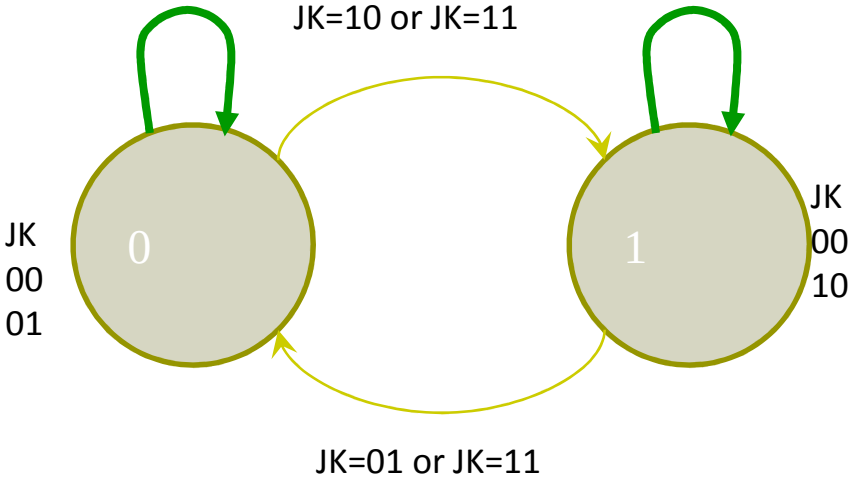
Representing a Finite State Machine

- It can also be represented using a state diagram which has the same information as the state transition diagram.



Flip-Flops as Finite state machines

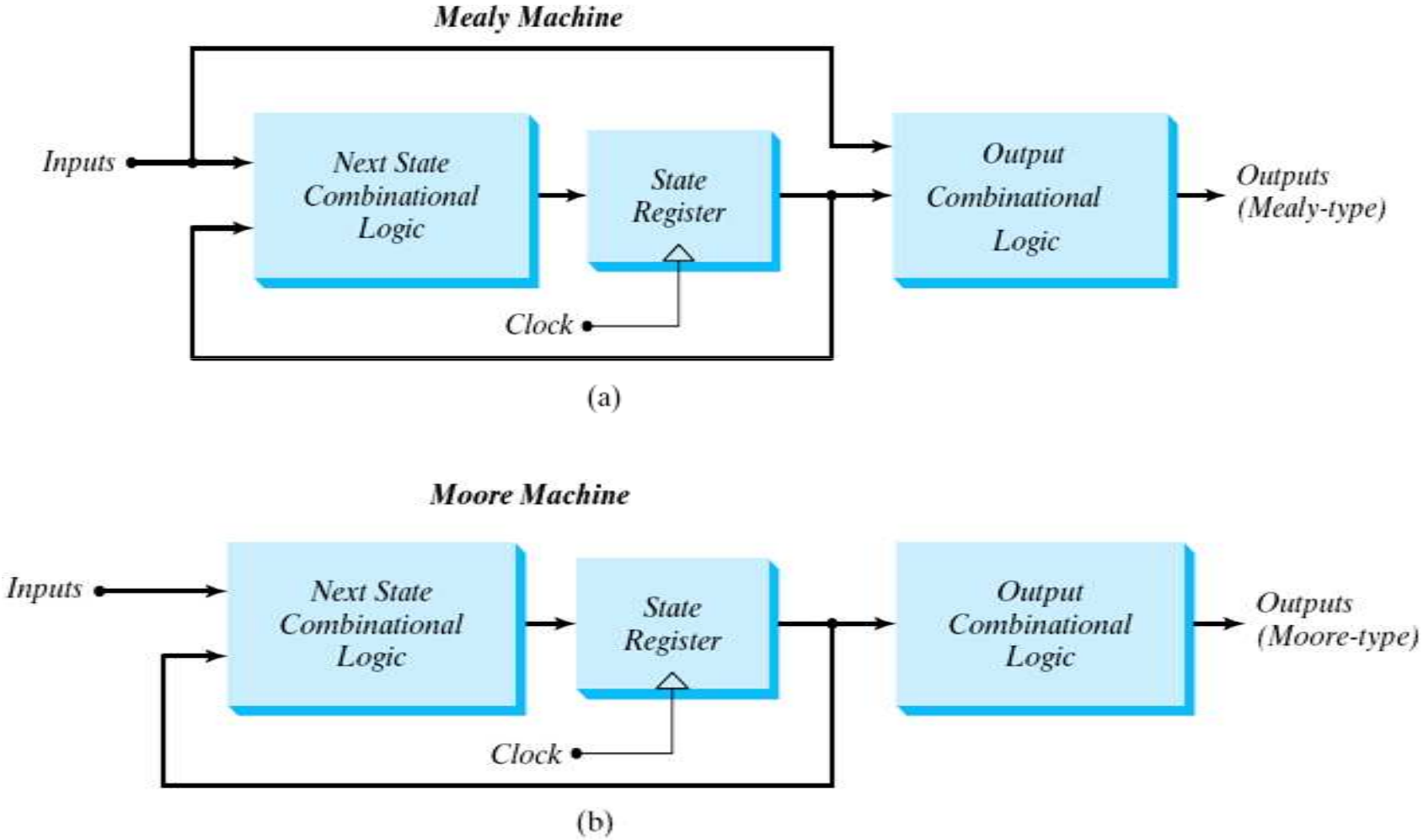




FSM models Mealy and Moore Models

- The Mealy model: the outputs are functions of both the present state and inputs .
  - The outputs may change if the inputs change during the clock pulse period.
- The Moore model: the outputs are functions of the present state only .
  - The outputs are synchronous with the clocks.

Mealy and Moore Models

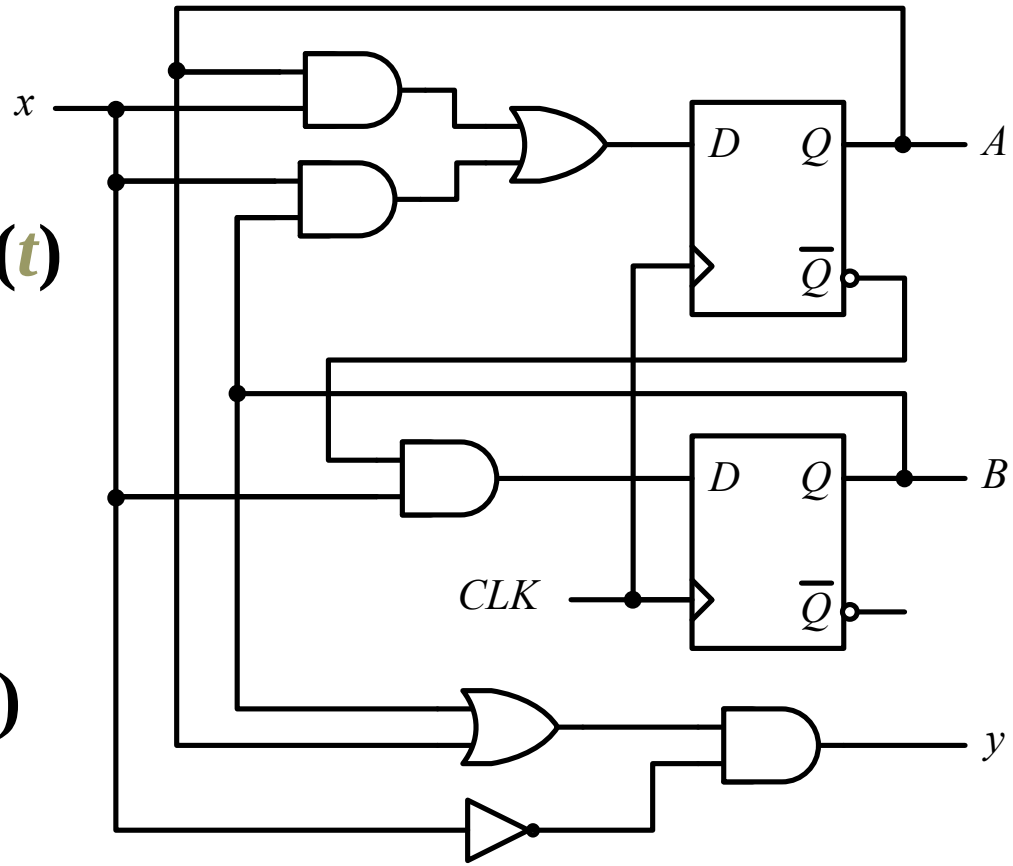


Block diagram of Mealy and Moore state machine

Analysis of Clocked Sequential Circuits

- State Equations

$$A(t+1) = D_A$$
$$= A(t)\,x(t) + B(t)\,x(t)$$
$$= A\,x + B\,x$$
$$B(t+1) = D_B$$
$$= A'(t)\,x(t)$$
$$= A'\,x$$
$$y(t) = [A(t) + B(t)]\,x'(t)$$
$$= (A + B)\,x'$$

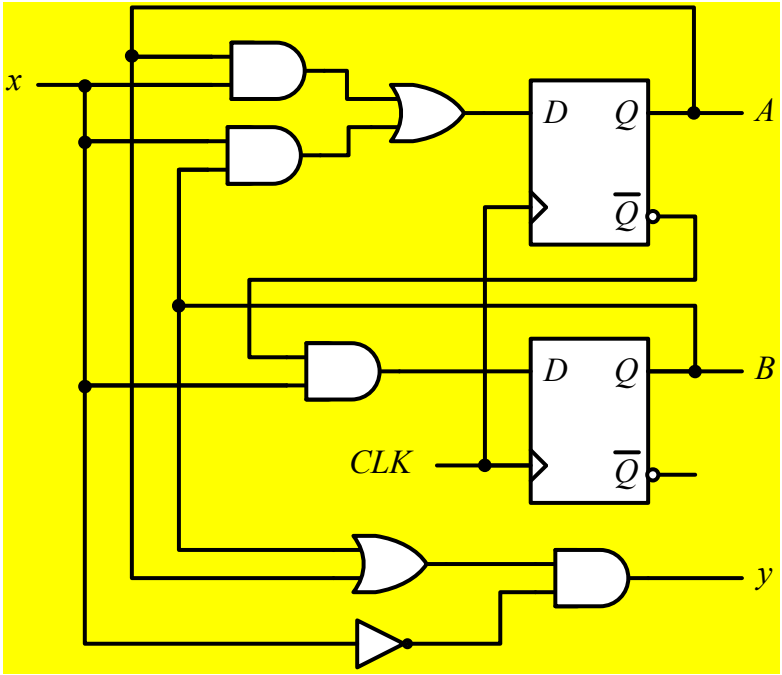


Analysis of Clocked Sequential Circuits

- State Table (Transition Table)

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

t *t*+1 *t*



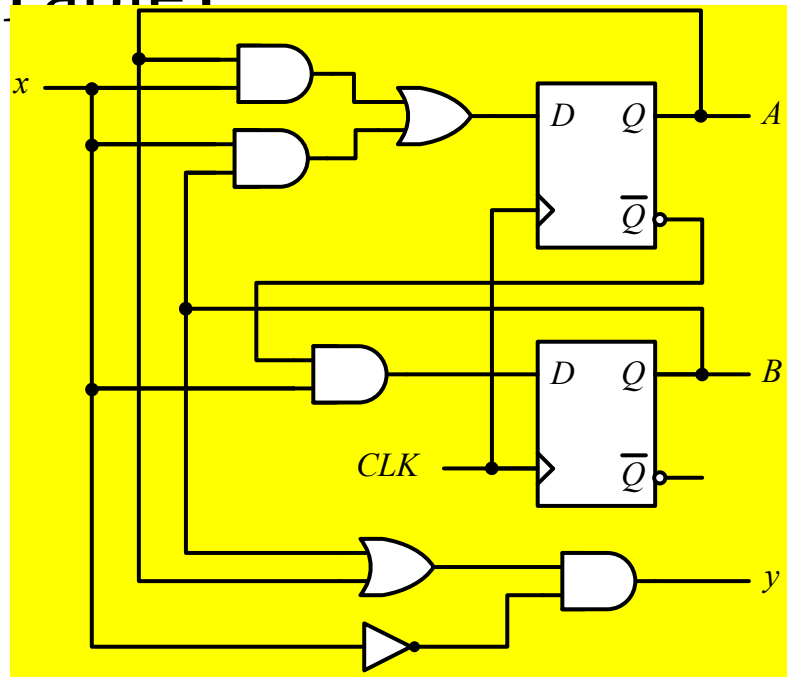
$$A(t+1) = A\,x + B\,x$$
$$B(t+1) = A'\,x$$
$$y(t) = (A + B)\,x'$$

Analysis of Clocked Sequential Circuits

- State Table (Transition Table)

Present State	Next State				Output	
	$x = 0$		$x = 1$		$x = 0$	$x = 1$
A B	A	B	A	B	y	y
0 0	0	0	0	1	0	0
0 1	0	0	1	1	1	0
1 0	0	0	1	0	1	0
1 1	0	0	1	0	1	0

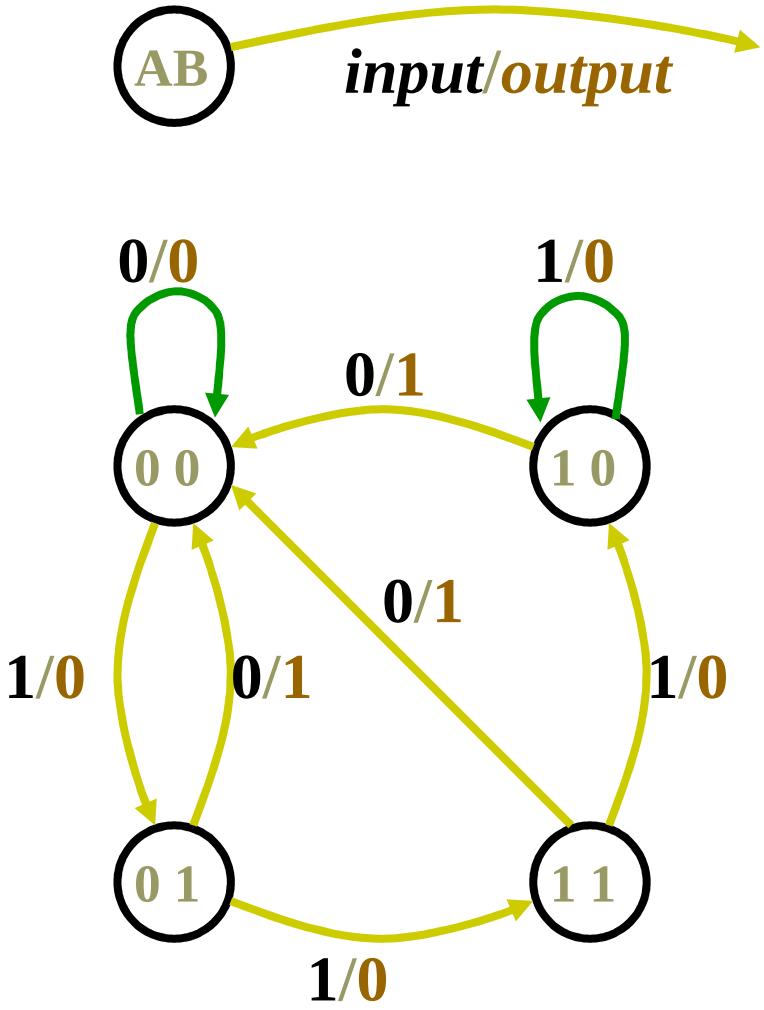
t $t+1$ t



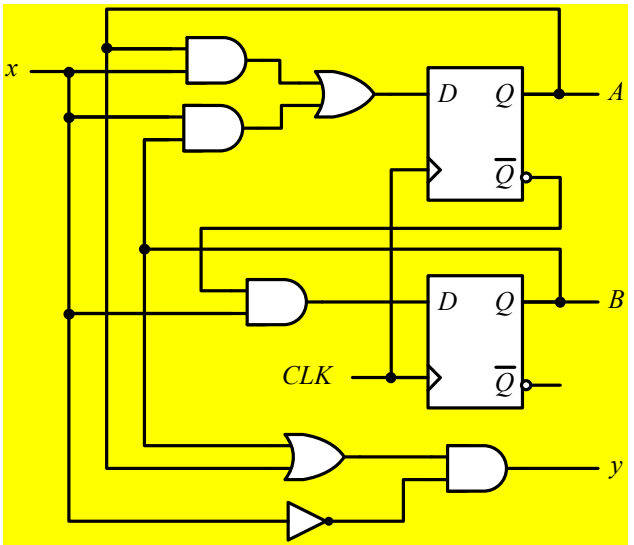
$$A(t+1) = A\,x + B\,x$$
$$B(t+1) = A'\,x$$
$$y(t) = (A + B)\,x'$$

Analysis of Clocked Sequential Circuits

- State Diagram



Present State	Next State				Output	
	$x = 0$		$x = 1$		$x = 0$	$x = 1$
A B	A	B	A	B	y	y
0 0	0	0	0	1	0	0
0 1	0	0	1	1	1	0
1 0	0	0	1	0	1	0
1 1	0	0	1	0	1	0



Analysis of synchronous counter (Refer 7-13)