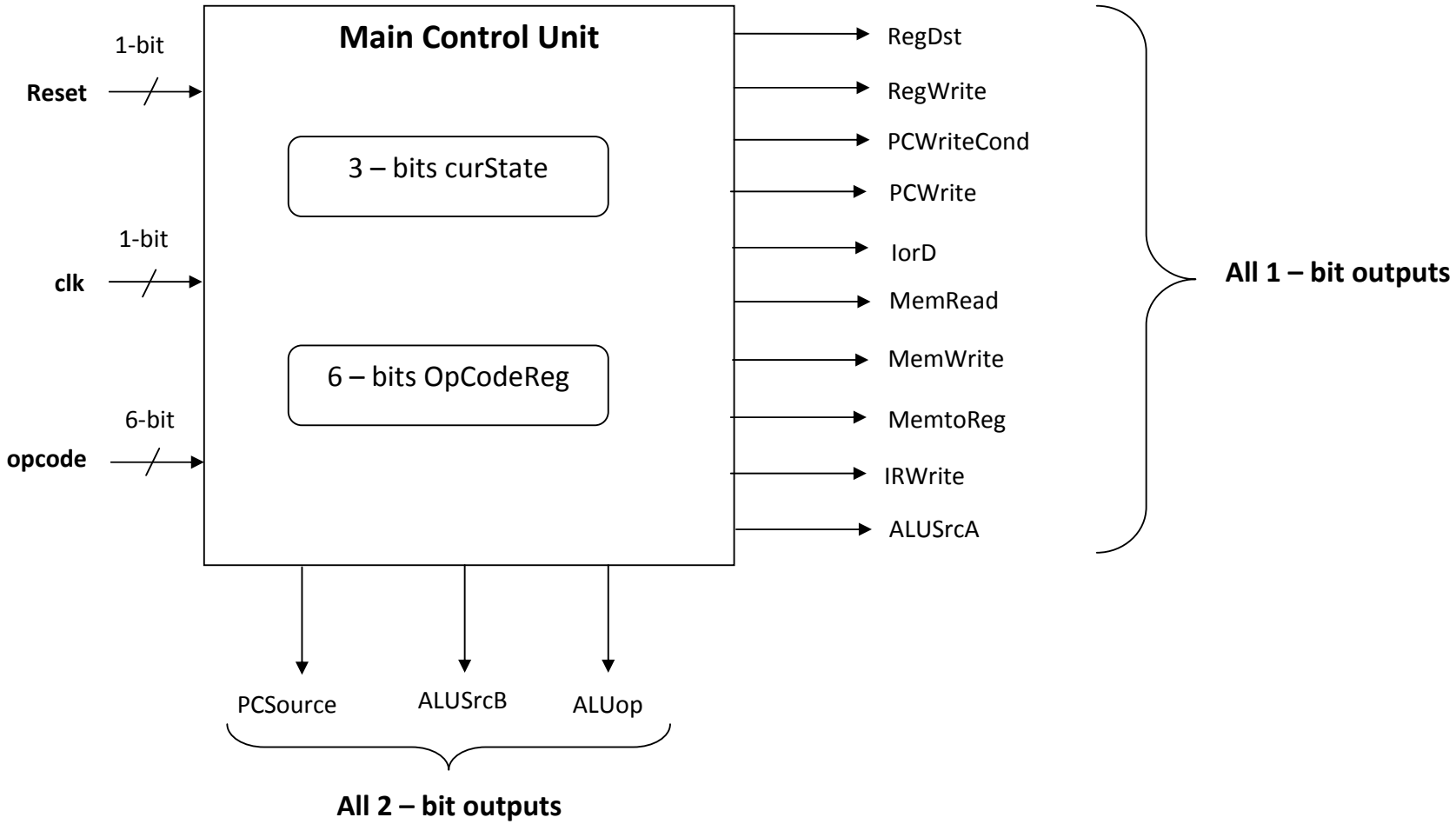
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
Second Semester 2012-2013
IS F242 Computer Organization
Lab – 5, 2nd April 2013

Design and implement the following using verilog HDL in Xilinx software with the following specifications.



Modules

1. module CtrlUnit (input clk, input Reset, input [5:0] opcode, output reg RegDst, output reg RegWrite, output reg PCWriteCond, output reg PCWrite, output reg IorD, output reg MemRead, output reg MemWrite, output reg MemtoReg, output reg IRWrite, output reg ALUSrcA, output reg [1:0] PCSource, output reg [1:0] ALUSrcB, output reg [1:0] ALUop);

2. TestBench;

Opcode for the instructions

ADD : opcode=0x00
SUB : opcode=0x00
BEQ : opcode=0x04
J : opcode=0x02
LW : opcode=0x23
SW : opcode=0x2b

```
At neg edge of the clock
        if Reset = 1
                curState = 3'b000
                All outputs are 0
        Else
                If curState = 3'b000
                        OpCodeReg=opcode
                        All outputs are set accordingly
                        curState = 3'b001
                Else if curState = 3'b001
                        All outputs are set accordingly
                        curState = 3'b010
                Else if curState = 3'b010
                        Depending on the opcode in OpCodeReg set outputs
                        Depending on the opcode in OpCodeReg set curState as 3'b011 or 3'b000
                Else if curState = 3'b011
                        Depending on the opcode in OpCodeReg set outputs
                        Depending on the opcode in OpCodeReg set curState as 3'b100 or 3'b000
                Else if curState = 3'b100
                        All outputs are set accordingly
                        curState = 3'b000
```

	Cycle	RegDst	RegWrite	PCSource	PCWriteCond	PCWrite	IorD	MemRead	MemWrite	MemtoReg	IRWrite	ALUSrcA	ALUSrcB	ALUop
ADD	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**
	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
	3	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**2**
	4	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**2**
SUB	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**
	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
	3	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**2**
	4	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**2**
BEQ	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**
	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
	3	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**
J	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**
	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
	3	**0**	**0**	**2**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
SW	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**
	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
	3	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**2**	**0**
	4	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**2**	**0**
LW	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**
	2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**3**	**0**
	3	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**2**	**0**
	4	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**2**	**0**
	5	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**2**	**0**