TUT-VI
IC LOGIC FAMILIES

18.09.2012

Standard Logic Gates: Data sheets

- Data sheets provide essential information:
  - Logic Function
  - Truth Table
  - Pin-out
  - Electrical Characteristics
  - Timing Characteristics
  - Package Description(s)
- This information is necessary when building logic circuits from discrete components.
- Each Logic Family has a unique set of characteristics.

Basic Logic Families

- **TTL** – transistor-transistor logic based on bipolar transistors.
- **CMOS** – complementary metal-oxide semiconductor logic based on metal-oxide-semiconductor field effect transistors (MOSFETs).
- **ECL** – emitter coupled logic based on bipolar transistors.

General Characteristics of Basic Logic Families

- CMOS consumes very little power, has excellent noise immunity, and is used with a wide range of voltages.
- TTL can drive more current and uses more power than CMOS.
- ECL is fast, with poor noise immunity and high power consumption.

Advantages of TTL

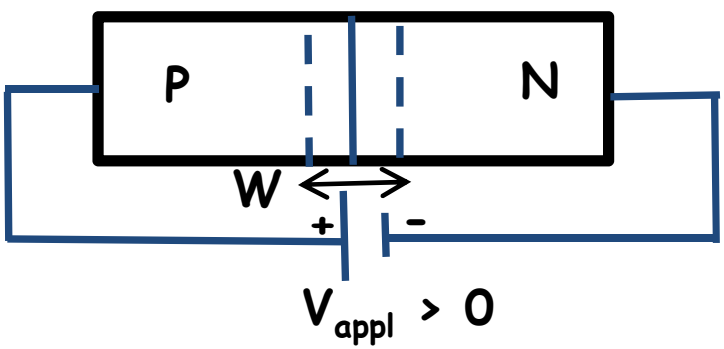
- These use saturated BJTs as switches.
- They have higher transconductance than their MOS counterparts, so they are less vulnerable to capacitive loading.
- They outperform MOS digital circuits when capacitive loads are connected such as in case of motherboards.
- They also exhibit faster raw speeds than MOS.

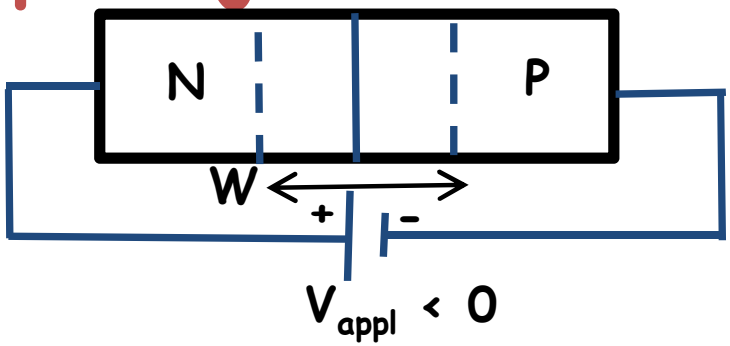
Logic Families

- TTL
  - Low-Power TTL (“L”)
  - High-Speed TTL (“H”)
  - Schottky (“S”)
  - Low-Power Schottky (“LS”)
  - Advanced Schottky (“AS”)
  - Advanced Low-Power Schottky (“ALS”)
  - Fast (“F”)
- CMOS
  - High-Speed CMOS (“HC”)
  - Advanced CMOS (“AC”)

TTL

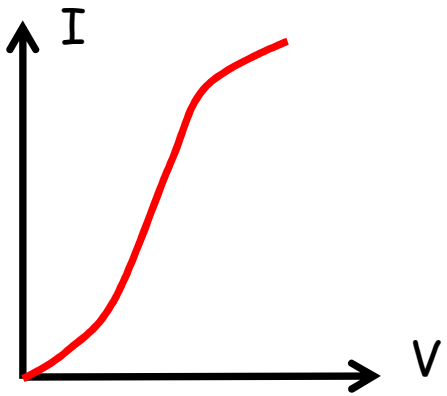
Recall p-n junction





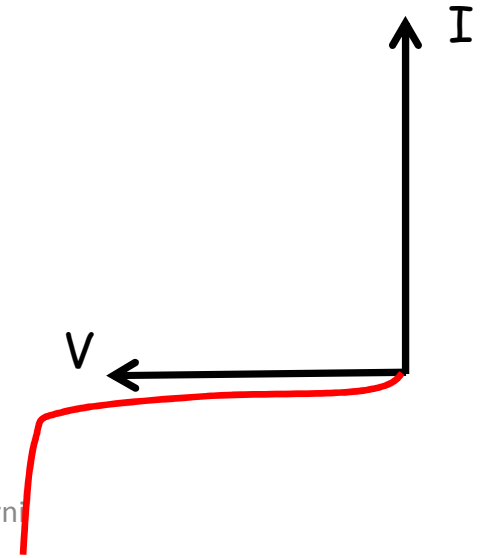
Forward bias, + on P, - on N
(Shrink W, V_{bi})

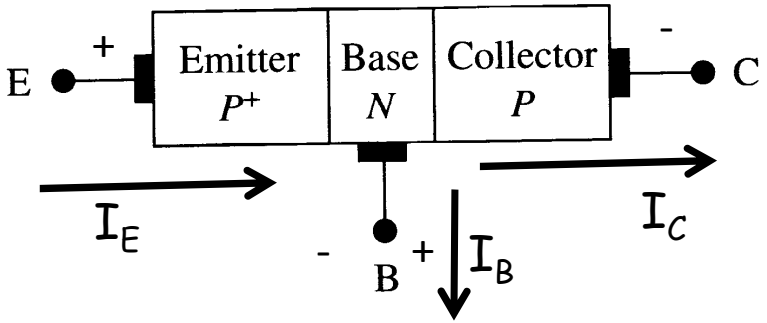
Allow holes to jump over barrier into N region as minority carriers



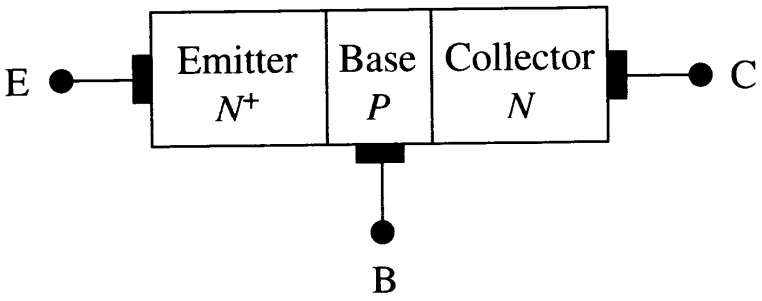
Reverse bias, + on N, - on P
(Expand W, V_{bi})

Remove holes and electrons away from depletion region





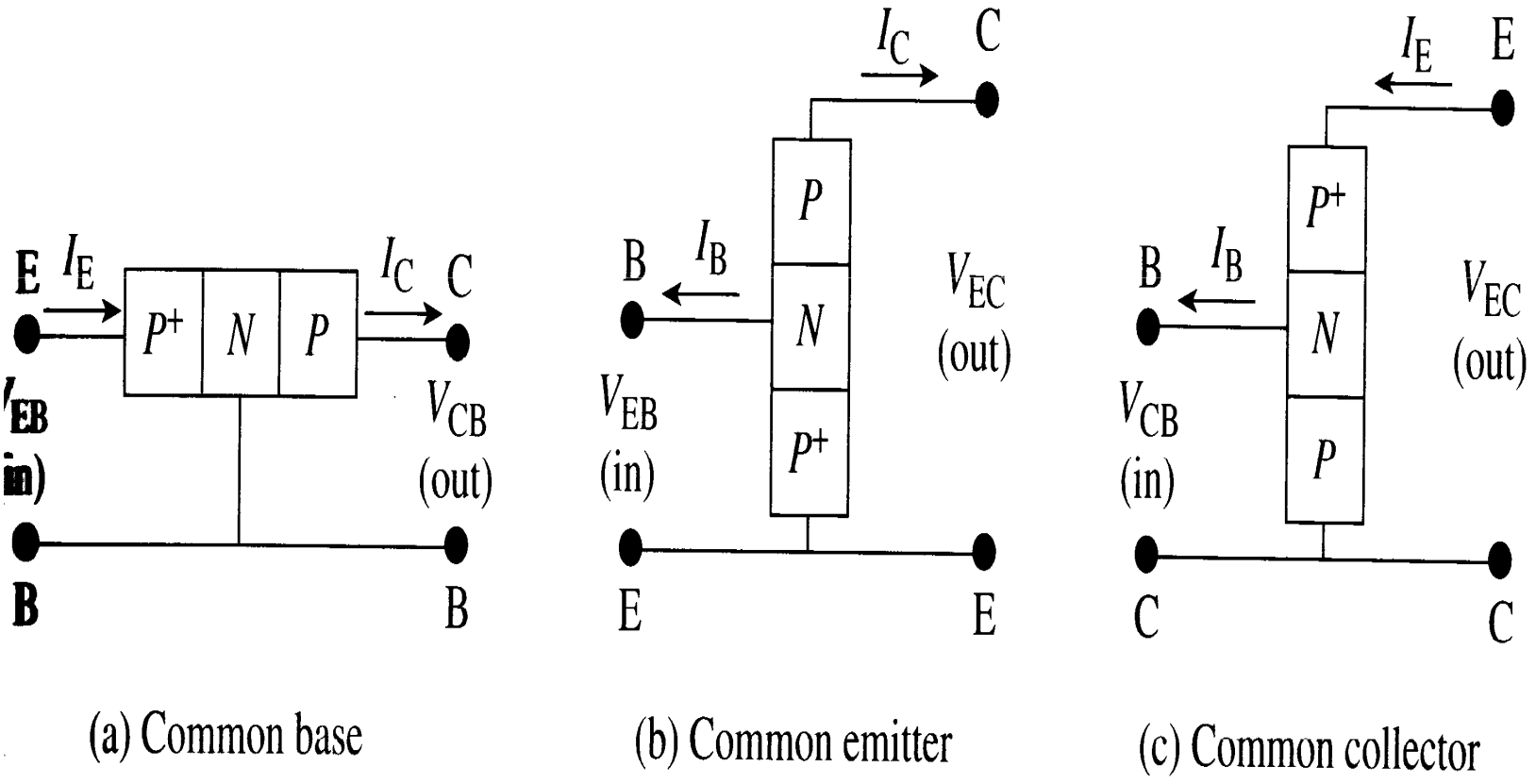
(a) *pnp*



(b) *npn*

Bias Mode	*E-B Junction*	*C-B Junction*
Saturation	Forward	Forward
Active	**Forward**	**Reverse**
Inverted	Reverse	Forward
Cutoff	Reverse	Reverse

BJT configurations

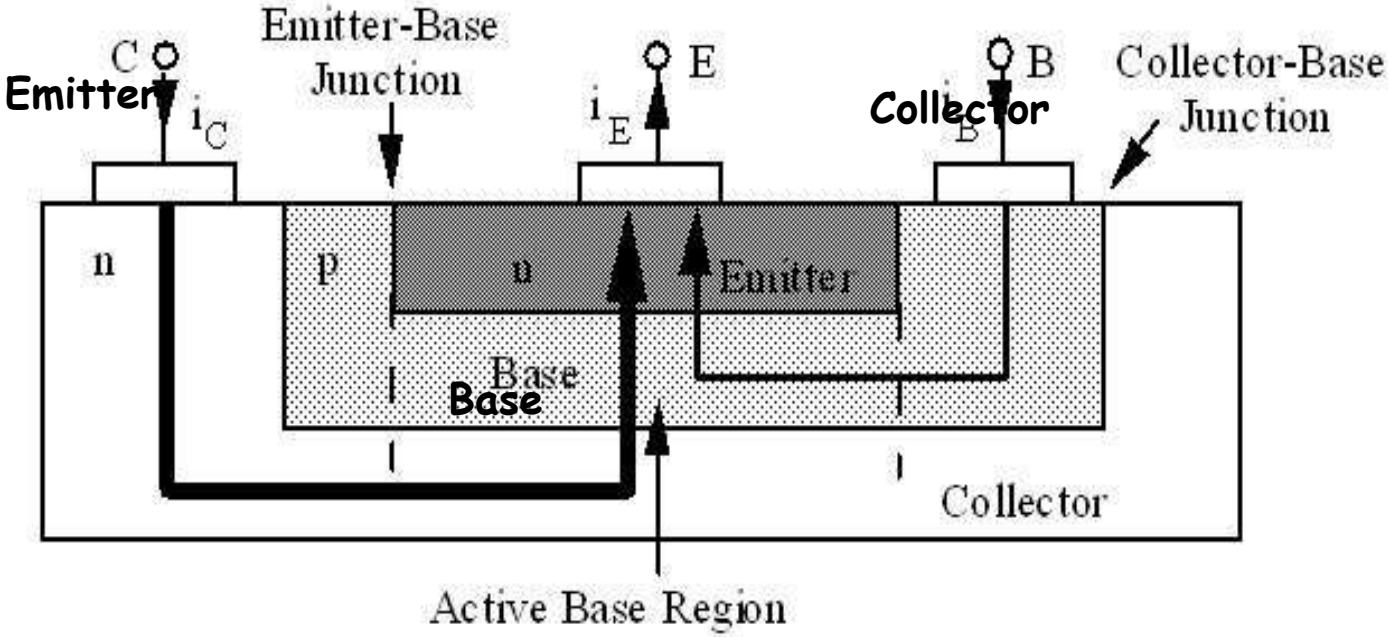


(a) Common base

(b) Common emitter

(c) Common collector

Physical Structure of Bipolar Junction Transistor (BJT): Simplified Cross Section

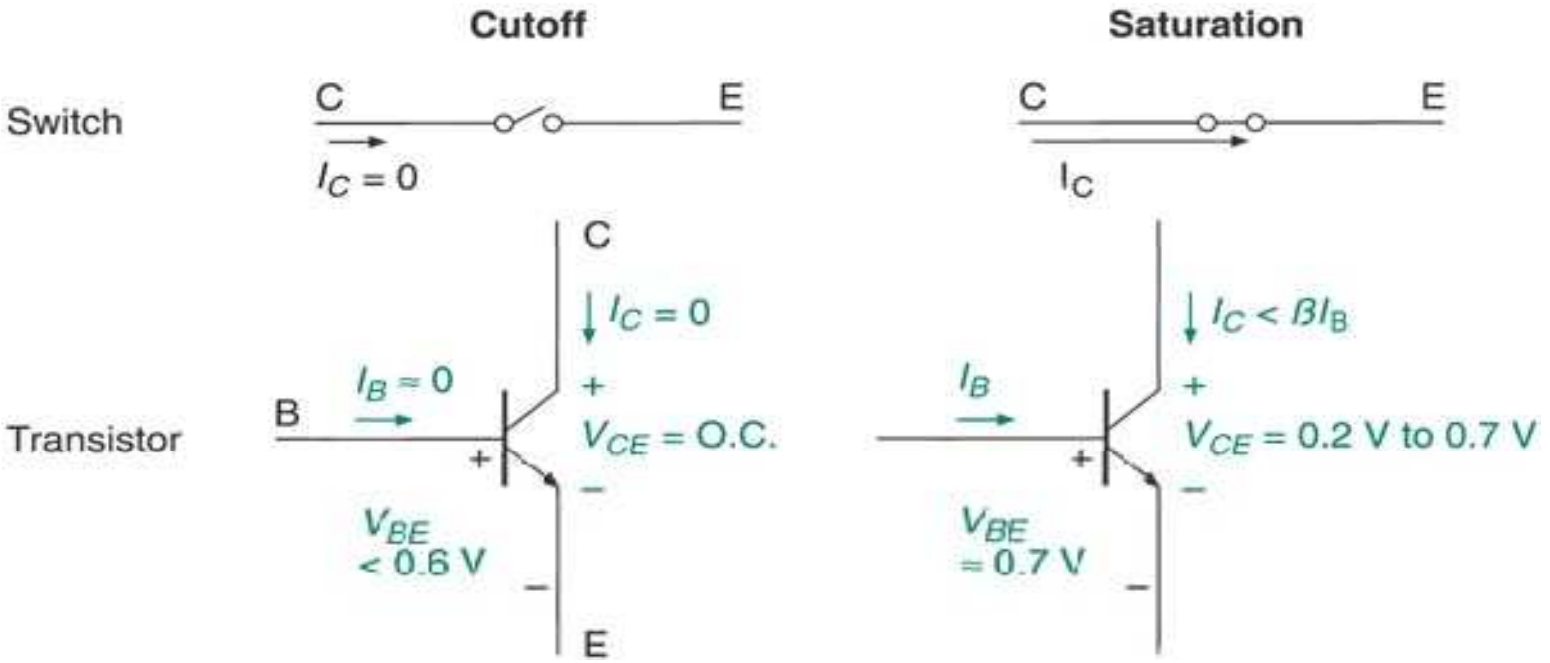


BJT

TTL Gates Internal Circuitry

- Uses the bipolar junction transistor.
- The transistors used are in one of two modes: cutoff or saturation.
- In cutoff mode, the transistor acts as an open switch.
- In saturation, the transistor acts as a closed switch.

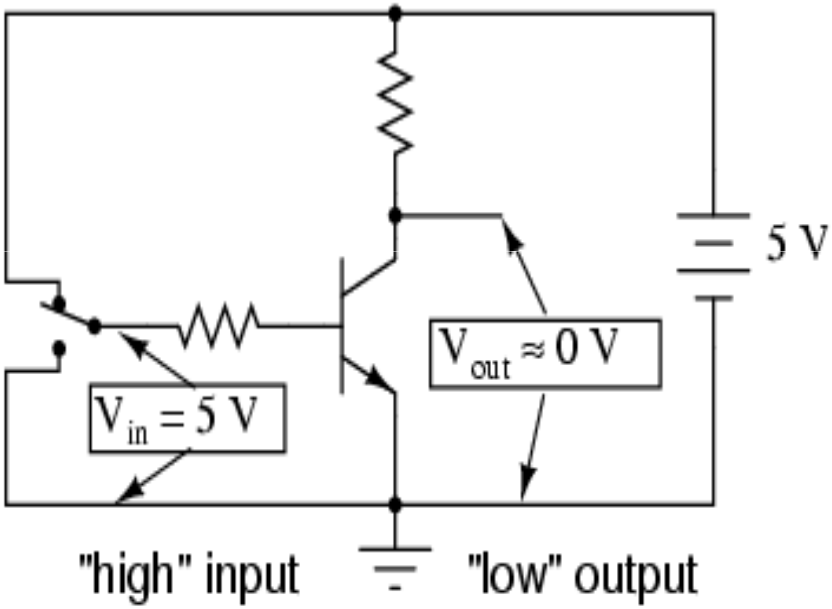
TTL Gates Internal Circuitry



	Cutoff	Active	Saturation
I_C	0	$= \beta I_B$	$< \beta I_B$
V_{CE}	Open cct.	>0.8 V	0.2 V - 0.7 V
V_{BE}	<0.6 V	0.6 V - 0.7 V	$\approx$ 0.7v

Transistor as a Switch

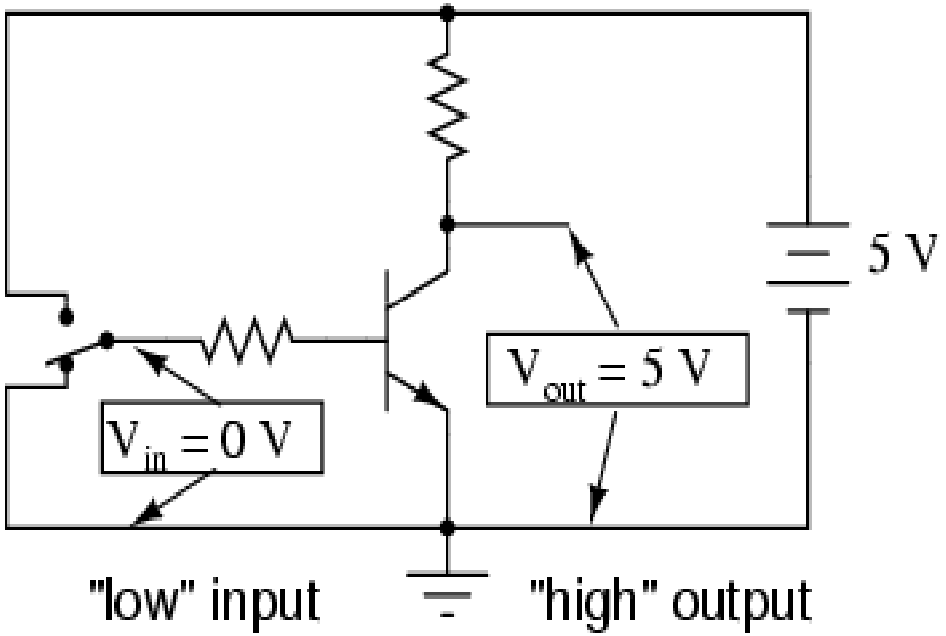
Transistor in saturation



0 V = "low" logic level (0)

5 V = "high" logic level (1)

Transistor in cutoff



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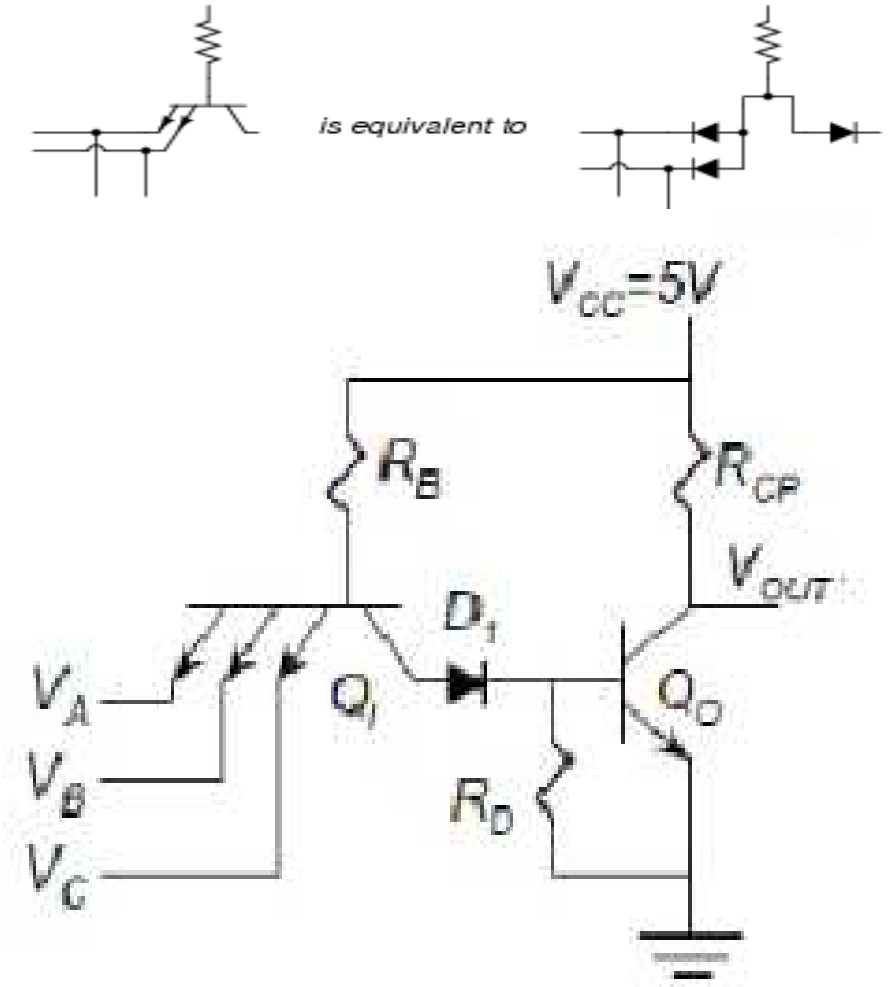
NAND LOGIC USING TTL

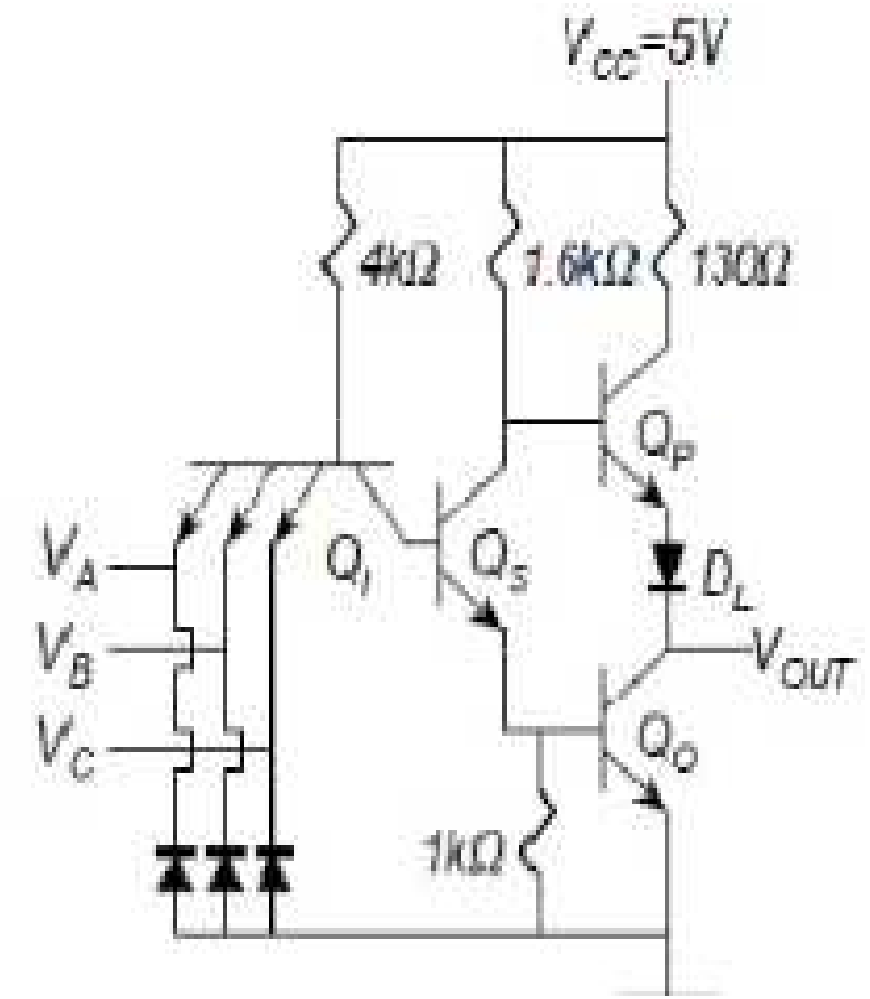


- **When all inputs are HIGH** EBJ of Q1 is reverse biased and CBJ forward biased so it enters reverse active mode.
- as Q o's base goes HIGH ,this makes Qo in saturation region so

  Vout is LOW (V Cesat =0 .2 Volts).
- **When any one of the inputs is LOW**
- Then EBJ of Q1 is forward biased and it enters saturation region.
- This makes Qo in cut off mode. As transistor in cut off mode so **output is HIGH**

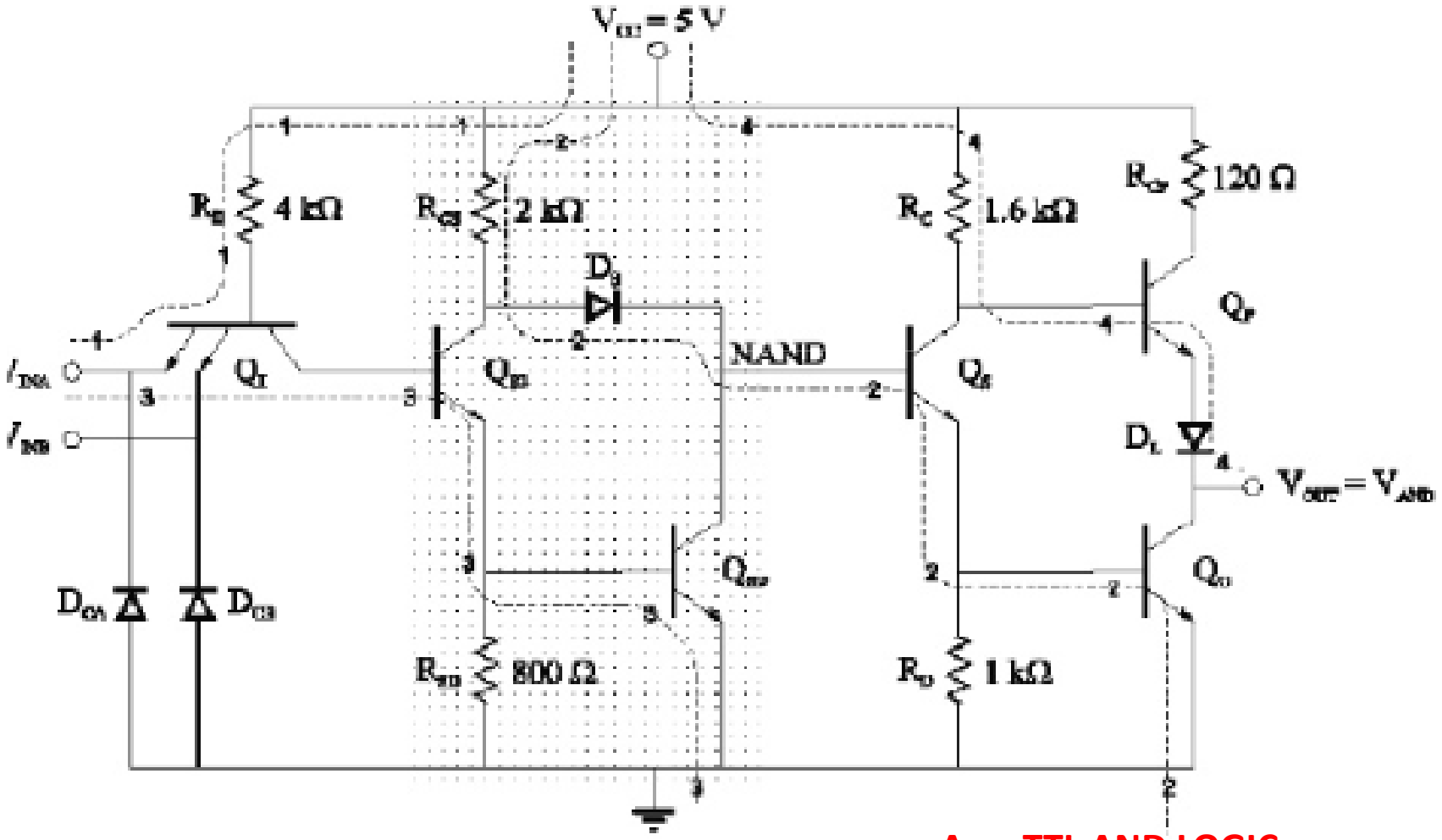
PROBLEM: both Q1 & Qo needs to discharge once any one of them has entered saturation.

IMPROVED NAND LOGIC using TTL



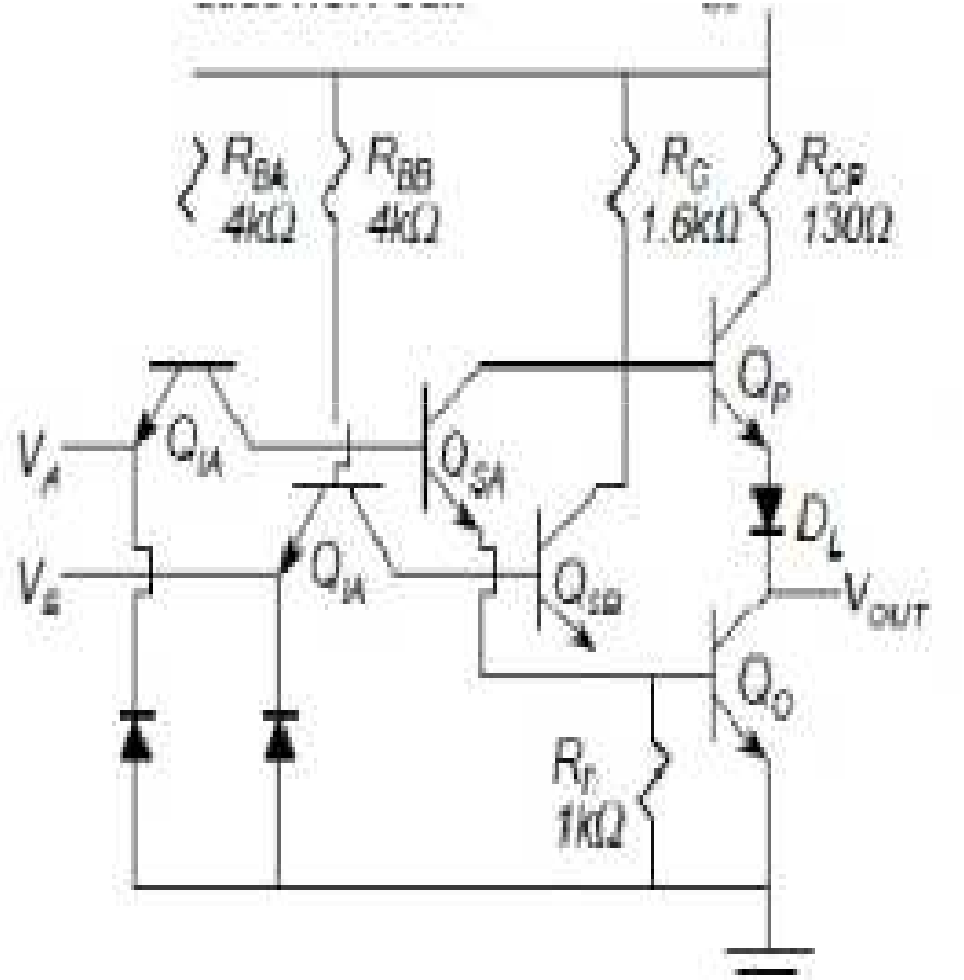
- **When any one of the inputs is LOW**
- Then EBJ of Q1 is forward biased and it enters saturation region.
- This makes Qs in cut off mode.
- Qp is active mode **WITH OUTPUT HIGH**
- **When all inputs are HIGH** EBJ of Q1 is reverse biased and CBJ forward biased so it enters reverse active mode.
- as Q s's base goes HIGH ,this makes Qs in saturation and Qp is Cut off **With OUTPUT LOW**
- **Three diodes at the input side to prevent circuit for negative input**

Can You Analyze?



Ans: TTL AND LOGIC

Analyze following TTL circuit

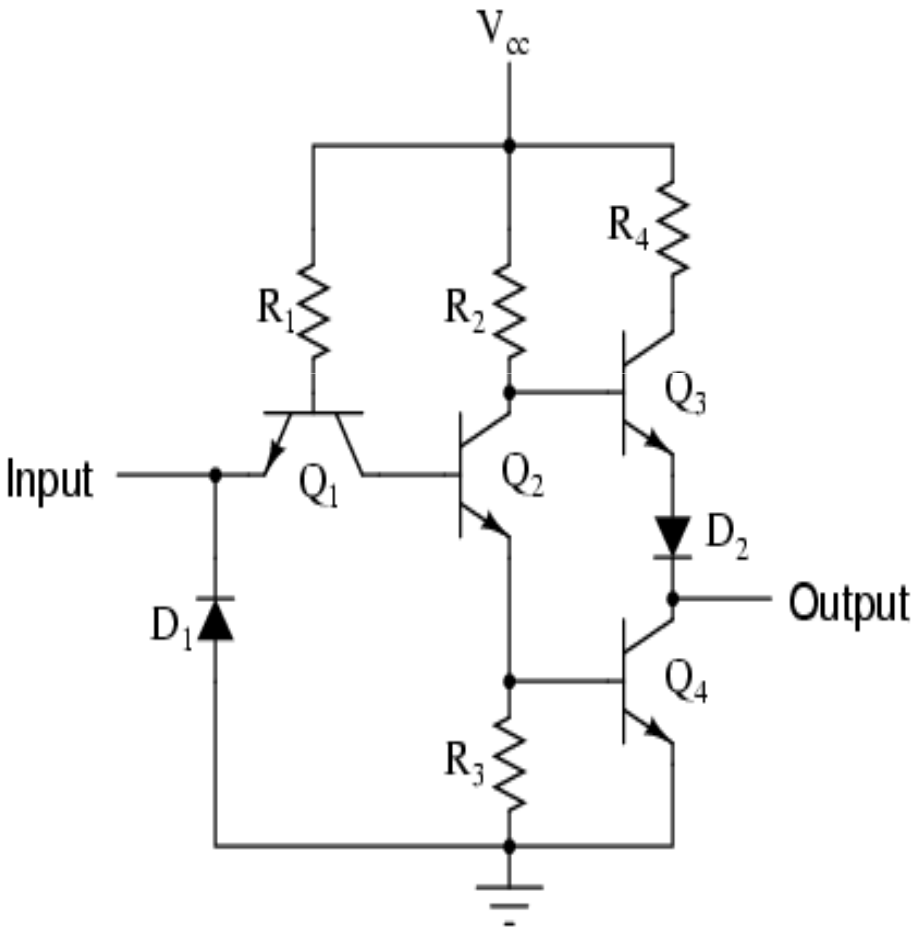


When V A is HIGH Q IA goes to saturation. Then regardless of the situation of Q SB ,Qp will be cut off and Qo will saturate (OFF). **Hence output will be low.**

When V A is LOW the current in Q IA 's collector is zero and Q SA is in Cut off. **VB will determine the output** in this case now if V B is also LOW then Q SB is also cut off andQp is in saturation and Qo will cutoff (ON). **Hence output is HIGH**.

Hence if either input goes HIGH the outputs goes LOW hence performing **NOR function.**

HA: NOT LOGIC Using TTL

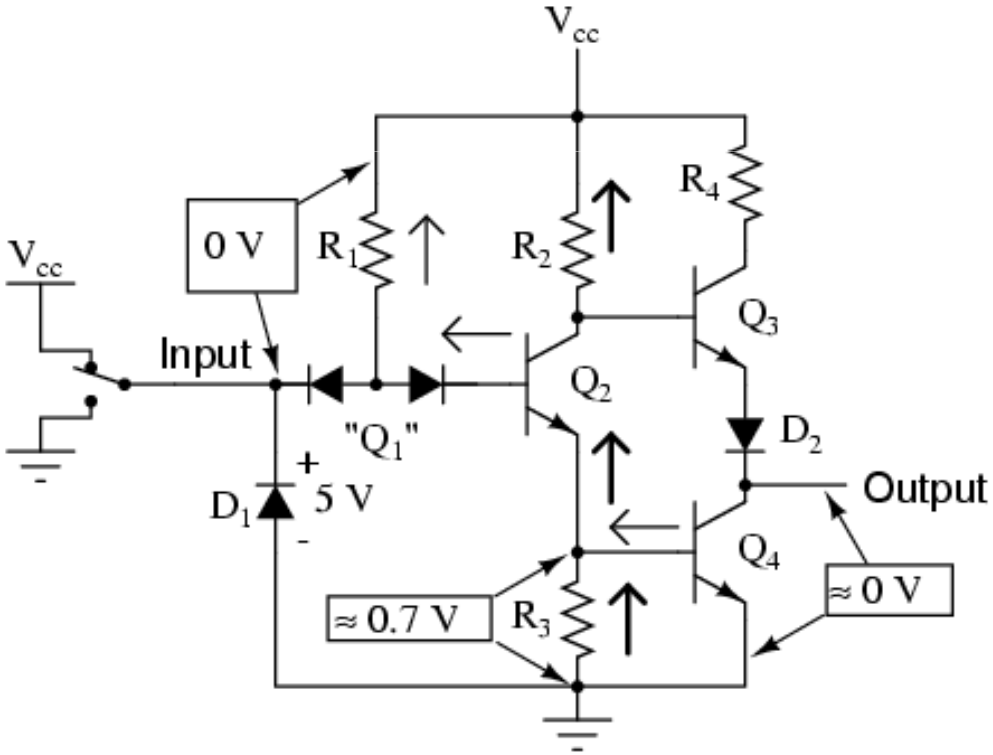


Let Input=HIGH (VCC).

Diode D1- RB

PD between base and Emitter of Q1 is zero

- Transistor Q_2 will be turned "on." More specifically, it will be *saturated* by virtue of the more-than-adequate current allowed by R_1 through the base.
- With Q_2 saturated, resistor R_3 will be dropping enough voltage to forward-bias the base-emitter junction of transistor Q_4, thus saturating it as well .
- Due to the presence of diode D_2, there will not be enough voltage between the base of Q_3 and its emitter to turn it on, so it remains in cutoff.



Analyze circuit for zero input

- No current through the base of Q2, thus turning it off.
- With Q2 off, there is no longer a path for Q4 base current, so Q4 goes into cutoff.
- Q3, on the other hand, now has sufficient voltage dropped between its base and ground to forward-bias its base-emitter junction and saturate it, thus raising the output terminal voltage to a "high" state.
- In actuality, the output voltage will be a "high" (1) logic level.
- The astute observer will note that this inverter circuit's input will assume a "high" state of left floating (not connected to either Vcc or ground). With the input terminal left unconnected, there will be no current through the left steering diode of Q1, leaving all of R1's current to go through Q2's base, thus saturating Q2 and driving the circuit output to a