Digital Electronics and Microprocessors

Class 6

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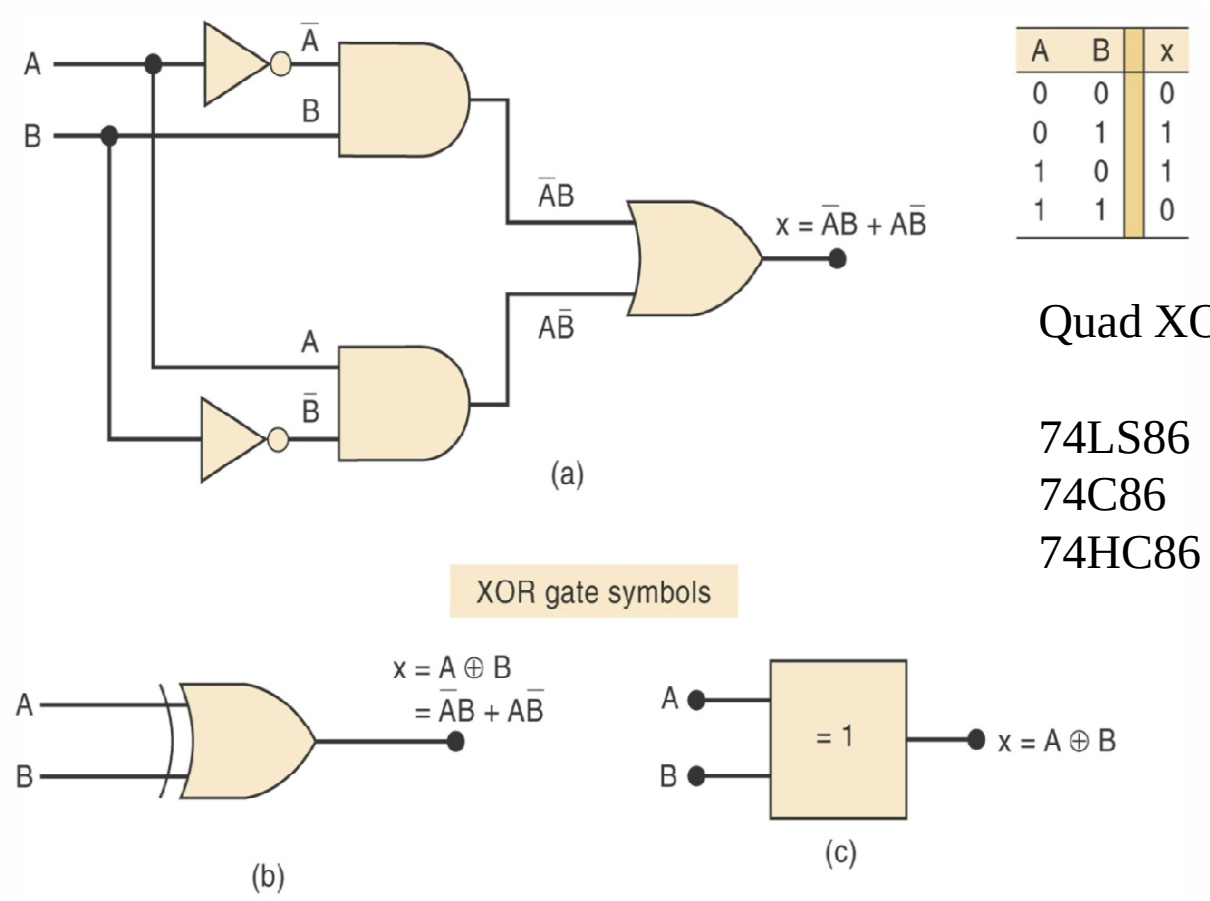
Exclusive OR and Exclusive NOR Circuits

- The exclusive OR (XOR) produces a HIGH output whenever the two inputs are at opposite levels.
- The exclusive NOR (XNOR) produces a HIGH output whenever the two inputs are at the same level.
- XOR and XNOR outputs are opposite.

(a) Exclusive-OR circuit and truth table; (b) traditional XOR gate symbol; (c) IEEE/ANSI symbol for XOR gate.

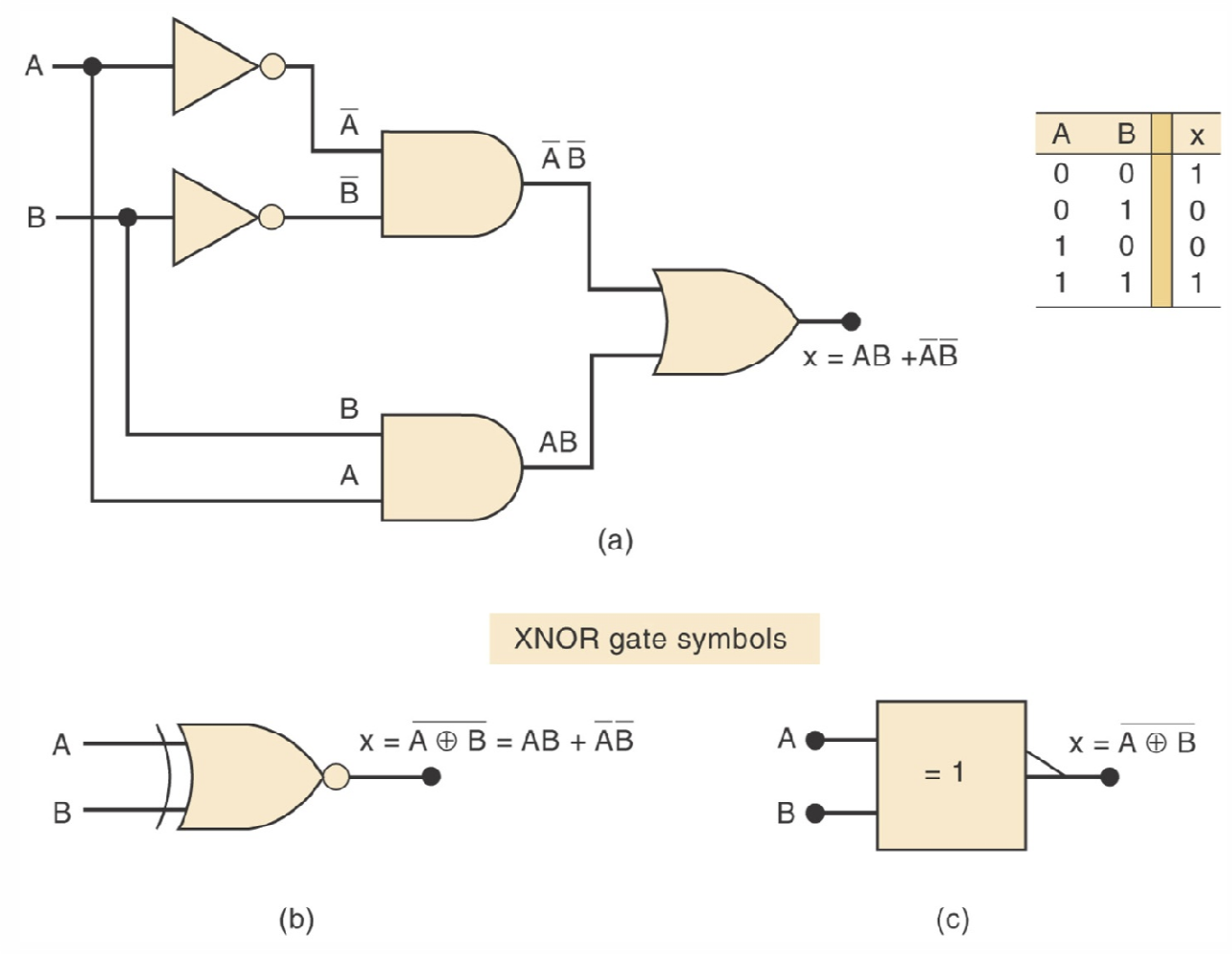


A	B	x
0	0	0
0	1	1
1	0	1
1	1	0

Quad XOR Chips

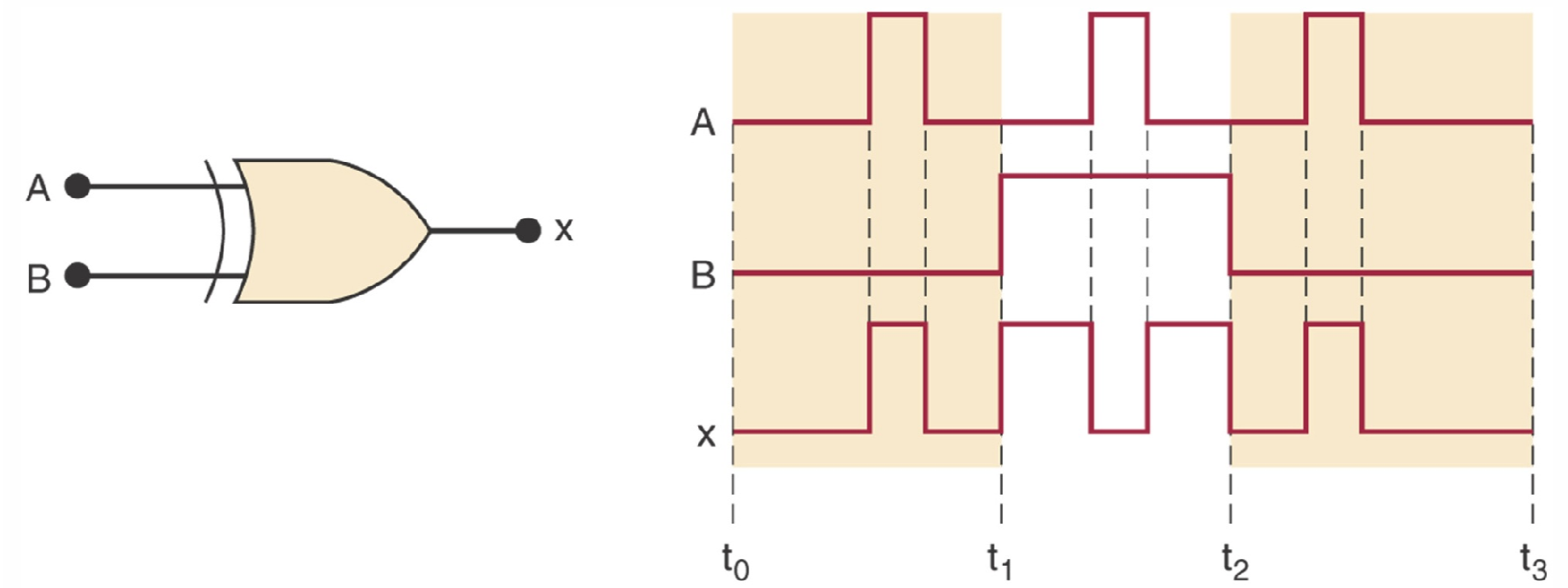
74LS86 Quad XOR(TTL family)
74C86 Quad XOR(CMOS family)
74HC86 Quad XOR(HS CMOS)

(a) Exclusive-NOR circuit; (b) traditional symbol for XNOR gate; (c) IEEE/ANSI symbol.



A	B	x
0	0	1
0	1	0
1	0	0
1	1	1

XOR Timing Diagram



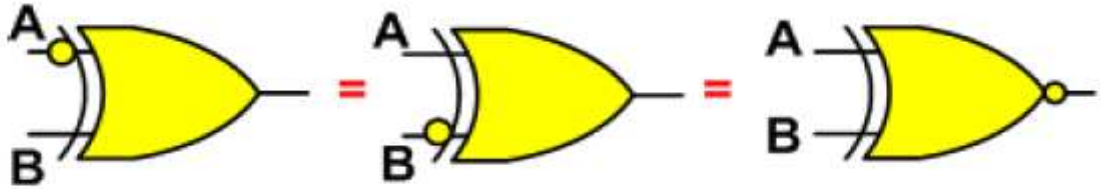
Basic Identities of XOR Operation:

- $X \oplus 0 = X$
- $X \oplus 1 = X'$
- $X \oplus X = 0$
- $X \oplus X' = 1$
- $X \oplus Y' = X' \oplus Y = (X \oplus Y)' = X \odot Y$

Graphical presentation of important XOR/XNOR rules and gate equivalence.

$$A \oplus B = \overline{A} \oplus \overline{B} = A\overline{B} + \overline{A}B$$

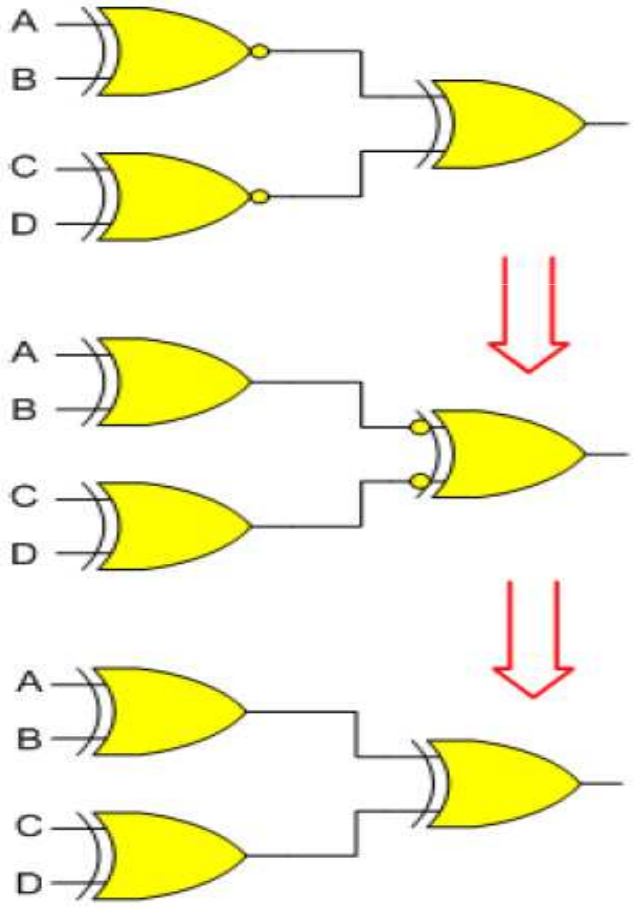
$$A \odot B = \overline{A} \odot \overline{B} = \overline{A}\,\overline{B} + AB$$



$$\overline{A} \oplus B = A \oplus \overline{B} = \overline{A}\,\overline{B} + AB = A \odot B$$

Example:

Show that **(A ʘ B) ⊕ (C ʘ D) = A ⊕ B ⊕ C ⊕ D**



Applications of X-OR/X-NOR

- Odd function/Even function
- Even/Odd parity generator and checker
- Binary to gray/Gray to binary

ODD Function:

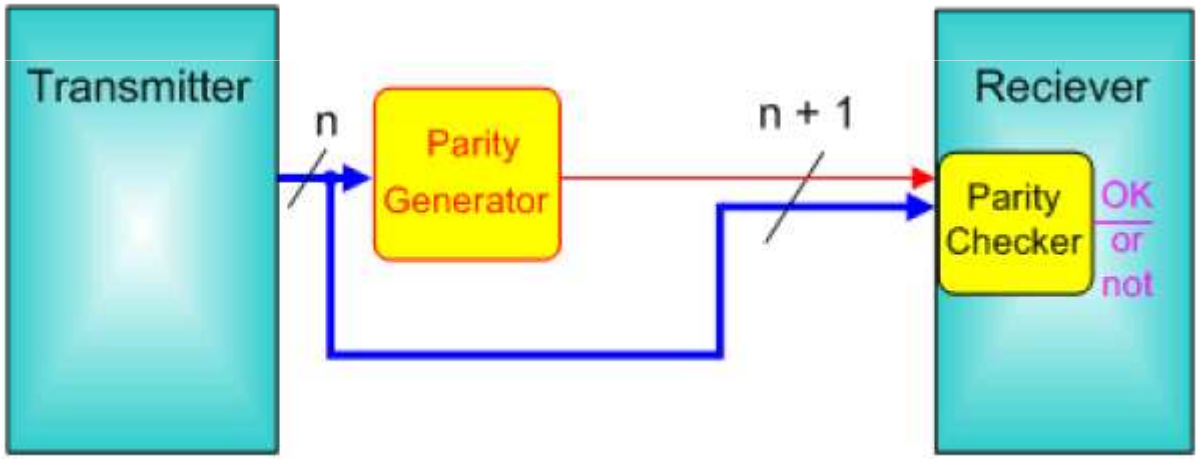
As shown in the K-map, **X ⊕ Y ⊕ Z = 1, IFF (if and only if) the number of 1's in the input combination is odd.**

X	Y	Z	ODD
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

xy \ z	Z'	Z
X'Y'	0	1
X'Y	1	0
XY	0	1
XY'	1	0

ODD= **X ⊕ Y ⊕ Z**

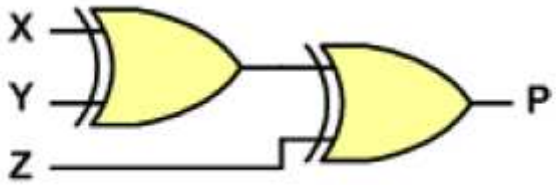
Parity Generation and checking



Even Parity Generation (Odd Function)

X	Y	Z	P(E)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

xy \ z	Z'	Z
X'Y'	0	1
X'Y	1	0
XY	0	1
XY'	1	0



P(E)= **X ⊕ Y ⊕ Z**

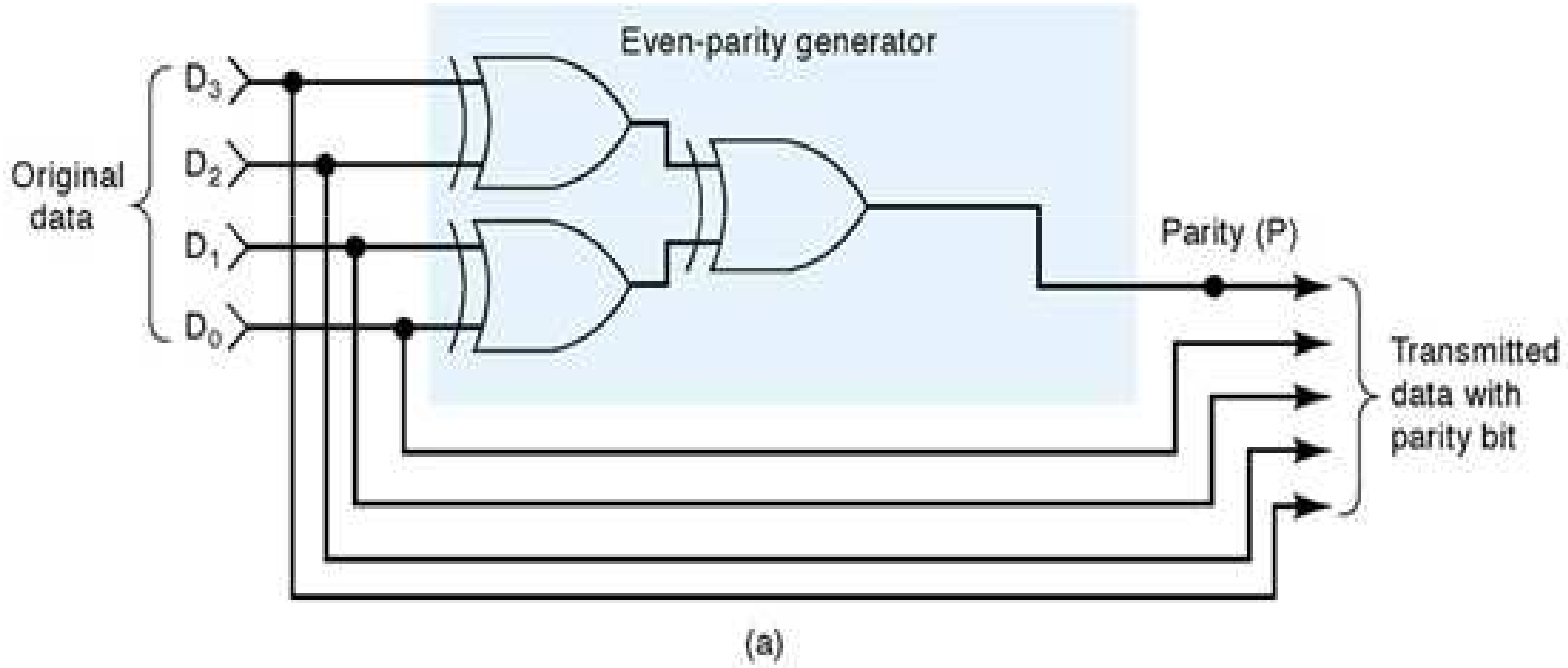
Parity Generator and Checker

- XOR and XNOR gates are useful in circuits for parity generation and checking.

Even Parity Generator truth table →

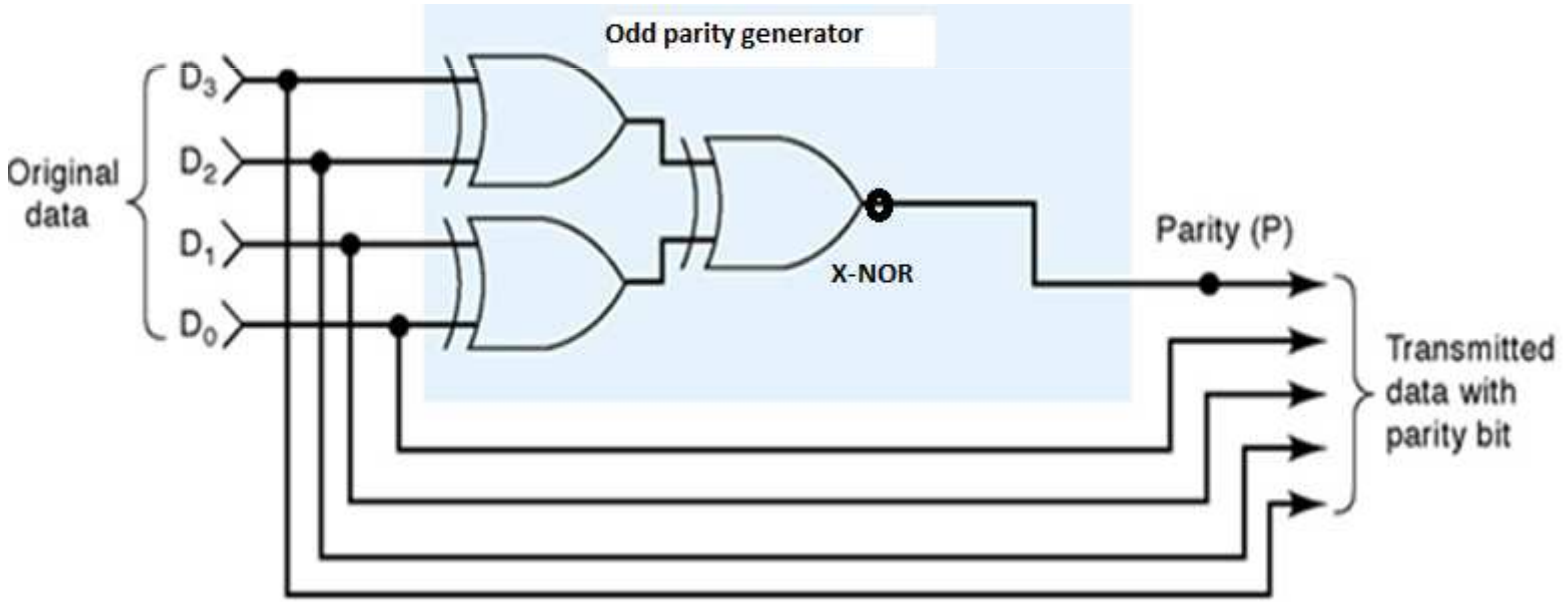
D3	D2	D1	D0	Parity
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Even Parity Generator Ckt for 4-bit data



Odd parity generation for 4 bit data

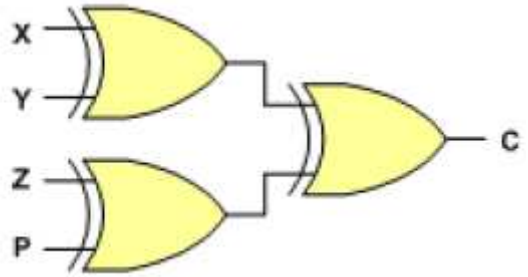
Add an inverter at the output of the previous(even parity generator ckt) ckt



3-bit even parity checker (4-input, 3 data inputs 1 parity input)

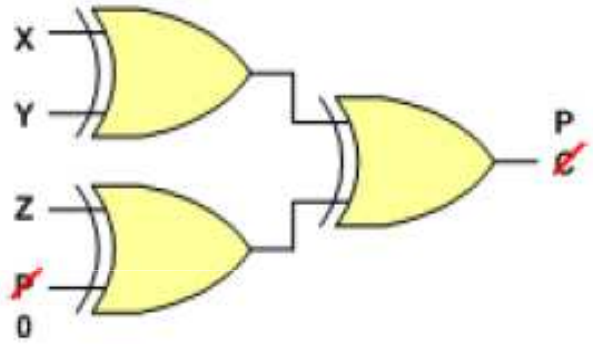
Four Bits Received				Parity Error Check
X	Y	Z	P	C
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

	Z'P'	Z'P	ZP	ZP'
X'Y'	0	1	0	1
X'Y	1	0	1	0
XY	0	1	0	1
XY'	1	0	1	0



C=0 (No Error)
C=1(Error)

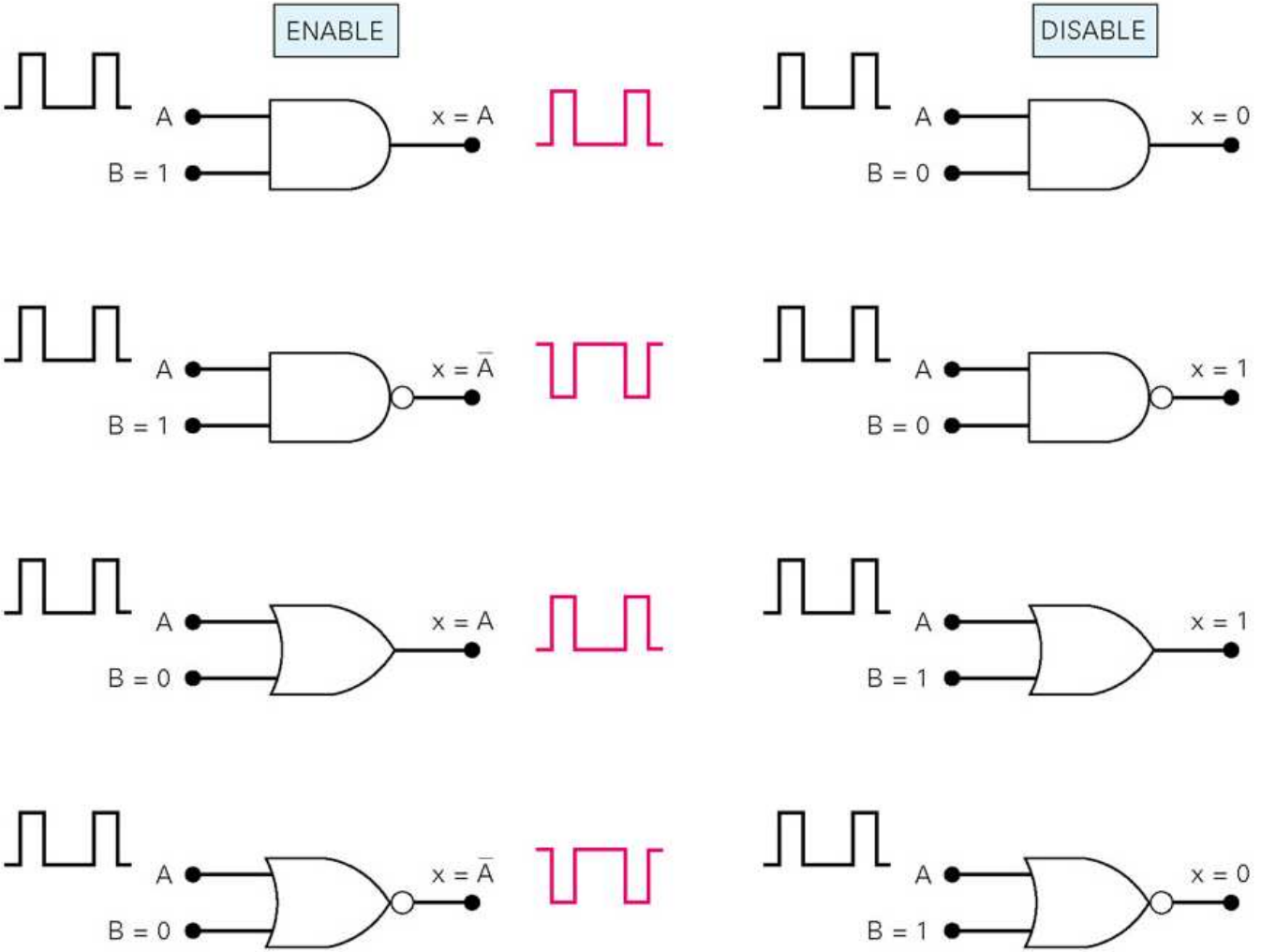
3-bit parity generator/checker ckt



For Generator P input of this circuit should be zero always and output will be parity bit

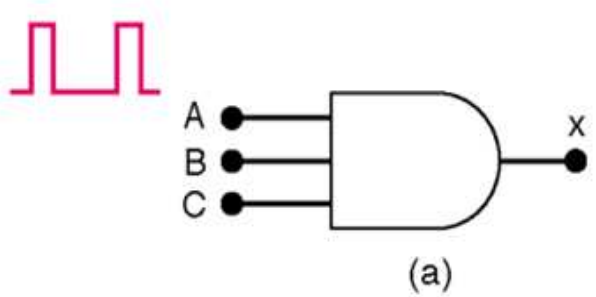
For checker the P input is the parity bit Input and output will be checked ouput(error/no error)

Enable/Disable Circuits



Enable/Disable Circuits cont.

Example:- Design a logic circuit that will allow a signal to pass to the output only when control inputs B and C are both HIGH; otherwise, the output will stay LOW.

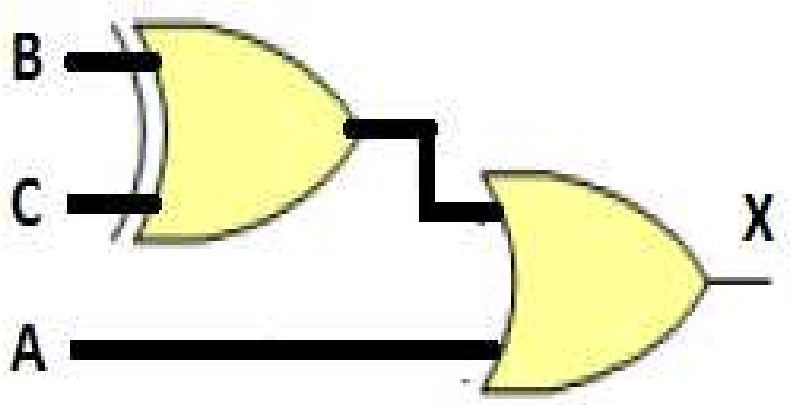


Refer example 4-23 of T1

Example:- Design a logic circuit that controls the passage of the signal A according to the following requirements:

1. Output X will equal A when control inputs B and C are same.
2. X will remain HIGH when B and C are Different

X=A when B=C and X=1 when B Not Equal to C



Take home problems

4-2,4-3,4-5,4-7,4-8,4-16,4-22,4-25,4-38