EXPERIMENT NO. 3

LATCHES & FLIP-FLOPS

NAME: ; ID: ;

GROUP NO.: ;DATE .

Objectives:

1. Understanding the operation and construction of various latches and flip-flops
2. Investigate the application of flip-flops in frequency division

Components Required: Push Buttons (2 NoS), LEDs, Multimeter, CRO, CRO Probes (2Nos.),

7474 – Dual D flip-flop

7476 – Dual master-slave J K flip-flop

7486 – Quad 2-input XOR

7400 – Quad 2-input NAND

7473– Dual J K flip-flop

Experiment:

Verify following parameters and complete the checklist before circuit implementation.

S.No.	Description	Remark (√ OR ×)
1	Check DC voltage from power supply	
2	Select proper voltage range of DC power supply	
4	Test all ICs using IC tester	
5	Place required ICs correctly on bread board	
6	Identify pin no.1 of each IC	
7	DC power supply is OFF till you complete the connections.	
8	Complete all the truth tables with theoretically calculated values and required circuit diagrams	
9	Include pin numbers of each gate in circuit diagram	

Run #01:

1. Turn on CRO in Dual mode and observe two trace lines on the CRO screen.
2. Connect one of the CRO probe to “CH-I” terminal. Test the probe using calibration signal of CRO.
3. Test another CRO probe with “CH-II” terminal by following same procedure as in step 2.
4. Connect “CH-I” to function generator to observe square wave of freq.8 kHz.

Run #02: Latches respond to change in the levels of clock pulses.

Implement an S-R latch using NAND gates only. Draw the diagram as Fig 3.1

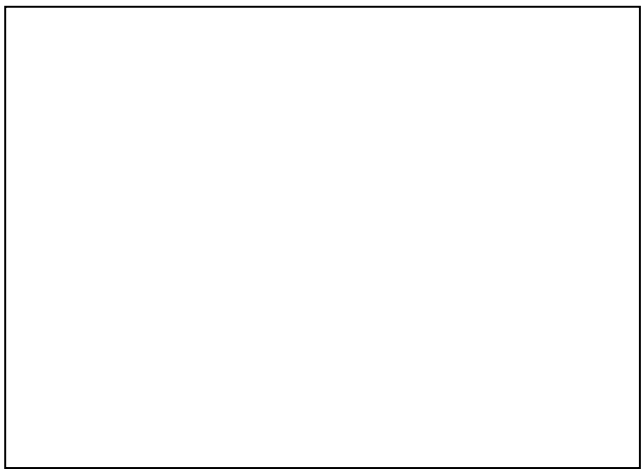

Fig 3.1: S-R Latch using NAND gates

Input		Output		Observed O/p	
Set	Clear	Q	Q’	Q	Q’
1	1				
0	1				
1	0				
0	0				

Table 3.2: Truth table for S-R latch

Connect the two inputs to toggle switches and the two outputs to LEDs. Note down the function table of the circuit in truth table given in Table 3.2.

Run #03: A flip-flop responds to only a transition in the clock pulse i.e. flip-flops are edge triggered and changes state either at the positive or negative edges of the clock.

IC 7474 is a dual positive edge triggered D flip-flop IC with preset and clear. Refer data sheet for pin configuration and function table of the IC. Draw Pin configuration and Logic Symbol as Fig 3.2 and 3.3 respectively.

The preset and clear inputs are asynchronous inputs and are independent of clock.

Fig 3.2: Pin configuration of IC 7474

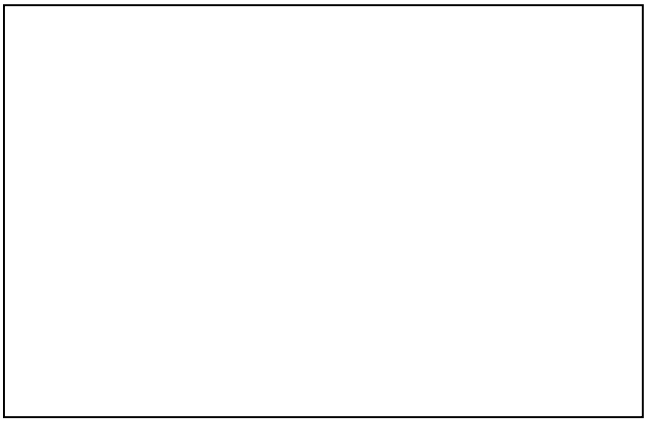

Fig 3.3: Logic Symbol of IC 7474

Verify the functioning of the IC by clock inputs and giving different D inputs. Also verify the functioning of preset (SET) and clear (RESET) inputs. Note your observations, in the function table below as in Table 3.3.

Operation Mode	Inputs				Outputs		Observed o/p	
	S_D'	R_D'	CP	D	Q	Q'	Q	Q'
Asynchronous SET								
Asynchronous RESET								
Undetermined								
Load"1" (SET)								
Load"0" (RESET)								

Table 3.3: Function table of IC 7474 (Dual D-FlipFlop)

Run #04: IC 7473 is a dual negative edge triggered J K flip-flop. Refer data sheet to know pin assignment and function table of the IC. Draw Pin configuration and Logic Symbol of the IC as Fig 3.4 and 3.5 respectively.

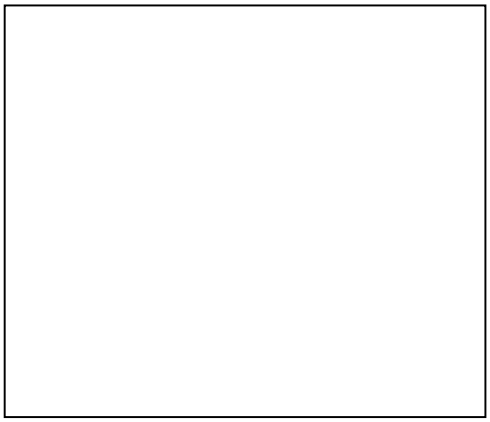

Fig 3.4: Pin configuration of IC 7473

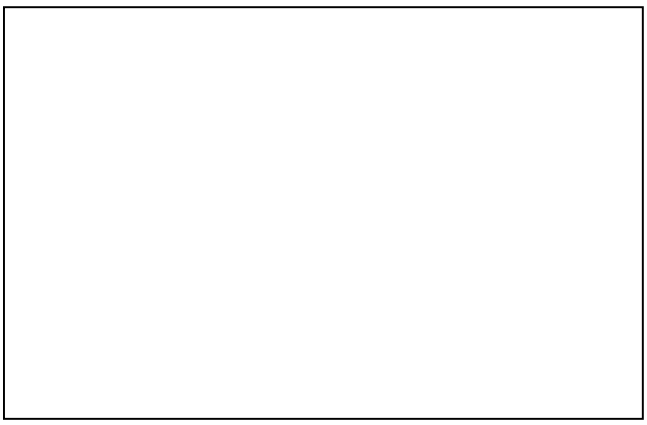

Fig 3.5: Logic Symbol of IC 7473

Verify the functioning of the IC with all required combinations of inputs. Note your observations, in the function table below as in Table 3.4.

Operation Mode	Inputs				Outputs		Observed o/p	
	R_D'	CP'	J	K	Q	Q'	Q	Q'
Asynchronous RESET (Clear)								
Toggle								
Load"0" (RESET)								
Load"1" (SET)								
HOLD "No Change"								

Table 3.4: Function table of IC 7473 (Dual negative edge triggered J K flip-flop)

Run #05: IC 7476 is a dual master-slave J K flip-flop with preset and clear. The pin assignment of IC 7476 is given in data sheet. .

Draw Pin configuration and Logic Symbol of the IC as Fig 3.6 and 3.7 respectively.

Verify the functioning of the IC with all required combinations of inputs. Note your observations, in the function table below as in Table 3.5

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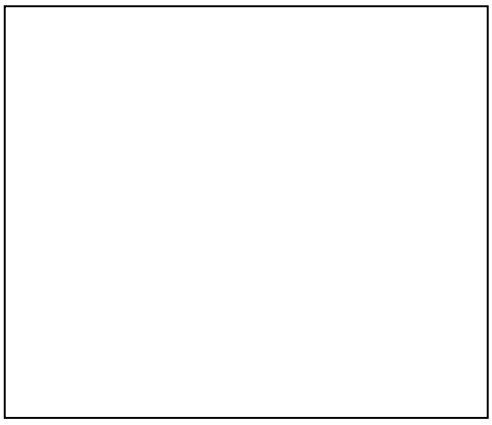

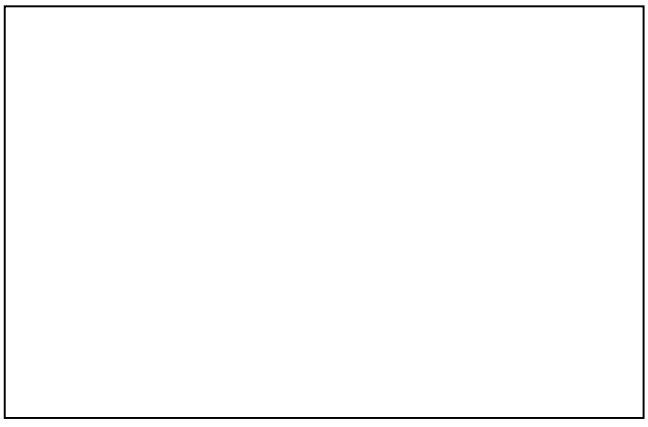

Fig 3.6: Pin configuration of IC 7476

Fig 3.7: Logic Symbol of IC 7476

t_n		t_{n+1}
J	K	Q

Table 3.5: Truth table of IC 7476 (Dual J K MASTER –SLAVE flip-flop)

Run #06: Implement a digital circuit using D-FF (IC) to obtain the output frequency as input clock frequency divide by four. Draw the circuit diagram using logical symbol of the IC as Fig 3.8

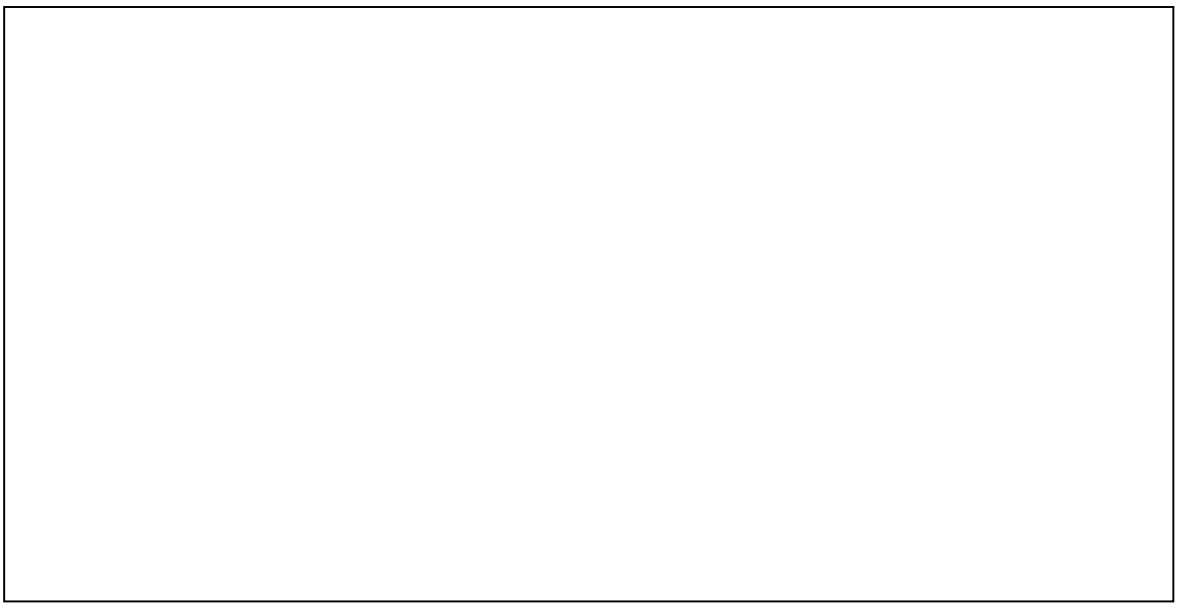

Fig 3.8: Frequency divider using D-FF

Feed input clock of 8 KHz from the function generator and observe the output on CRO screen. Sketch the output waveform below. State the relationship between the frequencies of the waveforms.

Clock:

Output Q: