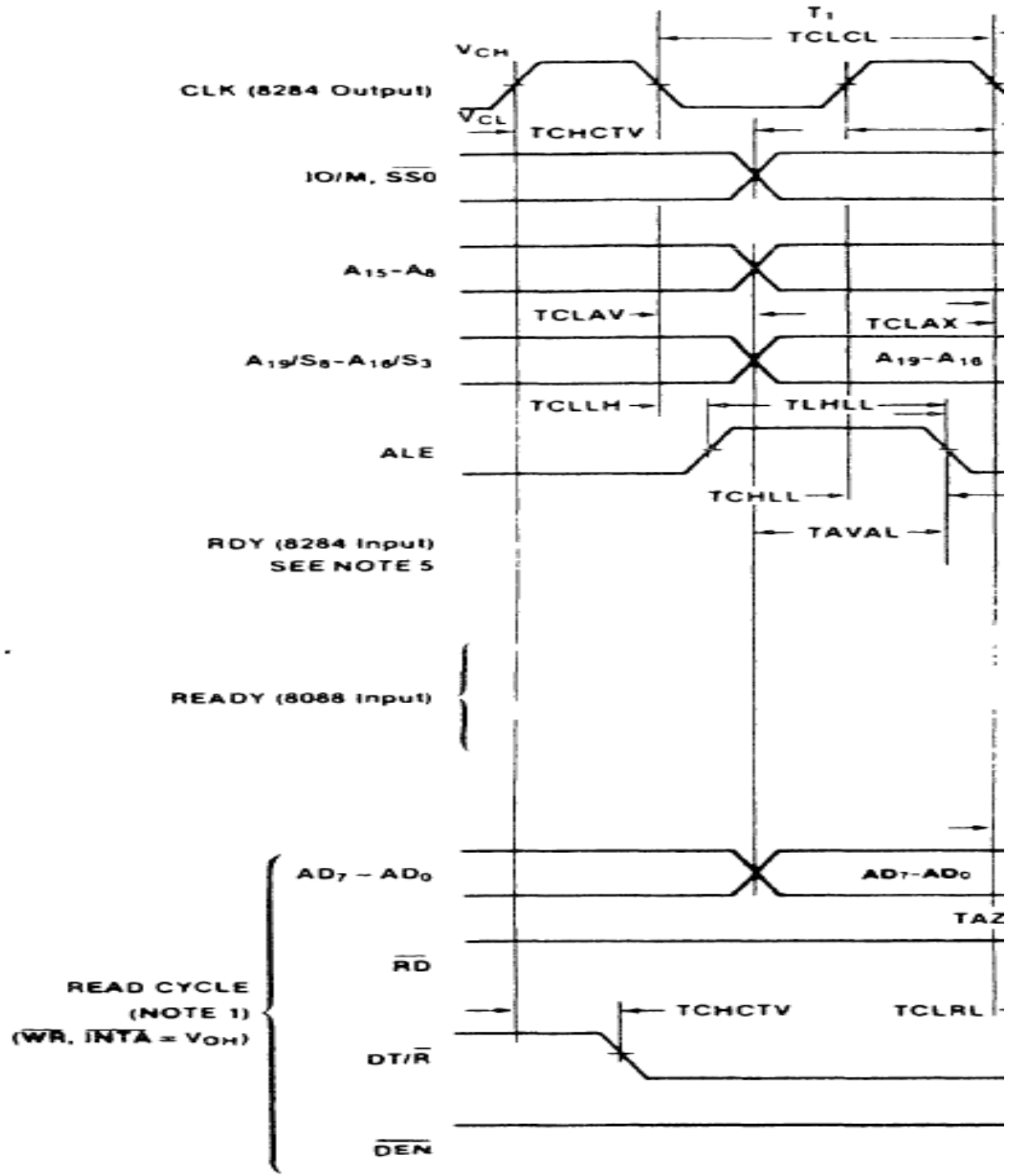
Hardware Characteristics:8086 (REVISITED)

27/11/12

Timing in General

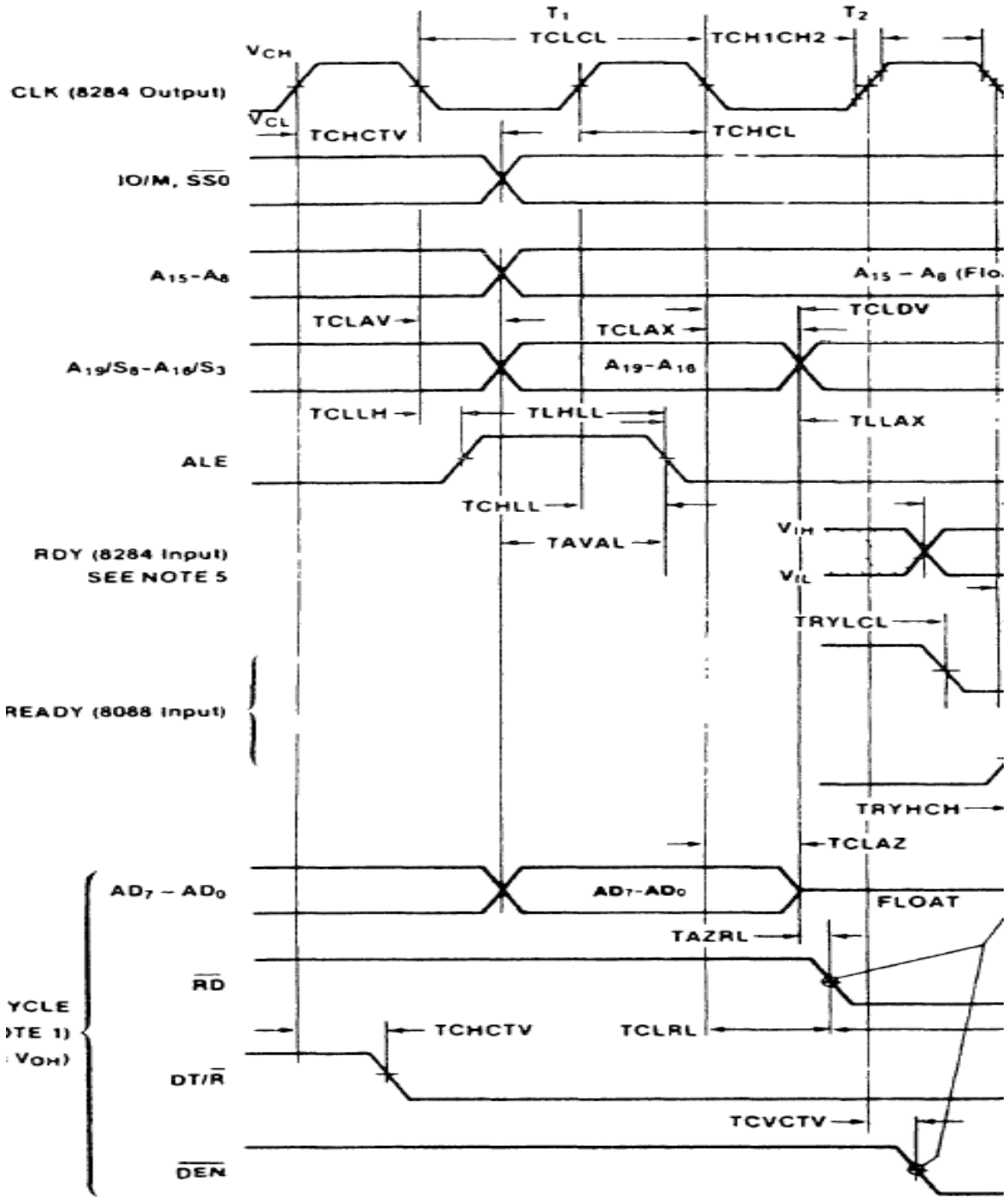
- 8086 use memory and I/O in periods called bus cycles.
- Each cycle equals four system-clocking periods (T states).
- If the clock is operated at 5 MHz, one 8086 bus cycle is complete in 800 ns.
  - basic operating frequency for these processors

- During the first clocking period in a bus cycle, called T1:
  - the address of the memory or I/O location is sent out via the address bus and the address/data bus connections.
  - control signals are also output.
  - indicating whether the address bus contains a memory address or an I/O device (port) number



TCHCTV: Control Active Delay
TCLAV: Address valid delay
TCLLH: ALE active delay
TCLAX: Address hold time
TLHLL: ALE width
TAVAL: Address valid to ALE low
TCHLL: ALE inactive delay

- During T2:
  - the processors issue the $\overline{RD}$ or $\overline{WR}$ signal, $\overline{DEN}$
  - in the case of a write, the data to be written appear on the data bus.
- These events cause the memory or I/O device to begin to perform a read or a write.
- READY is sampled at the end of T_2.
  - if low at this time, T_3 becomes a wait state (T_w)
  - this clocking period is provided to allow the memory time to access data



TAZAL: Address float to read active
TCVCTV: control active delay
TLLAX: Address HOLD time to ALE inactive
TCLDV: Data valid delay
TCHCL: Clock high time
TCH1TCH2: Clock rise time

- If a read bus cycle, the data bus is sampled at the end of T_3.
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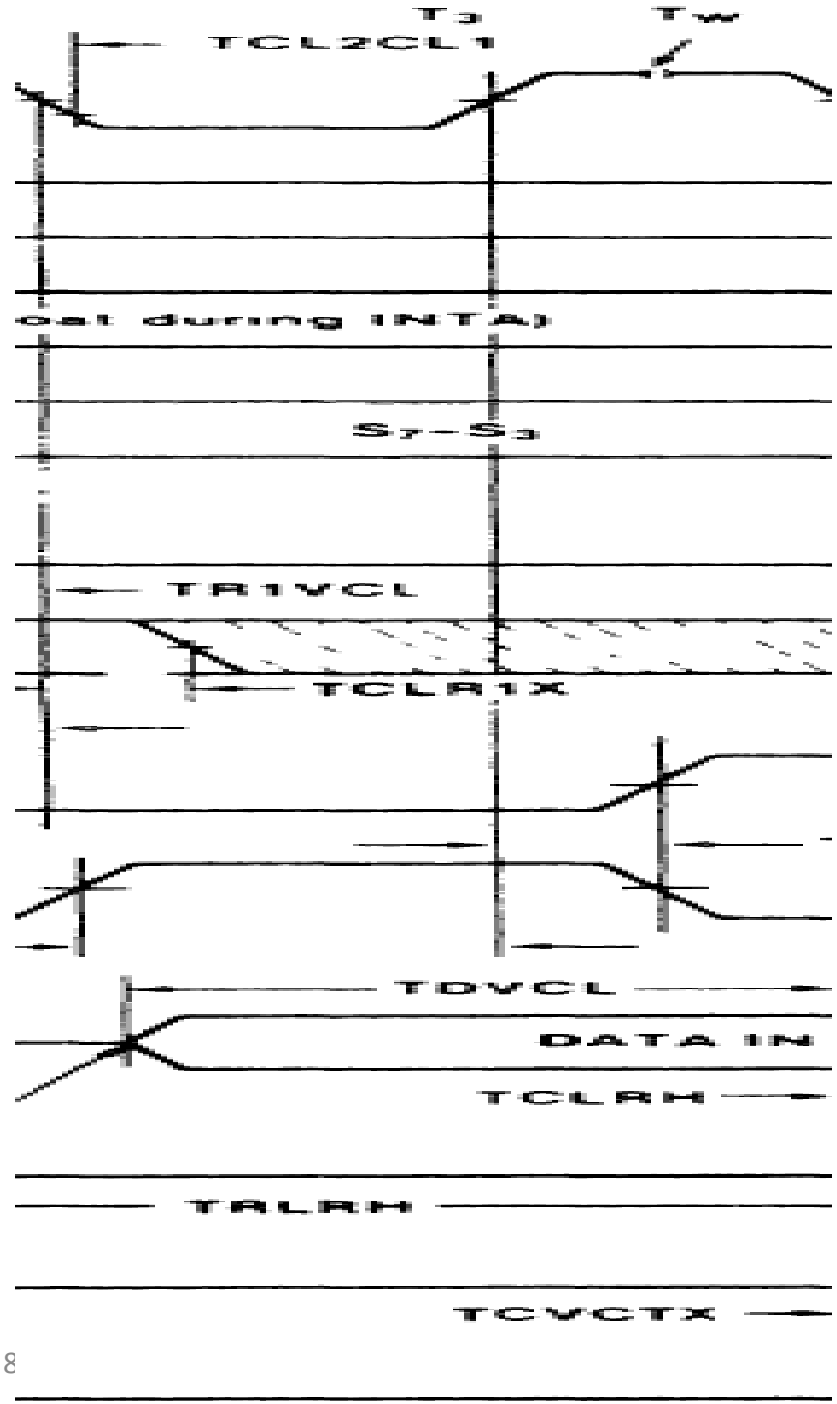
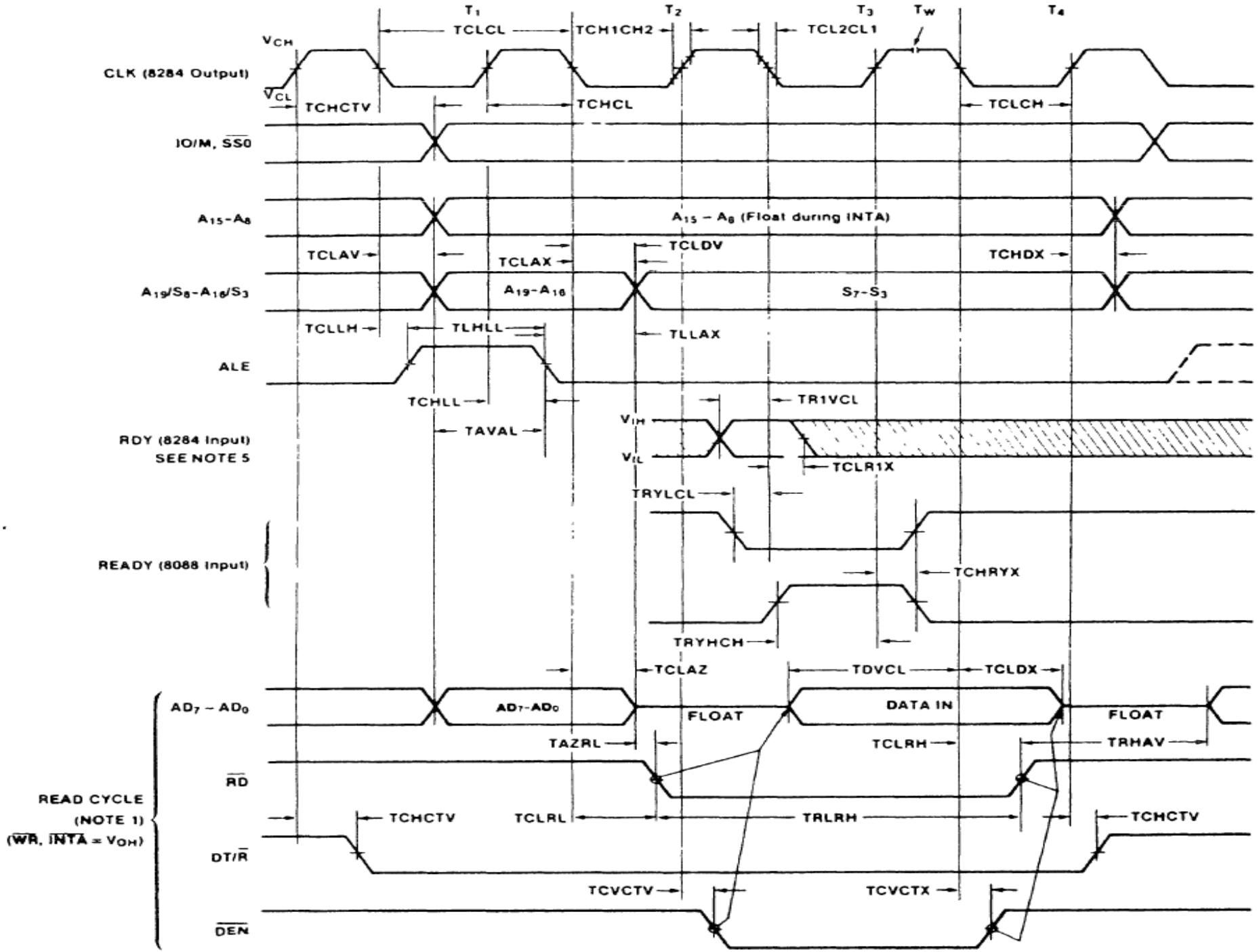


TCL2CL1: Clock fall time
TW:
TR1VCL: Ready setup time
TCLR1X: Ready hold time
TDVCL: Data in set up time
TCVCTX: Control inactive delay
TALAH:

- In T_4, all bus signals are deactivated in preparation for the next bus cycle
  - data bus connections are sampled for data read from memory or I/O


T1
T2
T3
Tw
T4
TCLCL
TCH1CH2
TCL2CL1
VCH
VCL
CLK (8284 Output)
TCHCTV
TCHCL
TCLCH
IO/M, SS0
A15-A8
A15 – A8 (Float during INTA)
TCLAV
TCLAX
TCLDV
TCHDX
A19/S6-A16/S3
A19-A16
S7-S3
TCLLH
TLHLL
TLLAX
ALE
TCHLL
TR1VCL
TAVAL
VIH
VIL
RDY (8284 Input)
SEE NOTE 5
TCLR1X
TRYLCL
READY (8088 Input)
TCHRYX
TRYHCH
TCLAZ
TDVCL
TCLDX
AD7 – AD0
AD7-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
READ CYCLE
(NOTE 1)
(WR, INTA = VOH)
TCHCTV
TCLRL
TRLRH
TCHCTV
DT/R
TCVCTV
TCVCTX
DEN

Timing factors to affect memory operation

- **ACCESS TIME**
- **RD' STROBE**
- **WR' STROBE**

Read Timing

- Important item in the read timing diagram is time allowed for memory & I/O to read data.
- Memory is chosen by its access time.
  - the fixed amount of time the microprocessor allows it to access data for the read operation
- Memory access time starts when the address appears on the memory address bus and continues until the microprocessor samples the memory data at T_3.
  - about three T states elapse between these times
- The address does not appear until T_{CLAV} time (110 ns if a 5 Mhz clock) after the start of T_1.

- T_{CLAV} time must be subtracted from the three clocking states (600 ns) separating the appearance of the address (T_1) and the sampling of the data (T_3).
- The data setup time (T_{DVCL}), which occurs before T_3 must also be subtracted.
- Memory access time is thus three clocking states minus the sum of T_{CLAV} and T_{DVCL}.
- Because T_{DVCL} is 30 ns with a 5 MHz clock, the allowed memory access time is only 460 ns (access time = 600 ns –110 ns – 30 ns).

- Memory devices chosen for connection to the 8086 operating at 5 MHz must be able to access data in less than 460 ns.
  - because of the time delay introduced by the address decoders and buffers in the system
  - a 30- or 40-ns margin should exist for the operation of these circuits

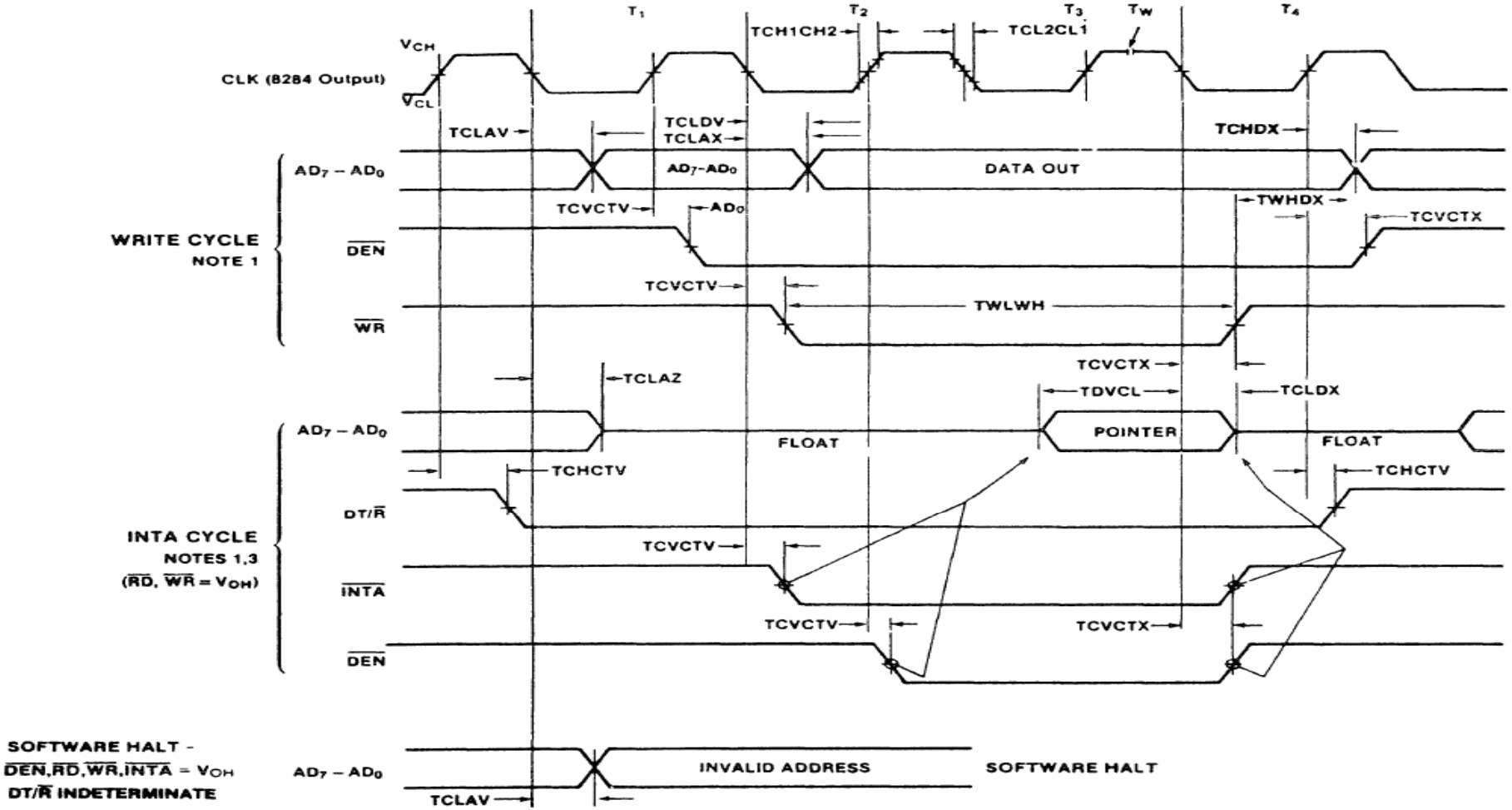
Strobe Width

- The other timing factor to affect memory operation is the width of the $\overline{RD}$ strobe.
- On the timing diagram, the read strobe is given as T_{RLRH}.
- The time for this strobe at a 5 MHz clock rate is 325 ns.
- This is wide enough for almost all memory devices manufactured with an access time of 400 ns or less.

Write Timing

- The $\overline{\text{RD}}$ strobe is replaced by the $\overline{\text{WR}}$ strobe,
  - the ~~da~~ta bus contains information *for* the memory rather than information *from* the memory,
  - DT/R remains a logic 1 instead of a logic 0 throughout the bus cycle

- Memory data are written at the trailing edge of the $\overline{WR}$ strobe.
- Hold time is often less than this.
  - in fact often 0 ns for memory devices
- The width of the WR strobe is T_{WLWH} or 340 ns with a 5 MHz clock.
- This rate is compatible with most memory devices with access time of 400 ns or less.



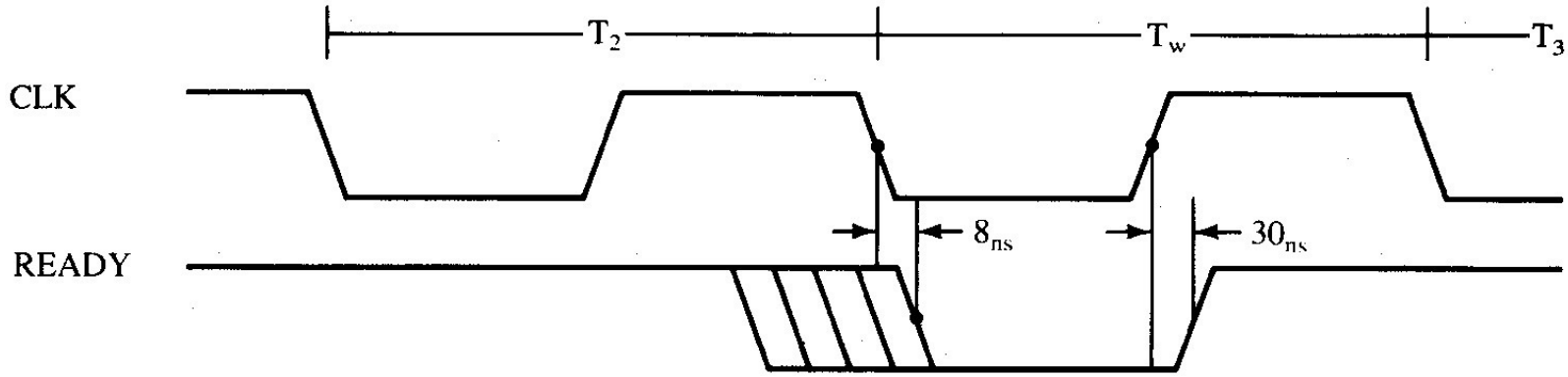
NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED

READY AND THE WAIT STATE

- The READY input is sampled at the end of T_2 and again, if applicable, in the middle of T_w.

- The READY input causes wait states for slower memory and I/O components.
  - a wait state (T_w) is an extra clocking period between T_2 and T_3 to lengthen bus cycle
  - on one wait state, memory access time of 460 ns, is lengthened by one clocking period (200 ns) to 660 ns, based on a 5 MHz clock

Figure 8086 READY input timing.



- If READY is logic 0 at the end of T_2, T_3 is delayed and T_w inserted between T_2 and T_3.
- READY is next sampled at the middle of T_w to determine if the next state is T_w or T_3.

16-Bit MEMORY INTERFACE

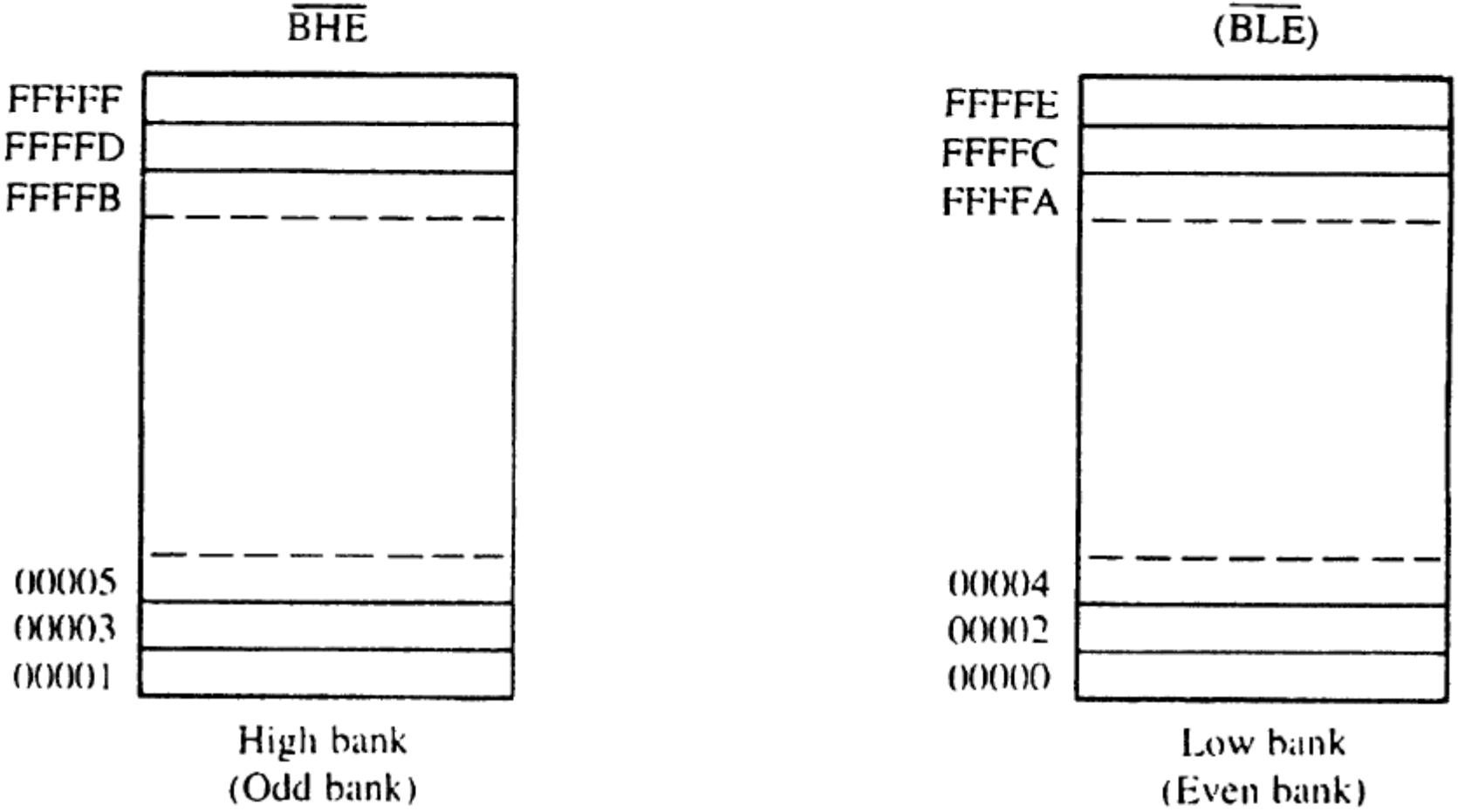
- 8086
  - the data bus is 16 bits wide
  - M/$\overline{IO}$ pin
  - a new control signal called bus high enable
  - 20-bit address bus (A_{19}–A_0) of the 8086

- .

16-Bit Bus Control

- processor must be able to write data to any 16-bit location—or any 8-bit location
- This means the 16-bit data bus must be divided into two separate sections (or **banks**) 8 bits wide so that the processor can write to either half (8-bit) or both halves (16-bit).

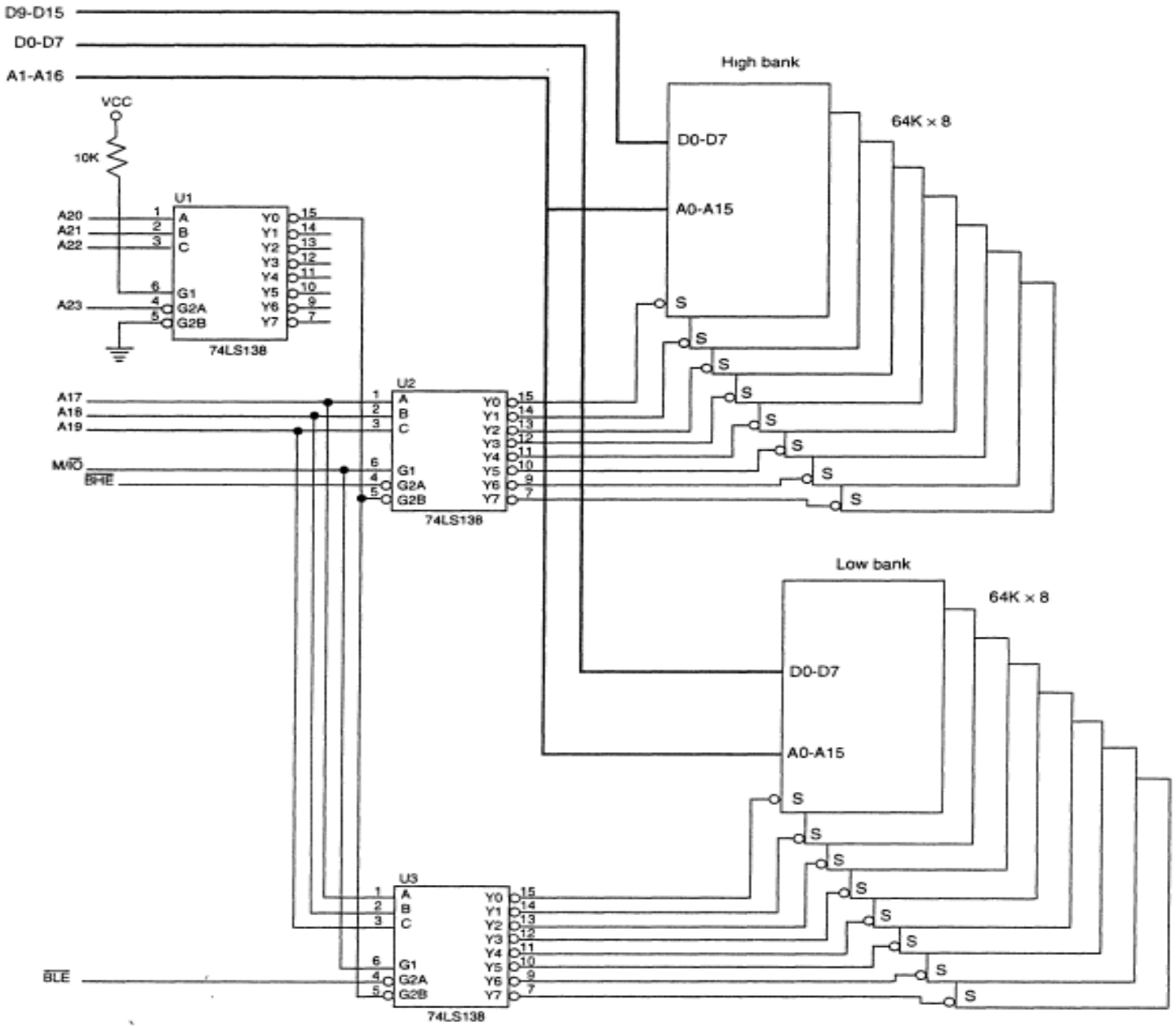
Figure The high (odd) and low (even) 8-bit memory banks of the 8086 microprocessor.



Note: A_0 is labeled $\overline{BLE}$ (Bus low enable) on the 80386SX.

- Bank selection is accomplished in two ways:
  - separate write signal is developed to select a write to each bank of the memory
    - least costly approach to memory interface.
  - separate decoders are used for each bank
    - used to achieve the most efficient use of the power supply.
    - as only banks selected are enabled

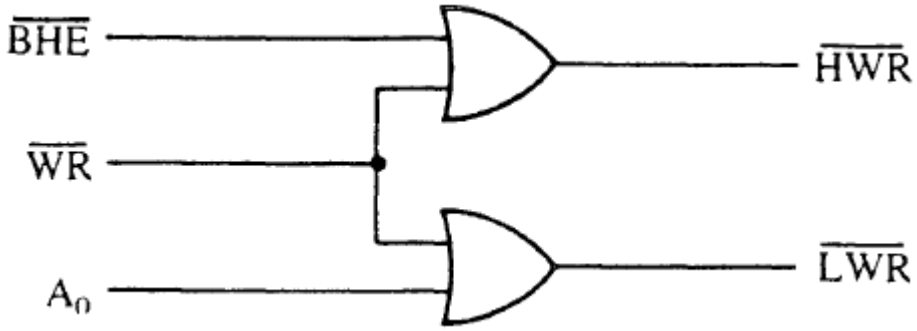
Figure Separate bank decoders.



Separate Bank Write Strobes

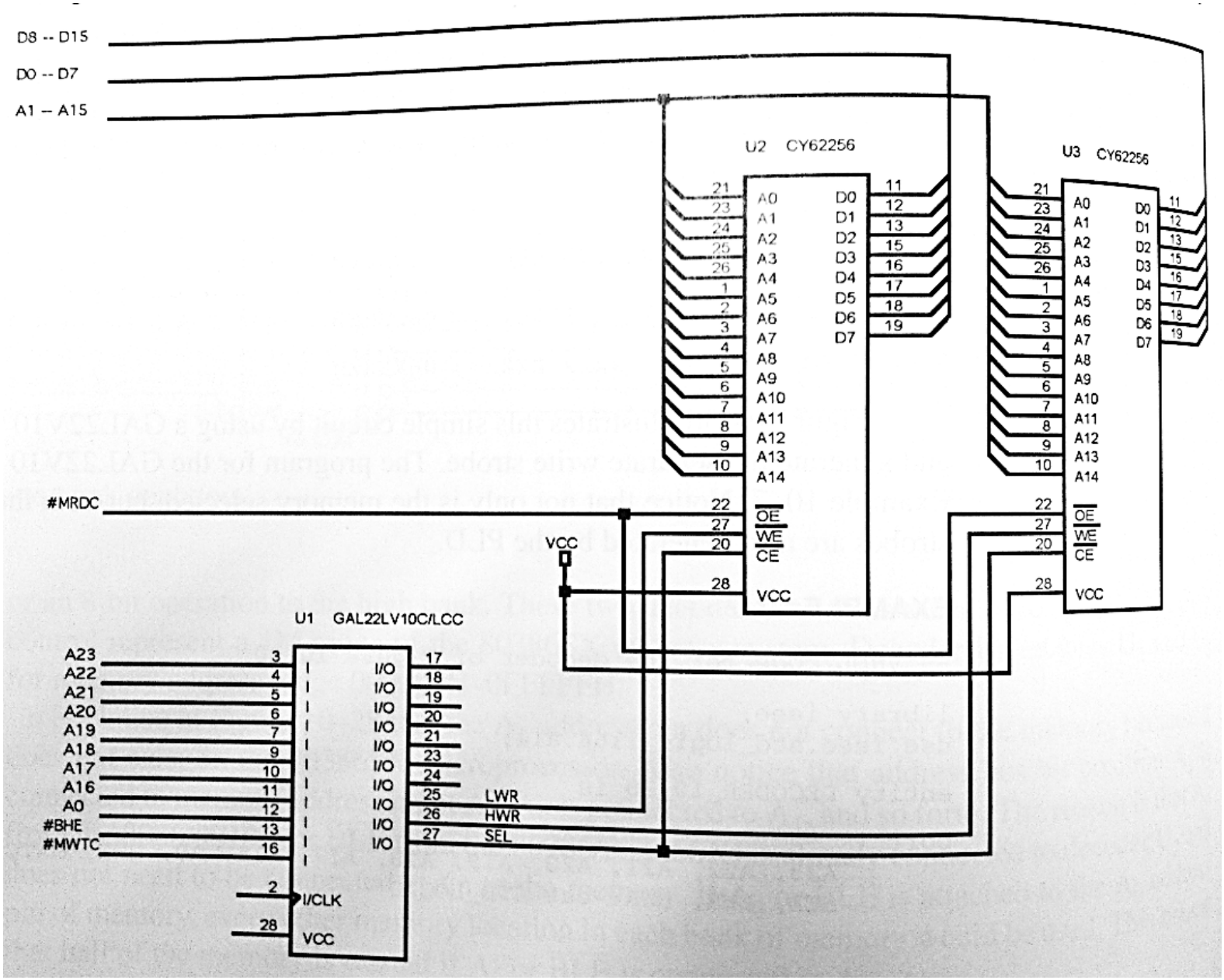
- The effective way to handle bank selection is a separate write strobe for each bank.
  - this requires only one decoder to select a 16-bit-wide memory, which saves money
- Separate read strobes for each bank are usually unnecessary because 8086 read only the byte of data they need at any given time from half of the data bus.

Figure The memory bank write selection input signals: $\overline{\text{HWR}}$ (high bank write) and $\overline{\text{LWR}}$ (low bank write).



- memory in a system using separate write strobes is decoded as 16-bit-wide

Figure A 16-bit-wide memory interfaced at memory locations 06000H–06FFFH.



PLD

PLD Programmable Decoders

- Three SPLD (**simple PLD**) devices function in the same manner but have different names:
  - PLA (**programmable logic array**)
  - PAL (**programmable array logic**)
  - GAL (**gated array logic**)

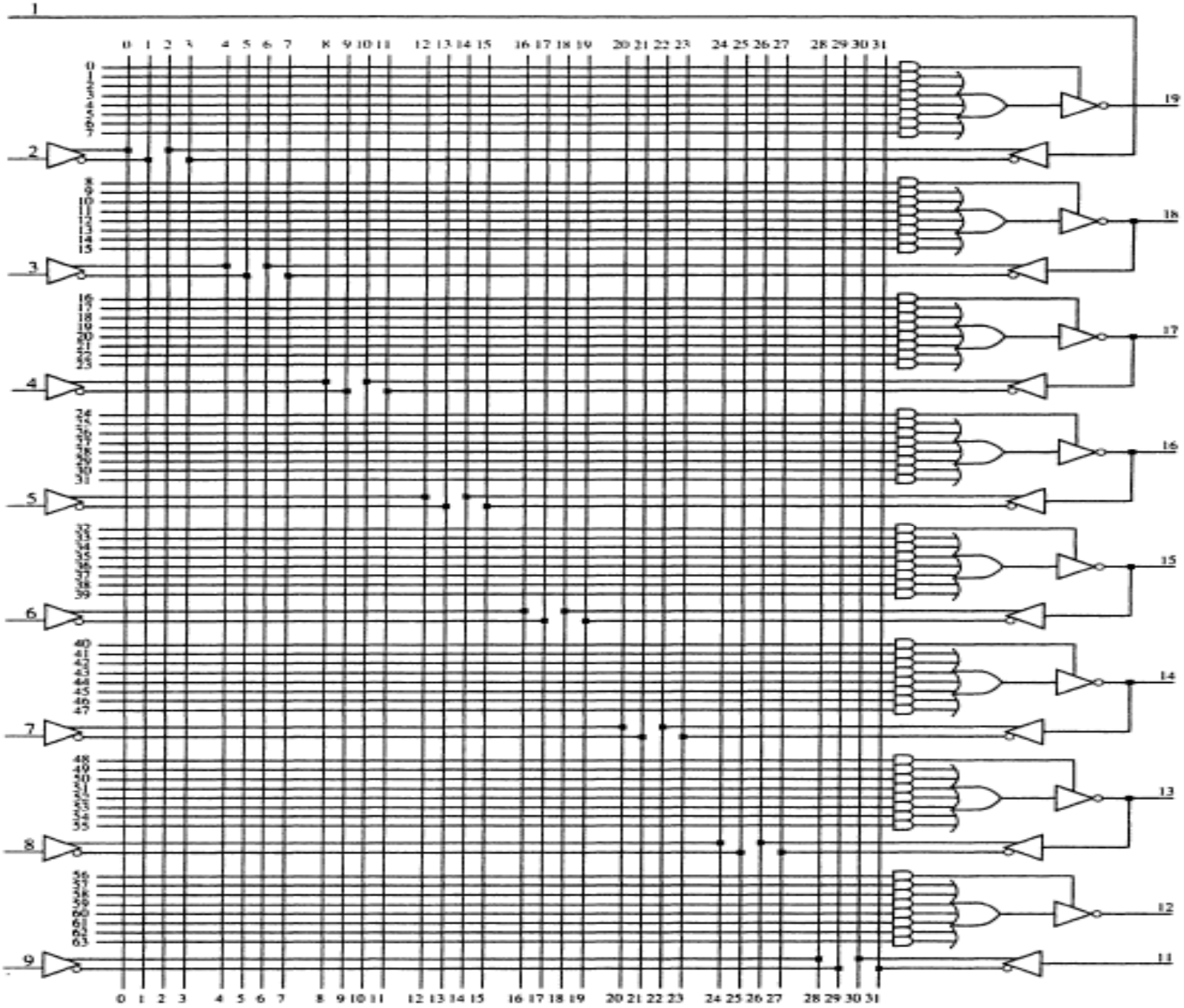
  - all are arrays of programmable logic elements

- Other PLDs available:
  - CPLDs (**complex programmable logic devices**)
  - FPGAs (**field programmable gate arrays**)
  - FPICs (**field programmable interconnect**)

- If the concentration is on decoding addresses, the SPLD is used.
- If the concentration is on a complete system, then the CPLD, FPLG, or FPIC is used to implement the design.
- These devices are also referred to as an ASIC (**application-specific integrated circuit**).

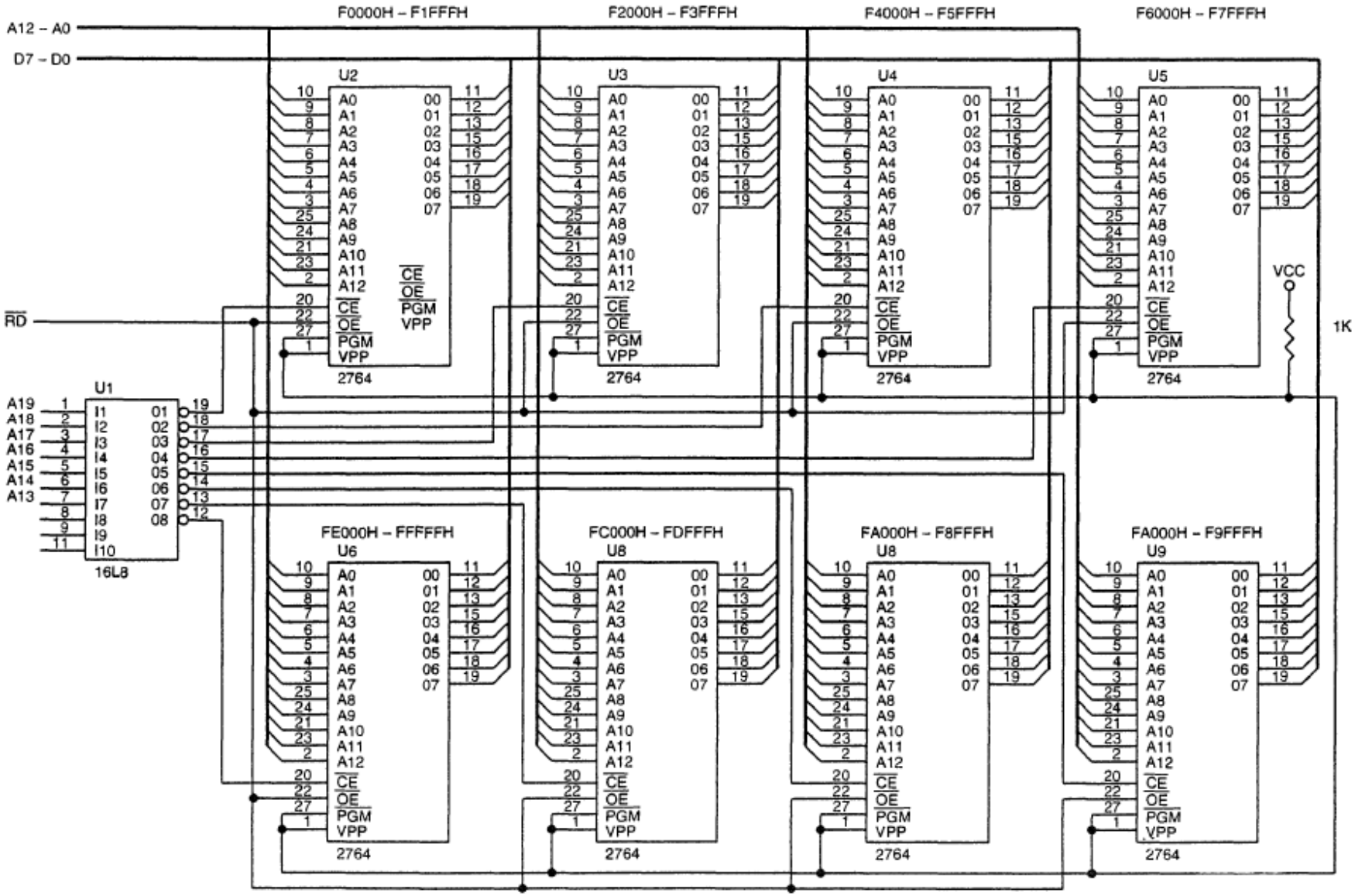
Combinatorial Programmable Logic Arrays

- It has 10 fixed inputs, two fixed outputs, and six pins programmable as inputs or outputs.
- Programming is accomplished by blowing fuses to connect inputs to the OR gate array.
- It is ideal as a decoder because of its structure, also because outputs are active low.

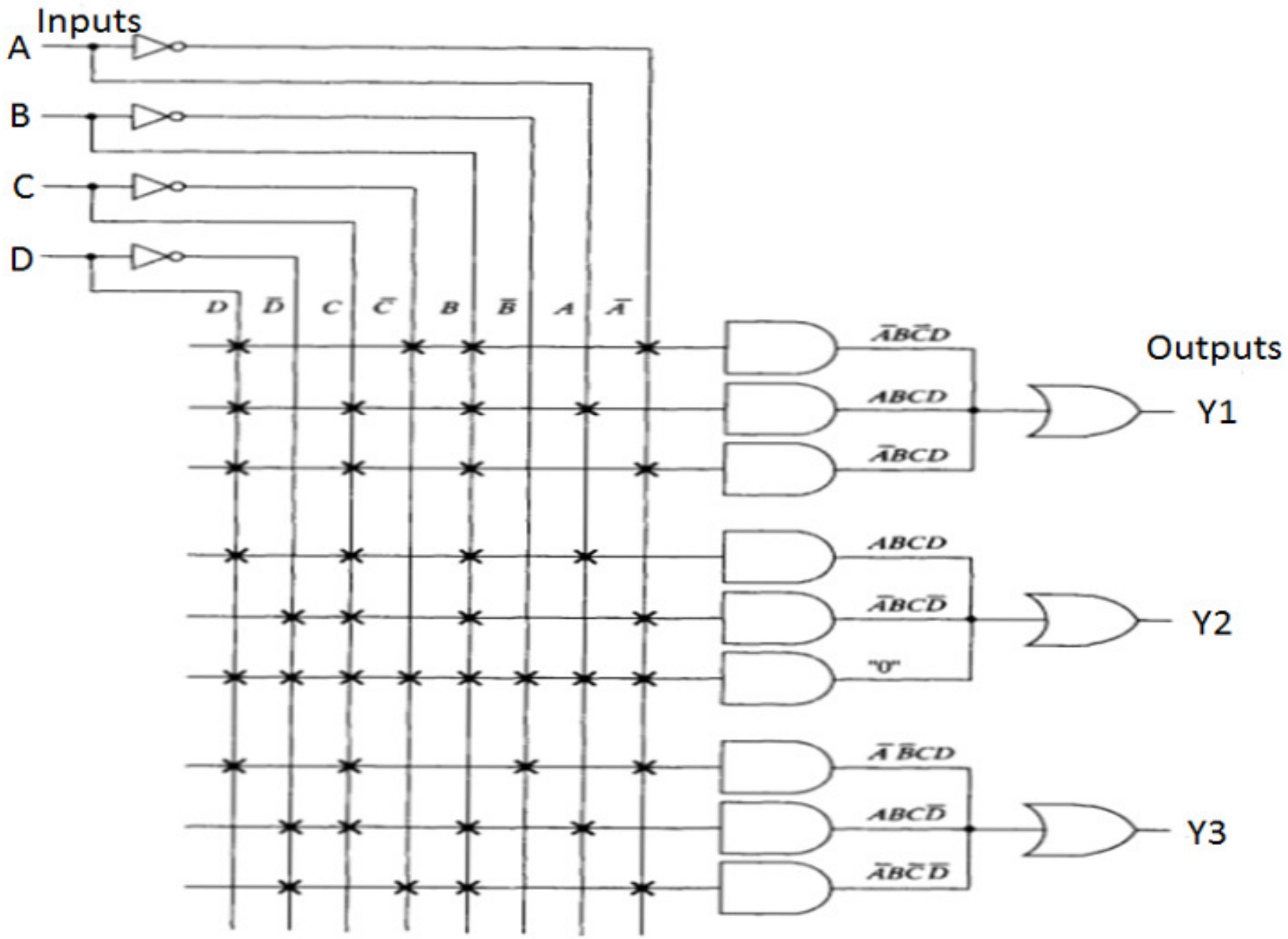

1
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
2
3
4
5
6
7
8
9
19
18
17
16
15
14
13
12
11

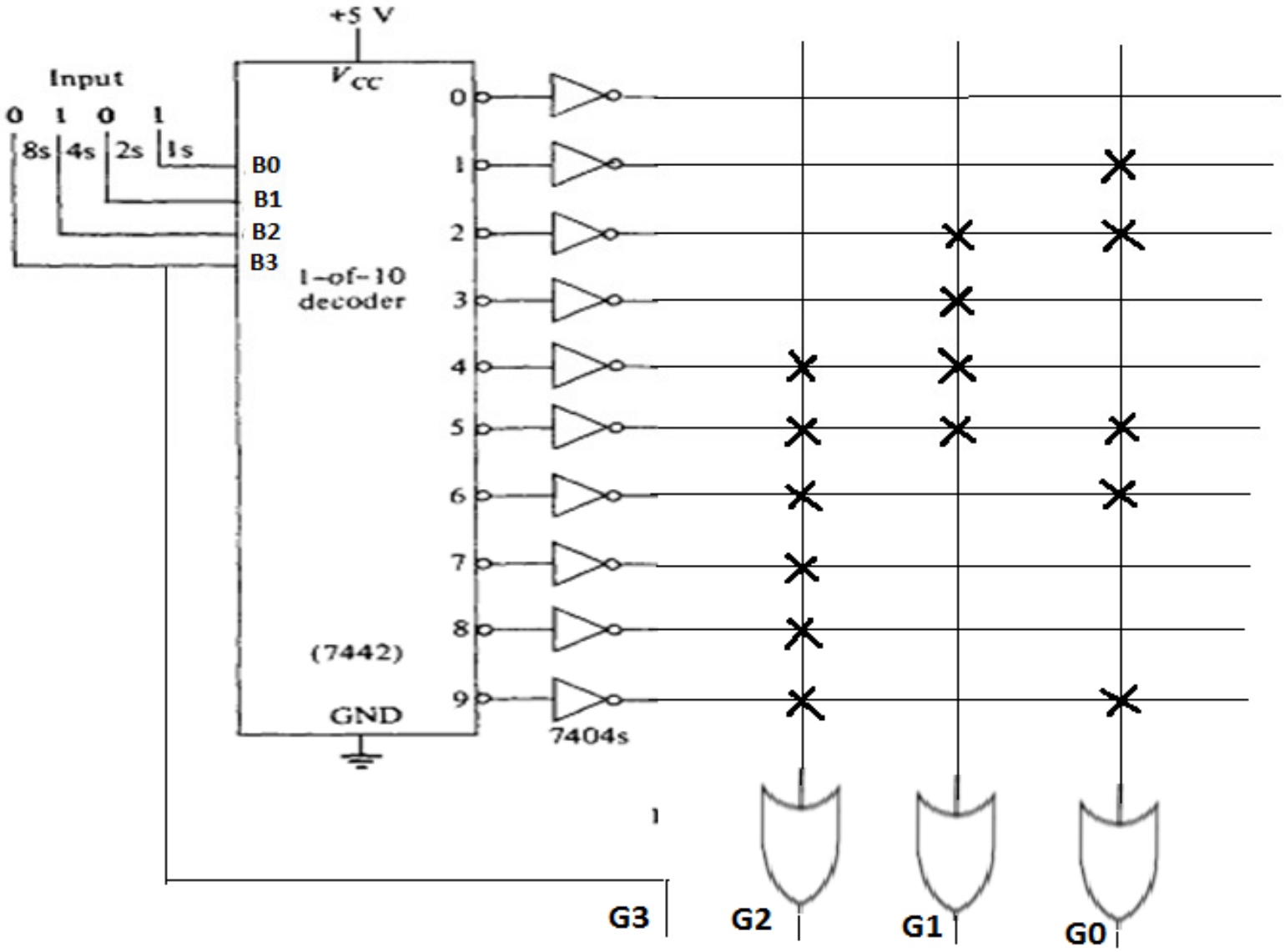
- A PAL is programmed with software such as PALASM, the PAL assembler program.
- PLD design is accomplished using HDL (**hardware description language**) or VHDL (**verilog HDL**).
  - VHDL and its syntax are currently the industry standard for programming PLD devices
- Various editors attempt to ease the task of defining the pins.
  - the authors believe it is easier to use NotePad

Figure A PAL16L8 that decodes 8 2764 (8K x 8) memory devices.



Solution :


Inputs
A
B
C
D
D
$\bar{D}$
C
$\bar{C}$
B
$\bar{B}$
A
$\bar{A}$
$\bar{A}\bar{B}\bar{C}D$
ABCD
$\bar{A}BCD$
ABCD
$\bar{A}BC\bar{D}$
"0"
$\bar{A}\bar{B}CD$
$AB\bar{C}D$
$\bar{A}B\bar{C}\bar{D}$
Outputs
Y1
Y2
Y3


+5 V
V_{CC}
Input
0 1 0 1
8s 4s 2s 1s
B0
B1
B2
B3
1-of-10
decoder
(7442)
GND
0
1
2
3
4
5
6
7
8
9
7404s
1
G3
G2
G1
G0

Q.1. Find out Expression for X1 and X2