TUT-IV

04.09.2012

Example -1

Design a synchronous mod 5 counter using JK flip-flop

ANS:

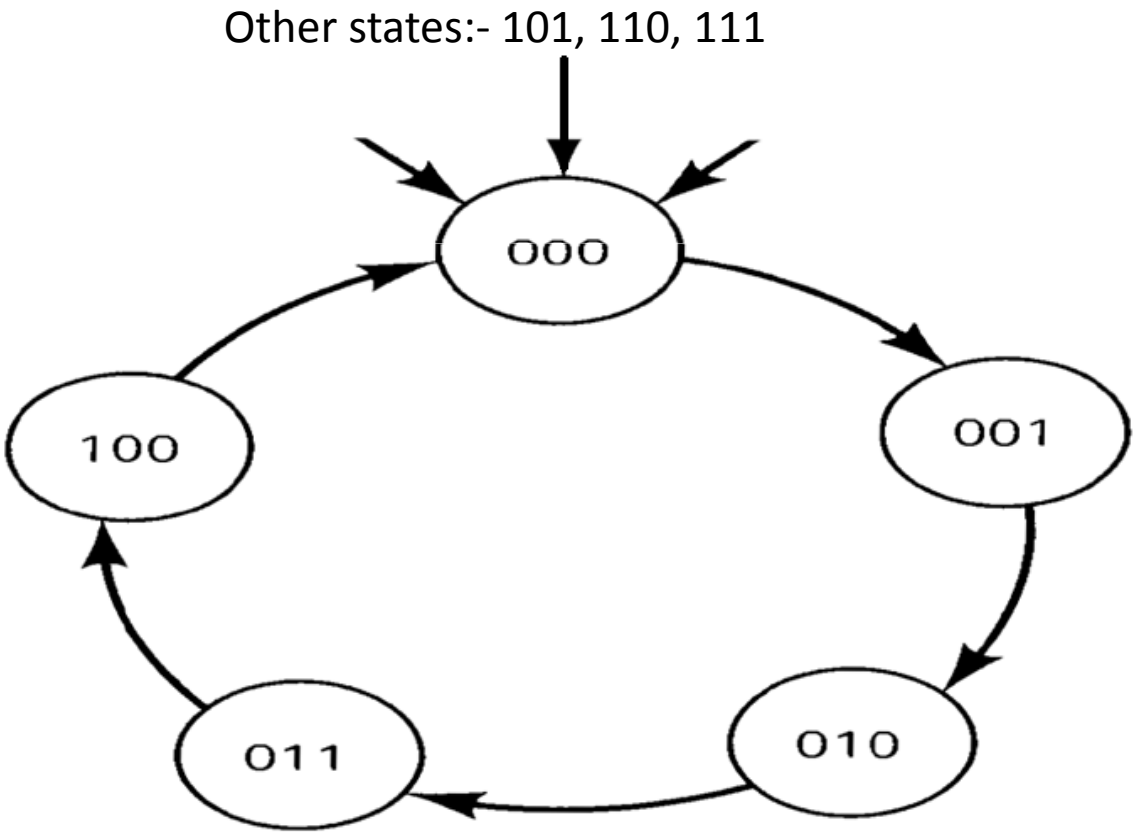
Steps to follow:-

1. Determine the number of flip-flops
2. Draw state diagram
3. Get excitation table
4. Obtain the minimal expressions for flip-flop inputs
5. Draw the logic diagram

Step1:- Determine the number of flip-flops

For MOD 5, $2^n >= 5$; Hence n= 3 FFs are required

Step2:- Draw state diagram



Flip-Flop Excitation Tables

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	F.F. Input	
$Q(t)$	$Q(t+1)$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

0 0 (No change)
0 1 (Reset)

1 0 (Set)
1 1 (Toggle)

0 1 (Reset)
1 1 (Toggle)

0 0 (No change)
1 0 (Set)

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

A synchronous mod 5 counter using JK flip-flop

Present state			Next state			Required inputs					
Q3	Q2	Q1	Q3	Q2	Q1	J3	K3	J2	K2	J1	K1
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

Present State	Next State	F.F. Input	
$Q(t)$	$Q(t+1)$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

A synchronous mod 5 counter using JK flip-flop

K-map for J1,k1

Present state			Next state			Required inputs					
Q3	Q2	Q1	Q3	Q2	Q1	J3	K3	J2	K2	J1	K1
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

	Q1’	Q1
Q3’Q2’	1	X
Q3’Q2	1	X
Q3Q2	0	X
Q3Q2’	0	X

J1=Q3’

	Q1’	Q1
Q3’Q2’	X	1
Q3’Q2	X	1
Q3Q2	X	1
Q3Q2’	X	1

K1=1

A synchronous mod 5 counter using JK flip-flop

Present state			Next state			Required inputs					
Q3	Q2	Q1	Q3	Q2	Q1	J3	K3	J2	K2	J1	K1
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

	Q1’	Q1
Q3’Q2’	X	X
Q3’Q2	0	1
Q3Q2	1	1
Q3Q2’	X	X

K2=Q3+Q1

	Q1’	Q1
Q3’Q2’	0	1
Q3’Q2	X	X
Q3Q2	X	X
Q3Q2’	0	0

J2=Q1Q3’

A synchronous mod 5 counter using JK flip-flop

Present state			Next state			Required inputs					
Q3	Q2	Q1	Q3	Q2	Q1	J3	K3	J2	K2	J1	K1
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

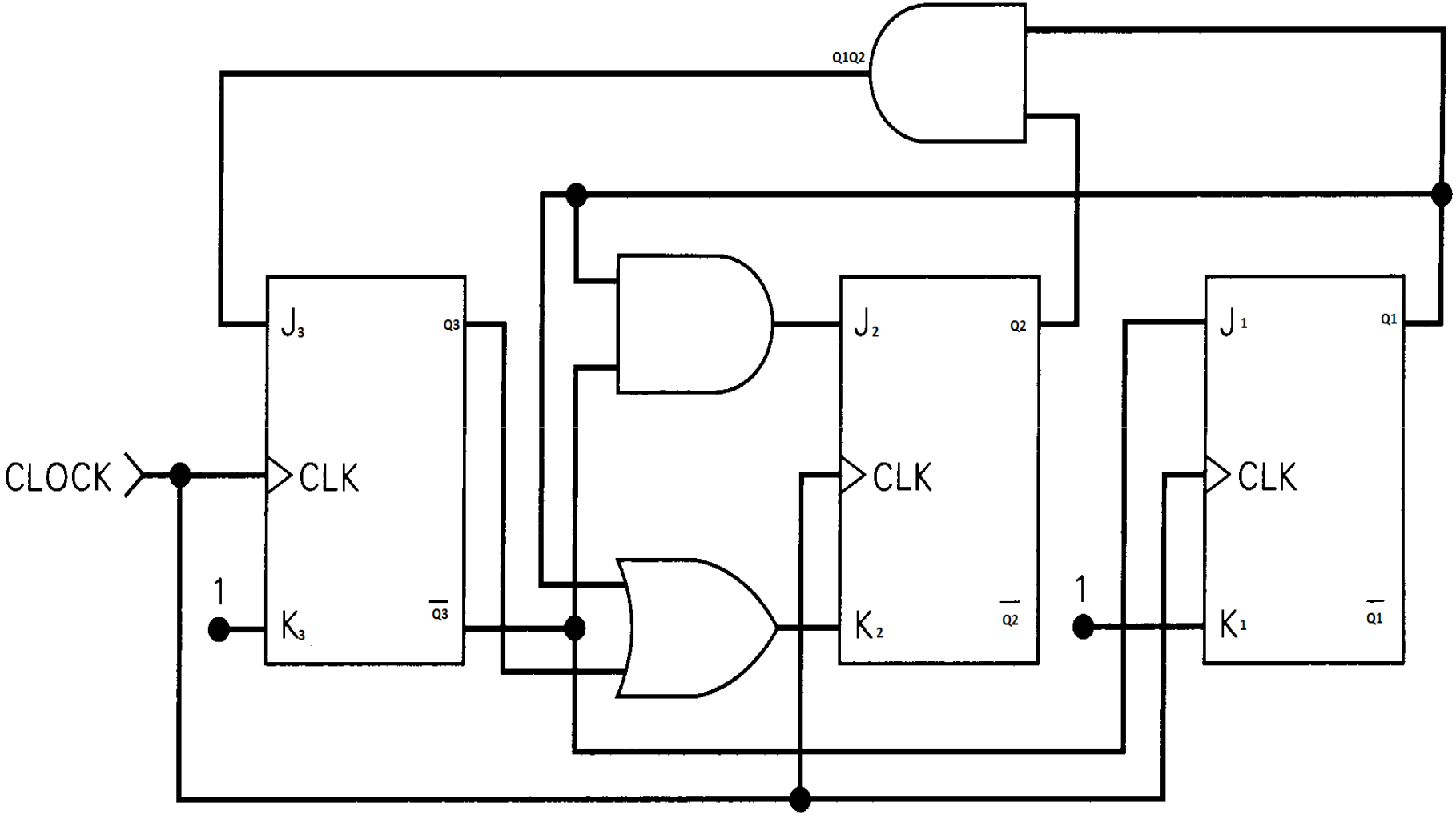
	Q1’	Q1
Q3’Q2’	X	X
Q3’Q2	X	X
Q3Q2	1	1
Q3Q2’	1	1

K3=1

	Q1’	Q1
Q3’Q2’	0	0
Q3’Q2	0	1
Q3Q2	X	X
Q3Q2’	X	X

J3=Q2Q1

A synchronous mod 5 counter using JK flip-flop



Example -2

Design a modulo-8 counter which counts in the way specified below, use J-K Flip-Flop.

Decimal	Gray
0	000
1	001
2	011
3	010
4	110
5	111
6	101
7	100

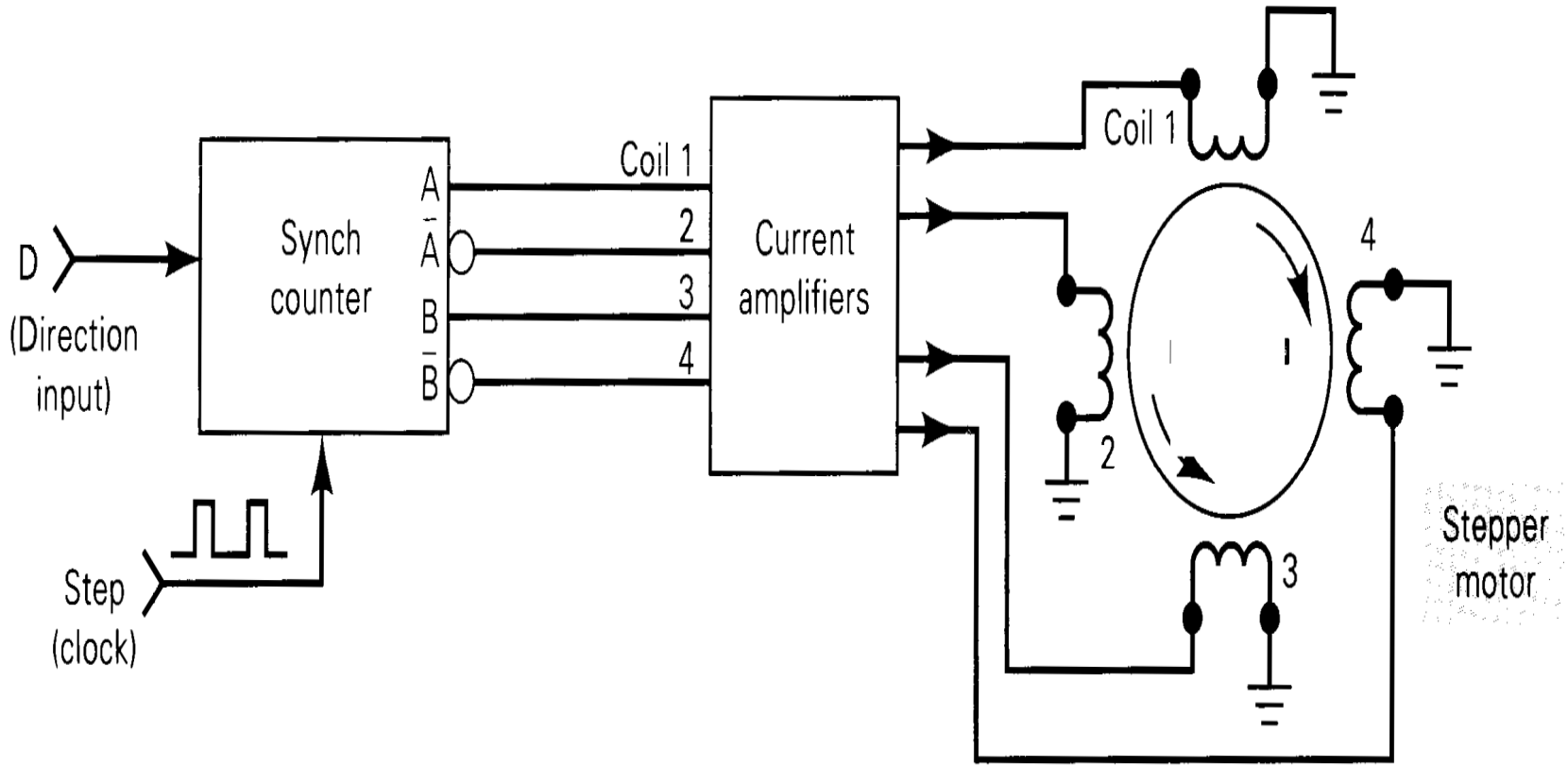
Prepare a excitation table for J-K FF for corresponding present state & next state

TRUTH TABLE

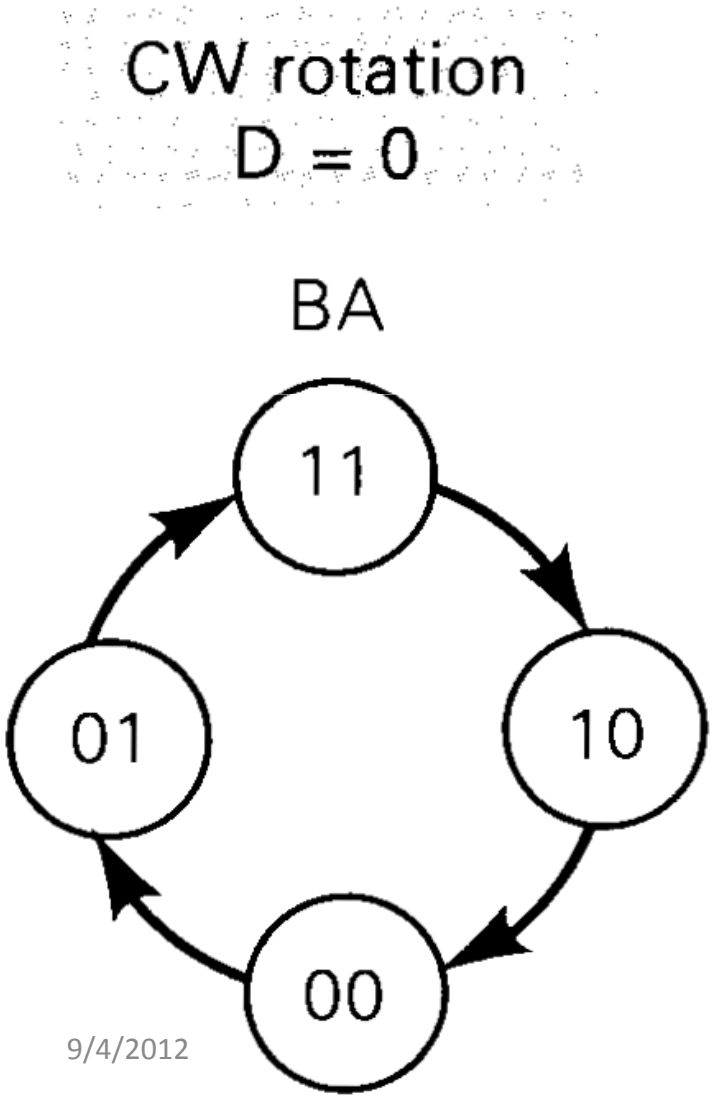
Present State			Next state		
y_3	y_2	y_1	y_{3+}	y_{2+}	y_{1+}
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

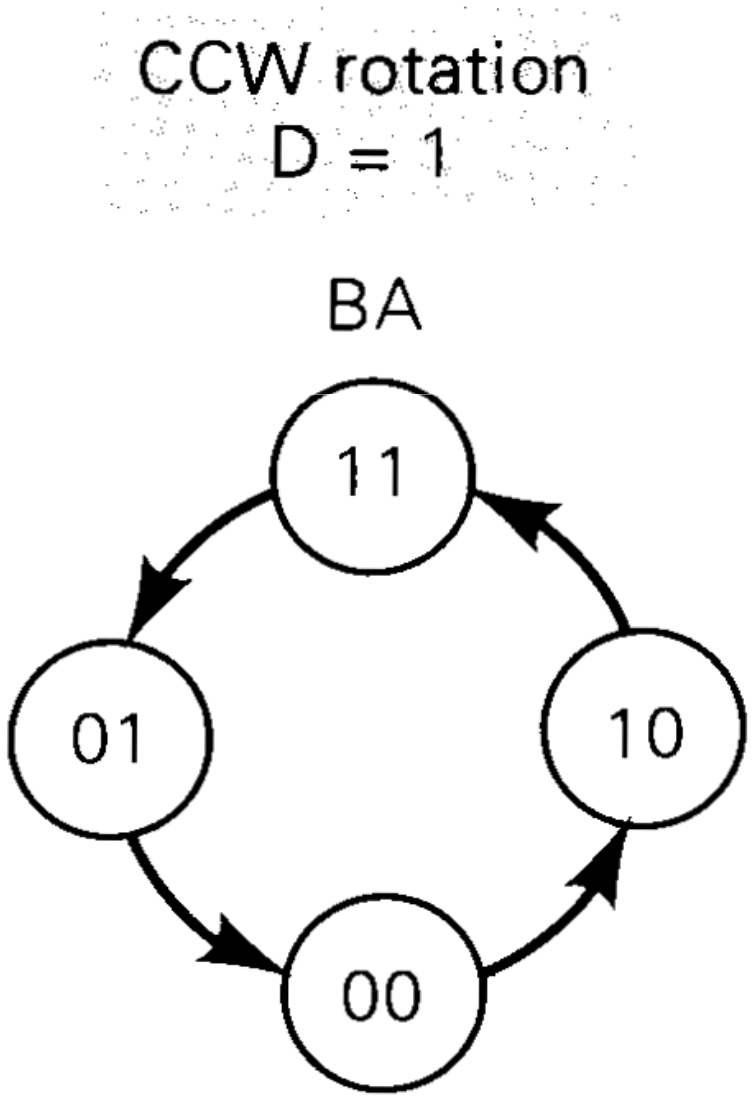
Counter Application: Stepper Motor control

For the motor to rotate properly, coils 1 & 2 must be in opposite states also coil 3 & 4 must be in opposite state. Output of 2-bit synchronous counter is used to control current in the four coils.



State diagram





K-map simplification

Prepare a excitation table for J-K FF for corresponding present state & next state

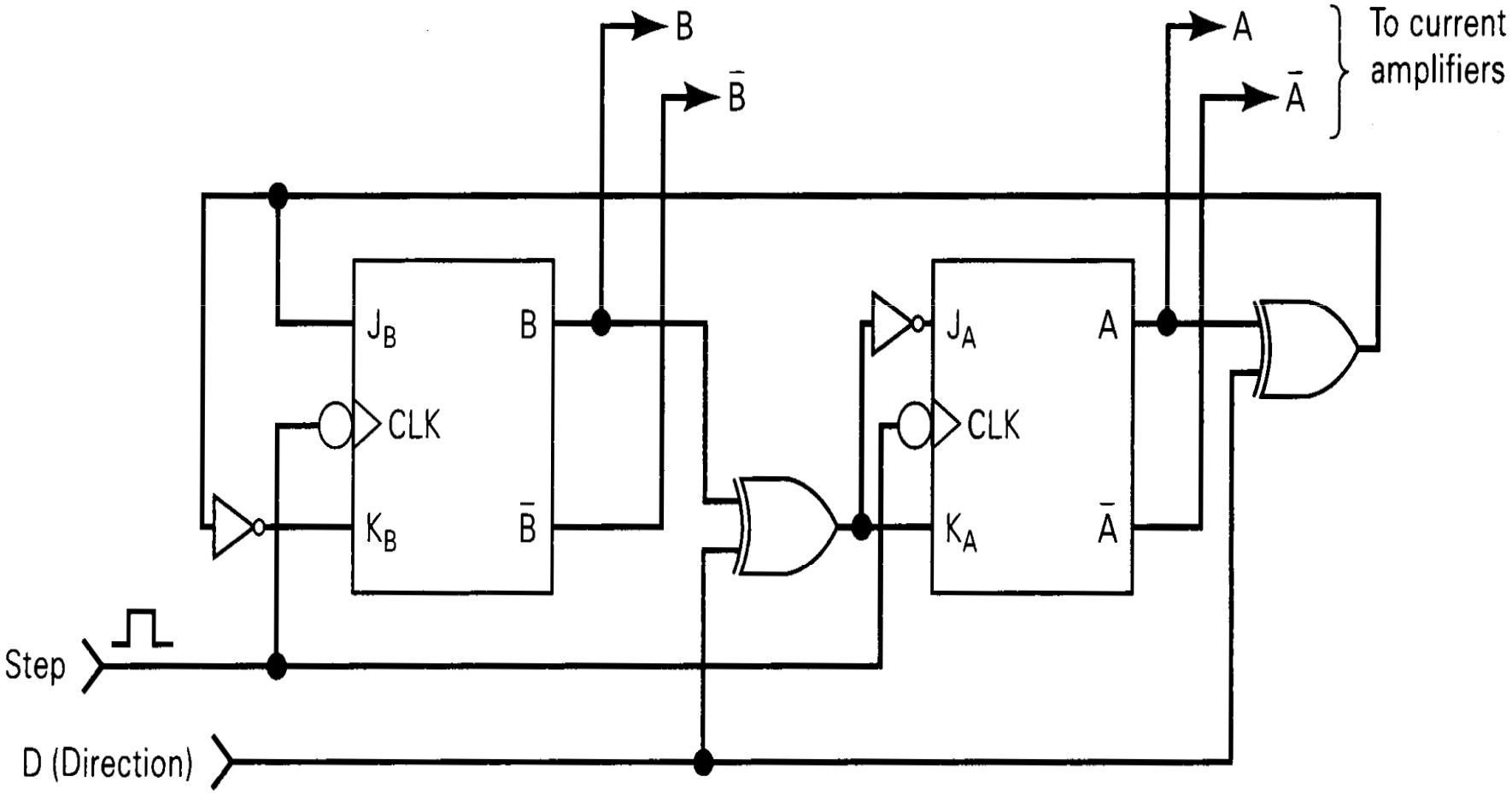
$$J_A = \overline{D}\,\overline{B} + DB$$
$$= \overline{D \oplus B}$$

$$K_A = \overline{D}B + D\overline{B}$$
$$= D \oplus B$$

$$J_B = \overline{D}A + D\overline{A}$$
$$= D \oplus A$$

$$K_B = \overline{D\overline{A} + DA}$$
$$= \overline{D \oplus A}$$

Final Circuit



Example 3

Design a sequence detector using D flip-flops. The circuit to be designed is to detect a sequence of 1001 from an input string of data, which is serial in nature. An output of 1 is generated when the sequence 1001 is detected.

Work out the state diagram for the detector (overlapping sequences also to be taken into account)

DESIGN PROCEDURE STEPS:

Step 1:

Make a state table based on the problem statement. The table should show the present states, inputs, next states and outputs. (It may be easier to find a state diagram first, and then convert that to a table.)

Step 2:

Assign binary codes to the states in the state table, if you haven't already. If you have n states, your binary codes will have at least $\lceil \log_2 n \rceil$ digits, and your circuit will have at least $\lceil \log_2 n \rceil$ flip-flops.

Step 3:

For each flip-flop and each row of your state table, find the flip-flop input values that are needed to generate the next state from the present state. You can use flip-flop excitation tables here.

Step 4:

Find simplified equations for the flip-flop inputs and the outputs.

Step 5:

Build the circuit!