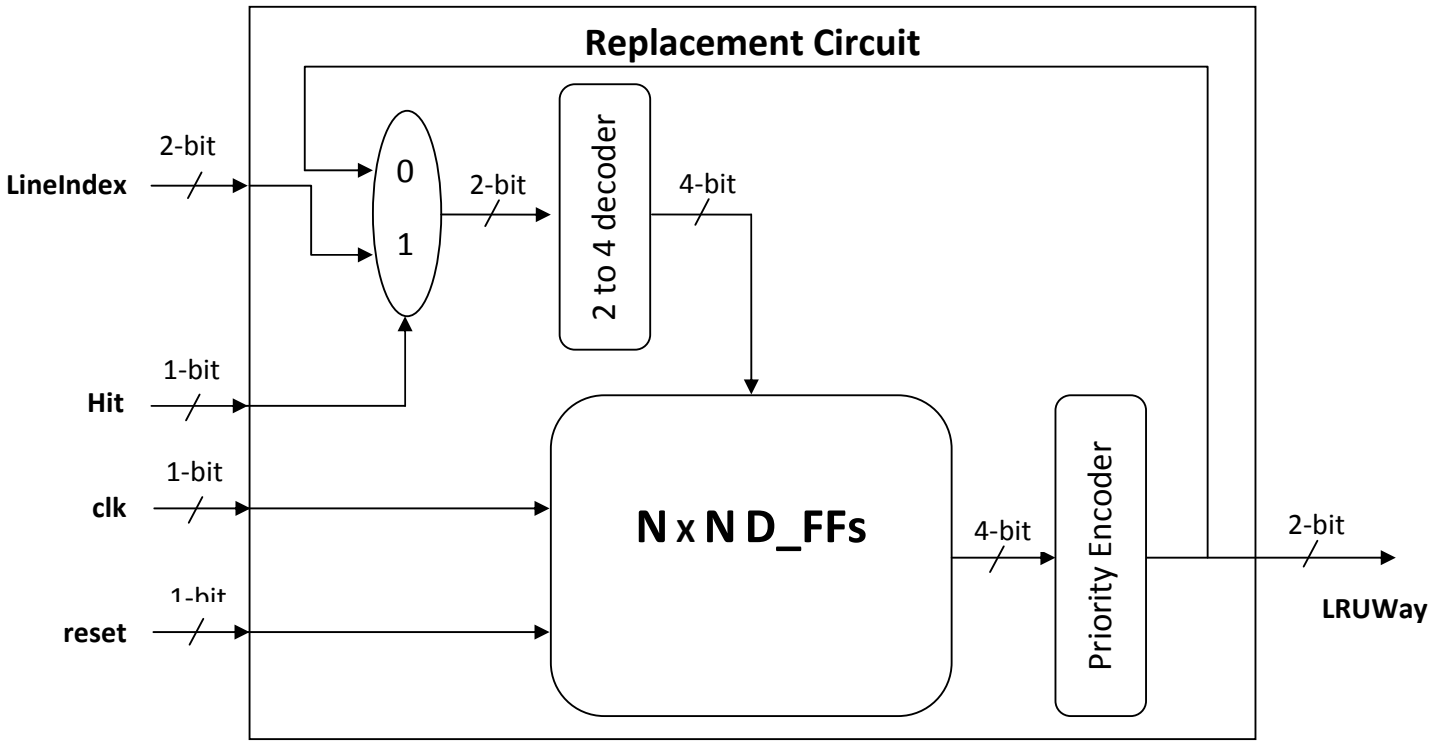
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K.
BIRLA Goa Campus
Second Semester 2012-2013
IS F242 Computer Organization
Lab – 6, 9th April 2013

Design and implement the following using verilog HDL in Xilinx software with the following specifications.



Modules

1. module D_FF(input clk, input set, input reset, output reg Q);
2. module NxN_DFFs(input clk, input reset, input [3:0] decOut, output reg [3:0] NxNOut);
3. module prio_Enc(input [3:0] NxNOut, output reg [1:0] LRUWay);
4. module mux(input [1:0] LineIndex, input [1:0] LRUWay, input Hit, output reg [1:0] muxOut);
5. module dec(input [1:0] muxOut, output reg [3:0] decOut);
6. module LRU(input [1:0] LineIndex, input clk, input reset, input Hit, output reg [1:0] LRUWay);
7. TestBench;