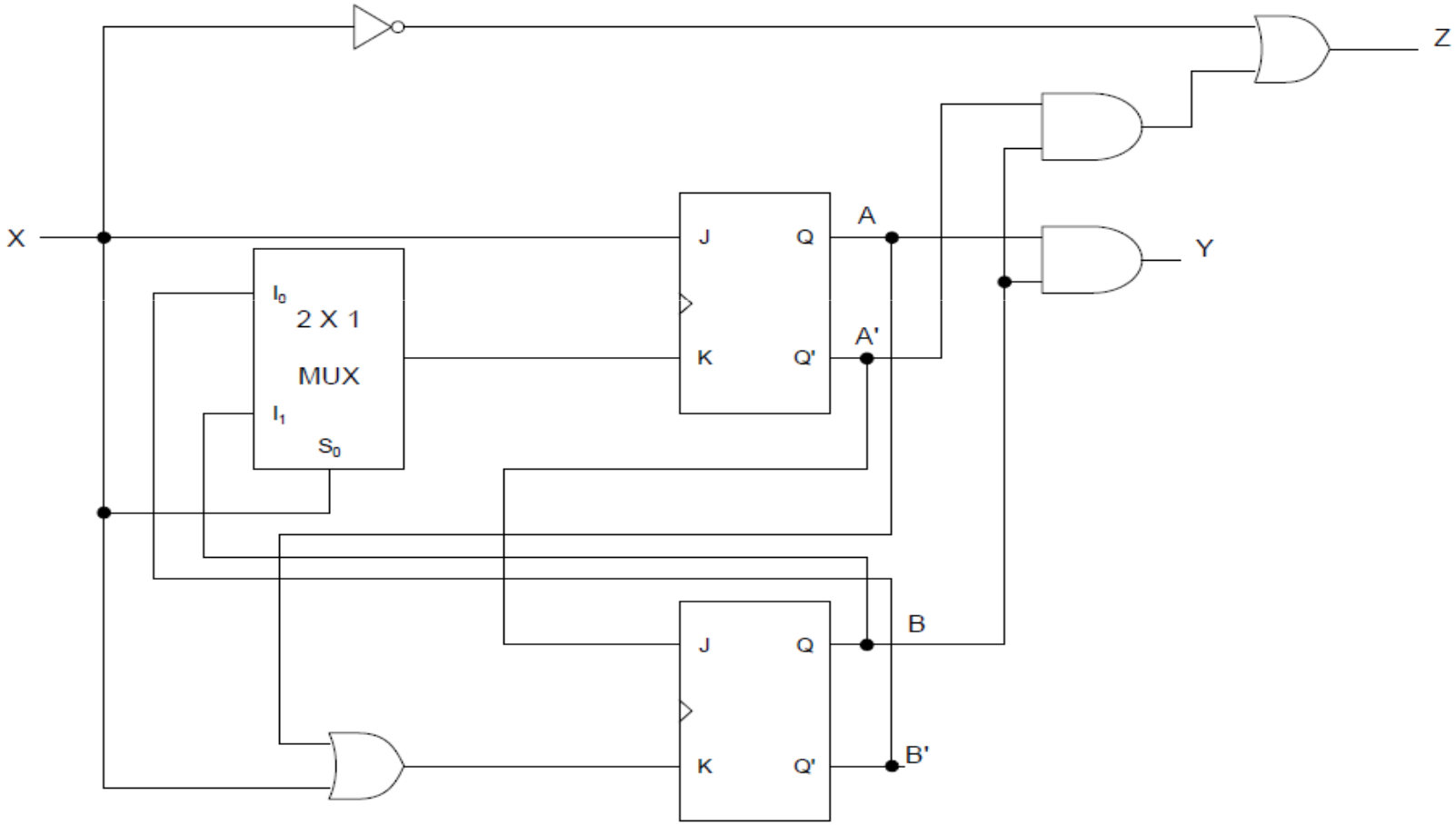
Q1:- Derive the state table and the state diagram of the sequential circuit shown in Fig

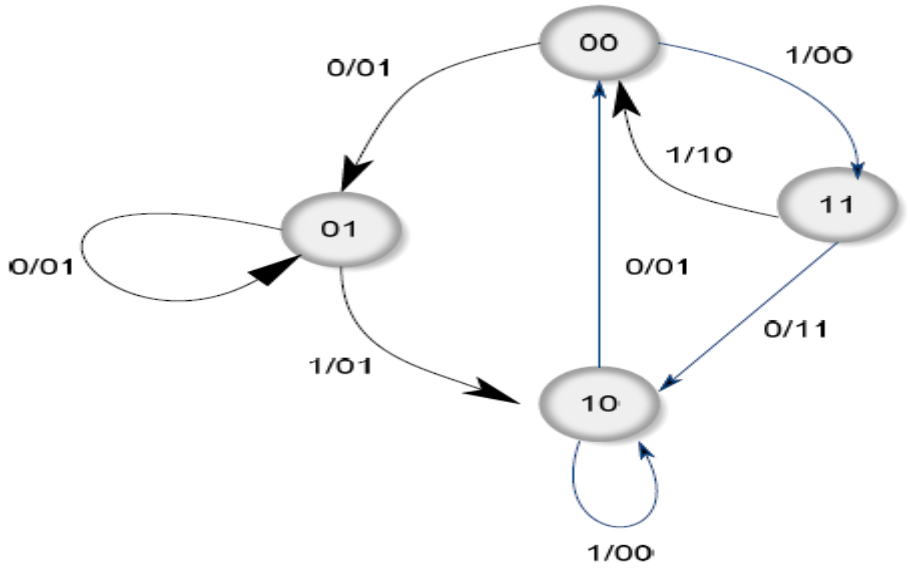


Q1:- Answer

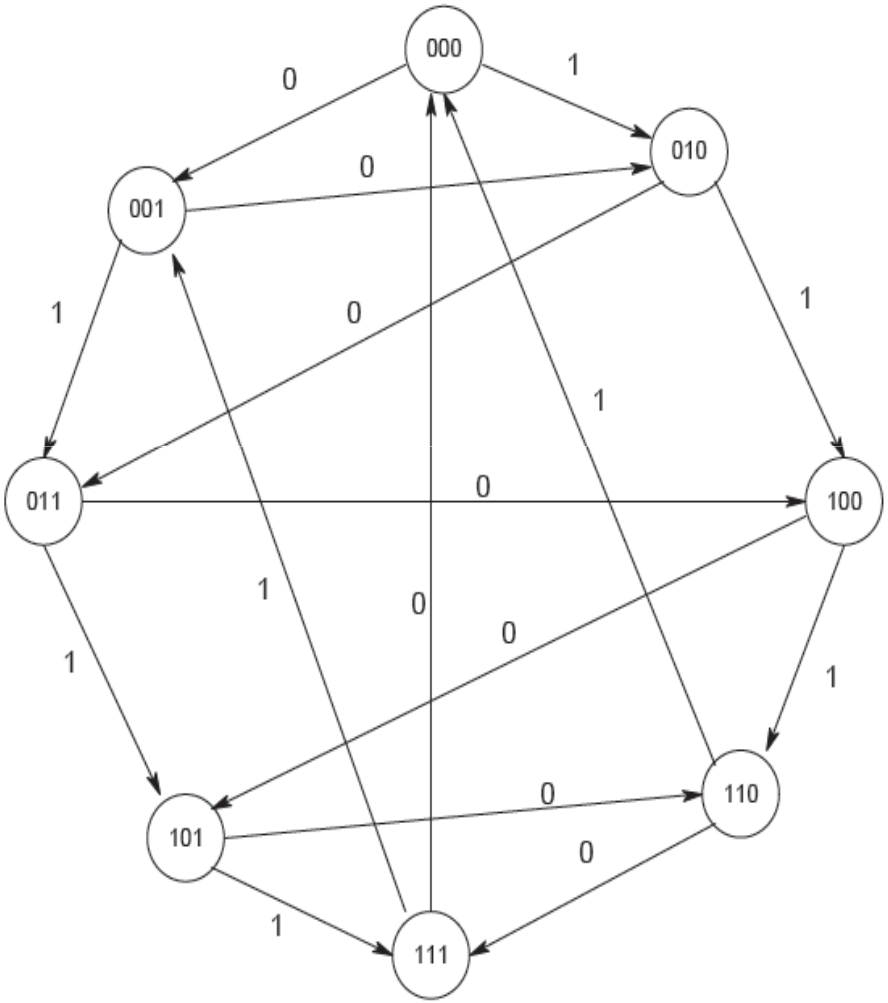
JA = x
KA= B’x’+Bx
JB= A’
KB=A+x
Y=AB
Z=A’B+x’

Q1:- Answer

Present State		Input	Next State		Output		Flip-flop Input			
A	B	x	A	B	Y	Z	J_A	K_A	J_B	K_B
0	0	0	0	1	0	1	0	1	1	0
0	0	1	1	1	0	0	1	0	1	1
0	1	0	0	1	0	1	0	0	1	0
0	1	1	1	0	0	1	1	1	1	1
1	0	0	0	0	0	1	0	1	0	1
1	0	1	1	0	0	0	1	0	0	1
1	1	0	1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	1	1	0	1



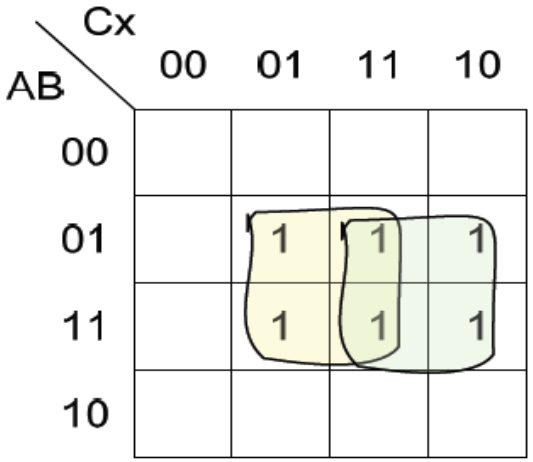
Q2:-Design the sequential circuit specified by the state diagram of Fig



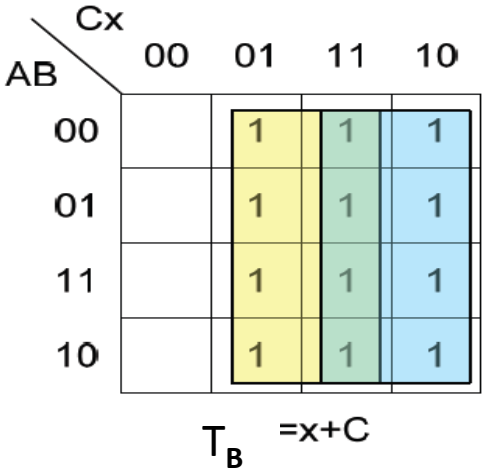
Q2:- Answer

Present State			Input	Next State			Flip-flop Inputs		
A	B	C	x	A	B	C	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	1
0	0	1	1	0	1	1	0	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	1	0	0	1	1	0
0	1	1	0	1	0	0	1	1	1
0	1	1	1	1	0	1	1	1	0
1	0	0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1	0
1	0	1	0	1	1	0	0	1	1
1	0	1	1	1	1	1	0	1	0
1	1	0	0	1	1	1	0	0	1
1	1	0	1	0	0	0	1	1	0
1	1	1	0	0	0	0	1	1	1
1	1	1	1	0	0	1	1	1	0

Q2:- Answer



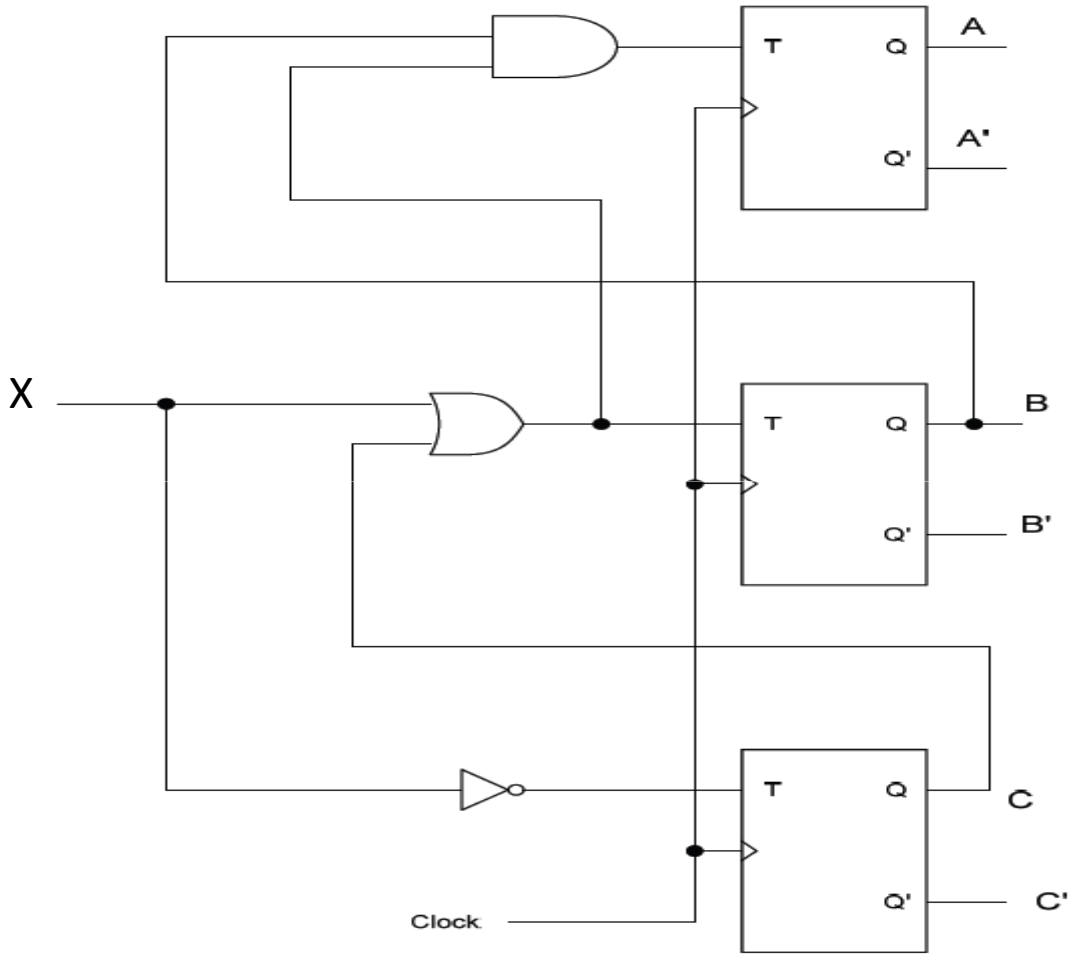
$T_A = Bx + BC = B(x + C)$



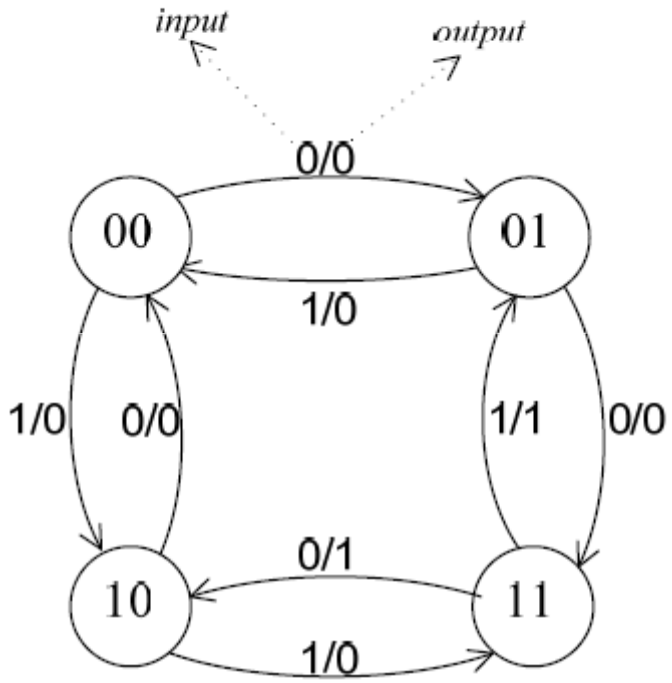
$T_B = x + C$

$T_C = x'$

Q2:- Answer

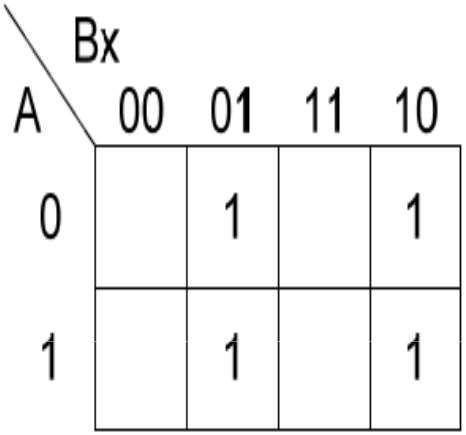


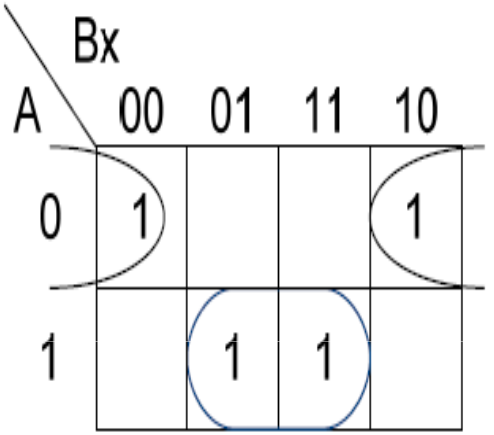
Q3:-Given the state diagram below, generate the state table and design a sequential circuit using D flip fops.



Q3:- Answer

PS		In	NS		Out
A	B	x	A	B	y
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	1	0





Flip – Flop inputs

$D_A = B'x + Bx' = B \oplus x$

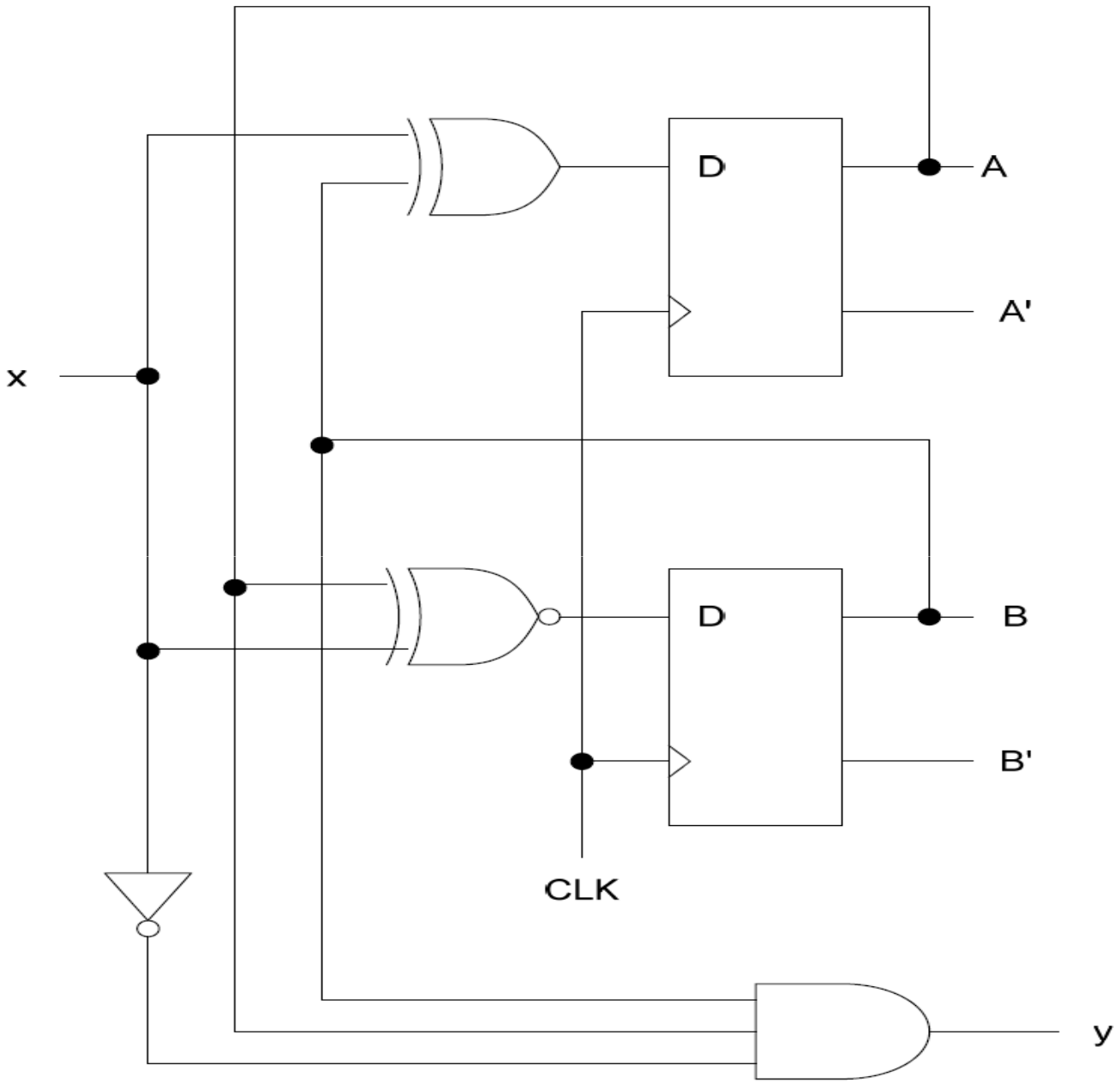
$D_B = Ax + A'x' = (A \oplus x)'$

$D_A = A(t+1)$

$D_B = B(t+1)$

$Y = ABx'$

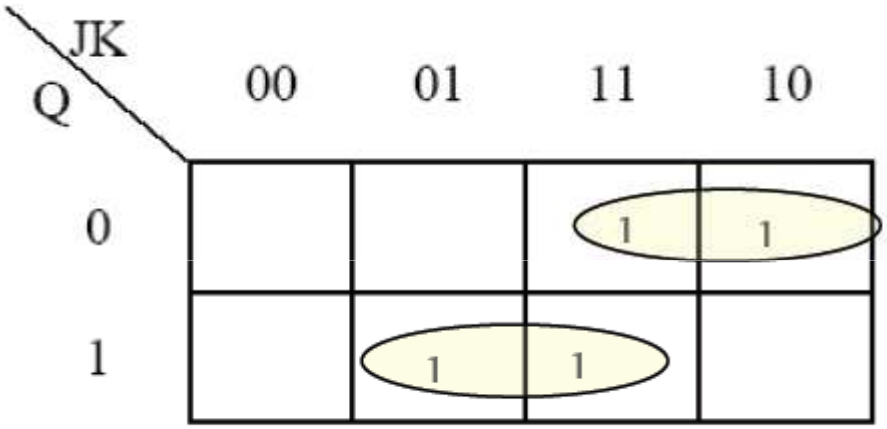
Q3:- Answer



Q4:-Convert a T flip-flop to a JK flip-flop by including input gates to the T flip flop. The gates needed for the input of the T flip flop can be determined by means of sequential circuit design procedures. The sequential circuit to be considered will have one T flip flop and two inputs, J and K.

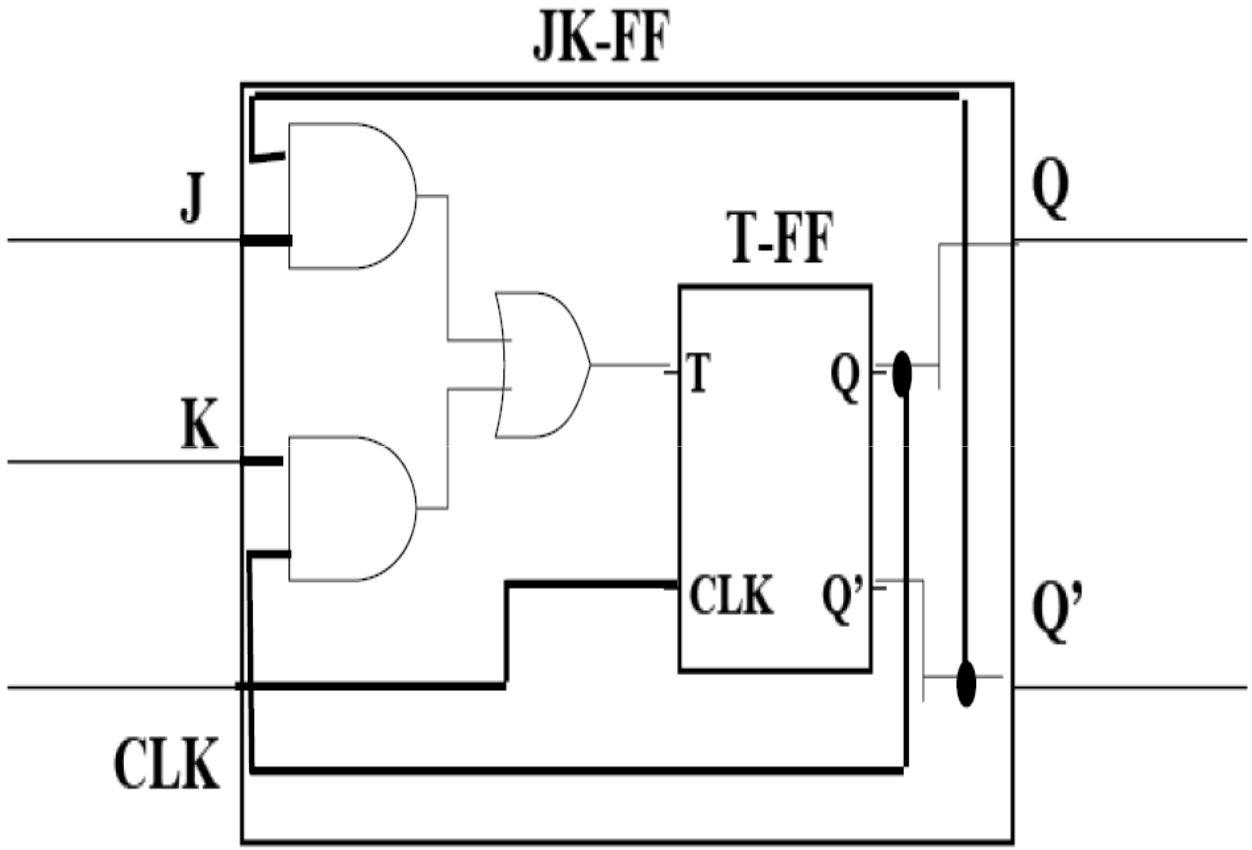
Present State	Inputs		Next State	Flip Flop Input
Q	J	K	Q	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

Q4:- Answer



T=Q'J+QK

Q4:- Answer

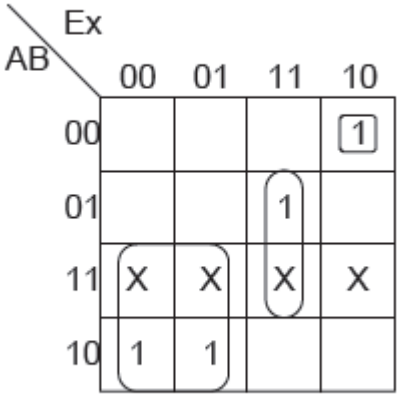


Q5:-Design a sequential circuit with two D flip flops, and two inputs, E and x. If E =0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 10 to 01 back to 00, and repeats. The circuit is to be designed by treating the unused state(s) as don't care condition(s). The final circuit must be analyzed to ensure that it is **self-correcting.**

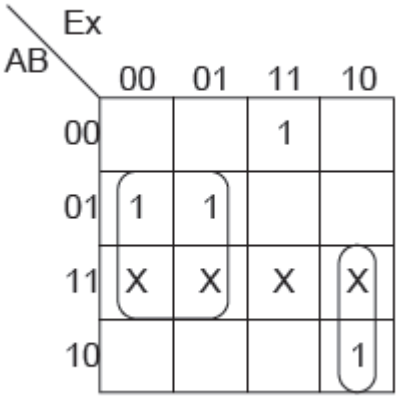
Q5:- Answer

Present State		Inputs		Next State		Flip Flop Inputs	
A	**B**	**E**	**x**	**A**	**B**	D_A	D_B
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	0
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	1	0	1
1	0	1	1	0	0	0	0
1	1	0	0			X	X
1	1	0	1			X	X
1	1	1	0			X	X
1	1	1	1			X	X

Q5:- Answer



$$D_A = AE' + BEx + A'B'Ex'$$



$$D_B = BE' + AEx' + A'B'Ex$$

Q5:- Answer

$D_A = AE' + BEx + A'B'Ex'$

$D_B = BE' + AEx' + A'B'Ex$

Present State		Inputs		Next State		Flip Flop Inputs	
A	B	E	x	A	B	D_A	D_B
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	1
1	1	1	1	0	0	1	0

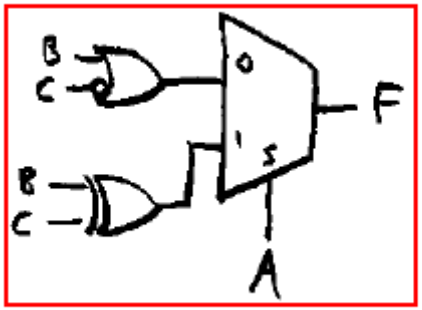
Q6:- For the following truth table, solve the following problems:
a.) By inspection of the truth table, use a 2:1 mux, with A as the select signal, to implement the logic function.
b.) Derive an algebraic equation for F then use a 2:1 mux, with B as the select signal, to implement the function. That is, use the algebraic method to derive the needed input logic.

Q6 a:- Answer

A	B	C	L
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

A = 0 $\quad F = B + C'$

A = 1 $\quad F = B \oplus C$



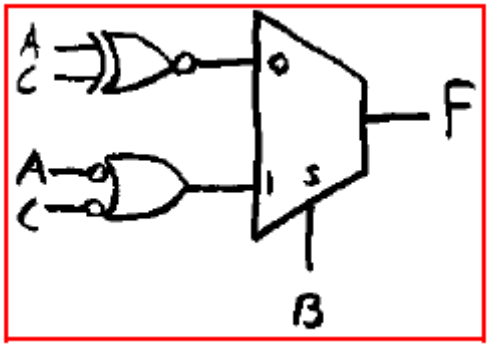
Q6b :- Answer

a \ bc	00	01	11	10
0	1		1	1
1		1		1

$F = A'B + A'C' + BC' + AB'C$

$F_{B=0} = A'(0) + A'C' + (0)C' + A(1)C = A'C' + AC = A \equiv C$

$F_{B=1} = A'(1) + A'C' + (1)C' + A(0)C = A' + A'C' + C' = A' + C'$



Q7:- Using a 3:8 decoder, implement the following logic function: F(A,B,C) = A + BC’ + A’B

Q7:- Answer

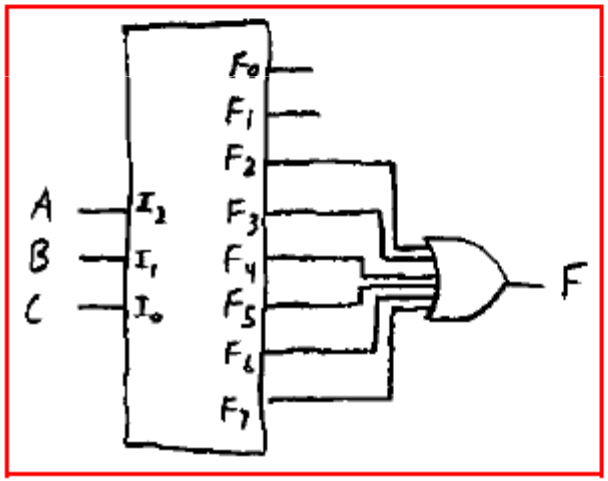
In order to use a decoder, we need to find the minterm expansion. This can be done by expanding the terms of the equation given.

$$F = \overbrace{AB'C' + AB'C + ABC' + ABC}^{A} + \overbrace{A'BC' + ABC'}^{BC'} + \overbrace{A'BC' + A'BC}^{A'B}$$

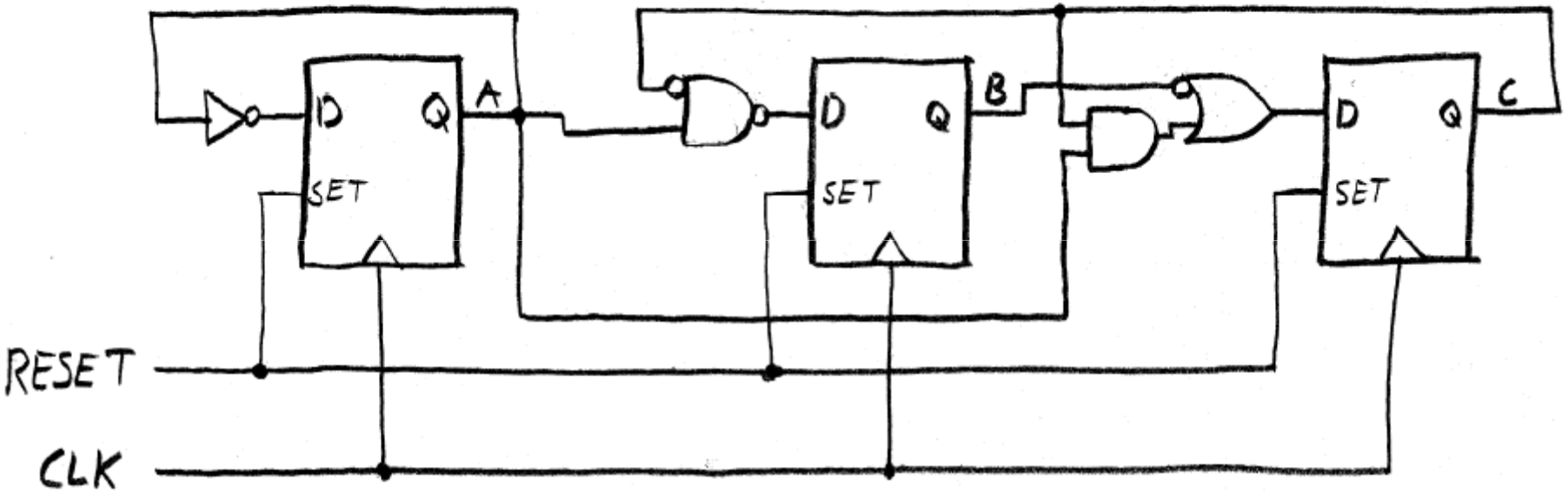
$$= m4 + m5 + m6 + m7 + m2 + m6 + m2 + m3$$

$$= m2 + m3 + m4 + m5 + m6 + m7$$

$$= \Sigma m(2, 3, 4, 5, 6, 7)$$



Q8:- Assuming the asynchronous **RESET signal is asserted briefly before the clock begins to** oscillate, what is the count sequence output on **A B C for the circuit shown below. Note that** the **RESET signal is connected to asynchronous SET inputs on these flip flops.**



Q8:- Answer

From the schematic, we can derive the following next state equations.

$N_A = A'$ $N_B = (AC')' = A' + C$ $N_c = AC + B'$

Since the reset is connected to "SET" inputs, the reset causes the sequence to start at "111". Based on these equations, we can fill out the next state table:

A	B	C	N_A	N_B	N_C
0	0	0	1	1	1
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	1	1

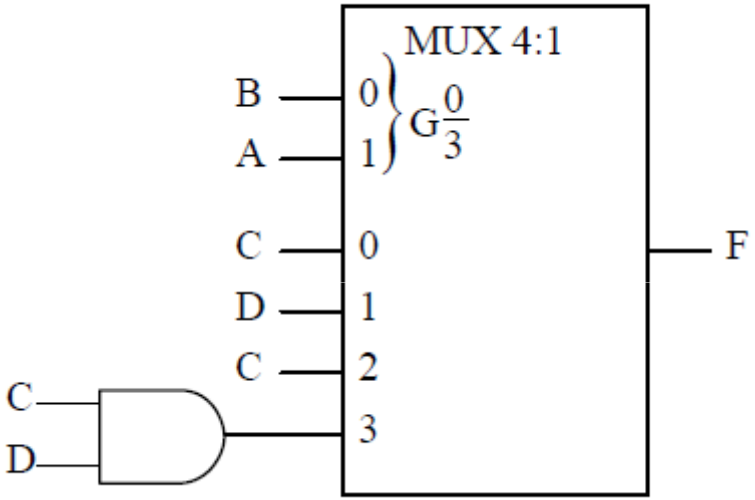
111, 011, 110, 000, 111, …

Q9:- Multiplexers as Data Selectors. Implement the following function using 4:1 Mux

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Q9:- Answer

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	0	C
0	0	1	0	1	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	1	D
0	1	1	0	0	
0	1	1	1	1	
1	0	0	0	0	
1	0	0	1	0	C
1	0	1	0	1	
1	0	1	1	1	
1	1	0	0	0	
1	1	0	1	0	CD
1	1	1	0	0	
1	1	1	1	1	



Q10:- Implement the above truth table using 2:1 mux

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	0	
0	0	1	0	1	$\overline{B}C + BD$
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	1	1	
1	0	0	0	0	
1	0	0	1	0	
1	0	1	0	1	$\overline{B}C + CD$
1	0	1	1	1	
1	1	0	0	0	
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	1