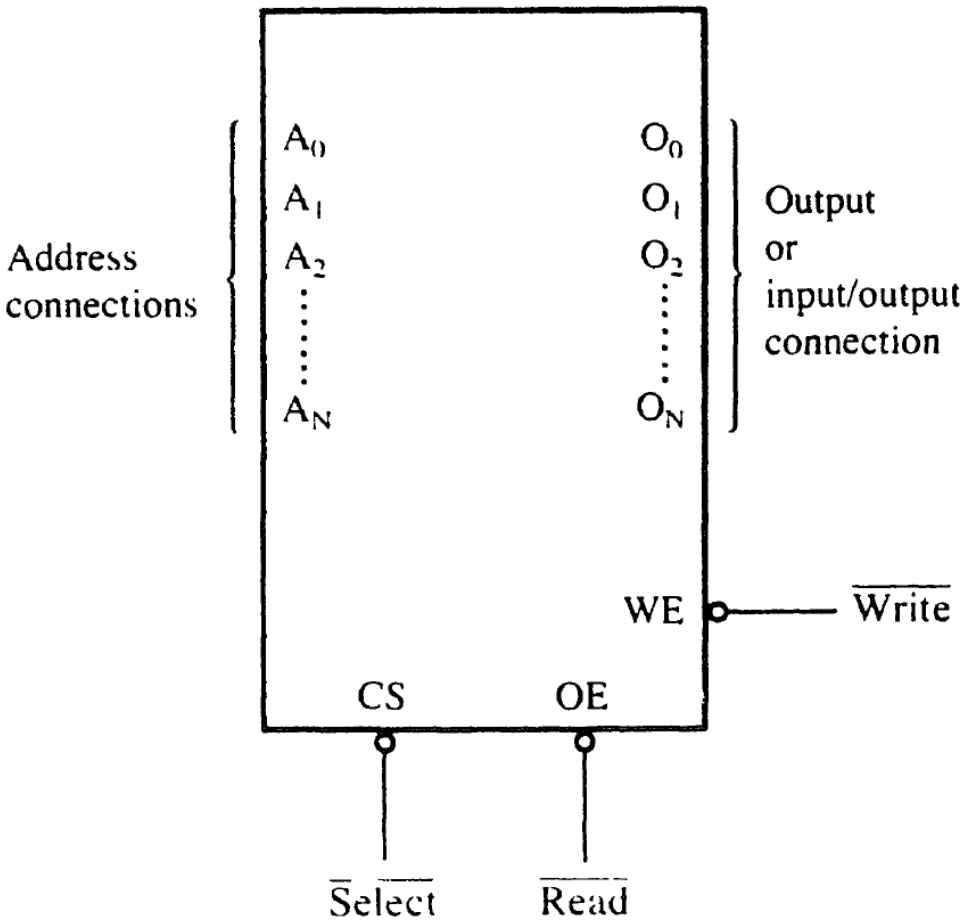
Memory Interfacing /8086

MEMORY DEVICES

- Before attempting to interface memory to the microprocessor, it is essential to understand the operation of memory components.
- In this section, we explain functions of the four common types of memory:
  - read-only memory (ROM)
  - Flash memory (EEPROM)
  - Static random access memory (SRAM)
  - dynamic random access memory (DRAM)

Memory Pin Connections



- address inputs
- data outputs or input/outputs
- some type of selection input
- at least one control input to select a read or write operation

Figure A pseudo memory component illustrating the address, data, and control connections.

Data Connections

- All memory devices have a set of data outputs or input/outputs.
  - today, many devices have bidirectional common I/O pins
  - data connections are points at which data are entered for storage or extracted for reading
- Data pins on memory devices are labeled D_0 through D_7 for an 8-bit-wide memory device.

- An 8-bit-wide memory device is often called a **byte-wide** memory.
  - most devices are currently 8 bits wide,
  - some are 16 bits, 4 bits, or just 1 bit wide
- Catalog listings of memory devices often refer to memory locations times bits per location.
  - a memory device with 1K memory locations and 8 bits in each location is often listed as a 1K $\times$ 8 by the manufacturer
- Memory devices are often classified according to total bit capacity.

Selection Connections

- Each memory device has an input that selects or enables the memory device.
  - sometimes more than one
- This type of input is most often called a **chip select** ($\overline{G2A}$) **chip enable** ($\overline{CE}$) or simply **select** ($\overline{S}$) input.
- RAM memory generally has at least one $\overline{}$ or $\overline{}$ input, and ROM has at least one $\overline{}$
- If more than one $\overline{CE}$ connection is present, all must be activated to read or write data.

Control Connections

- ROM usually has one control input,
- Control input often found on ROM is the **output enable** or **gate** connection, which allows data flow from output data pins.
- The $\overline{OE}$ connection enables and disables a set of three-state buffers located in the device and must be active to read data.

- RAM has either one or two control inputs.
  - if one control input, it is often called R/$\overline{W}$
- If the RAM has two control inputs, they are usually labeled $\overline{WE}$ (or $\overline{W}$), and $\overline{OE}$ (or $\overline{G}$).
  - **write enable** must be active to perform memory write, and $\overline{OE}$ active to perform a memory read
  - when the two controls are present, they must never both be active at the same time
- If both inputs are inactive, data are neither written nor read.
  - the connections are at their high-impedance state

ROM Memory

- **Read-only memory** (ROM) permanently stores programs/data resident to the system.
  - and must not change when power disconnected
- Often called **nonvolatile memory**, because its contents *do not* change even if power is disconnected.
- A device we call a ROM is purchased in mass quantities from a manufacturer.
  - programmed during fabrication at the factory

- The EPROM (**erasable programmable read-only memory**) is commonly used when software must be changed often.
  - or when low demand makes ROM uneconomical
- An EPROM is programmed in the field on a device called an EPROM programmer.
- Also erasable if exposed to high-intensity ultraviolet light.
  - depending on the type of EPROM

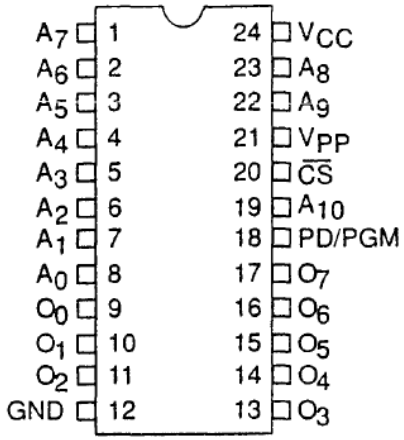
- PROM memory devices are also available, although they are not as common today.
- The PROM (**programmable read-only memory**) is also programmed in the field by burning open tiny NI-chrome or silicon oxide fuses.
- Once it is programmed, it cannot be erased.

- A newer type of **read-mostly memory** (RMM) is called the **flash memory**.
  - also often called an EEPROM (**electrically erasable programmable ROM**)
  - EAROM (**electrically alterable ROM**)
  - or a NOVRAM (**nonvolatile RAM**)
- Electrically erasable in the system, but they require more time to erase than normal RAM.
- The flash memory device is used to store setup information for systems such as the video card in the computer.

- Flash has all but replaced the EPROM in most computer systems for the BIOS.
  - some systems contain a password stored in the flash memory device
- Flash memory has its biggest impact in memory cards for digital cameras and memory in MP3 audio players.
- 2716 EPROM, is representative of most common EPROMs.

Figure The pin-out of the 2716, 2K × 8 EPROM.

PIN CONFIGURATION



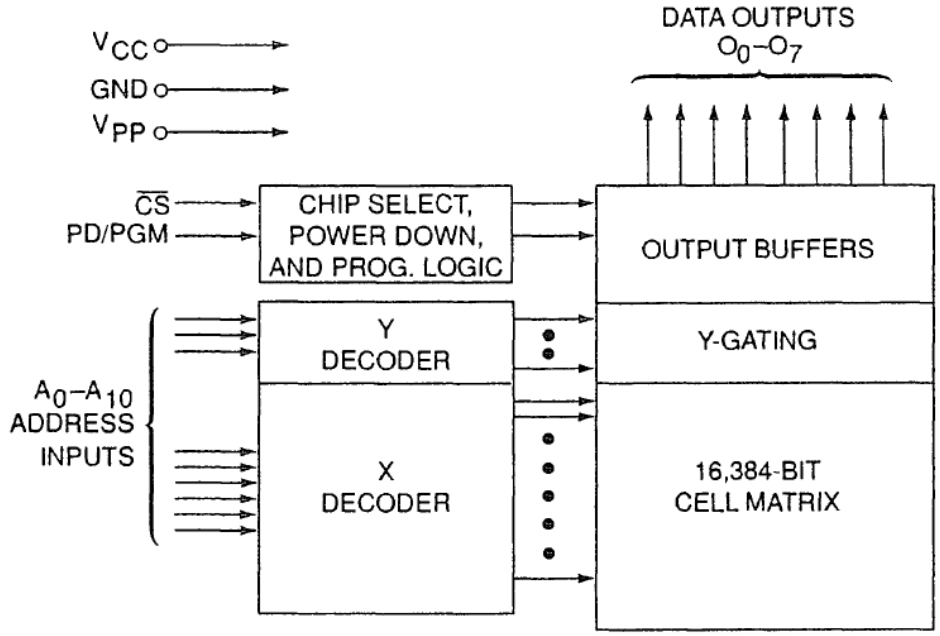
MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

BLOCK DIAGRAM



- In some cases, the V_{PP} pin is in the same position as the $\overline{WE}$ pin on the SRAM.
- This will allow a single socket to hold either an EPROM or an SRAM.
  - an example is the 27256 EPROM and 62256 SRAM, both $32K \times 8$ devices with the same pin-out, except for V_{PP} on the EPROM and $\overline{WE}$ on the SRAM.

Figure A.C. Characteristics of 2716 EPROM .

A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

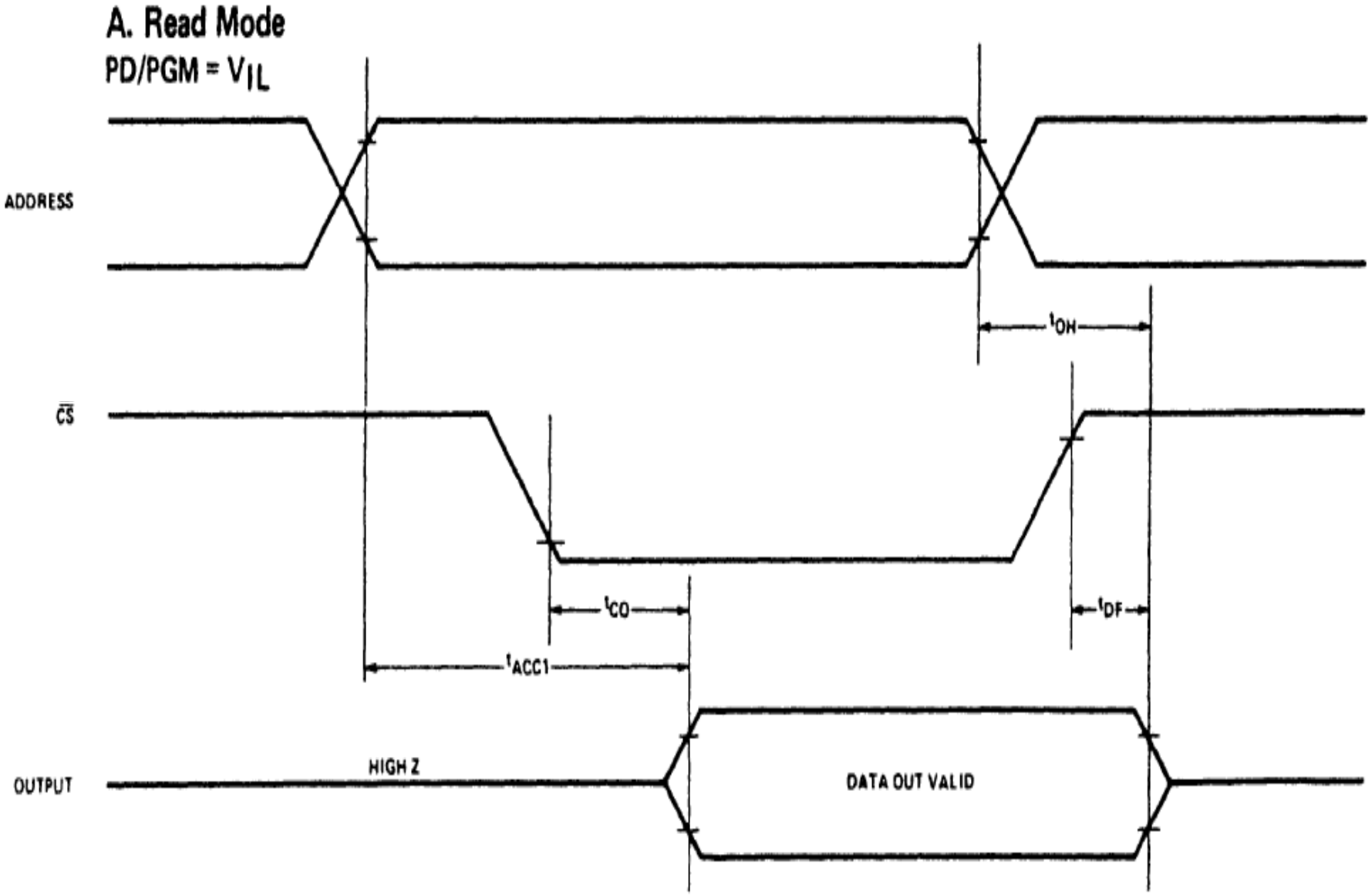
Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V

Figure The timing diagram of AC characteristics of the 2716 EPROM.



- The basic speed of this EPROM is 450 ns.
  - recall that 8086/8088 operated with a 5 MHz clock allowed memory 460 ns to access data
- This type of component requires wait states to operate properly with 8086/8088 because of its rather long access time.
  - if wait states are not desired, higher-speed EPROMs are available at additional cost
  - EPROM memory is available with access times of as little as 100 ns
- Obviously, wait states are required in modern microprocessors for any EPROM device.

ADDRESS DECODING

- In order to attach a memory device to the microprocessor, it is necessary to decode
  the address sent from the microprocessor.
- Decoding makes the memory function at a unique section or partition of the memory map.
- Without an address decoder, only one
  memory device can be connected to a microprocessor, which would make it virtually useless.

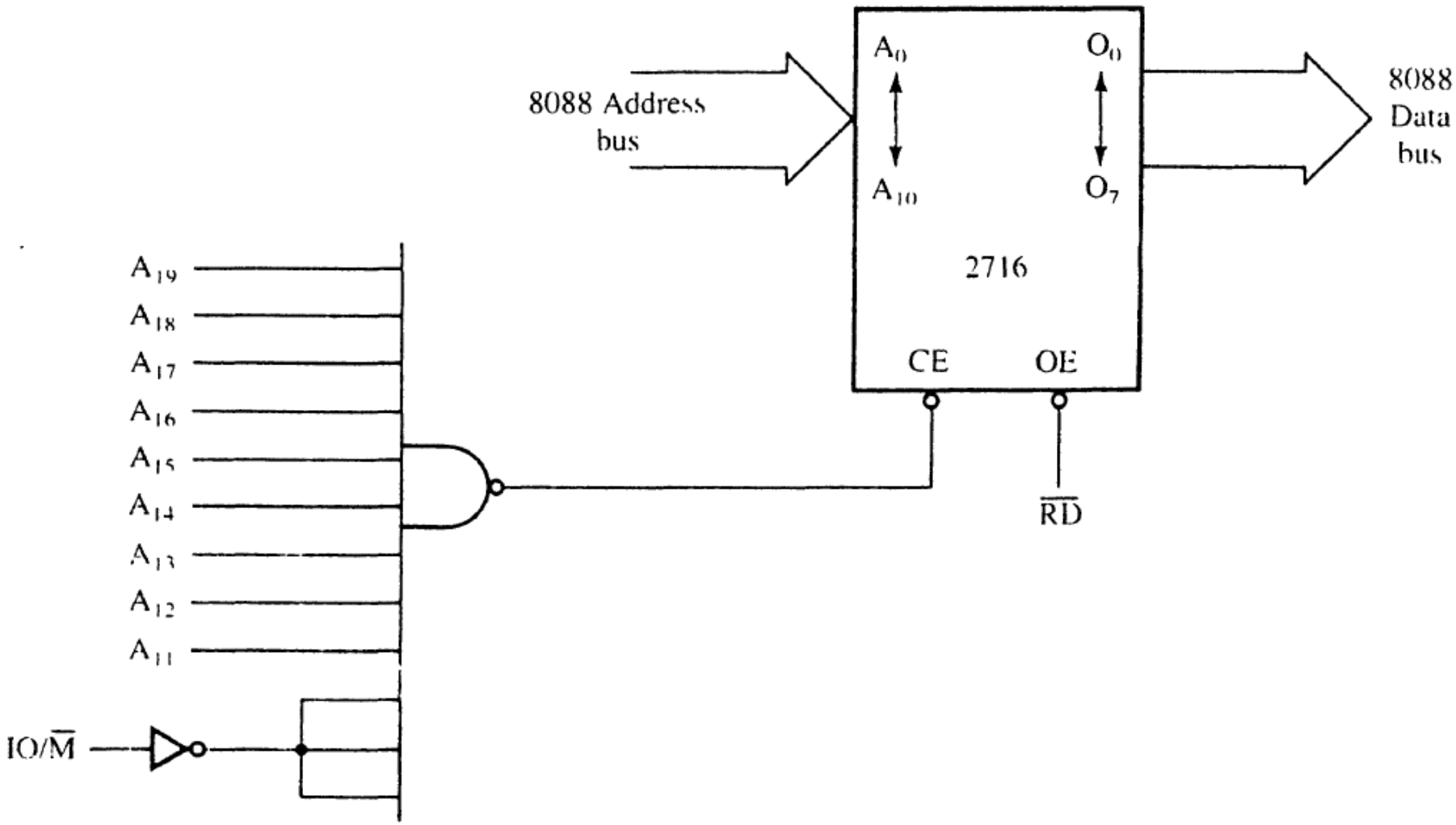
Why Decode Memory?

- The 8086 has 20 address connections and the 2716 EPROM has 11 connections.
- The 8086 sends out a 20-bit memory address whenever it reads or writes data.
  - because the 2716 has only 11 address pins, there is a mismatch that must be corrected
- The decoder corrects the mismatch by decoding address pins that do not connect to the memory component.

Simple NAND Gate Decoder

- When the 2K $\times$ 8 EPROM is used, address connections A_{10}–A_0 of 8086 are connected to address inputs A_{10}–A_0 of the EPROM.
  - the remaining nine address pins (A_{19}–A_{11}) are connected to a NAND gate decoder

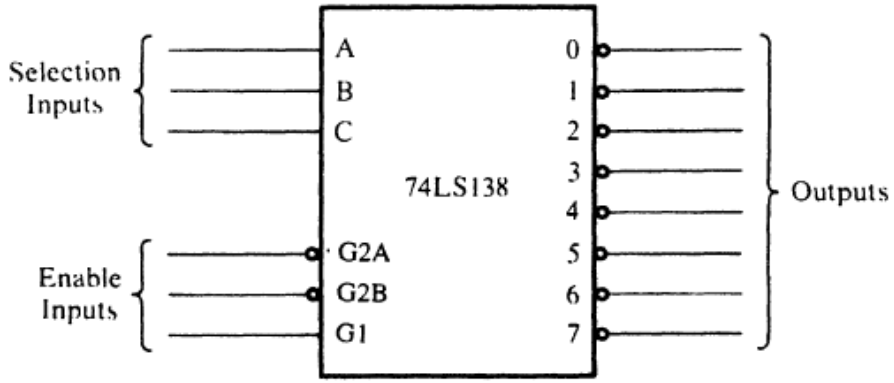
Figure A simple NAND gate decoder that selects a 2716 EPROM for memory location FF800H–FFFFFH.



- If the 20-bit binary address, decoded by the NAND gate, is written so that the leftmost nine bits are 1s and the rightmost 11 bits are don't cares (X), the actual address range of the EPROM can be determined.
  - a *don't care* is a logic 1 or a logic 0, whichever is appropriate

- Because of the excessive cost of the NAND gate decoder and inverters often required, this option requires an alternate be found.

The 3-to-8 Line Decoder (74LS138)



Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

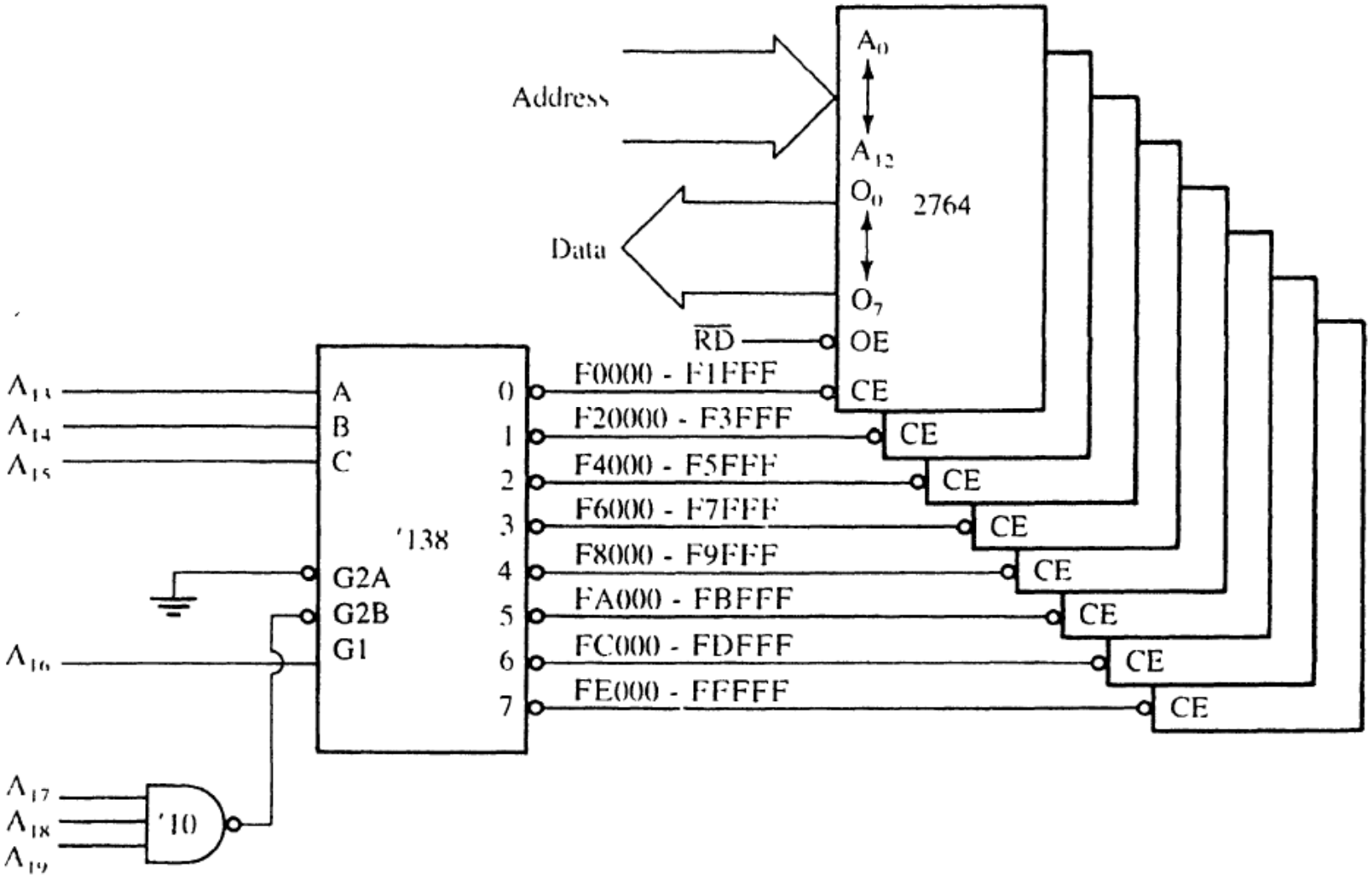
- a common integrated circuit decoder found in many systems is the 74LS138 3-to-8 line decoder.

Figure The 74LS138 3-to-8 line decoder and function table.

Sample Decoder Circuit

- The outputs of the decoder can be connected to eight different 2764 EPROM memory devices.
- The decoder selects eight 8K-byte blocks of memory for a total capacity of 64K bytes.
- This figure also illustrates the address range of each memory device and the common connections to the memory devices.

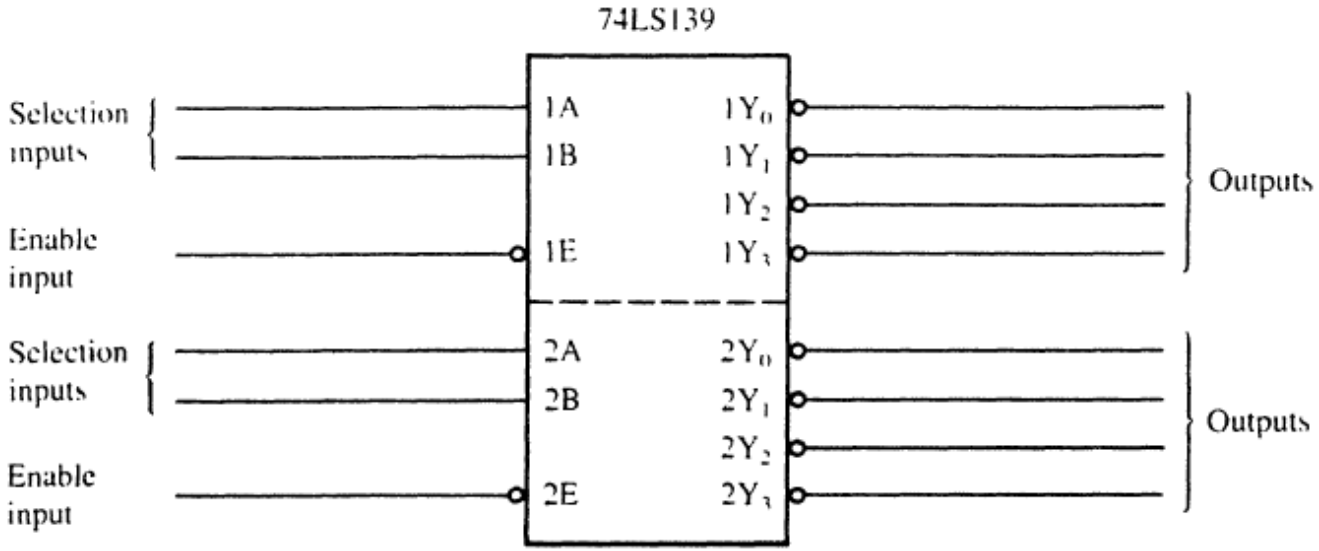
Figure A circuit that uses eight 2764 EPROMs for a 64K × 8 section of memory in an 8086 microprocessor-based system. The addresses selected in this circuit are F0000H–FFFFFH.



The Dual 2-to-4 Line Decoder (74LS139)

- Figure 10–16 illustrates both the pin-out and the truth table for the 74LS139 dual 2-to-4 line decoder.
- 74LS139 contains two separate 2-to-4 line decoders—each with its own address, enable, and output connections.

Figure 10–16 The pin-out and truth table of the 74LS139, dual 2-to-4 line decoder.



Inputs			Outputs			
$\overline{E}$	A	B	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1