Digital Electronics and Microprocessors

Class 21

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Microprocessor

- A **microprocessor** incorporates the functions of a computer's central processing unit (CPU) on a single integrated circuit (IC), or at most a few integrated circuits. It is a multipurpose, programmable device that accepts digital data as input, processes it according to instructions stored in its memory, and provides results as output. It is an example of sequential digital logic, as it has internal memory. Microprocessors operate on numbers and symbols represented in the binary numeral system.

Microprocessor

- General-purpose microprocessors in personal computers are used for computation, text editing, multimedia display, and communication over the Internet.
- Many more microprocessors are part of embedded systems, providing digital control of a myriad of objects from appliances to automobiles to cellular phones and industrial process control.

4-bit designs

- First commercial 4 bit processor from intel “Intel 4004”

8-bit designs

- Intel’s 8085
- Zilogs Z80
- Motorola 68000(68K)

16-bit designs

- 16-bit Intel 8086, the first member of the x86 family, which powers most modern PC type computers.

32-bit designs

- Intels
- ARM
- The MIPS R2000 (1984) and R3000 (1989) were highly successful 32-bit RISC microprocessors

Classification of instruction set Architecture

- RISC
- CISC

CISC (features)

- Richer instruction set, some simple, some very complex
- Instruction generally take more than one clock cycle to execute
- Instruction of variable size
- Instructions interface with memory in mechanisms with complex addressing modes
- Microcode control
- Work well with simpler compiler

RICS (features)

- Fixed length simple instructions
- Few data types
- Simple addressing modes
- Large register sets
- Overhead goes to the compiler designer.

Processor design issues

- Number of addresses
  - Three address machines

    Ex :-Add dest,src1,src2
  - Two address machines

    Ex Add dest, src
  - One address machines (accumulator machine instructions)

    Ex:-Add addr
  - Zero address machines(stack machine instructions)

    Ex:- add
- The load store architecture

  only load and store instructions move data between registers and memory
- Processor registers

Instruction set design issues

- Operand types (integers, FP, character)
- Addressing modes

  refers to how operands are specified(operands can be in registers, memory or part of the instruction as a constant)
- Instruction types

  data movement instructions

  arithmetic and logic instruction
- Instruction formats

Features of Instruction Set

- Should be complete

One should be able to construct a machine level program to evaluate any function

- Should be efficient

Frequently required functions can be completed quickly using relatively few instructions

- Should be regular

Should contain expected op codes and addressing modes
Compatible with existing machines

Intel 8086 Microprocessor

Key Features:

- **Released by Intel in 1978**
- **Produced from 1978 to 1990s**
- **A 16-bit microprocessor chip.**
- **Max. CPU clock rate :**
  5 MHz to 10 MHz
- **Instruction set: x86-16**
- **Package: 40 pin DIP**
- **The 8086 gave rise to**
  the x86 architecture of Intel's future processors.
- **Common manufacturer(s): Intel, AMD, NEC, Fujitsu, Harris (Intersil), OKI, Siemens AG, Texas Instruments, Mitsubishi.**

Fig1:Intel 8086 Microprocessor

The Intel 8088, released in 1979, was a slightly modified chip with an external 8-bit data bus and is notable as the processor used in the original IBM PC.

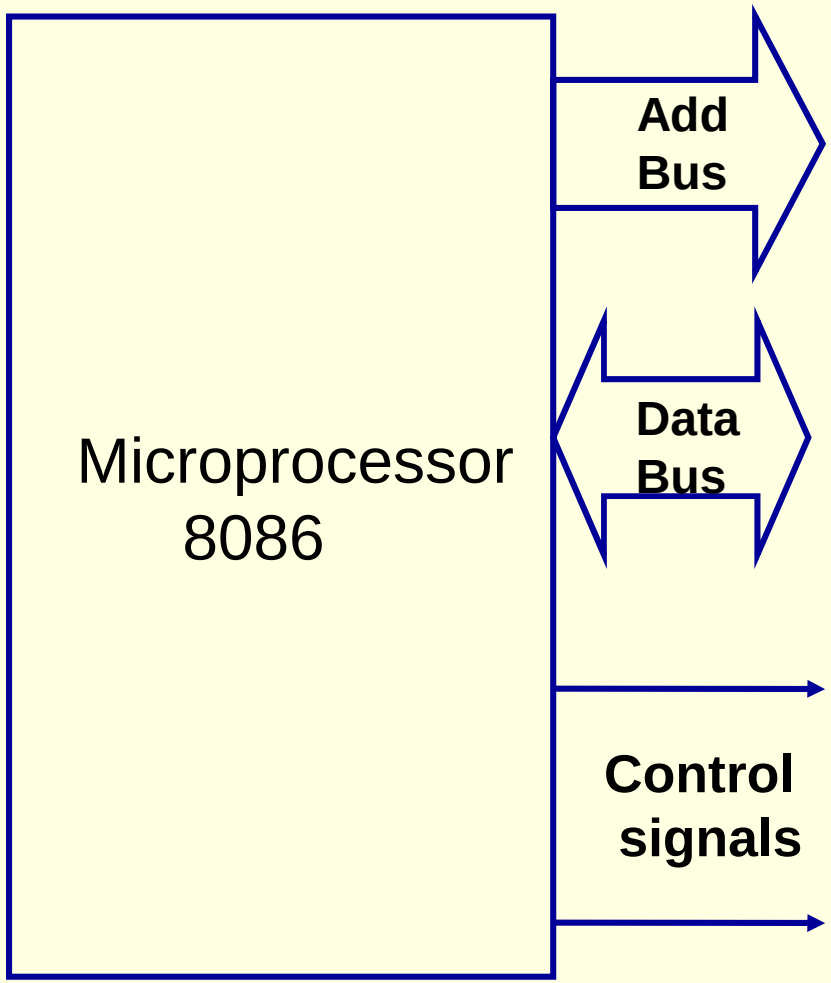
Current x86 processors
http://en.wikipedia.org/wiki/8086

- *x86-32:* EP80579 · Intel CE · Atom
- *x86-64:* Atom (some) · Celeron · Pentium (Dual-Core) · Core (i3 · i5 · i7) · Xeon
- *Other:* IOP · Itanium
- x86 Assemblers: A86/A386 · FASM · GAS · HLA · MASM · NASM · TASM · WASM · YASM

8086 microprocessor

Address Bus – 20 lines – A_{19} – A_0

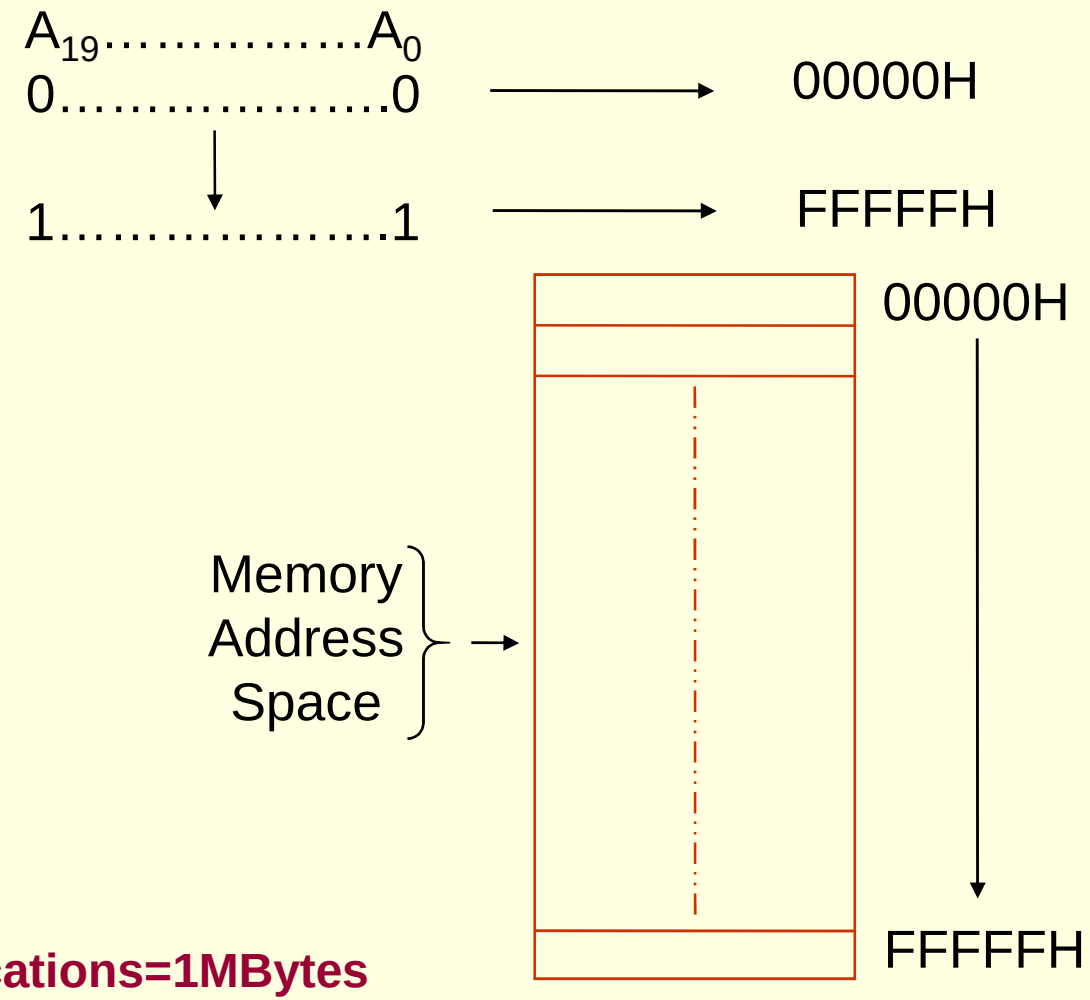
Data Bus – 16 lines – D_{15} – D_0



- 16 bit- microprocessor ?
- 16-bits data bus?

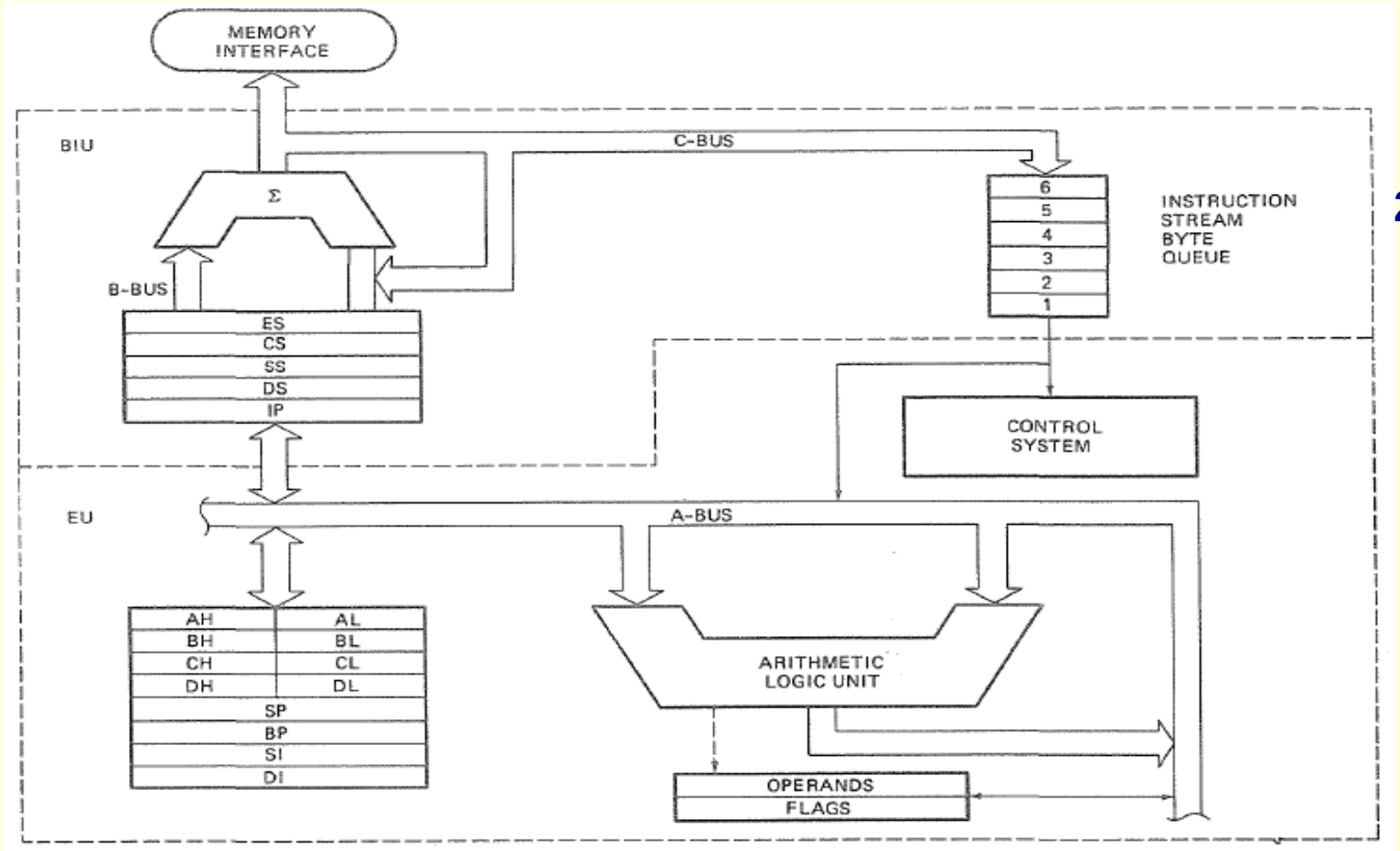
20 bits address bus?

- **It can address any one of 1,048,576 (=2^{20}) memory locations/addresses.**
- **Each memory location is one byte wide.**
- **To store a word of 16 bit 2 memory locations are required.**
- **If the first byte of the word is at even address 8086 can read the entire word in one operation.**
- **If the first byte of the word is at an odd address, the 8086 will read the first byte with one bus operation and the second byte with another bus operation.**



1,048,576 memory locations=1MBytes

8086 INTERNAL ARCHITECTURE



2 units are:

1. **BIU**
2. **EU**

Fig: 8086 Internal block diagram .

BIU and EU

- **BIU (bus interface unit)** sends out addresses, fetches instructions from memory, reads data from ports and memory, and writes data to ports and memory. In other words, the BIU handles all transfers of data and addresses on the buses for the execution unit.
- **EU (execution unit)** of the 8086 tells the BIU where to fetch instructions or data from, decodes instructions, and executes instructions.

EU (execution unit)

Major components are

- Control circuitry
- Instruction decoder
- ALU
- Flag register
- General purpose registers

Control circuitry

- Control circuitry directs internal operation

Decoder

- Decoder in EU translates instructions fetched from memory into series of actions which the EU carries out

ALU

- The EU has a 16-bit ALU which can add, subtract. AND, OR, XOR, Increment, Decrement, complement, shift binary numbers.

Flag Register

A flag is a flip-flop which indicates some condition produced by the execution of an instruction or controls certain operations of the EU.

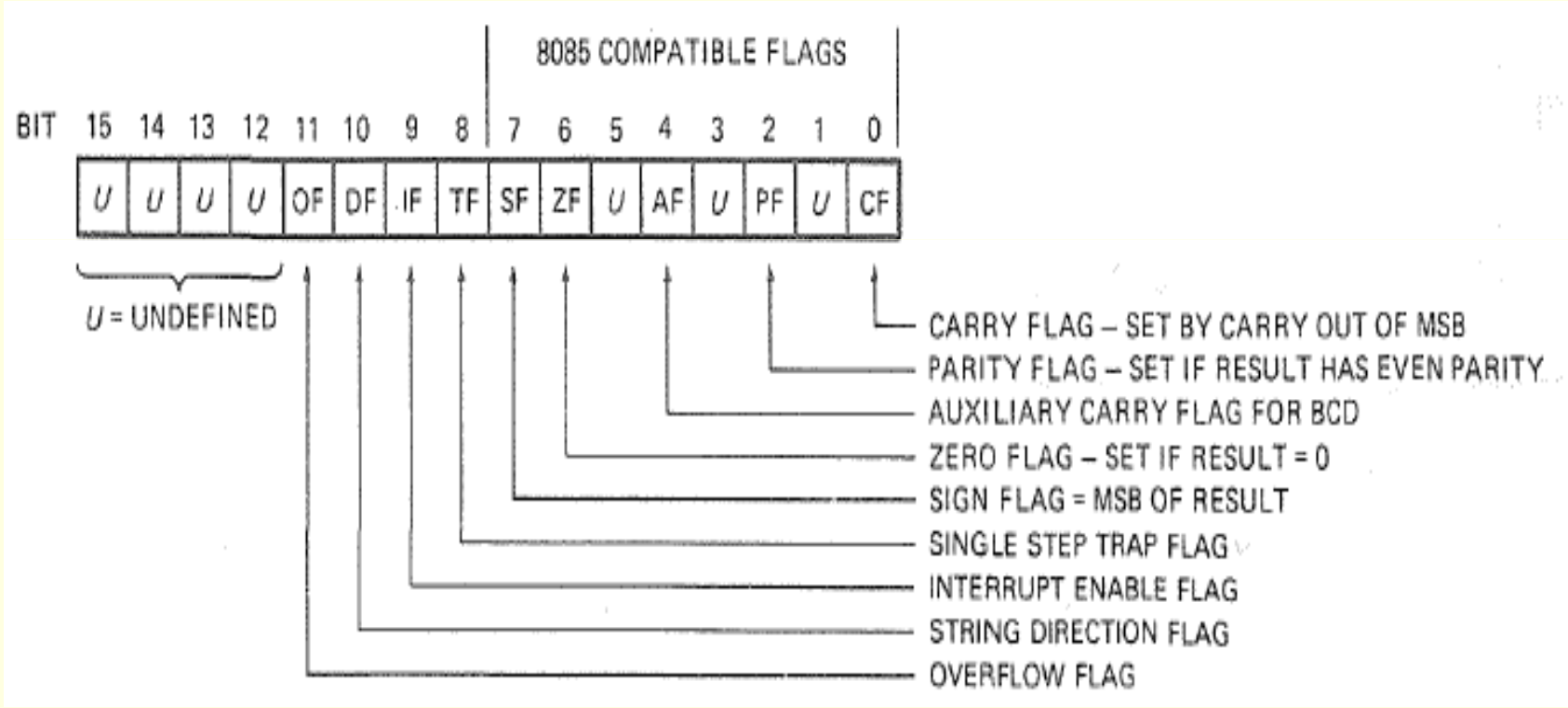


Fig: Flag register

Contd..

Flags:

- -Conditional Flags
- -Control Flags

Conditional Flags:

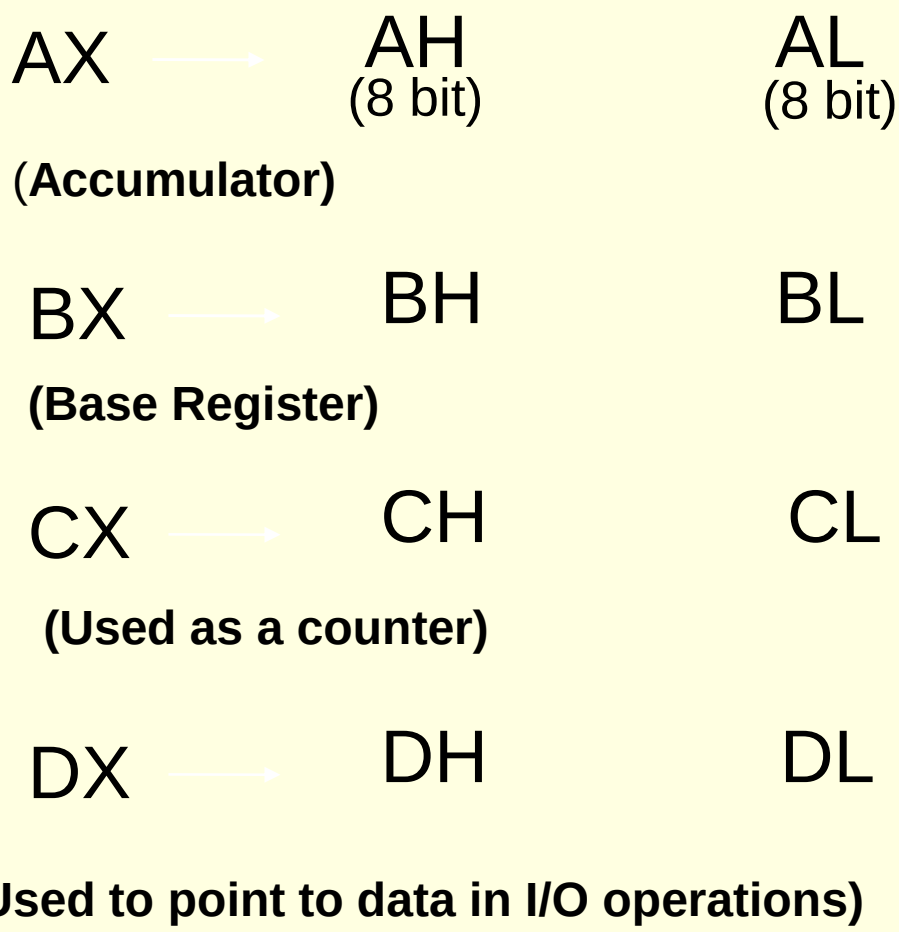
- C (Carry)
- P (Parity)
- A (Auxiliary Carry)
- Z (Zero)
- S (Sign)
- O (Overflow)

Control Flags:

- T (Trap)
- I (Interrupt)
- D (Direction)

General purpose registers

- 8 GP registers are there
- Each GP register is of 8 bits.
- To store 16 bit data pairs of registers can be used as shown here.
- Why GP registers are designed like this?
- GP registers are used for temporary data storage.



BIU (bus interface unit)

Major Components are

- Queue
- Segment registers and IP register

The Queue

- While the EU is decoding an instruction or executing an instruction which does not require use of the buses, the BIU fetches up to six instruction bytes for the following instructions. The BIU stores these prefetched bytes in a first-in—first-out register set called a queue.
- This prefetch-and-queue scheme greatly speeds up processing.
- Except in the cases of JMP and CALL instructions, where the queue must be dumped and then reloaded starting from a new address.
- Fetching the next instruction while the current instruction executes is called pipelining.

Segment registers and Instruction Pointer (IP)

- **1. Code Segment (CS) register, 2. Data Segment (DS) register, 3. Stack Segment (SS) register and 4. Extra Segment (ES) register.**
- IP register holds the 16-bit address, or offset, of the next code byte within code segment.
- Contents of IP decide which instruction will be executed next.

Memory organization

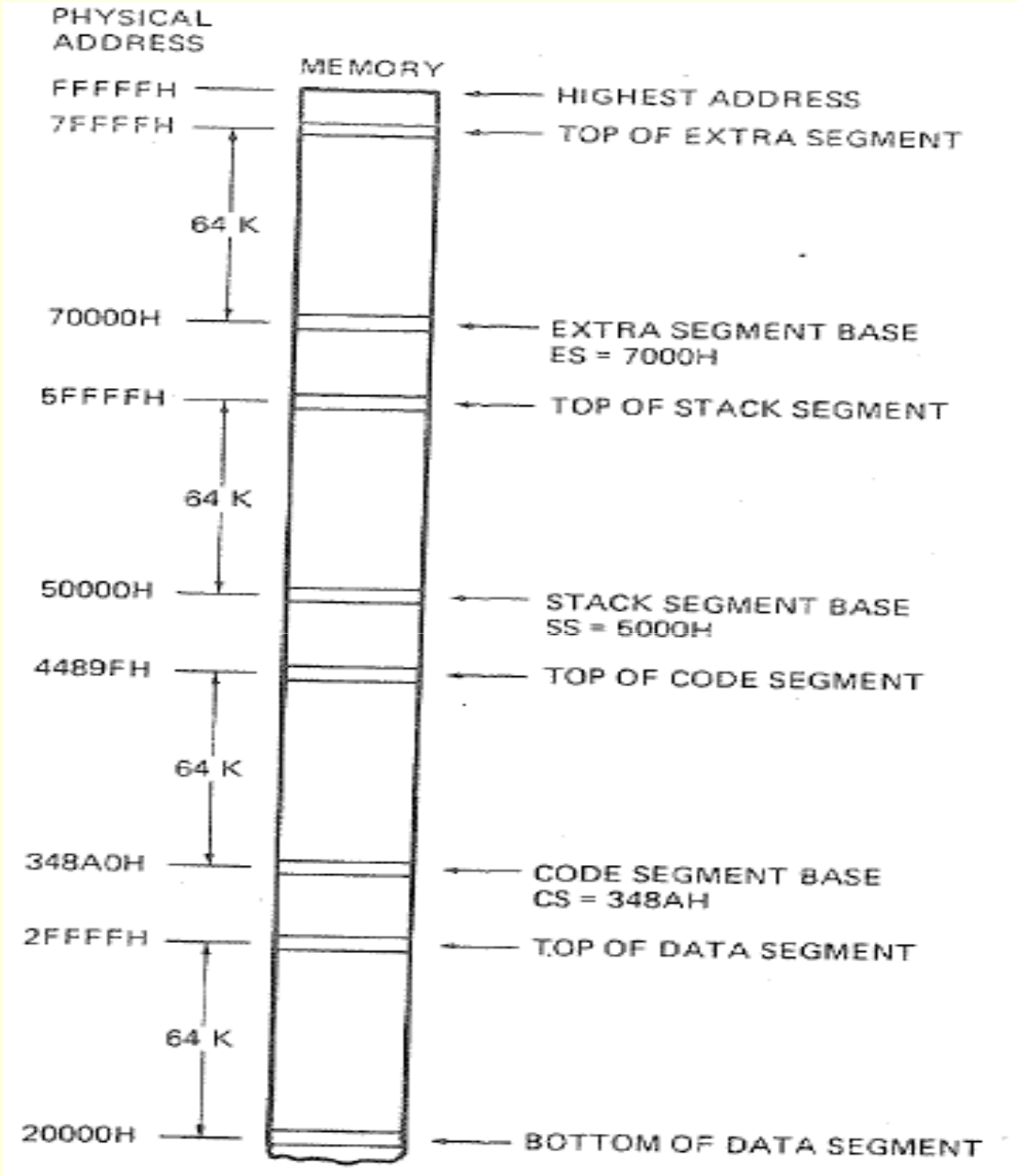
- At any given time the 8086 works with only four 65,536-byte (64-Kbyte) segments within the 1,048,576- byte (1-Mbyte) range.
- Four segment registers in the BIU are used to hold the upper 16 bits of the starting addresses of four memory segments that the 8086 is working with at a particular time.

8086 introduced memory segmentation to overcome the 16-bit addressing barrier of earlier chips.

Memory Segmentation

Fig:

One way four 64-Kbytes segments might be positioned within 1MByte address space of 8086.



This constraint was put on the location of segments so that it is only necessary to store and manipulate 16-bit numbers when working with the starting address of a segment.