Digital Electronics and Microprocessors

Class 4

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Alternate Logic-Gate Representations

- To convert a standard symbol to an alternate:
  - Invert each input and output (add an inversion bubble where there are none on the standard symbol, and remove bubbles where they exist on the standard symbol.
  - Change a standard OR gate to and AND gate, or an AND gate to an OR gate.

Alternate Logic-Gate Representations

- The equivalence can be applied to gates with any number of inputs.
- No standard symbols have bubbles on their inputs. All of the alternate symbols do.
- The standard and alternate symbols represent the same physical circuitry.

Alternate Logic-Gate Representations

- Active high – an input or output has no inversion bubble.
- Active low – an input or output has an inversion bubble.
- An AND gate will produce an active output when all inputs are in their active states.
- An OR gate will produce an active output when any input is in an active state.

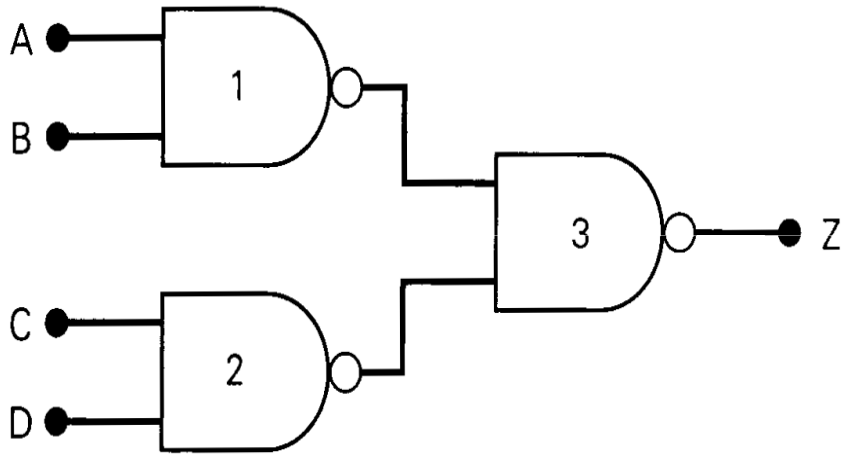
Which Gate Representation to Use

- Using alternate and standard logic gate symbols together can make circuit operation clearer.
- When possible choose gate symbols so that bubble outputs are connected to bubble input and nonbubble outputs are connected to nonbubble inputs.

Which Gate Representation to Use

- When a logic signal is in the active state (high or low) it is said to be asserted.
- When a logic signal is in the inactive state (high or low) it is said to be unasserted.
- A bar over a signal means asserted (active) low.
- The absence of a bar over a signal means asserted (active) high.

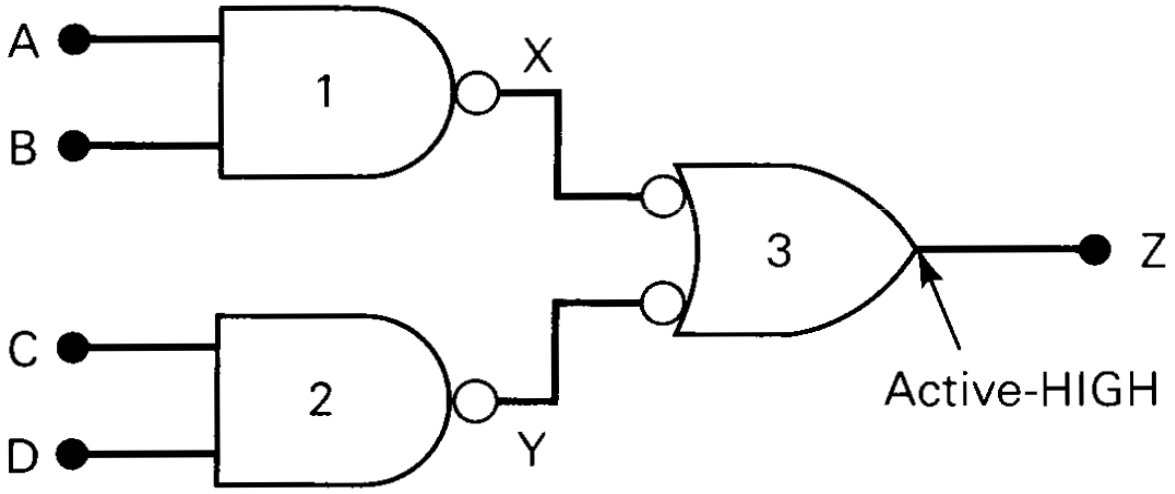
Example



A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

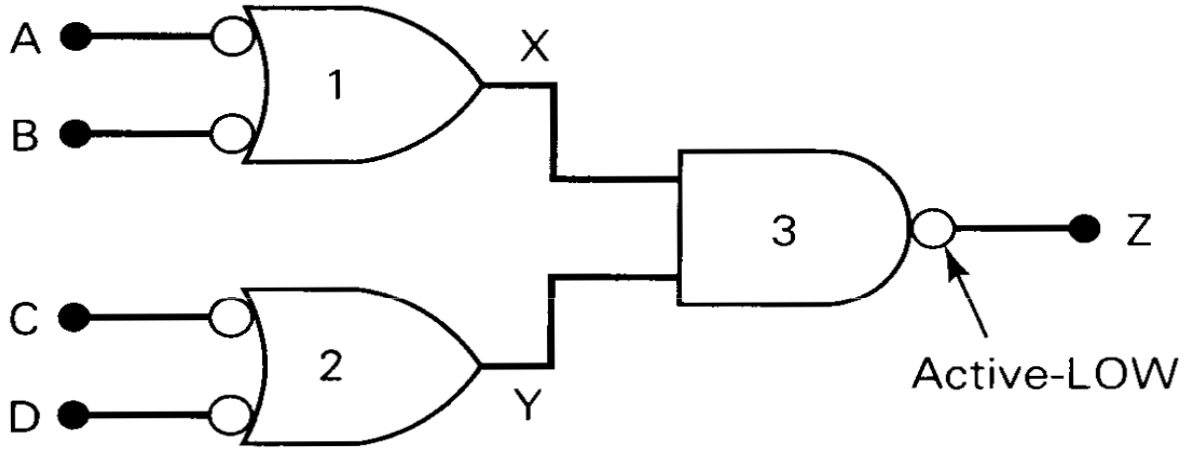
This circuit does not facilitate an understanding of how the circuit functions

Example continued



Output Z will go high whenever either A=B=1 or C=D=1 (Or both)

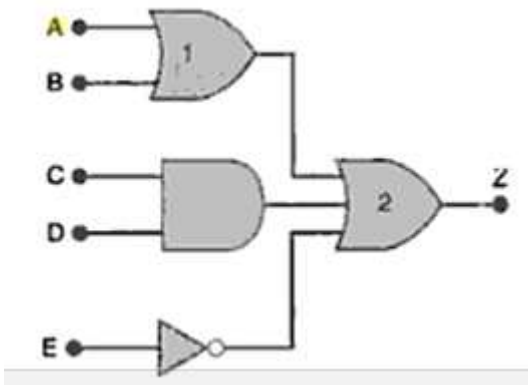
Example continued



Output Z will go low only when A or B is low and C or D is low

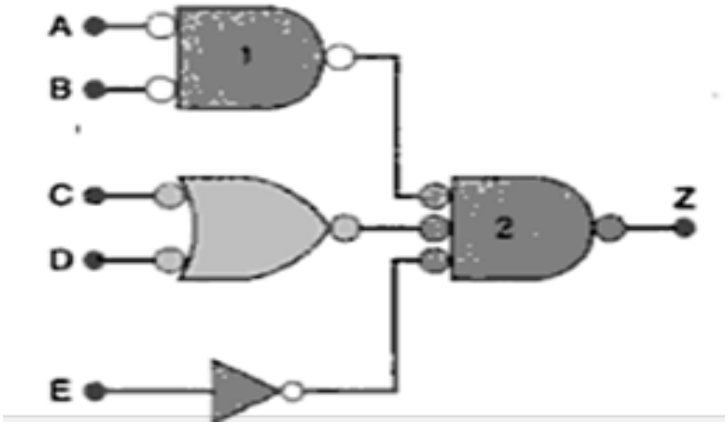
Example

- when the output of the logic ckt in fig goes low it activates another logic ckt. Modify the ckt diagram to represent the circuit operation more effectively



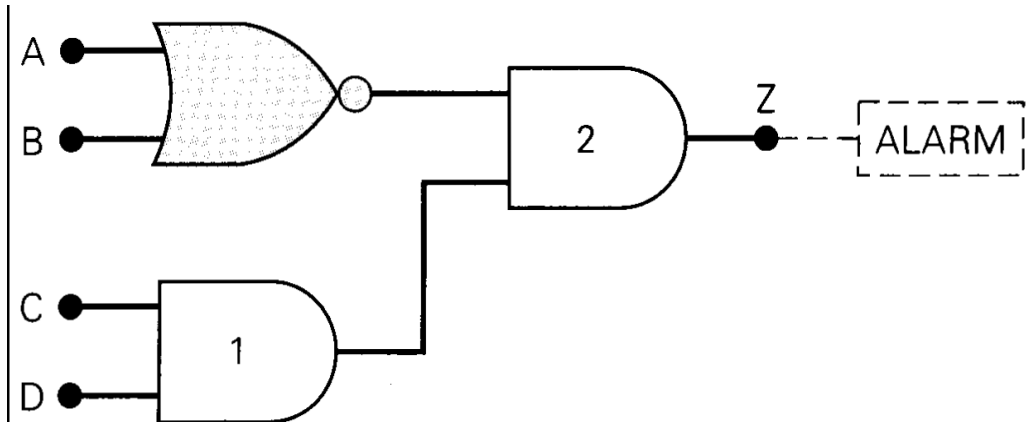
Alternate gate representation

- Because Z is to be active low, the symbol for OR gate 2 must be changed to its alternate symbol. The new OR gate2 symbol has bubble inputs, and so the AND gate and OR gate symbols must be changed to bubled outputs.
- The inverter has already bubble output

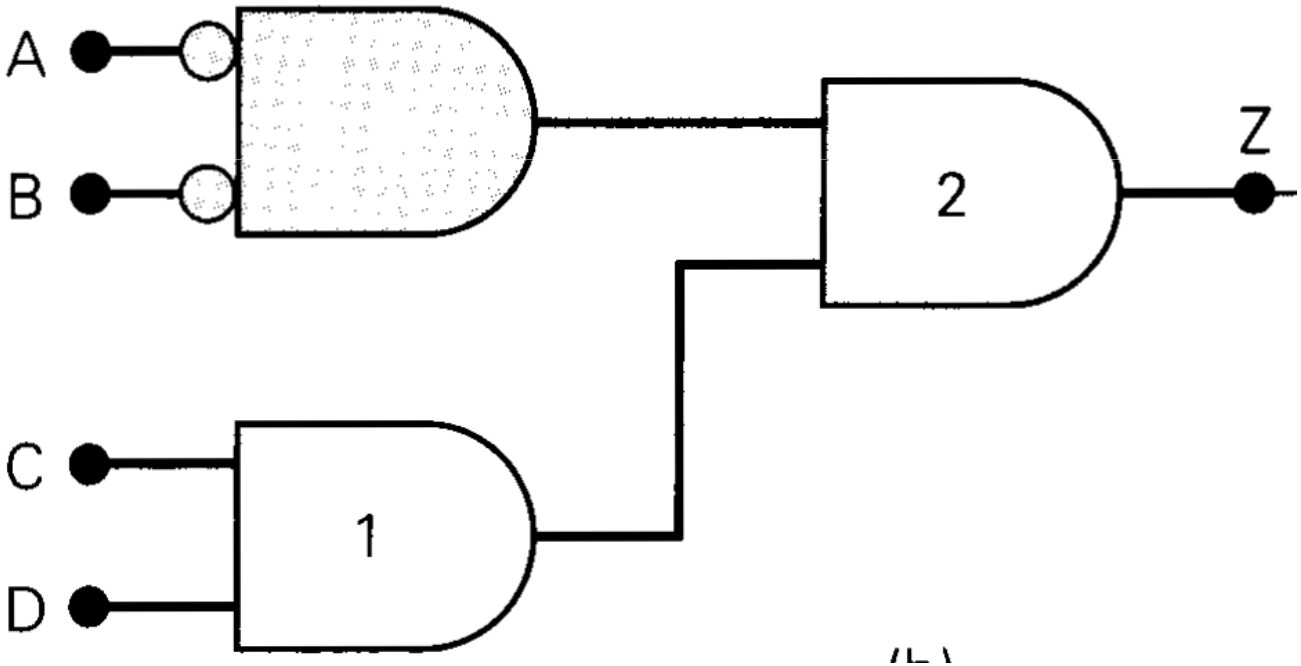


Example

- The logic ckt in fig is being used to activate an alarm when its output Z goes High. Modify the circuit diagram so that it represents the ckt operation more effectively.



Alternate logic ckt



Algebraic Simplification

- Place the expression in SOP form by applying DeMorgan's theorems and multiplying terms.
- Check the SOP form for common factors and perform factoring where possible.
- Note that this process may involve some trial and error to obtain the simplest result.

Designing Combinational Logic Circuits

- To solve any logic design problem:
  - Interpret the problem and set up its truth table.
  - Write the AND (product) term for each case where the output equals 1.
  - Combine the terms in SOP form.
  - Simplify the output expression if possible.
  - Implement the circuit for the final, simplified expression.

Example application:- Majority Circuit

A logic circuit having 3 inputs, A, B, C will have its output HIGH only when a majority of the inputs are HIGH.

Step 1 Set up the truth table

Step 2 Write the AND term for each case where the output is a 1.

A	B	C	x	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\rightarrow \bar{A}BC$
1	0	0	0	
1	0	1	1	$\rightarrow A\bar{B}C$
1	1	0	1	$\rightarrow AB\bar{C}$
1	1	1	1	$\rightarrow ABC$

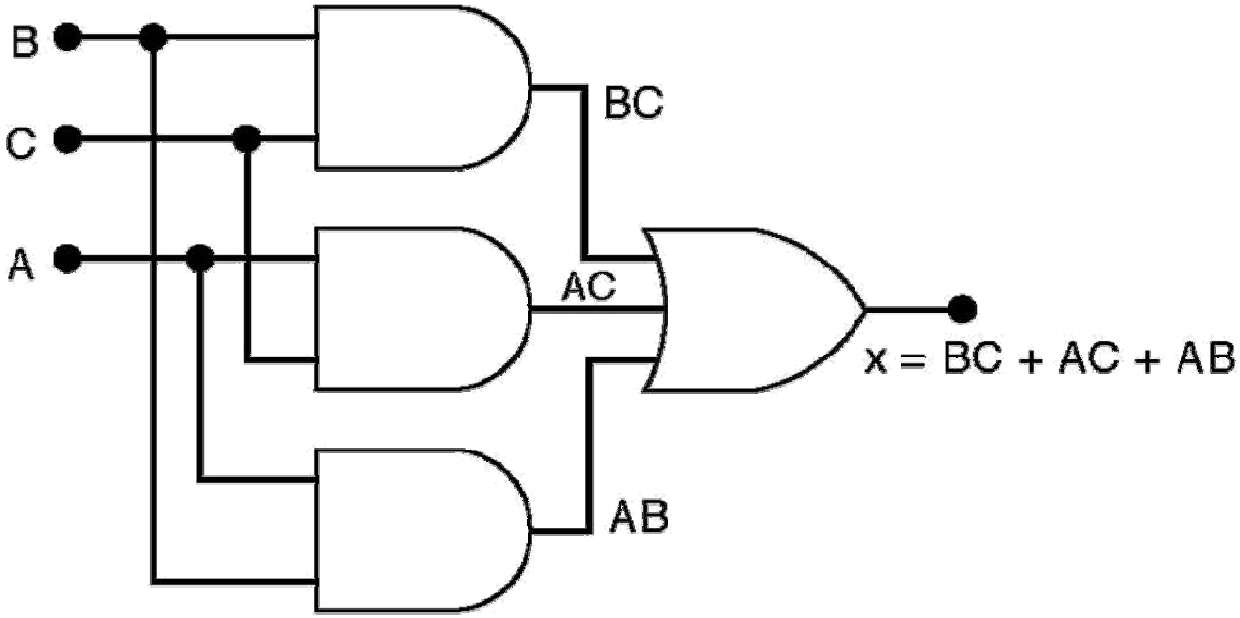
Step 3 Write the SOP form the output

$$X = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

Step 4 Simplify the output expression (ref. p. 119 of T1)

$$\begin{aligned} x &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\ x &= \bar{A}BC + ABC + A\bar{B}C + ABC + AB\bar{C} + ABC \\ &= BC(\bar{A} + A) + AC(\bar{B} + B) + AB(\bar{C} + C) \\ &= BC + AC + AB \end{aligned}$$

Step 5 Implement the circuit



Karnaugh Map Method

- A graphical method of simplifying logic equations or truth tables. Also called a K map.
- Theoretically can be used for any number of input variables, but practically limited to 5 or 6 variables.
- K Map shows the relationship between inputs & outputs

Karnaugh Map Method

- The truth table values are placed in the K map as shown in the next page.
- Adjacent K map square differ in only one variable both horizontally and vertically. $\overline{A}\,\overline{B}, \overline{A}B, AB, A\overline{B}$
- A SOP expression can be obtained by ORing all squares that contain a 1.

A	B	X
0	0	1 → $\overline{A}\,\overline{B}$
0	1	0
1	0	0
1	1	1 → AB

$$x = \overline{A}\,\overline{B} + AB$$

(a)

	$\overline{B}$	B
$\overline{A}$	1	0
A	0	1

Karnaugh maps and truth tables for three variables.

A	B	C	X	
0	0	0	1	$\rightarrow \bar{A}\bar{B}\bar{C}$
0	0	1	1	$\rightarrow \bar{A}\bar{B}C$
0	1	0	1	$\rightarrow \bar{A}B\bar{C}$
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	1	$\rightarrow AB\bar{C}$
1	1	1	0	

$$X = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C}$$

(b)

	$\bar{C}$	C
$\bar{A}\bar{B}$	1	1
$\bar{A}B$	1	0
AB	1	0
$A\bar{B}$	0	0

Karnaugh maps and truth tables for four variables.

A	B	C	D	X	
0	0	0	0	0	
0	0	0	1	1	→ $\bar{A}\bar{B}\bar{C}D$
0	0	1	0	0	
0	0	1	1	0	
0	1	0	0	0	
0	1	0	1	1	→ $\bar{A}B\bar{C}D$
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	
1	0	1	0	0	
1	0	1	1	0	
1	1	0	0	0	
1	1	0	1	1	→ $AB\bar{C}D$
1	1	1	0	0	
1	1	1	1	1	→ $ABCD$

$$X = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + AB\bar{C}D + ABCD$$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}B$	0	1	0	0
$\bar{A}B$	0	1	0	0
AB	0	1	1	0
$A\bar{B}$	0	0	0	0

(c)