WM9713 / 14 - Inverting the Jack Detect GPIO Logic

INTRODUCTION

The WM9713 and WM9714 AC'97 audio CODECs are often used in portable audio applications requiring headphone output. They include a feature to automatically switch from stereo speaker output to headphone audio output when the headphone jack is inserted. This note describes how to ensure that jack detection is correctly recognised by the WM9713 and WM9714 devices when designing such an application.

AUDIO SWITCH PROPERTIES

A typical headphone circuit configuration is shown in figure 1. It is important to understand the properties of a standard 3.5mm headphone jack. When the jack is removed from the socket, the switch is closed (Pin 11 connected to pin 3) and the GPIO line is typically designed to be pulled low via a low resistance path to ground (R4 in this example). When the jack is inserted into the socket, the switch opens (Pin 11 not connected to pin 3) and the GPIO line is typically designed to be pulled high to the supply voltage rail via a large resistance (R2 in this example). R2 is a 1 MΩ resistor and limits the current drawn from the supply. This effect is summarised in table 1.

JACK STATUS	ACTUAL GPIO VOLTAGE
Jack in	High (AVDD)
Jack out	Low (GND)

Table 1 Effect of Jack Insertion on GPIO Input Voltage Level
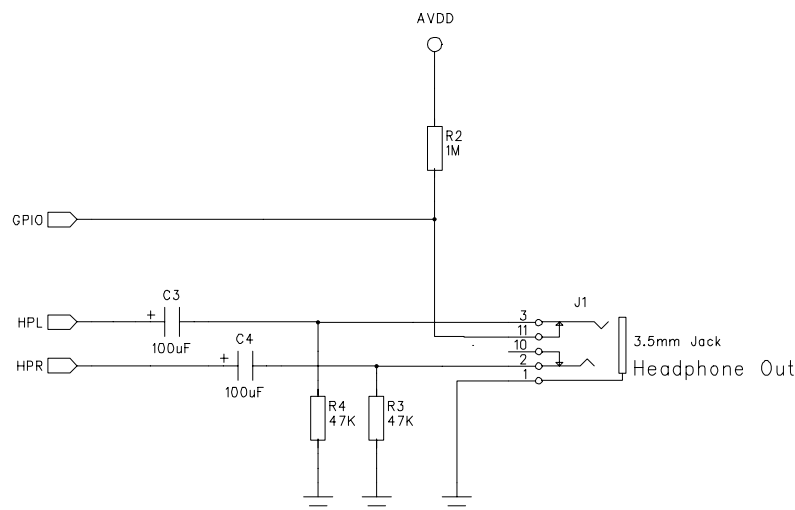

Figure 1 Typical Headphone Circuit Configuration

WM9713 AND WM9714 PROPERTIES

The presence of a headphone can be detected using one of four WM9713 / WM9714 GPIO pins. GPIO1/6/7/8 pins (pins 44, 3, 11 & 12) are available for this functionality. When the jack is inserted the GPIO expects to see a low voltage (logic 0) when the switch on the socket opens. When the jack is removed the GPIO expects to see a high signal level (logic 1) as the switch on the socket closes. If the JIEN bit is set, the WM9713 and WM9714 will automatically switch between headphone and any other output configuration, typically ear speaker or stereo speaker. This configuration can be set up in the Powerdown and output PGA Mux select registers.

Table 2 shows the expected logic levels on the GPIO line of the WM9713 and WM9714 devices when the jack is inserted and removed.

JACK STATUS	EXPECTED GPIO VOLTAGE
Jack in	Low (GND)
Jack out	High (VDD)

**Table 2 WM9713 / 14 GPIO Pin Expected Voltage Level for Jack Insert Status**

INVERTING THE SIGNAL POLARITY

It can be clearly observed from tables 1 and 2 that there is a difference between the actual GPIO logic level and the expected GPIO logic level.

JACK STATUS	ACTUAL GPIO VOLTAGE	EXPECTED GPIO VOLTAGE AT WM9713 / WM9714 DEVICE PIN
Jack in	High (AVDD)	Low (GND)
Jack out	Low (GND)	High (VDD)

Table 3 Comparison Between Expected and Actual Voltage on GPIO Line for Jack Insert Status

A signal inversion is needed to ensure that the GPIO line is at the correct logic level to enable jack detection to function properly. This signal inversion can be achieved using 2 extra components configured to operate as an inverting amplifier, as shown in figure 2. This circuit will invert the GPIO logic level from the jack switch circuit to ensure that it is at the correct level for jack detection at the GPIO pin (GPIO8 in this example) on the WM9713 or WM9714.
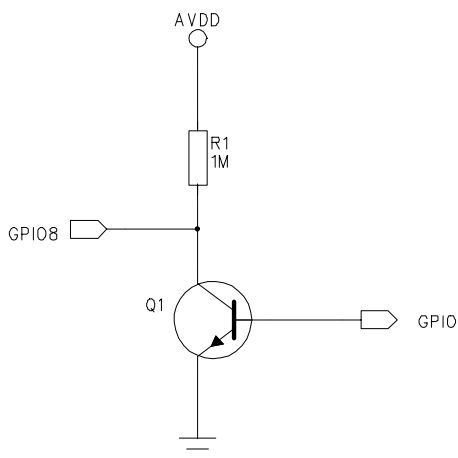

Figure 2 Inverting Amplifier

GPIO LOGIC LEVEL FROM 3.5MM SWITCH CIRCUIT	GPIO8 LOGIC LEVEL
High	Low
Low	High

Table 4 Input / Output Characteristics of Inverting Amplifier

The complete circuit from the headphone socket to the WM9713 / WM9714 device is shown in figure 3, with the WM9713 / 14 GPIO8 pin configured for jack insert detection. The HPL and HPR pins of the device are connected to the socket.
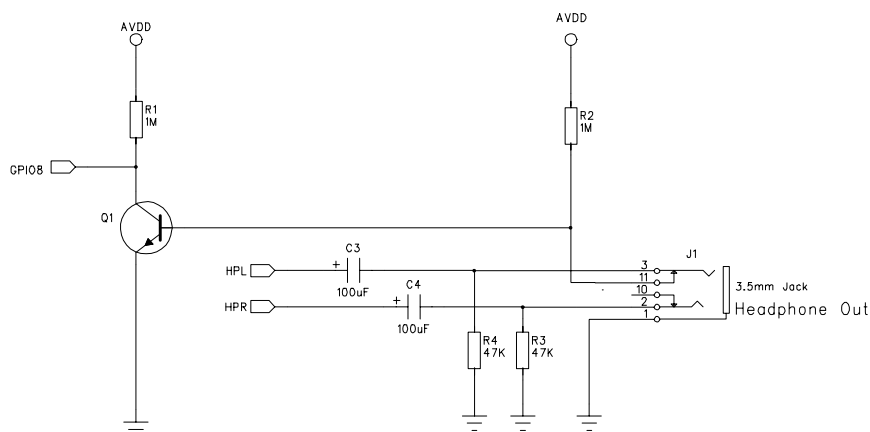
Figure 3 Complete Headphone Interface Circuit

USING THE GPIO LINE ON THE HOST PROCESSOR

Another method for enabling Jack detection is to use a GPIO pin on the system processor. The circuit from Figure 1 can be used in this configuration. Connect the GPIO line to the processor GPIO pin. The processor can be programmed to write a series of instructions to the appropriate WM9713 / WM9714 registers to enable headphone output and disable speaker output when the jack is inserted and the GPIO line logic level goes high. This method requires that the processor has a free GPIO pin.

SUMMARY

Jack detection is a key feature in many applications. This technical note has illustrated how to design the necessary circuitry between the 3.5 mm headphone socket and the WM9713 / WM9714 device. Applications based on these devices should ensure that the correct logic level is presented to the GPIO pin from the headphone jack circuit by following the circuit design detailed in this application note. Alternatively, the system processor GPIO system can be used to detect jack insertion and adjust audio output configuration as desired.

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

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