Tentative

BU26507GUL Function Description

BU26507GUL is “Matrix LED Driver” that is the most suitable for the cellular phone.
It can control 5x6 (30 dot) LED Matrix by internal 5-channel PMOS SWs and 6-channel LED drivers.
It can control the luminance and firefly lighting of the LED matrix by the setting of the internal register.
It supports SPI and I2C interface.
VCSP50L2(2.5 mmx2.5mm maximum 0.55mm height), small and thin type chip size package.
It adopts the very thin CSP package that is the most suitable for the slim phone.

● Functions LED Matrix driver (5x6)

- It has 5-channel PMOS SWs and 6-channel current drivers with 1/5 timing driven sequentially.
- Put ON/OFF(for every dot).
- The current drivers can drive 0-20.00mA current with “16” step(for every dot)(ISET=100kΩ).
- The current drivers can drive maximum 42.5mA/Line(ISET=47kΩ).
- 64 steps of the luminance control by PWM (common setting for all dots)
- Easy register setting by A/B 2-side map for each dot.
- Automatic Slope function
- Cycle time, Slope time can be set for each dot.
- 8-directions automatic scroll function.

Interface

・SPI and I^2C BUS FS mode（max 400kHz） Compatibility

・For I2C mode, I2C Device address is selectable (74h or 75h)

Thermal shutdown

Small and thin CSP package

・25pin VCSP50L2 (2.5mmx2.5mm maximum 0.55mm height) 0.5mm ball pitch

*This chip is not designed to protect itself against radioactive rays.
*This material may be changed on its way to designing.
*This material is not the official specification.

● Absolute Maximum Ratings (Ta=25 °C)

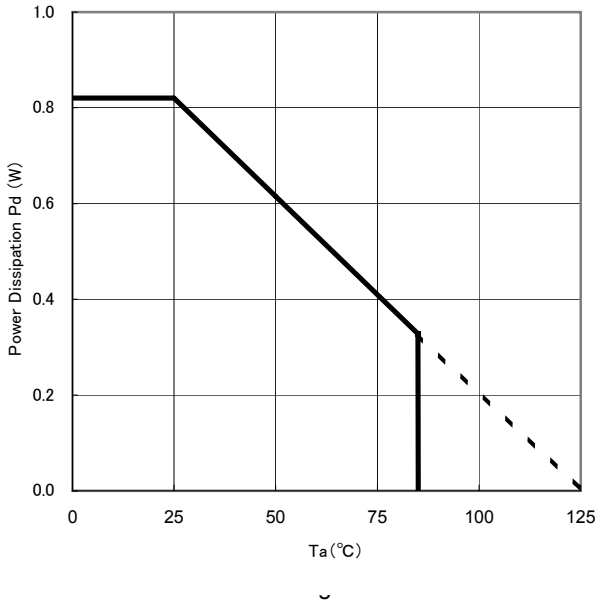
Parameter	Symbol	Limits	Unit
Maximum voltage (note2)	VMAX	7	V
Maximum voltage (note1)	VIOMAX	7	V
Power Dissipation (note3)	Pd	820 (TBD)	mW
Operating Temperature Range	Topr	-40 ～ +85	℃
Storage Temperature Range	Tstg	-55 ～ +125	℃

note1) VIO,RESETB,CE,SDA,SCL,IFMODE,SYNC,CLKIO,TEST1,TESTO, terminal

note2) Except the above

note3) Power dissipation deleting is 8.2(TBD)mW/ °C , when it's used in over 25 °C.
(ROHM's standard board has been mounted.)
The power dissipation of the IC has to be less than the one of the package.

● Power dissipation (On the ROHM's standard board)



Information of the ROHM's standard board
Material : glass-epoxy
Size : 50mm×58mm×1.75mm (8th layer)
Wiring pattern figure Refer to after page.

● Operating conditions (VBAT≥VIO, Ta=-40~85 °C)

Parameter	Symbol	Limits	Unit
VBAT input voltage	VBAT	2.7 ～ 5.5	V
VINSW input voltage	VINSW	2.7 ～ 5.5	V
VIO pin voltage	VIO	1.65 ～ 3.3	V

● Block Diagram / Application Circuit example 1

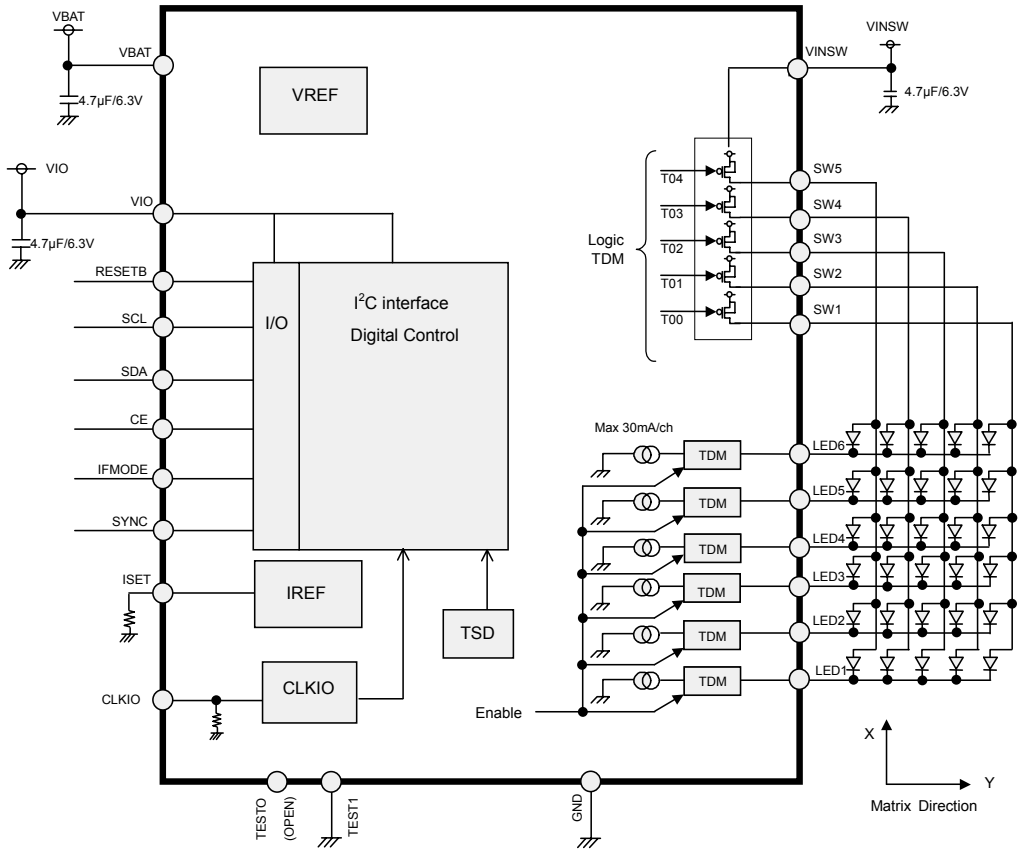


Fig.2 Block Diagram / Application Circuit example 1

● Pin Arrangement［Bottom View］

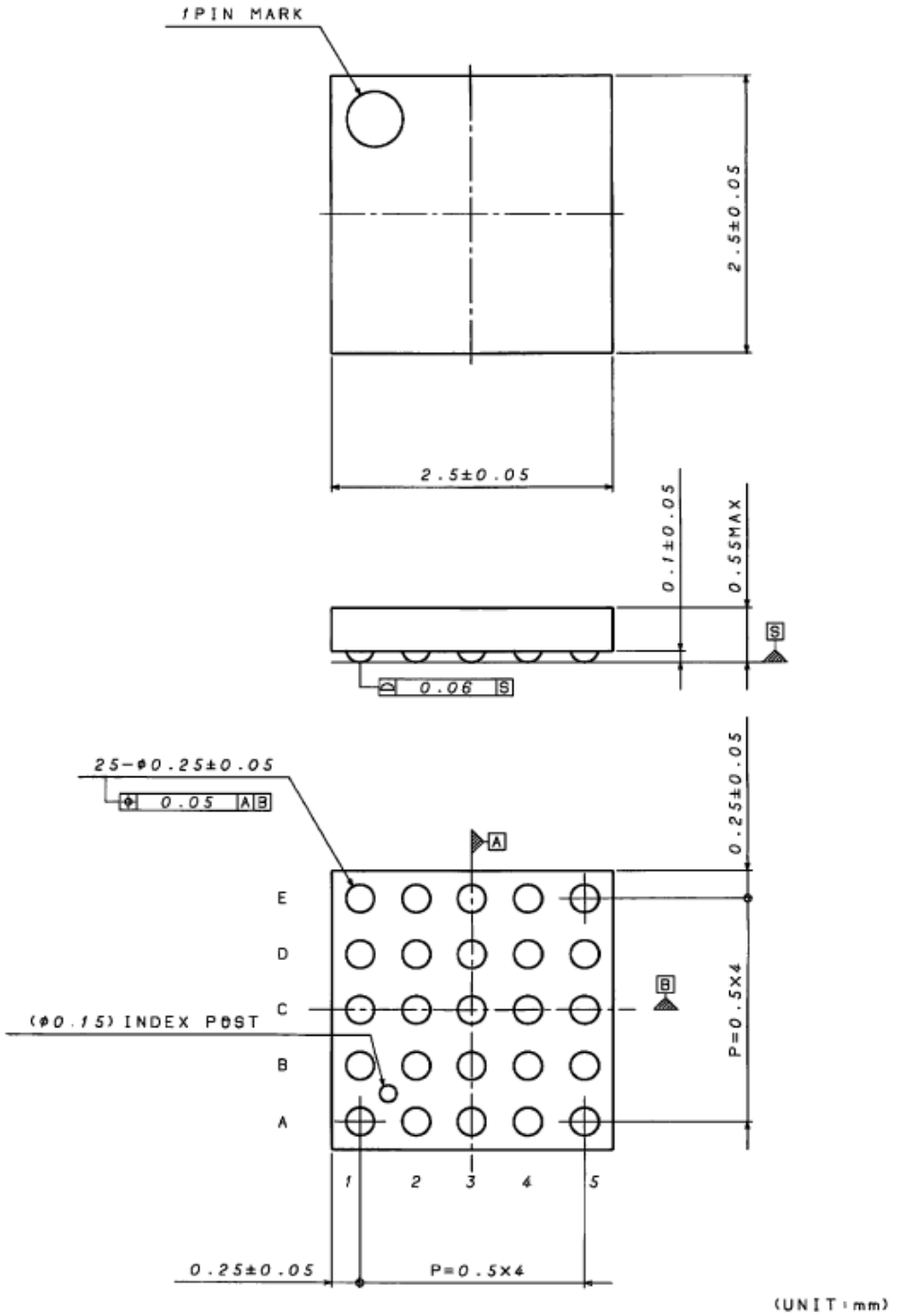
E	TEST1	SCL	SDA	SW5	SW4
D	CE	RESETB	SYNC	SW3	VINSW
C	VIO	IFMODE	TESTO	SW2	SW1
B	CLKIO	ISET	LED2	LED4	LED5
A	VBAT	LED1	LED3	GND	LED6
	1	2	3	4	5

Index

Total 25Balls

● Package

25Pin VCSP50L2　CSP small package
SIZE : 2.5mm x 2.5mm
A ball pitch : 0.5mm
Height : 0.55mm max



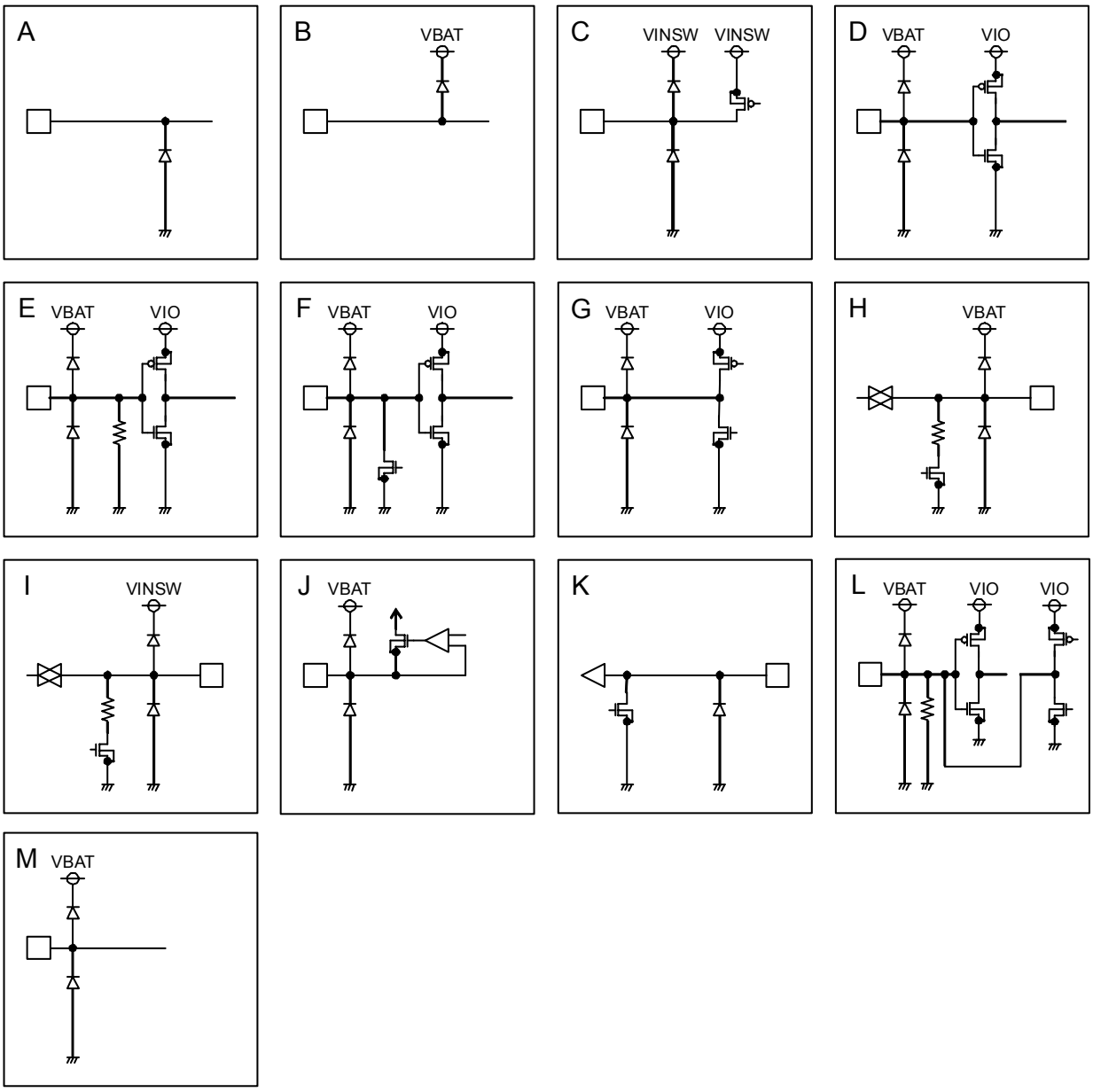
● Pin Functions

No	Ball No.	Pin Name	I/O	Pull down [ohm]	Unused processing setting	ESD Diode		Functions	Equivalent Circuit
						For Power	For Ground		
1	D5	VINSW	-	-	VINSW	–	GND	Power supply for SW1-5	A
2	A1	VBAT	-	-	VBAT	–	GND	Battery is connected	A
3	C1	VIO	-	-	VIO	VBAT	GND	I/O Power supply is connected	M
4	D2	RESETB	I	-	GND	VBAT	GND	Reset input pin (L: reset, H: reset cancel)	D
5	E2	SCL	I	-	GND	VBAT	GND	SPI, I2C CLK input pin	D
6	E3	SDA	I/O	-	GND	VBAT	GND	SPI DATA input / I2C DATA input-output pin	F
7	D1	CE	I	-	GND	VBAT	GND	SPI enable pin(H;Enable), or I2C slave address selection (L: 74h, H: 75h)	D
8	C2	IFMODE	I	-	GND	VBAT	GND	I2C/SPI select pin (L: I2C, H: SPI)	D
9	D3	SYNC	I	-	GND	VBAT	GND	External synchronous input pin	D
10	B2	ISET	I	-	OPEN	VBAT	GND	LED Constant Current Driver Current setting pin	J
11	B1	CLKIO	I/O	500k	OPEN	VBAT	GND	Reference CLK in/out pin	L
12	C3	TESTO	O	-	OPEN	VBAT	GND	Test output pin	H
13	E1	TEST1	I	100k	GND	VBAT	GND	Test input pin 1	E
14	A4	GND	-	-	GND	VBAT	-	Ground	B
15	A2	LED1	O	-	GND	–	GND	LED1 driver output	K
16	B3	LED2	O	-	GND	–	GND	LED2 driver output	K
17	A3	LED3	O	-	GND	–	GND	LED3 driver output	K
18	B4	LED4	O	-	GND	–	GND	LED4 driver output	K
19	B5	LED5	O	-	GND	–	GND	LED5 driver output	K
20	A5	LED6	O	-	GND	–	GND	LED6 driver output	K
21	C5	SW1	O	-	VINSW	VINSW	GND	P-MOS SW１output	C
22	C4	SW2	O	-	VINSW	VINSW	GND	P-MOS SW2 output	C
23	D4	SW3	O	-	VINSW	VINSW	GND	P-MOS SW3 output	C
24	E5	SW4	O	-	VINSW	VINSW	GND	P-MOS SW4 output	C
25	E4	SW5	O	-	VINSW	VINSW	GND	P-MOS SW５ output	C

* Please connect the unused LED pins to the ground.
* It is prohibition to set the registers for unused LED.

Total 25 pins

● Equivalent Circuit



● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[Circuit Current]						
VBAT Circuit current 1	IBAT1	-	0	3.0	μA	RESETB=0V, VIO=0V
VBAT Circuit current 2	IBAT2	-	0.5	5.0	μA	RESETB=0V, VIO=1.8V
VBAT Circuit current 3	IBAT3	-	0.8	1.4	mA	When LED1-6 are active with default settings.
[UVLO]						
UVLO Threshold	VUVLO	-	2.1	2.5	V	VBAT falling
UVLO Hysteresis	VHYUVLO	50	-	-	mV	
[LED Driver] (LED1-6)						
Maximum output current	ILEDMax1	-	20.00	-	mA	LED1-6 ,ISET＝100kΩ
	ILEDMax2	-	42.50	-	mA	LED1-6 ,ISET＝47kΩ
Output current	ILED	-7.0%	10.67	+7.0%	mA	I=10.67mA setting, VLED=1V,ISET=100 kΩ
LED current Matching	ILEDMT	-	-	5	%	ILEDMT= (ILEDMax-ILEDMin)/(ILEDMax+ILEDMin) I=10.67mA setting, VLED=1V
Driver pin voltage range	VLED	0.2	-	VBAT - 1.4	V	ISET=100 kΩ
LED OFF Leak current	ILKLED	-	-	1.0	μA	
[PMOS switch]						
Leak current at OFF	ILEAKP	-	-	1.0	μA	
Resistor at ON	RonP	-	1.0	-	Ω	Isw=60mA, VINSW=4.5V
[OSC]						
OSC frequency	fosc	0.96	1.2	1.44	MHz	
[CE, SYNC, IFMODE]						
L level input voltage	VIL1	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH1	0.75 x VIO	-	VIO +0.3	V	
L level input current	IIL1	-	0	1	μA	
H level input current	IIH1	-	0	1	μA	
[SDA, SCL]						
L level input voltage	VIL2	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH2	0.75 x VIO	-	VIO +0.3	V	
Input hysteresis	Vhys	0.05 x VIO	-	-	V	
L level output voltage (for SDA pin)	VOL2	0	-	0.3	V	At 3mA sink current
Input current	Iin1	-3	-	3	μA	Input voltage = from (0.1 x VIO) to (0.9 x VIO)
[RESETB]						
L level input voltage	VIL3	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH3	0.75 x VIO	-	VIO +0.3	V	
Input current	Iin2	-	0	1	μA	Input voltage = from (0.1 x VIO) to (0.9 x VIO)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[CLKIO(OUTPUT)]						
L level output voltage	VOL1	-	-	0.4	V	IOL=2mA
H level output voltage	VOH1	0.75 x VIO	-	-	V	IOH=-2mA
[CLKIO(INPUT)]						
L level input voltage	VIL4	-0.3	-	0.25 x VIO	V	
H level input voltage	VIH4	0.75 x VIO	-	VIO +0.3	V	
Input current	Iin3	-	3.6	10	μA	input voltage=1.8V

●Serial Interface

1. SPI format

- When IFMODE is set to “H”, it can interface with SPI format.
- The serial interface is three terminals (serial clock terminal (SCL), serial data input terminal (SDA), and chip selection input terminal (CE)).

（1）Write operation

- Data is taken into an internal shift register with rising edge of CLK. (Max of the frequency is 13MHz.)
- The receive data becomes enable in the “H" section of CE. (Active “H".)
- The transmit data is forwarded (with MSB-First) in the order of write command “0”(1bit), the control register address (7bit) and data (8bit).

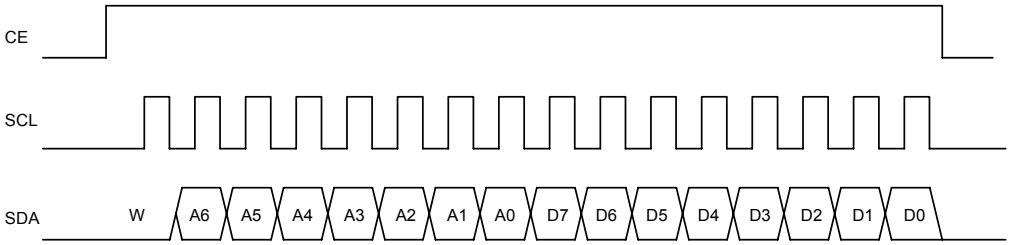


Fig.4 Writing format

（2）Timing diagram

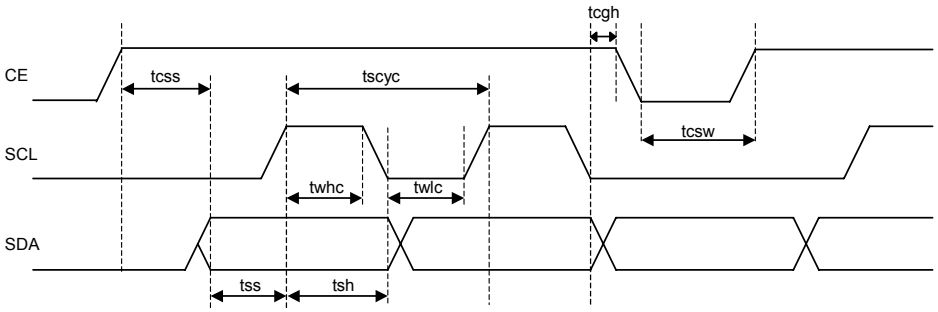


Fig.5 Timing diagram (SPI format)

(3) Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
SCL cycle time	tscyc	76	-	-	ns	
H period of SCL cycle	Twhc	35	-	-	ns	
L period of SCL cycle	twlc	35	-	-	ns	
SDA setup time	tss	38	-	-	ns	
SDA hold time	tsh	38	-	-	ns	
Read and Write interval	tcsw	2.1	-	-	μs	*1
Read and Weite interval (after A or B map accsess)		ECLK x 2	-	-	s	*2
CE setup time	tcss	55	-	-	ns	
CE hold time	tcgh	55	-	-	ns	

*1 When it used internal clock.

*2 When it used external clock. ECLK means the cycle of external PWM clock.)

2. I^2C BUS format

When IFMODE is set to “L”, it can interface with I^2C BUS format.

(1) Slave address

CE	A7	A6	A5	A4	A3	A2	A1	R/W
L	1	1	1	0	1	0	0	0
H	1	1	1	0	1	0	1	

(2) Bit Transfer

SCL transfers 1-bit data during H. During H of SCL, SDA cannot be changed at the time of bit transfer. If SDA changes while SCL is H, START conditions or STOP conditions will occur and it will be interpreted as a control signal.

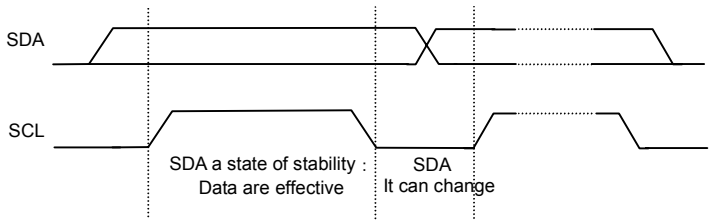


Fig.6 Bit transfer (I2C format)

(3) START and STOP condition

When SDA and SCL are H, data is not transferred on the I^2C- bus. This condition indicates, if SDA changes from H to L while SCL has been H, it will become START (S) conditions, and an access start, if SDA changes from L to H while SCL has been H, it will become STOP (P) conditions and an access end.

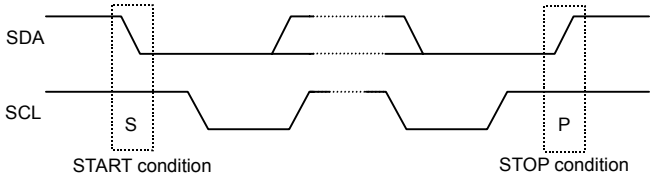


Fig.7 START/STOP condition (I2C format)

(4) Acknowledge

It transfers data 8 bits each after the occurrence of START condition. A transmitter opens SDA after transfer 8bits data, and a receiver returns the acknowledge signal by setting SDA to L.

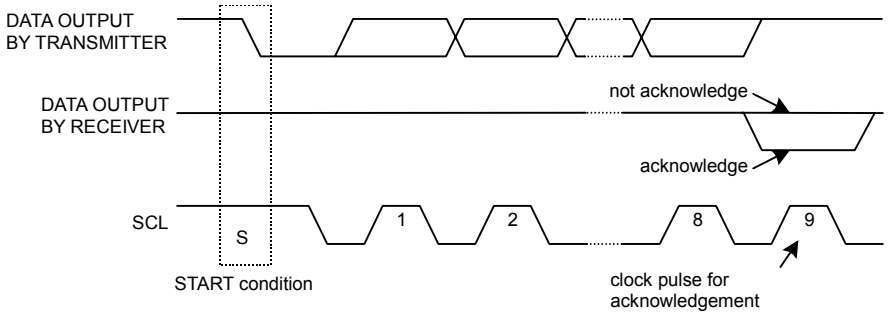
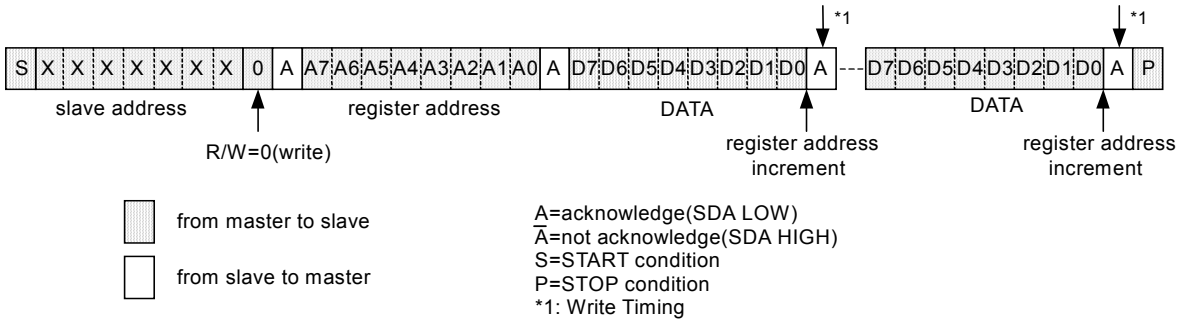


Fig.8 Acknowledge (I2C format)

(5) Writing protocol

A register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The 3rd byte writes data in the internal register written in by the 2nd byte, and after 4th byte or, the increment of register address is carried out automatically. However, when a register address turns into the last address (77h), it is set to 00h by the next transmission. After the transmission end, the increment of the address is carried out.



(6) Timing diagram

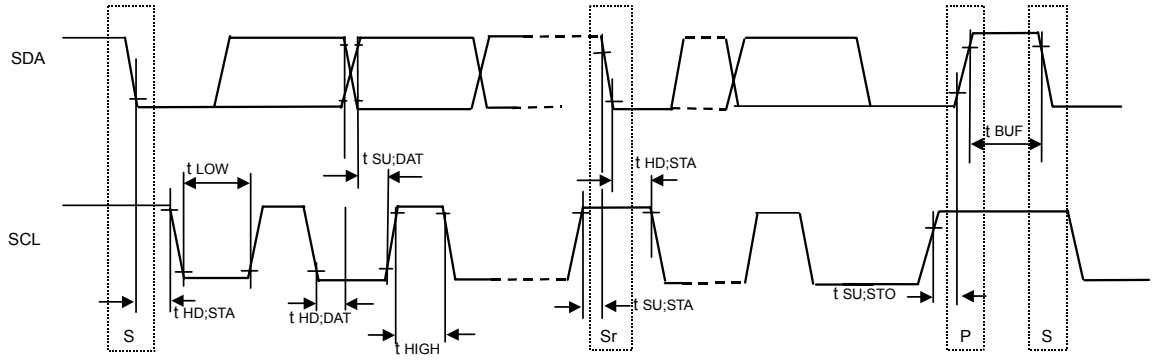


Fig.9 Timing diagram (I2C format)

(7) Electrical Characteristics(Unless otherwise specified, Ta=25 °C, VBAT=3.6V, VINSW=3.6V, VIO=1.8V)

Parameter	Symbol	Standard-mode			Fast-mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
【I²C BUS format】								
SCL clock frequency	fSCL	0	-	100	0	-	400	kHz
LOW period of the SCL clock	tLOW	4.7	-	-	1.3	-	-	µs
HIGH period of the SCL clock	tHIGH	4.0	-	-	0.6	-	-	µs
Hold time (repeated) START condition After this period, the first clock is generated	tHD;STA	4.0	-	-	0.6	-	-	µs
Set-up time for a repeated START condition	tSU;STA	4.7	-	-	0.6	-	-	µs
Data hold time	tHD;DAT	0	-	3.45	0	-	0.9	µs
Data set-up time	tSU;DAT	250	-	-	100	-	-	ns
Set-up time for STOP condition	tSU;STO	4.0	-	-	0.6	-	-	µs
Bus free time between a STOP and START condition	tBUF	4.7	-	-	1.3	-	-	µs

● Register List

* Please be sure to write “0” in the register which is not assigned.
* It is prohibition to write data to the address which is not assigned.

Control register

Address	default	D7	D6	D5	D4	D3	D2	D1	D0	Block	R/W	Remark
00h	00h	-	-	-	-	-	-	-	SFTRST	RESET	W	Software Reset
01h	00h	-	-	-	-	OSCEN	-	-	-	OSC	W	OSC ON/OFF control
11h	00h	-	-	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1ON	LED driver	W	LED1-6 Enable
20h	00h	-	-	PWMSET[5:0]						PWM	W	LED1-6 PWM setting
21h	00h	CLKSEL[1:0]		-	-	SYNCACT	SYNCON	CLKOUT	CLKIN	CLK	W	CLK selection, SYNC operation control
2Dh	00h	-	-	-	SLP[1:0]		PWMEN	SLPEN	SCLEN	MATRIX	W	PWM,SLOPE,SCROL ON/OFF setting
2Eh	00h	-	-	-	-	-	-	-	SCLRST		W	Reset SCROL
2Fh	00h	SCLSPEEDUP	SCLSPEED[2:0]			UP	DOWN	RIGHT	LEFT		W	Scroll setting
30h	00h	-	-	-	-	-	-	-	START		W	LED matrix control
31h	0h	-	-	-	-	-	-	CLRB	CLRA		W	Matrix data clear
7Fh	00h	-	-	-	-	-	IAB	OAB	RMCG	RMAP	W	Resistor map cahnge

A-pattern register

Address	default	D7	D6	D5	D4	D3	D2	D1	D0	Block	R/W	Remark
01h	08h	SCYCA00[1:0]		SDLYA00[1:0]		ILEDA00SET[3:0]				MATRIX DATA	W	Data for Matrix 00(DA00)
02h	08h	SCYCA01[1:0]		SDLYA01[1:0]		ILEDA01SET[3:0]					W	Data for Matrix 01(DA01)
03h	08h	SCYCA02[1:0]		SDLYA02[1:0]		ILEDA02SET[3:0]					W	Data for Matrix 02(DA02)
04h	08h	SCYCA03[1:0]		SDLYA03[1:0]		ILEDA03SET[3:0]					W	Data for Matrix 03(DA03)
05h	08h	SCYCA04[1:0]		SDLYA04[1:0]		ILEDA04SET[3:0]					W	Data for Matrix 04(DA04)
06h	08h	SCYCA10[1:0]		SDLYA10[1:0]		ILEDA10SET[3:0]					W	Data for Matrix 10(DA10)
07h	08h	SCYCA11[1:0]		SDLYA11[1:0]		ILEDA11SET[3:0]					W	Data for Matrix 11(DA11)
08h	08h	SCYCA12[1:0]		SDLYA12[1:0]		ILEDA12SET[3:0]					W	Data for Matrix 12(DA12)
09h	08h	SCYCA13[1:0]		SDLYA13[1:0]		ILEDA13SET[3:0]					W	Data for Matrix 13(DA13)
0Ah	08h	SCYCA14[1:0]		SDLYA14[1:0]		ILEDA14SET[3:0]					W	Data for Matrix 14(DA14)
0Bh	08h	SCYCA20[1:0]		SDLYA20[1:0]		ILEDA20SET[3:0]					W	Data for Matrix 20(DA20)
0Ch	08h	SCYCA21[1:0]		SDLYA21[1:0]		ILEDA21SET[3:0]					W	Data for Matrix 21(DA21)
0Dh	08h	SCYCA22[1:0]		SDLYA22[1:0]		ILEDA22SET[3:0]					W	Data for Matrix 22(DA22)
0Eh	08h	SCYCA23[1:0]		SDLYA23[1:0]		ILEDA23SET[3:0]					W	Data for Matrix 23(DA23)
0Fh	08h	SCYCA24[1:0]		SDLYA24[1:0]		ILEDA24SET[3:0]					W	Data for Matrix 24(DA24)
10h	08h	SCYCA30[1:0]		SDLYA30[1:0]		ILEDA30SET[3:0]					W	Data for Matrix 30(DA30)
11h	08h	SCYCA31[1:0]		SDLYA31[1:0]		ILEDA31SET[3:0]					W	Data for Matrix 31(DA31)
12h	08h	SCYCA32[1:0]		SDLYA32[1:0]		ILEDA32SET[3:0]					W	Data for Matrix 32(DA32)
13h	08h	SCYCA33[1:0]		SDLYA33[1:0]		ILEDA33SET[3:0]					W	Data for Matrix 33(DA33)
14h	08h	SCYCA34[1:0]		SDLYA34[1:0]		ILEDA34SET[3:0]					W	Data for Matrix 34(DA34)
15h	08h	SCYCA40[1:0]		SDLYA40[1:0]		ILEDA40SET[3:0]					W	Data for Matrix 40(DA40)
16h	08h	SCYCA41[1:0]		SDLYA41[1:0]		ILEDA41SET[3:0]					W	Data for Matrix 41(DA41)
17h	08h	SCYCA42[1:0]		SDLYA42[1:0]		ILEDA42SET[3:0]					W	Data for Matrix 42(DA42)
18h	08h	SCYCA43[1:0]		SDLYA43[1:0]		ILEDA43SET[3:0]					W	Data for Matrix 43(DA43)
19h	08h	SCYCA44[1:0]		SDLYA44[1:0]		ILEDA44SET[3:0]					W	Data for Matrix 44(DA44)
1Ah	08h	SCYCA50[1:0]		SDLYA50[1:0]		ILEDA50SET[3:0]					W	Data for Matrix 50(DA50)
1Bh	08h	SCYCA51[1:0]		SDLYA51[1:0]		ILEDA51SET[3:0]					W	Data for Matrix 51(DA51)
1Ch	08h	SCYCA52[1:0]		SDLYA52[1:0]		ILEDA52SET[3:0]					W	Data for Matrix 52(DA52)
1Dh	08h	SCYCA53[1:0]		SDLYA53[1:0]		ILEDA53SET[3:0]					W	Data for Matrix 53(DA53)
1Eh	08h	SCYCA54[1:0]		SDLYA54[1:0]		ILEDA54SET[3:0]					W	Data for Matrix 54(DA54)

B-pattern register

Address	default	D7	D6	D5	D4	D3	D2	D1	D0	Block	R/W	Remark
01h	08h	SCYCB00[1:0]		SDLYB00[1:0]		ILEDB00SET[3:0]				MATRIX DATA	W	Data for Matrix 00(DB00)
02h	08h	SCYCB01[1:0]		SDLYB01[1:0]		ILEDB01SET[3:0]					W	Data for Matrix 01(DB01)
03h	08h	SCYCB02[1:0]		SDLYB02[1:0]		ILEDB02SET[3:0]					W	Data for Matrix 02(DB02)
04h	08h	SCYCB03[1:0]		SDLYB03[1:0]		ILEDB03SET[3:0]					W	Data for Matrix 03(DB03)
05h	08h	SCYCB04[1:0]		SDLYB04[1:0]		ILEDB04SET[3:0]					W	Data for Matrix 04(DB04)
06h	08h	SCYCB10[1:0]		SDLYB10[1:0]		ILEDB10SET[3:0]					W	Data for Matrix 10(DB10)
07h	08h	SCYCB11[1:0]		SDLYB11[1:0]		ILEDB11SET[3:0]					W	Data for Matrix 11(DB11)
08h	08h	SCYCB12[1:0]		SDLYB12[1:0]		ILEDB12SET[3:0]					W	Data for Matrix 12(DB12)
09h	08h	SCYCB13[1:0]		SDLYB13[1:0]		ILEDB13SET[3:0]					W	Data for Matrix 13(DB13)
0Ah	08h	SCYCB14[1:0]		SDLYB14[1:0]		ILEDB14SET[3:0]					W	Data for Matrix 14(DB14)
0Bh	08h	SCYCB20[1:0]		SDLYB20[1:0]		ILEDB20SET[3:0]					W	Data for Matrix 20(DB20)
0Ch	08h	SCYCB21[1:0]		SDLYB21[1:0]		ILEDB21SET[3:0]					W	Data for Matrix 21(DB21)
0Dh	08h	SCYCB22[1:0]		SDLYB22[1:0]		ILEDB22SET[3:0]					W	Data for Matrix 22(DB22)
0Eh	08h	SCYCB23[1:0]		SDLYB23[1:0]		ILEDB23SET[3:0]					W	Data for Matrix 23(DB23)
0Fh	08h	SCYCB24[1:0]		SDLYB24[1:0]		ILEDB24SET[3:0]					W	Data for Matrix 24(DB24)
10h	08h	SCYCB30[1:0]		SDLYB30[1:0]		ILEDB30SET[3:0]					W	Data for Matrix 30(DB30)
11h	08h	SCYCB31[1:0]		SDLYB31[1:0]		ILEDB31SET[3:0]					W	Data for Matrix 31(DB31)
12h	08h	SCYCB32[1:0]		SDLYB32[1:0]		ILEDB32SET[3:0]					W	Data for Matrix 32(DB32)
13h	08h	SCYCB33[1:0]		SDLYB33[1:0]		ILEDB33SET[3:0]					W	Data for Matrix 33(DB33)
14h	08h	SCYCB34[1:0]		SDLYB34[1:0]		ILEDB34SET[3:0]					W	Data for Matrix 34(DB34)
15h	08h	SCYCB40[1:0]		SDLYB40[1:0]		ILEDB40SET[3:0]					W	Data for Matrix 40(DB40)
16h	08h	SCYCB41[1:0]		SDLYB41[1:0]		ILEDB41SET[3:0]					W	Data for Matrix 41(DB41)
17h	08h	SCYCB42[1:0]		SDLYB42[1:0]		ILEDB42SET[3:0]					W	Data for Matrix 42(DB42)
18h	08h	SCYCB43[1:0]		SDLYB43[1:0]		ILEDB43SET[3:0]					W	Data for Matrix 43(DB43)
19h	08h	SCYCB44[1:0]		SDLYB44[1:0]		ILEDB44SET[3:0]					W	Data for Matrix 44(DB44)
1Ah	08h	SCYCB50[1:0]		SDLYB50[1:0]		ILEDB50SET[3:0]					W	Data for Matrix 50(DB50)
1Bh	08h	SCYCB51[1:0]		SDLYB51[1:0]		ILEDB51SET[3:0]					W	Data for Matrix 51(DB51)
1Ch	08h	SCYCB52[1:0]		SDLYB52[1:0]		ILEDB52SET[3:0]					W	Data for Matrix 52(DB52)
1Dh	08h	SCYCB53[1:0]		SDLYB53[1:0]		ILEDB53SET[3:0]					W	Data for Matrix 53(DB53)
1Eh	08h	SCYCB54[1:0]		SDLYB54[1:0]		ILEDB54SET[3:0]					W	Data for Matrix 54(DB54)

● Register Map

Address 00H < Software Reset >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	W	-	-	-	-	-	-	-	SFTRST
Initial value	00H	-	-	-	-	-	-	-	0

Bit 0：SFTRST Software Reset
“0”： Reset cancel
“1”： Reset（All register initializing）
* SFTRST register return to 0 automatically.

Address 01H <OSC control >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01H	W	-	-	-	-	OSCEN	-	-	-
Initial value	00H	0	0	0	0	0	0	0	0

Bit 3：OSCEN OSC block ON/OFF control
“0”：OFF（Initial）
“1”：ON

* This register should not change into "1 "→" 0" at the time of START (30h, D0) register ="1" setup (under lighting operation).
This register must be set to "0" after LED putting out lights ("START register = 0"), and please surely stop an internal oscillation circuit.

Address 11H < LED1-6 Enable >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11H	W	-	-	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1ON
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：LED1ON LED1 ON/OFF setting
“0”：LED1 OFF（initial）
“1”：LED1 ON

Bit 1：LED2ON LED2 ON/OFF setting
“0”：LED2 OFF（initial）
“1”：LED2 ON

Bit 2：LED3ON LED3 ON/OFF setting
“0”：LED3 OFF（initial）
“1”：LED3 ON

Bit 3：LED4ON LED4 ON/OFF setting
“0”：LED4 OFF（initial）
“1”：LED4 ON

Bit 4：LED5ON LED5 ON/OFF setting
“0”：LED5 OFF（initial）
“1”：LED5 ON

Bit 5：LED6ON LED6 ON/OFF setting
“0”：LED6 OFF（initial）
“1”：LED6 ON

* Current setting follows ILEDAXXSET[3:0] or ILEDBXXSET[3:0] register.
(The “XX” shows the matrix number from “00” to “54”. Please refer 5x6 LED Matrix coordinate.)

Address 20H < LED1-6 PWM setting >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20H	W	-	-	PWMSET [5:0]					
Initial value	00H	0	0	0	0	0	0	0	0

Bit 5-0：PWMSET[5:0] LED1-6 PWM DUTY setting

“000000”	0/63＝0%(initial)
“000001”	1/63＝1.59%
	:
“100000”	32/63＝50.8%
	:
“111110”	62/63＝98.4%
“111111”	63/63＝100%

*Please refer to Description of operation, chapter 2 SYNC operation control

Address 21H <Clock control SYNC operation control>

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21H	W	CLKSEL[1:0]		-	-	SYNCACT	SYNCON	CLKOUT	CLKIN
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：CLKIN Selection CLK for PWM control

“0”：Internal OSC (initial)

“1”：External CLK input

*When use external clock for TDM, Set OSCEN (01h, D3) register =”1”.

Bit 1：CLKOUT Output CLK enable

“0”：CLK is not output (initial)

“1”：Output selected CLK from CLKOUT pin

*As for CLKIN & CLKOUT, setting change is forbidden under OSCEN (01h, D3) register =”1” and also under clock input to CLKIN terminal.

*CLKIN=CLKOUT=1 is forbidden

Bit 2：SYNCON SYNC operation enable

“0”：Disable SYNC operation (initial)

“1”：SYNC pin control LED driver ON/OFF

Bit 3：SYNCACT SYNC operation setting

“0”：When SYNC pin is “L”, LED drivers are ON (initial)

“1”：When SYNC pin is “H”, LED drivers are ON

Bit 7-6：CLKSEL[1:0] Select Clock Frequency

“00”：1.2MHz

“01”：300kHz

“10”：150kHz

“11”：37.5kHz

Address 2DH < PWM, SLOPE, SCROLL ON/OFF setting >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2DH	W	-	-	-	SLP[1:0]		PWMEN	SLPEN	SCLEN
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：SCLEN SCROLL operation ON/OFF setting
“0”：SCROL operation OFF（initial value）
“1”：SCROL operation ON

Bit 1：SLPEN SLOPE operation ON/OFF setting
“0”：SLOPE operation OFF（initial value）
“1”：SLOPE operation ON

Bit 2：PWMEN PWM control at LED1-6ON/OFF setting
“0”：PWM operation is invalid（initial value）
“1”：PWM operation is valid

Bit 4-3：SLP SLOPE setting
“00”：1/4 slope cycle time
“01”：None slope
“10”：1/2 lope cycle time
“11”：1/4 slope cycle time

*Please refer to Description of operation, chapter 2
When start register (Address=30H Bit0) is 1, Don’t change SLP[1:0] register.

Address 2EH < Reset scroll >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2EH	W	-	-	-	-	-	-	-	SCLRST
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：SCLRST Reset scroll state
“0”：Not reset（initial value）
“1”：Reset scroll state
* SCLRST register return to 0 automatically

Address 2FH < Scroll setting >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2FH	W	SCL SPEEDUP	SCLSPEED [2:0]			UP	DOWN	RIGHT	LEFT
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：LEFT Setting the scroll operation from right to left
“0”：Scroll operation OFF (initial value)
“1”：Scroll operation ON

Bit 1：RIGHT Setting the scroll operation from left to right
“0”：Scroll operation OFF (initial value)
“1”：Scroll operation ON

*When LEFT operation is valid, RIGHT setting is ignored.

Bit 2：DOWN Setting the scroll operation from top to bottom
“0”：Scroll operation OFF (initial value)
“1”：Scroll operation ON

Bit 3：UP Setting the scroll operation from bottom to top
“0”：Scroll operation OFF (initial value)
“1”：Scroll operation ON

*When UP operation is valid, DOWN setting is ignored.

Bit 6-4：SCLSPEED[2:0] Setting the scroll speed
Bit 7 ：SCLSPEEDUP Setting the scroll speed UP

SCLSPEED[2:0]	SCLSPEEDUP=0	SCLSPEEDUP=1
“000”	0.1 sec (initial value)	0.0119 sec
“001”	0.2 sec	0.0238 sec
“010”	0.3 sec	0.0357 sec
“011”	0.4 sec	0.0476 sec
“100”	0.5 sec	0.0595 sec
“101”	0.6 sec	0.0714 sec
“110”	0.7 sec	0.0833 sec
“111”	0.8 sec	0.0952 sec

*Setting time is based on OSC frequency, and the above-mentioned shows the value under Typ (1.2MHz).
*Setting time changes on CLKIO terminal input frequency at the external clock operation.

Example) SCLSPEEDUP=0
CLKIO input frequency=1.2MHz→SCLSPEED[2:0] = "000": 0.1[s] (it is the same as the above)
CLKIO input frequency=2.4MHz→SCLSPEED[2:0] = "000": 0.05[s]
CLKIO input frequency= 0.6MHz→SCLSPEED[2:0] = "000”: 0.2[s]

* SCLSPEED[2:0] and SCLSPEEDUP should not change value at the time of START (30h, D0) register ="1" setup (under lighting operation).

Address 30H < LED Matrix control >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30H	W	-	-	-	-	-	-	-	START
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：START Lighting/turning off bit of MATRIX LED(LED1-6)
“0”：MATRIX LED（LED1-6） Lights out
“1”：MATRIX LED（LED1-6） Lighting, SLOPE and SCROLL sequence start

Address 31H < Matrix data clear >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31H	W	-	-	-	-	-	-	CLRB	CLRA
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：CLRA Reset A-pattern register
“0”：A-pattern register is not reset and writable（initial value）
“1”：A-pattern register is reset

Bit 0：CLRB Reset B-pattern register
“0”：B-pattern register is not reset and writable（initial value）
“1”：B-pattern register is reset

*CLRA and CLRB register return to 0 automatically.

Address 7FH < Register map change >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7FH	W	-	-	-	-	-	IAB	OAB	RMCG
Initial value	00H	0	0	0	0	0	0	0	0

Bit 0：RMCG Change register map
“0”：Control register is selected（initial value）
“1”：A-pattern register or B-pattern register is selected

Bit 1：OAB Select register to output for matrix
“0”：A-pattern register is selected（initial value）
“1”：B-pattern register is selected

Bit 2：IAB Select register to write matrix data
“0”：A-pattern register is selected（initial value）
“1”：B-pattern register is selected

Address 01H-1EH < A-pattern register data >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01-1EH	W	SCYCAXX [1:0]		SDLYAXX [1:0]		ILEDAXXSET [3:0]			
Initial value	08H	0	0	0	0	1	0	0	0

Bit 3-0：ILEDAXXSET[3:0] LED output current setting for A-pattern matrix data

“0000”： 0.00mA	“1000”：10.67mA（initial value）
“0001”： 1.33mA	“1001”：12.00mA
“0010”： 2.67mA	“1010”：13.33mA
“0011”： 4.00mA	“1011”：14.67mA
“0100”： 5.33mA	“1100”：16.00mA
“0101”： 6.67mA	“1101”：17.33mA
“0110”： 8.00mA	“1110”：18.67mA
“0111”： 9.33mA	“1111”：20.00mA

*ISET=100kΩ

Bit 5-4：SDLYAXX[1:0] SLOPE delay setting for A-pattern matrix

SDLYAXX[1:0]	SLP[1:0]		
	“00” or “11”	“01”	“10”
“00” （initial value）	No delay	No delay	No delay
“01”	1/4 x(slope cycle time)	1/2 x(slope cycle time)	1/2 x(slope cycle time)
“10”	1/2 x(slope cycle time)	2/2 x(slope cycle time)	2/2 x(slope cycle time)
“11”	3/4 x(slope cycle time)	3/2 x(slope cycle time)	3/2 x(slope cycle time)

Bit 7-6：SCYCAXX[1:0] SLOPE cycle time setting for A-pattern matrix

SCYCAXX[1:0]	SLP[1:0]		
	“00” or “11”	“01”	“10”
“00” （initial value）	No SLOPE control	No SLOPE control	No SLOPE control
“01”	(slope cycle time)= 1sec	(slope cycle time)=0.5sec	(slope cycle time)=1sec
“10”	(slope cycle time)= 2sec	(slope cycle time)=1sec	(slope cycle time)=2sec
“11”	(slope cycle time)= 3sec	(slope cycle time)= 1.5sec	(slope cycle time)=3sec

* The “XX” shows the matrix number from “00” to “54”. Please refer 5x6 LED Matrix coordinate.
*Setting time is based on OSC frequency, and the above-mentioned shows the value under Typ (1.2MHz).
*Setting time changes on CLKIO terminal input frequency at the external clock operation.

Example)
CLKIO input frequency=1.2MHz→"01": Slope cycle =1[s] (it is the same as the above)
CLKIO input frequency=2.4MHz→"01": Slope cycle =0.5[s]
CLKIO input frequency= 0.6MHz→"01”: Slope cycle =2[s]

* In a SPI interface, the interval to the following access has regulation after this address access. For details, please refer to the clause of the chapter of serial interface, and the electrical property of a SPI format.

Address 01H-1EH < B-pattern register data >

Address (Index)	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01-1EH	W	SCYCBXX [1:0]		SDLYBXX [1:0]		ILEDBXXSET [3:0]			
Initial value	08H	0	0	0	0	1	0	0	0

Bit 3-0：ILEDBXXSET[3:0] LED output current setting for B-pattern matrix data

“0000”： 0.00mA	“1000”：10.67mA（initial value）
“0001”： 1.33mA	“1001”：12.00mA
“0010”： 2.67mA	“1010”：13.33mA
“0011”： 4.00mA	“1011”：14.67mA
“0100”： 5.33mA	“1100”：16.00mA
“0101”： 6.67mA	“1101”：17.33mA
“0110”： 8.00mA	“1110”：18.67mA
“0111”： 9.33mA	“1111”：20.00mA

*ISET=100kΩ

Bit 5-4：SDLYBXX[1:0] SLOPE delay setting for B-pattern matrix

SDLYBXX[1:0]	SLP[1:0]		
	“00” or “11”	“01”	“10”
“00” （initial value）	No delay	No delay	No delay
“01”	1/4 x(slope cycle time)	1/2 x(slope cycle time)	1/2 x(slope cycle time)
“10”	1/2 x(slope cycle time)	2/2 x(slope cycle time)	2/2 x(slope cycle time)
“11”	3/4 x(slope cycle time)	3/2 x(slope cycle time)	3/2 x(slope cycle time)

Bit 7-6：SCYCBXX[1:0] SLOPE cycle time setting for B-pattern matrix

SCYCBXX[1:0]	SLP[1:0]		
	“00” or “11”	“01”	“10”
“00” （initial value）	No SLOPE control	No SLOPE control	No SLOPE control
“01”	(slope cycle time)= 1sec	(slope cycle time)=0.5sec	(slope cycle time)=1sec
“10”	(slope cycle time)= 2sec	(slope cycle time)=1sec	(slope cycle time)=2sec
“11”	(slope cycle time)= 3sec	(slope cycle time)= 1.5sec	(slope cycle time)=3sec

* The “XX” shows the matrix number from “00” to “54”. Please refer 5x6 LED Matrix coordinate.
*Setting time is based on OSC frequency, and the above-mentioned shows the value under Typ (1.2MHz).
*Setting time changes on CLKIO terminal input frequency at the external clock operation.

Example)
CLKIO input frequency=1.2MHz→"01": Slope cycle =1[s] (it is the same as the above)
CLKIO input frequency=2.4MHz→"01": Slope cycle =0.5[s]
CLKIO input frequency= 0.6MHz→"01”: Slope cycle =2[s]

* In a SPI interface, the interval to the following access has regulation after this address access. For details, please refer to the clause of the chapter of serial interface, and the electrical property of a SPI format.

● Description of operation

1. LED Matrix

1-1. Lighting method of dot Matrix

It can control 5 x 6 Matrix.

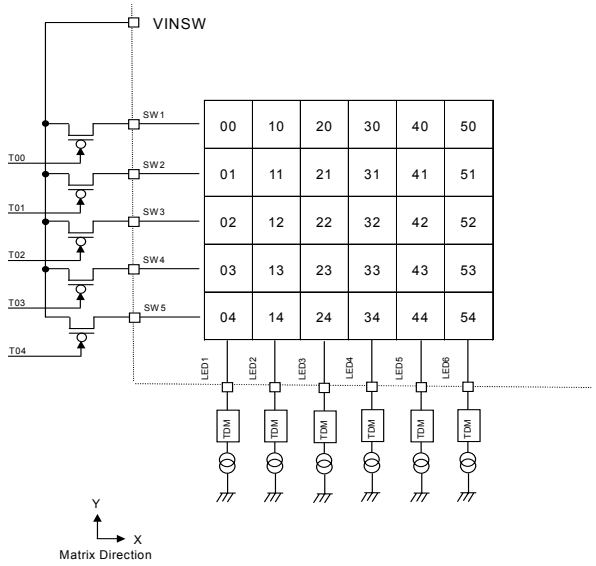


Fig.10 5x 6LED Matrix coordinate

The SW1 – SW5is turned on by serial. LED is driven one by one within the ON period.

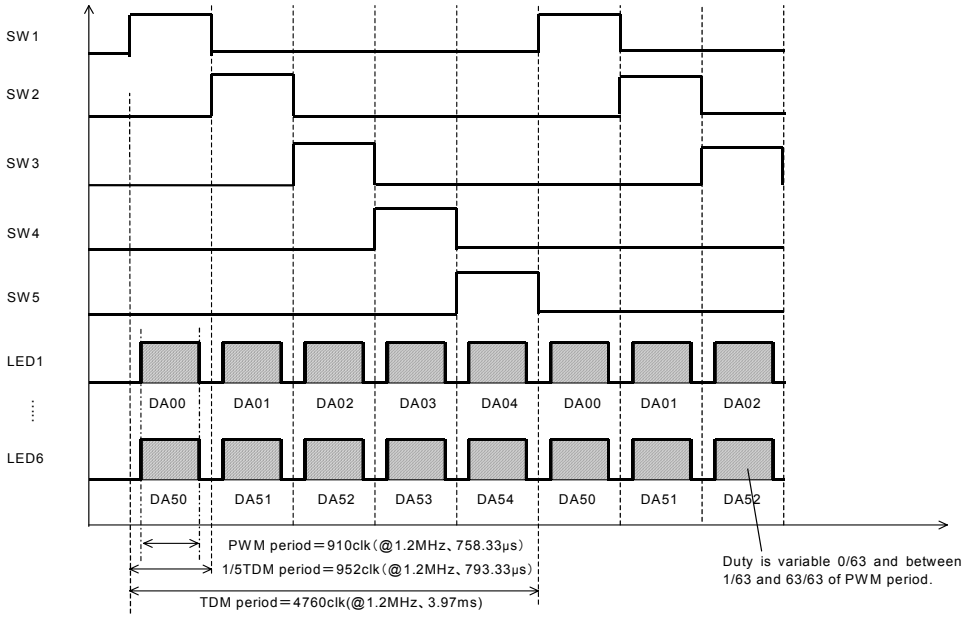


Fig.11 SW timing

1-2. LED lighting example

The firefly lighting example.

The following command set is the example of LED matrix firefly lighting.
It can control the turn on/off time in detail by SLOPE setting registers.

1) 7FH	00000000	Select control register
2) 21H	00000000	Select internal OSC for CLK
3) 01H	00001000	Start OSC
4) 11H	00111111	Set LED1-6 enable
5) 20H	00111111	Set Max Duty at Slope
6) 7FH	00000001	Select A-pattern or B-pattern register, Select A-pattern register to write matrix data
7) 01-1EH	xxxxxxxx	Write A-pattern data
8) 7FH	00000000	Select control register, Select A-pattern register to output for matrix
9) 2DH	00000010	Set SLOPE control enable
10) 30H	00000001	Start SLOPE sequence
11) 30H		00000000Lights out

2. LED Driver Current, SLOPE and SCROLL Sequence Control

2-1. LED driver current control

It can be controlled PWM Duty and DC current for LED driver current.

	Item	Control object	Control detail	Setting Registers	
				Name *	Bits
(A)	PWM Duty	Whole matrix	0/63～63/63 (64 step)	PWMSET	6
(B)	DC current	Each matrix dot	0～20mA (16 step) **	ILEDAXXSET ILEDBXXSET	4

* The “XX” shows the matrix number from “00” to “54”. Please refer 5x6 LED Matrix coordinate.
** ISET=100kΩ

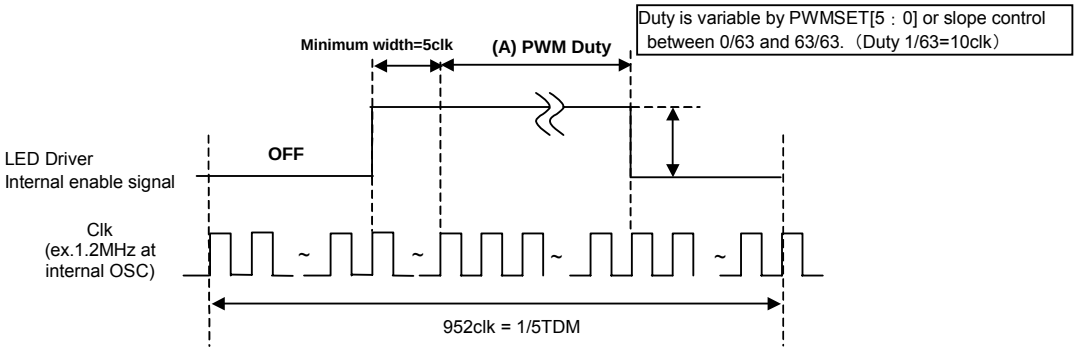


Fig.12 LED output current timing and PWM cycle

910clk of PWM period is set in the 1/5 TDM period (952clk).
PWM is operated 63 steps of 14clk. TDM period is 3.97ms (@1.2MHz).
Moreover, it has the starting waiting time of a constant current driver by 5clk(s).
PWM"H" time turns into ON time after waiting 28 clk.
(However, LED driver is set “OFF” compulsorily at PWM=0% setting.)

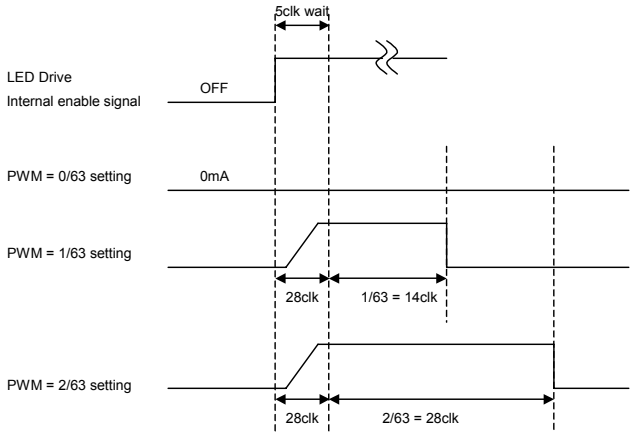


Fig.13 LED output current timing and a PWM cycle

2-2. SLOPE control

It can be controlled Delay and SLOPE cycle time for LED driver current.

	Item	Control object	Control detail	Setting Registers	
				Name *	Bits
(A)	Delay	Each matrix dot	0～3/4 x slope cycle time (4 step)	SDLYAXX SDLYBXX	2
(B)	SLOPE cycle time	Each matrix dot	0～3[s] (4 step)	SCYCAXX SCYCBXX	2
	SLOPE time	Whole matrix	0,1/4,2/4 x slope cycle time	SLP	2

* The “XX” shows the matrix number from “00” to “54”. Please refer 5x6 LED Matrix coordinate.

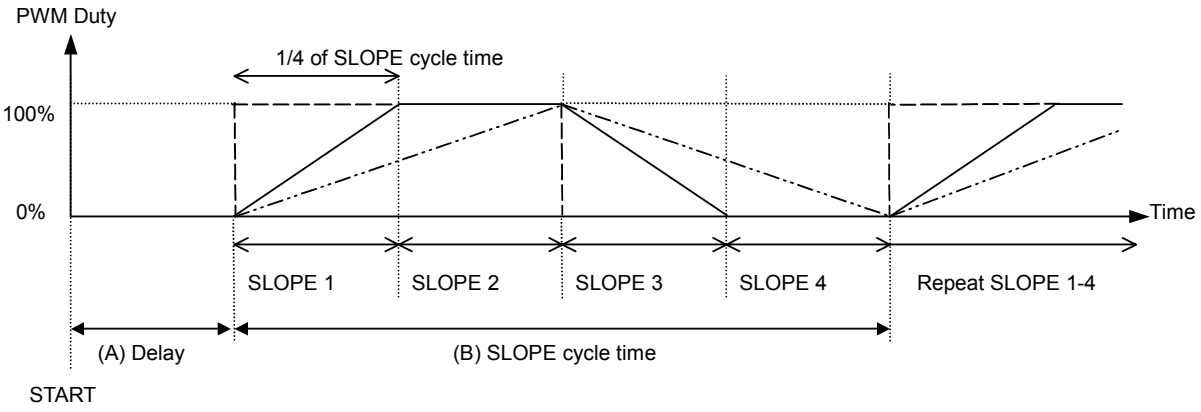
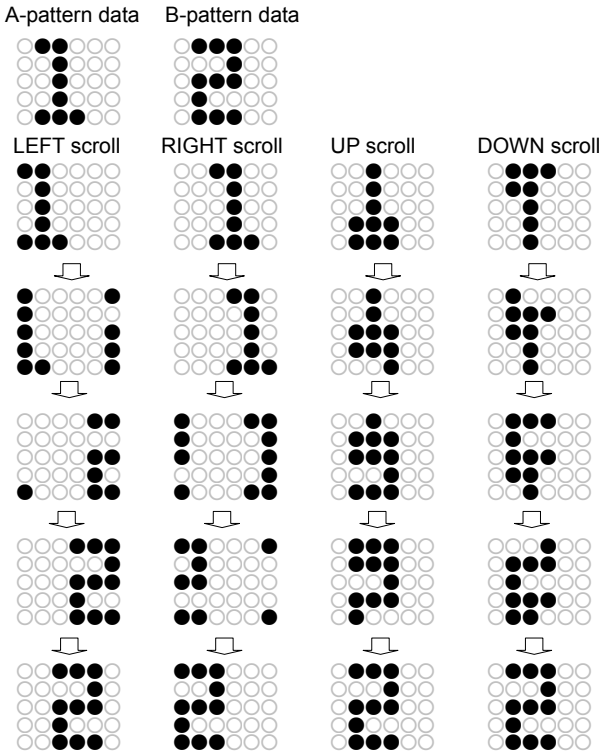


Fig.14 SLOPE operation

When SLPEN=”1” and PWMEN=SCLEN=”0”, SLOPE operation starts (like upper figure).
After “Delay” time start SLOPE by SLP register.

2-3. SCROLL control

2-3-1 Normal operation



2-4. Relation of PWM, SLOPE and SCROLL control

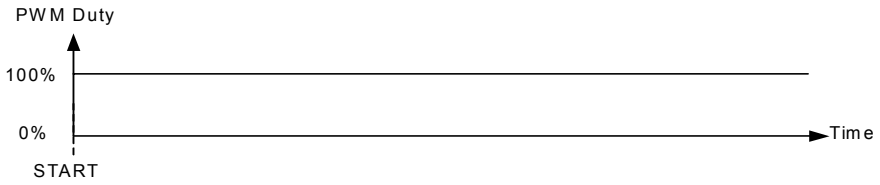
Register of condition and enable

	PWM	SLOPE	SCROLL
Condition	PWMSET [5:0]	SCYCXXX [1:0] SDLYXXX [1:0]	SCLSPEED [2:0] UP/DOWN/RIGHT/LEFT
Enable	PWMEN	SLPEN	SCLEN

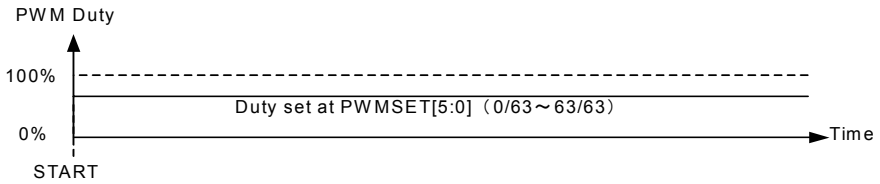
Combination of command

Operation	PWMEN	SLPEN	SCLEN
1	OFF	OFF	OFF
2	ON	OFF	OFF
3	OFF	ON	OFF
4	ON	ON	OFF
5	OFF	OFF	ON
Do not use this combination	ON	OFF	ON
	OFF	ON	ON
	ON	ON	ON

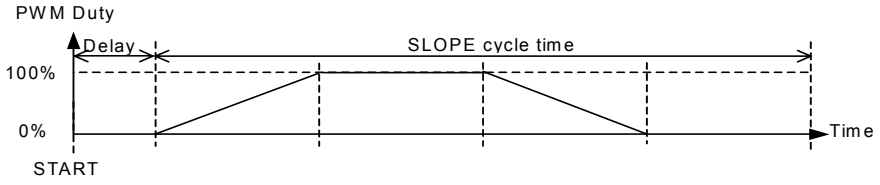
Operation 1



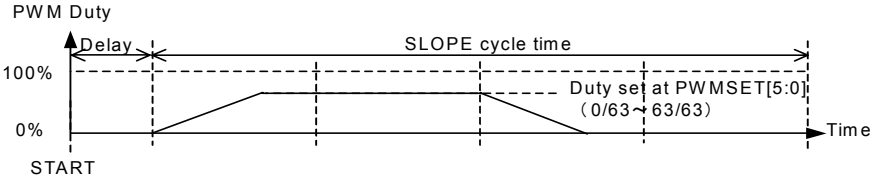
Operation 2



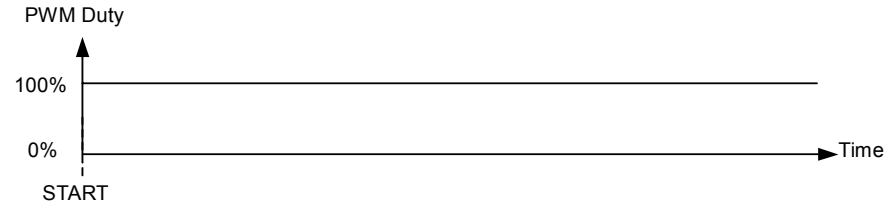
Operation 3



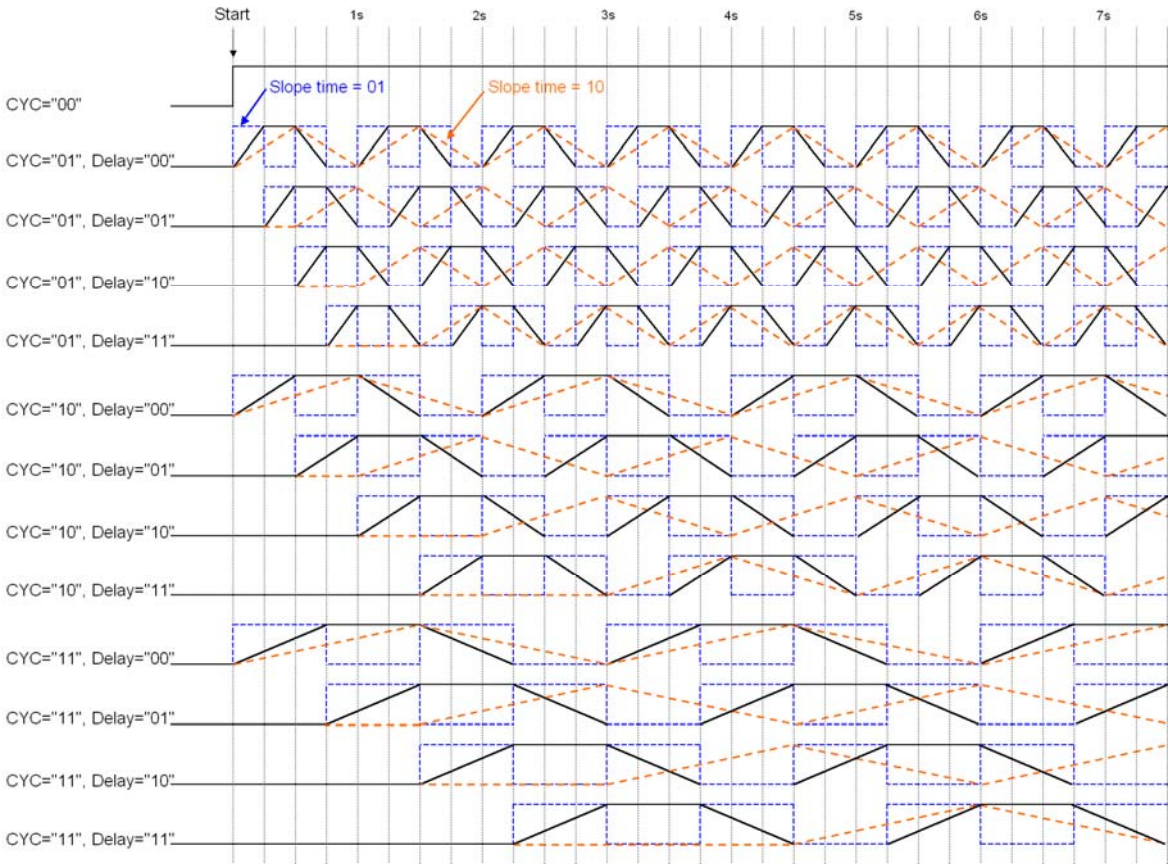
Operation 4



Operation 5



2-5. SLOPE control



Pattern can be set each dot.
Slope Time is common setting for whole matrix.
Orthodox auto pattarn can be make by combine pattarn.

3. Power up sequence

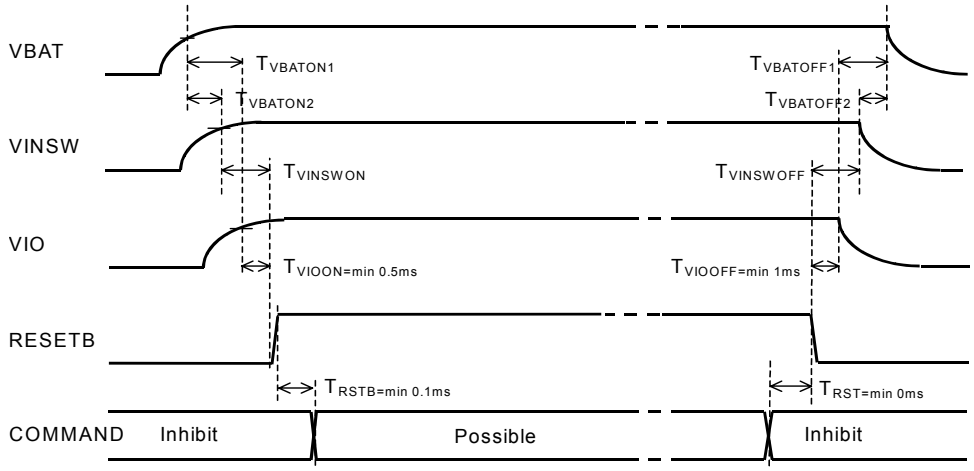


Fig.15 Power up sequence

Please take sufficient wait time for each Power/Control signal.

However, if VBAT<2.1V(typ) or On TSD, the command input is not effective because of the protection operation

4. Reset

There are two kinds of reset, software reset and hardware reset

(1) Software reset

- All the registers are initialized by SFTRST="1".
- SFTRST is an automatically returned to "0". (Auto Return 0).

(2) Hardware reset

- It shifts to hardware reset by changing RESETB pin “H” → “L”.
- The condition of all the registers under hardware reset pin is returned to the Initial Value, and it stops accepting all address.
  All LED driver turn off.
- It’s possible to release from a state of hardware reset by changing RESETB pin “L” → “H”.
  RESETB pin has delay circuit. It doesn’t recognize as hardware reset in "L" period under 5μs.

5. Thermal shutdown

A thermal shutdown function is effective at all blocks of those other than VREF.
Return to the state before detection automatically at the time of release.

6. UVLO Function (VBAT Voltage Low-Voltage Detection)

UVLO function is effective at all blocks of those other than VREF, and when detected, those blocks function is stopped.
Return to the state before detection automatically at the time of release.

7. I/O

When the RESETB pin is Low, the input buffers (SDA and SCL) are disabling for the Low consumption power.

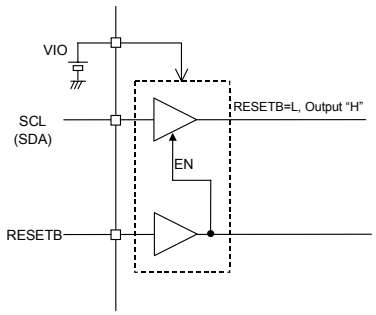


Fig.16 Input disabling by RESETB

8. Standard Clock Input and Output

It is possible to carry out synchronous operation of two or more ICs using the input-and-output function of a standard clock.

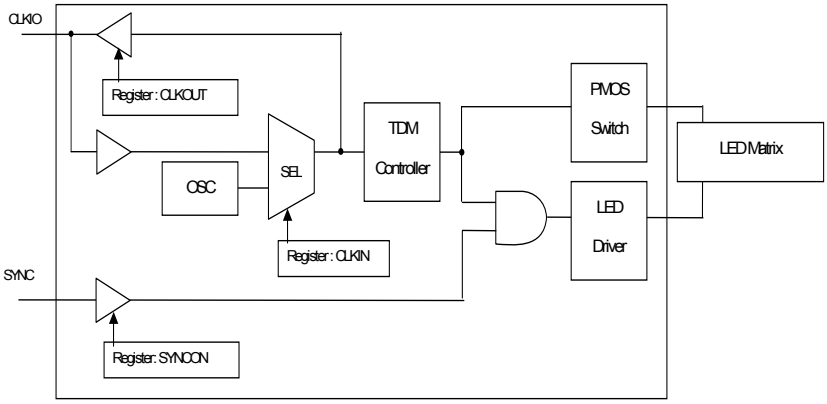


Fig.17 I/O part equivalent circuit diagram

・When a clock is supplied from the exterior

Inputting an external standard clock from CLKIO and setting register CLKIN=1,IC operates with the clock inputted from CLKIO as a standard clock.

・When the built-in oscillation circuit of one IC is used

When a clock cannot be supplied from the exterior, it is possible to synchronize between ICs by the connection as the following figure.

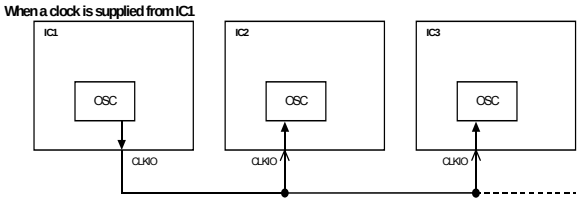


Fig.18 It is an example of application for the usage of two or more.

9. External ON/OFF Synchronization (SYNC Terminal)

Lighting of LED that synchronized with the external signal is possible.
By setting H/L of SYNC terminal, LED drivers output is set ON/OFF.
It's asynchronous operation with the internal TDM control.

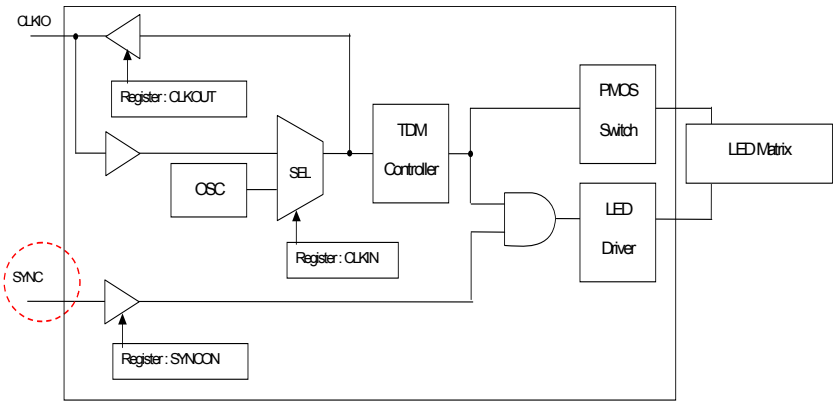


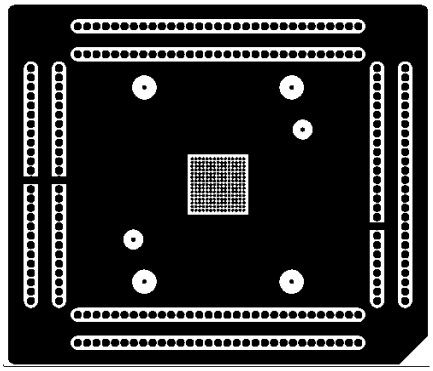
Fig.19 I/O part equivalent circuit diagram

10. About terminal processing of the function which is not used

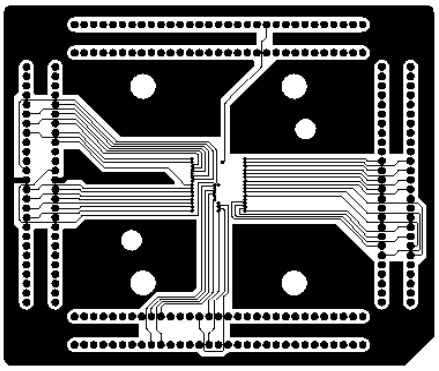
Please set up a test terminal and the unused terminal as the following table.
Especially, if an input terminal is not fixed, it may occur the unstable state of a device and the unexpected internal current.

Terminal name	Processing	Reason
SYNC	GND Short	The input terminal
CLKIO	Open	Initial valus is the input terminal
TEST1	GND Short	The input terminal for a test
TESTO	Open	The output terminal for a test
LED Terminal	GND Short	In order to avoid an unfixed state. (A register setup in connection with LED terminal that is not used is forbidden.)
SW Terminal	VINSW Short	In order to avoid an unfixed state. (A register setup in connection with SW terminal that is not used is forbidden.)

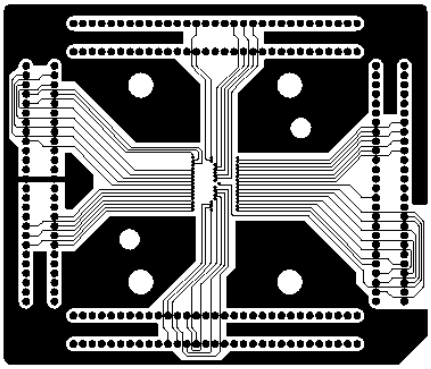
●PCB pattern of the Power dissipation measuring board



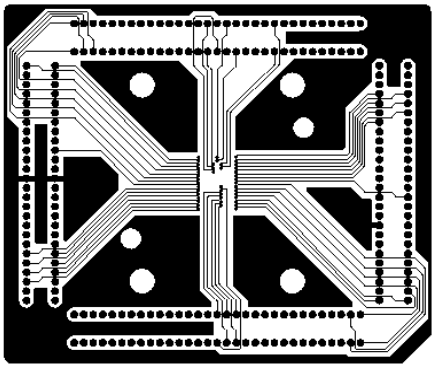
1st layer(component)



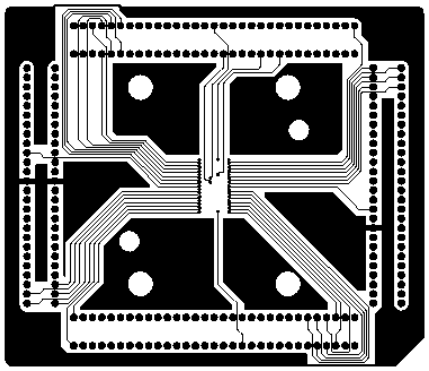
2nd layer



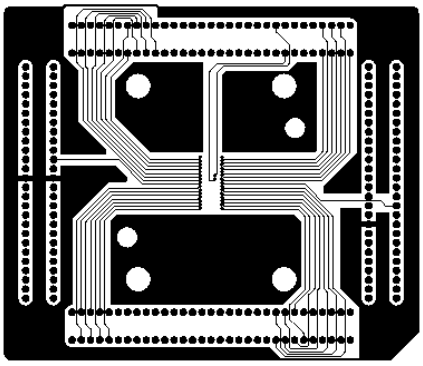
3rd layer



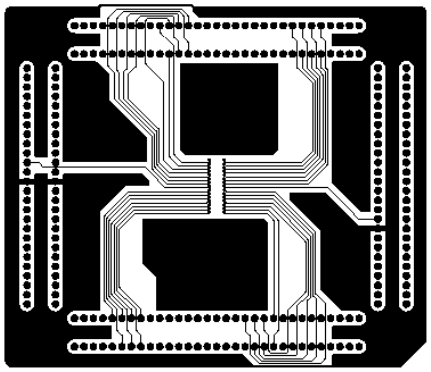
4th layer



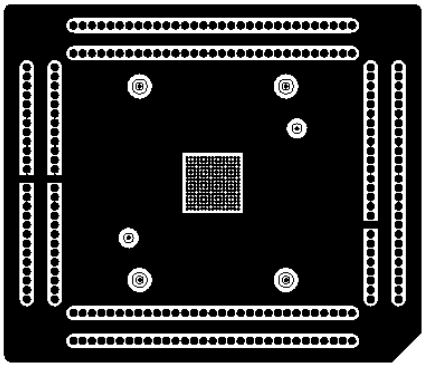
5th layer



6th layer



7th layer



8th layer(solder)

● Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and ground line

Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) Ground voltage

Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

(4) Short circuit between pins and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input pins

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) About the pin for the test, the un-use pin

Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

(11) About the rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of wiring.

(12) About the function description or application note or more.

The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements.

(13) SW1-5 don’t have short protection. When need protection, please use fuse element.

● Document History

Ver	Date	Contents
0.1	2010/7/28	Draft
0.11	2010/8/9	P1,9 LED Driver Max Current 30mA → 42.5mA P9 Add Condition for “Driver pin voltage range”
0.12	2010/10/1	P2 VIOMAX = 4.5V → 7V P27 Fig.11 TDM Period modify P14,23 SCLSPEED[3:0] → SCLSPEED[2:0] Add SCLSPEEDUP P14,21 Add CLKSEL[1:0]
0.13	2010/10/28	P5,7 Add Ball No. P22 Add comment for SLP[1:0]
0.14	‘10/11/11	P23 Change Scroll Speed at SCLSPEEDUP=1 Add comment for SCLSPEED[2:0] and SCLSPEEDUP P27,29 Change timing for TDM、PWM P34 Change command input timing
0.15	‘10/11/17	P25,33 Change Slope timing
0.16	‘10/12/02	P38 Add comment on “● Cautions on use”
0.17	‘10/12/14	P6 Add the package outline
0.18	‘11/01/05	P21 Add CLKIN information P26 Change < B-pattern register data >
0.19	‘11/01/18	P1 Remove “Continuous (TDM off) lighting function for LED1-LED6” in functions. ---- Remove “Block Diagram / Application Circuit example 2” P13 Remove “Address=17” ---- Remove “Explanation page for Address=17” P28 Remove “Explanation for TDM off”