IITB-CPU

EE 224 Course Project

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Implementations

We have implemented IITB-CPU in the following two ways:

Using Sub States	One-State-One-Clock Cycle
One state is executed in multiple clock cycles.	One state is executed in one clock cycle.
No Transients. Signals do not have incorrect/ unexpected values at any instant.	May have Transients. Signals can be incorrect for an infinitesimal time period but get corrected soon after.
Has ~2 substates for every state and takes ~2 clock cycles to complete one state.	Has no substates, just on state that is completed in one clock cycle.
Appears to be more reliable for FPGA implementation since has no transients.	Possibility of incorrect results for FPGA implementation.

How to test the code?

- Compile the project.
- Run RTL Simulation
- After ModelSim launches, paste the contents of CLI.txt(different for each implementation) into the command line.

Test sheet

There are sheets in Instructions.xlsx
In both sheets, we have initialised the memory as well as explained what change each instruction will do.

We have made a video to show our RTL Simulation. You can find it here :
https://drive.google.com/file/d/1XLHvWSPj6krHIl7TCshj_E2tJiAgJ9z5/view?usp=sharing

Some Errors we encountered (and solved) while designing and implementing IITB-CPU

- Tried using if generate but realised it doesn't work for connections, so used Muxes (later failed due to structural +behavioural)
- We were getting loops as we combined structural and behavioural code together and there was feedback in the circuit. This was a failure and we redesigned our main program flow using process.
- Delays in ALU due to signal which we converted to variable
- Added Init state to allow initial transition without which the FSM wasn't triggering.
- Delays in datapath (including Control Signals not changing,etc. in mem and RF) due to signals hence had to make substates so that signal settles. Counter issue – solved by changing sensitivity list of the process appropriately.