EE 224 Course Project : CPU

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State Descriptions

S_0 (Fetching instruction from memory)

Data Transfer	Commands
PC $\rightarrow$ M_add	MDR
M_data $\rightarrow$ T1	T1_E

S_1 (Updating PC)

Data Transfer	Commands
PC $\rightarrow$ ALU_A	PC_E
+1 $\rightarrow$ ALU_B	ALU_J
ALU_CND $\leftarrow$ 11	
ALU_S $\rightarrow$ PC	

S_2 (Reading operands)

Data Transfer	Commands
$T1_{11-9} \rightarrow$ RF_A1	T2_E
$T1_{8-6} \rightarrow$ RF_A2	T3_E
RF_D1 $\rightarrow$ T2	
RF_D2 $\rightarrow$ T3	

S_3 **(Execution)**

Data Transfer	Commands
T2 $\rightarrow$ ALU_A	T2_E
T3 $\rightarrow$ ALU_B	ALU_J
$T1_{1-0} \rightarrow$ ALU_CND	
ALU_S $\rightarrow$ T2	
ALU_C $\rightarrow$ FC	
ALU_Z $\rightarrow$ FZ	

S_4 **(Storing the output)**

Data Transfer	Commands
T2 $\rightarrow$ RF_D3	RF_WE
$T1_{5-3} \rightarrow$ RF_A3	

S_5 **(Reading operands (for ADI))**

Data Transfer	Commands
$T1_{11-9} \rightarrow$ RF_A1	T2_E
RF_D1 $\rightarrow$ T2	T3_E
$T1_{5-0} \rightarrow$ SE_6 $\rightarrow$ T3	

S_6 **(Checking whether the two operands are equal, and storing zero flag into T2 (without changing FZ))**

Data Transfer	Commands
T2 $\rightarrow$ ALU_A	ALU_J
T3 $\rightarrow$ ALU_B	T2_E
ALU_C $\rightarrow$ SE_2 $\rightarrow$ T2	
ALU_CND $\leftarrow$ 00	

S_7 **(Updating PC if BEQ)**

Data Transfer	Commands
PC $\rightarrow$ ALU_A	ALU_J
$T1 \rightarrow$ SE_10 $\rightarrow$ ALU_B	PC_E
ALU_CND $\leftarrow$ 11	
if($T2_0 == 0$) then ALU_C $\rightarrow$ PC	
else PC $\rightarrow$ PC	

S_8 **(Storing PC into REG_A)**

Data Transfer	Commands
$T1_{11-9} \rightarrow$ RF_A3	RF_WE
PC $\rightarrow$ RF_D3	

S_9 **(Branching PC to the address PC + immediate)**

Data Transfer	Commands
PC $\rightarrow$ ALU_A $T1_{8-0} \rightarrow$ SE_9 $\rightarrow$ ALU_B ALU_CND $\leftarrow$ 11 ALU_S $\rightarrow$ PC	ALU_J

S_{10} **(Branching PC to the address in REG_B)**

Data Transfer	Commands
$T1_{8-6} \rightarrow$ RF_A1 RF_D1 $\rightarrow$ PC	PC_E

S_{11} **(Executing Load Higher Immediate)**

Data Transfer	Commands
$T1_{11-9} \rightarrow$ RF_A3 $T1_{11-9} \rightarrow$ PZ_7 $\rightarrow$ RF_D3	RF_WE

S_{12} **(Executing Load Higher Immediate)**

Data Transfer	Commands
$T1_{11-9} \rightarrow$ RF_A3 $T1_{11-9} \rightarrow$ PZ_7 $\rightarrow$ RF_D3	RF_WE

S_{14} **(Computing address of the memory destination)**

Data Transfer	Commands
T3 $\rightarrow$ ALU_A $T1_{5-0} \rightarrow$ SE_16 $\rightarrow$ ALU_B ALU_C $\rightarrow$ T3	ALU_CND T3_E

S_{15} **(Writing to the memory)**

Data Transfer	Commands
T3 $\rightarrow$ M_add T2 $\rightarrow$ M_data	MWR

S_{16} **(Computing address of the memory destination)**

Data Transfer	Commands
T3 $\rightarrow$ ALU_A $T1_{5-0} \rightarrow$ SE_16 $\rightarrow$ ALU_B ALU_C $\rightarrow$ T3	ALU_CND T3_E ALU_CND

S_{17} **(Reading from memory)**

Data Transfer	Commands
T3 → M_add	MDR
T2 → M_data	T2_E

S_{18} **(Writing to the register)**

Data Transfer	Commands
$T1_{11-9}$ → RF_A3	RF_WE
T2 → RF_D3	

S_{19} **(Initial step of SM)**

Data Transfer	Commands
(0000000000000000) → T2	T2_WE
$T1_{11-9}$ → RF_A2	T3_E
RF_D2 → T3	

S_{20} **(Looping step 1 of SM)**

Data Transfer	Commands
counter := int($T2_{2-0}$)	MWR
if($T1_{counter}$==1) then T3 →	
RF_D1 → M_data	
$T2_{2-0}$ → RF_A1	

S_{21} **(Looping step 2 of SM)**

Data Transfer	Commands
T3 → ALU_A	T3_E
1 → ALU_B	ADD
if($T1_{counter}$==1) then ALU_C → T3	

S_{22} **(Looping step 3 of SM)**

Data Transfer	Commands
T2 → ALU_A	ADD
1 → ALU_B	T2_E
ALU_C → T2	

S_{23} **(Initial step of LM)**

Data Transfer	Commands
(0000000000000000) → T2	T2_WE
$T1_{11-9}$ → RF_A2	T3_E
RF_D3 → T3	

S_{24} **(Looping step 1 of LM)**

Data Transfer	Commands
counter := int($T2_{2-0}$)	MDR
$T1_{counter}$ → RF_WR	MDR
T3 → M_add	
M_data → RF_D3	
$T2_{2-0}$ → RF_A3	

S_{25} **(Looping step 2 of LM)**

Data Transfer	Commands
T3 → ALU_A	T3_E
1 → ALU_B	ADD
if($T1_{counter}$==1) then ALU_C → T3	

S_{26} **(Looping step 3 of LM)**

Data Transfer	Commands
T2 → ALU_A	ADD
1 → ALU_B	T2_E
ALU_C → T2	

Instructions with their State Diagrams and Control Signals

Instruction	State flow	Control
ADD	$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$	
ADC	$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$	
ADZ	$S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$	
ADI	$S_0 \rightarrow S_1 \rightarrow S_5 \rightarrow S_3 \rightarrow S_4$	