# EE 224 Course Project : CPU

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## State Descriptions

### $S_0$ (Fetching instruction from memory)

| Data Transfer | Commands |
|---|---|
| PC $\rightarrow$ M_add | MDR |
| M_data $\rightarrow$ T1 | T1_E |

### $S_1$ (Updating PC)

| Data Transfer | Commands |
|---|---|
| PC $\rightarrow$ ALU_A | PC_E |
| $+1 \rightarrow$ ALU_B | ALU_J $\leftarrow 00$ |
| ALU_CND $\leftarrow 11$ | |
| ALU_S $\rightarrow$ PC | |

### $S_2$ (Reading operands)

| Data Transfer | Commands |
|---|---|
| $T1_{11-9} \rightarrow$ RF_A1 | T2_E |
| $T1_{8-6} \rightarrow$ RF_A2 | T3_E |
| RF_D1 $\rightarrow$ T2 | |
| RF_D2 $\rightarrow$ T3 | |

$S_3$ **(Execution)**

| Data Transfer | Commands |
|---|---|
| T2 $\rightarrow$ ALU_A | T2_E |
| T3 $\rightarrow$ ALU_B | ALU_J $\leftarrow T1_{14-13}$ |
| $T1_{1-0} \rightarrow$ ALU_CND | |
| ALU_S $\rightarrow$ T2 | |
| ALU_C $\rightarrow$ FC | |
| ALU_Z $\rightarrow$ FZ | |

$S_4$ **(Storing the output)**

| Data Transfer | Commands |
|---|---|
| T2 $\rightarrow$ RF_D3 | RF_WR |
| $T1_{5-3} \rightarrow$ RF_A3 | |

$S_5$ **(Reading operands (for ADI))**

| Data Transfer | Commands |
|---|---|
| $T1_{11-9} \rightarrow$ RF_A1 | T2_E |
| RF_D1 $\rightarrow$ T2 | T3_E |
| $T1_{5-0} \rightarrow$ SE_6 $\rightarrow$ T3 | |

$S_6$ **(Checking whether the two operands are equal, and storing zero flag into T2 (without changing FZ))**

| Data Transfer | Commands |
|---|---|
| T2 $\rightarrow$ ALU_A | ALU_J $\leftarrow$ 11 |
| T3 $\rightarrow$ ALU_B | T2_E |
| ALU_Z $\rightarrow$ SE_1 $\rightarrow$ T2 | |
| ALU_C $\rightarrow$ FC | |
| ALU_CND $\leftarrow$ 00 | |

$S_7$ **(Updating PC if BEQ)**

| Data Transfer | Commands |
|---|---|
| PC $\rightarrow$ ALU_A | ALU_J $\leftarrow$ 00 |
| if($T2_0 == 0$) then +1 $\rightarrow$ ALU_B | PC_E |
| else $T1 \rightarrow$ SE_10 $\rightarrow$ ALU_B | |
| ALU_CND $\leftarrow$ 11 | |
| ALU_S $\rightarrow$ PC | |

$S_8$ **(Storing PC into REG_A)**

| Data Transfer | Commands |
|---|---|
| $T1_{11-9} \rightarrow$ RF_A3 | RF_WR |
| PC $\rightarrow$ RF_D3 | |

$S_9$ **(Branching PC to the address PC + immediate)**

| Data Transfer | Commands |
|---|---|
| PC $\rightarrow$ ALU_A | ALU_J |
| $T1_{8-0} \rightarrow$ SE_9 $\rightarrow$ ALU_B | |
| ALU_CND $\leftarrow$ 11 | |
| ALU_S $\rightarrow$ PC | |

$S_{10}$ **(Branching PC to the address in REG_B)**

| Data Transfer | Commands |
|---|---|
| $T1_{8-6} \rightarrow$ RF_A1 | PC_E |
| RF_D1 $\rightarrow$ PC | |

$S_{11}$ **(Executing Load Higher Immediate)**

| Data Transfer | Commands |
|---|---|
| $T1_{11-9} \rightarrow$ RF_A3 | RF_WR |
| $T1_{11-9} \rightarrow$ PZ_7 $\rightarrow$ RF_D3 | |

$S_{12}$ **(Computing address of the memory destination)**

| Data Transfer | Commands |
|---|---|
| T3 $\rightarrow$ ALU_A | ALU_J $\leftarrow$ 00 |
| $T1_{5-0} \rightarrow$ SE_16 $\rightarrow$ ALU_B | T3_E |
| ALU_S $\rightarrow$ T3 | |

$S_{13}$ **(Writing to the memory)**

| Data Transfer | Commands |
|---|---|
| T3 $\rightarrow$ M_add | MWR |
| T2 $\rightarrow$ M_data | |

$S_{14}$ **(Reading from memory)**

| Data Transfer | Commands |
|---|---|
| T3 $\rightarrow$ M_add | MDR |
| M_data $\rightarrow$ T2 | T2_E |

$S_{15}$ **(Writing to the register)**

| Data Transfer | Commands |
|---|---|
| $T1_{11-9} \rightarrow$ RF_A3 | RF_WR |
| T2 $\rightarrow$ RF_D3 | |

$S_{16}$ **(Initial step of SM)**

| Data Transfer | Commands |
|---|---|
| (0000000000000000) $\rightarrow$ T2 | T2_E |
| $T1_{11-9} \rightarrow$ RF_A2 | T3_E |
| RF_D2 $\rightarrow$ T3 | |

$S_{17}$ **(Looping step 1 of SM)**

| Data Transfer | Commands |
|---|---|
| counter := int($T2_{2-0}$) | MWR |
| T3 $\rightarrow$ ALU_A | T3_E |
| 1 $\rightarrow$ ALU_B | ALU_J $\leftarrow$ 00 |
| if($T1_{counter}$==1) then | |
| {T3 $\rightarrow$ M_add | |
| $T2_{2-0} \rightarrow$ RF_A1 | |
| RF_D1 $\rightarrow$ M_data | |
| ALU_S $\rightarrow$ T3 } | |

$S_{19}$ **(Looping step 3 of SM)**

| Data Transfer | Commands |
|---|---|
| T2 $\rightarrow$ ALU_A | ALU_J $\leftarrow$ 00 |
| 1 $\rightarrow$ ALU_B | T2_E |
| ALU_C $\rightarrow$ T2 | |

$S_{20}$ **(Initial step of LM)**

| Data Transfer | Commands |
|---|---|
| (0000000000000000) $\rightarrow$ T2 | T2_E |
| $T1_{11-9} \rightarrow$ RF_A2 | T3_E |
| RF_D3 $\rightarrow$ T3 | |

### $S_{21}$ (Looping step 1 of LM)

| Data Transfer | Commands |
|---|---|
| counter := int($T2_{2-0}$) | MDR |
| $T1_{counter}$ → RF_WR | |
| T3 → M_ALU_J ← 00 | |
| M_data → RF_D3 | |
| $T2_{2-0}$ → RF_A3 | |

### $S_{22}$ (Looping step 2 of LM)

| Data Transfer | Commands |
|---|---|
| T3 → ALU_A | T3_E |
| 1 → ALU_B | ALU_J ← 00 |
| if($T1_{counter}$==1) then ALU_C → T3 | |

### $S_{23}$ (Looping step 3 of LM)

| Data Transfer | Commands |
|---|---|
| T2 → ALU_A | ALU_J ← 00 |
| 1 → ALU_B | T2_E |
| ALU_C → T2 | |

## Instructions with their State Diagrams and Control Signals

| Instruction | State flow |
|---|---|
| ADD | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$ |
| ADC | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$ |
| ADZ | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$ |
| ADI | $S_0 \rightarrow S_1 \rightarrow S_5 \rightarrow S_3 \rightarrow S_4$ |
| NDU | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$ |
| NDC | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$ |
| NDZ | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4$ |
| LHI | $S_0 \rightarrow S_1 \rightarrow S_{11}$ |
| LW | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{13} \rightarrow S_{15} \rightarrow S_{16}$ |
| SW | $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_{13} \rightarrow S_{14}$ |
| SM | $S_0 \rightarrow S_1 \rightarrow S_{16} \rightarrow S_{17} \rightarrow S_{18} \rightarrow S_{19}$ |
| LM | $S_0 \rightarrow S_1 \rightarrow S_{20} \rightarrow S_{21} \rightarrow S_{22} \rightarrow S_{23}$ |
| BEQ | $S_0 \rightarrow S_2 \rightarrow S_6 \rightarrow S_7 \rightarrow S_{23}$ |
| JAL | $S_0 \rightarrow S_8 \rightarrow S_9$ |
| JLR | $S_0 \rightarrow S_8 \rightarrow S_{10}$ |