IITB-CPU

EE 224 Course Project

Atharva Kulkarni(210070047)

Harshit Raj(20d070033)

Shreyas Grampurohit(21d070029)

Varad Deshpande(21d070024)

Implementations

We have implemented IITB-CPU in the following two ways:

Using Sub States	One-State-One-Clock Cycle
One state is executed in multiple clock cycles.	One state is executed in one clock cycle.
No Transients. Signals do not have incorrect/ unexpected values at any instant.	May have Transients. Signals can be incorrect for an infinitesimal time period but get corrected soon after.
Has ~2 substates for every state and takes ~2 clock cycles to complete one state.	Has no substates, just on state that is completed in one clock cycle.
Appears to be more reliable for FPGA implementation since has no transients.	Possibility of incorrect results for FPGA implementation.

How to test the code?

- Compile the project.
- Run RTL Simulation
- After ModelSim launches, paste the contents of CLI.txt(different for each implementation) into the command line.

Test sheet

There are sheets in Instructions.xlsx
In both sheets, we have initialised the memory as well as explained what change each instruction will do.

We have made a video to show our RTL Simulation. You can find it here :
https://drive.google.com/file/d/1XLHvWSPj6krHIl7TCshj_E2tJiAgJ9z5/view?usp=sharing