EE214 - Digital Circuits Lab

Tone Generator

Experiment 10

Instructions:

1. Use **Behavioral** modeling for writing VHDL description
2. Perform Pin-Planning, run on Xenon board and demonstrate to your TA.
3. Submit the entire project files in .zip format in moodle.

Tone Generator [40 Marks]

In this experiment, you will generate the seven major notes in the Indian classical music named sa, re, ga, ma, pa, dha, ni and sa (upper octave). You will use the 8 slide switches on the Xenon Board to play these notes. The frequency for the above mentioned notes is to be generated using clock divider introduced in last week's experiment.

Table 1: Frequency Table

Note	Frequency(Hz)	Count Value
Sa	240	104168
Re	270	
Ga	300	
Ma	320	
Pa	360	
Dha	400	
Ni	450	
Sa (upper octave)	480	

- Fill up the **Count Value** column in Table 1. You need to calculate the count value for each note by taking the **master clock as 50 MHz** (Xenon's On-board clock). [5 Marks]
- **NOTE:** If the count value comes in fraction take the nearest integer value.
- Write the VHDL code for playing the notes Sa, Re, Ga, Ma, Pa, Dha, Ni, Sa(upper octave). [15 Marks]
- Map the **8 Slide Switches** of the Xenon board like the keys of a Piano/Keyboard for playing the notes. The note will play when corresponding slide switch gets ON.
- **Note:** Reset is not there for Tone Generator module.
- Corresponding to each note(slide switch on), an LED on Xenon board should be mapped to indicate the note being played. The **LED will glow when the respective slide switch is switched ON** (all 8 LEDs will be used, one for each note/slide switch).
- The GPIO pins of the Xenon Board can not drive a Speaker directly because of current limitation, therefore, use **SL100 Transistor to drive the Speaker**. The output you need to connect to the SL100 transistor taken from **Header 1 PIN 1** written on the board. The circuit schematic are illustrated in **figure(3)**.
- Sa (lower octave) need to be played when SW1 is ON, Re note should be played when SW2 and SW1 is ON, Ga played when SW3, SW2, SW1 is ON and so on for other notes.
- Take **supply voltages +3.3V and GND** for the speaker from **OLED VCC and GND** written on the board.

PIN Map for Xenon Board [10 Marks]

- **50 MHz Clock:** PIN 26
- **Slide Switch(S1-S8):** PIN (38,39,41,43,44,45,46,47)
- **LEDs (LED1-LED8):** PIN (50,52,54,56,57,58,59,60)
- **Music Output:** PIN 75 (Header 1 PIN 1)

Take **VCC (+3.3V):** from OLED VCC on board and take **GND (0V):** from OLED GND on board

Play the notes on Xenon board by assembling the circuit as per figure(3) on breadboard and show the output to your respective TA. [10 Marks]

Clock Source Frequency	FPGA Pin no.
1 Hz CLK	55
50 MHz CLK	26
Ext CLK	27
10 MHz CLK	29

Figure 1: Pin-mapping for on-board Clock Sources

Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Figure 2: Pin-mapping for on-board Switches and LED's

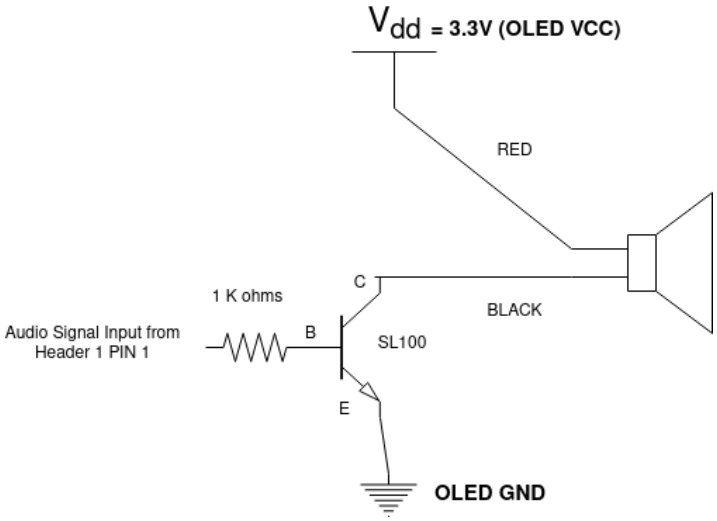

Figure 3: Speaker driver circuit

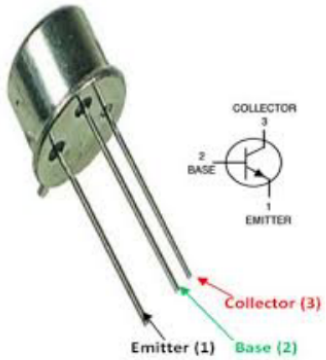

Figure 4: SL100 pinout