EE214 - Digital Circuits Lab

Universal Shifter

Friday Batch

02/09/2022

Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA.
3. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
4. Perform RTL simulation using the given testbench and tracefile.
5. Perform scan-chain evaluation on board using the given tracefile.
6. Demonstrate the RTL simulations and board scanchain output to your TA
7. Submit the entire project files in .zip format in Moodle.

Problem Statement:

1. **Design [5 Marks]**

   Design a universal shifter circuit, which can perform logical right shift or left shift on 8-bit input by the specified number of bits.

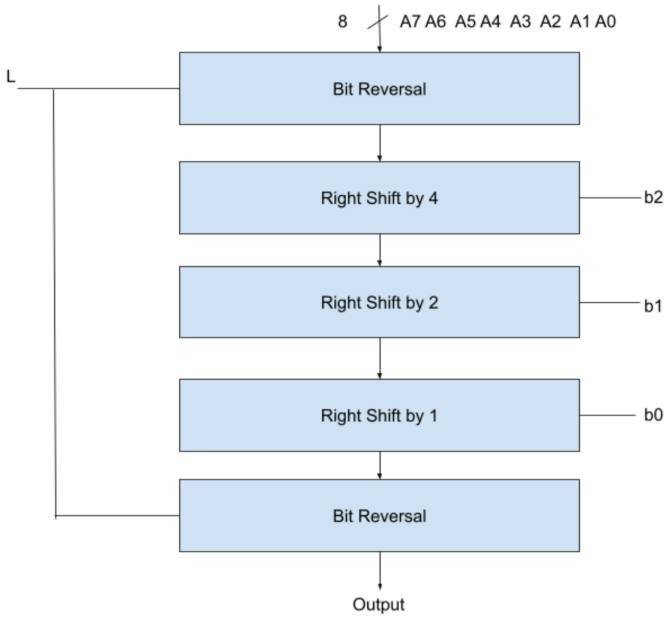

Figure 1: Block diagram

For L = 0, output will be right shifted version of input.
For L = 1, output will be left shifted version of input.

Figure(2) is the design of right shift by 4 block.

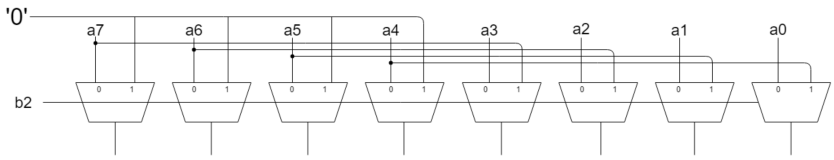

Figure 2: Right shift by 4 bits

The output of shift block in figure(2) will be a7 a6 a5 a4 a3 a2 a1 a0 for b2 = 0.
For b2 = 1 its output will be 0 0 0 0 a7 a6 a5 a4.

2. **VHDL description [5 Marks]**

   Describe your designed circuit in VHDL. Block in figure(2) can be described in VHDL as follows

```
n4_bit : for i in 0 to 7 generate
lsb: if i < 4 generate
b2: mux port map(I(0) => a(i), I(1) => a(i+4), S => b(2), Y => s(i));
end generate lsb;
msb: if i > 3 generate
b2: mux port map(I(0) => a(i), I(1) => '0', S => b(2), Y => s(i));
end generate msb;
end generate ;
```

   You need to design the mux used in the above code using logic gates from Gates.vhdl.
   Similarly you can describe Right shift by 2 bit/1 bit and Bit reversal block.

3. **Simulation [5 Marks]**
   Simulate your design using the generic testbench to confirm the correctness of your description.
   To do this, use the tracefile given below and modify the testbench given to you appropriately.

   Tracefile format: ($< L\ B2\ B1\ B0\ A7\ A6\ A5\ A4\ A3\ A2\ A1\ A0 >\ \ < S7\ S6\ S5\ S4\ S3\ S2\ S1\ S0 >\ \ \ 11111111$) Tracefile

4. **Scanchain [5 Marks]**
   Test the correctness of your design using scanchain