# EE214 - Digital Circuits Lab

## **BCD Number Subtraction**

Friday Batch

26/08/2022

#### **Instructions:**

- 1. For the design part do pen-paper design and get it verified by your TA.
- 2. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
- 3. Perform RTL simulation using the provided testbench and tracefile.
- 4. Demonstrate the simulations to your TA
- 5. For reference you can go through this link: BCD Addition and Subtraction
- 6. Perform the experiment on Xenon board and verify with your TA.
- 7. Submit the entire project files in .zip format in moodle.

#### **Problem Statement:**

1. Design a circuit on pen paper for subtraction of two BCD numbers (A-B) using 4 bit binary adder/subtractor and additional logic gates from Gates.vhdl. Input numbers are BCD(0 to 9) format only. The result is in BCD format. The MSB of the output is '1' if the final result is negative and MSB is '0' if the final result is positive. [5 Marks]

### Hint:

- (a) Use 4-bit binary subtractor to get the 10's complement of the subtrahend.
- (b) Use 4-bit binary adder to add A and the 10's complement of B.
- (c) Design a logic circuit to detect sum greater than 9.
- (d) Use 4-bit binary adder to add  $(0110)_2$  in the sum if sum is greater than 9 or carry is 1.
- (e) Use one 4-bit binary adder-subtractor and decide the inputs properly to get the output in desired BCD format.
  - i. If carry is generated, the obtained result is positive. Discard the carry to get the result.
  - ii. If carry is not generated, the obtained result is negative, find the 10's complement to get the final result.
- 2. Write a VHDL description for the same. [5 Marks]
- 3. Simulate the BCD Subtractor using the generic testbench and given tracefile to confirm the correctness of your design and show simulation results to your TA. [5 Marks]
- 4. Tracefile format:  $(< A3\ A2\ A1\ A0\ B3\ B2\ B1\ B0> < Y4\ Y3\ Y2\ Y1\ Y0> < 1\ 1\ 1\ 1>)$  Tracefile
- 5. Pin plan switches S8 to S1 as input and LEDs as output and show the correctness of the design on board to your TA. [5 Marks]