

1. Description

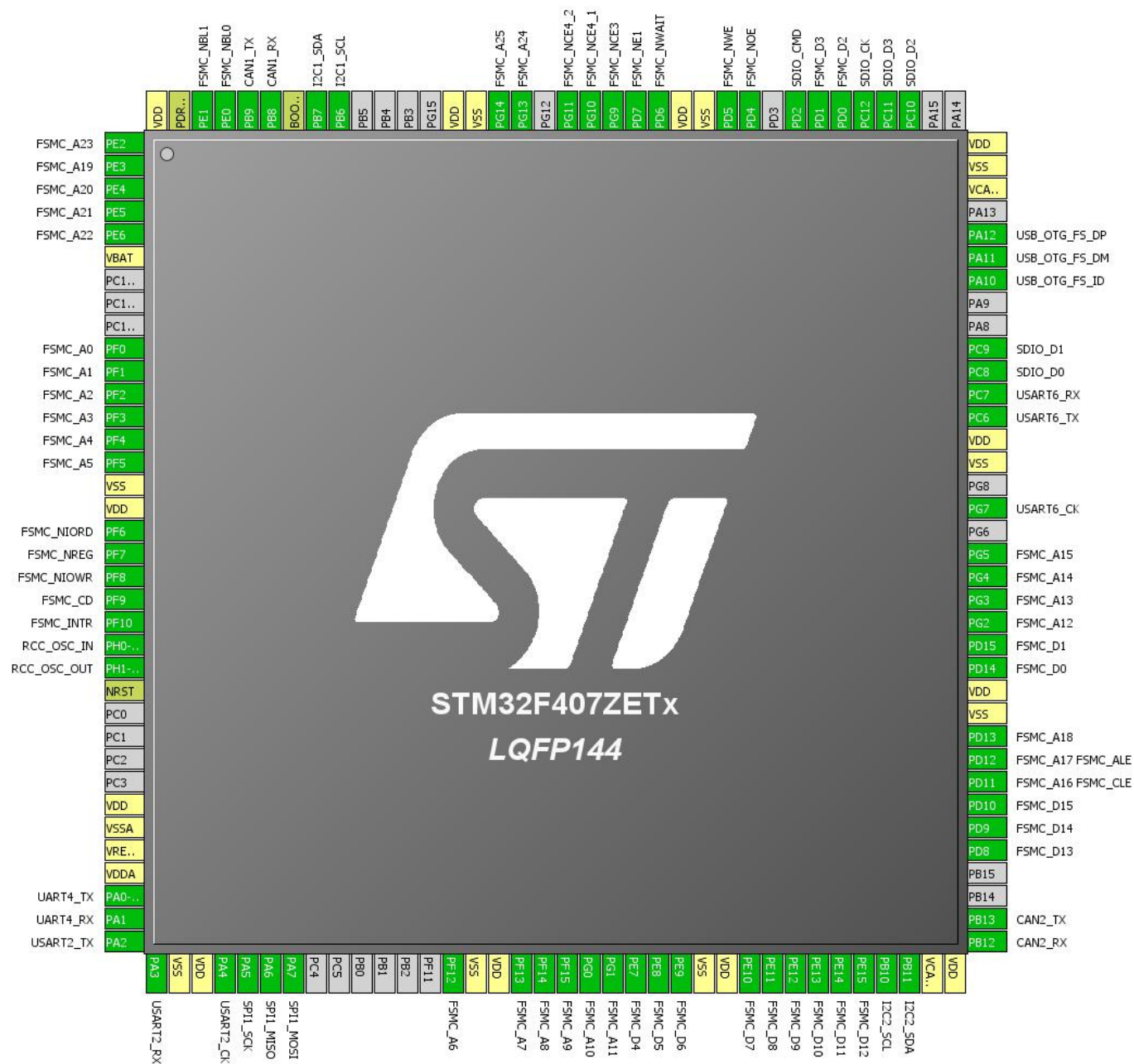
1.1. Project

Project Name	STCubeGenerated
Board Name	No information
Generated with:	STM32CubeMX 4.9.0
Date	11/16/2015

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	FSMC_A23	
2	PE3	I/O	FSMC_A19	
3	PE4	I/O	FSMC_A20	
4	PE5	I/O	FSMC_A21	
5	PE6	I/O	FSMC_A22	
6	VBAT	Power		
10	PF0	I/O	FSMC_A0	
11	PF1	I/O	FSMC_A1	
12	PF2	I/O	FSMC_A2	
13	PF3	I/O	FSMC_A3	
14	PF4	I/O	FSMC_A4	
15	PF5	I/O	FSMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	FSMC_NIORD	
19	PF7	I/O	FSMC_NREG	
20	PF8	I/O	FSMC_NIOWR	
21	PF9	I/O	FSMC_CD	
22	PF10	I/O	FSMC_INTR	
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	UART4_TX	
35	PA1	I/O	UART4_RX	
36	PA2	I/O	USART2_TX	
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	USART2_CK	
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
50	PF12	I/O	FSMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FSMC_A7	
54	PF14	I/O	FSMC_A8	
55	PF15	I/O	FSMC_A9	
56	PG0	I/O	FSMC_A10	
57	PG1	I/O	FSMC_A11	
58	PE7	I/O	FSMC_D4	
59	PE8	I/O	FSMC_D5	
60	PE9	I/O	FSMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FSMC_D7	
64	PE11	I/O	FSMC_D8	
65	PE12	I/O	FSMC_D9	
66	PE13	I/O	FSMC_D10	
67	PE14	I/O	FSMC_D11	
68	PE15	I/O	FSMC_D12	
69	PB10	I/O	I2C2_SCL	
70	PB11	I/O	I2C2_SDA	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	CAN2_RX	
74	PB13	I/O	CAN2_TX	
77	PD8	I/O	FSMC_D13	
78	PD9	I/O	FSMC_D14	
79	PD10	I/O	FSMC_D15	
80	PD11	I/O	FSMC_A16, FSMC_CLE	
81	PD12	I/O	FSMC_A17, FSMC_ALE	
82	PD13	I/O	FSMC_A18	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FSMC_D0	
86	PD15	I/O	FSMC_D1	
87	PG2	I/O	FSMC_A12	
88	PG3	I/O	FSMC_A13	
89	PG4	I/O	FSMC_A14	
90	PG5	I/O	FSMC_A15	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
92	PG7	I/O	USART6_CK	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
102	PA10	I/O	USB_OTG_FS_ID	
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
111	PC10	I/O	SDIO_D2	
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
114	PD0	I/O	FSMC_D2	
115	PD1	I/O	FSMC_D3	
116	PD2	I/O	SDIO_CMD	
118	PD4	I/O	FSMC_NOE	
119	PD5	I/O	FSMC_NWE	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	FSMC_NWAIT	
123	PD7	I/O	FSMC_NE1	
124	PG9	I/O	FSMC_NCE3	
125	PG10	I/O	FSMC_NCE4_1	
126	PG11	I/O	FSMC_NCE4_2	
128	PG13	I/O	FSMC_A24	
129	PG14	I/O	FSMC_A25	
130	VSS	Power		
131	VDD	Power		
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
139	PB8	I/O	CAN1_RX	
140	PB9	I/O	CAN1_TX	
141	PE0	I/O	FSMC_NBL0	
142	PE1	I/O	FSMC_NBL1	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
143	PDR_ON	Reset		
144	VDD	Power		

4. IPs and Middleware Configuration

4.1. CAN1

mode: Mode

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	380.95238095238096 *
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	1142 *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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4.2. CAN2

mode: Mode

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	380.95238095238096 *
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	1142 *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable

Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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4.3. CRC

mode: Activated

4.4. FSMC

4.4.1. [NOR Flash/PSRAM/SRAM/ROM 1]

Chip select: NE1

Memory type: SRAM

Address: 26 bits

Data: 16 bits

Wait: Asynchronous

mode: Byte enable

NOR/PSRAM control:

Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	Disabled
Extended mode	Disabled
Wait signal polarity	Low polarity
Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	Disabled
Extended mode	Disabled
Wait signal polarity	Low polarity

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15
Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

4.4.2. [NAND Flash 1]

Chip select: NCE3

Data/Address: 16 bits

Ready or busy: NWAIT

NAND control:

Bank	NAND bank 3
Data size	16 bits
ECC computation	Disabled
ECC page size	256 bytes
CLE low to RE low delay in HCLK cycles	1 *
ALE low to RE low delay in HCLK cycles	1 *

NAND common space timing in HCLK cycles:

Common space setup time	253 *
Common space wait setup time	253 *
Common space hold setup time	252
Common space Hi-Z setup time	253 *

NAND attribute space timing in HCLK cycles:

Attribute space setup time	253 *
Attribute space wait setup time	253 *
Attribute space hold setup time	252
Attribute space Hi-Z setup time	252

4.4.3. [Compact Flash]

mode: NCE4_1+NCE4_2 Chip Selects

Address: 11 bits

mode: Data: 16 bits

mode: Wait

mode: Interrupt

CF control:

Bank	CF bank 4
CLE low to RE low delay in HCLK cycles	1 *
ALE low to RE low delay in HCLK cycles	1 *

CF common space timing in HCLK cycles:

Common space setup time	253 *
Common space wait setup time	253 *
Common space hold setup time	252
Common space Hi-Z setup time	252

CF attribute space timing in HCLK cycles:

Attribute space setup time	253 *
Attribute space wait setup time	253 *
Attribute space hold setup time	252
Attribute space Hi-Z setup time	252

CF I/O space timing in HCLK cycles:

I/O space setup time	253 *
I/O space wait setup time	253 *
I/O space hold setup time	252
I/O space Hi-Z setup time	252

4.5. I2C1

I2C: I2C

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

4.6. I2C2

I2C: I2C

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit

Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

4.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
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Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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4.8. RNG

mode: Activated

4.9. SDIO

Mode: MMC 4 bits Wide bus

4.10. SPI1

Mode: Full-Duplex Master

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	42.0 MBits/s *

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

4.11. UART4

Mode: Asynchronous

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

4.12. USART2

Mode: Synchronous

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
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Clock Parameters:

Clock Polarity	Low
Clock Phase	One Edge
Clock Last Bit	Disable

4.13. USART6

Mode: Synchronous

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
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Clock Parameters:

Clock Polarity	Low
Clock Phase	One Edge
Clock Last Bit	Disable

4.14. USB_OTG_FS

Mode: OTG/Dual_Role_Device

*** User modified value**

5. System Configuration

5.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PB8	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB9	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
CAN2	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB13	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
FSMC	PE2	FSMC_A23	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE3	FSMC_A19	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE4	FSMC_A20	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE5	FSMC_A21	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE6	FSMC_A22	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF0	FSMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF1	FSMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF2	FSMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF3	FSMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF4	FSMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF5	FSMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF6	FSMC_NIORD	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF7	FSMC_NREG	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF8	FSMC_NIOWR	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF9	FSMC_CD	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF10	FSMC_INTR	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF12	FSMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF13	FSMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF14	FSMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF15	FSMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG0	FSMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG1	FSMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE7	FSMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE8	FSMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE9	FSMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE10	FSMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE11	FSMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE12	FSMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE13	FSMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE14	FSMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE15	FSMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD8	FSMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD9	FSMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD10	FSMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD11	FSMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD12	FSMC_A17	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD13	FSMC_A18	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD14	FSMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD15	FSMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG2	FSMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG3	FSMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG4	FSMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG5	FSMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD0	FSMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD1	FSMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD4	FSMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD5	FSMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD6	FSMC_NWAIT	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD7	FSMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG9	FSMC_NCE3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG10	FSMC_NCE4_1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG11	FSMC_NCE4_2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG13	FSMC_A24	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG14	FSMC_A25	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE0	FSMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE1	FSMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	High	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	High *	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	High *	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	High *	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	High *	
UART4	PA0-WKUP	UART4_TX	Alternate Function Push Pull	Pull-up	High *	
	PA1	UART4_RX	Alternate Function Push Pull	Pull-up	High *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA4	USART2_CK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
USART6	PG7	USART6_CK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
USB_OTG_FS	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	High *	

5.2. DMA configuration

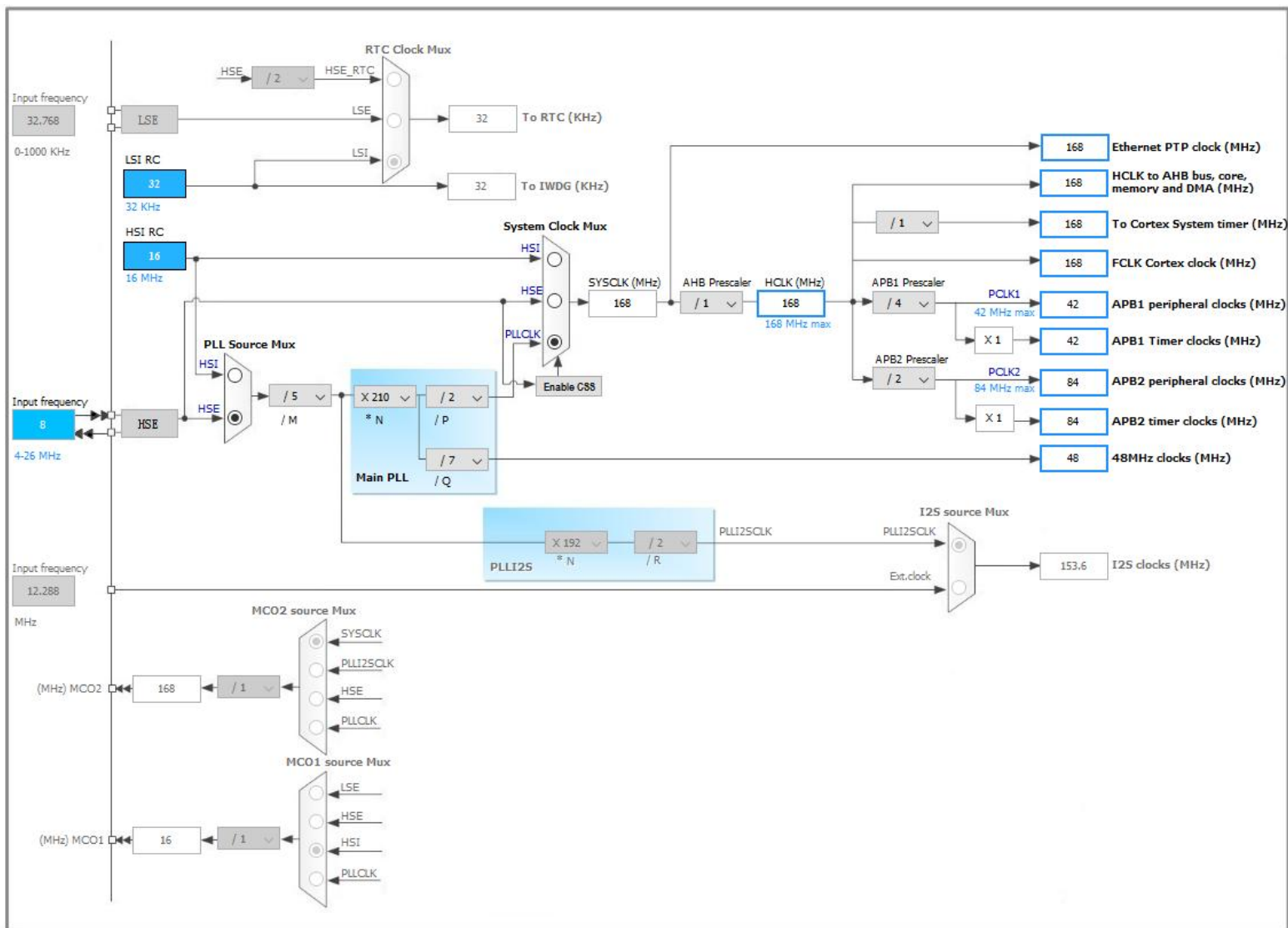
nothing configured in DMA service

5.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
Non Maskable Interrupt		unused	
Memory management fault		unused	
Pre-fetch fault, memory access fault		unused	
Undefined instruction or illegal state		unused	
Debug Monitor		unused	
RCC global interrupt		unused	
CAN1 TX interrupts		unused	
CAN1 RX0 interrupts		unused	
CAN1 RX1 interrupt		unused	
CAN1 SCE interrupt		unused	
I2C1 event interrupt		unused	
I2C1 error interrupt		unused	
I2C2 event interrupt		unused	
I2C2 error interrupt		unused	
SPI1 global interrupt		unused	
USART2 global interrupt		unused	
FSMC global interrupt		unused	
UART4 global interrupt		unused	
CAN2 TX interrupts		unused	
CAN2 RX0 interrupts		unused	
CAN2 RX1 interrupt		unused	
CAN2 SCE interrupt		unused	
USART6 global interrupt		unused	
HASH and RNG global interrupt		unused	

* User modified value

6. Clock Tree Configuration



7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407ZETx
Datasheet	022152_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STCubeGenerated
Project Folder	D:\git\Lib\DJISDK\MDK\RTE\Device\STM32F407ZETx\STCubeGenerated
Toolchain / IDE	MDK-ARM
Firmware Package Name and Version	STM32Cube FW_F4 V1.7.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

8.3. Toolchains Settings

Name	Value
Compiler Optimizations	Balanced Size/Speed