Ajay Kumar Garg Engineering College, Ghaziabad
Department of MCA
Solution Sessional Test-2

Course: MCA
Session: 2017-18
Subject: IPCO
Max Marks:50

Semester: III
Section: MCA-1 & 2
Sub Code: RCA-A01
Time: 2 hour

Section- A

Q.1. Differentiate signed and unsigned binary number representation.

Solu: The numbers without positive or negative signs are known as unsigned numbers. The unsigned numbers are always considered as positive numbers. In case of signed binary number system, the most significant bit represents the sign of the number. When MSB is 1, the number is negative, and when it is 0, the number is positive.

eg. $(B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0)_2$

B_7 ← Sign

$B_6 B_5 B_4 B_3 B_2 B_1 B_0$ → Magnitude of Binary Number

Q.2. What do you mean equivalance relation?

Solu. A relation R on set A is said to be an equivalance relation if R is reflexive, symmetric, and transitive. So for proving any relation on a given set to be an equivalence relation we shall have to prove that the relation satisfies all the three properties of being reflexive, symmetric, and transitive.

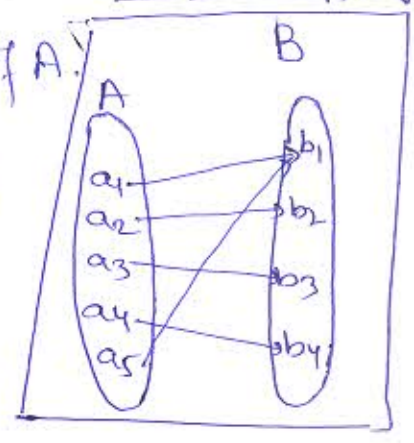
Q.3 What is onto mapping?

Solu: If each element of B is the image of A.

or

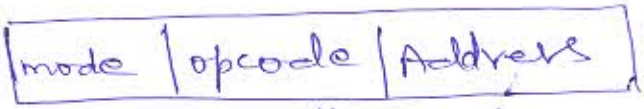
All the element of B (Co-domain) are the image of A (domain).

Onto Mapping



Q.4 List different type of Instruction formats.

Solu.



Instruction code

Operation code :- specifies, operations to be performed such as add, subtract, shift, complement

Address field :- specifies a memory address or a processor register.

Mode field :- specifies the way to determine the Operand or effective address depending on the addressing mode used.

There are in general of 4 type

a) zero address instruction
b) One address instruction
c) Two address instruction
d) three address instruction.

Q.5 > what is the concept of pipelining?

Solu. Pipelining is a techniques of decomposing a sequential process into sub-operations, with each sub-process being executed in a special dedicated segment that operates concurrently with all other segments. A pipeline can be visualized as a collection of processing segments through which binary information flows. The name pipe-line implies a flow of information analogous to an industrial assembly line.

—.

section-B

Q. 6. Let $x = \{1,2,3\}$ and f, g, h, and s are functions from x to x given by

$f = \{(1,2),(2,3),(3,1)\}$ $g = \{(1,2),(2,1),(3,3)\}$ $h = \{(1,1),(2,2),(3,1)\}$

$s = \{(1,1),(2,2),(3,3)\}$, then find fog, gof, $fohog$, sog, gos.

Solu. $fog = \{(1,3),(2,2),(3,1)\}$

$gof = \{(1,1),(2,3),(3,2)\} \neq fog$

$fohog = \{(1,3),(2,2),(3,2)\}$

$sog = \{(1,2),(2,1),(3,3)\} = g = gos$

$gos = \{(1,2),(2,1),(3,3)\}$

Q. 7. Prove that $1.2 + 2.3 + \ldots + n(n+1) = (n(n+1)(n+2)/3)$, where n belongs from set of natural numbers N. Prove it through principle of mathematical Induction.

Solu. Let the statement $P(n)$ be given by

$$P(n): \quad 1.2 + 2.3 + \cdots + n.(n+1) = \frac{n(n+1)(n+2)}{3} \quad -(1)$$

Step-I :- (Basic step) :- putting $n = 1$ in eq (1), we have

$$L.H.S = 1.2 = 2 \quad \& \quad R.H.S = \frac{1(1+1)(1+2)}{3} = 2$$

$$\Rightarrow \quad L.H.S. = R.H.S.$$

So, eqn (1) is true for $n = 1$.

Step II : (Inductive Hypothesis) :- Let $P(m)$ is true.

then $$1.2 + 2.3 + \cdots + m.(m+1) = \frac{m(m+1)(m+2)}{3} \quad -(2)$$

Step III :- (Inductive Step) :- If $p(m)$ is true then $p(m+1)$ must be true.

$$\Rightarrow \underbrace{[1\cdot2 + 2\cdot3 + \cdots + m(m+1)]}_{} + (m+1)(m+2) = \frac{(m+1)(m+2)(m+3)}{3} \quad \text{---(3)}$$

from eqn (2) & (3),

$$\frac{m(m+1)(m+2)}{3} + (m+1)(m+2) = \frac{(m+1)(m+2)(m+3)}{3}$$

$$\Rightarrow (m+1)(m+2)\left[\frac{m+3}{3}\right] = \frac{(m+1)(m+2)(m+3)}{3}$$

$$\Rightarrow \frac{(m+1)(m+2)(m+3)}{3} = \frac{(m+1)(m+2)(m+3)}{3}$$

$$\Rightarrow \text{L.H.S.} = \text{R.H.S.}$$

So, given inequality is true for every value of n.

Hence proved.

Q.6> $f(x) = \frac{(x+2)}{(x+1)}$, then calculate the inverse function of x.

Solu. Let $f(x) = y$

$$\Rightarrow y = \frac{(x+2)}{(x+1)}$$

$$\Rightarrow y(x+1) = (x+2)$$

$$\Rightarrow yx + y = x + 2$$

$$\Rightarrow yx - x = 2 - y$$

$$\Rightarrow x(y-1) = 2 - y$$

$$\Rightarrow \quad x = \frac{2-y}{y-1}$$

$$\Rightarrow \quad \boxed{f^{-1}(x) = \frac{2-x}{x-1}}$$

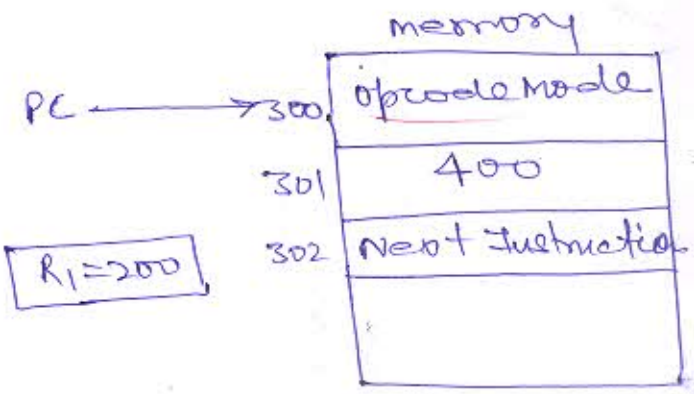
(3)

Q. 9> An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is —

i> Direct ii> Immediate iii> Relative

iv> Register Indirect v> Index with R1 as the index Register.

Sol>



The effective address are as follows:-

i> Direct : 400

ii> Immediate : 301

iii> Relative : 302 + 400 = 702

iv> Register Indirect : 200

v> Index with R1 as the index Register :- 200 + 400 = 600

Q.10. Define the Instruction Pipeline in detail.

Soln. The instruction pipeline reads consecutive instructions from memory while previous instructions are being executed in other segments. This type of unit that forms a queue rather than stack. The instructions are inserted into FIFO buffer so that they can be executed on a first in first out basis. Thus the instruction stream can be placed in a queue, waiting for decoding and processing by the execution segment. In most general case, the computer needs to process ~~each~~ each instruction with the following sequence of steps:-

i) Fetch the instruction from memory
ii) Decode the instruction
iii) Calculate the effective address.
iv) Fetch the operands from memory
v) Execute the instruction
vi) Store the result on the proper place.

Section C

Q.11 Explain different types of functions in detail. Also explain one-one-onto mapping.

Soln: 1) One-to-one function: A mapping or function $f: A \to B$ is said to be one-to-one if for each pair of distinct elements of A, their f-images are also distinct in B. if for $x_1, x_2 \in A$ $(x_1 \neq x_2) \Rightarrow f(x_1) \neq f(x_2)$ in B

2) Many one function: A mapping $f: A \to B$ is many one if two or more different elements in A have the same f-image in B i.e $x_1, x_2 \in A$

and $x_1 \neq x_2 \Rightarrow f(x_1) = f(x_2)$

3) Onto mapping: A mapping $f: A \to B$ is said to onto if $\forall$ $y \in B$ $\exists$ $x \in A$ such that $y = f(x)$

It means every element in B has its preimage in A.

4) Into mapping: A mapping $f: A \to B$ is said to be into mapping if there exist at least one element of the co-domain set B which is not the f-image of any element in A.

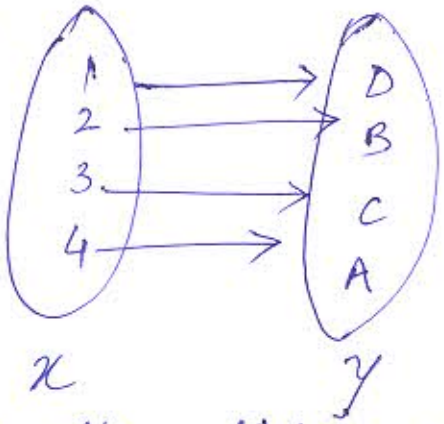
5) One-One-into mapping: A mapping which is one-to one and into is called one-one into mapping from A to B. It means that

a) $f(x_1) \neq f(x_2)$ if $x_1 \neq x_2$ i.e f image of two distinct elements in A shall be the two distinct elements in B and

b) there exist at least one element in B

which is not the f-image of any element in A

One-One Onto mapping: if every element of the co-domain is mapped to by exactly one element of the domain is called One-One-Onto mapping of function.



Q12. What is the difference between instruction stream and data stream? What is Flynn's classification about computer system?

Soln: There are variety of ways that parallel processing can be classified. Based on the multiplicity of Instruction streams and Data Streams:-

1) Instruction stream is a sequence of Instructions read from memory constitutes an instruction stream

2) Data stream - Operations performed on the data in the processor constitutes a data stream.

flynn's Classification

1) Single Instruction Single data stream
2) Single Instruction multiple data stream
3) Multiple Instruction multiple data stream
4) Multiple Instruction Single data stream

SISD (Single Instruction Single Data Stream) represents the organization of a single computer containing a control unit, a processor unit, a memory unit Instructions are executed sequentially and the system may or may not have internal parallel processing capabilitities.

SIMD (Single Instruction Multiple Data Stream) represents an organization that includes many processing units under the supervision of a common control unit. All processors receive the same instruction from the control unit but operate on different items of data. The shared memory unit must contain multiple modules so that it can communicate with all processors simultaneously.

MISD (Multiple Instruction Single Data Stream) This structure is only of theortical interest since no practical system has been constructed using MISD.

MIMD refers to a computer system capable of processing several programs at the same time Most multiprocessor and multicomputer system can be classified in this category.