Solution of ST-2

Course - B.Tech. Session - 2017-18

Subject - Computer organisation & Architecture

Max Marks - 50 Time = 2 Hours

Semester - III Subject Code - RCS-302

Section → IT - I, J, CS - 1, 2, 3

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Section-A

Q1:- Define Micro-instruction and Micro-operation with example.

Ans. Micro instruction :- It is the most elementary instruction in the computer, such as moving the contents of a register to the ALU. It takes several micro instructions to carry out one complex machine instruction (CISC).

for eg. For fetching data :-

If index
ELSE next
inst. map

Microoperation :- It performs basic operations on the data stored in one or more registers including transferring data between registers or external buses of the CPU.

For eg. Shift, count, clear, load, etc.

Q2:- Write control steps for conditional Branching with the branch condition <0.

Ans. A programming instruction that directs the computer to another part of the program based on the results of a compare of HL languages such as IF THEN ELSE and CASE, are used to express the compare and conditional branch.

conditional branch instructions allows the CPU to follow a course of action dependent on the results of computations. They use the ALU codes to determine whether to branch or not.

Q3.— Explain Hit, Miss and Hit-Rate in Cache Memory.

Ans. When the CPU refers to memory and finds the word in cache, it is said to produce a hit. If the word is not found in cache, it is in main memory and then it counts as a miss.

$$\text{Hit ratio} = \frac{\text{No. of hits}}{\text{Total number of CPU references.}}$$

Q4:— Define the Role of Presence-Bit in Memory-page Table.

Ans. It indicates the status of each column with respect to its nullability multivalue compressibility and auto compressibility.

Nullability
- 0 → Non-nullable
- 1 → Nullable.

Compressibility
- 0 → Not compressed
- 1 → Compressed on values.

Ques5:- Differentiate between DRAM and SRAM.

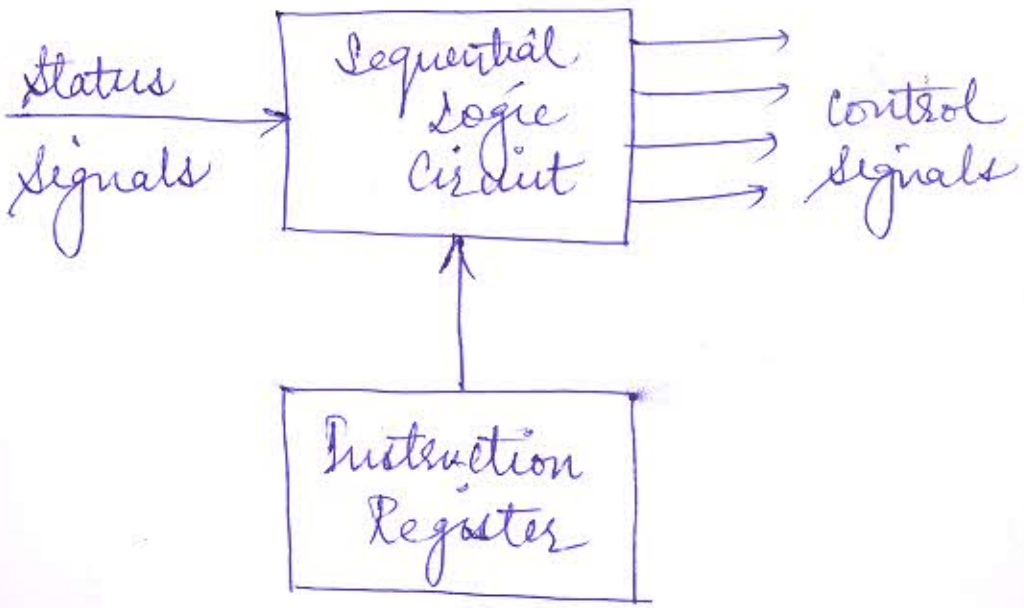
Ans. DRAM :- loses its stored information in a very short time (millisec). Dynamic memory cells represents single bit capacitor holds and transistor acts as switch.

SRAM :- It retains information only as long as the power supply is on. It is costlier in comparison to DRAM.

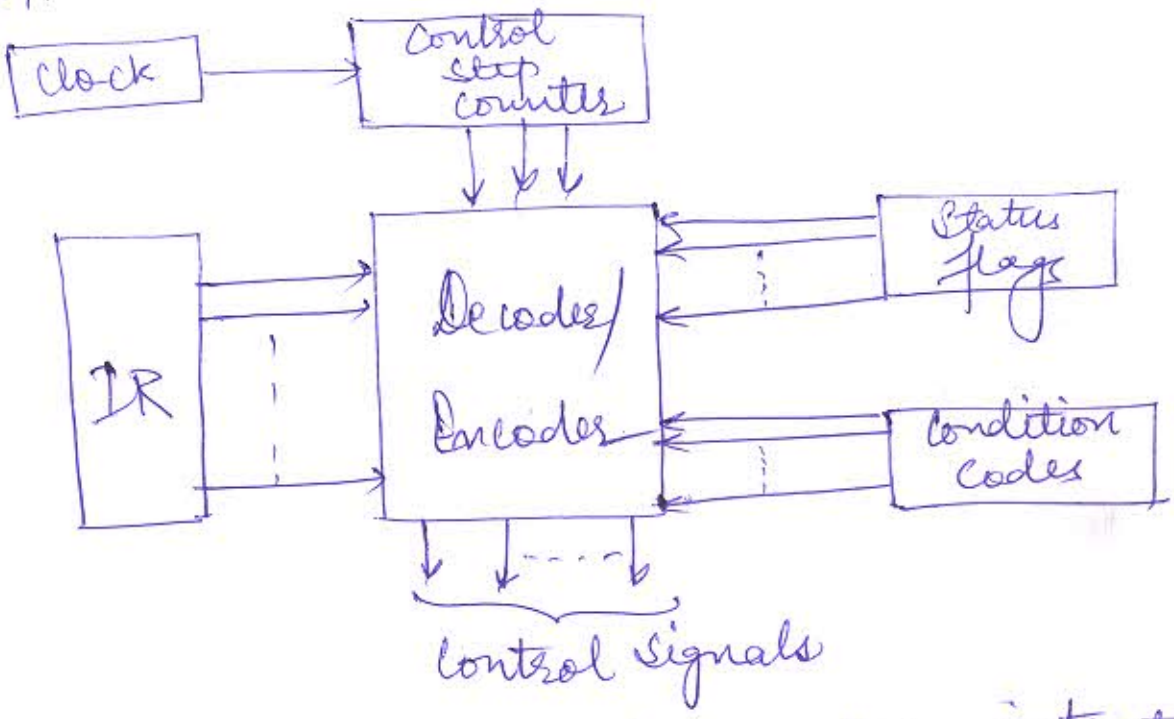
Section-B

Q6:- what do you understand by hardwired control? Describe any one method used for designing of hardwired control unit.

Ans.



The hardwired control unit is used only for particular applications. It is designed by minimizing the components used to maximize the system operation.



The decoder circuit takes the instruction from instruction register and execute that instruction by using status flags and condition codes. The control step counter increment in the instruction format and transfer this signal to decoder/ encoder circuit that generate the control signal for that instruction.

Q7:- Explain all the components of control unit connected through single bus structure. Discuss the basic structure of micro-program control unit.

Ans.

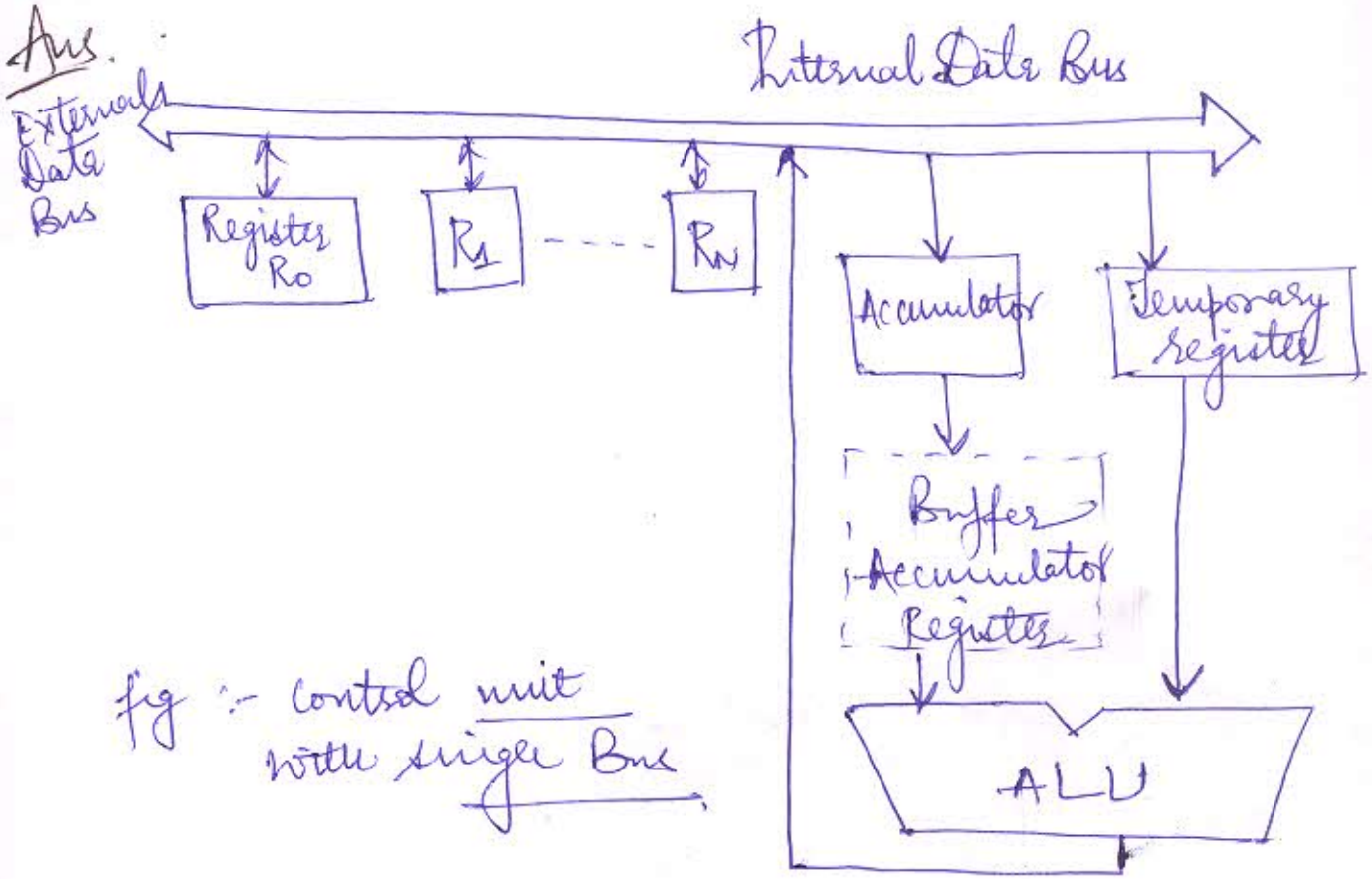


fig :- control unit with single Bus

The control memory assumed to be ROM within which control information is permanently stored. The location of the next address memory microinstruction may be the one next in sequence or it may be located somewhere else in the control memory. The next address may also be a function of external input condition.

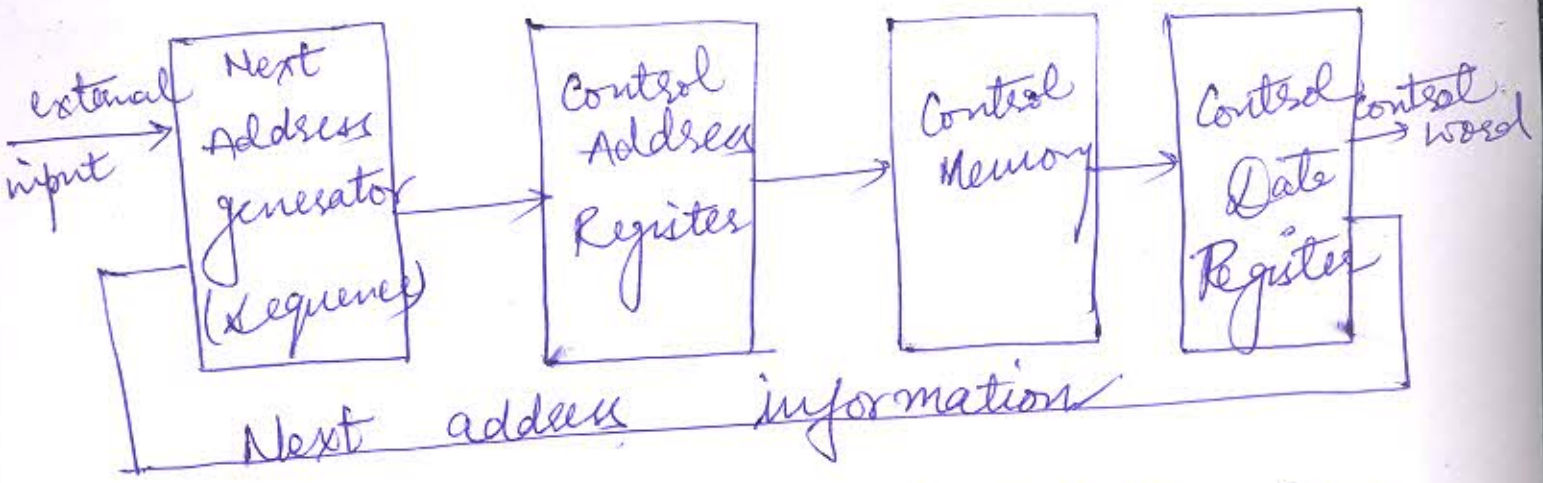


fig:- Micro programmed Control Unit

Q8:- Draw a circuit and timing diagram for write operation.

Ans:- Opcode R_1, R_2, R_3

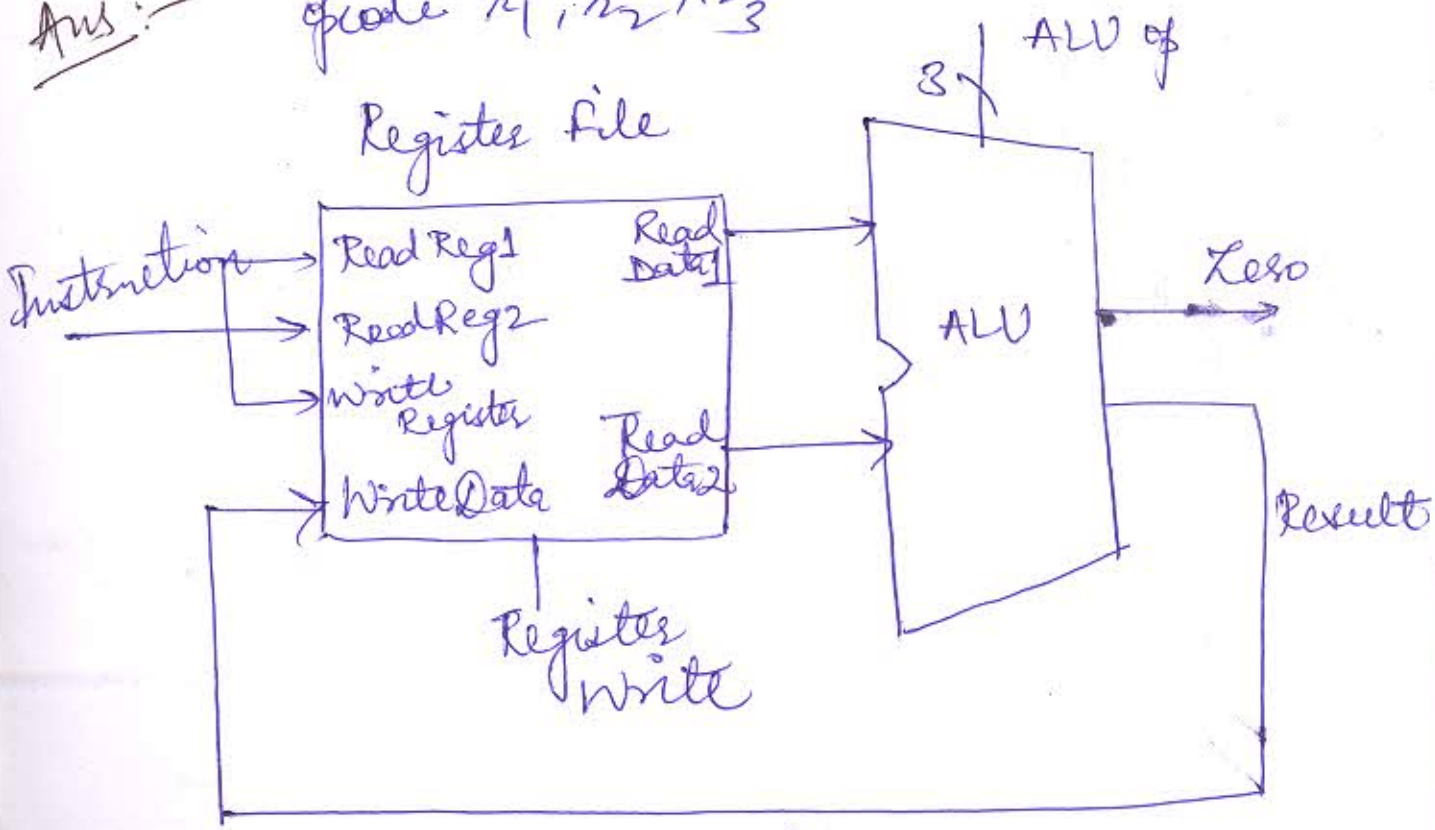


fig:- Circuit Diagram

Memory Write Cycle

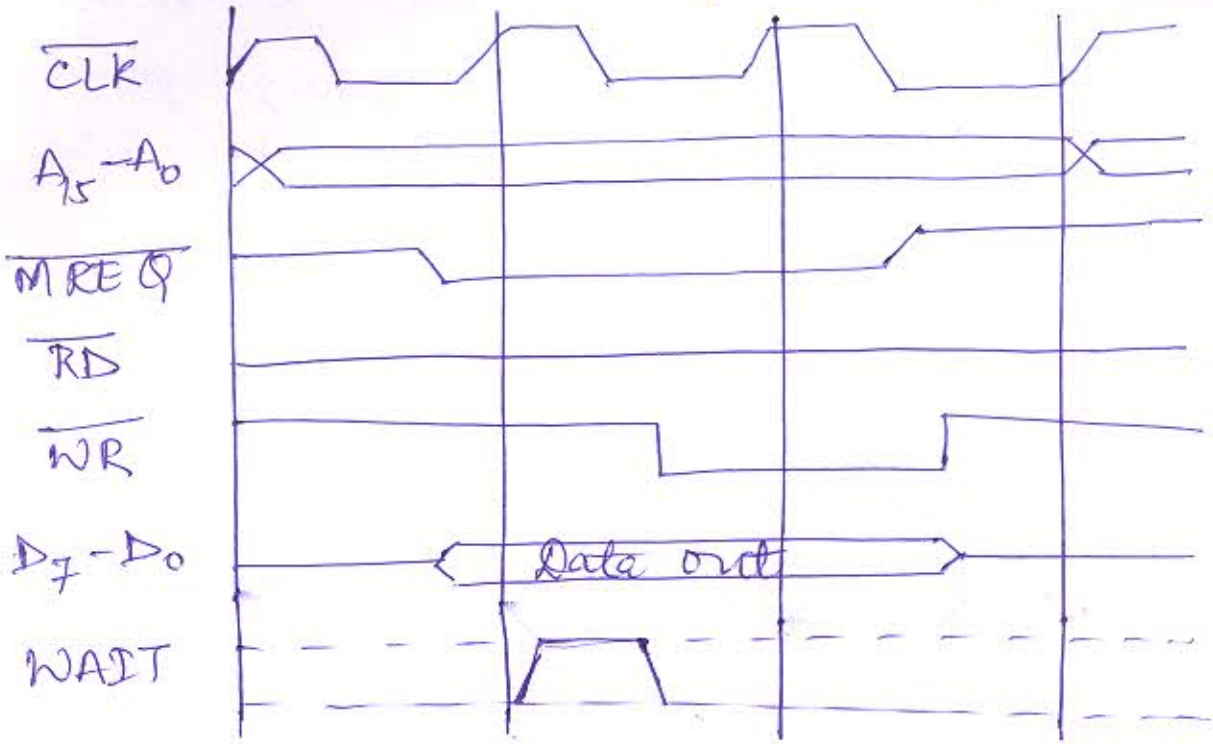
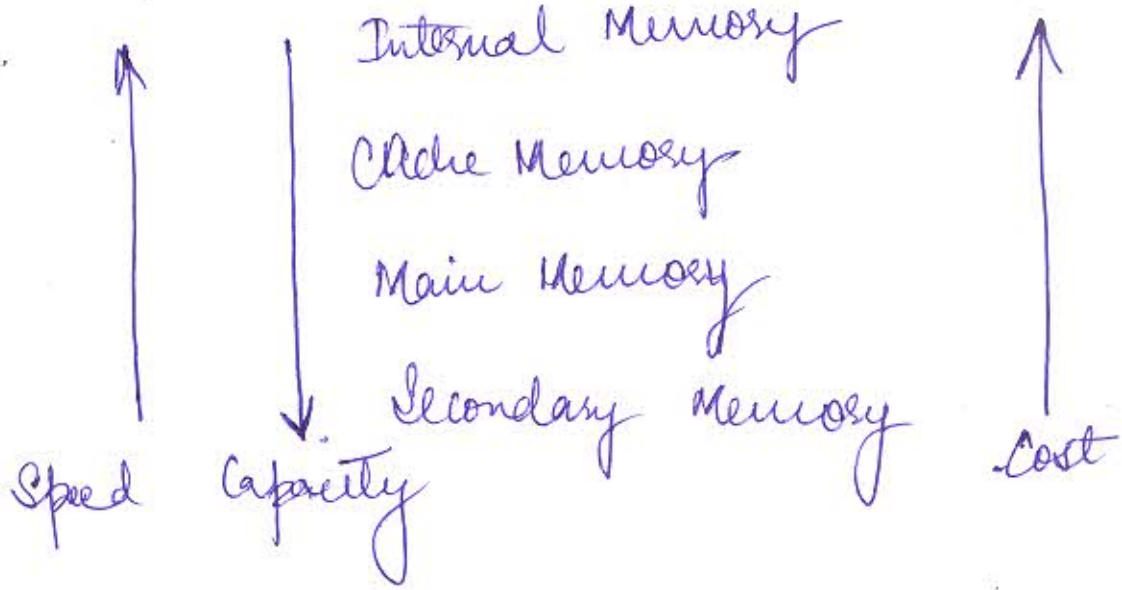


Fig:- Timing Diagram

Q9:- Explain the memory Hierarchy in computer organization. Formulate the average access time for cache memory.

Ans.



The memory unit is an essential component in any digital computer since it is needed for storing programs and data.

The memory unit that communicates directly with the CPU is called the main memory. The devices which provides the backup storage are called auxiliary memory.

Average Access Time for cache memory :-

$$T_{avg} = h * T_c + (1 - h) * M$$

where, h = hit rate

$(1-h)$ = miss rate

T_c = Time to access information from cache

M = Miss penalty (Time to access main memory).

Q10 :- A computer system has a memory consisting of 1M 16 bit words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block. Calculate the no. of bits in each of the TAG, BLOCK and WORD fields for direct mapping and TAG, SET & WORD fields for associative mapping in the main memory address format.

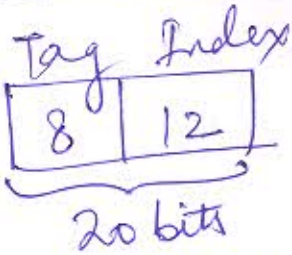
Ans. Main memory size $= 1M \times 16 = 2^{20} \times 16$

Cache memory size $= 4K \times 16 = 2^{12} \times 16$

Block size $= 64 \times 16 = 2^6 \times 16 \Rightarrow$ no. of blocks $= \frac{2^{12} \times 16}{2^6 \times 16} = 2^6 = 64$

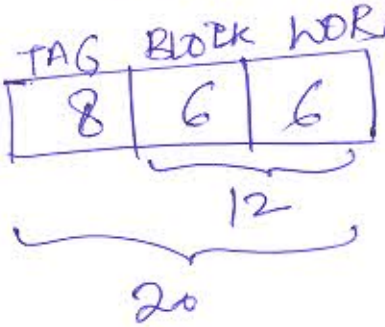
Set size $= 4$ blocks $= 2^2$ blocks.

Direct mapping - main memory address



non Index < Block = 6 bits, Word = 6 bits

TAG = 8 bits, Index = 12 bits



Set - Associative Mapping :-

no. of sets = $\frac{\text{no. of Blocks}}{4} = \frac{64}{4} = 16 = 2^4$

TAG	SET	WORD
10	4	6

20

Section - C

Q11 :- Write all the control steps to execute following instruction with operation in right to left direction :-

MULT R_3, (R_2), R_1

Ans Given instruction :-

$R_3 = R_2 * R_1$

This instruction can be understood as:- The content of register R_1 is multiplied with the content of memory location stored in register R_2 and the result is stored in Register R_3. Executing this instruction requires the following actions:-

(i) Fetch the instruction.

(ii) Fetch the first operand (contents of memory location pointed to by R_2).

(iii) Perform multiplication

(iv) Load the result into R_3.

Steps	Action
1.	PCout MARin, Read, ClearY, Set Carryin, Add, Zin
2.	Zout, PCin, WMFC
3.	MDRout, IRin
4.	R2out, MARin, Read
5.	Riout, Yin, WMFC
6.	MDRout, Yout, Mul, Zin
7.	Zout, R3in, End

Q12:- A computer employs RAM chips of 256*8 and ROM chips 1024*8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and 4 interface units, each with four registers. A memory mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.

(a) How many RAM, ROM chips are needed?

(b) Draw a memory address map for the system.

(c) Give the address range in Hexadecimal for

RAM, ROM and Interface Unit.

Ans Size of RAM $= 256 \times 8 = 2^8 \times 8$

Size of ROM $= 1024 \times 8 = 2^{10} \times 8$

Memory for RAM $= 2k$ bytes $= 2 \times 2^{10} \times 8 = 2^{11} \times 8$

Memory for ROM $= 4k$ bytes $= 2^{12} \times 8$

no. interface registers $= 4 \times 4 = 16$

(a) no. of RAM chips $= \frac{2^{11} \times 8}{2^8 \times 8} = 2^3 = 8$

no. of ROM chips $= \frac{2^{12} \times 8}{2^{10} \times 8} = 2^2 = 4$

(b) & (c)

Components	Address	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RAM	0000 - 07FF	0	0	0	0	0	← 3×8 decoder →				x	x	x	x	x	x	x
ROM	4000 - 4FFF	0	1	0	0	← 2×4 Decoder →					x	x	x	x	x	x	x
Interface registers	8000 - 800F	1	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x

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