Ajay Kumar Garg Engineering College, Ghaziabad

Department of ECE

Model Solution Sessional Test-2

Course:	**B.Tech**	**Semester:**	**V**
Session:	**2017-18**	**Section:**	**EC-1, 2, 3 & EI-1**
Subject:	**Integrated Circuits**	**Sub. Code:**	**NEC-501R**
Max Marks: 50		**Time: 2 hour**	

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Note : Answer all sections

Section-A

Q.A Attempt all parts

Q1. How the quality factor changes the frequency response of the filter?

Ans. Quality factor $= \frac{f_c}{B.W}$

where, f_c = centre frequency

B.W = Bandwidth

As Q is inversely proportional to bandwidth, frequency response of the filter becomes wide or narrow as the bandwidth increases or decreases.

Q2. Write down the performance parameters of a digital logic family.

Sol' a) Noise Margin
b) Propagation delay
c) Power dissipation
d) Delay. Power product
e) fan-in, fan-out
f) Silicon Area

Q3. Given CMOS implementation of $F = \bar{A}B + A\bar{B}$.

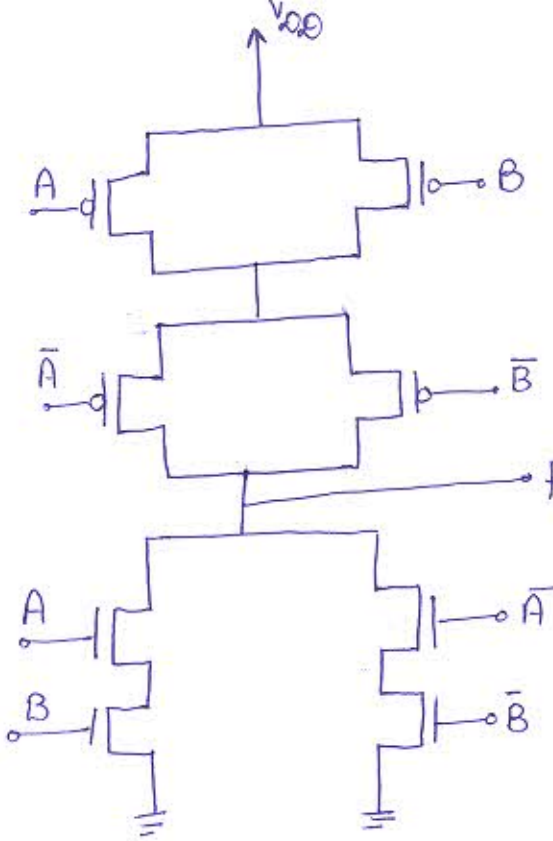
Ans

$$F = \bar{A}B + A\bar{B}$$

$$\bar{F} = \overline{\bar{A}B + A\bar{B}}$$

$$= (A+\bar{B})(\bar{A}+B)$$

$$= \bar{A}\bar{B} + A.B$$



$$F = \overline{A.B + \bar{A}.\bar{B}} = (\bar{A}+\bar{B})(A+B)$$

$$= \bar{A}B + A\bar{B}$$

Q4. What are the limitations of an ideal differentiator & Ideal integrator circuit?

Sol^{n} Ideal Differentiator :- i) Gain $A = -s.RC$, $s = j\omega = j2\pi f$

$$\Rightarrow A \propto f$$

As $f \to \infty$
$A \to \infty$, differentiator saturates for high frequencies.

ii) As frequency increases, input impedance decreases & the circuit becomes more sensitive towards noise.

Ideal Integrator :- i) Gain $A = \frac{-1}{sRC}$

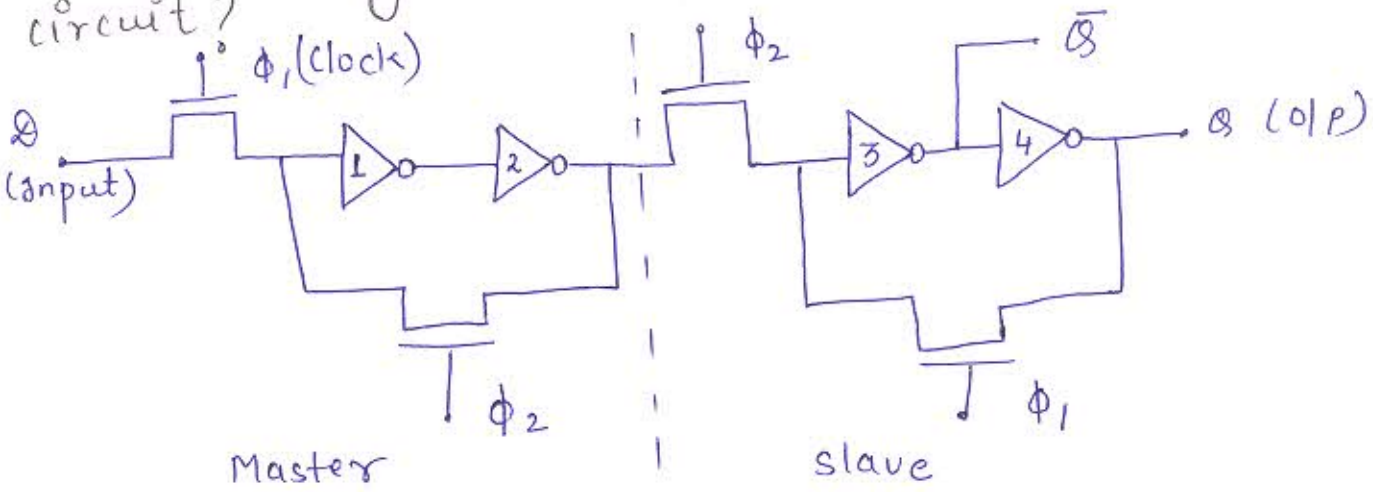
$$A \propto \frac{1}{f}$$

As $f \to 0$
$A \to \infty$

Integrator saturates at low frequencies.

Q5. Sketch properly labeled Master Slave D flip-flop circuit?

Sol^n.



Section-B

Q6. Design a wide band pass filter with $f_1 = 100Hz$ & $f_2 = 2KHz$ & a pass band gain = 4. Also obtain the value of quality factor for it.

Sol^n

Designing of wide Band Pass filter :- A wide band Pass filter is a combination of High pass filter & low pass filter.

Given, $f_1 = 100Hz$, $f_2 = 2KHz$

$$f_H > f_L$$

$\therefore$ $f_H = f_2 = 2KHz$

$f_L = f_1 = 100Hz$

Gain $A = 4$

$A_T = A_{f_1} * A_{f_2}$ { for $A_{f_1} = A_{f_2}$ }

$4 = (A_f)^2$

$A_f = \sqrt{4} = 2$

$\Rightarrow A_{fH} = A_{fL} = 2$

HPF :-

$$f_L = \frac{1}{2\pi RC}$$

selecting $C = 0.1\,\mu f$

$$100 = \frac{1}{2\pi R \times 0.1 \times 10^{-6}}$$

$$\boxed{R = 15.93\ k\Omega}$$

$$A_{f_L} = 1 + \frac{R_f}{R_{in}}$$

$$2 = 1 + \frac{R_f}{R_{in}}$$

$$\Rightarrow R_f = R_{in} = 10k\Omega$$

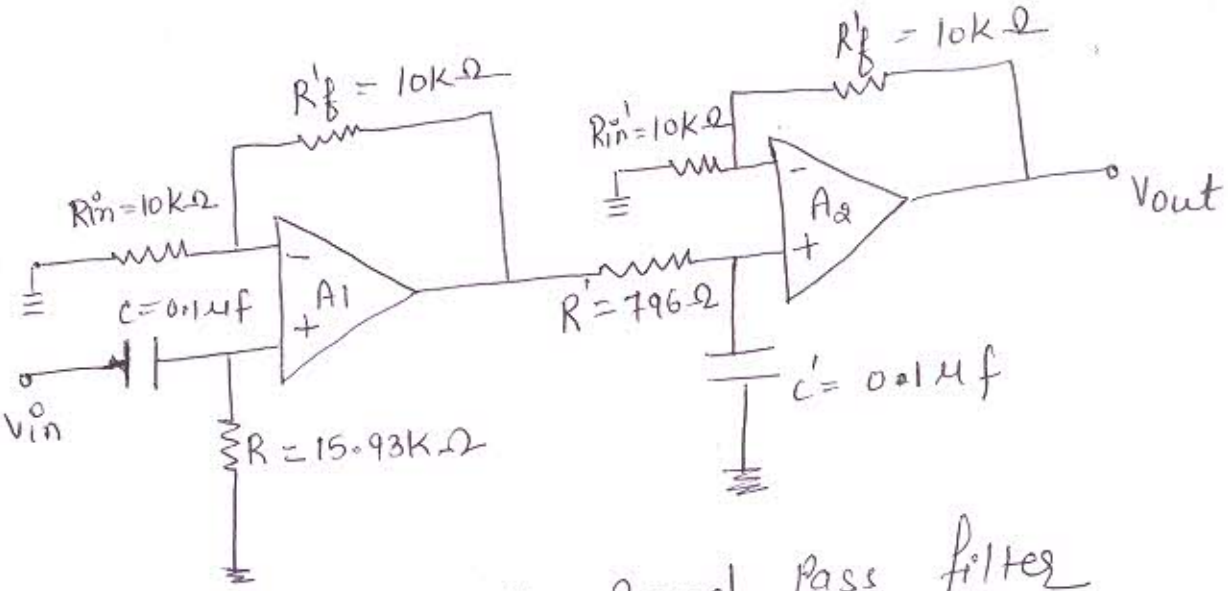
LPf :-

$$f_H = \frac{1}{2\pi R'C'}$$

$$2000 = \frac{1}{2\pi R' \times 0.1 \times 10^{-6}} \quad \{\text{selecting } C = 0.1\mu f\}$$

$$\boxed{R' = 796\ \Omega}$$

$$A_{f_H} = 1 + \frac{R_f'}{R_{in}'} \Rightarrow 2 = 1 + \frac{R_f'}{R_{in}'} \Rightarrow R_f' = R_{in}' = 10k\Omega$$



Wide Band Pass filter

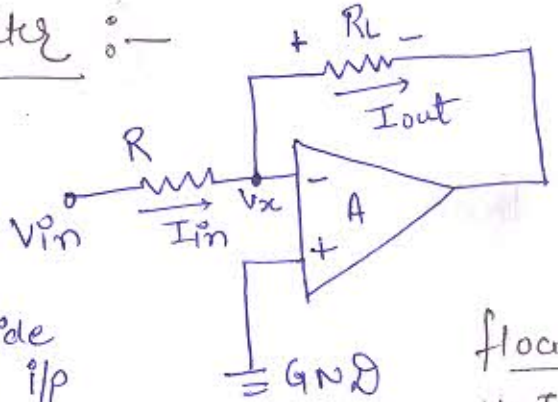
Quality factor $Q = \frac{f_c}{B.W}$

$$Q = \frac{\sqrt{f_H \cdot f_L}}{f_H - f_L} = \frac{\sqrt{100 \times 2 \times 10^3}}{2000 - 100}$$

$$\boxed{Q = 0.235} \text{ Ans.}$$

Qf. Derive the output voltage equation for both floating & grounded load V to I converter using relevant diagram. Also mention applications of V-I converter.

Sol: Floating load V-I Converter :-



from the circuit diag.

$I_{in} = I_{out}$

As NO current will enter inside the op-amp due to high i/p Impedance.

$$\frac{V_{in} - 0}{R} = I_{out} \quad \{V_x = 0 \because \text{virtual Gnd}\}$$

$\Rightarrow \boxed{I_{out} \propto V_{in}}$ $\Rightarrow$ Current across the load is directly proportional to applied i/p voltage

floating load V-I converter

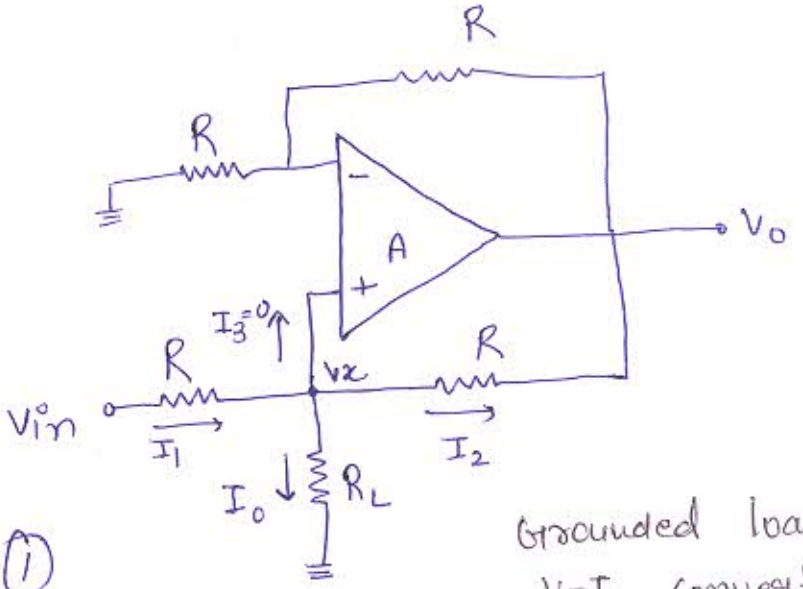
Grounded load V-I converter :-

from the circuit diagram :-

$$I_1 = I_0 + I_2$$

$$\frac{V_{in} - V_x}{R} = I_0 + \frac{V_x - V_0}{R} \quad \text{—(1)}$$

for non-inverting configuration:-



$$\frac{V_o}{V_x} = 1 + \frac{R}{R}$$

$$V_x = V_o/2$$

Putting this value in eq^n (1)

$$I_{on} = \frac{V_{in}}{R}$$

Grounded load V-I converter

$I_{out} \propto V_{in}$ current across grounded load is directly proportional to applied input voltage.

Application of V-I converter

i) low voltage A.C. voltmeter
ii) Zener diode testing, Diode matching

Q8. Give truth table of CMOS realization of Half adder with input A & B.

Sol^n

Truth Table for Half Adder

A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

Expression for Sum

$$S = \bar{A}B + A\bar{B}$$

for carry

$$C_Y = A \cdot B$$

CMOS Implementation :-

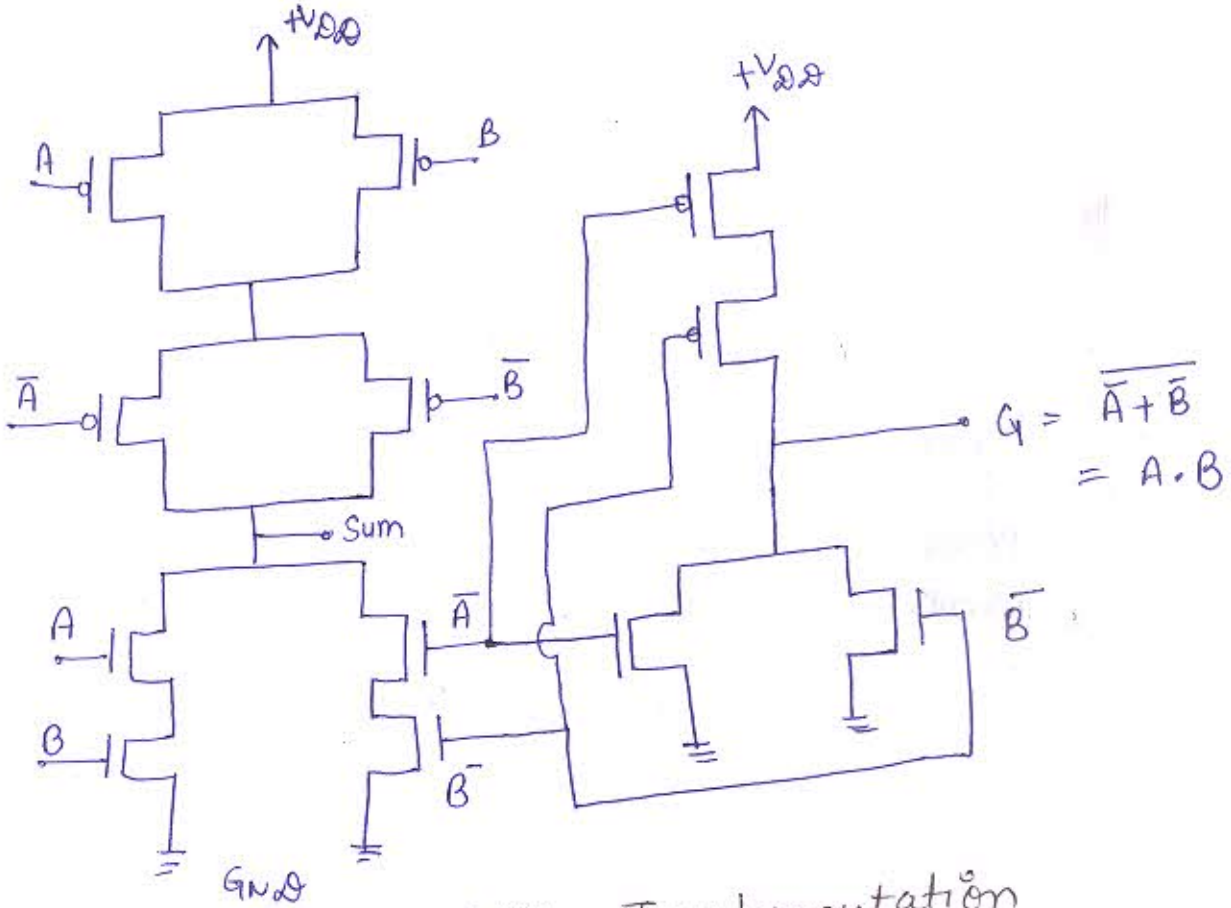
$$S = \bar{A}B + A\bar{B}$$

$$\bar{S} = \overline{\bar{A}B + A\bar{B}} = A \cdot B + \bar{A} \cdot \bar{B}$$

&

$$C_Y = A \cdot B$$

$$\bar{C}_Y = \overline{A \cdot B} = \bar{A} + \bar{B}$$

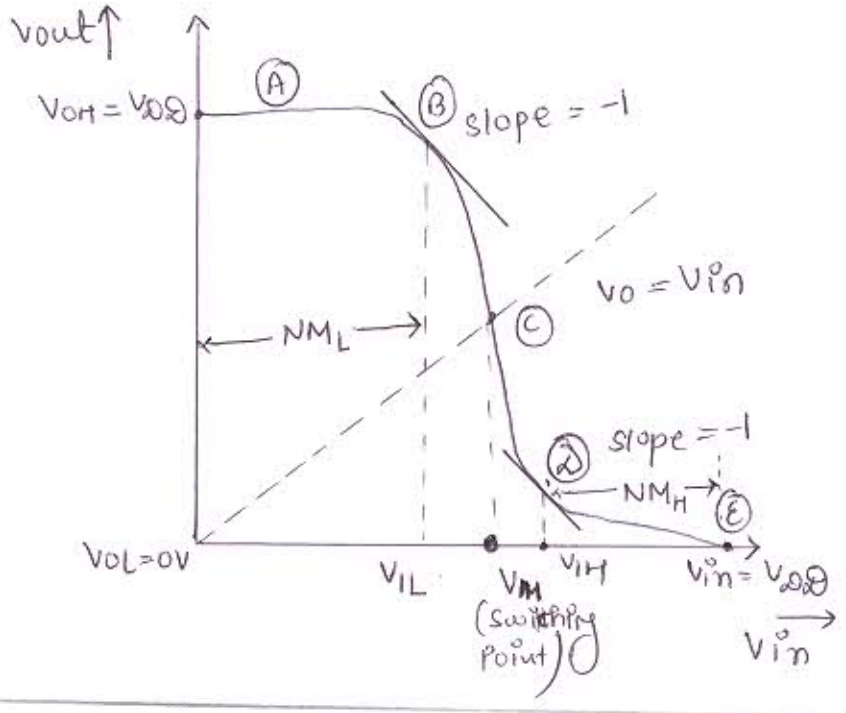


CMOS Implementation of Half Adder

Q9. Draw the properly labeled VTC curve for the CMOS inverter. Describe each region & define the terms V_{IH}, V_{IL}, V_{OH} & V_{OL}.

Sol^{n}

VTC Curve for CMOS Inverter :-



Region	MOSFET Operation	Vin	Vo ut
A	PMOS – Active NMOS – Cut-off	0V $< V_{t,n}$	V_{DD}
B	PMOS – Active NMOS – Saturation	V_{IL}	$\cong V_{DD}$
C	PMOS – Saturation NMOS – Saturation	$V_{th} = V_{DD}/2$	Vout
D	PMOS = Saturation NMOS = Active	V_{IH}	$\cong$ GND
E	PMOS = Cut-off NMOS = Active	V_{DD}	= GND

V_{IH} = Minimum high input voltage that can be treated as logic '1' at the input.

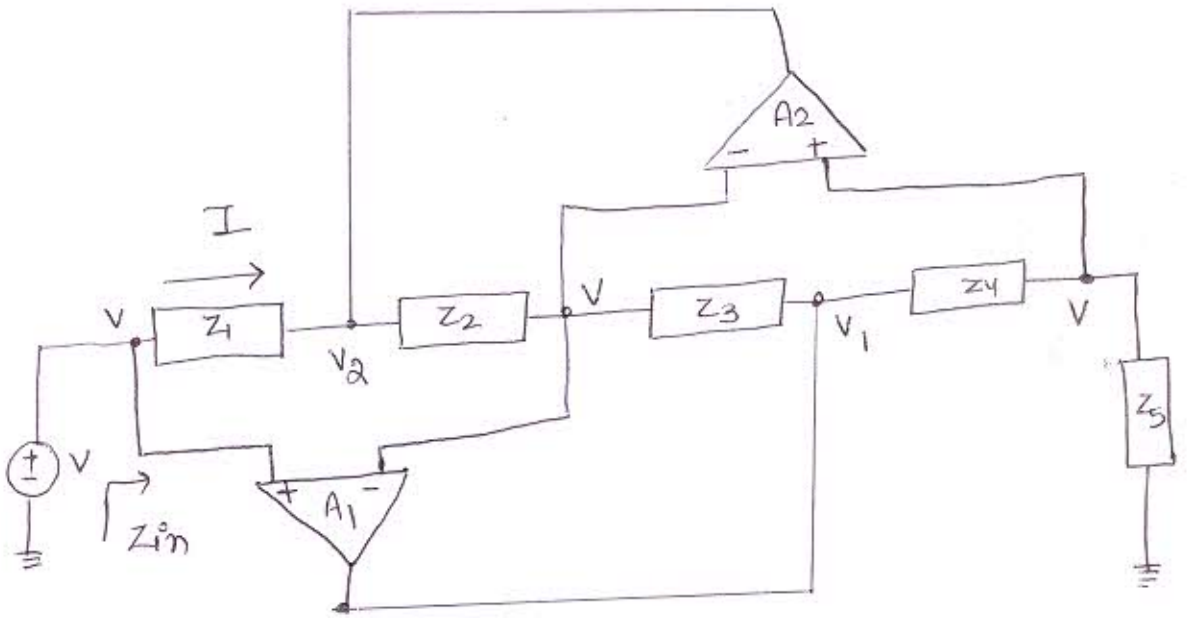
V_{IL} = Maximum low input voltage that can be treated as logic '0' at the input.

V_{OH} = Maximum output voltage that can be treated as logic '1' at the output.

V_{OL} = Minimum o/p voltage that can be treated as logic '0' at the output.

Q10. Draw GIC circuit & obtain expression for its equivalent input impedance. How we can simulate inductor with the help of a GIC circuit?

Sol^n GIC (Generalized Impedance Converter) :-



from the circuit diagram;

$$I = \frac{V - V_2}{Z_1} \quad -(1)$$

writing expression for current b/w node Z_2 & Z_3 and b/w node Z_4 & Z_5

$$\frac{V_2 - V}{Z_2} + \frac{V_1 - V}{Z_3} = 0 \quad -(2)$$

$$\frac{V_1 - V}{Z_4} + \frac{0 - V}{Z_5} = 0$$

$$Z_5(V_1 - V) - V_1 Z_4 = 0$$

$$Z_5 V_1 - Z_5 V - V_1 Z_4 = 0$$

$$V_1 = \frac{(Z_5 + Z_4) \cdot V}{Z_5} \quad \text{— (3)}$$

putting value of V_1 from eq^n (3) in eq^n (2)

$$V_2 = \frac{1}{Z_3}\left[V(Z_2 + Z_3) - V(Z_5 + Z_4)\frac{Z_2}{Z_5} \right]$$

$$V_2 = \frac{V(Z_3 + Z_3)Z_5 - V(Z_5 + Z_4)Z_2}{Z_5 \cdot Z_3}$$

putting this value in eq^n (1)

$$I = V\left[\frac{Z_5 Z_3 - Z_5 Z_2 - Z_5 Z_3 + Z_5 Z_2 + Z_4 Z_2}{Z_5 Z_3} \right] \Big/ Z_4$$

$$I = V\left[\frac{Z_4 Z_2}{Z_1 Z_3 Z_5} \right]$$

or $$\frac{V}{I} = \frac{Z_5 Z_3 Z_1}{Z_2 Z_4}$$

or $$\boxed{Z_{in} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}}$$ This is the required expression for input impedance of GIC

Simulation of inductor using GIC :-

Inductance $X_L = \omega L$

By replacing either Z_2 or Z_4 with a capacitor & rest of the impedances with resistors,

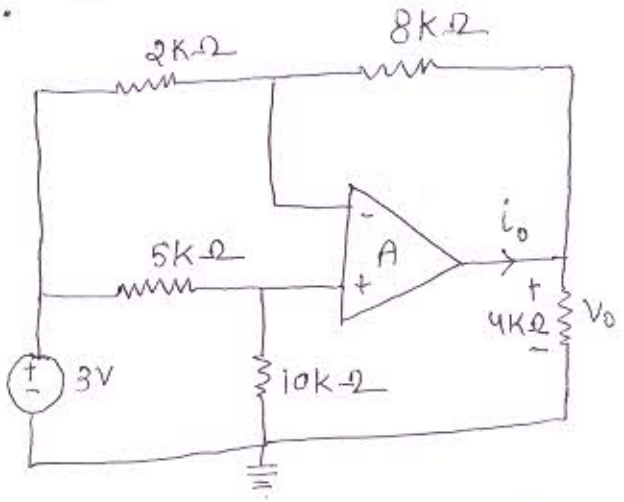
$$Z_{in} = \frac{R_1 R_3 R_5}{\frac{1}{\omega C_2} \cdot R_4} = \frac{\omega R_1 R_3 R_5 \cdot C_2}{R_4}$$

Comparing it with X_L

$$\boxed{L_{eq} = \frac{R_1 R_3 R_5 C_2}{R_4}}$$

Section - C

Q11. Design a second order Low pass filter with cut-off frequency 4KHz. Also obtain its frequency response curve. 4
for the circuit diagram given below find out the value of V_o and I_o.



Sol^n Designing of 2nd order Low pass filter :-

for a 2nd order LPF, frequency is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

Considering, $R_1 = R_2$ & $C_1 = C_2$ 1

$$f = \frac{1}{2\pi RC}$$

Selecting $C = 0.1\,\mu f$ for $f = 4KHz$ (given)

$$4000 = \frac{1}{2\pi R \times 0.1 \times 10^{-6}}$$

$$\boxed{R = 398.08\ \Omega}$$

for Non-Inverting configuration

$$A_f = 1 + \frac{R_f}{R_{in}}$$

for 2nd order filters Gain $A_f = 1.586$

$$\therefore \quad 1.586 = 1 + \frac{R_f}{R_{in}}$$

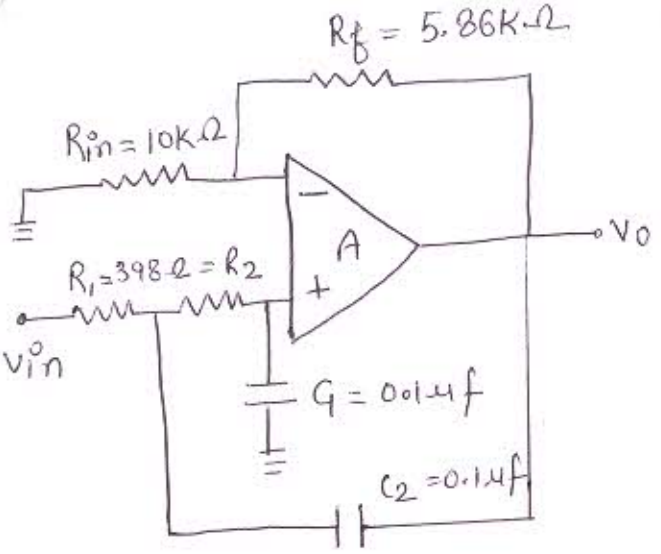
$$\text{or} \quad R_f = 0.586 R_{in}$$

Selecting $R_{in} = 10\,K\Omega$, $R_f = 5.86\,K\Omega$

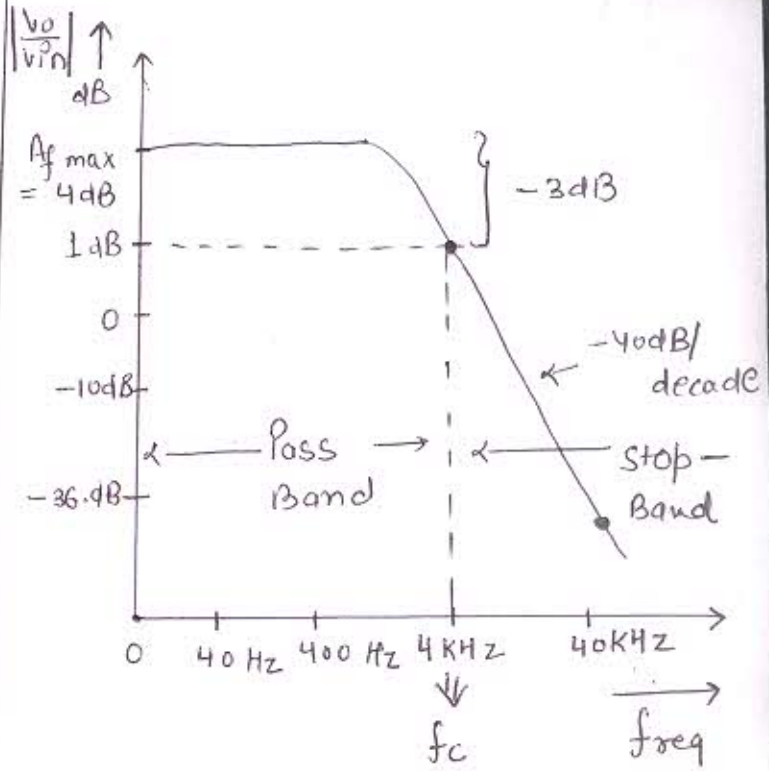
frequency response :- for 2nd order LPF -

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1 + (f/f_c)^4}}$$

f (Hz)	$\left\|\frac{V_o}{V_{in}}\right\|$	$20\log\left\|\frac{V_o}{V_{in}}\right\|$ dB
0	1.586	$4.006 \cong 4$
40	1.586	$4.006 \cong 4$
400	1.585	$4.005 \cong 4$
4000	1.121	$0.995 \cong 1$
40 KHZ	0.0158	$-35.99 \cong 36$



2nd Order LPF



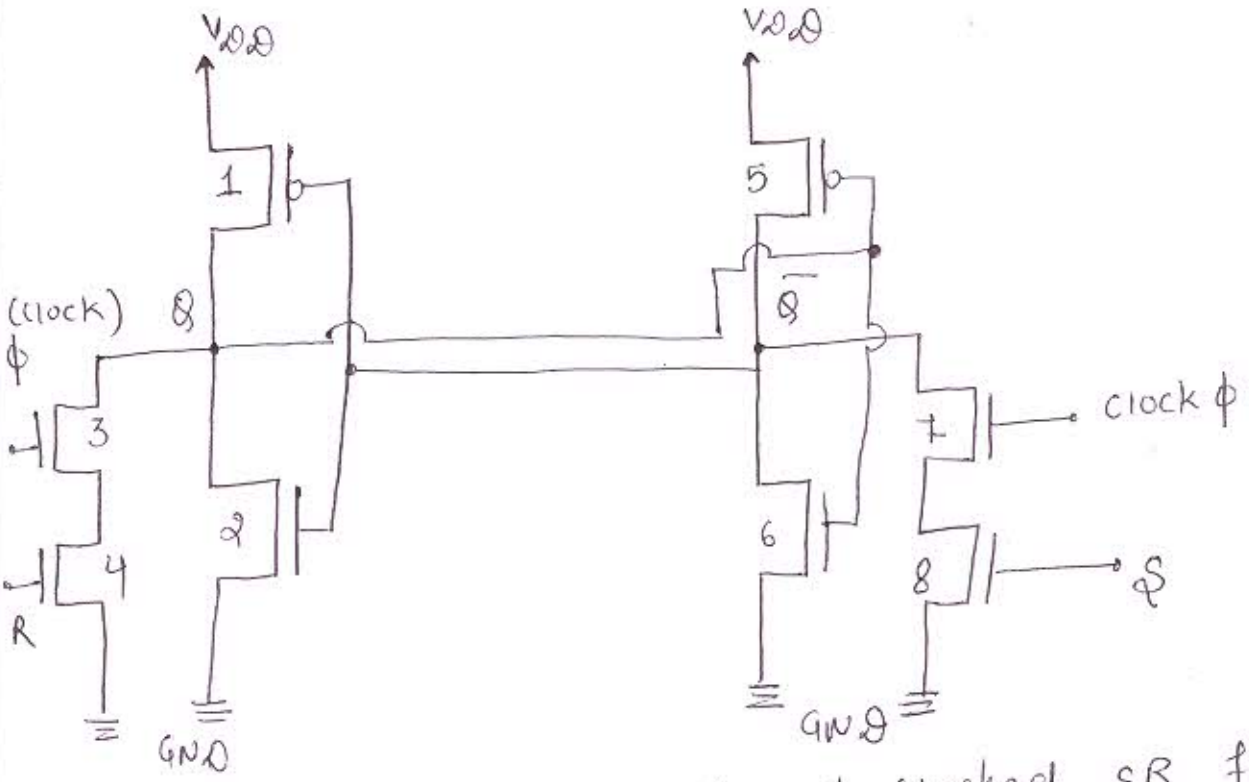
Frequency Response Curve for 2nd Order LPf at f_c = 4KHz

Q12. Why CMOS has less power dissipation. Draw CMOS implementation of clocked SR flip-flop circuit & explain its working operation.

Soln CMOS has Less power Dissipation :- CMOS is a combination of PMOS & NMOS. Both are complementary of each other. When PMOS works, NMOS remains in off mode & when NMOS works, PMOS remains in off mode. Power dissipation is of two types; static & dynamic. Static power consumption occurs if there exist a direct path between power supply & ground. In CMOS PMOS is connected to power supply & NMOS is connected to the Gnd. In

CMOS either PMOS are operating or NMOS are operating so, in CMOS there never exist a direct path between power supply & ground. & therefore static power consumption is ideally zero. That is why CMOS has only one (dynamic) type of power consumption & has least power dissipation.

Clocked SR-flip-flop :-



CMOS Implementation of clocked SR flf

For the flip-flop to be Set or Reset, clock should be high always.

Case I :- $R = 1$, $S = 0$, $\phi = 1$

For this input combination, M_4 & M_3 will work & output Q will connect to the Gnd & it will become 0. Due to that M_5 will turn ON & will make $\bar{Q} = 1$

$\bar{Q} = \bar{0} = 1$ } RESET condition
$Q = 0$ }

Case II :- R = 0, S = 1 & Φ = 1

for this input combination M7 & M8 will turn ON & make $\bar{Q} = 0$. Due to this M1 will turn ON & make $Q = 1$. It will set the flip-flop.

$\bar{Q} = 0$
$Q = 1$ } SET condition

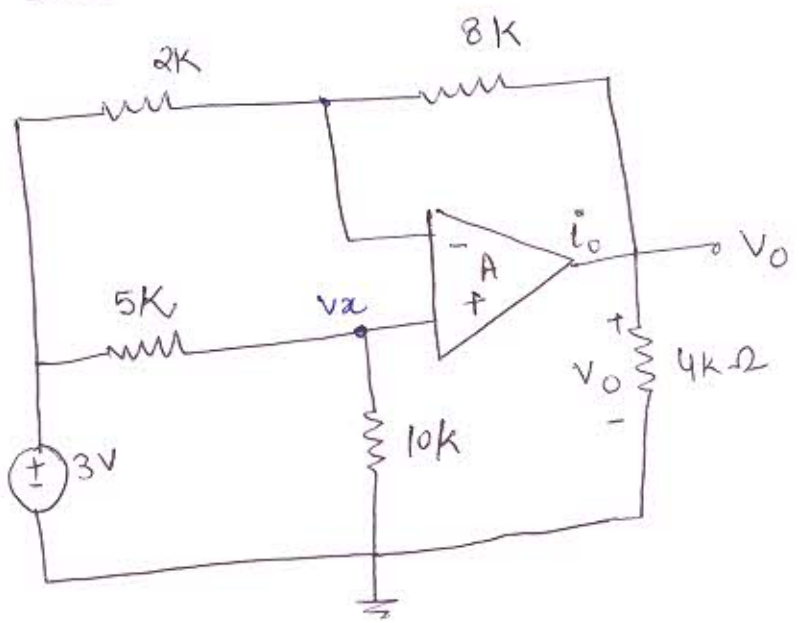
Case III :- R = 0, S = 0, & Φ = 1

for this input combination flip-flop continues the previous state. If it was in SET state then it will maintain its SET state, or if it was previously in RESET state it will hold that state.

Cas IV :- R = 1, S = 1, Φ = 1

This is invalid condition. for this input combination both Q & $\bar{Q}$ tends to become '0', which is not possible. Therefore this combination is prevented.

Q11 (b) Numerical :-



$V_o = ?$
$I_o = ?$

Given circuit is a subtractor with $V_1 = V_2 = 3V$.

$$\therefore \quad V_o = V^+ + V^-$$

$$V^+ = \left(1 + \frac{R_f}{R_{in}}\right) V_{in} \qquad \{V_{in} = V_x\} \text{ (Non-Inverting)}$$

$$V^+ = \left[1 + \frac{8}{2}\right] \cdot \frac{3 \times 10}{10 + 5} \qquad \{\text{Applying potential divides at } V_x\}$$

$$V^+ = 5 * 2 = 10V$$

$$V^- = -\frac{R_f}{R_{in}} \cdot V_{in} \quad \text{(Inverting)}$$

$$= -\frac{8}{2} * 3 = -12V$$

$$\therefore \quad V_o = 10 + (-12)$$

$$\boxed{V_o = -2V} \quad \text{Ans.}$$

$$I_o = \frac{V_o}{R} = \frac{-2V}{4k\Omega}$$

$$\boxed{I_o = -0.5 \text{ mAmp}} \quad \text{Ans.}$$