Ajay Kumar Garg Engineering College, Ghaziabad

Department of CSE

Model Solution- ODD Semester (2017-18)

Sessional Test -2

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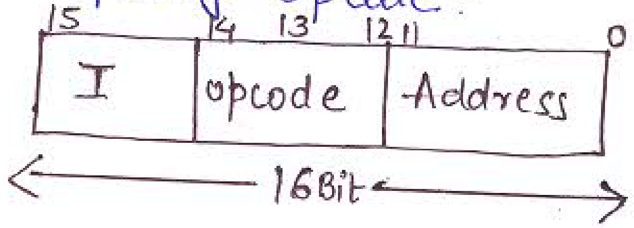
Section - A

Q1 → What are Memory Reference instruction. How many bits are required for mode, opcode, and address in Memory Reference instruction.

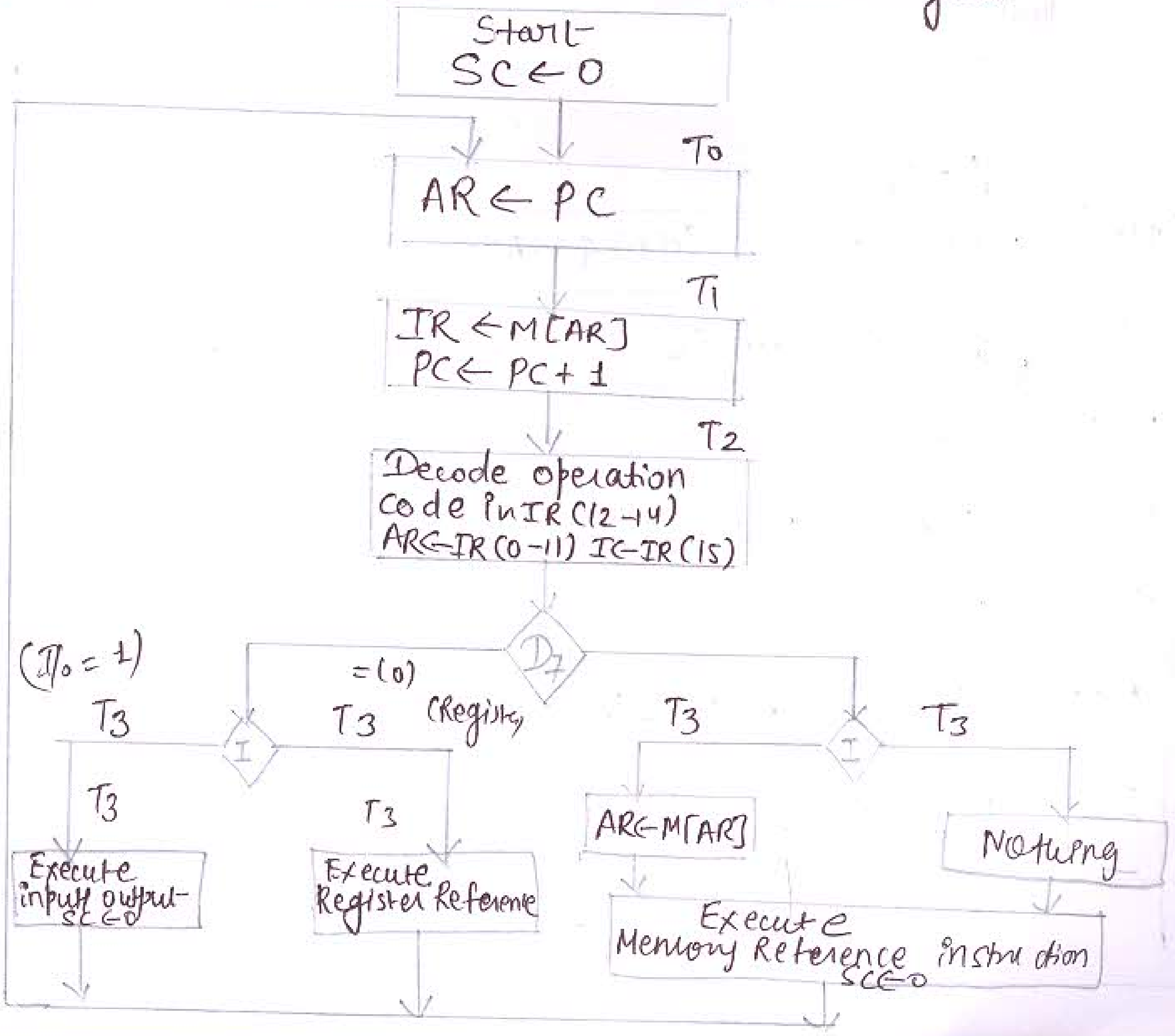
Ans1 In Basic computer has three instruction code formate one of them is Memory Reference instructions.

A memory Reference instruction use 12 bit to specify an address and one bit to specify the addressing mode. 3 Bit to specify opcode:



(opcode =000 to 110)

Q2 Draw the flowchart of Instruction cycle



Q3→ Explain Dirty / Modified Bit concept. How this concept is used in write Back cache.

sol for write operation, the system proceed in two ways. In the first technique called write through protocol, the cache location and the Main Memory location are updated Simultaneously. The second technique is to update Only the cache location and Mark it updated with an associated flag bit often called as Dirty / Modified bit.

The Main Memory location updated later, when the Block containing this Marked word is to be removed from Cache to make room for a new Block.

This technique is called write Back / copy Back protocol

Q4 Describe the Steps of Execution of complete instruction of operation Add(R_3), R_1.

	Action
1	PCout, MARin, Read, Select4, Add, Zin
2	Zout, PCin, Yin, WMFC
3	MDRout, IRin
4	R_3out, MARin, Read
5	R_1out, Yin, WMFC
6	MDRout, Select Y, Add, Zin
7	Zout, R_1in, End.

Q5- A computer has 256KByte, 4 way set associative Write Back Data cache with Block size of 32 bytes The Processer send 32 bit address to tue cache controller. Each tag directory Entry contain , in addition to address tag 2 bit, 1 Modified bit, 1 Replacement bit, find tue number of bit in tue tag field of an address ?

Sol A computer have 256 K Byte cache 4 way set associative

Block size = 32 Byte

Tag	Set	word
16	11	5

← 32 bit →

Total number of Blocks $= \frac{256 \text{ KByte}}{32 \text{ Byte}}$

$= \frac{2^8 \times 2^{10}}{2^5} = 2^{13}$

Total number of set $= 2^{13}/2^2 = 2^{11}$

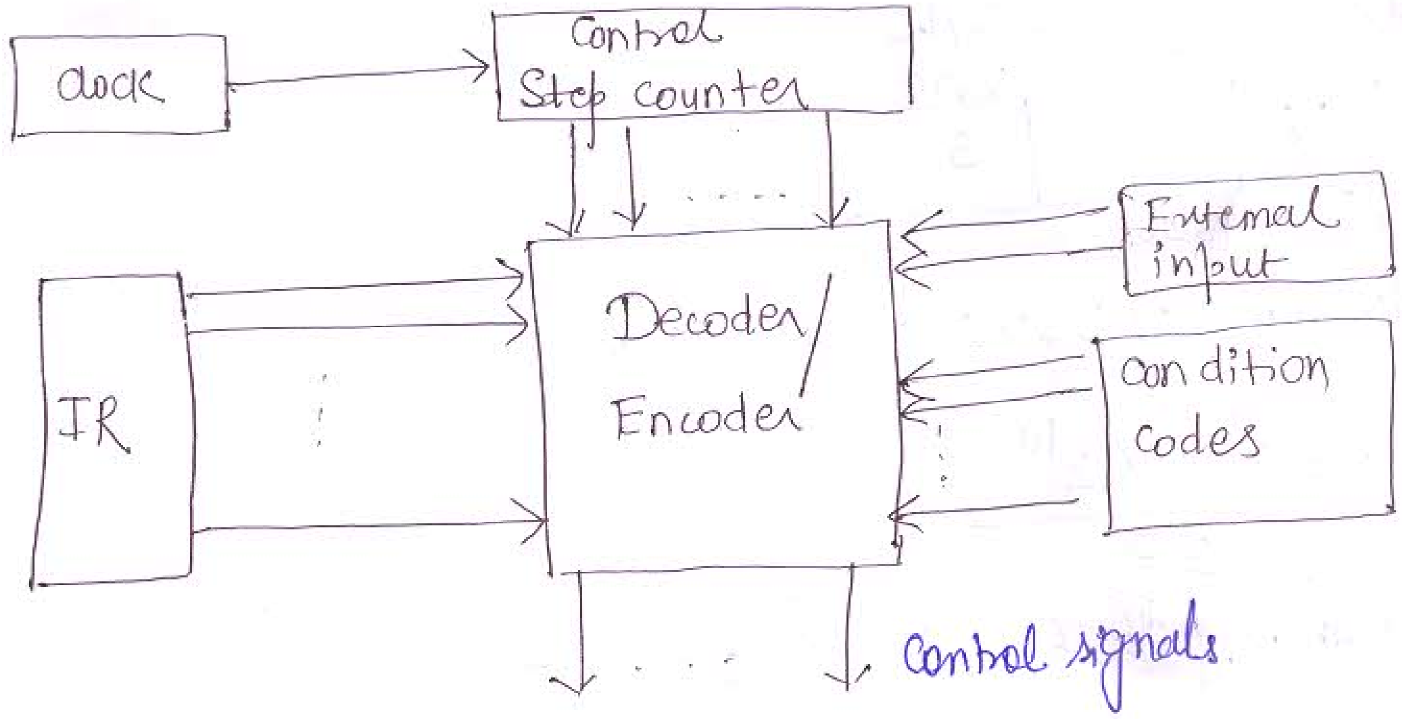
Total number of tag bits $= 32-(11+5) = 16$ Bit.

Section - B

Q6 → Describe Hardwired Control unit with Block diagram.

Solution To Execute an instruction, the Processor must have some mean of generating the control signals needed in proper sequence. the computer designer have a wide Variety of technique to solve this Problem.

The approach used fall in one of two categories are hardwired control and Microprogrammed control



Hardwired control organization

Each Step in this sequence is completed in one clock Period.

- A counter used may used to keep track a control Step.

Each state or count of this counter correspondes to one control step.

The required control signals are determined By the following information

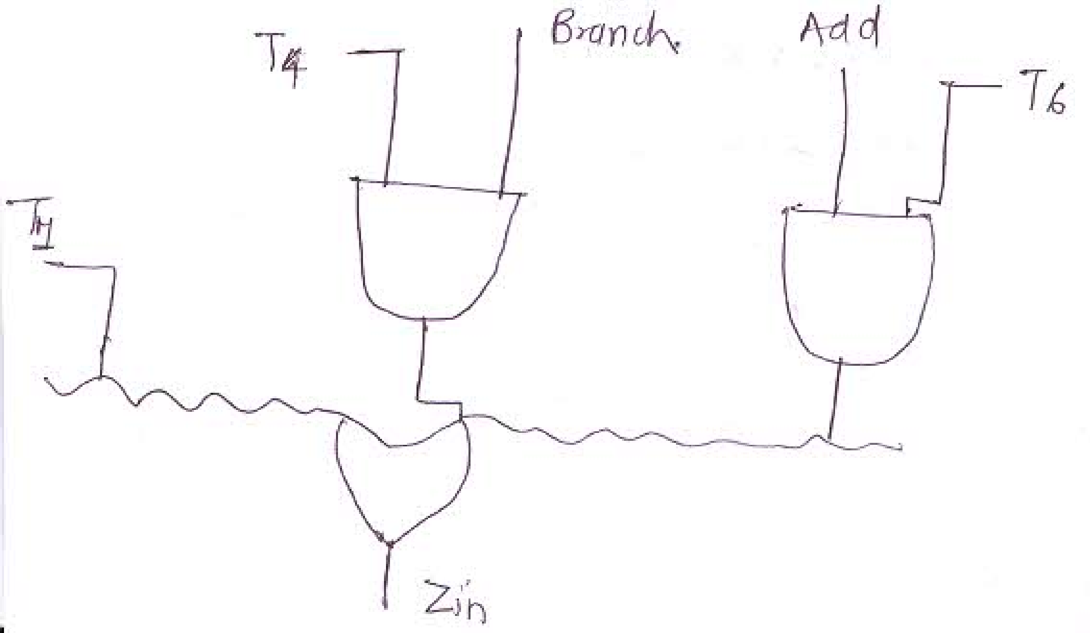
- Content of the control step counter.
- Content of the Instruction Register.
- Content of condition code flag.
- Extend input signals, such as MFC or interrupt request.

The output of instruction decoder consist of separate line for each Machine instruction., for any instruction loaded in IR, one of the output line INS_1 through INS_2 is set to 1 and all other line are set to 0.

An Example how the Encoder generate the control signal

$$\boxed{Z_{in} = T_1 + T_6 \cdot Add + T_4 \cdot BR}$$

The signal generated is asserted during timeslot T_1, for all instruction, during T_6 for an Add instruction, during T_4 for an unconditional Branch Instruction and so on.



(7) Consider 4way set associative cache with total 16 cache Block. The main memory Consist of 256 Block and the request of Memory Block is in the following order 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155, which of the memory Block will not be in cache if LRU Replacement policy is used.

Sol 4way set associative cache with total of 16 cache Block.

Total number of set are 4.

0	~~0~~ 48	~~4~~ 32	8	~~216~~ 92
1	1	133	73	
2				
3	~~255~~ 155	3	159	63

The Every memory Block request has been Putted to Respective Cache location by taking Mod with 4 for Every memory Block request. After Applying LRU Replacement Policy, the blocks that are not in cache are given Below. 0, 4, 216, 255

(1) 0 % 4 = 0

(2) 255 % 4 = 3

(3) 1 % 4 = 1

(4) 4 % 4 = 0

(5) 3 % 4 = 3

(6) 8 % 4 = 0

(7) 133 % 4 = 1

(8) 159 % 4 = 3

(9) 216 % 4 = 0

(10) 129 % 4 = 1

(11). 63 % 4 = 3

(12) 8 % 4 = 0 (hit)

(13) 48 % 4 = 0 (full Replace with LRU Policy here from Zero)

(14) 32 % 4 = 0

(15) 73 % 4 = 1

(16) 92 % 4 = 0

(17) 155 % 4 = 3

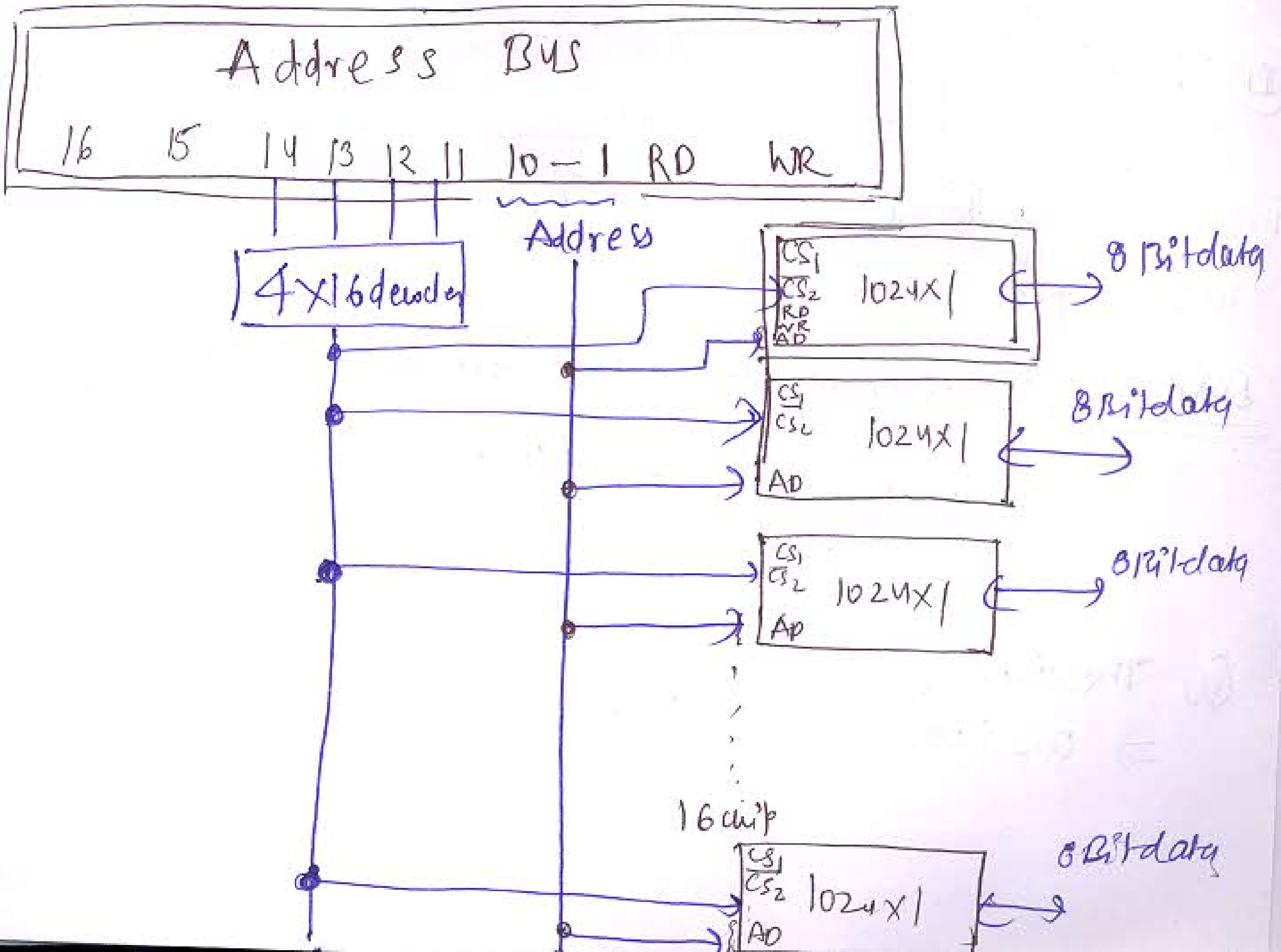
Q8 A Computer use RAM chip of 1024*1 capacity
(i) How many chips are needed to provide the memory capacity of 16KB? Explain in word how the chip ale tobe connected to the address Bus?
(ii) How many chip are needed and how should their addren line be connected to provide a memory capacity of 1024*8?

Sol → (1) 1024 X1 capacity RAM

Total number of chips needed = $\frac{16KB}{1024X1}$

$$= \frac{2^4 \times 2^{10} \times 8}{1024 \times 1} = \frac{2^{14} \times 8}{2^{10} \times 1} = 2^4 \times 8 = 128 \text{ chips.}$$

10 lines specify the chip address (1024X1) and 4 lines are decoded into 16 chip select input



(ii) 1024×8

$\frac{1024\times8}{1024\times1}$ = 8chip are required.

The 8 chip are needed with address line Connected in parallel.

Q9 The Access time of a cache memory is 100 ns and that of Main memory 1000ns. It is estimated that 80 Percent of memory request is for Read and Remaining 20 percent for write. The hit ratio for read access only is 0.9.

A write through Procedure is used

(i) What is the average Access time of the system Considering only memory read cycle.

(ii) What is the average Access time of the system for read and write request.

(iii) What is the hit ratio taking into consideration the write request/cycle.

Solution (i) the Average Access time For read request →

$\Rightarrow 0.9 \times 100 + 0.1 \times (100ns + 1000ns)$

$\Rightarrow 200ns.$

(ii) The Average Access time for read and write Request.

$\Rightarrow 0.2 \times 1000ns + 0.8 \times 200ns = 200 + 160$

$= 360ns$

(pii) To take into consideration write cycles means that given overall hit ratio.

To take into consideration write cycles means that we should discard write requests from the given overall hit ratio.

So we have hit-ratio_read = read request_percentage X hit ratio = 0.8 X 0.9 = 0.72.

Q10 Briefly define the following term-

(i) Microperations (II) Micro-Instruction (iii) Microprogram (iv) Microcode (v) Control Memory.

(1) Microperation → A Elementary digital computer operation are detailed low level instruction used in some design to implement complex Machine Instruction.

(2) Microinstruction - Microinstruction are the instruction stored in control Memory.

A microinstrution is simple command that make the hardware operate properly.

(3) Micropregram → sequence of Micro instruction (set of Microinstruction in a cpu, used to implement Machine instruction)

(4) Micro code - A Microcode is a layer of hardware level instruction. The collective Microprogram in a cpu used to run Machine instruction

(5) Control Memory - control Memory is assumed to be a RoM, within which all control information is Permanently stored.

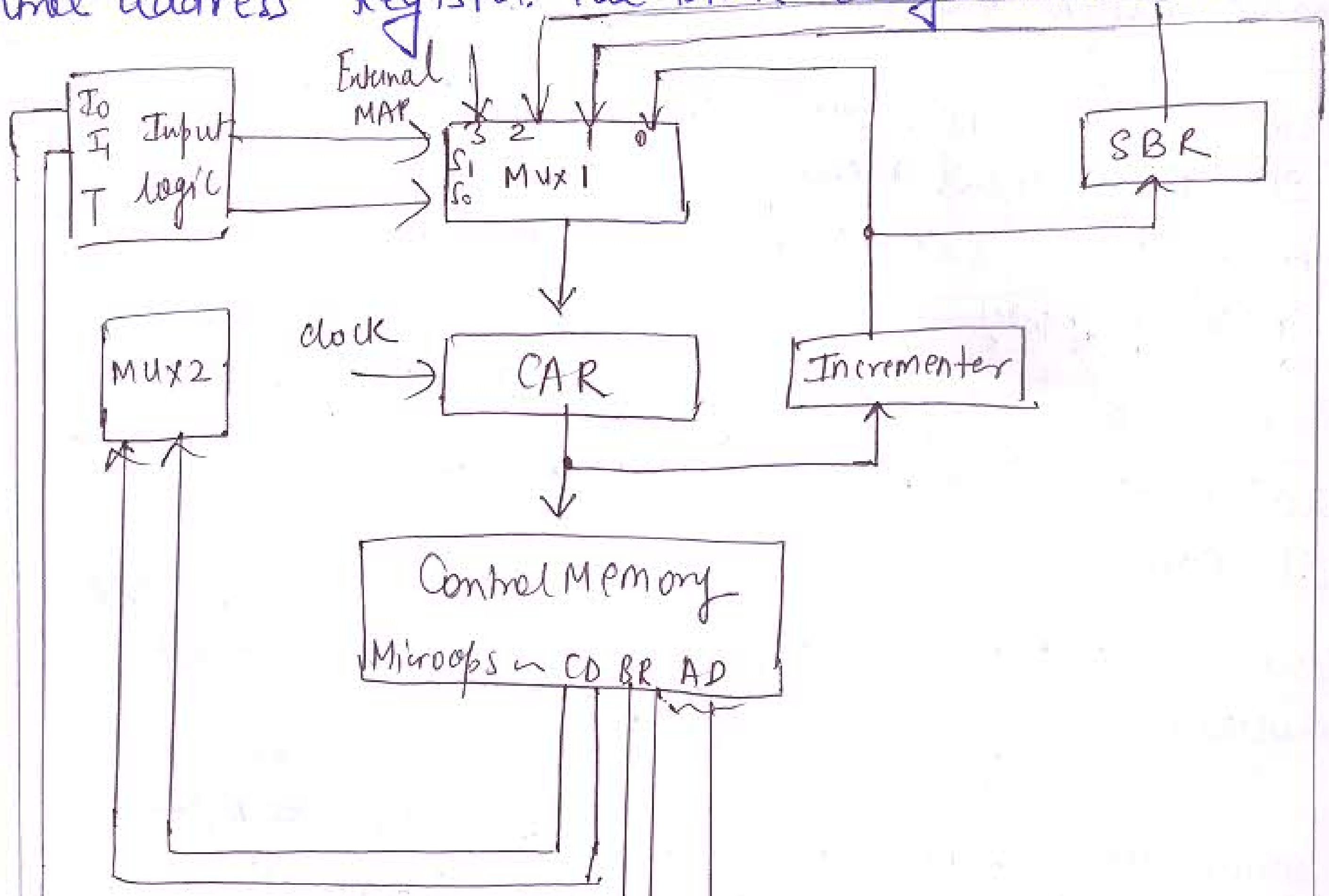
Section C

(11) what is Micro program sequencer. Explain in Details with diagram.

Sol The Basic concept of Microprogramm control unit are the control Memory and the circuit that select the next address. the address selection part is Micro-programm sequencer.

The purpose of Microprogram sequencer is to Present an address to the control Memory. so that Microinstruction may be read and Executed.

The next address logic of the sequencer determine the specific address source to be loaded into the Control address Register. the Block diagram shown Below.



Micro program Sequencer Block diagram

Micro program sequencer block diagram shown above - let's discuss its working.

These are two Mux in detail

1st Mux Sect an address from one of the four source and route it into a control address register

The second Mux test the value of selected status Bit and result of test is applied to an input Register / logic ckt.

The output from CAR provide the address from control Memory.

the content of CAR is incremented and applied to one of the Multiplexer input and to the Subroutine Register (SBR)

the other three input to MUX1 come from Address field of the present Microinstruction, from the output of SBR, and from external source that MAP the instruction.

the CD (condition) field of the Micro instruction select one of the status Bit in the second Multiplexer.

If the Bit selected is equal to 1. the test (T) variable is equal to 1, otherwise equal to zero.

The T value together within the two Bit from BR (Branch) field go to an input logic ckt. The input logic in a particular sequencer will determine the type of operation are available in the unit.

Design of Input logic

The Input logic ckt has three input I_0, I_1, T and three output S_0, S_1 ... and T. variable S_0 and S_1 select one of the source address for CAR Variable 2 enable the load input in SBR.

The Binary value of the two selection variable determine the path in the Multiplexers. for Example with $S_1 S_0 = 10$, the multiplexer input number 2 is selected and establish a transfer path from SBR to CAR. Note that Each of the four input as well as the output of Mux 1 Contain Bit address. The truth table for the input logic ckt Input I_1 and I_0 are identical to the bit value in the BR field.

BR field	Input I_1 I_0 T	MUX1	load SBR
00	0 0 0	0 0	0
00	0 0 1	0 1	0
01	0 1 0	1 0	0
01	0 1 1	1 1	1
10	1 0 X	1 0	0
11	1 0 X	1 1	0

Truth table

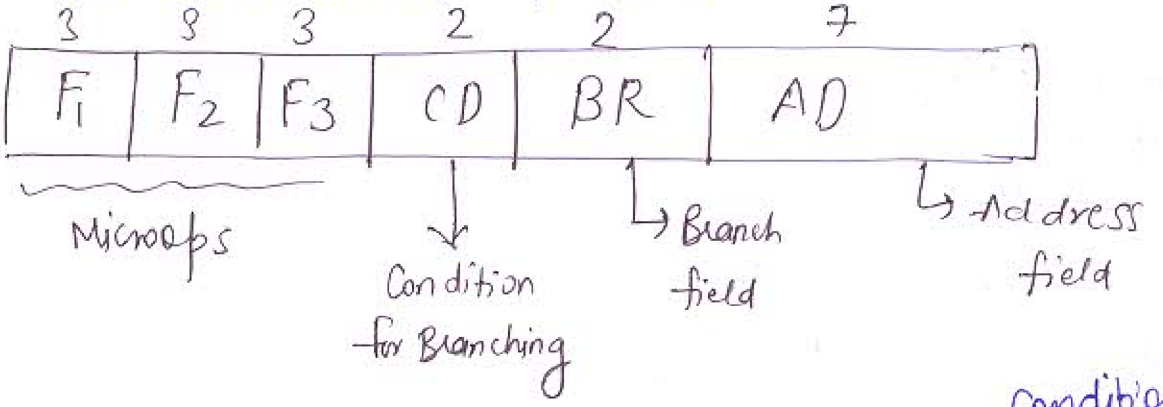
$S_1 = I_1$

$S_0 = I_1 I_0 + I_1' T$

$T = I_1' I_0 T$

Condition field

The field consist of two Bit which are Encoded to Specify four status Bit condition are listed, The first condition is always a 1, so that Reference to CD = 00 (asymbol o)



Condition Bits

CD	Condition	Symbol	Comment
00	Always 1	U	Unconditional Branch
01	DR(15)	I	Indirect Address
10	AC (15)	S	Sign bit of AC
11	(AC = 0)	Z	Zero value in AC.

Branch Bits

BR	Symbol	function

00	JMP	CAR ← AD if condition = 1
		CAR ← CAR+1 if condition = 0

01	CALL	CAR ← AD, SBR ← CAR+1
		if condition = 1

10	RET	CAR ← SBR if condition = 1
11	MAP	

Q12 Explain Rifferent Kind of cache mapping with Example ? what is the limitation of direct mapped cache.

Ans there are three different type of cache mapping namely.

→ Associative mapping
→ Direct mapping
→ set Associative mapping

Cache Mapping → first we will discuss about what ~~is~~ we mean By cache Mapping. cache Mapping is technique through which we can Map a main memory Block into a cache memory As we know cache memory is of small size, Very limited number of Block can be reaide in cache, So we need to place a Block in cache in order to Enchance hit ratio. and Acces time. ~~to~~ There are three type of mapping

① Associative Mapping → Associative mapping is costly But a fast mapping technique. A cpu address of 15 Bit is placed to the argument Register and associative Memory is searched for Matching Addren.

↓ cpu addren (15 Bit)

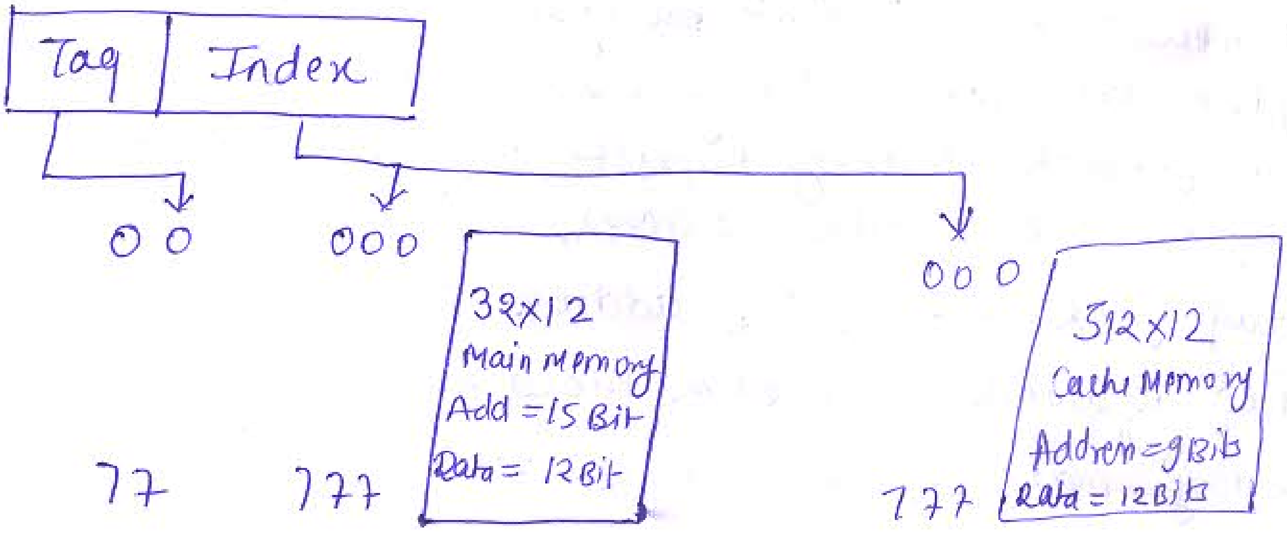
Arugment Register

Address	Data
0100	3450
02777	6710
2345	1234

Tag	Word

If the address is found; the corresponding 12 Bit data is read and sent to the cpu. If no match occur, the Main memory is accessed for word. The address - data pair is then transferred, to associative Cache memory. Cache is full an address - data pair must be displaced to make room for a Pair that is needed and not presently in the Cache. The decision as to what pair is replaced. is determined from the replacement algorithm that designer choose for the cache.

② Direct Mapped cache -



Direct Mapping technique Representation

Associative Memory are Expensive compared to Random Access memories B/c of added logic associated with each cell.

The cpu address of 15 Bit is divided into two field The nine least significant Bit constitute the index and remaining six from tag field.

The figure Shows Main Memory needs an Address that Includes Both tag and the index Bit. the number of Bits in the index field is equal to the number of address Bit required to acess cache Memory.

The general 2^k word in cache Memory and 2^n word in Main Memory. the n bit memory address is divided into two field K bit for the index field and n-K bit for the tag field, n bit to acces main memory.

Each word in cache consist of the data word and its associated tag.

When a new word is first Brought into the cache the tag Bit are stored along side the data Bit, when the cpu generate memory Request the index field is used for the address to access the cache.

The tag field of the cpu address is compared with the tag in word read from the cache.

If two tag matches there is a hit and desired data word is the cache.

If there is no Match there is a Miss and the required word is read from Main Memory.

The Disadvantage of Direct Mapped Cache

The direct Mapped is that the hit ratio can drop ~~[illegible]~~ considerably, if two or more word whose address have the same index, But different tag are accessed Repedeatly.

③ Set Associative Cache Memory

The third type of cache Memory is set - associative mapping, is an Improvement over Direct organization, in that Each word of cache (can store two or omore word of memory under the same index address)

Each data word is stored together with its tag and number of tag data item in one word of cache is said to form a set.

An Example of set associative cache organization of size two shown Below

	Tag	Data		Tag	Data
000	01			02	5670
777	02	6710		00	2340

More than two tag can reside on the same index

———— X ————