Ajay Kumar Garg Engineering College, Ghaziabad

Department of CSE

Sessional Test-2

Course:	B.Tech	Semester:	V
Session:	2017-18	Section:	CS1,CS2,CS3
Subject:	Computer Architecture	Sub. Code:	NCS-505
Max Marks:	50	Time:	2 hour

Note : Answer **all** the Sections.

Section-A

A. Attempt **all** the parts. **(5 X 2 = 10)**

(1) What are Memory Reference instructions.How many bits are required for mode,opcode and address in memory reference instruction.

(2) Draw the Flowchart of Instruction Cycle.

(3) Explain Dirty/Modified bit concept.How this concept is used in write back cache.

(4) Describe the steps of execution of complete instruction for the operation, Add(R3),R1

(5) A computer has a 256K Byte, 4 way set associative , write back data cache with block size of 32 bytes. The processor sends 32 bit address to the cache controller. Each cache tag directory entry contain , in addition to address tag, 2 valid bit , 1 modified bit , 1 replacement bit . Find the number of bit in the tag field of an address ?

Section-B

B. Attempt **all** the parts. **(5 X 5 = 25)**

(6) Describe Hardwired Control Unit with block Diagram.

(7) Consider a 4 way set associative cache (initially empty) with total 16 cache block. The main memory consist of 256 blocks and the request of memory block is in the following order : 0,255,1,4,3,8,133,159,216,129,63,8,48,32,73,92,155. Which of the memory block will not be in cache if LRU Replacement policy is used(Specify block number).

(8) A computer use RAM chip of 1024*1 capacity

i) How many chip are needed to provide the memory capacity of 16 KB? Explain in words how the chips are to be connected to the address bus.

ii) How many chip are needed and how should their address line be connected to provide a memory capacity of 1024*8.

(9) The access time of a cache memory is 100 ns and that of the main memory 1000ns. It is estimated that 80 percent of the memory request are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.

i) What is the average access time of the system considering only memory readcycle.

ii) What is the average access time of the system for read and write requests.

iii) What is the hit ratio taking into consideration the write cycles.

(10) Briefly define the following terms:

i) Micro Operation ii) Micro Instruction iii) Microprogram iv) Micro Code v) Control Memory

Section-C

C. Attempt **all** the parts. **(2 X 7.5 = 15)**

(11) What is Microprogram sequencer. Explain in detail with diagram

(12) Describe various types of Cache mapping in detail with Example ?What is the limitation of Direct mapped cache.