Ajay Kumar Garg Engineering College, Ghaziabad

Department of ECE

Model Solution ST-2

Course: B.Tech
Session: 2017-18
Subject: Analog & Digital Electronics
Max Marks: 50

Semester: 3rd
Section: EN-1 & EN-2
Sub. Code: REC-309
Time: 2 hours

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SECTION – A

Q1 :– Write down the advantages of negative feedback.

Soln –:
1. It desensitize the gain.
2. It reduces non-linear distortion.
3. It controls I/P & O/P impedance.
4. It extends bandwidth of the amplifies.

Q2 :– Give the applications of Multiplexer.

Soln –:
1. In designing combinational circuits.
2. As a data selector
3. In D/A converter.
4. In communication purpose.

Q3 –: What is Barkhausen Criteria.

Soln –: A small change in DC power supply in oscillator ckt can start oscillation & to maintain oscillations the ckt must satisfy Barkhausen criteria.
It states that the loop gain is equal to unity
i.e. $|A\beta| = 1$.

Q4-: Differentiate between Combinational and Sequential circuits.

Soln:- Combinational circuits performs arithmetic & logical operations which don't have memory element in it while sequential circuits stores binary data in the memory element attached in its feedback.

The combinational ckt o/p depends only on the present input while the output of sequential ckt depends not only on the present i/p but also on past output.

Examples: Combinational ckts: Adders / Substractors
MUX / DEMUX
Encoders / Decoders

Sequential ckts: Flip flops, Registers, Counters.

Q5-: Name two Piezoelectric Materials used in the construction of crystal oscillator.

Soln:- (1) Quartz
(2) Rochelle Salt

SECTION - B

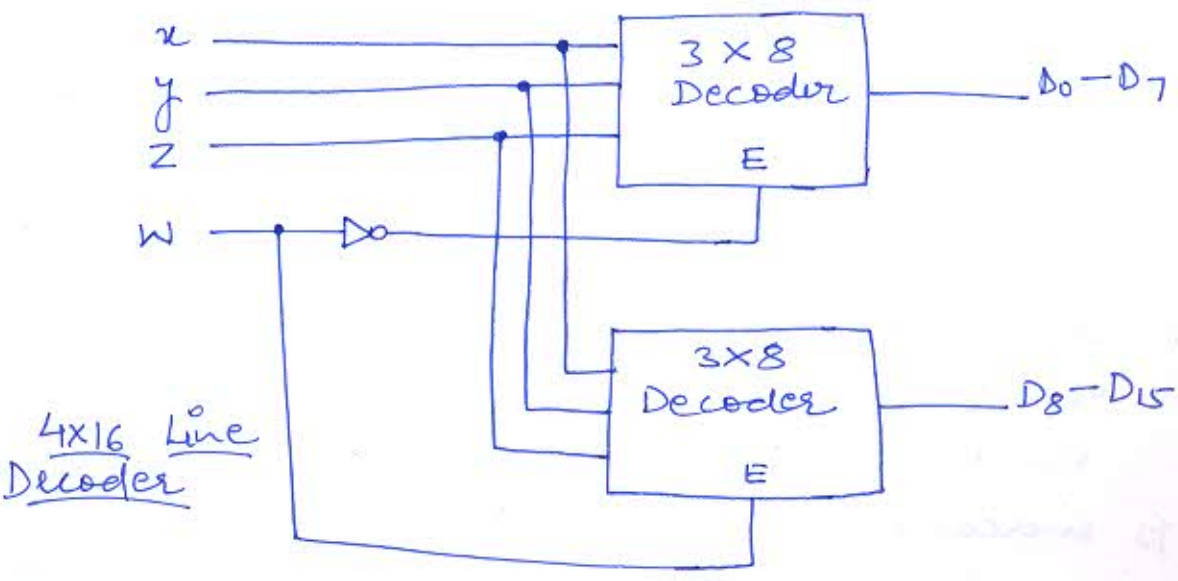
Q6 – List 5 characteristics of an amplifier modified by negative feedback.

Soln :–

1. It makes the value of the gain less sensitive to variations in the value of circuit components, such as might be caused by changes in temp^{n}.
2. It makes the output proportional to the input or make the gain constant, independent of s/g level.
3. It minimizes the contribution to the output of unwanted electric signals generated either by the circuit components themselves, or by interference.
4. It raises or lower the input and output impedance by the selection of an appropriate feedback topology.
5. It extends the bandwidth of the amplifier.

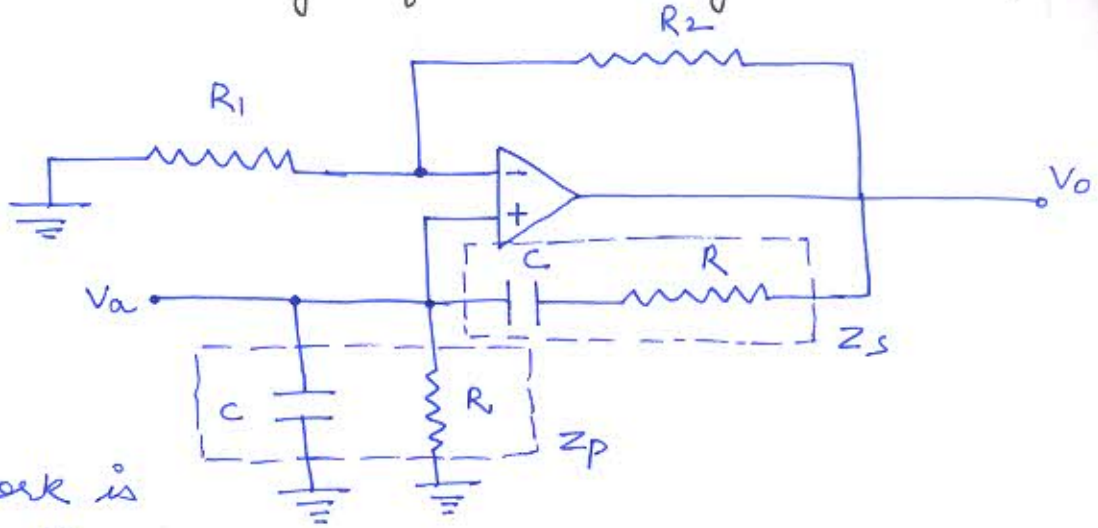
Q7 – Explain Decoders. Realize a 4X16 decoder using two 3X8 decoders.

Soln :– Decoders are combinational logic circuits that converts binary information from n input lines to a maximum of 2^n output lines.
These decoders are n to m line decoders where $m \leq 2^n$.



Q8 :- Discuss the working of Wien-Bridge Oscillator.

Soln :-



→ An RC network is connected in the feedback path of this positive gain amplifier.

→ The loop gain is given by

$$L(s) = \frac{1 + R_2/R_1}{3 + sCR + 1/sCR}$$

The loop gain will be a real no. (phase will be zero) at one freq. given by

$$\omega_0 CR = \frac{1}{\omega_0 CR}$$

i.e. $$\omega_0 = \frac{1}{CR}$$

To obtain sustained oscillations at this freq., one should set the magnitude of the loop gain to unity. This can be achieved by selecting

$$R_2/R_1 = 2$$

However, the Wien-bridge oscillator has two limitations -

(1.) It can be used only for relatively low freq. generation (1–5 kHz).

(2.) It has a high degree of distortion due to the use of diodes, which saturates the amplitude and hence creates non-linearity.

To overcome this problem, Twin-T oscillator is used.

Q-1 What is Priority Encoder? Explain it with its truth table and logic circuit.

Soln ⇒ It is an encoder circuit that includes the priority function. The operation of priority encoder is such that if two or more I/P are equal to 1, at the same time, the I/P having the highest priority will take precedence.

→ Apart from two O/P x and y, the ckt has a third O/P designated by V; this is a valid bit indicator that is set to 1; when one or more I/P are equal to 1.

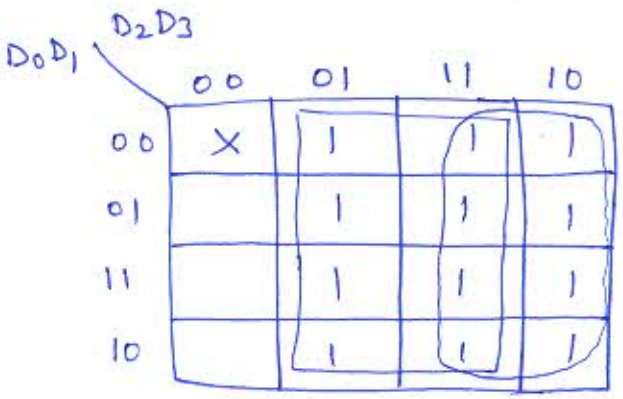
→ The truth table uses an x in I/P to represent either 1 or 0. Higher the subscript number, the higher the priority of the I/P.

→ Input D_3 has highest priority, D_2 has the next priority and then D_1 and D_0.

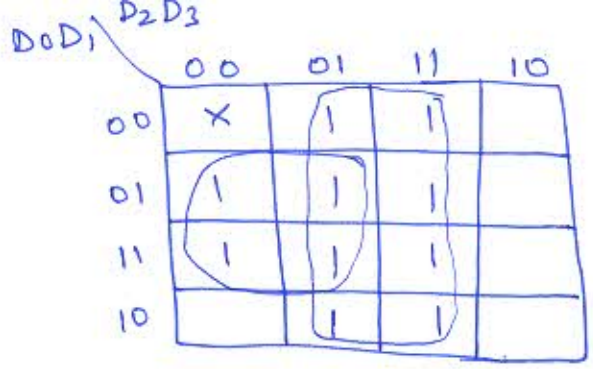
Truth Table :

Input				Output		
D_0	D_1	D_2	D_3	X	Y	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

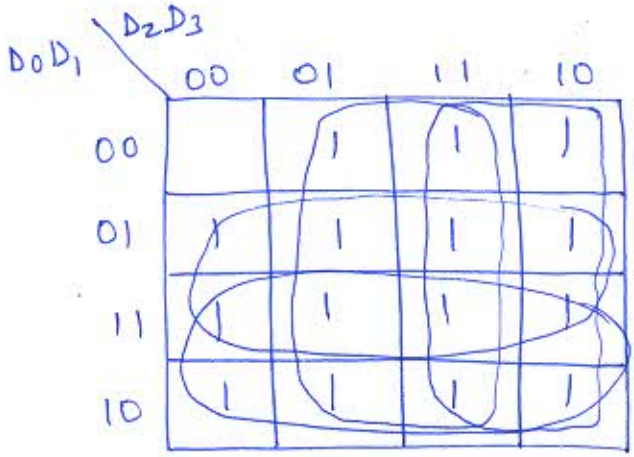
K-Maps :



$x = D_2 + D_3$

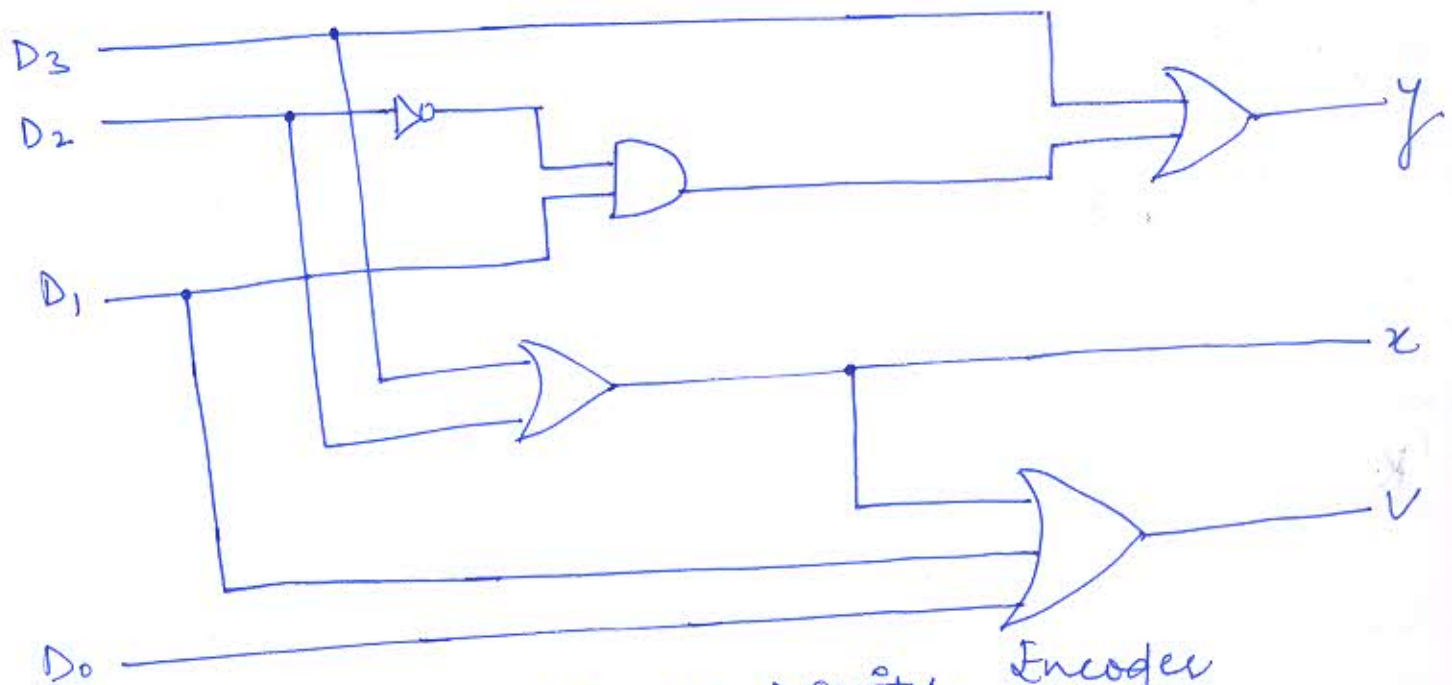


$y = D_3 + D_1\overline{D_2}$



$V = D_0 + D_1 + D_2 + D_3$

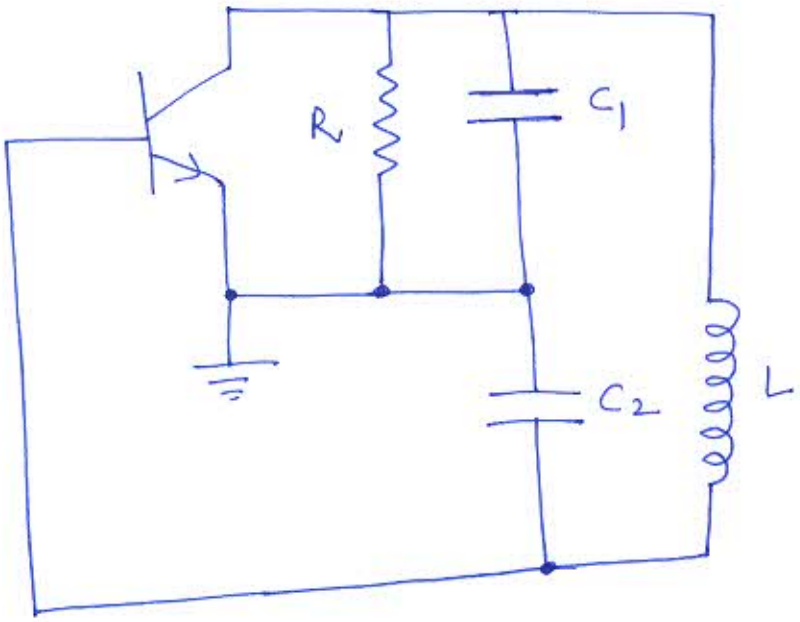
Logic Diagram:



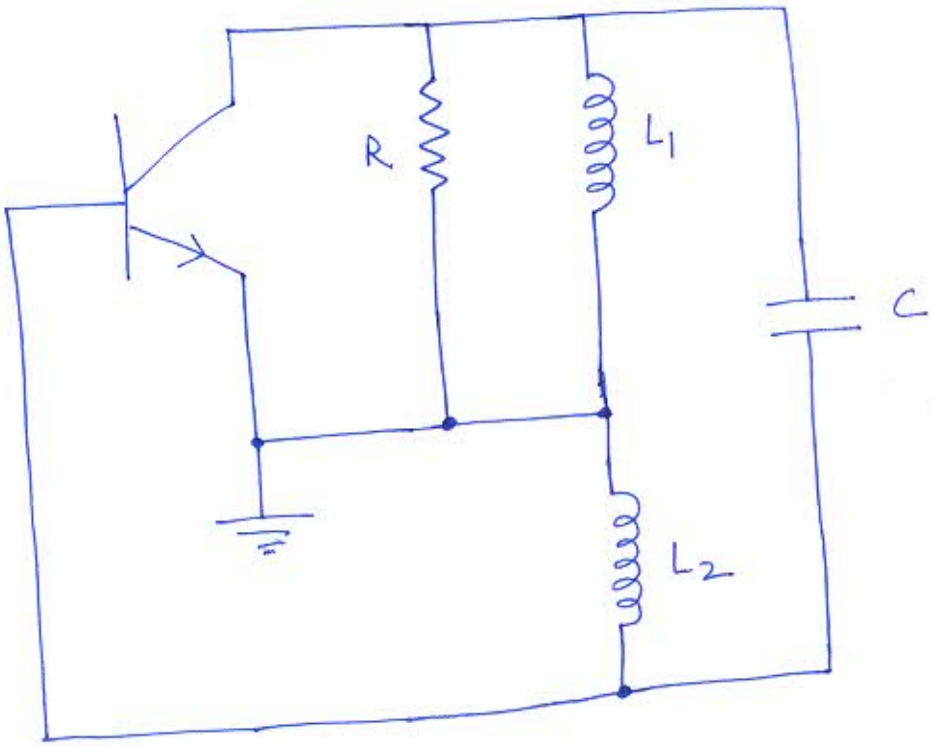
Four Input Priority Encoder

Q10)— Discuss how the circuit of Hartley oscillator differs from that of a Colpitts Oscillator.

Sol"):— The ckt. of Colpitts Oscillator is as under:



The ckt of Hartley Oscillator is as under:



→ The feedback is achieved by the way of a capacitive divider in colpitts oscillator and by the way of an inductive divider in the hartley oscillator.

→ If the freq. of operation is sufficiently low that we can neglect the transistor capacitances, the freq. of oscillation will be determined by the resonance freq. of the parallel tuned circuit.

Thus,

for Colpitts Oscillator, we've

$$\omega_0 = 1 \Big/ \sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}$$

for Hartley Oscillator, we've

$$\omega_0 = 1 \Big/ \sqrt{(L_1 + L_2)C}$$

SECTION-C

Q11-: What are Flip Flops? Find the Characteristic eq^n. of SR, D, JK and T flip flop with the help of k-Map.

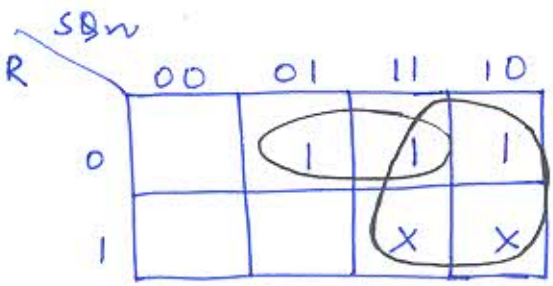
Sol^n -: Flip flops are the sequential logic circuits which has only two stable states. The basic unit of memory is the flip flop. The o/p of the flip flop is either 0 (logic 0) or +5V (logic 1). It's output depends not only on the present input but also on past output. It has a memory element attached in its feedback.

Characteristic Eq^n :-

(1.) **For RS Flip flop:** Truth Table

Flip flop Inputs		Present State	Next State	
R	S	Q_n	Q_{n+1}	
0	0	0	0	
0	0	1	1	
0	1	0	1	
0	1	1	1	
1	0	0	0	
1	0	1	0	
1	1	0	X	Indeterminate state
1	1	1	X	

Expression for Q_{n+1}

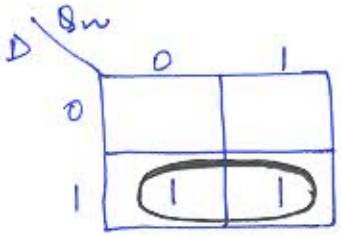


$$Q_{n+1} = S + \bar{R} Q_n$$

(2.) for D flip flop : Truth Table

Flip flop Input	Present state	Next state
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Expression for Q_{n+1}

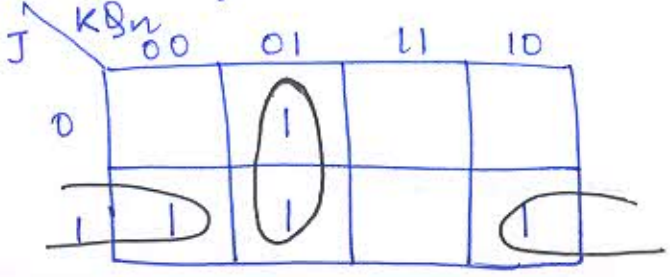


$$Q_{n+1} = D$$

(3.) for JK flip flop : Truth Table

Flip flop Inputs		Present state	Next state
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Expression for Q_{n+1}

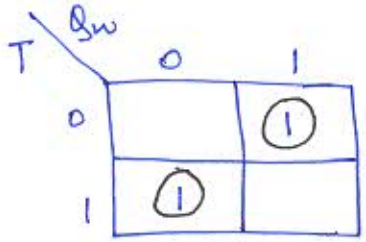


$$Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$$

(9) for T flip flop; Truth Table

Flip flop Input	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

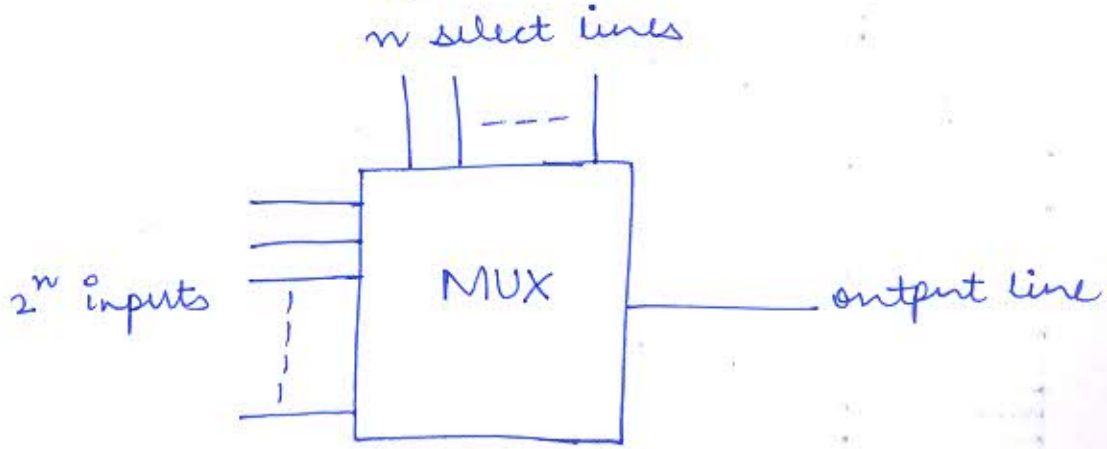
Expression for Q_{n+1}



$$Q_{n+1} = \bar{T}Q_n + T\bar{Q_n}$$

Q12:- Explain Multiplexers with an example. Implement the following boolean function using all 4:1 multiplexers. $F(A, B, C, D, E) = \Sigma m(0,1,2,3,6,8,9,10,13,15,17,20,24)$

Soln: Multiplexers are special type of combinational logic circuits. Its output is directed from one of the various inputs. The multiplexer is sometimes referred to as data selector which provides a no. of I/P one by one at a single output & which I/P will be out at any instant depends upon the status of selection line at that instant.



Example → 4 to 1 Multiplexer :

Truth Table

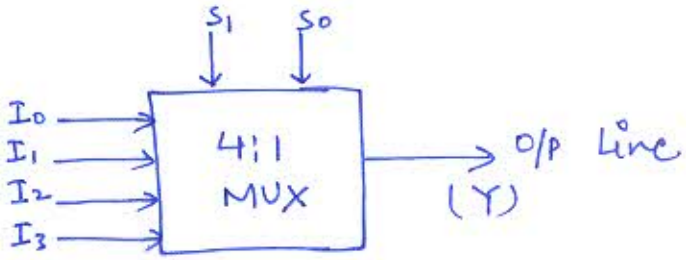
Enable Input	Select Lines		output (Y)
E	S_1	S_0	(Selected I/P)
0	X	X	0
1	0	0	I_0
1	0	1	I_1
1	1	0	I_2
1	1	1	I_3

$Y = I_0 \bar{S_1} \bar{S_0}$

$Y = I_1 \bar{S_1} S_0$

$Y = I_2 S_1 \bar{S_0}$

$Y = I_3 S_1 S_0$



Boolean Function Implementation :

Inputs	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
$\bar{A}$	(0)	(1)	(2)	(3)	4	5	(6)	7	(8)	(9)	(10)	11	12	(13)	14	(15)
A	16	(17)	18	19	(20)	21	22	23	(24)	25	26	27	28	29	30	31
I/P to MUX	$\bar{A}$	1	$\bar{A}$	$\bar{A}$	A	0	$\bar{A}$	0	1	$\bar{A}$	$\bar{A}$	0	0	$\bar{A}$	0	$\bar{A}$