AJAY KUMAR GARG ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGG.

SESSIONAL TEST – 2

Course	**: B. Tech.**	**Semester**	**: V**
Session	**: 2017-18**	**Section**	**: EN-1,2**
Subject	**: Microprocessor & its Applications**	**Sub. Code**	**: NEE-504**
Max. Marks	**: 50**	**Time**	**: 2hours**

Note: Answer all the sections.

Section A

A. Attempt all the parts **(5x2=10)**

(1) Identify the contents of the Accumulator and the Flag Status as the following instructions are executed: (H)

```
MVI A, 7FH
ORA A
CPI A2
```

(2) If the CS register contain the number 5ACEH and the IP contains the number FA3CH, what is the address of the instruction? (L)

(3) Draw the flag Register of 8086 MPU. (M)

(4) Differentiate between PC and SP Registers (L)

(5) What is instruction queue? What happens when branch instruction comes? (M)

Section B

B. Attempt all the parts **(5x5=25)**

(6) Sixteen bytes of data are stored in memory locations at 0050H to 005FH. Transfer the entire block of data to new memory locations starting at 0070H. (M)

(7) Explain the various addressing modes of 8085 Microprocessor with a suitable example. (H)

(8) Explain the following instructions: (H)

i. MOV CS: TOTAL [BP], AX

ii. MOVSB

iii. XCHG

iv. AAA

v. OR BL,AL

(9) Explain all the vectored interrupts of the 8085 MPU and give their vector address. (M)

(10) Explain the function of following given pins of 8086μP (L)

i. S_3, S_4

ii. M/$\overline{IO}$

iii. $\overline{DEN}$

iv. $\overline{TEST}$

v. $\overline{LOCK}$

Section C

C. Attempt all the parts. **(2x7.5=15)**

(11) List the sequence of events that occurs when the 8085 MPU reads from memory and also draw the timing of the memory read cycle. (H)

(12) Draw the architecture of the 8086 MPU. Explain its register organization. (M)