AJAY KUMAR GARG ENGINEERING COLLEGE, GHAZIABAD
DEPARTMENT OF IT
SESSIONAL TEST -2

Course: B. Tech. | Semester: III
Session: 2017-18 | Section: IT-I, J, CS-1,2,3
Subject: Comp. Org. & Architecture | Sub. Code: RCS-302
Max Marks: 50 | Time: 2 Hours

Note : Answer **all** the Sections.

SECTION A

A. Attempt **all** the parts. (5*2=10)

1. Define Micro-instruction and Micro-operation with example.
2. Write control steps for conditional Branching with the branch condition **<0**.
3. Explain Hit, Miss, and Hit-Rate in Cache memory.
4. Define a role of Presence-Bit in Memory-page Table.
5. Differentiate b/w DRAM and SRAM.

SECTION B

B. Attempt **all** the parts. (5*5=25)

6. What do you understand by hardwired control? Describe any one method used for designing of hardwired control unit.
7. Explain all the components of control unit connected through single bus structure. Discuss the basic structure of micro-program control unit.
8. Draw a circuit and timing diagram for Write-Operation.
9. Explain the Memory Hierarchy in computer organization. Formulate the average access time for cache memory.
10. A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block. Calculate the number of bits in each of the TAG, BLOCK, and WORD fields for direct mapping and TAG, SET, and WORD fields for associative mapping in the main memory address format.

SECTION C

C. Attempt **all** the parts. (7.5*2=15)

11. Write all the control steps to execute following instruction with operation in right to left direction: MULT R_3, (R_2), R_1
12. A computer employs RAM chips of 256*8 and ROM chips 1024*8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and 4 interface units, each with four registers. A memory mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.
    a) How many RAM, ROM chips are needed?
    b) Draw a memory address map for the system.
    c) Give the address range in Hexadecimal for RAM, ROM and Interface unit.