Ajay Kumar Garg Engineering College, Ghaziabad
Department of MCA
Solution Sessional Test-2

Course: MCA		Semester:	I
Session: 2017-18		Section:	MCA-1
Subject: Computer Organization		Sub Code:	RCA-104
Max Marks:50		Time:	2 hour

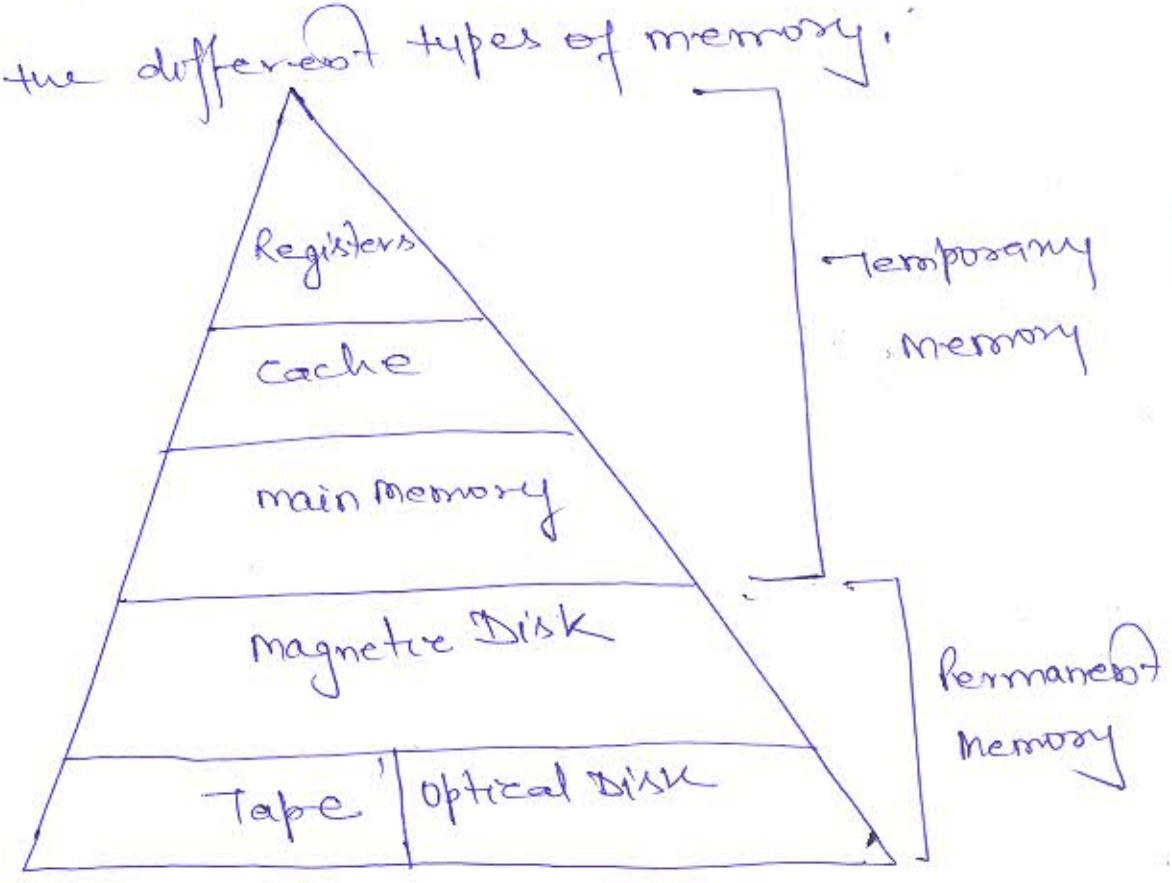
Section-A

Q.1. What do you mean by BUS master?

Solu. A bus master is the program, either in a interprocessor or more usually in a separate I/O controller, that directs traffic on the computer bus or input/output paths. The bus master is the "master" and the I/O devices on the bus are the "slaves". At a time only one bus can be of bus master and rest of "slaves".

Q.2. Explain the different types of memory.

Solu.



Five - level Memory Hierarchy

Q. 3. What do you mean by micro-operation?

Soln The operations executed on data stored in registers are called micro-operations. A micro-operation is an elementary operation performed on the information stored in one or more registers. The result of the operation may replace the previous binary information of a register or may be transferred to another register.

eg. shift, count, clear, load etc.

Q. 4. What do you mean by wide Branch addressing?

Soln. Generating branch addresses means the circuitry becomes more complex as the number of branches increases. A simple and inexpensive way of generating the required branch addresses is to use a programmable logic array (PLA). When we use PLAs for branch address generation then such concept is known as wide Branch Addressing.

Q. 5. What is micro-program sequencing?

Soln. A sequencer or microsequencer generates the addresses used to step through the microprogram of a control store. It is used as a part of the control unit of a CPU or as a stand alone generator for address ranges. In it sequencer set the order in which the micro-instructions are fetched from the control store.

Section-B

Q.6> Write the sequence of control step required for the structure of single bus organization for each of the following.

i. Add number NUM to register R1

ii. Add the content of memory location NUM to register R1

Soln.

i) Add number NUM to register R1

1. PCout, MARin, read, select, add, Zin
2. Zout, PCin, Yin, WMFC
3. MDRout, IRin
4. R1out, Yin
5. MDRout, SelectY, add, Zin
6. Zout, R1in, end.

ii) Add the content of memory location NUM to Register R1

1. PCout, MARin, read, select, add, Zin
2. Zout, PCin, Yin, WMFC
3. MDRout, IRin
4. NUMout, MARin, read
5. R1out, Yin, WMFC
6. MDRout, SelectY, add, Zin
7. Zout, R1in, end.

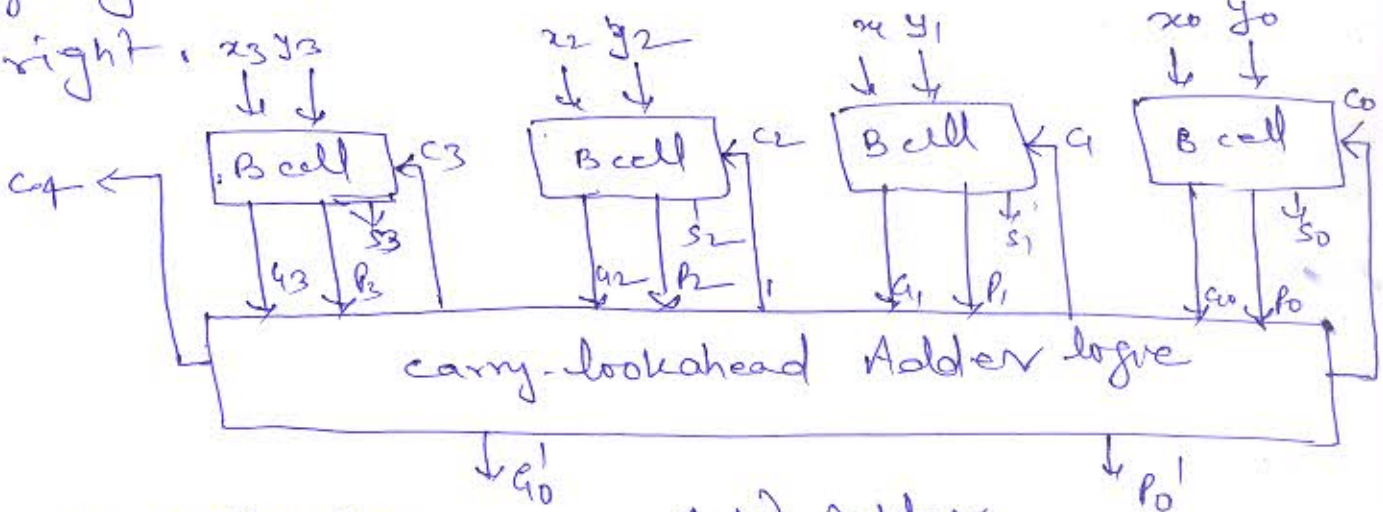
Q.7. Design a 4 bit fast adder and explain working of it.

Soln. A carry-lookahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits.

The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

carry lookahead adder depends on two things:-

1. calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the ~~right~~ right.
2. combining these calculated values to be able to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right.



4-bit Adder

$S_i = x_i \oplus y_i \oplus c_i$

$c_{i+1} = x_i y_i + x_i c_i + y_i c_i$

$c_{i+1} = x_i y_i + (x_i + y_i) c_i$

$c_{i+1} = g_i + p_i c_i$

where $G_i = x_i y_i$ & $P_i = x_i + y_i$

—.

Q9. What is 2D and 2-½ DRAM? Explain in detail.

Soln.

2D RAM :- In large capacity memory chips are often the row and the column addresses are multiplexed.
- Here the n-bit address word is divided into two parts x & y for address selection and column selections respectively.
- The cells are arranged in a rectangular array of $N_x \leq 2^{m_x}$ rows and $N_y \leq 2^{m_y}$ columns where m_x and m_y are number bits for address and column lines respectively.
- So the total number of cells in two dimensional memory organization is $N_x N_y$.
- 2-D organization requires much less circuitry than a 1-D organization for the same storage capacity.

2½ D RAM :-

- If the column and row lines are split into equal size it is referred to as 2D organization.
- If the column line and row lines are split into unequal size, it is referred to as 2½ D Ram organization.
- Two decoders are used to implement 2½ D organization. One decoder is called as row decoder and other is called column decoder. —

Q.8. What is the difference b/w Hardwired and micro-prog control unit, explain in detail.

Sol. To execute instructions the processor have required of some mean of generating the control signals needed in the proper sequence. when the control signals are generated by it is known as hardwired control. while the control signals are generated by the program, then such is known as micro-programmed control unit.

the difference b/w both are as :-

i) speed of hardwired control is fast where as micro-programmed control speed is slow.

ii) Hardwired is costly where as micro-programmed control is cheap.

iii) micro-programmed is flexible where as hardwired control is not flexible.

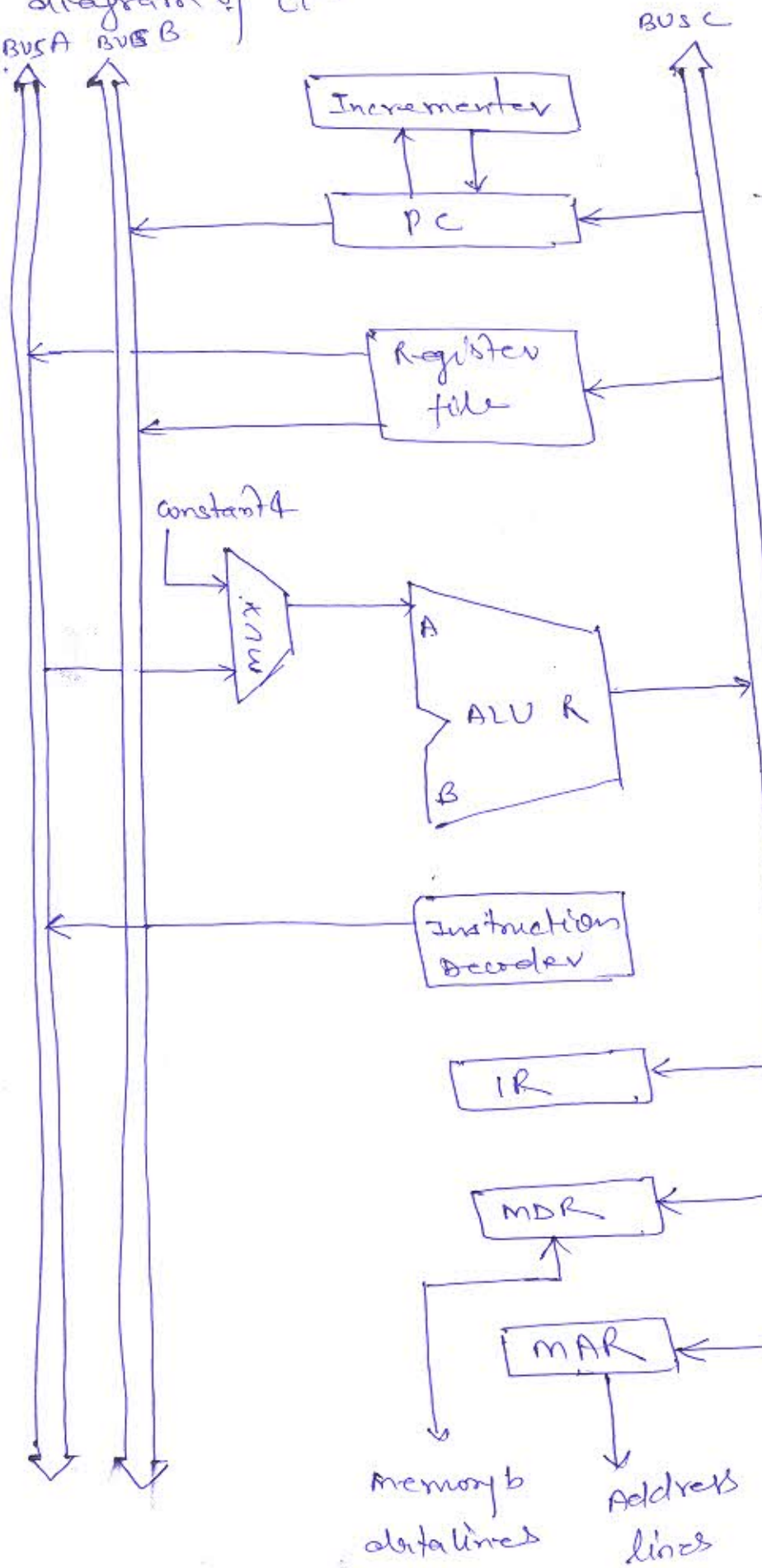
iv) Design process of hardwired control is complicated but not in micro-programmed control unit.

v) Applications of hardwired control are RISC where in microprogrammed control. CISC.

vi) Less chip area required in hardwired control but more chip area required in micro-programmed control.

10. Explain multiple Bus organizations with suitable block diagram of it.

Soln:



- Allow the contents of two different registers to be accessed simultaneously and have their contents passed on buses A & B
- Allow the data on bus C to be loaded into a third register during the same clock cycle.
- Incrementer unit
- ALU simply passes one of its two input operands unmodified to bus C.
- control signal:
  R = A
  OR
  R = B.

Section C

Q. 11. Write short notes on
i) micro Instruction
ii) Register Transfer
iii) Prefetching

Soln:

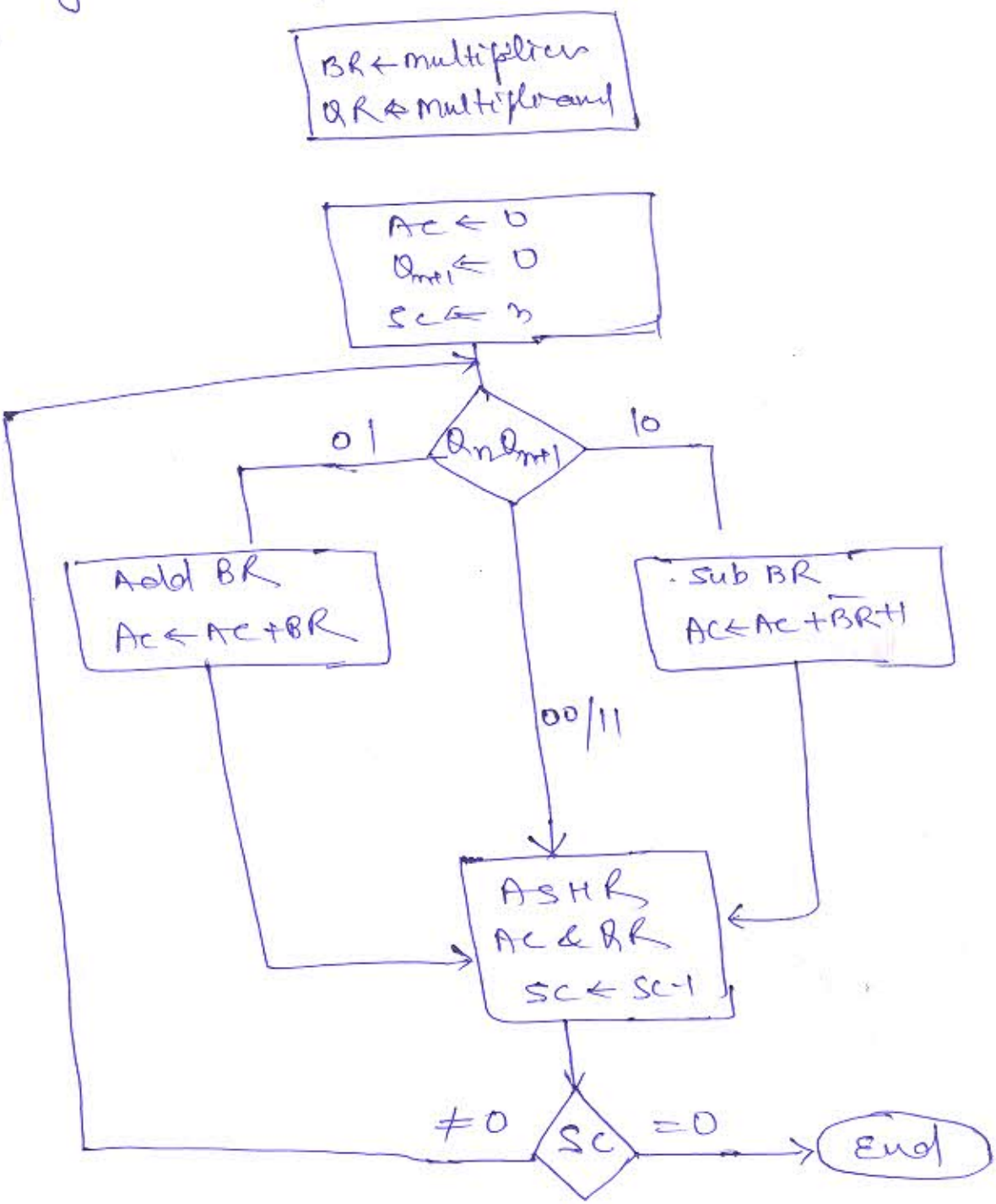
i) **Micro Instruction**:- A single instruction in microcode. It is the most elementary instruction on the computer, such as moving the content of a register to the arithmetic logic unit (ALU). It takes several microinstructions to carry out one complex machine instruction (CISC). microinstruction controls data flow and instruction execution sequencing in a processor at a more fundamental level than machine instruction.

ii) **Register Transfer**:- A micro-operation can be expressed in terms of Register Transfer language. Trying to describe the design in words is pure folly. A register transfer language is a type of Hardware description language (HDL).

iii) **Prefetching**:- transfer data from main memory to temporary storage in readiness for later use is known as prefetching.

Q.12> Write Booth multiplication Algorithm, and also do the multiplication of two numbers 11 X -18 using Booth Algorithm.

Sol n>-



11 X -18

BR = 11

⇒ BR ⇒ 001011

⇒ $\overline{BR}$ + 1 ⇒ 110101

QR = -18

⇒ QR = 101110

⇒ SC = 6

AC ← 000000

Q_{n+1} ← 0

$Q_n Q_{n+1}$	BR = 00101 BR+1 = 11011	AC 00000	QR 10110	Q_{n+1}	SC
	Initial	00000	10110	0	6
0 0	ASHR	00000	01011	0	5
1 0	Sub BR	11011			
		11011			
	Ashr	11101	10011	1	4
1 1	Ashr	11110	01001	1	3
1 1	Ashr	11111	01010	1	2
0 1	Add BR	00101			
		00100			
	ASHR	00010	11010	0	1
1 0	SUB BR	11011			
		11001			
	Ashr	11100	11101	1	0

⇒ AQ ⇒ 11100111010

⇒ Since result is in negative so for actual decimal input we have need to calculate 2's complement of AQ.

⇒ AQ ⇒ 11000110

⇒ AQ ⇒ −198

23/10/17