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Department of ECE

Model Solution ST-2

Course:	B.Tech	Semester:	VII
Session:	2017-18	Section:	EC-1, EC-2, EC-3
Subject:	VLSI Design	Sub. Code:	NEC-703
Max Marks:	50	Time:	2 hour

Section A

Que 1: What is ratioed logic and ratioless logic.

Ans: In ratioed logic V_{OL} and V_{OH} depends on the ratio of the ratio of the transistor or resistor in the circuit and in the load like resistive load inverter

In ratioless logic V_{OL} and V_{OH} donot depend on the transistor ratio like CMOS inverter.

Que 2: Define logical effort.

Ans Logical effort is the ratio of the input capacitance of a gate to the input capacitance of inverter. It is ~~defined~~ as denoted as g. Or it is defined as the measurement of relative ability of gate to deliever current.

$$g = \frac{C_{in}(gate)}{C_{in}(inv)}$$

Logical effort (g) of inverter 1.

Que 3: What is parasitic Delay.

Ans: Parasitic delay represents delay of gate deriving no load. It is set by internal parasitic capacitance. It is denoted by P.

P for inverter = 1 (It also depends on no. of inputs of gate)

Qu-4 What is EDP and how it is better than PDP.

Ans EDP – Energy delay product ; PDP – Power delay product.

PDP = Pavg tp and Pavg = $CV_{DD}^2 f$

$tp = \frac{1}{2f}$ ∴ PDP = $CV_{DD}^2 f \cdot \frac{1}{2f} = \frac{CV_{DD}^2}{2}$

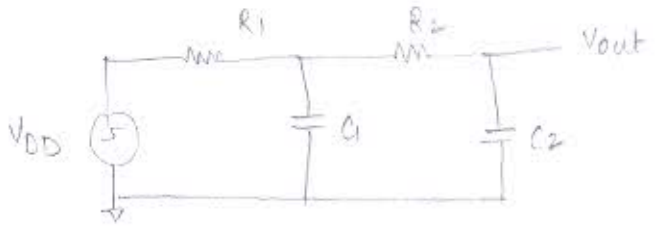
In EDP = PDP × tp

$= \frac{C^2 \cdot V_{DD}^3}{2K_2(V_{DD} - V_T)}$

∴ In PDP, out of C or V_{DD} we can handle only only parameter.

Qu-5. Calculate the delay of following circuit using elmore delay model.

Ans.



→ ON transistors look like resistors

→ Pull up or pull down network modelled as RC ladder

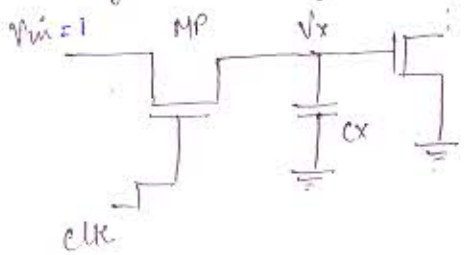
→ Elmore delay of RC ladder

$$t_{pd} = \sum_{\text{node } i} R_{i\text{-to-source}} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 .$$

Que-6 Derive the expression for voltage across pass transistor for transmission of logic '0' and logic '1'.

Ans: Logic '1' Transfer:



when clk = 1 and Vin = 1 Vx node will be charged upto logic 1

MP only provides the current path to the intermediate capacitive node (soft node). when clock become inactive the MP ceases to conduct and the charge stored in the parasitic capacitance Cx continues to determine the o/p level of the inverter.

Assume that $V_x = 0$ at $t = 0$

$V_{in} = V_{OH} = V_{DD}$ is applied. Now the gate signal at the gate of MP goes from 0 to V_{DD} at $t = 0$. MP starts to conduct and operate in saturation mode throughout this cycle

Since $V_{DS} = V_{GS}$

$V_{DS} > V_{GS} - V_t$ – the MP operates in saturation region

Starts to charge up the capacitance.

$$\text{So} \quad C\frac{dV_x}{dt} = \frac{K_n}{2}\left(V_{GS} - V_x - V_{T,n}\right)^2$$

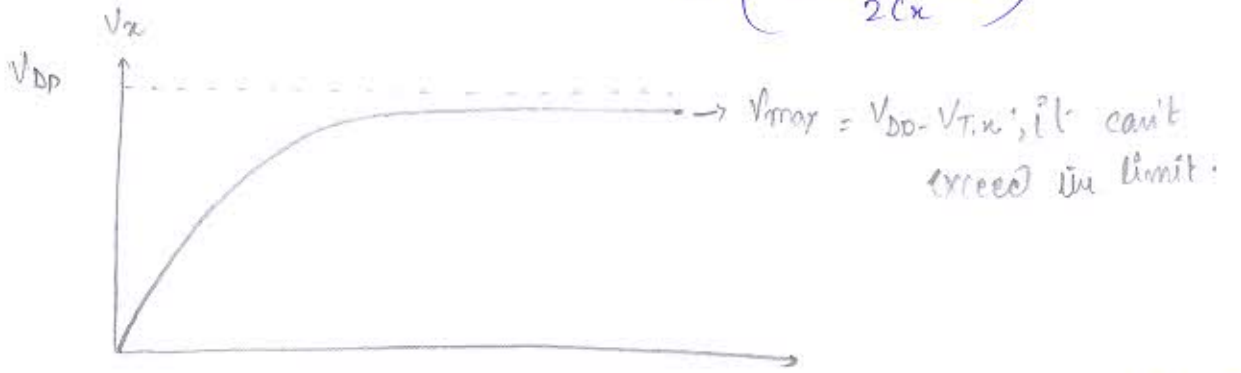
$$\frac{C\,dV_x}{dt} = \frac{K_n}{2}\left(V_{DD} - V_x - V_{T,n}\right)^2$$

$$\int_0^t dt = \frac{2C_x}{K_n}\int_0^{V_x} \frac{1}{(V_{DD} - V_x - V_{T,n})} \cdot dV_x = \frac{2C_x}{K_n}\left(\frac{1}{V_{DD} - V_x - V_{T,n}}\right)\Big|_0^{V_x}$$

$$t = \frac{2C_x}{K_n}\left[\left(\frac{1}{V_{DD} - V_x - V_{Tn}}\right) - \frac{1}{V_{DD} - V_{Tn}}\right]$$

The eqn can be solved for $V_x(t)$

$$V_x(t) = (V_{DD} - V_{T,n}) \frac{K_n \left(\frac{V_{DD} - V_{T,n}}{2C_x}\right) t}{1 + \left(\frac{K_n (V_{DD} - V_{Tn})}{2C_x}\right) t}$$



The MP will be turned off when $V_x = V_{max}$. Since at this point $V_{GS} = V_{T,n}$. The voltage at node x can never attain the full power supply voltage level of V_{DD} during the logic '1' transfer.

Logic '0' Transfer: Assume that the soft node voltage $V_x = 1$ level initially. i.e $V_x(t=0) = V_{max} = V_{DD} - V_{Tn}$.

When logic '0' is applied @ the i/p terminal which corresponds @ $V_{in} = 0V$ (when a logic 0) at clock ⊓ 0 @ V_{DD} at $t=0$ The pass transistor starts @ conduct when clocks become active, and it will operate in linear mode.

$$-C_x \frac{dV_x}{dt} = \frac{K_n}{2} \left(2(V_{DD} - V_{Tn}) V_x - V_x^2\right)$$

$$dt = -\frac{2C_x}{K_n} \left(\frac{dV_x}{2(V_{DD} - V_{Tn}) V_x - V_x^2}\right)$$

Note that the source voltage of the nmos pass transistor is equal @ 0V during this event. Hence there is no substrate bias effect for MP. But the initial condition $V_x(t=0) = (V_{DD} - V_{tn})$ considers the contains the Threshold voltage with substrate effect because voltage V_x is set during the preceeding logic 1 transfer event.

$$dt = -\frac{2C_x}{K_n} \cdot \frac{dV_x}{2(V_{DD}-V_{Tn})V_x - V_x^2}$$

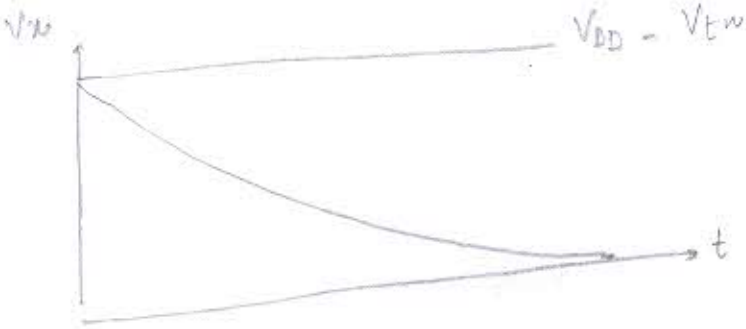
$$= -\frac{2C_x}{K_n} \frac{dV_x}{[2(V_{DD}-V_{Tn})-V_x]\cdot V_x}$$

$$= \frac{A}{2(V_{DD}-V_{Tn})-V_x} + \frac{B}{V_x}$$

$$1 = A V_x + B[2(V_{DD}-V_{Tn}) - V_x]$$

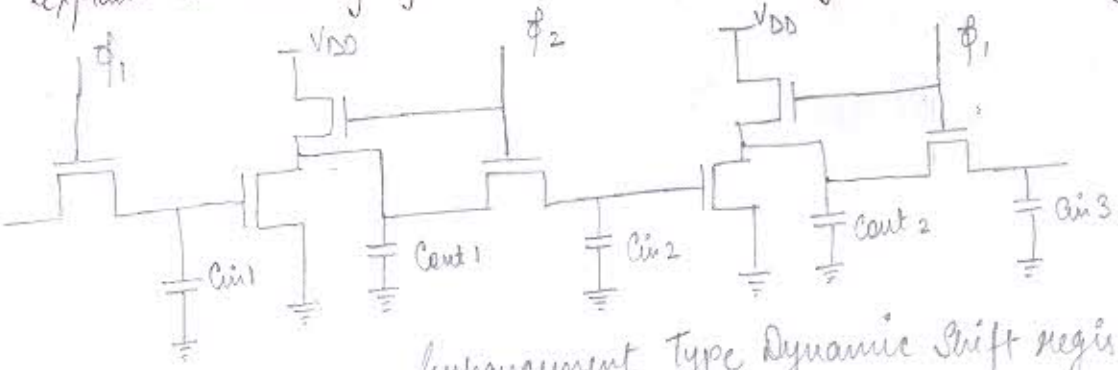
Solving this equation ; we will have

$$= \frac{C_x}{K_n (V_{DD}-V_{tn})} \left[\ln \left(\frac{2V_{DD}-V_{t,n})-V_x}{V_x} \right) \right] \Bigg|_{V_{DD}-V_{tn}}^{V_x}$$



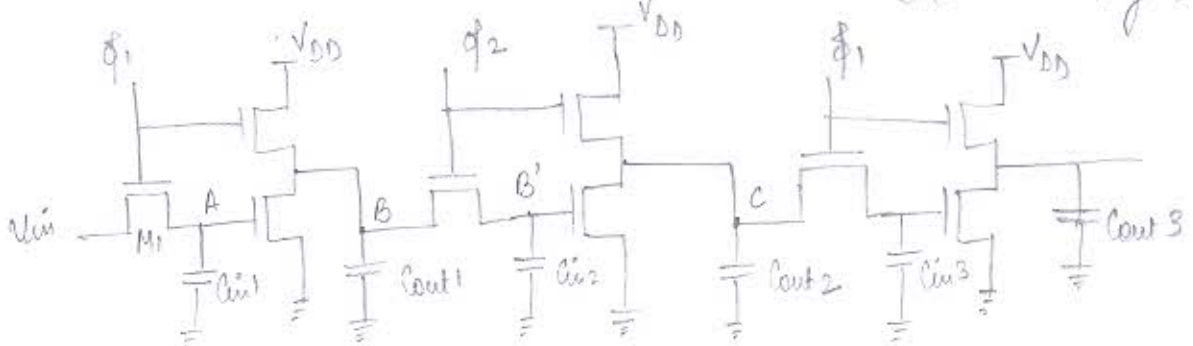
Que-7 Explain the working of enhancement load dynamic shift register.

Ans



Enhancement Type Dynamic Shift register

(Ratioed logic)



Ratioed logic with different clocking schemes

In dynamic shift register two phase clocking system is used when ϕ_1 is active. M_1 and first inverter is activated. If the o/p across $C_{out_1} = 1$ at the end of ϕ_1 phase, this voltage is transferred to C_{in2} via charge sharing over the pass transistor during $\phi_2 = 1$

Logic high level at the o/p node is subjected to impressed voltage drop i.e. one V_t lower than V_{DD}. To correctly transfer the logic high level after charge sharing, the ratio of the C_{out}/C_{in} should be kept large enough during circuit design.

If o/p $C_{out} 1 = 0$ at the end of ϕ_1, the $cout_1$ will be completely drained to voltage of $V_{OL} = 0V$ when ϕ_1 is turned ON. Since the valid logic low level of $V_{OL} = 0V$ can be achieved regardless of the driver to load ratio, the ckt arrangement is called Ratioless dynamic logic.

During $\phi_1 = 1$ V_{in} is transferred to C_{in_1}. And valid V_{out} of the first stage is determined as the inverse of the current i/p during this cycle.

When ϕ_2 is active during the next phase, the o/p voltage level of the S_1 stage is transferred to the S_2 input capacitance C_{in2}. During active ϕ_2, the first stage i/p capacitance continues to retain its previous level via charge storage.

⇒ If we take narrow clock pulse, load transistor is also ON for a very short time during duration, so for most of the load is OFF. So power dissipation is less.

Que 8 What is interconnect engineering explain in detail.

Ans: As the gate delay continues to improve while long wire delays remain constant or even get slower, so wire engineering has become a major part of integrated circuit design. So it is necessary to also develop a floorplanning in such a way that critical communicating units are close to one another.

The designers selects the wire width, spacing, and layer usage to tradeoff delay, B.W, energy and noise. By default, minimum pitch wires are preferred for noncritical interconnection for best density and wider when the load is dominated by wire capacitance, the best way to reduce delay is to increase spacing, reducing the capacitance to nearby neighbours.

→ This also reduces energy and coupling noise

→ When the delay is dearm dominated by the gate capacitance and wire resistance, widening the wire reduces resistance and delay.

→ It may increase the capacitance of top and bottom plate.

→ Wire thickness depends on the choice of metal layer.

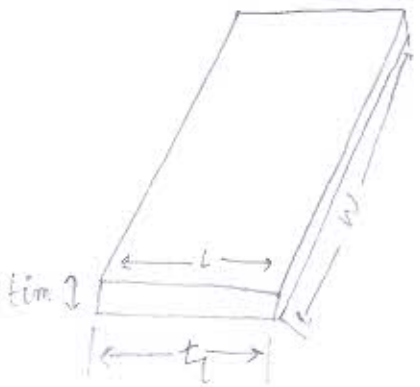
→ The lower layers are thin and optimized for a tight routing pitch.

→ Middle layers are often thick to provide low or resistance and better current handling capacity

→ Upper layer may be even thicker to provide a low resistance power grid and fast global interconnect

Que-10 Explain with expressions the buffer insertion in interconnects & optimize delay.

Ans. Buffer insertion or repeater insertion



$$R = \rho \frac{L}{W t_m} \; ; \; C = \epsilon \frac{WL}{t_i}$$

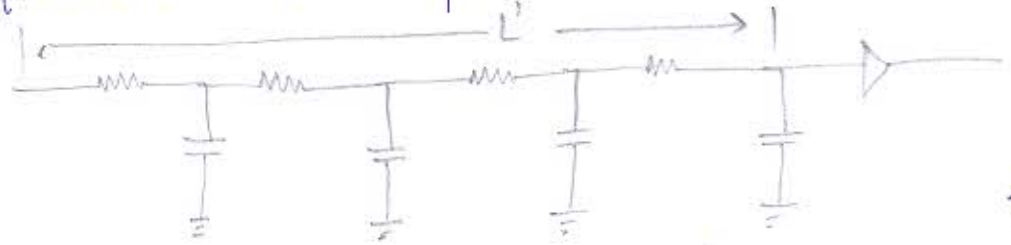
$$\tau = RC = \rho \frac{\epsilon L^2}{t_m t_i}$$

Here ρ, ϵ, t_m, t_i are derived by the technology and L can be controlled in design

Wire delay $\rho \frac{\epsilon L^2}{t_m t_i} = AL^2$

→ Now to minimize delay of global interconnect, we divide the long length interconnect into smaller segments and insert buffer in between them.

→ We define certain critical wire length, if wire length exceed their length, then we will insert a buffer.



L' → Small segment of wire of length L

τ → buffer delay.

∴ Segment wire delay = AL'^2

for n segment, there will be n-1 buffers and $L = nL'$

$$\Delta = nAL'^2 + (n-1)\tau = \frac{L}{L'} AL'^2 + \left(\frac{L}{L'} - 1\right)\tau$$

$$= AL'L' + \left(\frac{L}{L'} - 1\right)\tau$$

Putting the derivation w.r.t to $L' = 0$

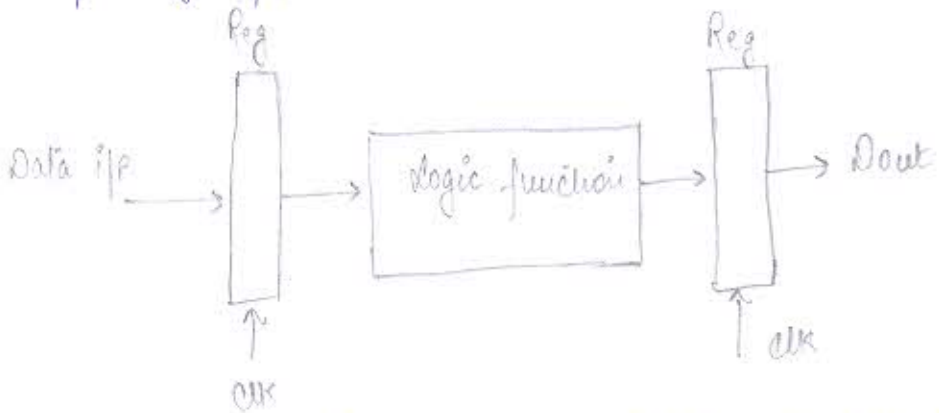
$$AL - \frac{L}{L'^2}\tau = 0 \quad \text{or} \quad AL'^2 = \tau$$

So L' should be chosen that the wire segment delay should be equal to the delay of the buffer.

Que-9. Explain the pipeline and parallel architecture for low power VLSI design.

Ans In the past parallism and pipelining have been effective ways to reduce the power consumption.

Pipelining Approach:



Above block implements a logic function i/p of the i/p vectors. Both the i/p and o/p vectors are sampled by register arrays, driven by a clock. Assume that the critical path in the logic block allows max. sampling frequency of f_{clk}.

→ max. i/p & o/p prop delay $T_{prop} \leq T_{clk} = \frac{1}{f_{clk}}$

C_{Total} = Total cap switched every cycle

will be the sum of (i) cap. switched at i/p reg. array + cap. switched at logic function + cap. switched in the o/p reg. array.

Then $P_{dynamic} = C_{Total} \cdot V_{DD}^2 \cdot f_{clk}$

Now consider N-stage pipelined structure for implementing the same logic function. The logic function F(i/p) has been partitioned into N successive stage and a total N-1 registers arrays have been

introduced, in addition to the original i/p and o/p required to create a pipeline structure.

→ All registers are clocked at original sample rate f_{clk}.

→ If all stages have equal delay.

→ $T_{p\,a} = \frac{T_{pmax}\,(i/p \text{ to } o/p)}{N} = T_{clk}$.

Then the logic block between two successive registers can operate N-times slower while maintaining the same functional block throughput as before. This implies that the power supply can be reduced to a new value of V_{DD} & effectively slowdown the clock by the factor of N.

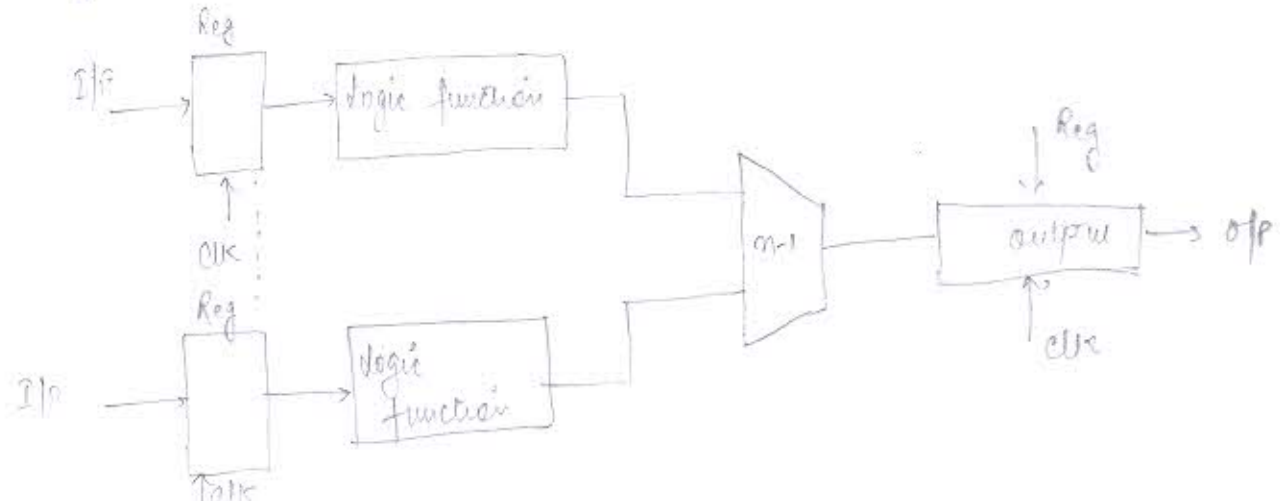
$$\text{Power}_{pipeline} = \left[C_{Total} + (N-1)\,C_{reg} \right] \cdot V_{DD\,New}^2 \cdot f_{clk}$$

$$\text{Power reduction factor} = P_{pipeline} / P_{ref.} = 1 + \frac{C_{reg}\,(N-1)}{C_{Total}} \cdot \frac{V_{DD_{new}}^2}{V_{DD}}$$

$$= \frac{1 + C_{reg}\,(N-1)}{C_{Total}} \cdot \frac{V_{DD\,new}^2}{V_{DD}}.$$

So the structure has a large area but the power is reduced.

Parallel Approach – or hardware replication: It is used for logic functions which are not suitable for pipeline.



→ Clock signal to each i/p register are skewed by T_{clk} such that each of the N consecutive i/p vectors is loaded into a different register.

→ Each register is clocked at lower frequency of f_{clk}/N the time allocated to compute the functions for each input vector is increased by the factor of N. So V_{DD} is decreased until the critical path delay equivalent to new clk period of T_{clk}.

Time allowed to compute each function for each i/p vector is increased by the factor of N. V_{DD} is decreased and the overall performance is slow.

$$P_{parallel} = N \cdot C_{Total} \cdot V_{DDnew}^2 \cdot \frac{f_{clk}}{N} + C_{reg} \cdot V_{DD}^2 new \, f_{clk}$$

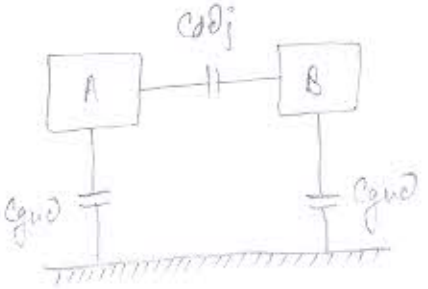
$$= \left(1 + \frac{C_{reg}}{C_{Total}}\right) C_{Total} \cdot V_{DDnew}^2 \cdot f_{clk}$$

$$\text{Power reduction function} = \frac{P_{parallel}}{P_{reg}} = \frac{V_{DD\,new}^2}{V_{DD}^2}\left(1 + \frac{C_{reg}}{C_{Total}}\right)$$

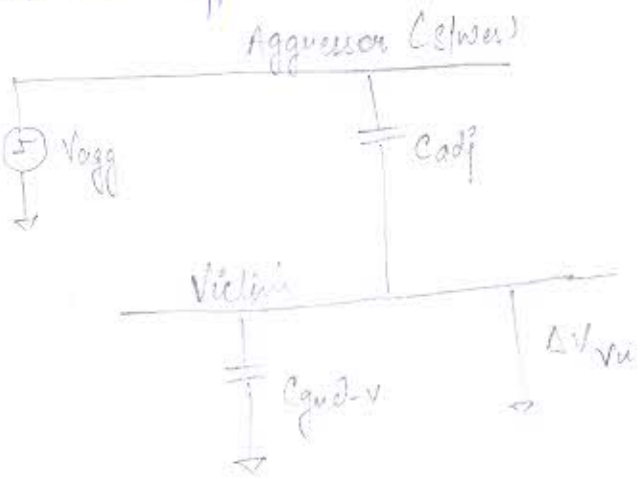
Section C

Que-1) Explain the crosstalk in interconnect and what are the methods to minimize the crosstalk.

Ans: Crosstalk : Wires have capacitance to their adjacent neighbours as well as to ground. When wire is switched, it tends to bring its neighbour B along with it on account of coupling capacitance. This is known as crosstalk. If B is supposed to switched simultaneously, this may increase or decrease the switching delay. If B is not supposed to switch, crosstalk causes noise on B



Crosstalk noise effect:



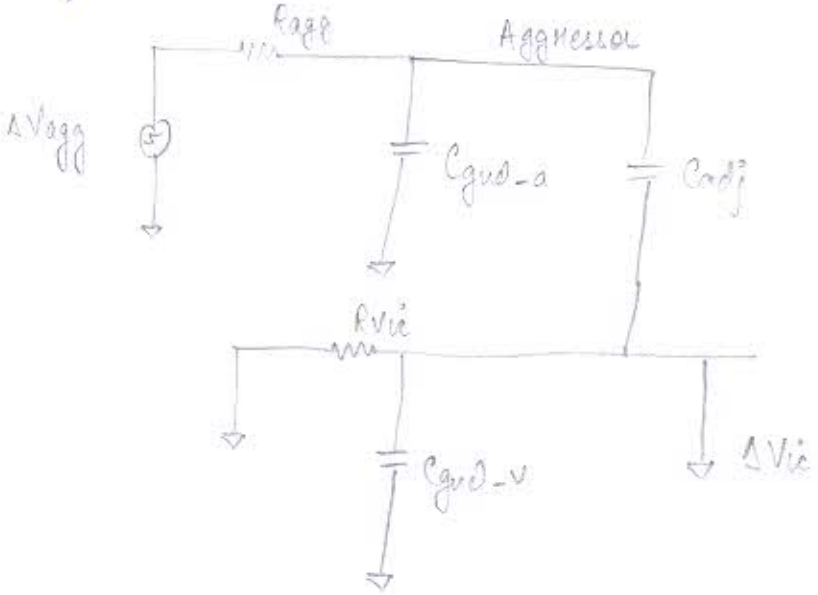
Wire A - switches — Aggressor
B - constant - Victim

This introduces noise as B partially switches. If Victim is floating, we can model the circuit as a capacitive voltage divides to compute the victim noise.

$$\Delta V = \frac{C_{adj}}{C_{adj} + C_{gnd-v}} \Delta V_{agg}$$

If the victim is actively driven, the driver will supply current to operate oppose and reduce the victim noise.

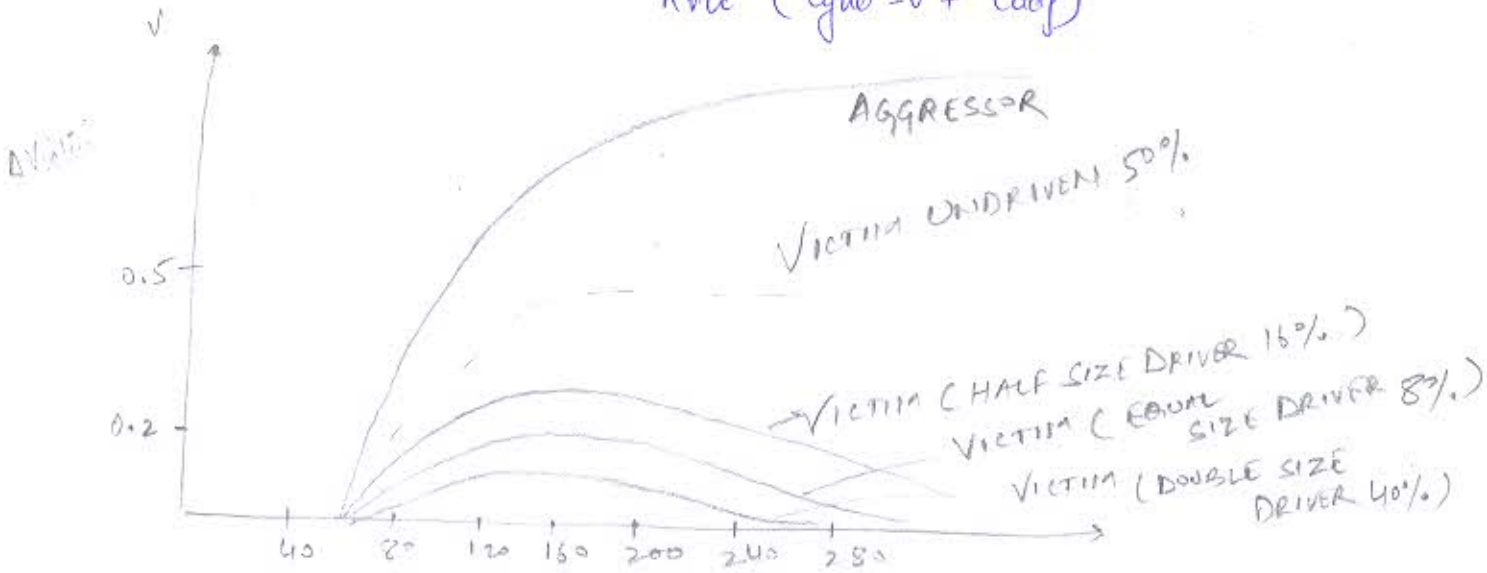
- If we model the driver as resistors.



The peak noise become dependent on the time constant ratio K of the aggressor & the victim.

$$\Delta V = \frac{C_{adj}}{C_{gvd-v} + C_{gu}\, C_{adj}} \frac{1}{1+K} \Delta V_{agg}$$

$$K = \frac{\tau_{agg}}{\tau_{vic}} = \frac{R_{agg}\,(C_{gvd-a} + C_{adj})}{R_{vic}\,(C_{gvd-v} + C_{adj})}$$



Waveforms Of Coupling Noise

We have only considered the case of a single neighbours switching when both neighbours switches the noise will be doubled.

Crosstalk Control : Capacitive crosstalk is proportional to the ratio of coupling capacitance to total capacitance

$$\text{Capacitive crosstalk} = \frac{\text{Coupling capacitance}}{\text{Total Cap.}}$$

For modern wires with an aspect ratio (t/w) of 2 or more. The coupling capacitor can account for 2/3 to 3/4 of the total capacitance and crosstalk can create large amount of noise and cause data dependent delay variation.

Approaches to control crosstalk

- Increase spacing to adjacent lines
- Shield wires
- Ensure neighbours switch at different time
- Crosstalk cancellation.

To fix minor crosstalk we can increase spacing.

Three methods to improve crosstalk → staggered repeaters
→ charge compensation
→ Twisted differential signaling

Each technique seeks to cause equal amounts of positive and negative crosstalk on the victim, effectively producing zero net crosstalk.

a) Staggered Repeaters:

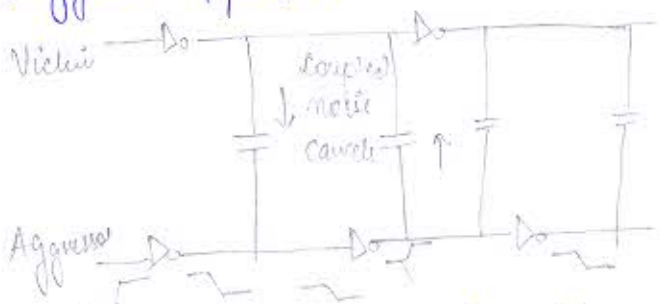
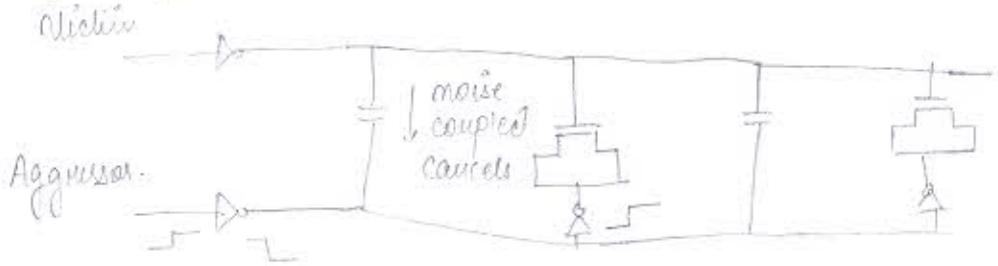


Diagram shows two wires with staggered repeaters. Each segment of the victim sees half of a rising aggressor segment and half of a falling aggressor segment.

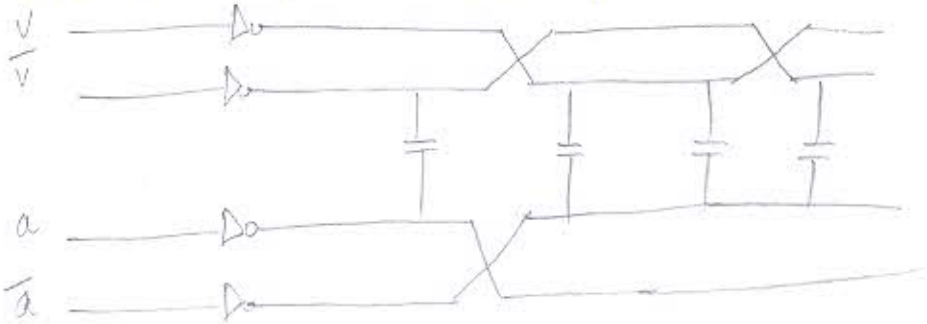
Although the cancellation is not perfect because of delays along the segments staggered staggering is a very effective approach.

(b) Charge Compensation:



→ An inverter and transistor are added between aggressor and victim.
→ Transistor is connected to behave as a capacitor.
→ When the aggressor rises and couples the victim upward, the inverter falls and couples the victim downward.
→ By choosing the appropriate sized compensation transistor, most of the noise can be cancelled at the expense of extra circuitry.

(c) TDS.: Twisted Differential Signaling:



Each signal is routed differentially. The signals are swapped or twisted such that the victim and its complement each see coupling from the aggressor and its components.

→ Expensive in wiring resources
→ Effective in eliminating crosstalk
→ Used in memory design

Que-12 Explain the electrical effort, logical effort, path effort and branch effort. Calculate the electrical effort, logical effort, branching effort, parasitic delay and overall delay.

Ans:- In general the propagation delay of a gate can be written as

$d = f + p$ → parasitic delay (when no load is attached)

↳ effort delay or stage delay that depends on the complexity and fanout of the gate.

Effort delay $f = gh$

h → Electrical effort

g → Logical effort

An inverter is defined to have logical effort = 1

And if the load is not identical copies of the gate, then the electrical effort can be computed as

$$\text{Electrical Effort} = h = \frac{C_{out}}{C_{in}} = \frac{\text{Capacitance of ext. load being driven}}{\text{I/P capacitance of the gate}}$$

Logical Effort – It describes the driving capability of gate relative to that of a reference inverter. or it the ratio of I/P capacitance of the gate to the I/P capacatance of an inverter that can deliver the same amount of current. It is denoted by g.

Parasitic delay – Parasitic delay (p) is calculated when no load is connected.

$$\text{Branching effort} = \frac{C_{on\,path} + C_{off\,path}}{C_{on\,path}}$$

In this path we have two branches

$$b_1 = \frac{x + (x+x)}{x} = \frac{3x}{x} = 3$$

$$b_2 = \frac{y+y}{y} = \frac{2y}{y} = 2$$

$$B = b_1 \times b_2 = 3 \times 2 = 6$$

Path effort $F = GBH$

$$= \frac{100}{27} \times 6 \times \frac{45}{8} = 125 \text{ for 3 three stages.}$$

Delay will be minimum if the stage effort is equal for all the three stages.

So best stage effort $= \sqrt[3]{125} = 5 = \hat{f} = \sqrt[N]{\text{Path effort } F}$

where N = no. of stages

Path parasitic delay $= 2+3+2 = 7$

Path delay or overall delay $D = P + \hat{f}N$

$$= 7 + 5 \times 3 = 22$$

For a path of logical effort gate, The logical effort of a chain of gate is

$$G = \prod_{i=1}^{n} g_i$$

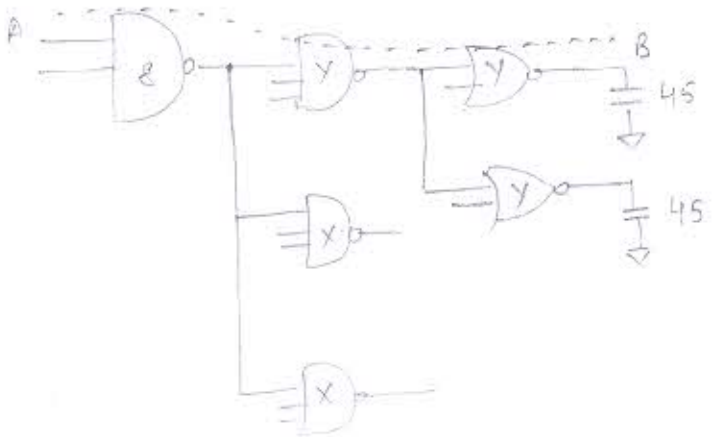
$$H = C_{out}/C_{in}$$

Branching effort takes fanout into account

$$b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}$$

Branching effort of the entire path $B = \prod_{i=1}^{n} b_i$

Path effort $F = GBH$



Path effort $F = \Pi f_i = \Pi g_i h_i$

Logical effort $G = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$

Path Electrical effort $H = \frac{C_{out}}{C_{in}} = \frac{45}{8}$

Branching effort $= \frac{C_{onpath} + C_{offpath}}{C_{onpath}}$

$B = \Pi b_i$