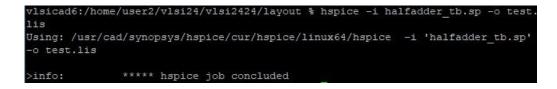
2023 超大型積體電路電腦輔助設計概論

2023 Introduction to VLSI CAD Lab 11

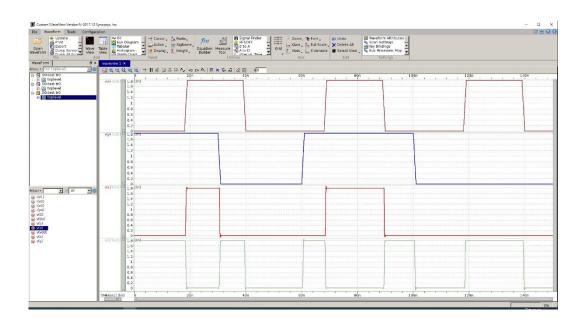
學號: E24116152 姓名: 劉冠妤

※作業要求的圖請使用**電腦截圖程式**截取,請勿用手機拍照的方式繳交 ※Report 檔請以 pdf 的格式繳交

- HA
 - Presim
 - 請截取 terminal 顯示 job concluded 的圖



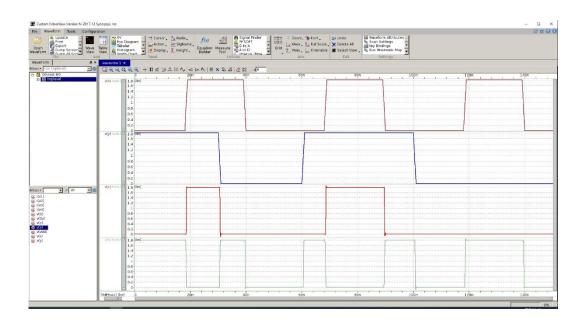
• 請截取 WaveView 中的波形



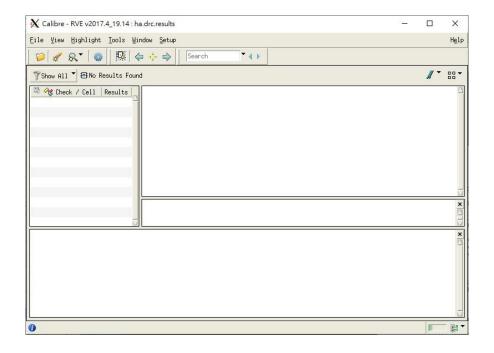
- Post-sim
 - 請截取 terminal 顯示 job concluded 的圖

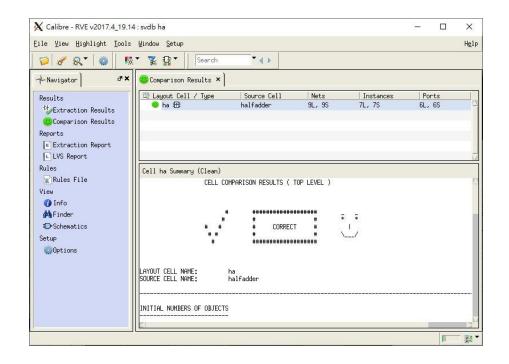
```
vlsicad6:/home/user2/vlsi24/vlsi2424/Labl1_E24116152 % hspice -i halfadder_tb.sp -o test.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice -i 'halfadder_tb.sp' -o test.lis
Warning(s) associated with encrypted block(s) were suppressed due to encrypted content.
>info: ***** hspice job concluded
```

• 請截取 WaveView 中的波形

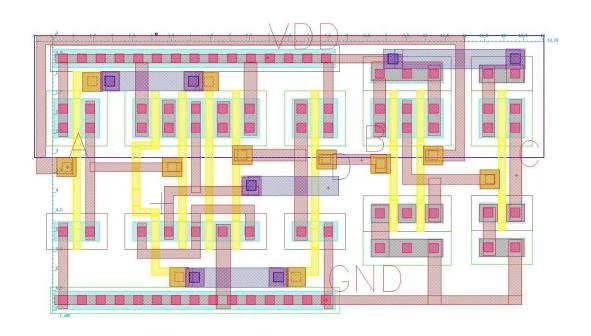


• DRC/LVS 結果





• Layout 截圖(顯示長寬)



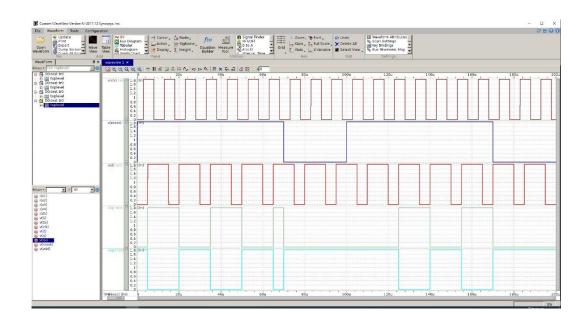
Area = $13.03 \times 7.085 = 92.31755$

• 嘗試簡單說明 Presim 與 Post-sim 結果比較

兩者大致相同,但從 Post-sim 的波型圖中可以觀察到訊號有較多雜訊, 推測為些許寄存電容影響。

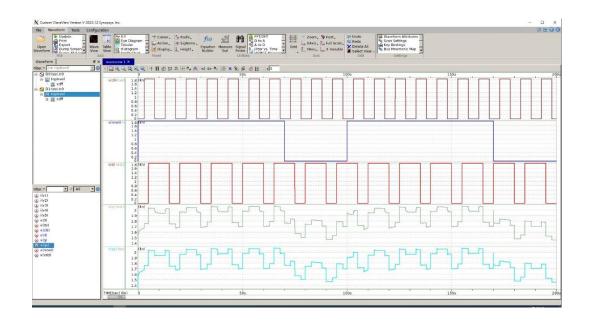
- DFF
 - Presim
 - 請截取 terminal 顯示 job concluded 的圖

• 請截取 WaveView 中的波形

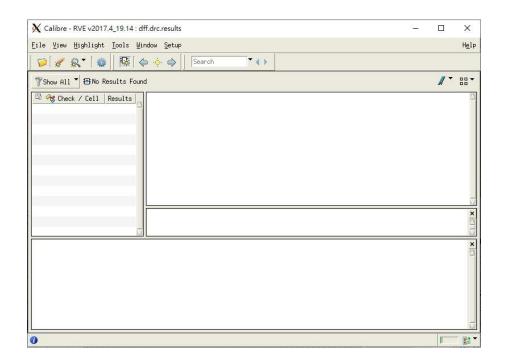


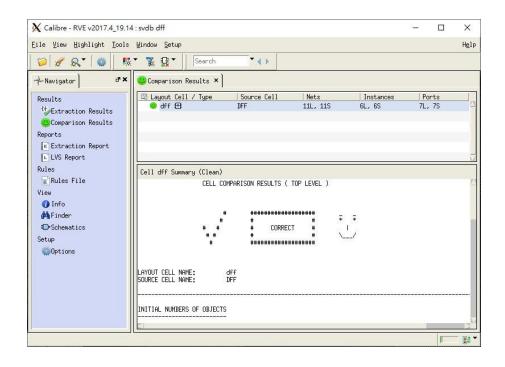
- Post-sim
 - 請截取 terminal 顯示 job concluded 的圖

• 請截取 WaveView 中的波形

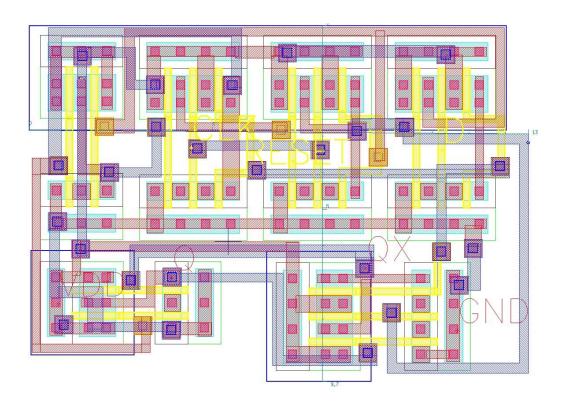


• DRC/LVS 結果





• Layout 截圖(顯示長寬)



Area = $13 \times 9.7 = 126.1$

• 嘗試簡單說明 Presim 與 Post-sim 結果比較

兩者大致相同,但從 Post-sim 的波型圖中可以觀察到訊號有很多雜訊, 推測為寄存電容影響,可能是因為 layout 畫得不好。

• 心得討論

這次的實驗花了很多時間在修正,可能是一開始的設計不夠好, 所以之後要先設計好再開始畫比較好。