

**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2024)***

**Lab Session 7**

**Design of Local Binary Pattern Facial  
Recognition System**

| Name      | Student ID |       |
|-----------|------------|-------|
| 劉冠妤       | E24116152  |       |
| Practical | Points     | Marks |
| Lab 7_1   | 30         |       |
| Lab 7_2   | 65         |       |
| Report    | 5          |       |
| Demo      | 10         |       |
| Notes     |            |       |

**Due: 15:00 May 1, 2024@ moodle**

## Summary

| Hardware  |         |             |                      |
|---|---------|-------------|----------------------|
| TOP   |         | RTL(✓/X)    | Synthesis(✓/X)       |
| Lab7_1  |         | ✓           | ✓                    |
| Lab7_2  |         | ✓           | X                    |
| Synthesis result  |         |             |                      |
| Clock period(ns)  |         | Area        | Simulation time (ns) |
| 0.34  |         | 9791.280244 | 33478060036          |
| Superlint(number of inline messages, just write down the final design result, i.e. if you only finish lab7_1, write your Superlint result of lab7_1, otherwise, write down lab7_2 only) |         |             |                      |
| Total lines   | Warning | Error       | coverage(%)          |
| 1873  | 329     | 0           | 82.43%               |

**Note: You must complete and fill out this form with your design information!!!**

## Deliverables

- 1) All Verilog codes including testbenches for each problem should be uploaded.  
NOTE: Please **DO NOT** include source code in the paper report!
- 2) All homework requirements should be uploaded in this file hierarchy.
- 3) NOTE: 1. Please **DO NOT** upload waveforms (.fsdb or .vcd)!
- 4) If you upload a dead body which we can't even compile, you will get NO credit!
- 5) All Verilog file should get at least **90%** SuperLint Coverage.
- 6) All homework requirements should be uploaded in this file hierarchy or you will not get full credit, if you want to use some sub modules in your design but you do not include them in your tar file, you will get 0 point.

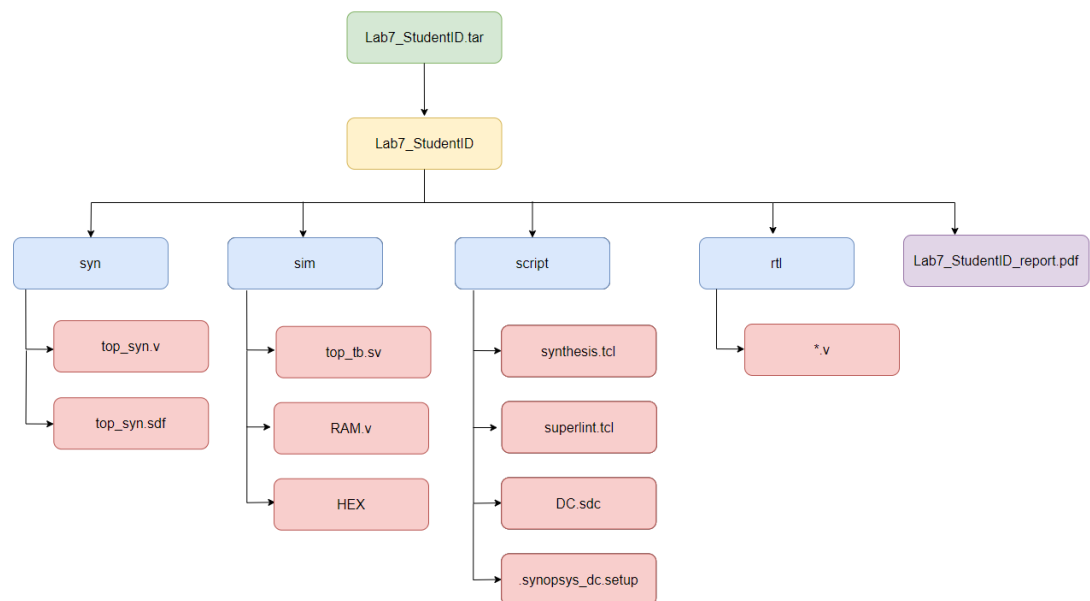


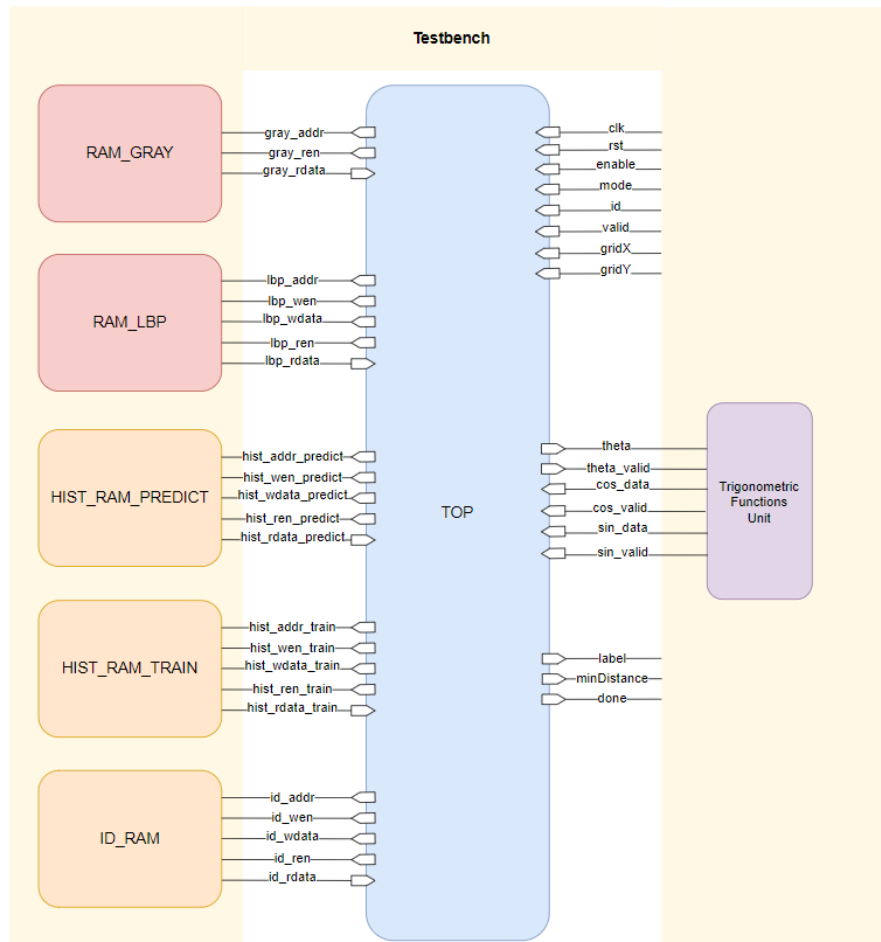
Fig.1 File hierarchy for Homework submission

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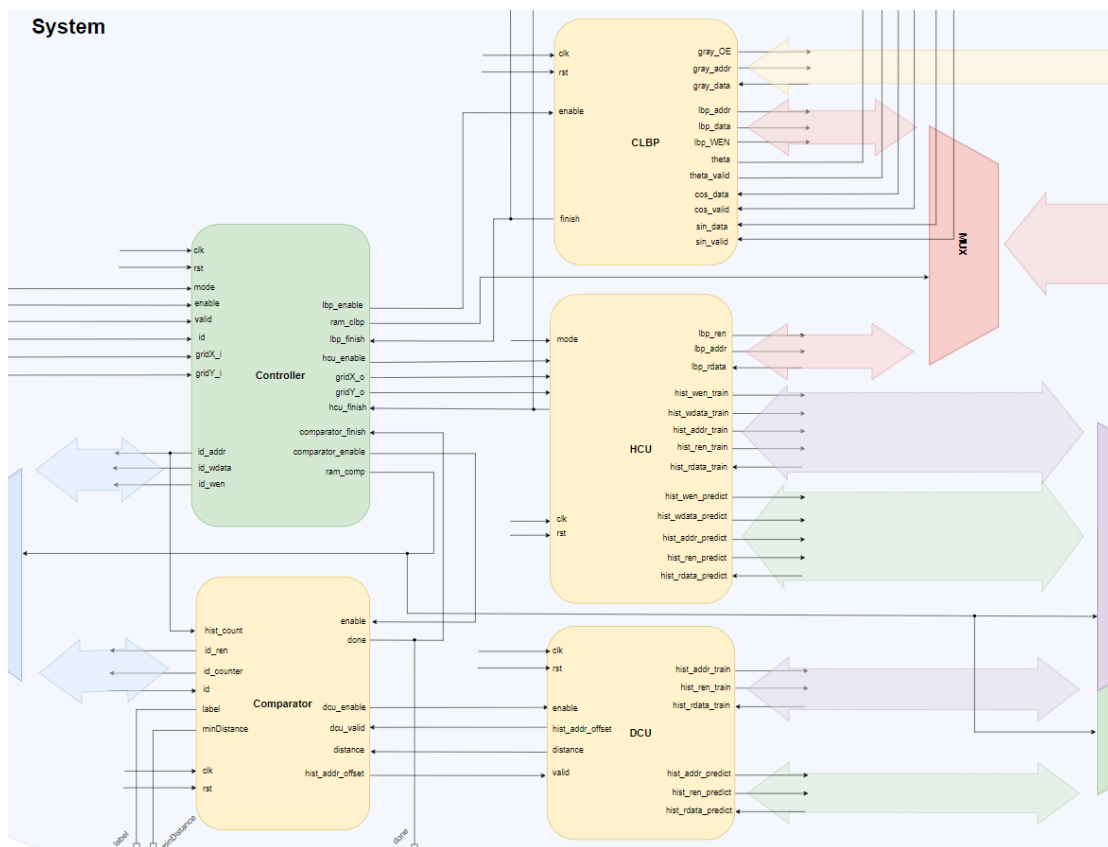
## Lab 7

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You are about to integrate all components (CLBP, HCU, Controller...) to form a LBP facial recognition system. The block diagram of system is as shown in **Fig2** and **Fig3**.



▲Fig2. The block diagram of system (external)



▲

➤ **Port list of top module:**

➤ **TOP**

| Signal      | I/O | Bit-width | Description  |
|-------------|-----|-----------|--|
| clk         | I   | 1         | Clock signal   |
| rst         | I   | 1         | Reset signal   |
| enable      | I   | 1         | Circuit enabling signal  |
| mode        | I   | 1         | Indication signal of whether the system is in prediction or training phase, 0 is training, 1 is prediction           |
| gridX       | I   | 4         | Image sliced portion in X direction, value is 8  |
| gridY       | I   | 4         | Image sliced portion in Y direction, value is 8  |
| valid       | I   | 1         | Indication that current subject ID is valid  |
| id          | I   | 5         | Subject ID   |
| hcu_finish  | O   | 1         | Indication that HCU circuit is done(should be asserted every time a subject picture is finished computing histogram) |
| label       | O   | 5         | Prediction result, output ID value   |
| minDistance | O   | 18        | Minimum distance between the prediction histogram and the closest histogram in HIST_TRAIN_RAM                        |
| done        | O   | 1         | Indication that prediction of one picture is finished  |

| Signal      | I/O | Bit-width       | Description  |
|-------------|-----|-----------------|--|
| gray_addr   | O   | 12              | Address signal connected to RAM_GRAY                   |
| gray_ren    | O   | 1               | Read enable signal to RAM_GRAY                         |
| gray_rdata  | I   | 8               | Read data signal from RAM_GRAY                         |
| lbp_addr    | O   | 12              | Address signal connected to RAM_LBP                    |
| lbp_wen     | O   | 1               | Write enable signal to RAM_LBP                         |
| lbp_wdata   | O   | 8               | Write data signal to RAM_LBP                           |
| lbp_ren     | O   | 1               | Read enable signal to RAM_LBP                          |
| lbp_rdata   | I   | 8               | Read data signal from RAM_LBP                          |
| theta       | O   | 25(fixed-point) | Current neighbor's theta signal(unit is in radian)     |
| theta_valid | O   | 1               | Indication signal of current neighbor's theta is valid |
| cos_data    | I   | 25(fixed-point) | Cosine value of the theta(from testbench)              |
| cos_valid   | I   | 1               | Indication signal of cosine value is valid             |
| sin_data    | I   | 25(fixed-point) | Sine value of the theta(from testbench)                |
| sin_valid   | I   | 1               | Indication signal of sine value is valid               |
| lbp_finish  | O   | 1               | Indication signal of the CLBP circuit is finished      |

| Signal             | I/O | Bit-width | Description                                  |
|--------------------|-----|-----------|--|
| id_addr            | O   | 8         | Address signal connected to ID_RAM           |
| id_ren             | O   | 1         | Read enable signal to ID_RAM                 |
| id_rdata           | I   | 5         | Read data signal from ID_RAM                 |
| id_wen             | O   | 1         | Write enable signal to ID_RAM                |
| id_wdata           | O   | 5         | Write data signal to ID_RAM                  |
| hist_addr_train    | O   | 21        | Address signal connected to HIST_RAM_TRAIN   |
| hist_wen_train     | O   | 1         | Write enable signal to HIST_RAM_TRAIN        |
| hist_wdata_train   | O   | 8         | Write data signal to HIST_RAM_TRAIN          |
| hist_ren_train     | O   | 8         | Read enable signal to HIST_RAM_TRAIN         |
| hist_rdata_train   | I   | 8         | Read data signal from HIST_RAM_TRAIN         |
| hist_addr_predict  | O   | 21        | Address signal connected to HIST_RAM_PREDICT |
| hist_wen_predict   | O   | 1         | Write enable signal to HIST_RAM_PREDICT      |
| hist_wdata_predict | O   | 8         | Write data signal to HIST_RAM_PREDICT        |
| hist_ren_predict   | O   | 8         | Read enable signal to HIST_RAM_PREDICT       |
| hist_rdata_predict | I   | 8         | Read data signal from HIST_RAM_PREDICT       |

➤ **Port list of each module:**

➤ **CLBP**

| Signal      | I/O | Bit-width       | Description   |
|-------------|-----|-----------------|---|
| clk         | I   | 1               | Clock signal  |
| rst         | I   | 1               | Reset signal  |
| enable      | I   | 1               | CLBP circuit enabling signal                                      |
| gray_addr   | O   | 12              | Address signal connected to RAM_GRAY                              |
| gray_OE     | O   | 1               | Read enable signal to RAM_GRAY                                    |
| gray_data   | I   | 8               | Read data signal from RAM_GRAY                                    |
| lbp_addr    | O   | 12              | Address signal connected to RAM_LBP <a href="#">MUX to memory</a> |
| lbp_WEN     | O   | 1               | Write enable signal to RAM_LBP                                    |
| lbp_data    | O   | 8               | Write data signal to RAM_LBP                                      |
| theta       | O   | 25(fixed-point) | Current neighbor's theta signal(unit is in radian)                |
| theta_valid | O   | 1               | Indication signal of current neighbor's thetas is valid           |
| cos_data    | I   | 25(fixed-point) | Cosine value of the theta (from testbench)                        |
| cos_valid   | I   | 1               | Indication signal of cosine value is valid                        |
| sin_data    | I   | 25(fixed-point) | Sine value of the theta(from testbench)                           |
| sin_valid   | I   | 1               | Indication signal of sine value is valid                          |
| finish      | O   | 1               | Indication signal of the LBP circuit is finished                  |

## ➤ HCU

| Signal    | I/O | Bit-width | Description  |
|-----------|-----|-----------|--|
| clk       | I   | 1         | Clock signal   |
| rst       | I   | 1         | Reset signal   |
| mode      | I   | 1         | Indication signal of whether the system is in prediction or training phase, 0 is training, 1 is prediction |
| enable    | I   | 1         | HCU circuit enabling signal  |
| gridX     | I   | 4         | Image sliced portion in X direction, value is 8  |
| gridY     | I   | 4         | Image sliced portion in Y direction, value is 8  |
| lbp_addr  | O   | 12        | Address signal connected to RAM_LBP <a href="#">MUX to memory</a>  |
| lbp_ren   | O   | 1         | Read enable signal to RAM_LBP  |
| lbp_rdata | I   | 8         | Read data signal from RAM_LBP  |

| Signal             | I/O | Bit-width | Description  |
|--------------------|-----|-----------|--|
| hist_addr_train    | O   | 21        | Address signal connected to HIST_RAM_TRAIN <a href="#">MUX to memory</a>   |
| hist_wen_train     | O   | 1         | Write enable signal to HIST_RAM_TRAIN  |
| hist_wdata_train   | O   | 8         | Write data signal to HIST_RAM_TRAIN  |
| hist_ren_train     | O   | 8         | Read enable signal to HIST_RAM_TRAIN <a href="#">MUX to memory</a>   |
| hist_rdata_train   | I   | 8         | Read data signal from HIST_RAM_TRAIN   |
| hist_addr_predict  | O   | 21        | Address signal connected to HIST_RAM_PREDICT <a href="#">MUX to memory</a>   |
| hist_wen_predict   | O   | 1         | Write enable signal to HIST_RAM_PREDICT  |
| hist_wdata_predict | O   | 8         | Write data signal to HIST_RAM_PREDICT  |
| hist_ren_predict   | O   | 8         | Read enable signal to HIST_RAM_PREDICT <a href="#">MUX to memory</a>   |
| hist_rdata_predict | I   | 8         | Read data signal from HIST_RAM_PREDICT   |
| done               | O   | 1         | Indication that HCU circuit is done(should be asserted every time a subject picture is finished computing histogram) |

## ➤ Comparator

| Signal           | I/O | Bit-width | Description   |
|------------------|-----|-----------|---|
| clk              | I   | 1         | Clock signal  |
| rst              | I   | 1         | Reset signal  |
| enable           | I   | 1         | Comparator circuit enabling signal  |
| histcount        | I   | 8         | # IDs encountered during training mode  |
| distance         | I   | 1         | DCU computed distance value   |
| dcu_valid        | I   | 1         | Indication that the current distance value is valid   |
| id               | I   | 5         | Id read data from ID_RAM  |
| id_ren           | O   | 1         | Read enable signal to ID_RAM  |
| id_counter       | O   | 8         | The current ID address it is processing <a href="#">MUX to memory</a>                         |
| dcu_enable       | O   | 1         | DCU circuit enabling signal   |
| label            | O   | 5         | Prediction result, output ID value  |
| minDistance      | O   | 18        | Minimum distance between the prediction histogram and the closest histogram in HIST_TRAIN_RAM |
| hist_addr_offset | O   | 21        | The address offset in HIST_RAM_TRAIN of the id it is processing currently                     |
| done             | O   | 1         | Indication signal of the Comparator circuit is finished                                       |



➤ **Controller**

| Signal     | I/O | Bit-width | Description  |
|------------|-----|-----------|--|
| clk        | I   | 1         | Clock signal   |
| rst        | I   | 1         | Reset signal   |
| mode       | I   | 1         | Indication signal of whether the system is in prediction or training phase, 0 is training, 1 is prediction |
| enable     | I   | 1         | Comparator circuit enabling signal   |
| valid      | I   | 1         | Indication that current subject ID is valid  |
| id         | I   | 5         | Subject ID   |
| id_addr    | O   | 8         | Address signal connected to ID_RAM <a href="#">MUX to memory</a>   |
| id_wen     | O   | 1         | Write enable signal to ID_RAM  |
| id_wdata   | O   | 5         | Write data signal to ID_RAM  |
| lbp_enable | O   | 1         | CLBP circuit enabling signal   |
| lbp_finish | I   | 1         | Indication of the CLBP circuit is finished   |
| ram_clbp   | O   | 1         | Indication that the CLBP circuit has the access to RAM_LBP   |

| Signal            | I/O | Bit-width | Description   |
|-------------------|-----|-----------|---|
| gridX_i           | I   | 4         | Image sliced portion in X direction, value is 8, from testbench   |
| gridY_i           | I   | 4         | Image sliced portion in Y direction, value is 8, from testbench   |
| hcu_enable        | O   | 1         | HCU circuit enabling signal   |
| gridX_o           | O   | 4         | Image sliced portion in X direction, value is 8, to HCU   |
| gridY_o           | O   | 4         | Image sliced portion in Y direction, value is 8, to HCU   |
| hcu_finish        | I   | 1         | Indication of the HCU circuit is finished   |
| comparator_finish | I   | 1         | Indication of the Comparator circuit is finished  |
| comparator_enable | O   | 1         | Comparator circuit enabling signal  |
| ram_comp          | O   | 1         | Indication that the Comparator circuit & DCU circuit has the access to ID_RAM, HIST_RAM_TRAIN, HIST_RAM_PREDICT |

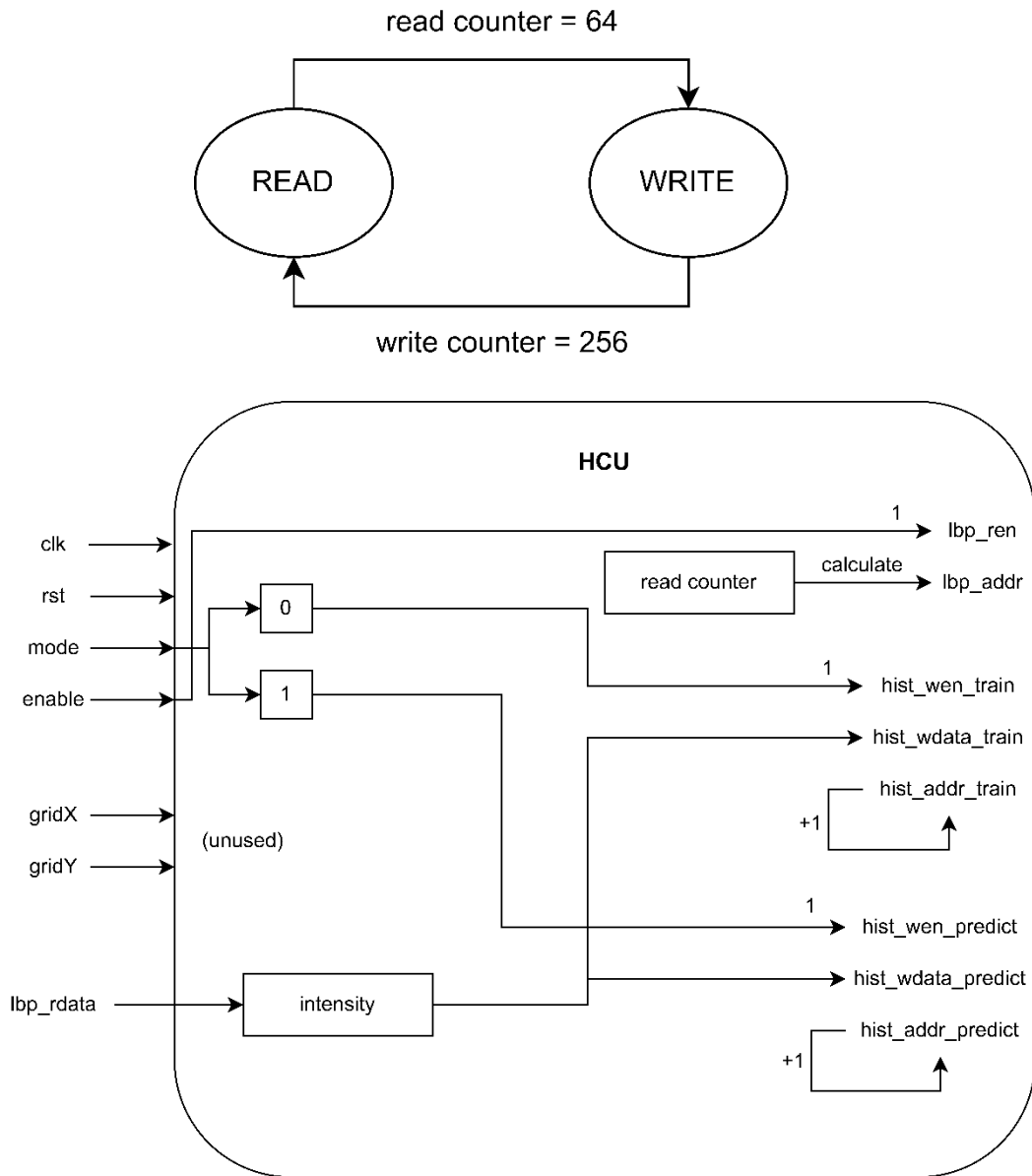
➤ Understanding the function:

Once system is initialized, it

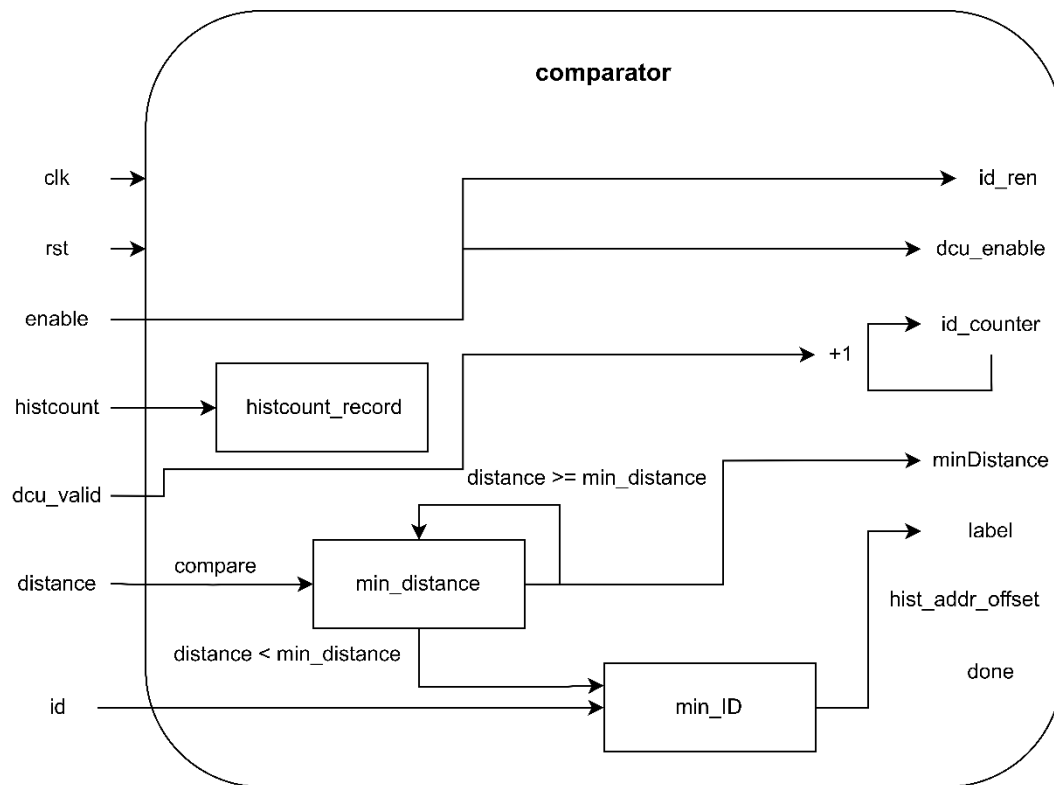
- a) Receives *gridX* and *gridY* signal.
- b) Receive *valid* and *id* signal, then compute local binary pattern value and store the result into RAM\_LBP.
- c) In training mode, computes histogram information from RAM\_LBP and store it to HIST\_RAM\_TRAIN.
- d) Repeat step(b)~(c) until encounter prediction mode.
- e) Prediction mode is detected, goes to step(b).
- f) In prediction mode, computes histogram information from RAM\_LBP and store it to HIST\_RAM\_PREDICT.
- g) Comparator starts to work, control DCU to compute D, where D is defined as:
$$D = \sum_{p=1}^n (hist\_predict_p - hist\_train_p)^2$$
, where n is 16384(8x8x256).
- h) Loop step(g) for 7xN times, where N is the different subject count, and find the closest histogram in HIST\_RAM\_PREDICT w.r.t the prediction histogram computed in step(f), see p.18 in handout.
- i) Output *label* & *minDistance* & *done* signal.
- j) Repeat step(e)~(i) until testbench stops the simulation.



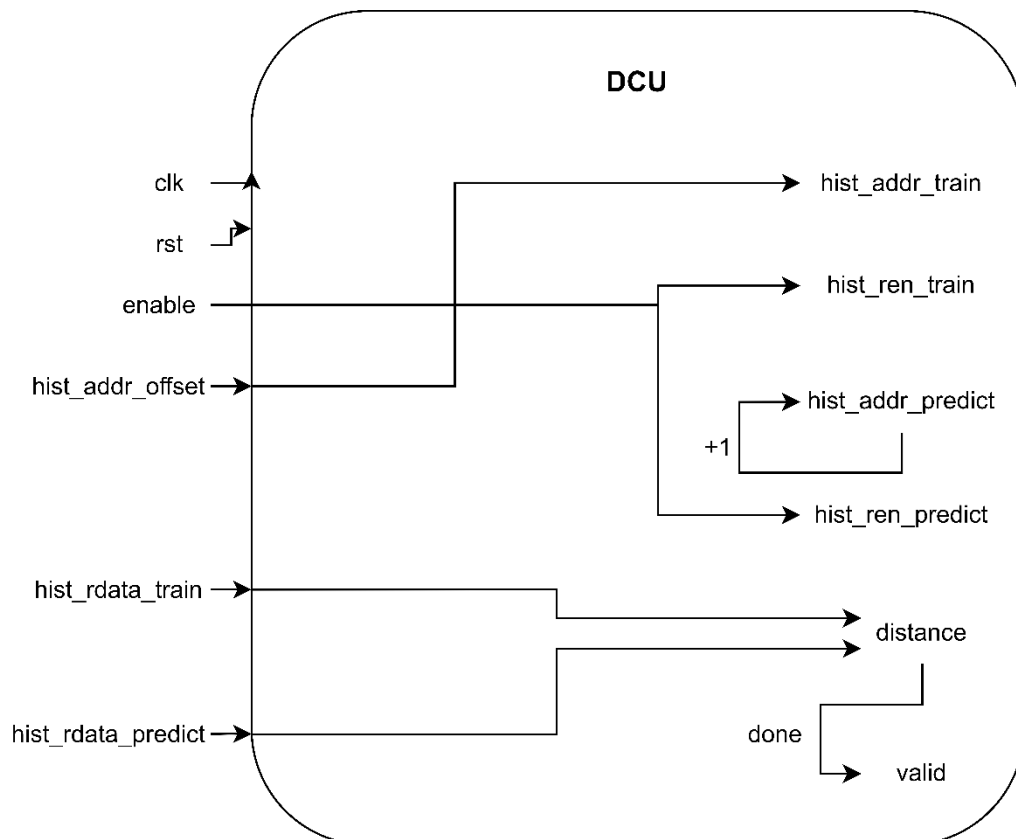
■ HCU



## ■ Comparator

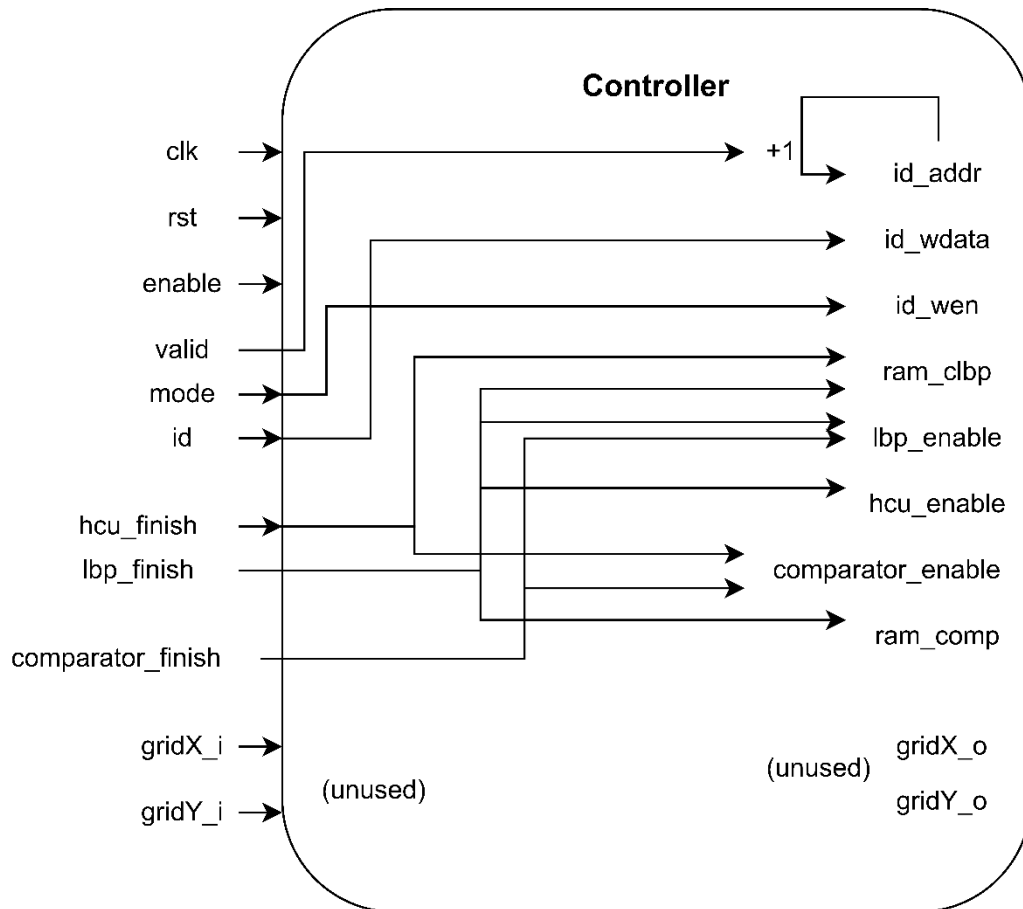


## ■ DCU



■ Controller

- ◆ Draw your state diagram in controller and explain it



■ Your own internal architecture

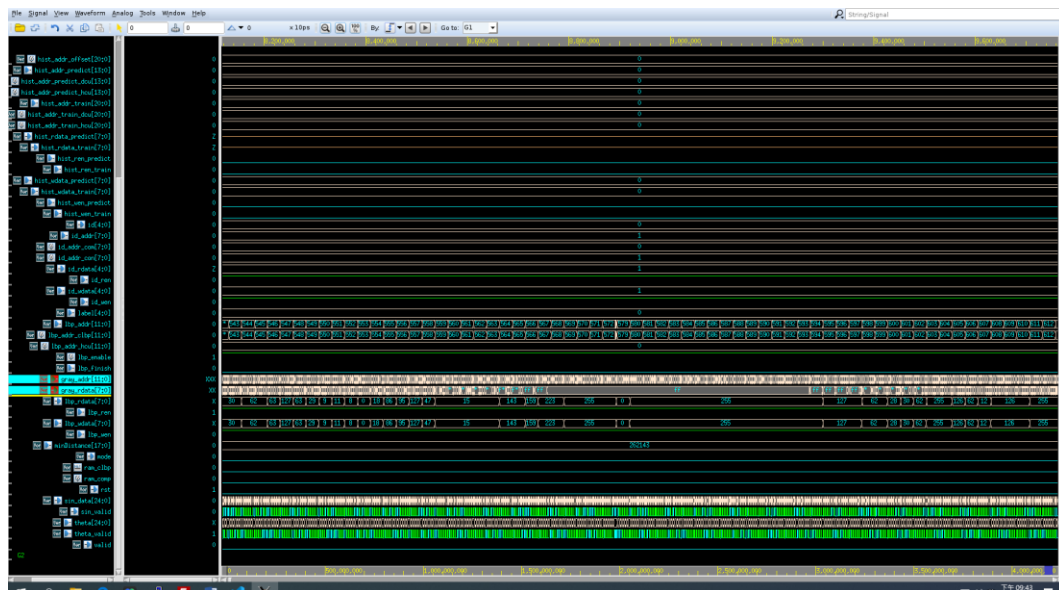
- ◆ Draw and explain if you design your own architecture, if don't, you can skip this section.

1) Complete the Controller, HCU, CLBP, DCU, Comparator, and TOP module, in the system. **If you design your own architecture, please add the submodule list here!**

Submodule list:

1. ...
- 2) Compile the verilog code to verify the operations of this module works properly.
- 3) Synthesize your *top.v* with following the constraints:
  - Clock period: no more than **2.0 ns**.
  - Don't touch network: `clk`.
  - Wire load model: Wire load model: N16ADFP\_StdCells0p72vm40c.
  - Synthesized verilog file: *top\_syn.v*.
  - Timing constraint file: *top\_syn.sdf*.

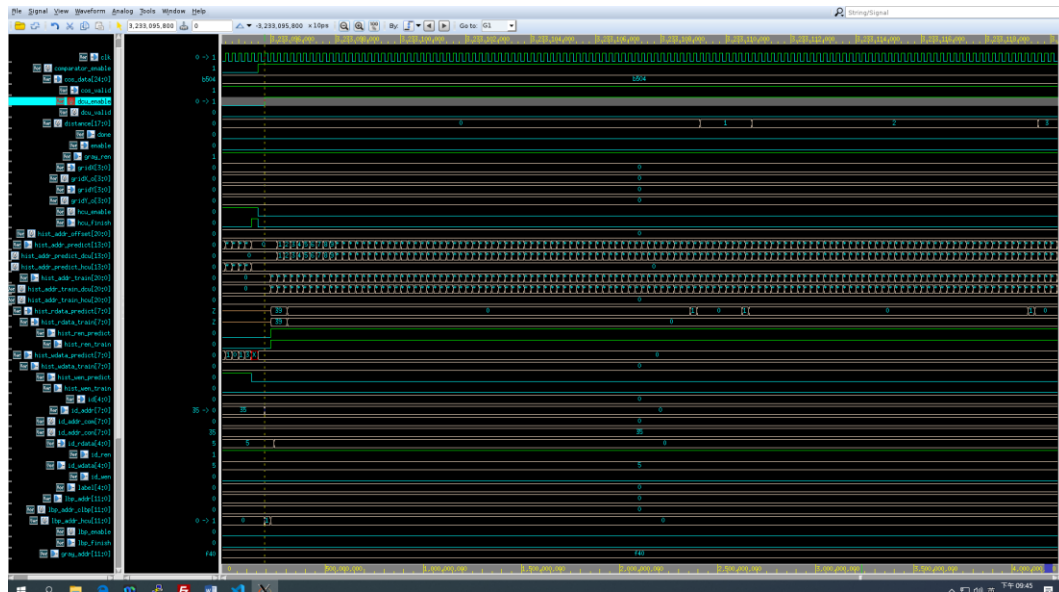
Lbp calculate



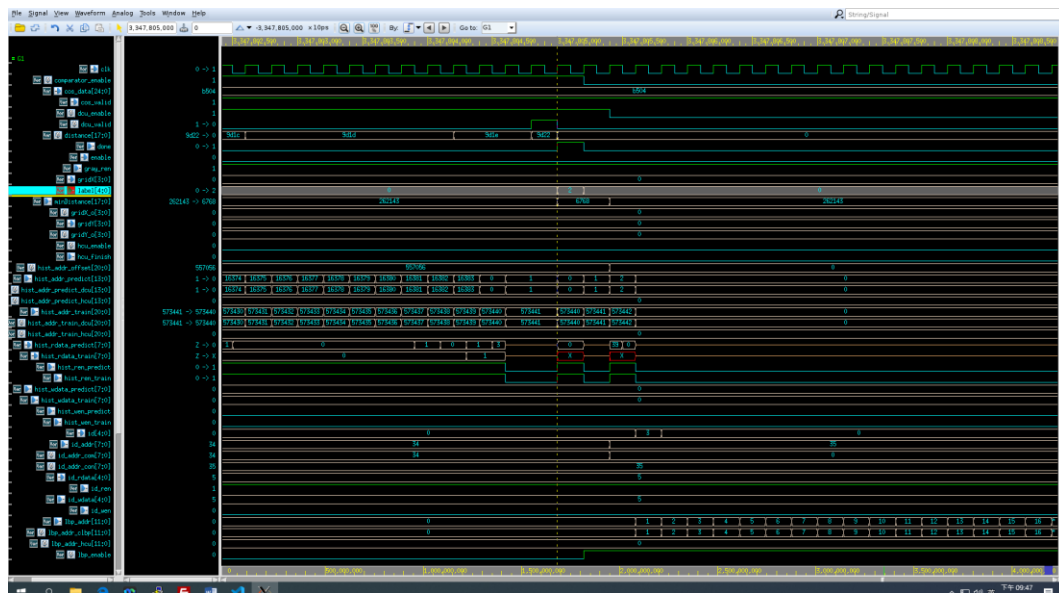
The screenshot shows the Signal View application interface. On the left, a tree view lists variables under the 'Signal View' window. The variables include:

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Dcu calculate



Output minDistance and label





## Pre-sim

```

140.116.156.6 - PuTTY

*****
** Prediction of Subject 4 PASS!! **
*****

*****
**                                     **
** Congratulations !!               **
**                                     **
** Simulation PASS!!                **
**                                     **
**                                     **
*****
                                     \m__m_|_|

total simulation time: 41658700 ns
$finish called from file "top_tb.sv", line 640.
$finish at simulation time          4165874400
      V C S   S i m u l a t i o n   R e p o r t
Time: 41658744000 ps
CPU Time:      230.580 seconds;          Data structure size:   4.1Mb
Wed May 1 22:10:46 2024
CPU time: 1.051 seconds to compile + .613 seconds to elab + .406 seconds to link
+ 230.629 seconds in simulation
vlsicad6:/home/user2/vlsi24/vlsi2424/Lab7 E24116152/sim %

```

## Post-sim

```

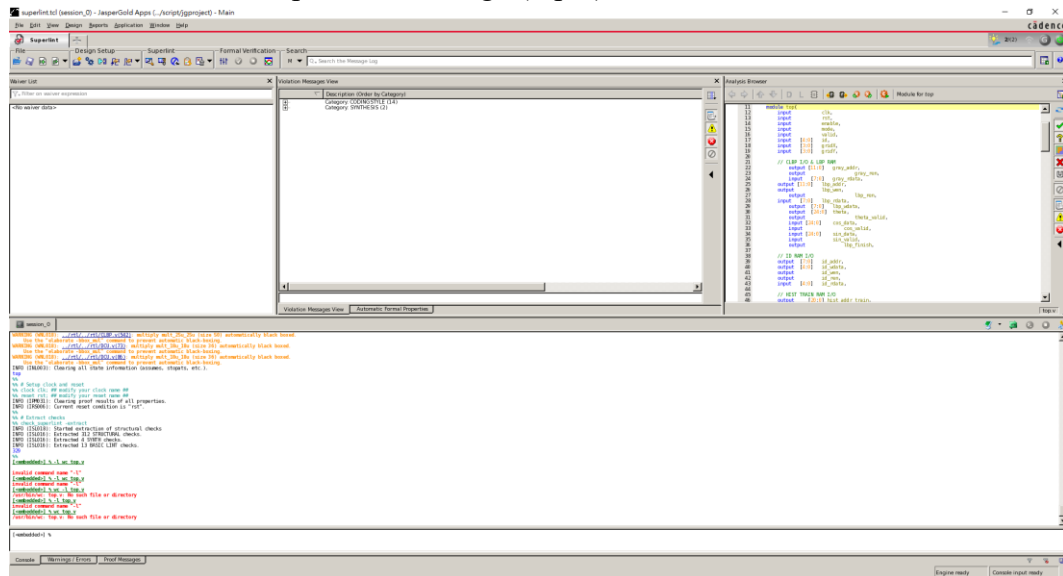
===== Prediction begins!!! =====
Prediction of subject P:          2 with pic T:          9.
Prediction sholud be  2, your answer is  2.
minDistance sholud be  6768, your answer is 262143.

*****
** Prediction of Subject 2 FAILED!! **
*****

$finish called from file "top_tb.sv", line 609.
$finish at simulation time      33478060036
      V C S  S i m u l a t i o n  R e p o r t
Time: 33478060036 ps
CPU Time:  3556.390 seconds;      Data structure size: 11.0Mb
Fri May  3 10:51:34 2024
CPU time: 17.443 seconds to compile + 2.184 seconds to elab + 1.095 seconds to l
ink + 3556.433 seconds in simulation
vlsicad6:/home/user2/vlsi24/vlsi2424/Lab7 E24116152/sim %

```

## 6) Show SuperLint coverage (top.v)



SuperLint coverage = 82.43%

## 7) Your clock period, total cell area, post simulation time (top.v) in screenshot.

Clock period: 0.34

| Report.1 - Timing                               |       |        |
|---|-------|--------|
| hcu/U4013/ZN (ND2D1BWP16P90LVT)                 | 0.08  | 1.50 f |
| hcu/U4012/Z (BUFFD1BWP16P90LVT)                 | 0.06  | 1.56 f |
| hcu/U1334/ZN (OA122D1BWP16P90LVT)               | 0.02  | 1.58 r |
| hcu/U1612/ZN (NR4D1BWP16P90LVT)                 | 0.01  | 1.59 f |
| hcu/U1083/ZN (OA122D1BWP16P90LVT)               | 0.01  | 1.60 r |
| hcu/U1080/ZN (NR4D1BWP16P90LVT)                 | 0.01  | 1.61 f |
| hcu/U1428/ZN (ND4D1BWP16P90LVT)                 | 0.01  | 1.63 r |
| hcu/add_399/A[0] (HCU_DW01_inc_5)               | 0.00  | 1.63 r |
| hcu/add_399/U1_1_1/CO (HA1D1BWP16P90LVT)        | 0.02  | 1.65 r |
| hcu/add_399/U1_1_2/CO (HA1D1BWP16P90LVT)        | 0.02  | 1.66 r |
| hcu/add_399/U1_1_3/CO (HA1D1BWP16P90LVT)        | 0.02  | 1.68 r |
| hcu/add_399/U1_1_4/CO (HA1D1BWP16P90LVT)        | 0.02  | 1.70 r |
| hcu/add_399/U1_1_5/CO (HA1D1BWP16P90LVT)        | 0.02  | 1.71 r |
| hcu/add_399/U1_1_6/CO (HA1D1BWP16P90LVT)        | 0.02  | 1.73 r |
| hcu/add_399/U1/Z (XOR2D1BWP16P90)               | 0.02  | 1.75 r |
| hcu/add_399/SUM[7] (HCU_DW01_inc_5)             | 0.00  | 1.75 r |
| hcu/U1293/ZN (AO122D1BWP16P90LVT)               | 0.01  | 1.76 f |
| hcu/U1183/Z (BUFFD1BWP16P90LVT)                 | 0.01  | 1.77 f |
| hcu/U893/Z (BUFFD1BWP16P90LVT)                  | 0.01  | 1.78 f |
| hcu/U656/Z (BUFFD1BWP16P90LVT)                  | 0.01  | 1.79 f |
| hcu/U251/Z (BUFFD1BWP16P90LVT)                  | 0.02  | 1.81 f |
| hcu/U2052/ZN (OA122D1BWP16P90LVT)               | 0.01  | 1.83 r |
| hcu/intensity_reg[154][7]/D (DFQD2BWP16P90LVT)  | 0.00  | 1.83 r |
| data arrival time                               |       | 1.83   |
| clock clk (rise edge)                           | 2.00  | 2.00   |
| clock network delay (ideal)                     | 0.20  | 2.20   |
| clock uncertainty                               | -0.02 | 2.18   |
| hcu/intensity_reg[154][7]/CP (DFQD2BWP16P90LVT) | 0.00  | 2.18 r |
| library setup time                              | -0.01 | 2.17   |
| data required time                              |       | 2.17   |
| data required time                              |       | 2.17   |
| data arrival time                               |       | -1.83  |
| slack (MET)                                     |       | 0.34   |
| ***** End Of Report *****                       |       |        |

Total cell area: 9791.280244

```
Report.2 - Area
*****
Report : area
Design : top
Version: 0-2018.06
Date   : Fri May  3 09:49:45 2024
*****

Library(s) Used:

N16ADFP_StdCells0p72vm40c (File: /usr/cad/CBDK/Executable_Package/Collaterals/IP/

Number of ports:          3929
Number of nets:          26005
Number of cells:         21140
Number of combinational cells: 18084
Number of sequential cells:  2997
Number of macros/black boxes:  0
Number of buf/inv:        4563
Number of references:      13

Combinational area:      6933.133638
Buf/Inv area:            753.857306
Noncombinational area:   2858.146605
Macro/Black Box area:    0.000000
Net Interconnect area:   undefined (Wire load has zero net area)

Total cell area:         9791.280244
Total area:              undefined

**** End Of Report ****
```

Post simulation time:

8) Please describe how you optimize your design when you run into problems in synthesis .ex: plug in some registers between two instances to shorten your datapath, resource sharing for some registers to reduce your cell area.

I add all the incoming values sequentially to a register, so I don't need to read values from the predict RAM and train RAM.

➤ Lessons learned from this lab

This lab focused on histogram and prediction, providing valuable experience in Verilog programming for signal handling and logic design. It enhanced my ability to describe digital circuits and work on practical implementations. The project also improved my problem-solving skills.

➤ Suggestions for us (we appreciate your feedback)

The diagram in the lecture notes could be labeled more clearly.

Please compress all the following files into one compressed file (".tar " format) and submit through Moodle website:

❌ **NOTE:**

1. **If there are other files used in your design, please attach the files too and make sure they're properly included.**
2. Simulation commands

| Lab7          | Commands   |
|---------------|--|
| superlint     | % cd script<br>% jg -superlint superlint.tcl                                       |
| synthesis     | % cd script<br>% dv -f synthesis.tcl   |
| Pre-sim       | % cd sim<br>% vcs -R -sverilog top_tb.sv -debug_access+all -full64                 |
| Post-sim      | % cd sim<br>% vcs -R -sverilog top_tb.sv -debug_access+all -full64 +define+SDF+SYN |
| Dump waveform | +define+FSDB   |

Don't use +define+FSDB when running post-sim, it'll occupy substantial amount of memory!