**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2024)***

**Lab Session 4**

**Register Files, Manhattan Distance and LFSR**

|  |  |  |
| --- | --- | --- |
| Name | Student ID | |
| 劉冠妤 | E24116152 | |
| **Practical Sections** | **Points** | **Marks** |
| Prob A | 30 |  |
| Prob B | 30 |  |
| Prob C | 20 |  |
| Report | 15 |  |
| File hierarchy, naming…etc. | 5 |  |
| Notes: | | |

**Due Date: 15:00, March 27, 2024 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should be uploaded in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body which we can’t even compile you will get NO credit!**
3. **All Verilog file should get at least 90% superLint Coverage.**
4. **File hierarchy should not be changed; it may cause** your code can not be recompiled by TA successfully using the autograding commands

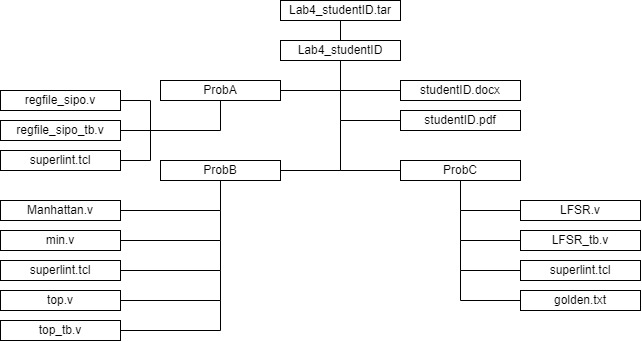


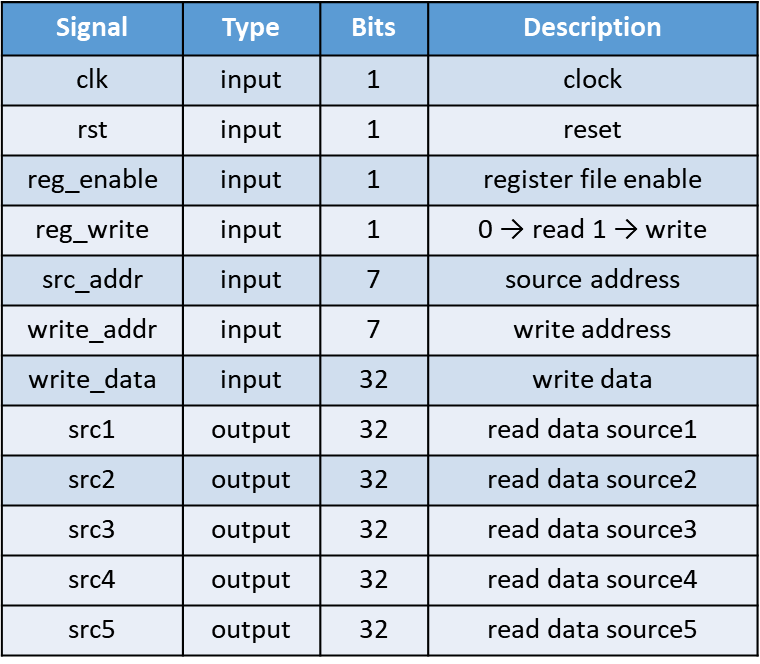
Fig.1 File hierarchy for Homework submission

Prob A: SIPO Register File

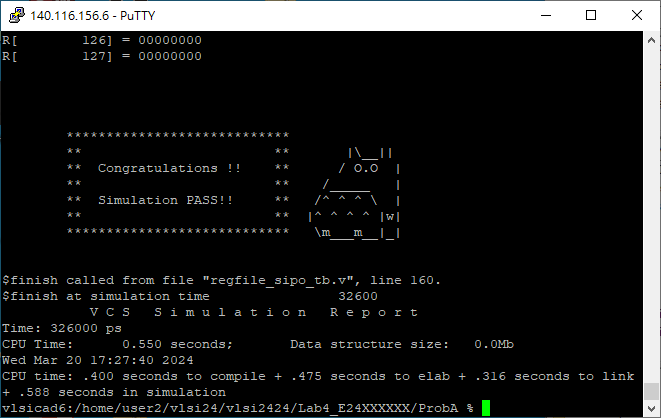
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自動產生的描述

1. Based on the SIPO register file structure in LabA, please design a 128 x 32 SIPO register file with 5 output ports.
2. Port list



1. Show the simulation result on the terminal.



1. Show waveforms to explain that your register work correctly when read and write.

When the pulse is triggered on the positive edge, and the register file is enabled and in read mode, src\_addr = 1 → write\_data is written into src1一張含有 螢幕擷取畫面, 電腦, 軟體, 陳列 的圖片

自動產生的描述

When the pulse is triggered on the positive edge, and the register file is enabled and in read mode, src\_addr = 2 → write\_data is written into src2

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自動產生的描述

When the pulse is triggered on the positive edge, and the register file is enabled and in read mode, src\_addr = 3 → write\_data is written into src3

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自動產生的描述

When the pulse is triggered on the positive edge, and the register file is enabled and in read mode, src\_addr = 4 → write\_data is written into src4

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自動產生的描述

When the pulse is triggered on the positive edge, and the register file is enabled and in read mode, src\_addr = 5 → write\_data is written into src5

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自動產生的描述

We can understand the operation of Serial-In Parallel-Out Register File through waveform diagrams. The latter part of the waveform diagram is reading. When the clock signal rises along the positive edge, the read value is output.

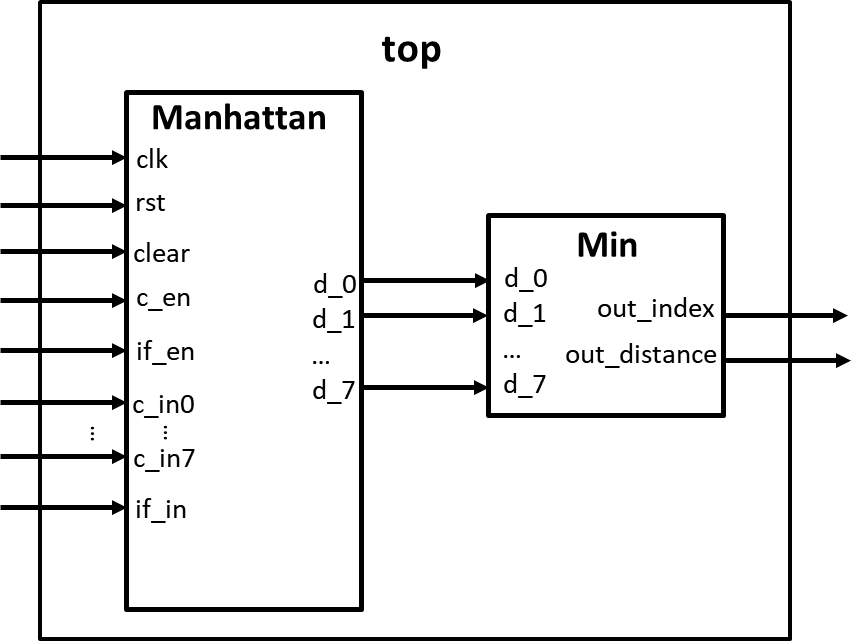
1. Show SuperLint coverage

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自動產生的描述

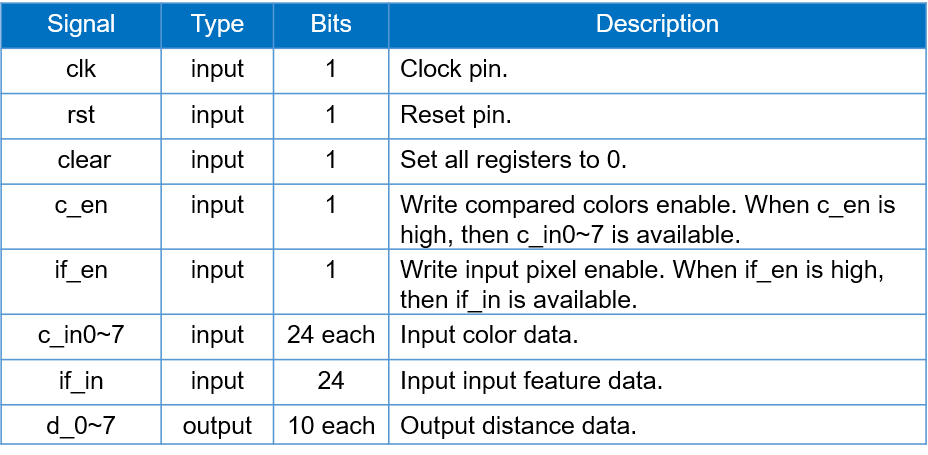
Coverage = 98.38%

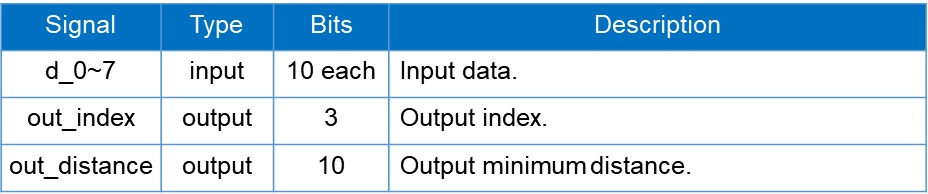
Prob B: Finding Smallest Distance



1. Please design a circuit that will find the smallest distance between the input feature and input colors, based on the structure given in the LAB4 slide.
2. Port list

Manhattan:

Min:



1. Show the simulation result on the terminal.

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自動產生的描述

1. Show waveforms to explain that your design works correctly.

From the waveform diagram, we can see that after the data is read in first, the calculated minimum distance and indexs are output only when the positive edge is triggered.

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自動產生的描述

But when the clear signal is positive, it is not triggered with the positive edge of the clock, because this is my design.

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自動產生的描述

Under normal circumstances, the changes are triggered by the positive edge of the clock signal.

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自動產生的描述

1. Show SuperLint coverage

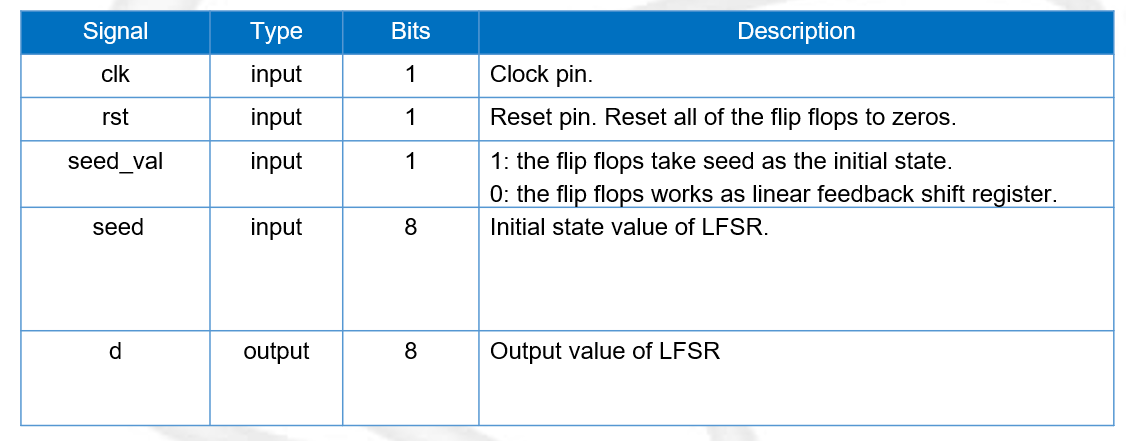
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自動產生的描述

Coverage = 98.61%

Prob C: LFSR

1. Please design an 8-bit-LFSR, with the given feedback function in the LAB4 slide.
2. Port list



1. Feedback function

***d[0] = ( d[7] ^ d[5] ) ^ ( d[4] ^ d[2] )***

1. Show waveforms to explain that your LFSR module works correctly.

Take this wave pattern as an example:

d = 1111\_1011, seed\_val = 0

On the positive edge of the next clock signal, d shift left one bit, and d[0] is equal to (d[7]^d[5]) ^ (d[4] ^ d[2]) which is (1^1)^(1^0) = 1.

So the next d = 1111\_0111, the waveform results are consistent with the expected results.

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自動產生的描述

1. Show the simulation result on the terminal.

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自動產生的描述

1. Show SuperLint coverage

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自動產生的描述

Coverage = 100%

At last, please write the lesson you learned from Lab4

In this experiment, I learned what Serial-In Parallel-Out Register is. Although this is something I have never been exposed to before, the lecture notes are very clear and easy to understand. In addition, I also learned about Manhattan distance and applied it in practice. I found that the concepts of blocking and nonblocking in Verilog are very important, because I made many mistakes in the experiment because of unclear concepts. Finally, I learned the principle and practical application of Linear feedback shift register, and I found that it was not as difficult as I thought. After these implementations, I am more familiar with Verilog’s syntax and design concepts.

Appendix A : Commands we will use to check your homework

