**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2024)***

**Lab Session 7**

**Design of Local Binary Pattern Facial Recognition System**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Student ID | | |
| 劉冠妤 | E24116152 | | |
| Practical | | Points | Marks |
| Lab 7\_1 | | 30 |  |
| Lab 7\_2 | | 65 |  |
| Report | | 5 |  |
| Demo | | 10 |  |
| Notes | |  |  |

**Due: 15:00 May 1, 2024@ moodle**

**Summary**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | |
| TOP | | | RTL(ˇ/X) | | | Synthesis(ˇ/X) |
| Lab7\_1 | | | ˇ | | | ˇ |
| Lab7\_2 | | | ˇ | | | X |
| Synthesis result | | | | | | |
| Clock period(ns) | Area | | | Simulation time (ns) | | |
| 0.34 | 9791.280244 | | | 33478060036 | | |
| Superlint(number of inline messages, just write down the final design result, i.e. if you only finish lab7\_1, write your Superlint result of lab7\_1, otherwise, write down lab7\_2 only) | | | | | | |
| Total lines | Warning | Error | | | coverage(%) | |
| 1873 | 329 | 0 | | | 82.43% | |

**Note: You must complete and fill out this form with your design information!!!**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should be uploaded in this file hierarchy.
2. NOTE: 1. Please **DO NOT** upload waveforms (.fsdb or .vcd)!
3. **If you upload a dead body which we can’t even compile, you will get NO credit!**
4. **All Verilog file should get at least 90% SuperLint Coverage.**
5. All homework requirements should be uploaded in this file hierarchy or you will not get full credit, if you want to use some sub modules in your design but you do not include them in your tar file, you will get 0 point.

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自動產生的描述

Fig.1 File hierarchy for Homework submission

Lab 7

You are about to integrate all components (CLBP, HCU, Controller…) to form a LBP facial recognition system. The block diagram of system is as shown in **Fig2** and **Fig3**.

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自動產生的描述

▲Fig2. The block diagram of system (external)

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自動產生的描述**

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自動產生的描述**

▲Fig3. The block diagram of system (internal)

* **Port list of top module:**
* TOP

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* **Port list of each module:**
* CLBP

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* **HCU**

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* **Comparator**

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自動產生的描述**

* **Controller**

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自動產生的描述**

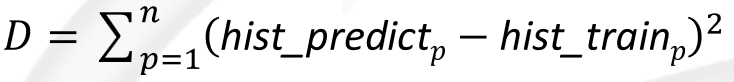
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自動產生的描述**

* Understanding the function:

Once system is initialized, it

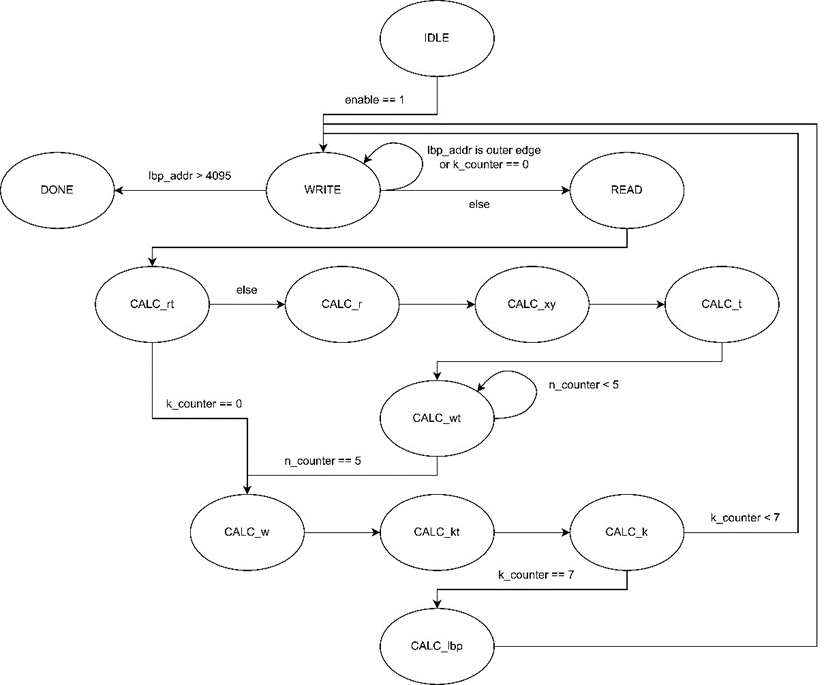
* 1. Receives *gridX* and *gridY* signal.
  2. Receive *valid* and *id* signal, then compute local binary pattern value and store the result into RAM\_LBP.
  3. In training mode, computes histogram information from RAM\_LBP and store it to HIST\_RAM\_TRAIN.
  4. Repeat step(b)~(c) until encounter prediction mode.
  5. Prediction mode is detected, goes to step(b).
  6. In prediction mode, computes histogram information from RAM\_LBP and store it to HIST\_RAM\_PREDICT.
  7. Comparator starts to work, control DCU to compute D, where D is defined as:

, where n is 16384(8x8x256).

* 1. Loop step(g) for 7xN times, where N is the different subject count, and find the closest histogram in HIST\_RAM\_PREDICT w.r.t the prediction histogram computed in step(f), see p.18 in handout.
  2. Output *label* & *minDistance* & *done* signal.
  3. Repeat step(e)~(i) until testbench stops the simulation.
* Describe your design in detail. You can draw internal architecture or block diagram to describe your dsign. If your submodule contains any FSM, you should also depict it and elaborate as well.

**Note**: **if you design your own internal architecture** other than using the provided one, please feel free to **alter the block** below, and add your own design as well as decribe them in detail.

* + CLBP

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自動產生的描述

* + HCU

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自動產生的描述

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自動產生的描述

* + Comparator

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自動產生的描述

* + DCU

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自動產生的描述

* + Controller
    - Draw your state diagram in controller and explain it

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自動產生的描述

* + Your own internal architecture
    - Draw and explain if you design your own architecture, if don’t, you can skip this section.

1. Complete the Controller, HCU, CLBP, DCU, Comparator, and TOP module, in the system. **If you design your own architecture, please add the submodule list here!**

Submodule list:

1. …
2. Compile the verilog code to verify the operations of this module works properly.
3. Synthesize your *top.v* with following the constraints:

* Clock period: no more than 2.0 ns.
* Don’t touch network: clk.
* Wire load model: Wire load model: N16ADFP\_StdCellss0p72vm40c.
* Synthesized verilog file: *top\_syn.v*.
* Timing constraint file: *top\_syn.sdf*.

1. Please **attach your waveforms** and **specify your operations** on the waveforms. The more you elaborate, the higher the score is.

Lbp calculate

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自動產生的描述

Hcu calculate read write into ram\_train and ram\_predict

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自動產生的描述

Dcu calculate

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自動產生的描述

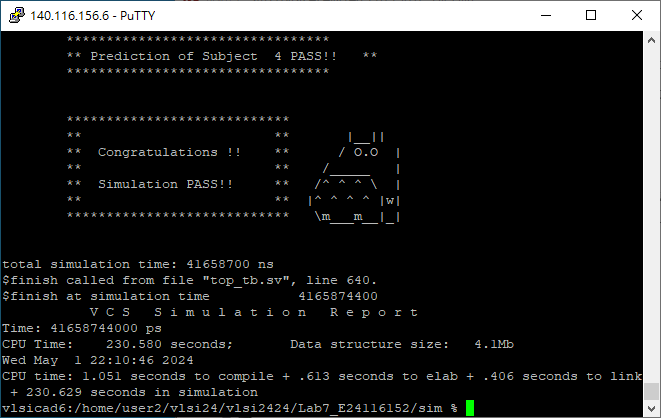
Output minDistance and label

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自動產生的描述

1. Show simulation result

Pre-sim



Post-sim一張含有 文字, 螢幕擷取畫面, 軟體, 陳列 的圖片

自動產生的描述

1. Show SuperLint coverage (top.v)

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自動產生的描述

SuperLint coverage = 82.43%

1. Your clock period, total cell area, post simulation time (top.v) in screenshot.

Clock period: 0.34

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自動產生的描述

Total cell area: 9791.280244

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自動產生的描述

Post simulation time:

1. Please describe how you optimize your design when you run into problems in synthesis .ex: plug in some registers between two instances to shorten your datapath, resource sharing for some registers to reduce your cell area.

I add all the incoming values sequentially to a register, so I don't need to read values from the predict RAM and train RAM.

* Lessons learned from this lab

This lab focused on histogram and prediction, providing valuable experience in Verilog programming for signal handling and logic design. It enhanced my ability to describe digital circuits and work on practical implementations. The project also improved my problem-solving skills.

* Suggestions for us (we appreciate your feedback)

The diagram in the lecture notes could be labeled more clearly.

Please compress all the following files into one compressed file (“.tar “ format) and submit through Moodle website:

※ **NOTE**:

1. **If there are other files used in your design, please attach the files too and make sure they’re properly included**.
2. Simulation commands

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自動產生的描述