Design of an Operational Amplifier Input Stage Immune to EMI

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***Abstract*—This paper presents a new analytical model to predict upsets, which are induced by electromagnetic interferences (EMI) in CMOS operational amplifiers (opamps). In particular, it is pointed out that the demodulation of EMI, which is experienced in feedback CMOS opamps, is related to the power spectral density of the interfering signals reaching the opamp input terminals. Furthermore, the new model is employed to design a differential stage immune to EMI.**

***Index Terms*—Electromagnetic interference (EMI), electromagnetic susceptibility, integrated circuits, nonlinear model, operational amplifier.**

I. Introduction

THE ELECTROMAGNETIC emission delivered by modern electronic equipment has significantly increased the level of electromagnetic pollution, and the amplitude of radio-frequency interference (RFI), which is collected by electronic system harnesses, can be higher than that of nominal signals. Currently, the amplitude of RFI reaching ICs is kept under control by electromagnetic interference (EMI) filters and electromagnetic shields, which are usually employed at printed circuit board (PCB) or system level. The use of these components does not guarantee the compliance to electromagnetic compatibility (EMC) specifications, and sometimes, susceptibility issues come out just before production. In addition, EMI filters cannot be included into electronic modules, like automotive ones, where a seamless integration of microelectronic devices (like system-on-chip) and mechanical parts is required, and where PCBs are usually missing [1]. As a consequence, in the last few years, the interest to fulfill EMC specifications by a proper design of ICs has significantly increased, and although some design rules are already known [2], the subject of susceptibility of analog and digital ICs to EMI deserves further investigation.

In this paper, the demodulation of EMI, which is operated by feedback operational amplifiers (opamps), is investigated, and unlike previous works [3], a new model that is valid for any kind of interfering signals is presented. In addition, such a model is employed in the design of a new opamp input stage to achieve the immunity to EMI.

The paper is organized as follows. In Section II, the distortion of EMI in a MOS differential pair is discussed, and a new analytical model is presented. In Section III, a new circuit topology, which is immune to EMI, is described, and its performance in terms of RFI demodulation is compared in Section IV with that of other circuit topologies. Finally, in Section V, some concluding remarks are drawn.

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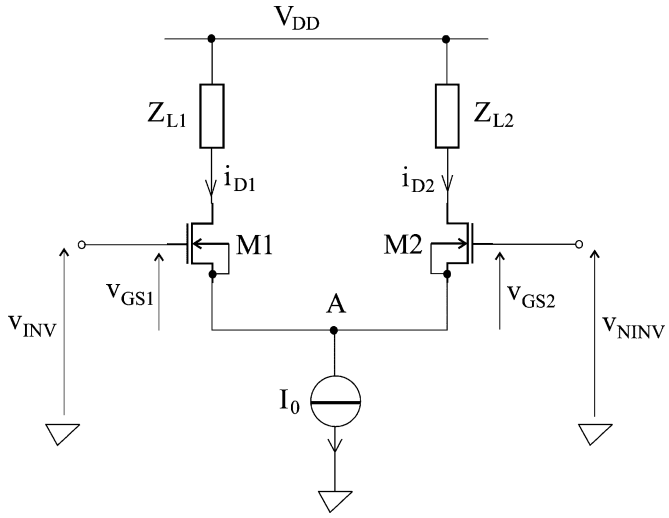

Fig. 1. Basic nMOS differential pair.

II. Susceptibility to EMI of CMOS Opamps

As mentioned in the introduction, feedback opamps demodulate EMI, and in the case of sinusoidal interference of constant amplitude and frequency a dc output offset voltage is experienced [4], [5]. Furthermore, other works have shown that EMI is demodulated mostly in the opamp input differential pair, and some analytical models describing the interaction of transistor nonlinearities and parasitic elements have been presented [3], [6]. However, these models are valid only for sinusoidal interfering signals that do not describe all possible disturbances. To this purpose, the following sections show a new simple and effective model for the prediction of EMI-induced upset in a MOS differential stage, which is suitable for any kind of interfering signal waveform.

A. EMI Distortion in MOS Differential Pair

Common CMOS opamps are composed of cascaded amplifying stages, the first of which is usually a differential pair (see Fig. 1) that amplifies the difference of the input voltages $v_{\rm INV}$ and $v_{\rm NINV}$

$$v_D = v_{\rm NINV} - v_{\rm INV} \tag{1}$$

while rejecting the common-mode voltage

$$v_{\rm CM} = \frac{v_{\rm NINV} + v_{\rm INV}}{2}. \tag{2}$$

Under the assumption of perfect matching of both transistors (M1, M2) and loads ($Z_{\rm L1}$, $Z_{\rm L2}$), and considering the input signal spectra within the differential pair bandwidth, the output current

$$i_D = i_{D1} - i_{D2} \tag{3}$$

is not affected by the common-mode input signal. However, the simultaneous presence of out-of-band common- and differential-mode input signals cause this property to fail. To this purpose, under the assumption that the transistors M1 and M2 are always biased in the saturation region, their drain currents can be expressed as

$$i_{Di} = \beta(v_{\rm GSi} - V_{\rm TH})^2, \qquad i = 1, 2 \tag{4}$$

in which

$$\beta = \frac{\mu_{\rm n} C_{\rm ox}}{2} \frac{W}{L} \tag{5}$$

where $\mu_{\rm n}$ is the mobility of electrons in nMOS devices, $C_{\rm ox}$ is the capacitance of the gate oxide per unit area, W and L are, respectively, the width and the length of the gate area, $V_{\rm TH}$ is the threshold voltage, while $v_{\rm GSi}$ is the gate-source voltage. Such voltages are expressed in the following as:

$$v_{\rm GSi} = \overline{v}_{\rm GSi} + v_{\rm gsi}(t), \qquad i = 1, 2 \tag{6}$$

where $\overline{v}_{\rm GSi}$ is the mean value of the gate-source voltage, and $v_{\rm gsi}(t)$ is the time-variant term, whose mean value is zero. On the basis of (6), the mean value of the differential output current can be written as

$$\overline{i}_D = \overline{i}_{D1} - \overline{i}_{D2} \tag{7}$$

where

$$\overline{i}_{Di} = \beta\big[(\overline{v}_{\rm GSi} - V_{\rm TH})^2 + \overline{v_{\rm gsi}^2}\big], \qquad i = 1, 2 \tag{8}$$

in which $\overline{v_{\rm gsi}^2}$ is the mean-square value of the gate-source voltage.

Assuming now that the input voltage sources $v_{\rm NINV}$ and $v_{\rm INV}$ have the same mean value ($\overline{v}_D = 0$), the gate-source voltages equal each other ($\overline{v}_{\rm GS1} = \overline{v}_{\rm GS2}$), and the mean value of the differential output current takes the form

$$\overline{i}_D = \beta\big(\overline{v_{\rm gs1}^2} - \overline{v_{\rm gs2}^2}\big) \tag{9}$$

while the bias current of the differential stage can be written as

$$I_0 = \beta\big[2\,(\overline{v}_{\rm GS1} - V_{\rm TH})^2 + \overline{v_{\rm gs1}^2} + \overline{v_{\rm gs2}^2}\big]. \tag{10}$$

In these equations, $\overline{v}_{\rm GS1}$, $\overline{v_{\rm gs1}^2}$, and $\overline{v_{\rm gs2}^2}$ are unknowns, and they are expressed in the following in terms of their power spectral density (PSD).

To this purpose, the mean-square value of the gate-source voltage ($\overline{v_{\rm gsi}^2}$) can be written as

$$\overline{v_{\rm gsi}^2} = \int_{-\infty}^{+\infty} S_{V_{\rm gsi}}(\omega)\, d\omega \tag{11}$$

where $S_{V_{\rm gsi}}(\omega)$ is the PSD of the gate-source that takes the form

$$S_{V_{\rm gsi}}(\omega) = V_{\rm GSi}(\omega) V_{\rm GSi}^{\star}(\omega), \qquad i = 1, 2 \tag{12}$$

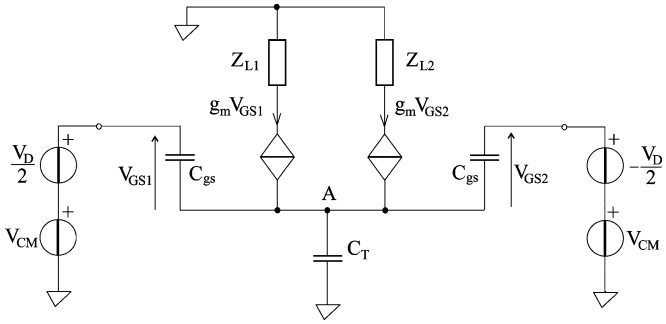

Fig. 2. Small signal equivalent circuit of the differential pair.

where $V_{\rm GSi}(\omega)$ is the Fourier transform of the ith gate-source voltage, which can be derived from the analysis of the equivalent circuit of Fig. 2. In particular

$$V_{\rm GS1}(\omega) = H(\omega) V_{\rm CM}(\omega) + \frac{V_D(\omega)}{2} \tag{13}$$

$$V_{\rm GS2}(\omega) = H(\omega) V_{\rm CM}(\omega) - \frac{V_D(\omega)}{2} \tag{14}$$

where

$$H(\omega) = \frac{j\omega C_T}{2g_m + j\omega(C_T + 2C_{\rm gs})}. \tag{15}$$

In (15), g_m is the transconductance of the transistors M1 and M2, which can be written as

$$g_m = 2\beta(\overline{v}_{\rm GS1} - V_{\rm TH}) \tag{16}$$

while C_T is the parasitic capacitance between the node A and the ground (see Fig. 2), and $C_{\rm gs}$ is the gate-source capacitance of the transistors M1 and M2.

The substitution of (11) and (13)–(15) in (10) and some algebraic passages gives

$$I_0 - \frac{g_m^2}{2\beta} = 2\beta \int_{-\infty}^{+\infty} \left[\frac{\omega^2 C_T^2}{4g_m^2 + \omega^2 (C_T + 2C_{\rm gs})^2} |V_{\rm CM}|^2 + \frac{|V_D|^2}{4} \right] d\omega \tag{17}$$

that has to be solved in the unknown g_m, the transistors' transconductance.

Furthermore, the substitution of (11), (13), and (14) in (9) gives

$$\overline{i}_d = \beta \int_{-\infty}^{+\infty} \Re\{H(\omega) V_{\rm CM}(\omega) V_D(\omega)\}\, d\omega \tag{18}$$

which can be further simplified if cyclical input signals are considered. In fact, the Fourier transform of the common- and

differential-mode input signals can be written as

$$V_{\rm CM}(\omega) = \sum_{q=-\infty}^{\infty} \mu_{\rm cm}\delta(f - qf_0) \tag{19}$$

$$V_D(\omega) = \sum_{p=-\infty}^{\infty} \mu_d\delta(f - pf_0) \tag{20}$$

where $\mu_{\rm cm}$ and μ_d are the coefficients of the Fourier series expansion of $v_{\rm CM}(t)$ and $v_D(t)$, respectively, and $f_0 = 1/T$ is the fundamental frequency. The substitution of (19) and (20) in (17) and (18) gives

$$I_0 - \frac{g_m^2}{2\beta} = 2\beta \sum_{n=-\infty}^{+\infty} \left[\frac{\left(\frac{2n\pi}{T}\right)^2 C_T^2}{4g_m^2 + \left(\frac{2n\pi}{T}\right)^2 (C_T + 2C_{\rm gs})^2} |\mu_{\rm cm}|^2 + \frac{|\mu_d|^2}{4} \right] \tag{21}$$

$$\bar{i}_d = \beta \sum_{n=-\infty}^{+\infty} \Re\left[H\left(\frac{2n\pi}{T}\right) \mu_{\rm cm}\mu_d \right]. \tag{22}$$

Finally, the input offset voltage of a feedback opamp, whose input nominal signals are corrupted by EMI, can be expressed as

$$v_{\rm off} = \frac{\bar{i}_d}{g_m} \tag{23}$$

that requires the evaluation of (17) and (18).

In Sections II-A1 and II-A2, this new model is employed to predict the susceptibility of MOS differential pair to sinusoidal and trapezoidal interfering signals of constant amplitude and frequency.

1) Differential Stage Susceptibility to Sinusoidal Interference: In the presence of sinusoidal interference added to the input nominal signals of an MOS differential pair, (17) takes the form

$$I_0 - \frac{g_m^2}{2\beta} = 2\beta \left[\frac{\omega_0^2 C_T^2}{4g_m^2 + \omega_0^2 (C_T + 2C_{\rm gs})^2} V_{\rm cm,pk}^2 + \frac{V_{\rm d,pk}^2}{4} \right] \tag{24}$$

where $\omega_0 = 2\pi f_0$, f_0 is the interference frequency, while $V_{\rm cm,pk}$ and $V_{\rm d,pk}$ are, respectively, the peak value of the common- and the differential-mode interference.

From (24), with some algebraic passages follows

$$g_m^2 = -\frac{b}{2} + \frac{1}{2}\sqrt{b^2 - 4c} \tag{25}$$

in which

$$b = \frac{(C_T + 2C_{\rm gs})^2}{4}\omega_0^2 - 2I_0\beta + \beta^2 V_{\rm d,pk}^2 \tag{26}$$

$$c = \beta^2\omega_0^2 \left(C_T^2 V_{\rm cm,pk}^2 - (C_T + 2C_{\rm gs})^2 \left(\frac{I_0}{2\beta} - \frac{V_{\rm d,pk}^2}{4} \right) \right). \tag{27}$$

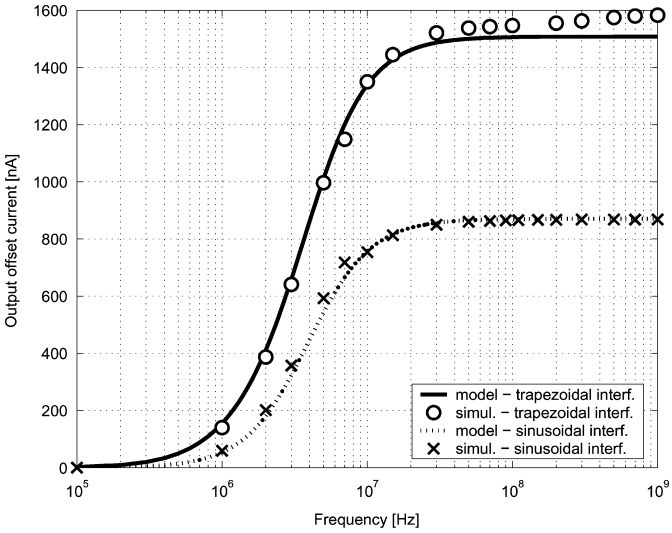

Fig. 3. Output offset current of a pMOS differential pair versus frequency. Continuous (dashed) line and circles (crosses) refer to trapezoidal (sinusoidal) interference, which were obtained by the new model and by computer simulations, respectively. In both cases, the peak amplitude of the differential mode is 200 mV while that of the common mode is 100 mV.

Furthermore, (18) can be written as

$$\bar{i}_d = \frac{\beta}{2} V_{\rm d,pk} V_{\rm cm,pk} |H(\omega_0)| \cos(\angle H + \theta) \tag{28}$$

and the evaluation of the RFI-induced offset becomes straightforward.

Let's now consider a differential pair made up by two pMOS transistors of a 0.8-μm CMOS technology process [7], with aspect ratio $(W/L) = 100/10$ μm, bias current $I_0 = 20$ μA, and parasitic capacitance $C_T = 2.1$ pF, is considered. It is powered by $V_{\rm DD} = 5$ V, its input nominal voltages are $V_{\rm cm-nom} = 3$ V and $V_{\rm d-nom} = 0$ V, and furthermore, its input terminals are driven simultaneously by sinusoidal differential-mode and common-mode interference whose amplitudes are $V_{\rm d,pk} = 200$ mV and $V_{\rm cm,pk} = 100$ mV, respectively. The effect of these signals on the mean value of the differential output current $(\bar{i}_d)$ is evaluated in the frequency range 100 kHz–1 GHz, and the results are plotted in Fig. 3. In this figure the continuous line refers to model predictions, while circles show the results of time-domain simulations, which were obtained by Spectre, a SPICE-like simulator. In addition, Fig. 4 shows the influence of CW interference on (g_m), the transistors' transconductance, for frequencies in the range 100 kHz–1 GHz.

2) Differential Pair Susceptibility to Trapezoidal-Shaped Interference: Most of the modern electronic equipment includes processing units and/or switching power transistors that behave as primary sources of interference. Trapezoidal waveforms describe these disturbances quite well, and for this reason, they are considered here as possible interference, which can affect the nominal operation of a MOS differential stage. In the following, differential- and common-mode disturbances having the same period T, the same risetime and falltime that also equal each others $(\tau_r = \tau_f)$, and zero mean value are

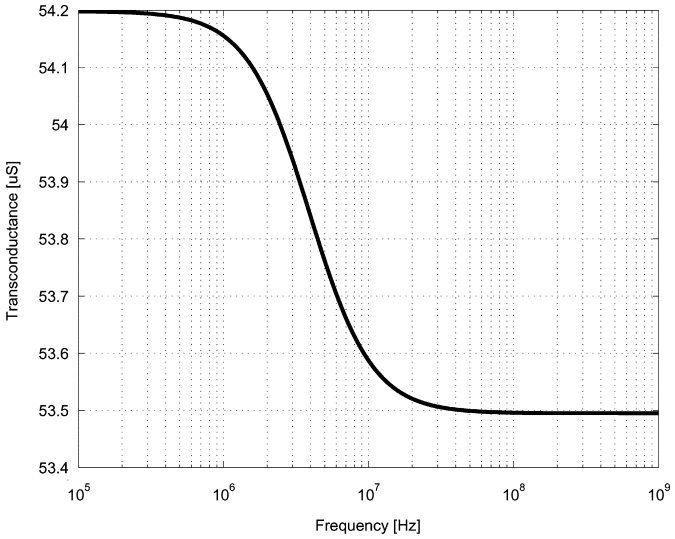

Fig. 4. Transconductance of the transistors of a pMOS differential pair versus frequency. Sinusoidal interference of constant amplitude $2V_{\mathrm{cm,pk}} = V_{\mathrm{d,pk}} = 200$ mV are considered.

considered. Nonetheless, these signals differ in amplitude and in phase.

On the basis of these assumptions, the coefficients of their Fourier series expansion can be written as

$$\mu_{\mathrm{cm-sq}} = -j\frac{A_{\mathrm{cm-sq}}}{2\pi n}\frac{\sin(\frac{n\pi\tau}{T})}{\frac{n\pi\tau}{T}}\frac{\sin\left(\frac{n\pi\tau_r}{T}\right)}{\frac{n\pi\tau_r}{T}} \times \exp\left(-j\frac{n\pi(\tau+\tau_r)}{T}\right) \tag{29}$$

$$\mu_{\mathrm{d-sq}} = -j\frac{A_{\mathrm{d-sq}}}{2\pi n}\frac{\sin(\frac{n\pi\tau}{T})}{\frac{n\pi\tau}{T}}\frac{\sin(\frac{n\pi\tau_r}{T})}{\frac{n\pi\tau_r}{T}} \times \exp\left(-j\left(\frac{n\pi(\tau+\tau_r)}{T}+\theta_{\mathrm{sq}}\right)\right) \tag{30}$$

where θ_{sq} is the phase shift between trapezoidal waveforms.

In addition, these expressions include the peak-to-peak amplitude of the common- and differential-mode voltages ($A_{\mathrm{cm-sq}}$, $A_{\mathrm{d-sq}}$), and the time between the 50% points of the waveform amplitude (τ) [8].

On the basis of these expressions, and assuming that $f_0 \gg (g_m/(2\pi(C_T+2C_{\mathrm{gs}}))$ and that infinity sums are truncated to the Nth harmonic, (21) and (22) can be easily evaluated, obtaining g_m and $\bar{i}_d$, respectively. For instance, let us now consider the same differential pair, which has been employed in Section II-A1, with the same nominal input voltages, while sinusoidal disturbances are replaced by trapezoidal ones. Such interfering signals have amplitudes $A_{\mathrm{cm-sq}} = 200$ mV and $A_{\mathrm{d-sq}} = 400$ mV (the same as the sinusoidal disturbances), fundamental frequency f_0 in the range 100 kHz–1 GHz, duty cycle of 50% ($\tau = T/2$), risetime (falltime) $\tau_r = T/10$, while the phase shift between them is null ($\theta_{\mathrm{sq}} = 0$). Therefore, running the new model with these parameters and considering ten harmonics of the interfering signals ($N = 10$), the results of Fig. 3 (dashed line) can be obtained, and the comparison with the results of time-domain simulations (crosses) becomes straightforward. To this purpose, it should be noticed that the agreement between the model predictions and the simulation results is quite good, but it is worse than that obtained with sinusoidal interference. This fact can be ascribed to the aforementioned approximations and to the frequency limitation of the model, which can be enhanced if a more accurate small signal equivalent circuit of the differential pair is employed (see Fig. 2).

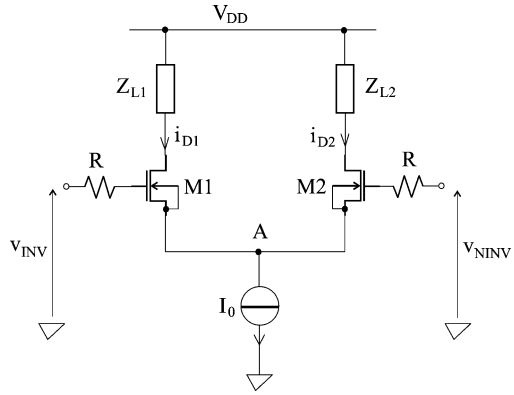

Fig. 5. nMOS differential stage including two resistors at the input terminals. Such resistors, together with the input capacitances of the differential stage, behave as input low-pass filters that improve the immunity to EMI.

In the following sections, it is shown how the new model can be employed to design an opamp input differential stage immune to EMI.

III. Double Differential Pair

Over the last few years, a few possible solutions to make opamps immune to EMI have been presented. Some of them are aimed to attenuate the amplitude of the interference reaching sensitive nonlinear devices. For instance, Fig. 5 shows a simple filtering solution, where two resistors (R) together with the input parasitic capacitances of a CMOS opamp behave as low-pass filters. Such integrated filters are critical for what concerns noise and circuit stability. Other circuits, like that shown in [9], are based on the compensation of EMI-induced upsets by means of proper circuit topologies. Such compensation networks usually require a silicon area larger than that of basic functional circuits (doubled at least), and in some cases, they affect some of the base-band circuit parameters, like the common-mode input voltage swing [10].

The following part of the paper shows a new differential stage that includes two cross-connected MOS differential pairs (see Fig. 6). In this circuit, the upset, which is induced by EMI in the primary differential stage (M1-M2), is compensated by that generated in the auxiliary differential pair (M3-M4). Unlike previous solutions, this compensation network provides high immunity to EMI, minimum silicon area, and almost no effect on the circuit base-band performance. More in detail, the total output current of the overall differential stage can be

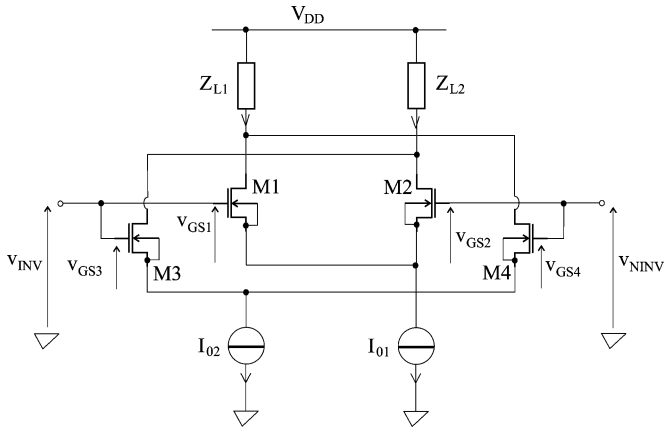

Fig. 6. Schematic view of the double differential pair.

written as

$$\bar{i}_d = \bar{i}_{d1-2} - \bar{i}_{d3-4} \tag{31}$$

that becomes

$$\bar{i}_d = \int_{-\infty}^{+\infty} \Re\{[\beta_1 H_1(\omega) - \beta_2 H_2(\omega)] V_{\rm CM}(\omega) V_D(\omega)\} d\omega \tag{32}$$

if (18) is employed. In (32)

$$\beta_i = \frac{\mu_{\rm n} C_{\rm ox}}{2} \frac{W_i}{L_i}, \qquad i = 1, 2 \tag{33}$$

$$H_i(\omega) = \frac{j\omega C_{Ti}}{2g_{mi} + j\omega(C_{Ti} + 2C_{{\rm gs}i})}, \qquad i = 1, 2. \tag{34}$$

Looking at (32) it can be easily noticed that the output offset current becomes null ($\bar{i}_d = 0$) if

$$\beta_1 H_1(\omega) = \beta_2 H_2(\omega). \tag{35}$$

Equation (35) is always verified if two identical differential pairs are considered, but this case is not of practical interest because the total output current is always null, even when nominal input signals are provided. For this reason, (35) has to be satisfied under the constraint $g_{\rm m1} \neq g_{\rm m2}$.

Furthermore, from (35), it follows

$$\frac{\beta_1 C_{T1}}{C_{T1} + 2C_{\rm gs1}} = \frac{\beta_2 C_{T2}}{C_{T2} + 2C_{\rm gs2}} \tag{36}$$

$$\frac{g_{\rm m1}}{C_{T1} + 2C_{\rm gs1}} = \frac{g_{\rm m2}}{C_{T2} + 2C_{\rm gs2}} \tag{37}$$

and

$$\beta_1 \left[\left(\frac{C_{T1}}{C_{T2}} \right)^2 \left(\overline{v_{\rm gs3}^2} + \overline{v_{\rm gs4}^2} \right) - \left(\overline{v_{\rm gs1}^2} + \overline{v_{\rm gs2}^2} \right) \right] = I_{01} - \frac{\beta_1}{\beta_2} \left(\frac{C_{T1}}{C_{T2}} \right)^2 I_{02} \tag{38}$$

in which $\overline{v_{{\rm gs}i}^2}$ is the mean-square value of the ith gate-source voltage, while I_{01} and I_{02} are, respectively, the bias currents of the differential pairs M1-M2 and M3-M4.

The left hand of (38) depends on the mean-square value of the gate-source voltages; hence, on the PSD of the common- and the differential-mode voltages, while the right hand includes constant design parameters. As a consequence, (38) must be solved referring to the worst case, i.e., the maximum amplitude of interference that could reach the differential pair input ports. As a result

$$2 \left[|H_2(\omega)|^2 \left(\frac{C_{T1}}{C_{T2}} \right)^2 - |H_1(\omega)|^2 \right] V_{\rm cm,pk}^2 + \left[\left(\frac{C_{T1}}{C_{T2}} \right)^2 - 1 \right] \frac{V_{\rm d,pk}^2}{2} = \frac{I_{01}}{\beta_1} - \left(\frac{C_{T1}}{C_{T2}} \right)^2 \frac{I_{02}}{\beta_2} \tag{39}$$

which becomes

$$2 \left[\frac{C_{T1}^2}{(C_{T2} + 2C_{\rm gs2})^2} - \frac{C_{T1}^2}{(C_{T1} + 2C_{\rm gs1})^2} \right] V_{\rm cm,pk}^2 + \left[\left(\frac{C_{T1}}{C_{T2}} \right)^2 - 1 \right] \frac{V_{\rm d,pk}^2}{2} = \frac{I_{01}}{\beta_1} - \left(\frac{C_{T1}}{C_{T2}} \right)^2 \frac{I_{02}}{\beta_2} \tag{40}$$

under the assumption $\omega \gg \max(g_{\rm m1}/(C_{T1} + 2C_{\rm gs1}), (g_{\rm m2}/(C_{T2} + 2C_{\rm gs2}))$.

The design of the double differential pair is now performed in order to fulfill both base-band and EMI specifications. In particular, the primary differential pair (M1-M2) is sized on the basis of base-band specifications, while the design of the auxiliary transistor pair (M3-M4) is performed through (36) and (40). As a consequence, the ratio C_{T2}/C_{T1} can be written as

$$\left(\frac{C_{T2}}{C_{T1}} \right)^2 = \frac{\frac{I_{02}}{\beta_2} + \frac{V_{\rm d,pk}^2}{2} + \left(\frac{1}{1 + 2\frac{C_{\rm gs2}}{C_{T2}}} \right)^2 V_{\rm cm,pk}^2}{\frac{I_{01}}{\beta_1} + \frac{V_{\rm d,pk}^2}{2} + \left(\frac{1}{1 + 2\frac{C_{\rm gs1}}{C_{T1}}} \right)^2 V_{\rm cm,pk}^2} \tag{41}$$

which is kept at the minimum, if $C_{\rm gs2}/C_{T2}$ is negligible. Under this assumption, (36) is simplified and β_2 takes the form

$$\beta_2 = \beta_1 \frac{C_{T1}}{C_{T1} + 2C_{\rm gs1}} \tag{42}$$

while C_{T2} is evaluated by (41). In (42), the maximum values of $V_{\rm cm,pk}$ and $V_{\rm d,pk}$ have to be considered and the maximum EMI-induced output offset current, which is induced by RFI in the differential pair M1-M2, is evaluated by (28). To avoid any upset compensation failure, the offset current in the primary differential pair should always be lower than the maximum M3-M4 output offset current, i.e., I_{02}. In Section III, the design of a double differential pair is shown, and its EMI performance is compared with that of other circuit topologies.

IV. Design Procedure and Simulation Results

This section describes a method to design a double differential pair immune to EMI. In particular, the same differential pair, which has been described in Section II-A1, is considered. It includes two pMOS transistors with aspect ratio $(W/L)_{1,2} = 100/10$ μm biased by the dc current source $I_{01} = 20$ μA, while its parasitic capacitance $C_{T1} = 2.1$ pF has been obtained from

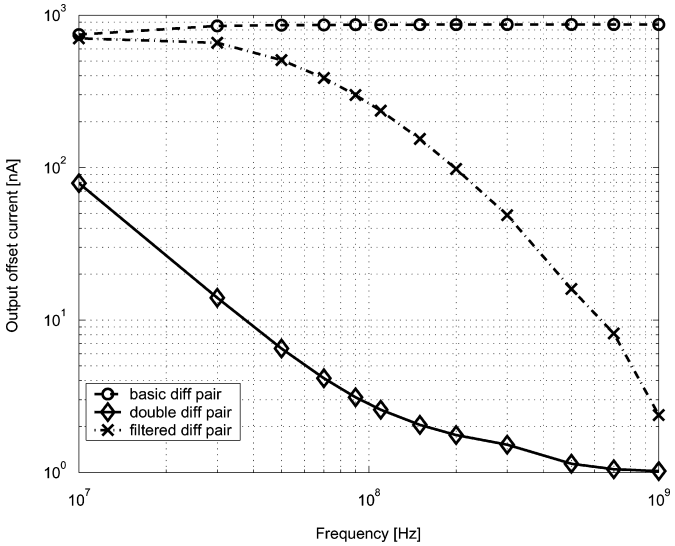

Fig. 7. Output offset current of the double differential pair (diamonds over continuous line), basic differential pair (circles over dashed line), and filtered differential pair (crosses over dashed-dotted lines) versus interference frequency. Sinusoidal interference of constant amplitude $2V_{\mathrm{cm,pk}} = V_{\mathrm{d,pk}} = 200\,\mathrm{mV}$ are considered.

the analysis of its layout view. On the basis of these data and considering the case of sinusoidal interference of maximum amplitude $2V_{\mathrm{cm,pk}} = V_{\mathrm{d,pk}} = 200$ mV, the maximum output offset current of M1-M2 is $\bar{i}_{d1} = 0.9$ μA. Therefore, with a bias current $I_{02} = 3$ μA, the aspect ratio of the transistor M3-M4 that minimize the total output offset current can be evaluated by (42); hence, $(W/L)_{3,4} = 5.5$. Furthermore, assuming $L_{3,4} = 1$ μm, and solving (41), it follows that $C_{T2} = 1.24$ pF.

These design parameters were employed to perform time-domain computer simulations with sinusoidal interference having amplitude of $2V_{\mathrm{cm,pk}} = V_{\mathrm{d,pk}} = 200$ mV and frequency in the range 10 MHz–1 GHz. The results of these simulations are shown in Fig. 7 by diamonds over continuous line. In the same figure circles over dashed line show the output offset current of the basic differential pair M1-M2, while crosses over the dashed-dotted line refers to the circuit in Fig. 5, in which the low-pass filters have cutoff frequency of $f_p = 60$ MHz. Concerning this last circuit, an opamp with gain-bandwidth product of GBW $= 6$ MHz and phase margin of PM $= 70^\circ$ has been considered, and the cutoff frequency f_p has been selected in order to improve the opamp immunity and to fulfill the opamp stability constraints as well. Further reduction of this cutoff frequency under 60 MHz can be accomplished only with a proper design of the opamp compensation network. These results point out that the double differential stage is more immune to RFI than conventional differential pairs, and the output offset current decreases with frequency. This fact can be ascribed to the RFI distortion in the pair M3-M4, which becomes completely effective at higher frequencies, compensating that induced by RFI in the main differential pair (M1-M2).

V. Conclusion

In this paper, the effect of electromagnetic interference on the operation of MOS differential stages has been evaluated. To this purpose, general interfering signals, which have been expressed in terms of power spectral density, have been elaborated by a new analytical model to predict EMI-induced upsets. Furthermore, some examples that highlight the benefits deriving from this new model have been shown, and in the last two sections of the paper, this model has been successfully employed in the design of a new differential stage that shows high immunity to EMI. Finally, the performance of this new circuit has been compared with those of other circuit topologies.

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