Boost bridge amplifier

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A novel boost bridge amplifier which inherently doubles the power supply voltage, thus providing up to four times higher peak output power than a comparable state-of-the-art class-D amplifier, is proposed. The efficiency and the total harmonic distortion of both amplifiers during the amplification of a music signal are shown to be similar.

Introduction: The amount of heat generated and power consumed are inherent drawbacks of all class-A, B and AB linear amplifiers due to the linear mode of operation of the power transistors. A class-D switching amplifier (CDA) [1, 2] overcomes these problems by forcing power transistors into the on or off state. Several alternative switching topologies cover the push-pull switching amplifier [3], boost DC-AC converter [4] and opposed current power converter [5].

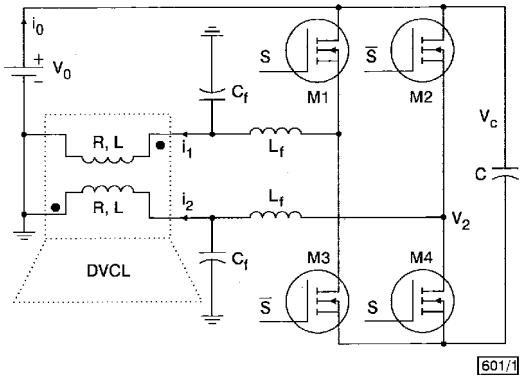

Fig. 1 *Power stage of BBA*

Boost bridge amplifier topology: On the top level of an amplifier's topology, all known audio amplifiers look similar, i.e. a power supply is connected to a bridge capacitor and power transistors, which drive a loudspeaker. In a novel boost bridge amplifier (BBA) topology, the power supply is connected to a centre tap of a dual-voice coil loudspeaker (DVCL), which is driven by the power transistors supplied from the bridge capacitor (Fig. 1). The operation of a switching bridge in the CDA and the BBA is identical. The two pulsewidth-modulated control signals S and $\bar{S}$ force the power transistors M1 and M4 into the on state while M2 and M3 are in the off state, and *vice versa*. Two phase currents i_1 and i_2 depend on DC and AC terms based on the modulation signal shape $f(t)$:

$$i_{1,2} = \frac{I_0 \pm I_m \cdot f(t)}{2} \tag{1}$$

The resultant force, providing a desired voice coil movement, is proportional to the difference i_f (eqn. 2) between the phase currents according to the phase reference markers of the DVCL. The power supply current i_0 (eqn. 3) is appropriate to the sum of the phase currents, which produce mutually cancelled forces at the voice coil according to the phase reference markers of the DVCL:

$$i_f = i_1 - i_2 = I_m \cdot f(t) \tag{2}$$

$$i_0 = i_1 + i_2 = I_0 \tag{3}$$

The power balance in eqn. 4 shows that the switching bridge efficiency η reduces the power generated by the power supply, which can be delivered to the DVCL as a DC and an AC RMS (root-mean-square) power P_{AC} dependent on an RMS factor k (eqn. 5):

$$\eta V_0 I_0 = \frac{RI_0^2}{2} + k \cdot \frac{RI_m^2}{2} \tag{4}$$

$$k = \frac{1}{T}\int_0^T f^2(t)\,dt \tag{5}$$

The bridge capacitor voltage (eqn. 6) is derived from the voltage loop covering the power supply, the DVCL and the switching bridge midpoint between the power transistors. The overall system efficiency η_0 (eqn. 7) is proportional to the bridge capacitor voltage:

$$\frac{V_C}{V_0} = 1 + \sqrt{1 - k \cdot \left(\frac{RI_m}{\eta V_0}\right)^2} \tag{6}$$

$$\eta_0 = \left(k \cdot \frac{RI_m^2}{2}\right) \Big/ (V_0 I_0) = \frac{\eta V_C}{2V_0} \tag{7}$$

The modulation index m (eqn. 8) provides a final theoretical equation (eqn. 9):

$$I_m = m \cdot \frac{\eta V_C}{R} \tag{8}$$

$$\frac{V_C}{V_0} = \frac{2}{1 + k \cdot m^2} \tag{9}$$

During music signal reproduction, high AC peak power P_{PK} is required during relatively short bursts. Amplifiers designed for high AC RMS power are expensive and bulky due to the high-rated power transistors, large mains transformer, bridge capacitors and heatsinks. It makes better engineering and economical sense to design an amplifier with the music Crest factor (eqn. 10) in mind [6], which is exactly the case in the BBA design.

$$CF = \frac{P_{PK}}{P_{AC}} = \frac{1}{k} \geq 10 \tag{10}$$

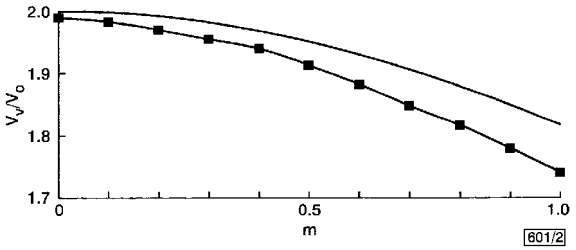

Fig. 2 *Theoretical and experimental bridge capacitor voltage for CF = 10*

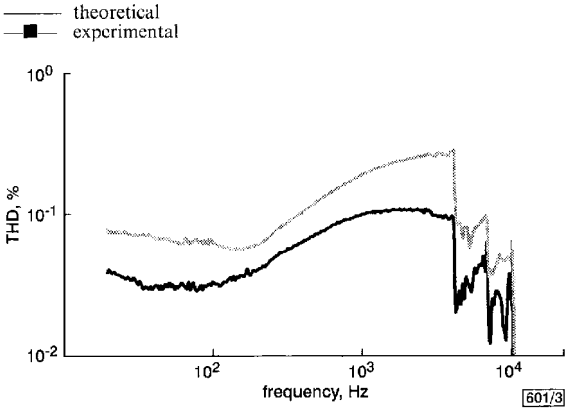

Fig. 3 *Measured THD for AC RMS power of 0.5 and 4 W*

0.5W
4W

Results: To test the proposed concept, a novel 5V BBA was designed, incorporating a triangle oscillator, an ultrafast comparator LT1016, TC4426/4427 MOSFET drivers, Si9936 dual N-channel and NDS8947 dual P-channel MOSFETs, 220μF bridge capacitor, two L_f = 15μH filtering inductors and two sets of filtering capacitors equivalent to C_f = 1.9μF each. Two 2Ω resistors emulated the loudspeaker during the voltage, current and THD measurements. A GF200 DVCL confirmed the mutual cancellation of the DC current's forces and associated absence of the position offset of the voice coil. The cut-off frequency of 30kHz determined by the output LC filter dictated a 100Hz period of pulse wave modulation with CF = 10 during the tests. The experimental results for the bridge capacitor voltage (Fig. 2), as well as the DC and AC currents (not shown) confirm the theoretical pre-

dictions reasonably well, especially considering that the ripple current and the switching loss were omitted from the analysis.

The total harmonic distortion (THD) was measured using a MultiSound Fiji sound card installed in a PC running Liberty Audiosuite Ver.3.01 software. An inherent 'brick-wall' software filtering at 20kHz eliminated all ultrasonic harmonics from the THD diagram (Fig. 3), measured for 0.5W and 4W AC RMS power using a sine wave modulation signal sweeping between 20Hz and 20kHz. The equivalent THD diagram (not shown) for the same amplifier in the CDA topology with twice as high a power supply voltage is almost identical.

Conclusions: We have proposed a BBA that, compared with a CDA supplied from the same power supply, provides more than three times as much AC peak power for a modulation signal with $CF = 10$ and almost four times as much AC peak power for a modulation signal with $CF = 100$ with negligible loss in efficiency and comparable THD. Since the BBA has been specifically designed for high AC peak power rather than AC RMS power, it provides the least cost per watt of all switching amplifiers.

19 March 2001
Electronics Letters Online No: 20010449
DOI: 10.1049/el:20010449

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Simple digitally programmable attenuator using FG-MOSFETs

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A very simple digitally programmable attenuator using FG-MOSFETs (floating-gate MOSFETs) is presented. HSPICE simulations of the circuit demonstrate a THD of less than –32dB and a variable gain range of –13 to –31dB with a supply voltage of ±1.5V, load resistance of 10kW and input signal of $3V_{p\text{-}p}$.

Introduction: Attenuators are important circuit components and are used in the multipliers, transmitters, etc. [1, 2]. In this Letter, a very simple attenuator is proposed. It is based on the conventional Class B CMOS output stage shown in Fig. 1. Power is supplied via M_n and M_p rather than via the one MOSFET, and each MOSFET conducts for alternate half cycles. The load resistance R_L is connected to the sources of M_n and M_p, making the devices act as source followers [3]. The circuit has the advantage of high efficiency. V_{out} of the circuit is given by [3]

$$V_{out} = \begin{cases} V_{in} + |V_{Tp}| & V_{SS} - |V_{Tp}| + V_{dsp(sat)} < V_{in} \le -|V_{Tp}| \\ 0 & -|V_{Tp}| < V_{in} \le V_{Tn} \\ V_{in} - V_{Tn} & V_{Tn} < V_{in} \le V_{DD} + V_{Tn} - V_{dsn(sat)} \end{cases} \quad (1)$$

where V_{Tn} and V_{Tp} are the threshold voltages of the *n*MOSFET and *p*MOSFET, respectively, and $V_{dsn(sat)}$ and $V_{dsp(sat)}$ are the minimum drain-to-source voltages maintaining the saturation region of the *n*MOSFET and *p*MOSFET, respectively. As shown in eqn. 1, the circuit has a deadband, which is approximately equal to $V_{Tn} + |V_{Tp}|$. This gives rise to crossover distortion. In this Letter, this problem is resolved by using FG-MOSFETs, which are then applied to the programmable attenuator.

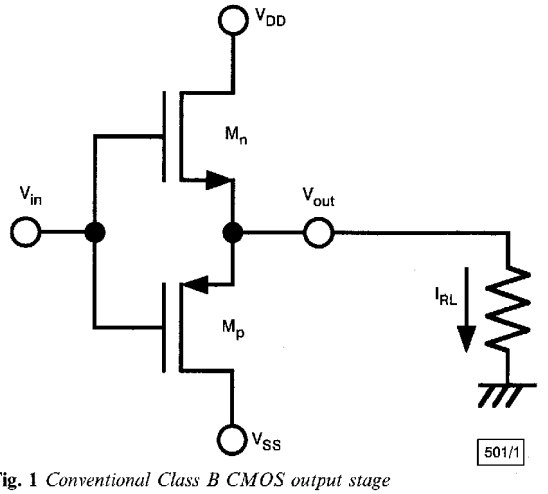

Fig. 1 *Conventional Class B CMOS output stage*

FG-MOSFET: The floating-gate voltage of the FG-MOSFETs (V_f) is given by [4]

$$V_f = \sum_{i=1}^{k} \frac{C_i}{C_0 + \sum_{j=1}^{k} C_j} V_i = \sum_{i=1}^{k} w_i V_i \quad (2)$$

where C_i is the capacitance between the floating gate and *i*th input gate and is defined as C_1, C_2, ..., C_k, in order from the source side, C_0 is the oxide capacitance between the floating gate and the substrate and w_i is referred to as a capacitive weight. Since the basic physical structure of the FG-MOSFET below the floating gate is the same as that of a MOSFET, the floating-gate voltage of the FG-MOSFET corresponds to the gate voltage of the MOSFET [4]. Therefore, using eqn. 2, $V_{fs} - V_{Tn}$ can be given by

$$V_{fs} - V_{Tn} = \sum_{i=1}^{k} w_i V_i - V_s - V_{Tn} = \sum_{i=1}^{k-1} w_i V_i - V_s - V_{Tn}^{*} \quad (3)$$

where V_{fs} is the floating-gate-to-source voltage, V_s is the source voltage and $V_{Tn}^{*} = V_{Tn} - w_k V_k$ is the appearance threshold voltage. From eqn. 3, V_{Tn}^{*} can be varied by w_k and V_k. This is referred to as the variable threshold function. In addition, the input signals $V_1 \sim V_{k-1}$ are weighted by $w_1 \sim w_{k-1}$ and are summed. This is known as the weighted sum operation function.

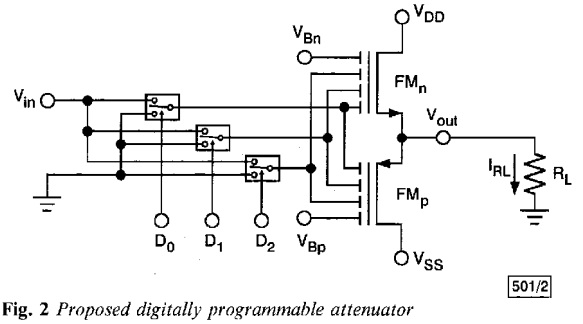

Fig. 2 *Proposed digitally programmable attenuator*

Circuit operation: Fig. 2 shows the proposed attenuator. FM_n and FM_p are the *n*-channel and *p*-channel FG-MOSFETs, respectively. The two-state switches shown in Fig. 2 are simply realised by two CMOS switches. In the circuit, w_i ($i = 1, ..., 4$) of FM_n and FM_p are defined by w_{in} and w_{ip}, respectively. In the proposed circuit, w_{4n} and w_{4p} are used as the V_{Tn} and V_{Tp} cancellation by using the