24.5 60GHz Transceiver Circuits in SiGe Bipolar Technology

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The increasing capabilities of silicon technologies make highly-integrated radio circuits possible at millimeter-wave frequencies. This reduces the cost and power consumption of millimeter-wave radios which are implemented today as an assembly of GaAs or InP chips [1]. One promising application is a 60GHz wireless personal-area network (WPAN) operating at data rates >150Mb/s [2].

This paper describes key front-end 60GHz SiGe transceiver circuits including an LNA, a direct downconverter, a PA and a VCO, as shown in Fig. 24.5.1. Each circuit is currently implemented separately as the first step towards realizing a fully-integrated 60GHz silicon transceiver. The downconverter block contains 80 transistors and 43 inductors or transmission lines, which is a very high level of integration at this frequency. The 0.12μm SiGe technology features NPNs with f_T and f_{MAX} both ≥200GHz [3], metal-film resistors, MIM capacitors, and two thick top Al layers.

The two-stage single-ended LNA is shown in Fig. 24.5.2. A common-base amplifier is used for the first stage, and the second stage is a degenerated cascode. Each stage provides ~8dB of gain at 3mA. By changing the second-stage bias current, adjustable gain is obtained while the noise figure remains relatively constant. Since a quarter-wavelength in SiO_2 is ~600μm at 60GHz, shunt-stub microstrip transmission line networks are used for the input, inter-stage, and output match. Numerous substrate contacts reduce substrate coupling. Two versions of the LNA are implemented; one uses a 50Ω coplanar waveguide (CPW) tapers at the input and output (to absorb pad parasitics), and the other uses normal pads at the input and output. In comparing the results, the CPW insertion loss is de-embedded from gain, noise, and linearity measurements.

Figure 24.5.3 shows the wafer-probed S-parameters and 50Ω NF of the taper-LNA operating at 6mA and V_{CC}=1.8V. At 61.5GHz, the gain is 17dB and S_{12} is -40dB, while input and output return losses are 14 and 12dB, respectively. In comparison, the pad-LNA shows 14.7dB gain, -6dB S_{11}, and -17dB S_{22}, at 6mA. Both LNAs are unconditionally stable over 30-65GHz, and have input P_{1dB}s and IIP3s of -20 and -8.5dBm, respectively. At 60 and 63GHz, where our noise source's excess noise ratio is calibrated, the NF is 3.3 and 4.2dB, respectively for the taper-LNA and 3.4 and 4.4dB for the pad-LNA. Mean NF across the band are 3.5 and 3.7dB, respectively. For reference, III-V LNAs have achieved 2-4dB NF at this frequency range.

The downconverter architecture is shown in Fig. 24.5.1. LNA2 has 12dB of gain and serves as an active balun, providing a differential RF signal to the two double-balanced Gilbert-cell mixers, which have 4dB of gain. The mixers are driven with quadrature LO signals from a differential branch-line directional coupler. A pilot signal comes on-chip at a third of the desired LO frequency, and a frequency tripler generates the final LO signal.

LNA2 consists of a cascoded differential pair with inductive load and degeneration. The four inductors are realized with AC short-circuited microstrip transmission lines. The input match is completed with a series inductor formed with top-metal over a substrate with oxide-filled trenches. LNA2 draws 8mA from 2.7V. The mixers are resistively-degenerated double-balanced Gilbert cells. Each mixer and associated LO buffer (shown in Fig. 24.5.1) together draw 12mA. The mixer load resistors are 300Ω, so unity-gain buffers are included to provide 100Ω differential baseband signals to drive off-chip. The baseband 3dB bandwidth is 1.5GHz. The buffers, which draw 26mA each, are for test only, since an analog baseband is planned to be integrated with the downconverter.

The frequency tripler block in Fig. 24.5.4 consists of two stages: the actual tripler, and an LO amplifier following the tripler and preceding the branch-line coupler. A 0dBm, 20GHz differential LO pilot signal is applied to the tripler (a cascoded differential amplifier with a tuned load), which produces third-harmonic distortion. The LO amplifier also has a tuned load to further amplify the third harmonic and reject the fundamental; it supplies 2dBm (simulated) with the fundamental >25dB down. The tripler alone draws 4 mA and LO amplifier 16mA. Finally, a stand-alone 21.2-22.4 GHz Colpitts VCO is implemented, showing a measured phase noise between -109 to -116dBc/Hz for 1MHz offset. The VCO draws 9mA from 3V.

Downconverter gain and NF are shown in Fig. 24.5.5. At 60GHz, gain is 18.6dB and NF is 13.3dB, while simulated gain is 17.1dB and NF is 14.9dB. Some samples show a dip in conversion gain at 64GHz, which may be due to interaction between the LO amplifier and branch-line coupler. LO leakage measured at LNA2's input varies with frequency and reaches -50dBm maximum at 60GHz. Mixer offset voltages are another measure of LO-RF isolation. Measured I and Q offsets on 8 chips have an average offset-voltage magnitude of 56mV, including 2 chips with offsets >200mV. The remaining 6 chips have an average offset of 21mV. These offsets indicate that direct conversion is practical for a 60GHz WPAN, given 650mVp-p mixer output swing and AC coupling.

The PA is a two-stage class-AB balanced amplifier, used to directly feed a differential antenna. The balanced amplifier is implemented by placing two unbalanced amplifiers in parallel. The unbalanced amplifier consists of two cascaded common-emitter amplifiers, with input, inter-stage, and output matching networks. Quarter-wavelength RF chokes supply V_{CC} to each stage. Temperature-compensated biasing is used to provide constant output power and gain. At 61.5GHz, the PA delivers 10dBm output power with 9dB of gain. The saturated output power level is >11.8dBm—limited by our measurement equipment. The PA draws 130mA from 1.1V. Wide bandwidth is observed, with return losses better than 10dB from 55 to >65GHz. Across 5-75°C, the measured gain and P_{1dB} vary by ±1dB and ±1.2dBm, respectively.

Figure 24.5.6 summarizes LNA, downconverter, and PA performance, while Fig. 24.5.7 shows die photos of the LNA, PA, and downconverter (the branch-line coupler, folded to reduce its size, is in the center). Based on these results, a fully-integrated transceiver with 5-6dB NF and +10dBm output power should be possible.

Acknowledgments:
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References:
[1] K. Ohata et al, "Wireless 1.25Gb/s Transceiver Module at 60GHz Band," *ISSCC Dig. Tech. Papers*, pp. 298-299, Feb. 2002.
[2] P. Smulders, "Exploiting the 60GHz Band for Local Wireless Multimedia Access: Prospects and Future Directions," *IEEE Communications Magazine*, pp. 140-147, Jan. 2002.
[3] B. Jagannathan et al, "Self-Aligned SiGe NPN Transistors with 285GHz fMAX and 207GHz fT in a Manufacturable Technology," *IEEE Electron Device Lett*, vol. 23, no. 5, 2002.

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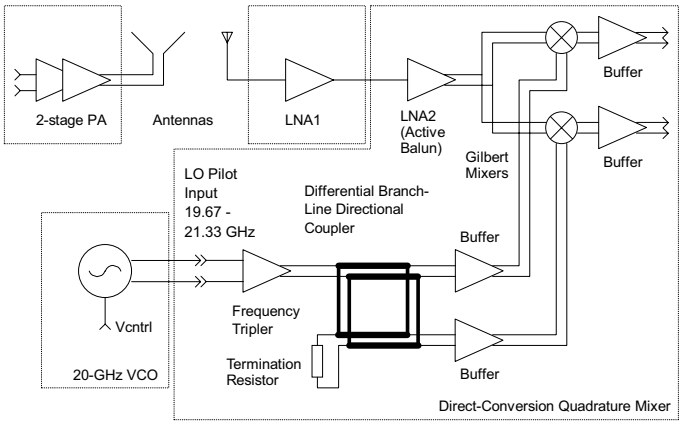

Figure 24.5.1: Block diagram of four 60GHz transceiver components. LNA, PA, VCO, and direct downconverter. Dashed boxes show boundaries of each chip.

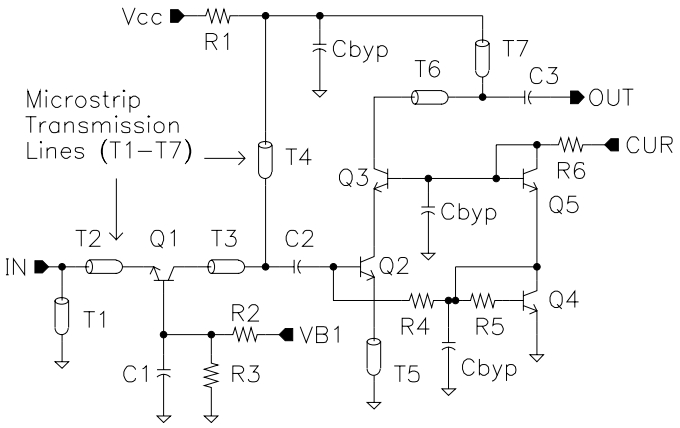

Figure 24.5.2: Schematic of 60GHz low-noise amplifier.

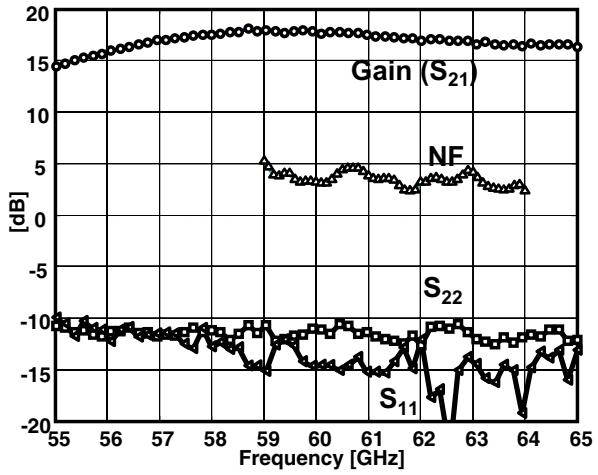

Figure 24.5.3: Measured gain, noise figure, S11, and S22 for LNA with CPW tapers.

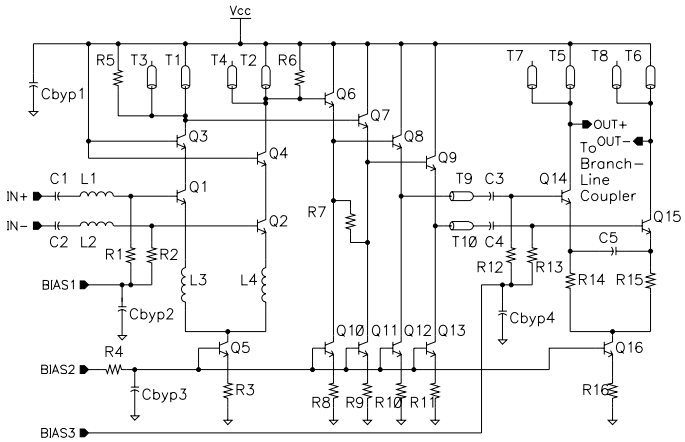

Figure 24.5.4: Simplified schematic of the frequency tripler block, consisting of the actual tripler and an LO amplifier.

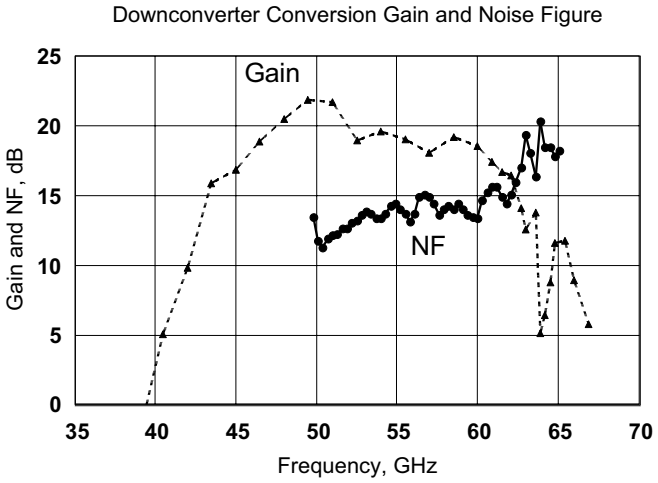

Figure 24.5.5: Measured conversion gain and NF for direct downconverter.

	LNA	PA	Downconverter
Freq.	61.5 GHz	61.5 GHz	61.5 GHz
Gain	17 dB	10.7 dB	16 dB
NF	4.2 dB	-	14.8 dB
P1dB	-20 dBm (in)	+8.7 dBm (out)	-17 dBm (in)
IIP3	-8.5 dBm	+1.4 dBm	-7 dBm
IIP2	-	-	+13 dBm
Psat	-	> +11.8 dBm	-
LO leakage to LNA2 input	-	-	< -50 dBm
S11	-14 dB	-14.5 dB	-12 dB
S22	-12 dB	-24 dB	-
S12	-40 dB	-40 dB	-
Supply Current	6 mA @ 1.8V	130 mA @ 1.1V	112 mA @ 2.7V (entire chip) 55 mA @ 2.7V (w/o output buffers)

Figure 24.5.6: Measured performance summary for LNA, PA, and downconverter.

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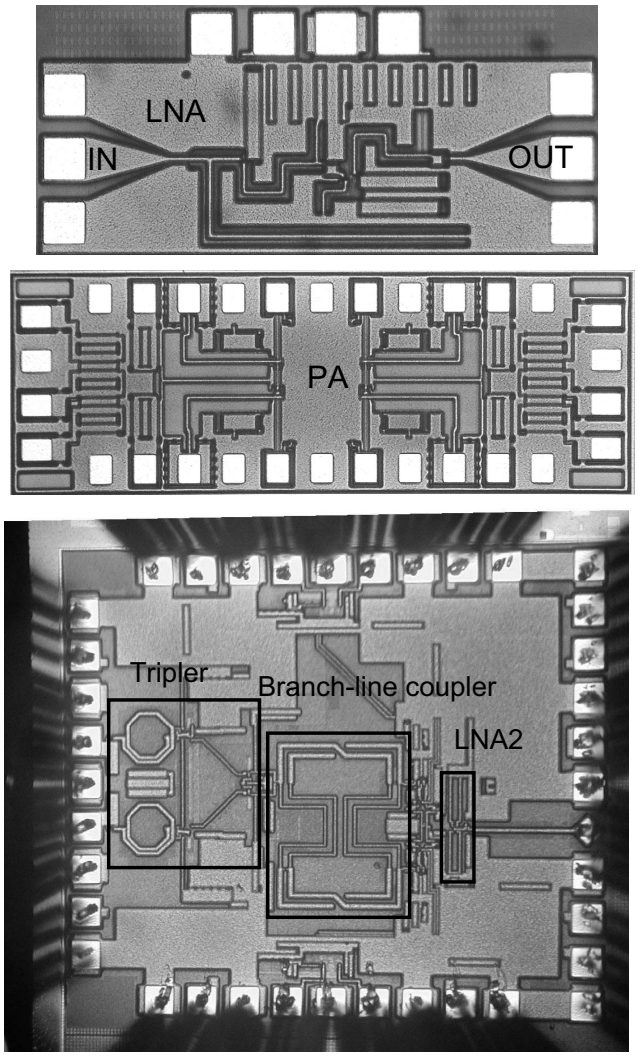
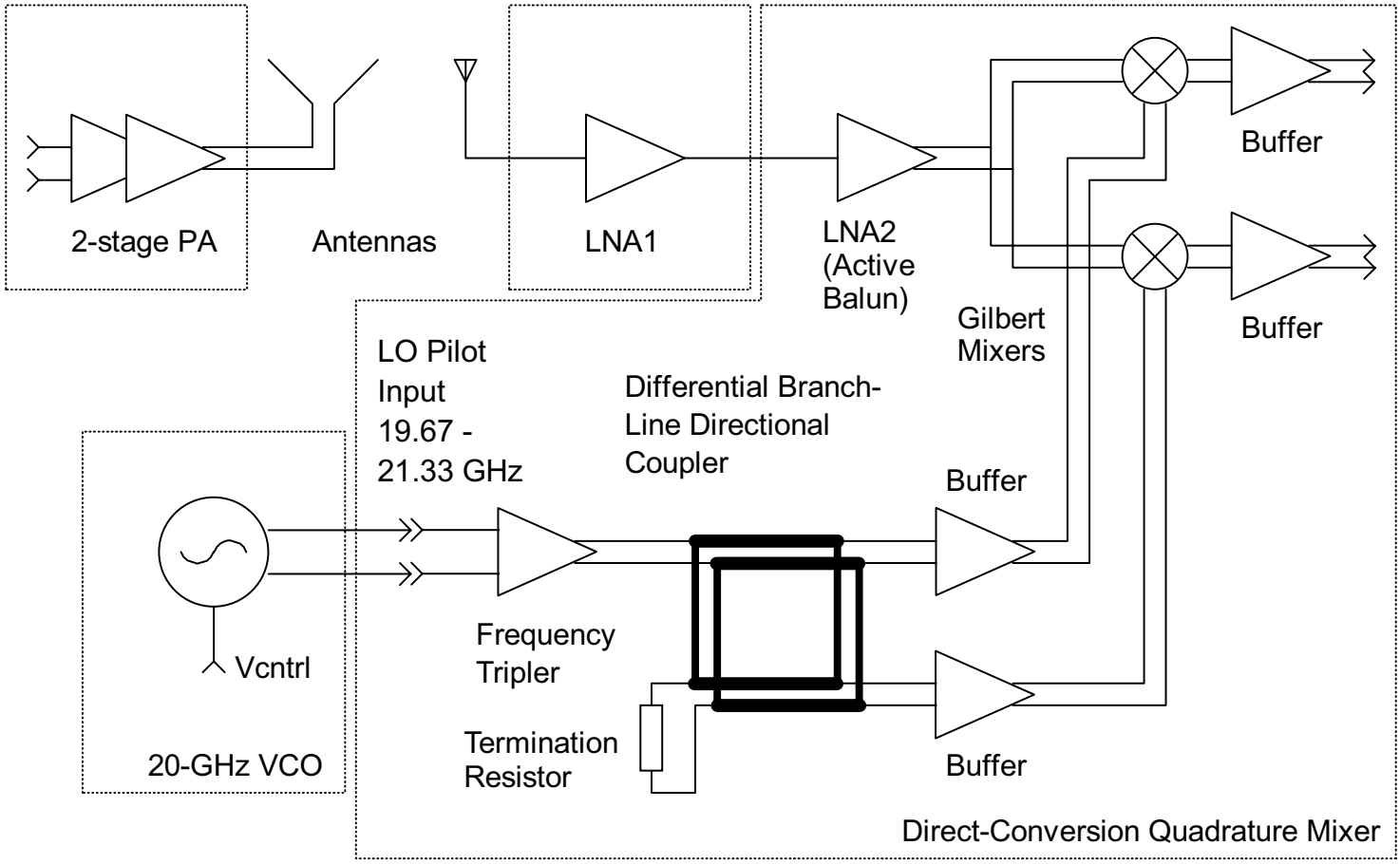


Figure 24.5.7: Die photographs of LNA (top, 1.3mm x 0.6mm), PA (center, 2.1mm x 0.75mm), and downconverter (bottom, 1.9mm x 1.65mm).



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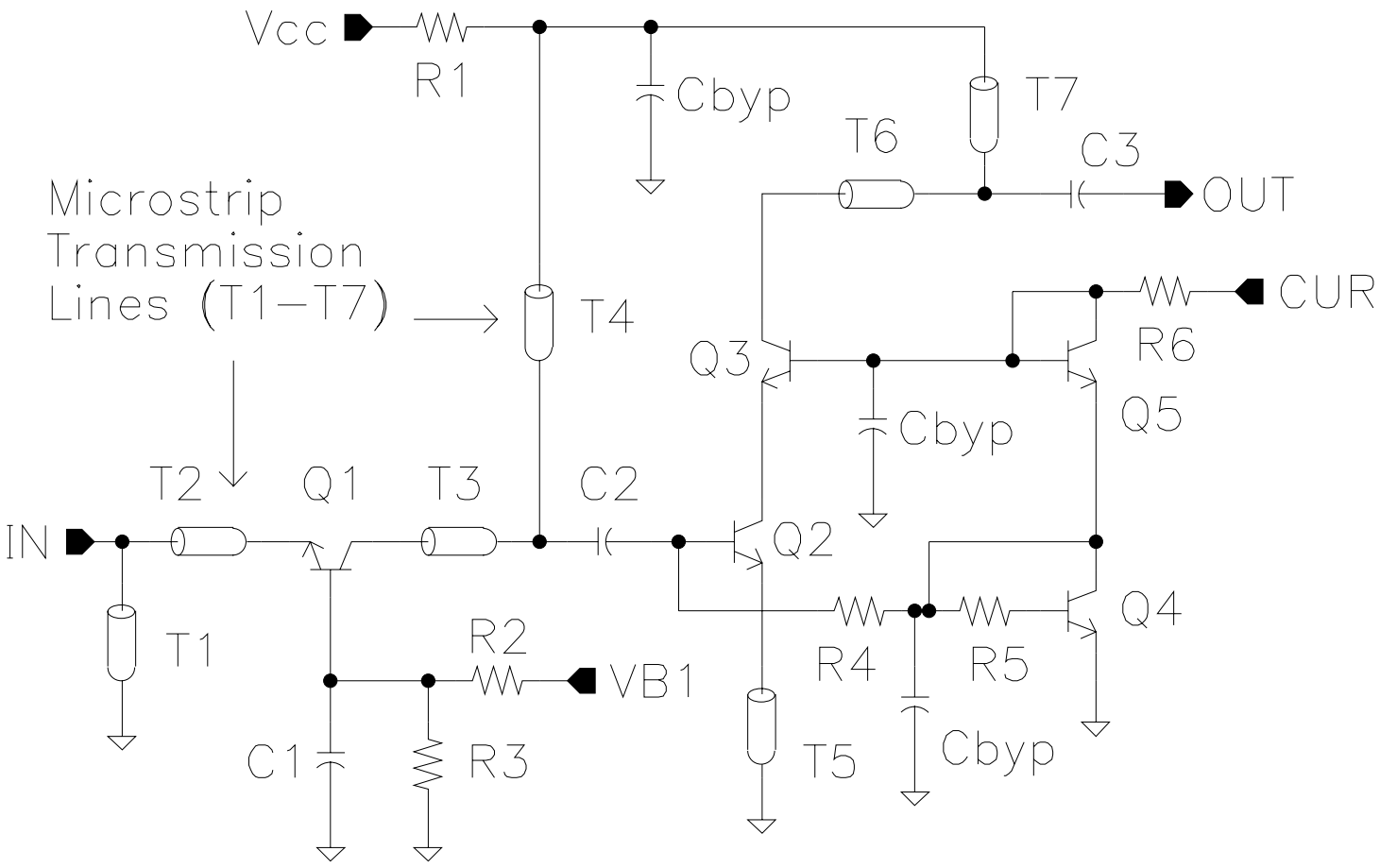

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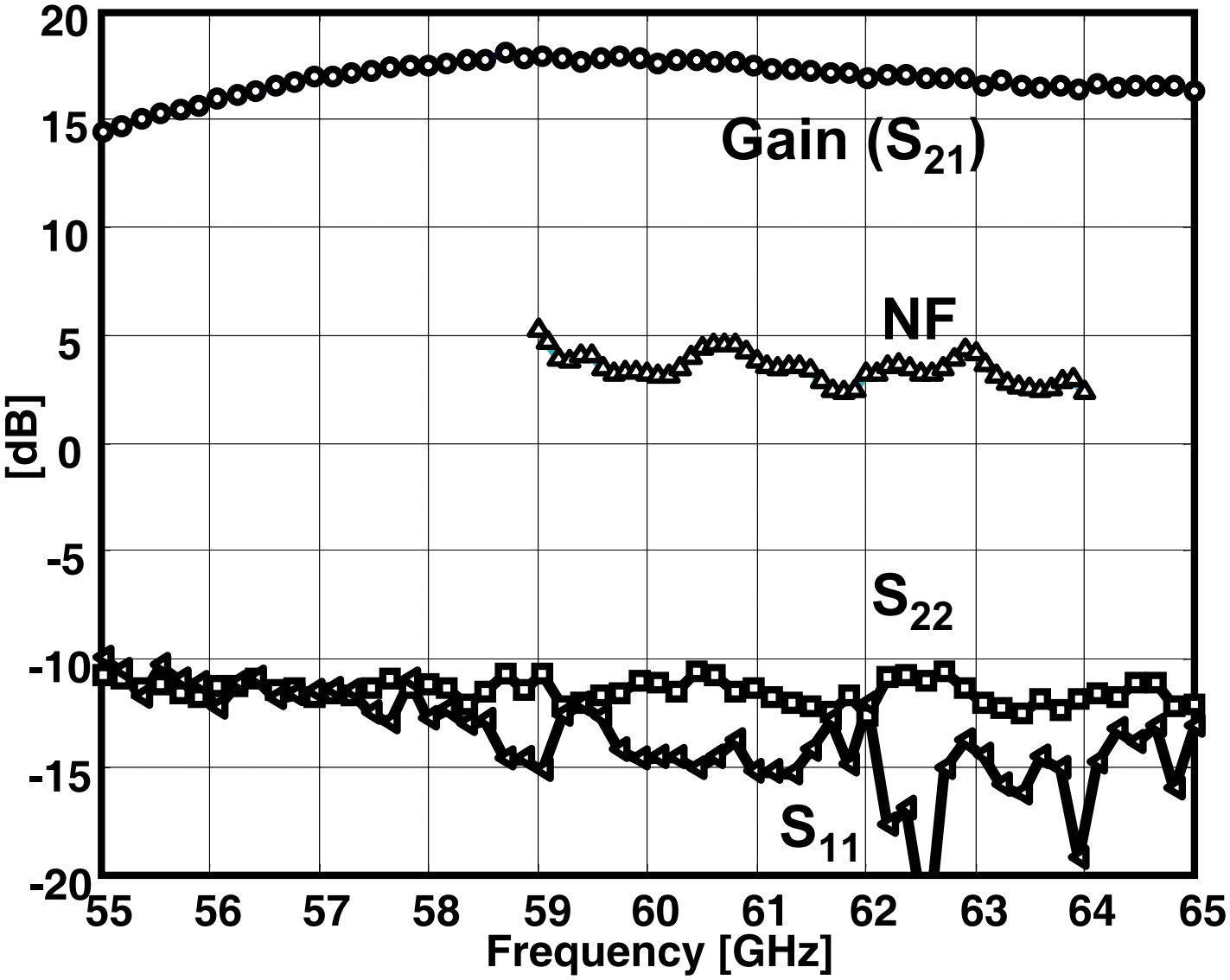

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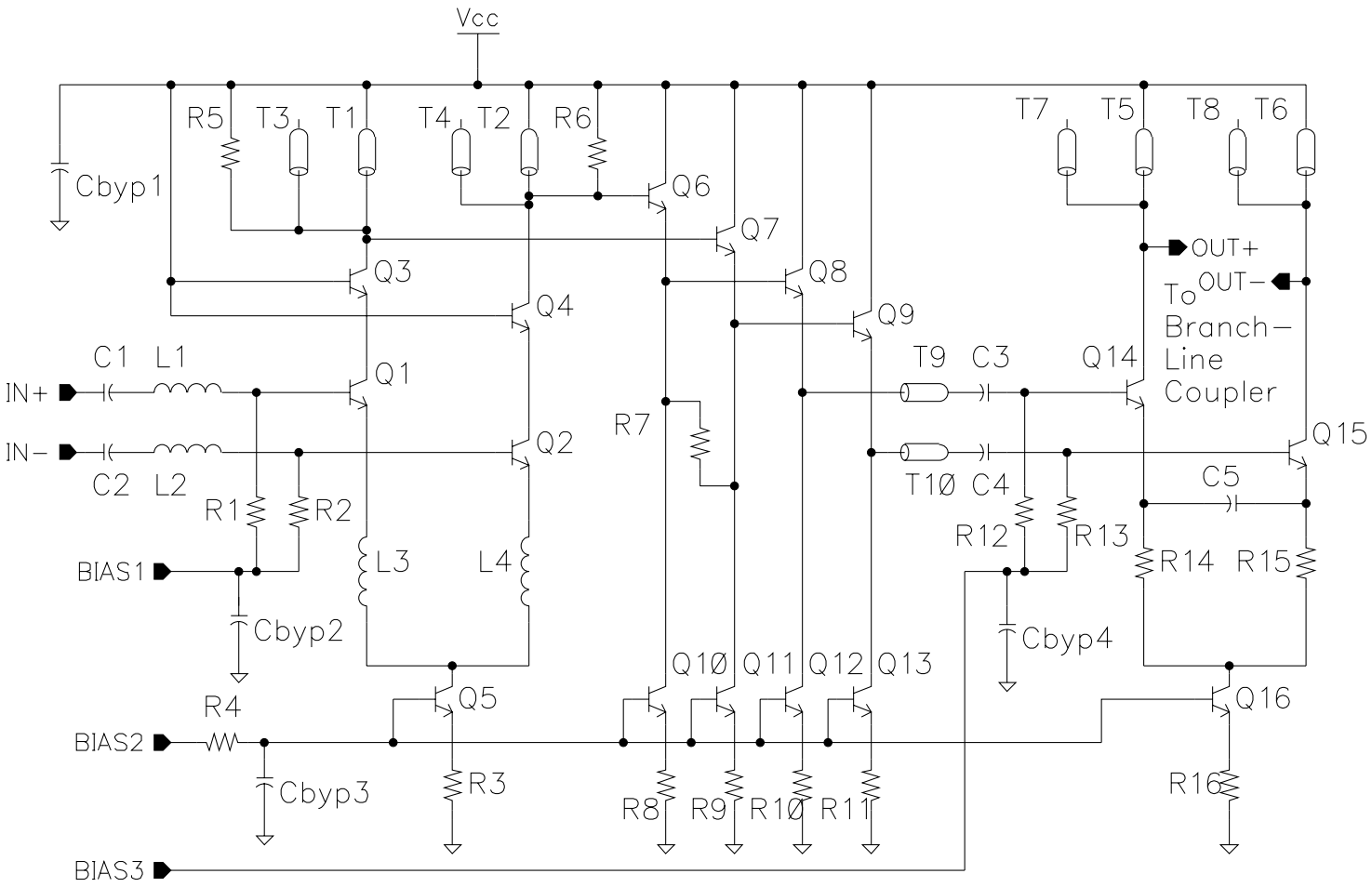

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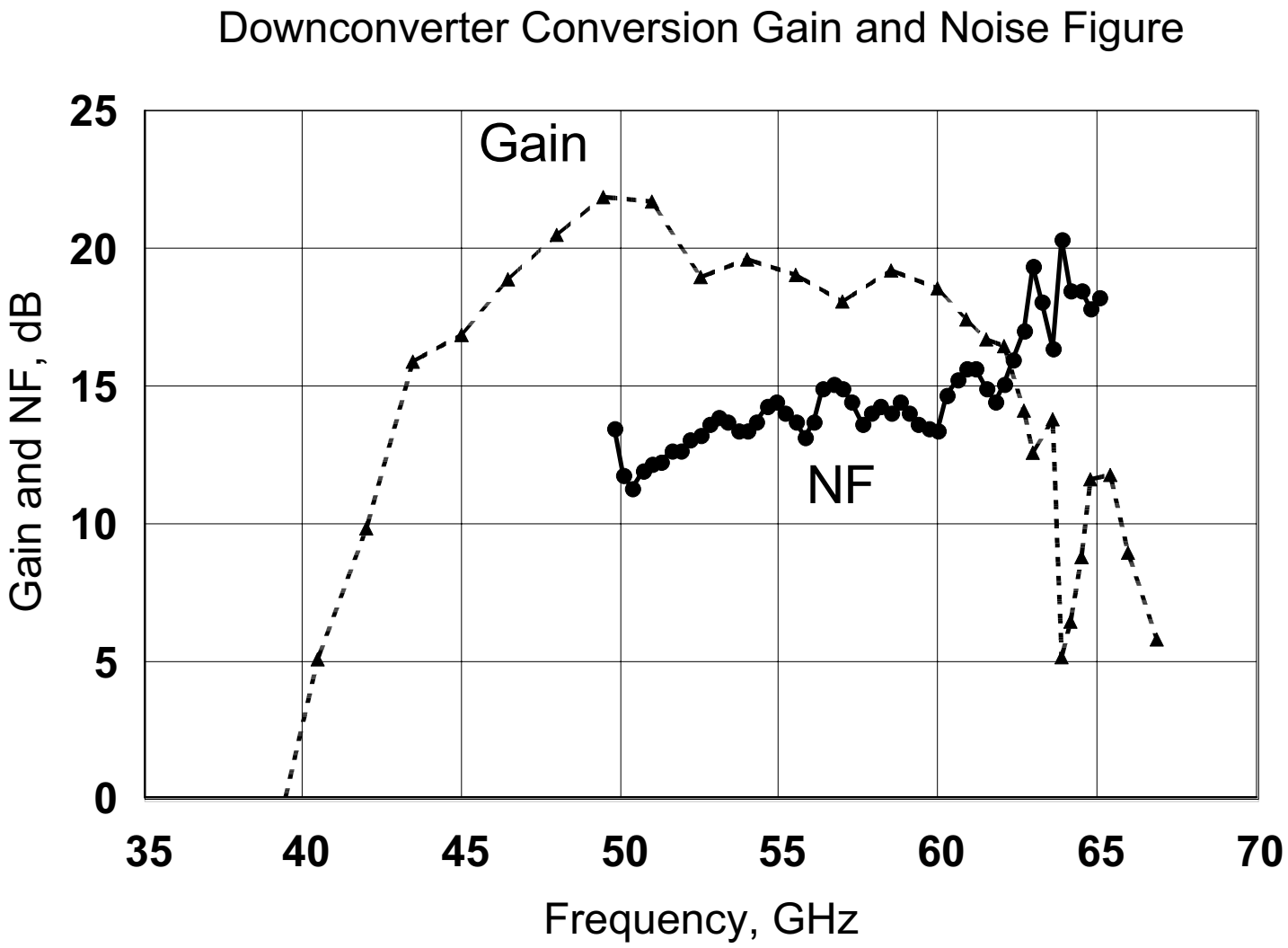

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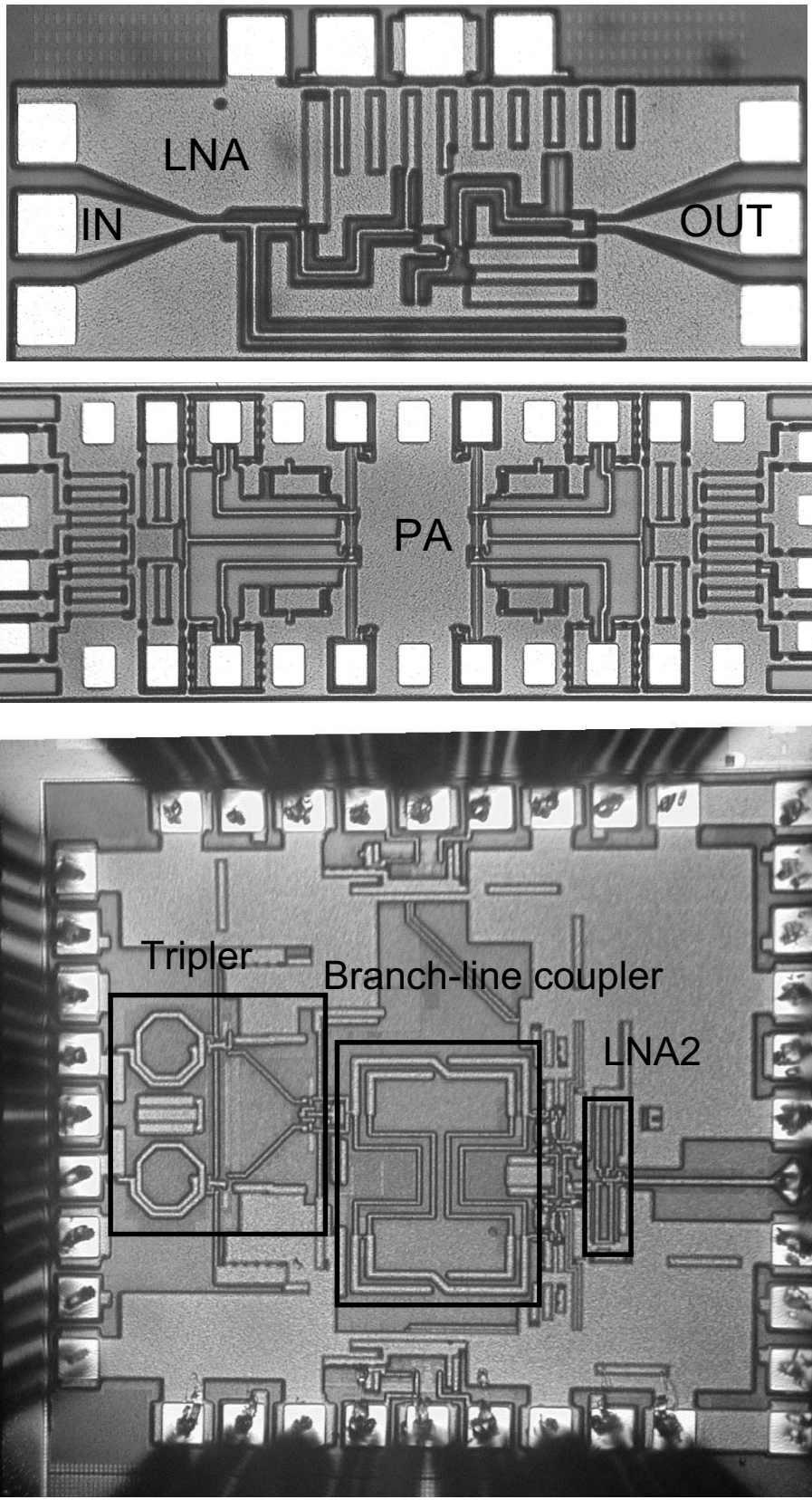

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