Design and Analysis of Broadband Dual-Gate Balanced Low-Noise Amplifiers

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***Abstract*—In this paper, we present three MMIC low-noise amplifiers using dual-gate GaAs HEMT devices in a balanced amplifier configuration. The designs target three different frequency bands including 4–9 GHz, 9–20 GHz, and 20–40 GHz. These dual-gate balanced designs demonstrate the excellent qualities of balanced amplifiers in terms of stability and matched characteristics, while demonstrating higher bandwidth than designs with a single-stage common-source device. Additionally, noise performance is excellent, with the 4–9 GHz LNA demonstrating <1.75 dB noise figure (NF), the 9–20 GHz LNA <2.75 dB NF and the 20–40 GHz LNA <2.5 dB NF. Demonstrating high gain and excellent bandwidth, the dual-gate devices seem a logical choice for the balanced amplifier topology.**

***Index Terms*—Balanced amplifier, dual gate, high electron mobility transistor (HEMT), low-noise amplifier (LNA).**

I. Introduction

THE balanced amplifier is one of the most commonly used amplifier topologies. It demonstrates a number of virtues, including excellent bandwidth, return loss and stability, making it a reliable broadband topology. The balanced nature also provides some mitigation against processing variation and yield. For instance, a single device failure will cause a balanced amplifier gain to drop by 6 dB rather than catastrophic failure. For these reasons, they are commonly used in monolithic microwave integrated circuit (MMIC) amplifiers and for rapid development, where mature device models might not be available.

Dual-gate transistors are often used in MMIC electronics as well, typically in variable-gain amplifiers [1], [2] and distributed amplifiers [3], although more recent work has demonstrated the possibility of developing dual-gate amplifiers for W-band operation [4]. In this paper, we present a family of balanced low-noise amplifiers (LNAs) which were developed to cover an operating range of 4–40 GHz. Each of the LNAs uses Lange couplers and dual-gate transistors.

Dual-gate transistors offer a number of benefits compared to single-gate transistors. The dual-gate device allows a higher gain/stage at the expense of only modestly more complicated biasing relative to a single-gate gain stage. Additionally, the size of a dual-gate gain amplifier stage is roughly comparable to that of a single common-source gain stage and processing complexity is comparable to single-gate transistors. Therefore, the additional gain comes with limited additional manufacturing cost for the MMIC amplifier. The two gates allow higher bias operation and an increase in the transistor output impedance. Finally, dual-gate transistors also show significant reduction in total feedback capacitance compared to a single-gate transistor. If an on-stage voltage divider is used to apply the second gate bias, the sequencing and biasing is no more complicated than a single-gate amplifier design. As an additional note, stabilizing the output of the dual-gate transistor is difficult to manage over a broad bandwidth. This is easily mitigated in a balanced amplifier. Therefore, for all of these reasons, balanced amplifiers using dual-gate device is a logical MMIC LNA topology. In this paper, we expand on the material presented in [5] to include detailed design and modeling information which is essential for the circuit design success.

It should be noted that the dual-gate transistor equivalent circuit is roughly equivalent to a cascode using two single-gate transistors. Compared to a cascode, a dual-gate should have lower inductances, potentially higher gain due to a reduced number of contact resistances and a more compact footprint. However, feedback capacitances of the dual-gate transistor compared to two physically separated transistors in a cascode configuration may limit maximum operating frequency of dual-gate amplifiers compared to a cascode, due to reduced gain and degraded stability.

This paper is arranged in three main parts. In the first section, basic processing and performance of our 0.1-μm GaAs high electron mobility transistor (HEMT) dual-gate transistors is introduced. The second section is concerned solely with modeling and performance of the of the dual-gate device. In the third section, design procedure and experimental results for a family of dual-gate balanced amplifiers is discussed. Three complete MMIC designs are presented, covering bands of 4–9, 9–20, and 20–40 GHz.

II. GaAs HEMT MMIC Process and Dual-Gate Transistor Fabrication

The work in this paper uses a 0.1-μm pseudomorphic InGaAs/AlGaAs/GaAs HEMT production process suitable for both military and commercial applications at millimeter frequencies [6], [7]. The devices use electron beam (E-beam) lithography on 4-inch molecular beam epitaxy (MBE) wafers. In this process, the Schottky gate is recessed to the undoped AlGaAs layer to improve the breakdown voltage; an additional planar doped layer is employed to increase the amount of charge in the two-dimensional electron gas (in 22% InGaAs channel) which provides high current density. Furthermore, with high aspect ratio (ratio of gate length to the gate-to-channel

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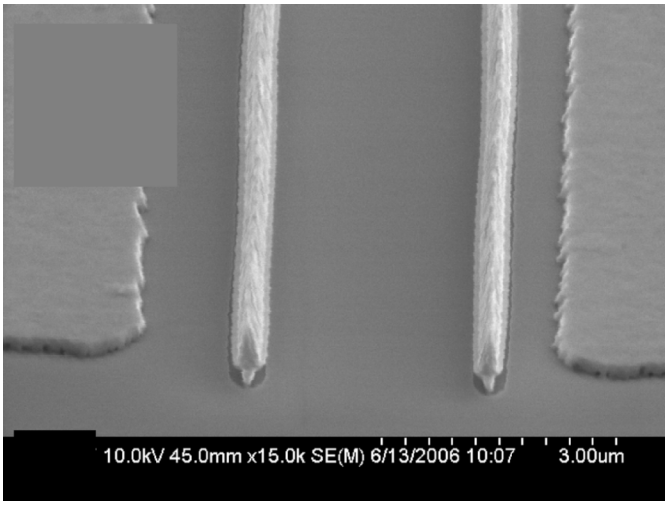

Fig. 1. SEM of a GaAs dual-gate device with 0.1-μm gate.

separation), the devices provide both high gain with high current density, and high breakdown voltage with high cutoff frequencies.

A high-yield dry-etch via process is used on 4-mil-thick GaAs substrate. With 1000 A of silicon nitride passivation, the devices show gate-to-drain breakdown voltage of up to 8 V (measured at 0.1 mA/mm reverse gate current), drain to-source voltage of about 10 V, threshold voltage of -0.4 V, maximum channel current of 630 mA/mm (measured at 0.8 V_{gs}), peak transconductance in the range of 625–725 mS/mm, and unity current gain frequency of 120 GHz at 2 V. The process uses 100 Ω/mm^2 NiCr resistors, and 300 pF/mm^2 SiN MIM capacitors.

A depiction of the dual-gate transistor taken with a scanning electron microscope (SEM) showing details is shown in Fig. 1. From a circuit perspective, a dual-gate device is biased in the same manner as two single-gate devices in a cascode configuration, with the first device being a common-source and the second a common-gate, as shown in Fig. 2. For our process, a typical biasing condition for the dual-gate device is at a drain voltage of $+4.5$ V, a second gate bias of $+1.5$ V and an appropriate bias for low-noise operation (250 mA/mm). The device is sequenced by first pinching off the first gate, then applying the second gate bias. After this, the drain bias is applied and the first gate is adjusted for appropriate current. Note that the $+1.5$ V on the second gate is chosen primarily to maintain decent circuit efficiency and can be adjusted upwards or downwards if desired. Both drains share identical current. Therefore, a method for optimizing total DC power consumption is to adjust the second gate bias while adjusting the total drain bias. By doing this, the proportion of voltage dropped internally across V_{ds1} and V_{ds2} can be optimized Since the second gate pulls little current and can be operated at a pre-determined fixed voltage, it is straightforward to use a voltage divider on the drain bias supply to apply the second gate voltage. While the voltage divider does consume some DC current, this can make biasing a high-gain dual-gate design as simple as the biasing of a single-stage, single-gate device.

A DC-IV for a single-gate and a dual-gate 200-μm device is shown in Fig. 3 for a fixed second gate bias of $+1.5$ V for the

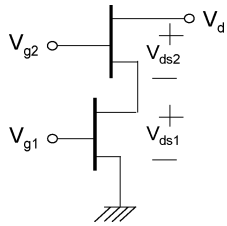

Fig. 2. Schematic configuration of HEMT dual-gate device.

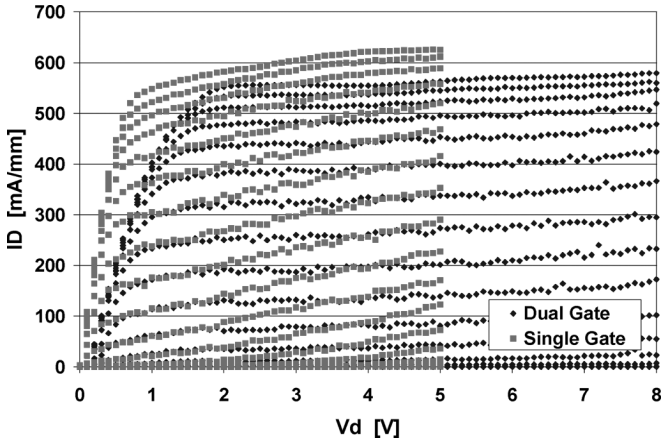

Fig. 3. Measured DC-IV of GaAs single-gate and dual-gate transistor with V_{G2} fixed at 1.5 V.

dual-gate transistor. With a fixed second-gate bias, the DC-IV closely resembles that of a single gate transistor with the exception that the dual-gate device can tolerate a higher drain breakdown voltage due to the fact that the bias appears across the entire dual-gate device.

Our device layout for the dual-gate device provides two second gate pads, one from the top and one from the bottom. These are located at the drain side of the device. For a four-finger device, the second gates are tied together using airbridges across the device. In a manner analogous to source grounding on a common-source device, the second gate bypassing plays a strong role in determining stability characteristics of the device in the circuit.

The dual gate transistor was fabricated using an electron beam lithography (EBL) process that has been employed in our production line. Vistec's EBPG-5000 system and a double layer resist scheme (PMMA-MAA/PMMA) are used. Due to the proximity of the two gate fingers, to avoid the proximity effect induced by the back-scattered electron during EBL exposure, special attention to exposure conditions and layout modification is carried out to ensure the size of each gate of the dual gate fingers are identical and they are the same as the referenced single gate size. A typical gate control of ± 0.02 μm (3 sigma) has been achieved by CDSEM measurements.

III. Dual-Gate Transistor Modeling

For our initial design iterations, we chose to model the dual-gate transistors simply with two standard single-gate device models that had been derived from common-source devices. Although this leaves out several important parasitics, it provides a simple starting model to pilot a basic topology.

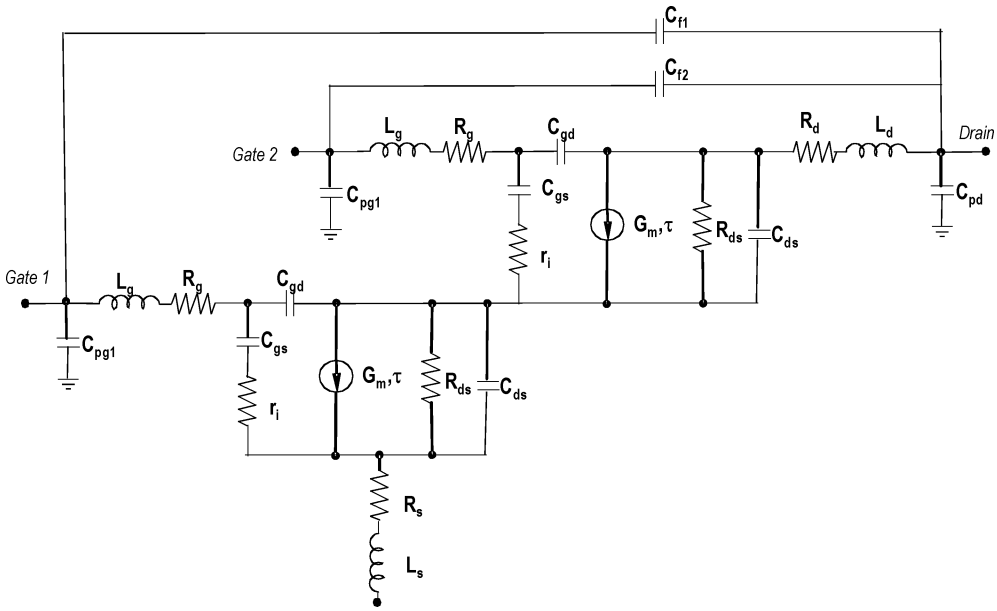

Fig. 4. Equivalent circuit of dual-gate transistor.

Once our first wafers were obtained, device measurements were performed on dual-gate measurement structures. Subsequently, a refined device model was developed for fine-tuned designs where additional device parasitics were added.

The more complete equivalent circuit model which we used is shown in Fig. 4. Note that the intrinsic parameters ($C_{\rm gs}$, $C_{\rm ds}$, etc.) for each of the two devices comprising the dual-gate transistor are assumed identical in the equivalent circuit model in Fig. 4. In reality, the true value of the parameters is likely to be different, due both to asymmetries in the dual-gate device configuration and differences in internal biasing. However, independently fitting each parameter in the equivalent circuit model is complicated due to the large number of variables and we have chosen to assume the values are identical for these designs. Additionally, five additional capacitors have been added to the equivalent circuit model to describe some coupling phenomena that the combination of simple single-gate models did not describe. $C_{\rm PG1}$, $C_{\rm PD}$, and $C_{\rm PG2}$ are added to model extrinsic feed capacitance and end of finger fringing capacitance that does not scale with device width. For a single-finger device model, these are often lumped with the other device capacitance by making total capacitance a sum of the intrinsic and extrinsic capacitance. This can lead to a misleading device model if the practice is done with a dual-gate device. In particular, if $C_{\rm PD}$ is added to the upper $C_{\rm ds}$ rather than going to ground, it would then appear in series with the lower $C_{\rm ds}$ and be shielded from ground. In this case, the model would predict a misleadingly low output capacitance. Feedback capacitances $C_{\rm f1}$ and $C_{\rm f2}$ are used to model coupling between the two gates and drain. From our design of different band amplifiers using different device sizes, these also appear to scale with device size. Although not a systematic rule of thumb, it has been experimentally determined that the additional capacitances can be largely ignored for our lowest band design (4–9 GHz), $C_{\rm f1}$ and $C_{\rm f2}$ need to be added for accurate prediction of the next higher band (9–20 GHz), and all capacitances appear necessary for the highest band that we have designed (20–40 GHz).

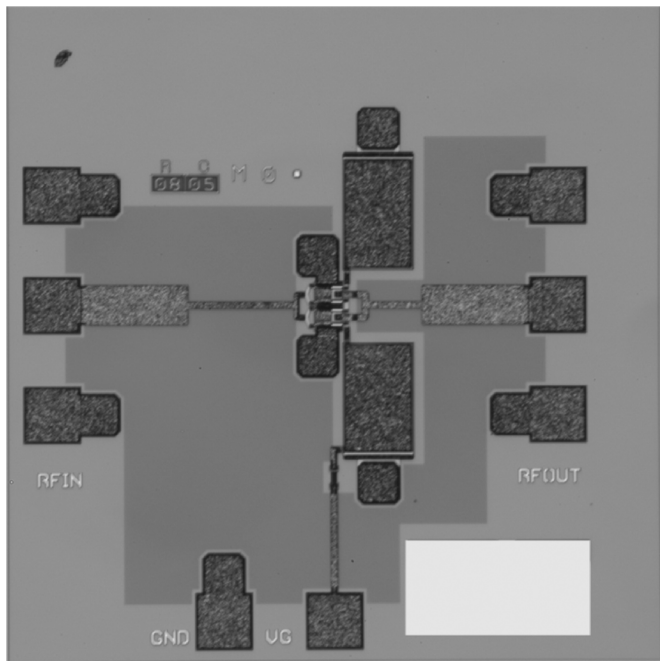

Fig. 5. Microphotograph of the dual-gate device "core" which has been used to optimize small-signal and noise models. Clearly visible are two bypass capacitors used as a bypass to the second gate. Gate 1 bias and drain bias are applied through the RF probes.

For LNA design, an accurate noise model is also necessary. In our initial iteration, we use a standard correlated noise model derived for a standard single-gate device in common-source configuration. A good overview on noise in FET and HEMT transistors can be found in [8]. Included with the first mask are simple device test structures which were used for noise parameter measurements and subsequent noise model optimization, which was done after first optimizing the small-signal S-parameter model.

Obtaining good device measurements for the dual-gate transistor is complicated by the fact that it is a multi-port network. In our case, two contacts are used for the second gate connection

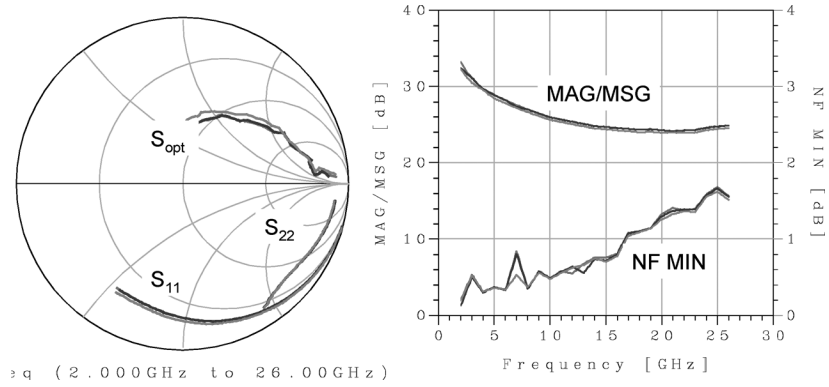

Fig. 6. Measured performance of dual-gate device core de-embedded to device reference plane. Measurement was performed over a 1–26 GHz bandwidth. Note that second gate bypassing network and source via are not de-embedded from the measurement.

to obtain symmetric feeding and low inductance. Therefore, the transistor layout has a total of four ports, which means it is impossible to fully characterize on a two-port vector network analyzer (VNA) setup. While this could potentially be remedied if we had a multi-port VNA available for characterization, device stability due to the second gate termination may still be an issue. Our solution to this is to include test structures on each masking consisting of the device "core" circuitry exactly as it appears in the circuit, as shown in Fig. 5. Bypassing of both terminals of the second gate is included on the die, and second gate bias is applied from the bottom. Although this is not an ideal solution for characterization, our experience to date shows that this can be effectively used to develop and fine tune the dual-gate device model.

Measured performance of the device test cell over a 1–26 GHz bandwidth is shown in Fig. 6, with S_{11}, S_{22}, and S_{OPT} shown on the left and the MAG/MSG and NF_{MIN} shown on the right. Note that NF_{MIN} appears to be trending towards 0 dB at frequencies less than 2 GHz, which is unphysical. This is due to the dynamic range of the noise parameter testset, which as a practical limit has difficulty providing accurate NF_{MIN} and S_{OPT} data for noise levels below 1 dB. This is also probably the cause for the atypical shape of the S_{OPT} trace at lower frequencies. Therefore, the noise parameter data is questionable below $\sim$4 GHz. In general, the shape of S_{11} is quite similar to a typical single gate transistor, but S_{22} is considerably different due to the shielding effect of the second gate.

As shown, the device cell shows more than 20-dB MAG at 26 GHz. Note that the data is referenced to the gate 1 and drain reference plane, but the network at the second gate or the substrate vias at the source has not been de-embedded, which causes the MAG/MSG in the plot to trend up as the frequency increases. This is due to feedback from the bypassing networks at the second gate, which in the measurement is an unseen additional port capable of modifying the measured two-port S-parameters. Series resistance is commonly used in the second gate bypassing network to prevent high frequency instability due to the *L-C* bypassing network. We have used an alternate technique of carefully optimizing the *L-C* bypassing network at the second gate for in-band stability and noise figure as well as gain flatness. Out-of-band stability is insured in the actual circuits through the design of the drain decoupling networks. Therefore, it is important to remember that the measured data is the for the composite device and bypassing networks.

IV. Circuit Design and Measurement Results

To develop the potential of dual-gate devices in a balanced amplifier configuration, we have performed designs for a number of frequency bands, including 4–9 GHz, 9–20 GHz and 20–40 GHz. In this section, we discuss basics behind the design including design and analysis of MMIC compatible Lange couplers as well as stabilization and biasing of the dual-gate transistors. This section also includes measured data for the three MMIC designs. The designs were performed over two masks, with the 4–9 GHz and the 9–20 GHz being piloted on the first mask and then iterated on the second. The 20–40 GHz design shown is from its first iteration. The 4–9 GHz and 9–20 GHz LNAs were prototyped using two single-gate device models in the correct configuration. The model was improved for the second mask set, with the feedback capacitances C_{f1} and C_{f2} added. The second mask added the 20–40 GHz design.

The 4–9 GHz and 9–20 GHz LNAs both use a single dual-gate device for each of the single-ended amplifiers in the balanced design. Both circuits use the same circuit topology with different frequency responses obtained by optimizing the passive circuitry. The schematic common to both of them is shown in Fig. 7. The device for both of these designs is embedded exactly as shown in Fig. 5.

For the 20–40 GHz design, the associated gain at the higher frequencies has dropped enough that the common-gate device has a fairly significant contribution on overall noise figure due to the fact that there can be no internal noise matching between the common-source and common-gate portions of the dual-gate device. Therefore, we use a common-source device at the input of each single-ended amplifier to help set the noise figure. A schematic illustrating this is shown in Fig. 8.

Each of these amplifiers uses a Lange coupler in a standard microstrip configuration. A broad review of coupled line microwave circuits including the Lange coupler can be found in [9]. The Lange coupler realizes a tight, 90° coupling by connecting two interdigitated couplers with airbridges interconnects. The Lange coupler is extremely useful for amplifiers circuits due to its property of showing matched return loss to

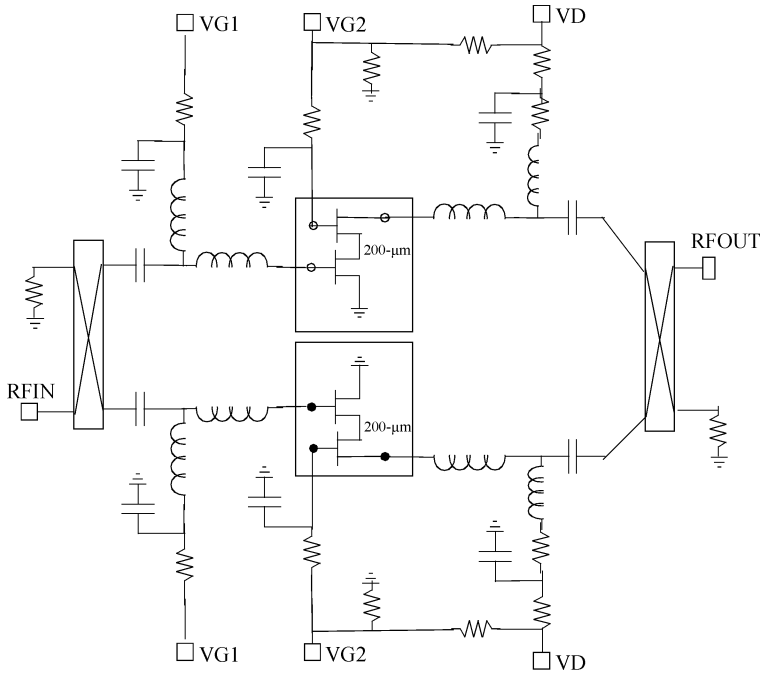

Fig. 7. Equivalent circuit of the 4–9 and 9–20 GHz dual-gate balanced amplifiers.

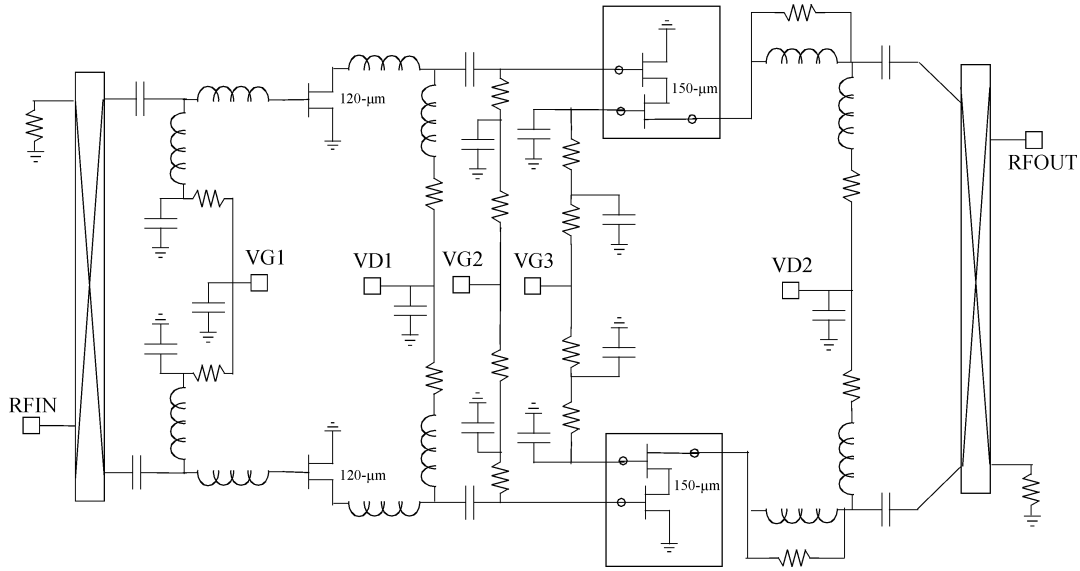

Fig. 8. Schematic of 20–40 GHz balanced dual-gate low-noise amplifier. Note that DC distribution is simplified.

the external circuit, while the internal circuit is matched for best noise performance if used in a low noise amplifier. The Lange coupler is widely used in broadband microwave frequency circuits. Since the physical length of the coupler is a quarter wavelength in the coupled microstrip mode, its implementation on chip is limited by its physical size to higher frequencies.

On a GaAs substrate, each of the coupled lines in our Lange coupler is implemented with a 7-μm wide strip and uses a 7-μm gap between adjacent lines. Our GaAs MMIC metallization process contains a 3.5-μm plated "top" metal and a 0.7-μm evaporated metal, with the top metal available for routing and airbridging. The 0.7-μm evaporated is used for routing and underpasses. For the Lange coupler presented in this work, the coupled lines are implemented entirely in top metal except for minimal regions where airbridges must be used to interconnect lines. Since the conductor thickness is fairly comparable to the coupled line gap, precise design requires electromagnetic simulation with metal thickness included.

The first design consists of the 4–9 GHz balanced amplifier. A photograph of the fixtured 4–9 GHz low-noise amplifier is shown in Fig. 9, with the RF input at the bottom left and RF output at the top right. At this frequency, chip size is strongly dominated by the length of the Lange couplers, which we did not meander. All bias is from the top of the chip, with DC bias lines airbridged across the top Lange coupler. Matching is done with both inductive microstrip transmission lines and spiral inductors. The dual-gate device is a 4-finger device with a total of 200-μm of periphery. Backside vias are placed in as close

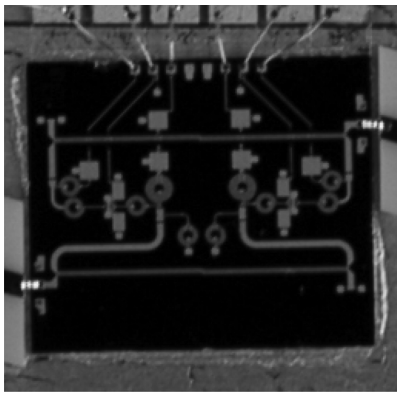

Fig. 9. Fixtured 4–9 GHz dual-gate low-noise amplifier. Chip size is 3200×3800 μm with all bias applied from the top.

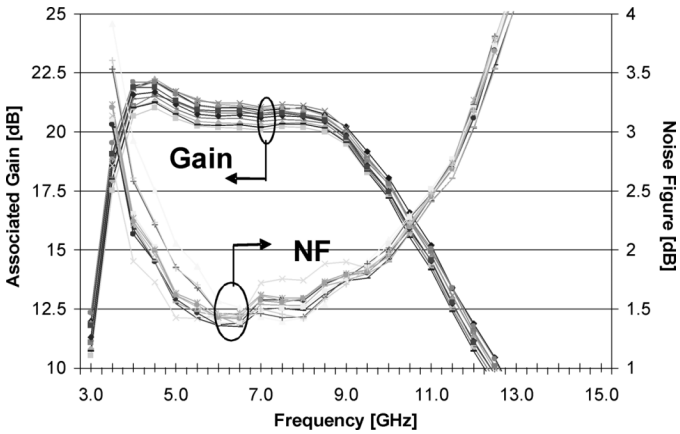

Fig. 10. Measured on-wafer noise figure and associated gain for 11 sites across the wafer for the 4–9 GHz design.

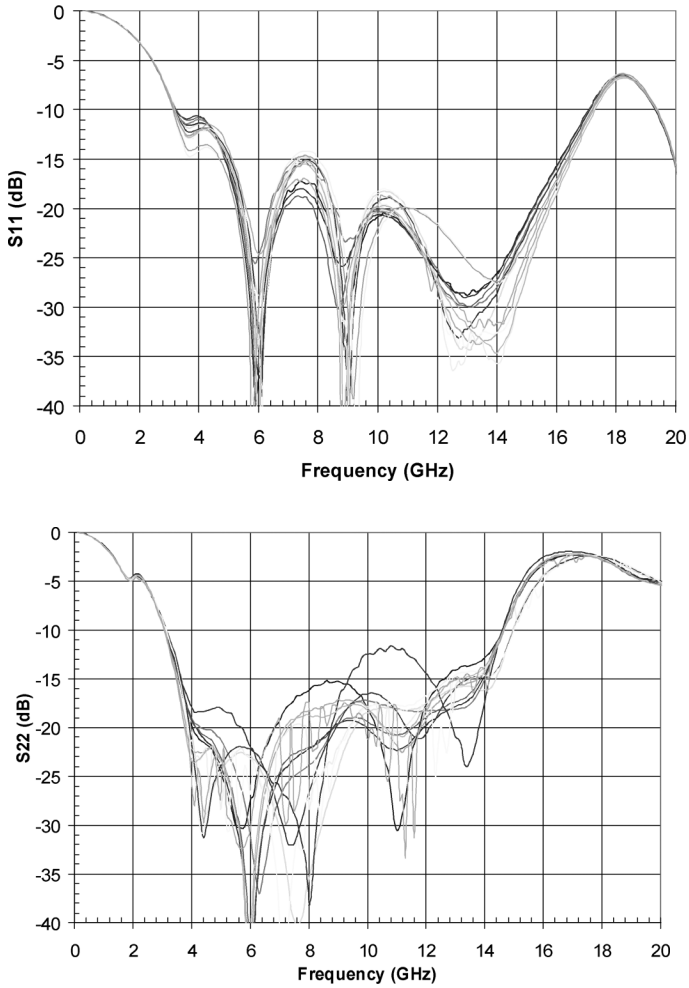

Fig. 11. Measured S_{11} and S_{22} across wafer for the 4–9 GHz design.

proximity as standard design rules will permit. For device stability, second gate bypassing is critical. To maximize gain, no resistive components were used. Instead, two 7.5 pF capacitors are used with the layout of the bypassing optimized for stability inside the operating band. Additionally, stability analysis was performed with all nodes of the dual-gate device, including the second gate. Outside the operating band, stability is taken care of through the DC biasing networks. An additional shunt spiral inductor is added to improve low-end match to S_{OPT}.

On-wafer measured noise figure and associated gain are shown in Fig. 10 for 11 sites measured across the wafer. While there is some site-to-site difference in gain, for a given site, measured gain flatness is $\sim \pm 0.5$ dB with a nominal value of ~ 20.5 dB. The high single-stage gain is one of the benefits of using dual-gate devices in a balanced configuration. The noise figure is < 2.0 dB across the entire 4–9 GHz band, except for two sites that lay out of family and are most likely due to poor probe contact during the on-wafer test. Note that the amplifier is biased at optimal low-noise bias of 3.75 V and a total current of 50 mA. Input and output match is shown in Fig. 11 and is better than 10 dB for both S_{11} and S_{22} from 4–14 GHz. All sites on the entire wafer are shown in Fig. 11.

The second design is a 10–20 GHz design which uses the same basic configuration (200-μm dual gate device with two 7.5 pF MIM capacitors for bypassing of the second gate). A photograph of the fixtured MMIC is shown in Fig. 12. For additional high frequency stability, two *R-L* stabilization networks are used added to the basic topology shown in Fig. 7. The first networks consists of a 40-Ω thin film resistor (TFR) with a 10×70-μm section of microstrip looped around it and placed as closely as possible to the device output. The second one also uses a 40-Ω TFR, but uses a loop of $\sim$ 150 μm length of microstrip line. These networks are properly modeled as a parallel *L-R* network which is increasingly dissipative at higher frequencies. Their practical purpose are for stabilization above 40 GHz.

Measured noise figure and associated gain are shown in Fig. 13 for 30 sites across the wafer. Site-to-site spread in gain is a maximum of approximately 2 dB. Nominal gain is $\sim$ 17 dB with ± 0.5 dB gain flatness from 8–22 GHz. Except for two outlier sites, noise figure is less than 2.25 dB for this bandwidth as well. Input and output match is shown in Fig. 14, with the match being better than 10 dB over a 6–24 GHz bandwidth. All sites on the wafer are shown in this plot. We have also measured saturated performance of this chip as well, as is shown in Fig. 15. From this, the measured $P_{1\mathrm{dB}}$ for the MMIC is 15 dBm. Note that the amplifier is biased at optimal low-noise bias of 3.75 V and a total current of 50 mA.

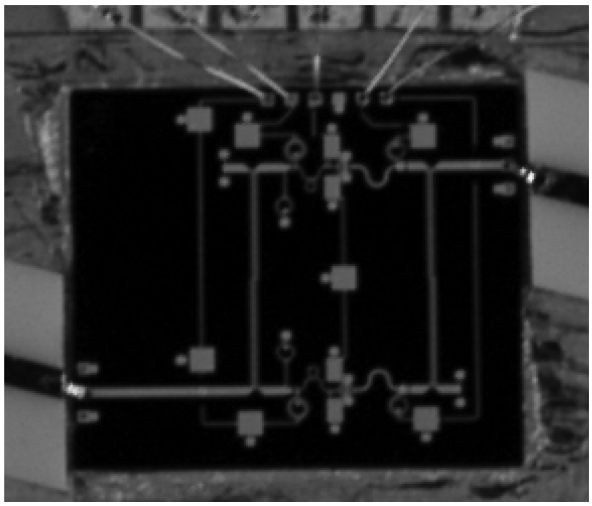

Fig. 12. Fixtured 9–20 GHz dual-gate low-noise amplifier. Chip size is 3200×3800 μm with all bias applied from the top.

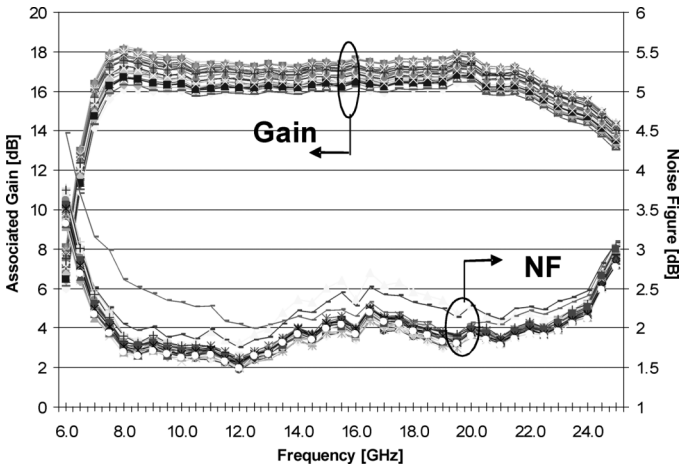

Fig. 13. Measured on-wafer noise figure and associated gain for 30 sites across the wafer for the 9–20 GHz design.

The final amplifier is designed to operate over an 18–40 GHz bandwidth. To keep noise performance as good as possible, a standard single-gate 120-μm device with four fingers is used at the input and a dual-gate 150-μm device with four fingers is used at the output. Although the previous two designs used two symmetric 7.5 pF second gate bypassing networks, this design uses bypassing at the top gate feed with a 4 pF MIM capacitor grounded by two backside vias and the second gate feed used to apply DC bias through a large value TFR directly at the second gate. High-end out-of-band stability is achieved with a 7.5-Ω TFR resistor with a loop of 60-μm to 10-μm wide transmission line around it. Spiral inductors are used only in the inter-stage, with most matching being accomplished using inductive microstrip transmission lines. The input uses capacitive open-ended microstrip transmission lines to optimize high-end match and radial stubs at the output for the same purpose. Total chip size is 4300–2000 μm. A microphotograph of the chip is shown in Fig. 16.

Measured on-wafer circuit performance is shown in Fig. 17. For this circuit, gain variation is considerably higher, $\sim \pm 3$ dB

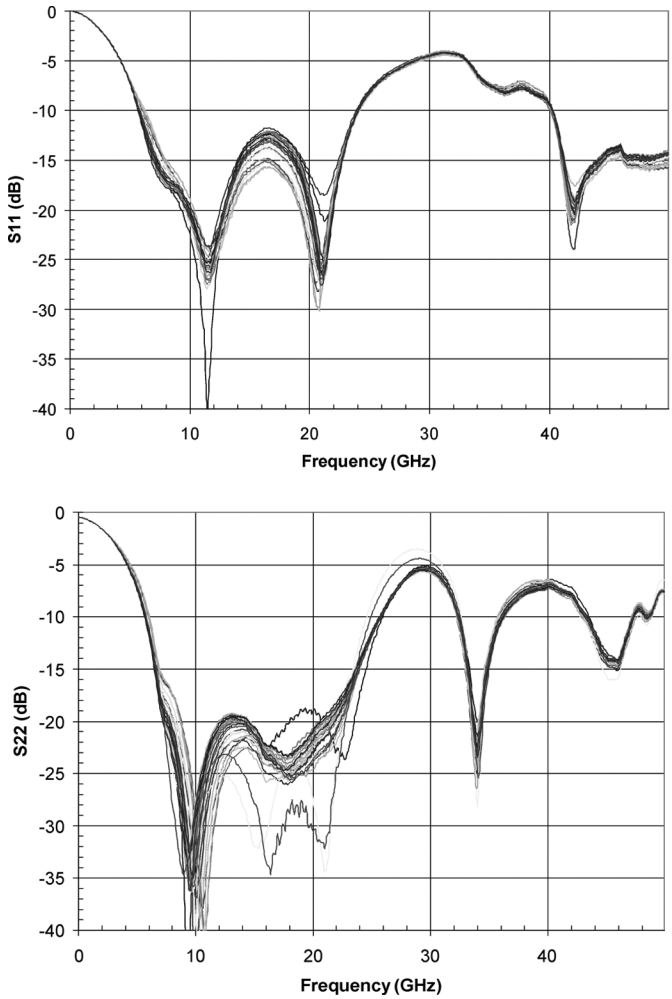

Fig. 14. Measured S_{11} and S_{22} of 9–20 GHz amplifier across the entire wafer.

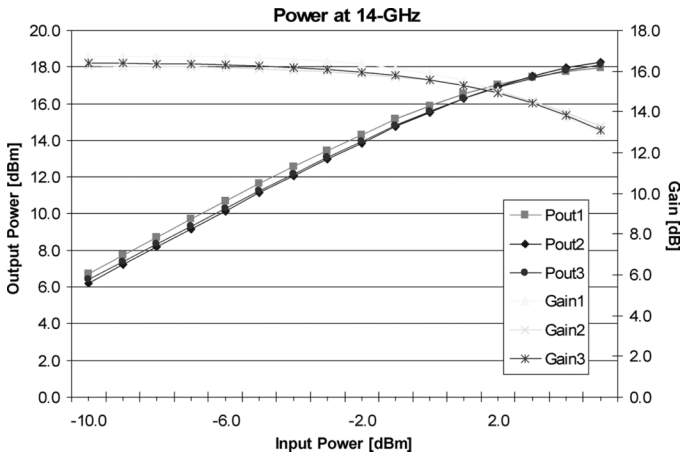

Fig. 15. Measured saturation characteristics of 9–18 GHz balanced amplifier for three sites measured on-wafer. $P_{1\mathrm{dB}}$ is approximately 15 dBm. The amplifiers are biased at 3.75 V across the dual-gate device and a total of 50 mA.

and optimal noise figure is not reached until 20 GHz. However, noise figure in the 20–40 GHz bandwidth is < 2.5 dB across the entire 20–40 GHz bandwidth. Gain is centered at ~ 20 dB. With additional iterations, it should be possible to improve the

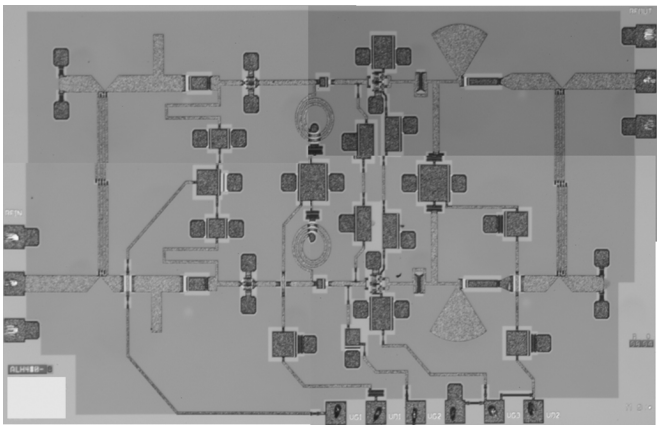

Fig. 16. Microphotograph of 20–40 GHz design.

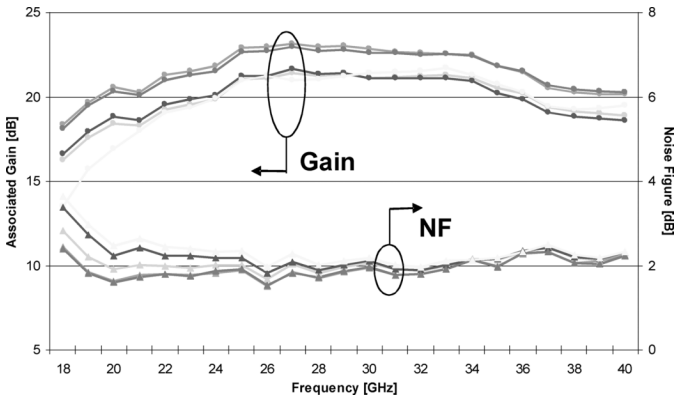

Fig. 17. Measured on-wafer noise figure and associated gain for four sites across the wafer for the 18–40 GHz design.

gain flatness across the bandwidth and improve low-end noise figure and gain.

V. Conclusion

In this paper, we have presented three broadband balanced low-noise amplifiers using dual-gate HEMT devices on a standard GaAs HEMT process. The dual-gate device enables high gain without compromising any of the beneficial attributes of the balanced design. Additionally, the higher frequency band uses a common-stage driver stage to insure excellent noise figure. We have also shown measured dual-gate transistor characteristics. At the expense of modestly more complicated biasing, the dual-gate device can be used in similar applications as compared to a single-gate device. However, the dual-gate device demonstrates significantly higher gain. In a balanced configuration, broadband high-performance MMICs can be realized.

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