Filterless Class-D Amplifier With Pseudorandomized Carrier Frequency Modulation for EMI Reduction

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***Abstract*—This paper presents a filterless Class-D amplifier with pseudorandomized carrier frequency modulation (PRCFM) to mitigate electromagnetic interference (EMI) issue associated with the removal of an off-chip *LC* filter. The designed filterless Class-D amplifier occupies a total area of 1 mm^2 and is fabricated in 0.18-μm CMOS process technology. The proposed PRCFM circuit occupies only less than 1% of the IC area. Measurement results have demonstrated the effectiveness of the PRCFM scheme for EMI reduction. The PRCFM scheme consumes very little additional power and therefore does not affect the power efficiency of the amplifier. In addition, the proposed scheme also maintains very good total harmonic distortion over the audio band of interest (100 Hz to 6 kHz) and modulation index range.**

***Index Terms*—Electromagnetic interference (EMI), filterless Class-D amplifier, pseudorandomized carrier frequency modulation (PRCFM), spread spectrum.**

I. Introduction

SIZE and power efficiency are critical design concerns in portable applications. Class-D amplifier offers a very attractive option in portable audio applications for its excellent power efficiency, typically higher than 80%. A Class-D amplifier consists of four basic building blocks, namely a modulation circuit, an output stage, a feedback network, and an *LC* low-pass filter. The first three building blocks are usually integrated within a chip with the *LC* filter realized off-chip due to its relatively large size. The purpose of the *LC* filter is to attenuate the high-frequency carrier and recover the low-frequency amplified input audio signal. However, the off-chip *LC* filter is both costly and area inefficient, which occupies about 70% of the printed circuit board (PCB) area and contributes about 30% of the total cost [1]. Hence, this *LC* filter is a major barrier for miniaturization of Class-D amplifier in portable audio applications. To circumvent the size issue, a Class-D amplifier architecture without the external *LC* filter, also known as a filterless Class-D amplifier, has been reported in recent years [2]–[4]. This type of Class-D amplifier takes advantage of the natural frequency response of the human ear, which acts as a band-pass filter in the audio frequency range.

As a result of its high-frequency switching-mode operation, a Class-D amplifier contributes significant electromagnetic interference (EMI). It is well known that the Class-D output stage is a major EMI generation source, which results in sharp spikes in both output pulsewidth modulation (PWM) signal and the power supply bus. These spikes translate to a wide spectrum of harmonics in the frequency domain and pose EMI threat to other circuits [5], [6]. The EMI generated by the switching operation during the power conversion process can be coupled to other circuits that share the same dc power bus through conduction or directly coupled to other circuits on the same PCB through near-field coupling. So it requires special attention in its design to ensure electromagnetic compatibility (EMC).

The most straightforward EMI mitigation technique is to add a low-pass passive filter after the output stage. Due to the relatively large L and C values, integration of an *LC* low-pass filter within the chip is prohibitive and an off-chip *LC* filter becomes the only option. However, the off-chip filter adds not only the design cost but also cost in terms of area. From the cost perspective, it is more effective to suppress EMI at the source instead of additional filter. Various EMI mitigation techniques for switching convertors have been reported, for examples, soft switching [7], [8] and spread spectrum modulation (SSM) [9]–[21], which directly work on the suppression of EMI caused by the high-frequency switching of the output stage.

Soft switching slows down the switching transitions and as a result, reduces the transient current drawn from the power source during the transition period so that the magnitudes of high-frequency harmonics can be reduced [8]. However, with the trend of higher switching frequency, there is a limit on using such method to mitigate EMI. On the other hand, SSM reduces the peak EMI noise amplitudes by spreading the EMI energy over a wider frequency spectrum, instead of concentrating the EMI energy in its respective harmonic frequencies, which makes it suitable for a high-frequency operation. In general, SSM can be categorized into three types, namely the randomized SSM, periodic SSM, and pseudorandomized (PR) SSM. True randomized SSM is difficult to realize in practice because the switching frequency is hopped in the entire spectrum. It is also not preferred for audio applications due to its uncontrollable switching frequency range. For periodic SSM, the switching signal is modulated with a periodic modulation signal, such as a sinusoidal and a triangular waveform. The switching frequency range is determined by the frequency of the modulation signal. However, the periodic SSM introduces sidebands around the original frequency of the modulated signal [22]. To eliminate sidebands in

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the frequency of interest, PR SSM closely resembles the operation of true randomized SSM but with additional control so that it can randomly vary the switching frequency within the predefined range to avoid signal violation in the audio band [23].

In recent years, the application of the PR SSM technique to reduce EMI in a Class-D amplifier has shown promising results [9]–[12]. The PR PWM technique, which was realized by linear feedback shift register (LFSR), was proposed and verified using discrete components for high-power Class-D amplifier applications [9], and integrated spread spectrum architecture was implemented for low-power Class-D amplifier in portable audio applications [10]–[12]. In [11] and [12], a spread spectrum technique based on PR modulation was designed using 0.5-μm CMOS technology. The PR modulation technique modulated the carrier frequency by using a current scaling DAC and a 17-bit LFSR. The reported energy attenuation about the carrier was about 12 dB. In these designs, the major challenge for the modulation is the realization of EMI mitigation scheme without compromising the total harmonic distortion (THD) performance, which is crucial in audio applications.

In this paper, we investigate the use of PR techniques for carrier frequency modulation and its effectiveness for EMI reduction in filterless Class-D audio amplifier. Based on our investigation, we propose a pseudorandomized carrier frequency modulation (PRCFM) scheme, which is realized by a 5-bit LFSR and an 8-bit clock divider, to generate the random modulated carrier. Although the proposed PRCFM uses only 5-bit, it has been demonstrated to be effective in suppressing EMI as well as meeting the THD requirement. We have also studied the relationship between the noise floor in audio band and the number of PR bits used. A first-order estimation of EMI reduction with the number of PR bits is also derived so that the designer can optimize the PR modulation design to achieve the best EMI reduction as well as modulation size. In addition, the impact of PR modulation on THD is investigated and a solution using clock divider is proposed to minimize such impact. The design is implemented in CSM 0.18-μm CMOS technology with the aim of further reducing the size in both Class-D amplifier and PRCFM architecture.

The paper is organized as follows. Section II describes the design of the proposed filterless Class-D amplifier and PRCFM circuit. In Section III, the effectiveness of PRCFM in EMI reduction is demonstrated. THD and power efficiency performances of the proposed Class-D amplifier are also validated experimentally. Finally, a conclusion is drawn in Section IV.

II. Proposed Filterless Class-D Amplifier With PRCFM

Fig. 1 shows the proposed filterless Class-D amplifier with the PRCFM. It consists of four major building blocks, a carrier generator with the PRCFM, a modulation circuit, a high-bridge output stage, and a differential-to-single feedback network.

The proposed filterless Class-D amplifier is designed with emphasis on low voltage and small chip area. The double-sided natural sampling PWM scheme eliminates common-mode distortion in the audio band. It utilizes an internally generated triangular waveform and a differential input signal pair. The

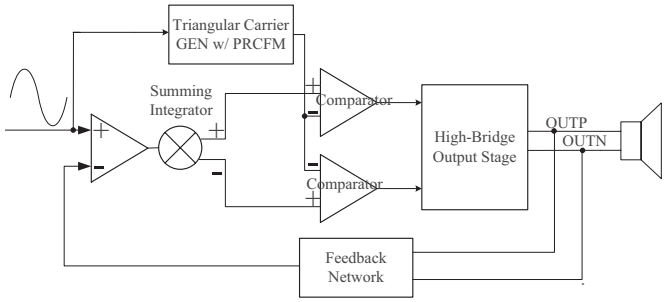

Fig. 1. Block diagram of the designed Class-D amplifier.

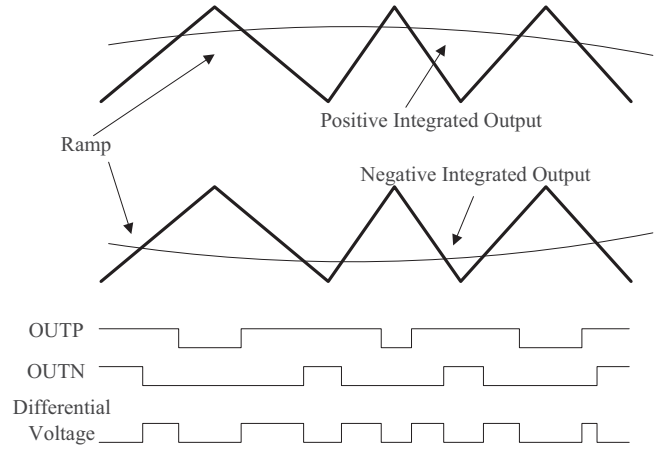

Fig. 2. Waveforms for the inputs, triangular signal, and differential signal across the speaker.

single-ended input signal, together with a feedback signal, is first fed into a preamplifier to generate the differential input signals. The outputs are subsequently connected to a summing integrator, which further removes the high-frequency residual in the feedback signal. The results and the internally generated triangular waveform are compared by the two comparators to generate nature sampling PWM signals as illustrated in Fig. 2. The frequency of the triangular waveform is controlled by the PRCFM. The output of the comparator goes high when the input signal is higher than the triangular waveform and vice versa. Since the input signals are differential, the PWM waveforms (OUTP & OUTN) generated at the output of the two comparators are in phase but having different duty ratios. As a result, the voltage across the speaker is made up of narrow pulses. Hence, the speaker is only loaded when needed, thereby reducing the power consumption.

Similar to the ordinary carrier generator, the triangular carrier waveform here is created by charging and discharging a capacitor**,** C1, as shown in Fig. 3 (upper part). The three-level cascaded current mirrors, controlled by three controlled signals, namely B, C, and D, are used to generate the varying charging currents. Signals B, C, and D are digitally controlled by weighted PR binary number resulting in random bias current levels. When PR code is at logic 0, the inverter turns OFF the PMOS and thus the current mirror and when PR code is at logic 1, the inverter turns ON the PMOS and thus the current mirror. When the current is reduced, the time period required

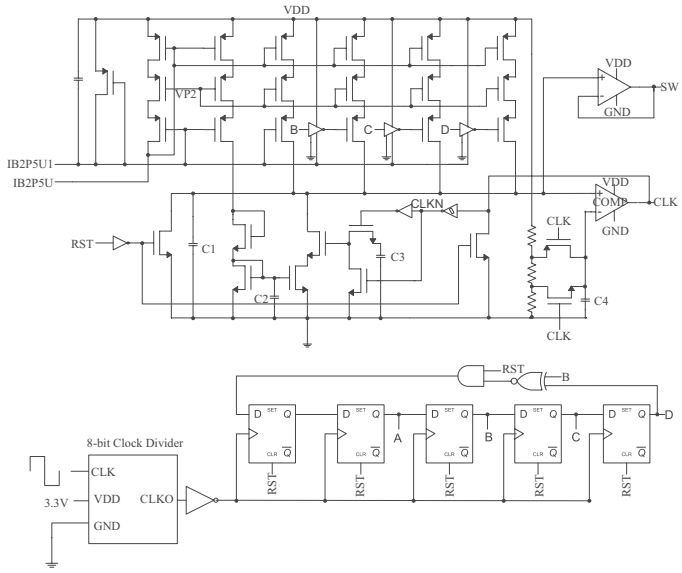

Fig. 3. Carrier generator with PRCFM.

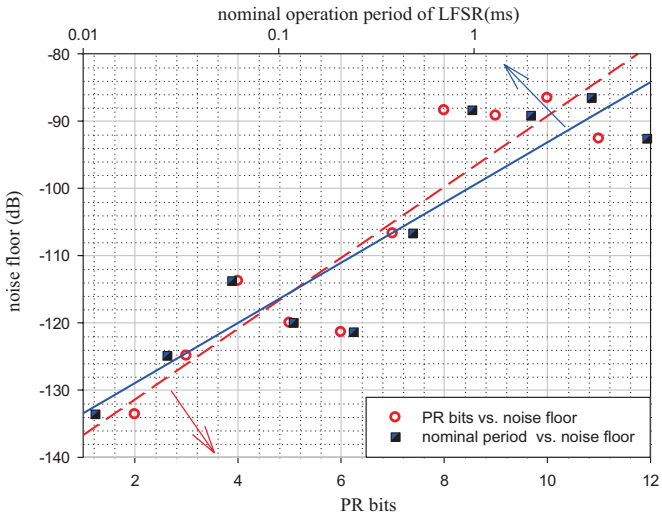

Fig. 4. Noise floor versus frequency hopping period.

for the ramp voltage to reach the high threshold voltage from low threshold voltage will be reduced. The threshold voltage is set by a resistive divider network as shown in Fig. 3. As a result, the frequency of the carrier waveform can be adjusted by varying the charging current. The spreading frequency range is determined by the variation range of the current. Fig. 3 (lower part) shows the schematic diagram of the designed PR number generator. It consists of an 8-bit clock divider and a 5-bit LFSR, which contains an array of registers with linear feedback implemented using XNOR gates. Both the clock divider and shift registers are implemented by D flip-flop. The input clock frequency f of the generator is the same as the carrier signal. In this way, the frequency is hopped at the end of carrier period if the path delay can be eliminated, to maintain good carrier linearity, which is significant for THD performance. The 8-bit clock divider first divides the input clock from f to $f/2^8$. This substantially reduces the operating frequency of the LFSR and thus the hopping frequency. In other words, each switching frequency step would be sustained for $2^8 = 256$ carrier cycles. It will be shown in the later part of this section that this design helps to improve noise performance in the audio band. The 5-bit LFSR subsequently generates the 5-bit PR numbers. The LFSR is connected such that the third and fifth register outputs are passed through the XNOR and then fed back to the first register, so that maximum PR sequence length $(2^n - 1)$ is obtained. In this case, 31 PR binary numbers (i.e., $2^5 - 1 = 31$) are generated and a 3-bit PR number is used to control the charging current.

Ideally without switching loss, the total energy of all the spread switching frequency steps is equal to the energy for one constant switching frequency. Assuming that the energy is uniformly distributed to all spread switching frequency steps, the resultant peak power noise can be calculated by the first-order estimation

$$20\log(V_s) = 20\log(V_T/2^s) \approx 20\log(V_T) - 6.02s \qquad (1)$$

where V_s and V_T are the peak output amplitudes of the amplifier with and without the PRCFM, and s is the number of the control bits. Theoretically, if the switching frequency is spread to s different frequency steps, an EMI reduction of $6.02s$ dB is expected. The practical value of s is limited by the order of the LFSR for a certain design. For the proposed design, s is set to 3.

However, the output of the LFSR is actually not truly randomized to some extent. In other words, some periodic signals are present in the random number sequence. The nominal frequency of the periodic components is $f/(2^{n+m})$, where f is the input switching frequency, n is the order of the LFSR, and m is the order of the clock divider. To make matters worse, the resultant periodic frequency steps may fall into the audio band and this will increase the noise floor. Fig. 4 shows the relationship between the noise floor and the number of PR bits used if the clock divider is not present. The same graph also shows the relationship between the noise floor and the nominal operation period of the LFSR. Note that the noise floor in the audio band would be increased when the PR bits is increased (i.e., the nominal period is increased), as illustrated in Fig. 4. This trend is reasonable, as the nominal periodic frequency of the LFSR is closer to the audio band for higher order LFSR. On the other hand, a high-order LFSR will result in more complex circuit implementation but better EMI reduction. To overcome this conflict, the clock divider is added to optimize the noise and EMI reduction performance by further pushing the nominal periodic frequency out of the audio frequency range. For example, the nominal periodic frequency for this 8-bit divider design is about 24 Hz. It may be worthwhile to note that the noise floor can be further improved with a longer hopping period and become closer to that of the conventional amplifier.

Fig. 5 demonstrates generated 1-bit PR number. It is PR and only predicable with known initial state. Fig. 6 shows the switching frequency step and time period corresponding to each digital number for the designed PRCFM. The time period for each frequency step is estimated using $\Delta t \approx 1/(f/2^8)$. As a result, the

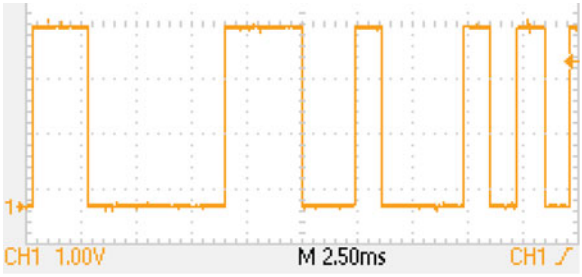

Fig. 5. Generated 1-bit PR number.

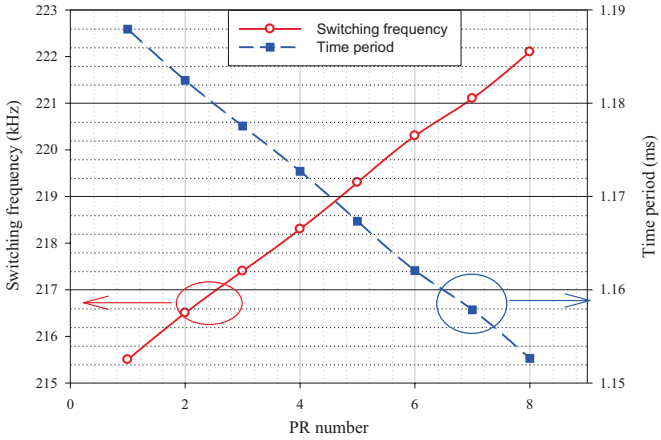

Fig. 6. Switching frequency and corresponding time period versus PR number.

frequency step is not uniformly distributed in time as illustrated in Fig. 6. Although [24] concludes that uniform distribution will lead to an optimal design taking into consideration the circuit complexity and spectrum spread, nonuniform distribution manner is adopted in this design based on two considerations: the THD issues and good noise reduction performance for a deviation from the uniform distribution.

III. Measurement Results

The proposed filterless Class-D amplifier with PRCFM is designed and fabricated using CSM 0.18-μm CMOS process. To access the effectiveness of the PRCFM for EMI reduction, an enable control is added to the design to enable or disable the PRCFM function.

The conducted EMI measurement setup is shown in Fig. 7, in accordance with CISPR 22 [25]. The Class-D amplifier is powered by a dc source through the line impedance stabilization network (LISN) and the conducted emissions from the Class-D amplifier are measured from the RF output of the LISN using the Advantest R3261 C spectrum analyzer with R3551 preselector. Fig. 8 shows the measured conducted emissions from 150 kHz to 30 MHz. Without the PRCFM, conducted emissions at the carrier frequency of 215 kHz and its harmonics are clearly observed. With the PRCFM, the conducted emissions at the carrier and its harmonics are well spread with a spectrum range of 24 kHz, which is about 10% of the nominal carrier frequency (215 kHz). By comparing the measurement results with and without PRCFM, it is obvious that conducted emissions

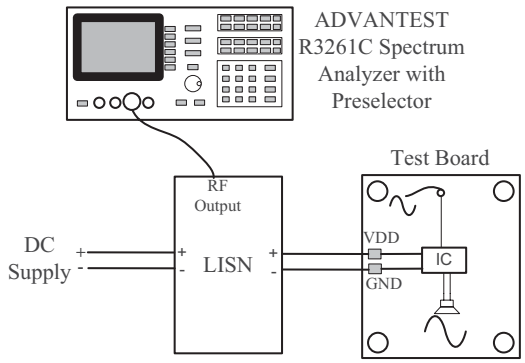

Fig. 7. Setup for conducted emission measurement.

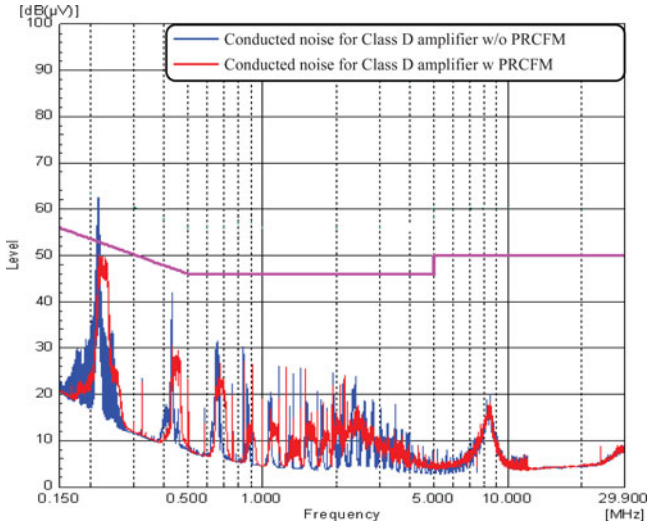

Fig. 8. Conducted emission with and without PRCFM.

with PRCFM are lower than those without PRCFM. Without PRCFM, the fundamental component has exceeded the CISPR 22 Class-B limit and several harmonics at the lower frequency end are very close to the limit. With PRCFM, the emissions are well below the limit with very comfortable margin. The reduction of the emission of the fundamental component is about 15 dB, which matches the theoretical expectation ($6.02\times3 = 18.06$ dB) rather well. The slight deviation is expected due to the switching loss. It is worth noting that further EMI reduction can be achieved by using more frequency hopping steps, if needed.

The measurement setup for near-field radiated emission is shown in Fig. 9. The near-field emission measurement is conducted using a Dectetus AB EM scanner system and measured with a Langer EMV-technik magnetic near-field probe. The probe is connected to a HP 8563E spectrum analyzer through a preamplifier (PA303). The measurement is split into two frequency bands, 150 kHz to 30 MHz and 30 MHz to 1 GHz with 9 and 120 kHz bandwidths, respectively. Fig. 10 shows the near-field emissions emitted from the test chip with and without the PRCFM, in the frequency band 150 kHz to 30 MHz. From the measurement result shown in the figure, it is noted that the near-field radiated emission at the fundamental frequency is reduced

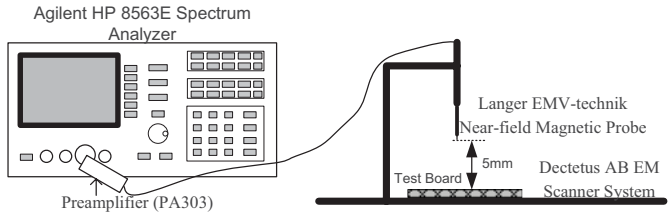

Fig. 9. Setup for near-field radiated emission measurement.

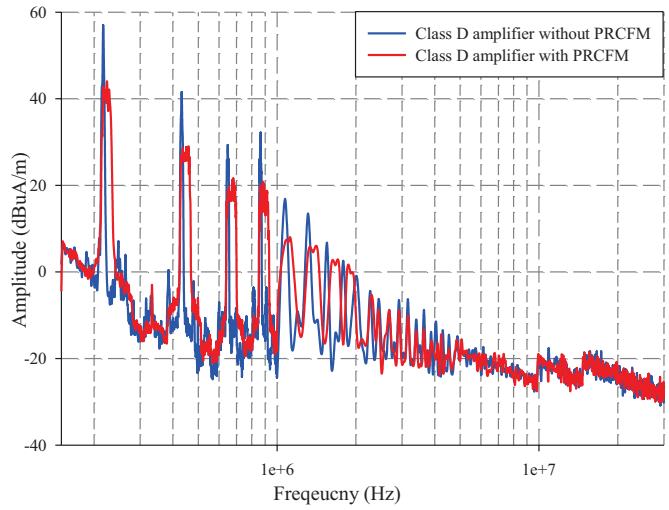

Fig. 10. Signal spectrum 150 kHz to 30 MHz of near-field radiated emission for both amplifiers.

by nearly 15 dB, which is consistent with the theoretical estimation. The measurement results also indicate that PRCFM is effective to reduce the near-field EMI coupling to other circuits that placed very close to the Class-D amplifier, which is an added merit in view of the continuing trend of product miniaturization. Fig. 11 shows the measured near-field radiated emissions of the Class-D amplifier without and with PRCFM for 30 MHz to 1 GHz range. As the near-field emissions above 30 MHz decay significantly, it is difficult to detect the difference in emissions with and without PRCFM.

Fig. 12 shows the THD performance comparison over the input modulation index range (0.4–95%) for 1 kHz input sinusoidal signal. The THD performance with the PRCFM is comparable to that without the PRCFM. With the proposed PRCFM, the measured THD results are below 0.07%. In general, all the THD performances are degraded when the modulation index is decreased. This is caused by the lower switching frequency when the modulation index of the input signal is small. Fig. 13 summarizes the measured THD performance in the audio band (100 Hz to 6 kHz) at 0.81 modulation index. Note that all the THD results are well below 0.09%. It also shows that the THD performance degrades when the frequency of the input signal is increased. As a summary, both figures have demonstrated that the proposed PRCFM does not degrade the THD performance of the Class-D amplifier and is suitable for mobile applications.

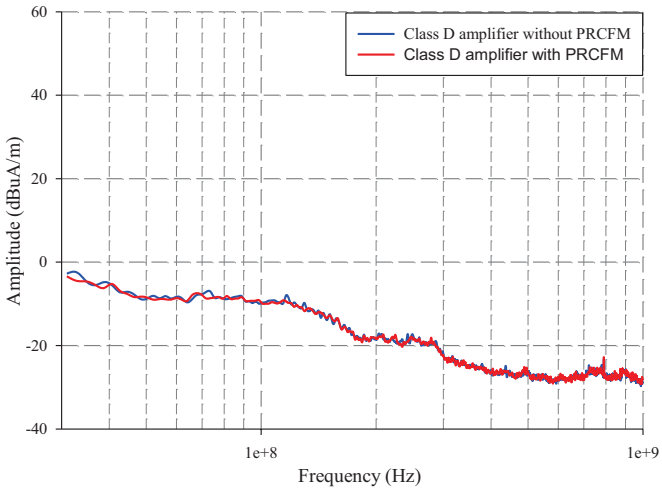

Fig. 11. Signal spectrum 30 MHz to 1 GHz of near-field radiated emission for both amplifiers.

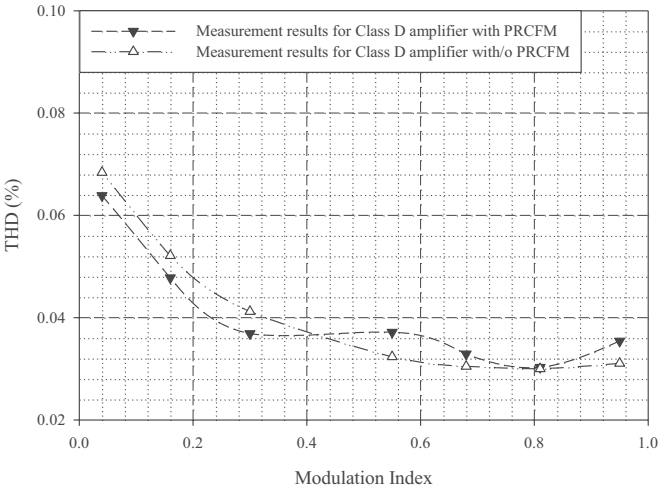

Fig. 12. THD performance over full input modulation index range with an input signal frequency of 1 kHz.

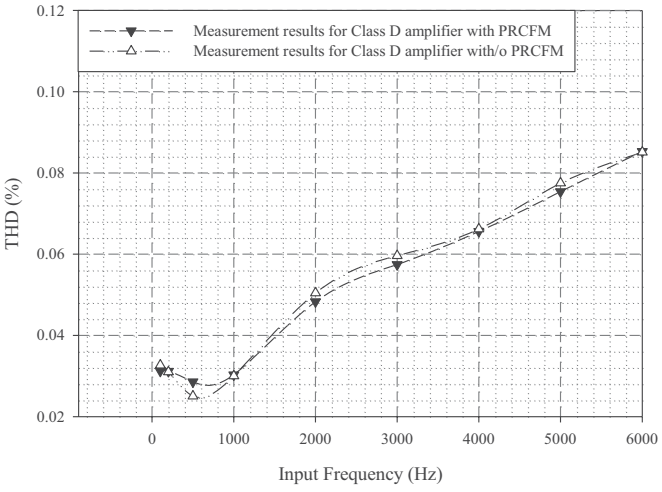

Fig. 13. THD performance over different input frequencies with an input modulation index of 0.81.

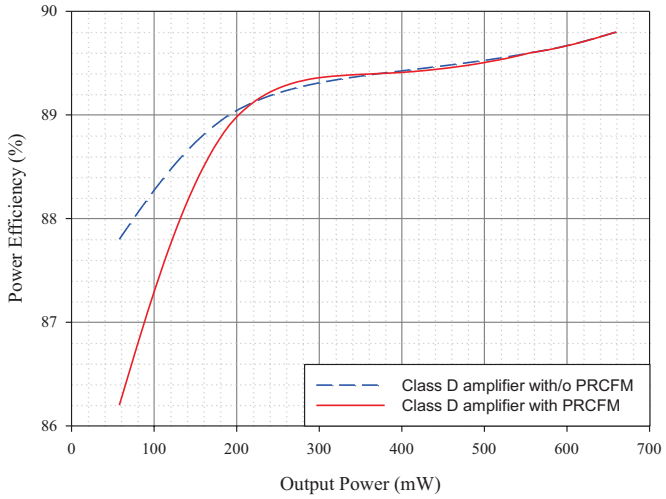

Fig. 14. Power efficiency over wide output power range.

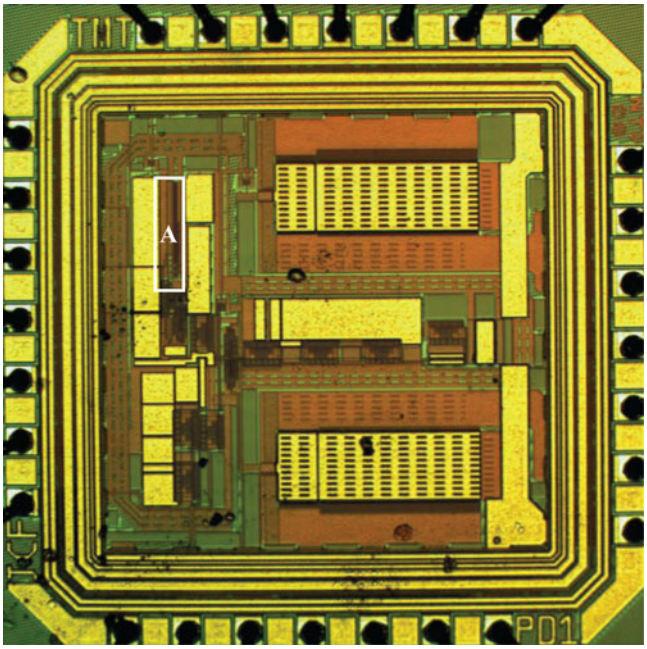

Fig. 15. Microphotograph of the proposed Class-D amplifier.

Fig. 14 shows the power efficiency of the amplifier with and without the PRCFM over a wide output power range. The efficiency performance is obtained with 1 kHz sinusoidal input waveform. The power efficiency with the PRCFM at lower output power range is slightly lower than that without the PRCFM. It is expected because of the additional power consumption by the PRCFM. However, as the output power increases, the power consumption of the PRCFM becomes negligible. Nevertheless, the worst case efficiency is still higher than 86% even for low output power (at about 58 mW).

Fig. 15 depicts the microphotograph of the integrated filterless Class-D amplifier designed using CSM 0.18-μm CMOS process. The chip occupies an area of 1 mm^2. The PRCFM circuit is located at block A and occupies less than 1% of the total chip area. Table I summarizes the performances comparison of

TABLE I
PERFORMANCE COMPARISON

	[10]	[12]	This work
Process	HHNEC 0.6 µm Bi-CMOS	CMSC 0.5 µm CMOS	CSM 0.18 µm
Die size (mm^2)	1.45*1.57	1.5*1.5	1 * 1
SSM circuit size (µm^2)	300*171	191*251	48 * 219
Topology	BD	BD	BD
LFSR stage	20	17	5
No. of PR bits	6	8	3
Load (Ω)	8	8	8
Power Supply (v)	2.5-5.5	2.4-5.5	3.3
Switch frequency (kHz)	1110	300	80 - 270
Frequency variation (%)	± 20	± 20	± 10
Best THD (%)	0.06 @ 0.1W	0.03 @ 0.1W	0.02 @ 0.5W
Output power (W)	0-4	0 - 2	0.05 - 0.7
Power efficiency (%) (0.05W – 0.7W)	Not given	80 - 90	86 - 90

the proposed filterless Class-D amplifier and the recently reported designs. As shown, the proposed design which embodies a 5-bit LFSR has achieved comparable performance in THD and power efficiency with significant size reduction (more than 50% size reduction in die size and about 80% reduction in SSM circuit size).

IV. CONCLUSION

A high-efficiency filterless Class-D amplifier with the PRCFM has been proposed and realized using CSM 0.18-μm CMOS process. The EMI-mitigation PRCFM circuit is area-efficient and occupies less than 1% of total chip size. The measurement results have demonstrated that the proposed PRCFM in the filterless Class-D amplifier is effective in reducing both the conducted and near-field radiated EMI below 30 MHz without significantly affecting the THD and power efficiency performances. It also shows that the noise floor in the audio band due to PR code generation frequency can be significantly reduced by increasing the frequency hopping period.

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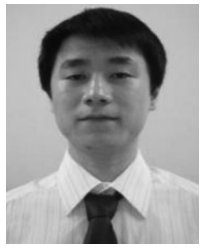

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