

Linear circuit applications of operational amplifiers

Operational amplifiers are based on the principle of using dc amplifiers employing feedback in order to control response characteristics for the purpose of performing various mathematical operations

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Some of the most frequently encountered linear circuit applications of operational amplifiers are discussed in this article. Included are details of differential dc amplifiers, bridge amplifiers, analog integrators, differentiators, line-driving amplifiers, ac coupled feedback amplifiers, current-to-voltage converters, reference-voltage sources, voltage regulators, current amplifiers, and charge amplifiers.

Differential dc amplifiers

The amplifiers to be discussed in this section are most descriptively known as differential dc amplifiers, denoting the fact that they amplify the difference between two signals, and that the inputs are directly coupled. Other common terms used for this basic type of amplifier are: transducer amplifier, bridge amplifier, data amplifier, instrumentation amplifier, difference amplifier, and error amplifier. Such amplifiers are easily realized through the use of one or more operational amplifiers with linear feedback. The idealized characteristics include infinite input impedance, zero output impedance, no dc offsets or drift, zero amplifier noise, a constant gain factor with no gain error, and complete rejection of signals common to both inputs (infinite common-mode rejection). Inputs are typically from transducers, which convert a physical

parameter and its variations to electric signals. Examples of such transducers include thermocouples and strain-gage bridges. Several types of such differential dc amplifiers, of varying complexity and performance characteristics, are discussed in the following paragraphs.

Differential dc amplifiers using one operational amplifier.¹⁻³ The circuit of Fig. 1(A) has the virtue of simplicity, in that it uses only one operational amplifier and four matched resistors. The presence of a common-mode voltage e_{cm} and a differential voltage ($e_1 - e_2$) is characteristic of most transducers. The common-mode voltage may represent a dc level, as in a bridge, or noise pickup. If an ideal operational amplifier is assumed, the following equations apply:

$$e_3 = (e_{cm} + e_2) \left(\frac{R_4}{R_3 + R_4} \right)$$
$$\frac{e_{cm} + e_1 - e_3}{R_1} = \frac{e_3 - e_2}{R_2}$$
$$e_\epsilon \approx 0$$

where e_ϵ is the amplifier input voltage.

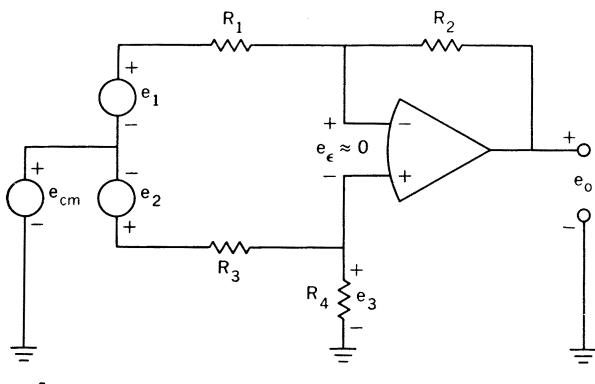
Combining the first two of these equations gives the resulting equation for output voltage:

$$e_o = e_{cm} \left[\frac{R_4 R_2 + R_4 R_1 - R_2 R_3 - R_2 R_4}{R_1 (R_3 + R_4)} \right] - \frac{R_2}{R_1} e_1$$
$$+ \left(\frac{R_4}{R_3} \right) \frac{1 + (R_2/R_1)}{1 + (R_4/R_3)} e_2$$

If $R_2/R_1 = R_4/R_3$, the foregoing equation reduces to

$$e_o = \frac{R_2}{R_1} (e_2 - e_1)$$

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A

B

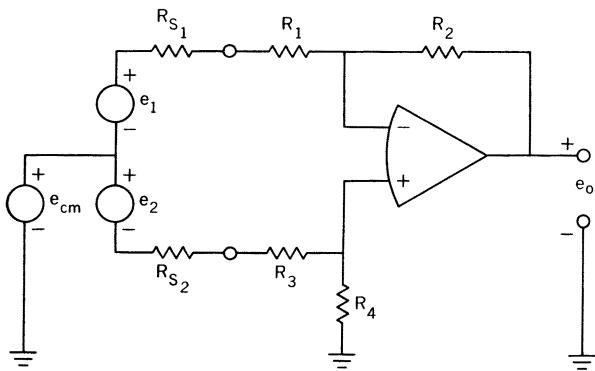
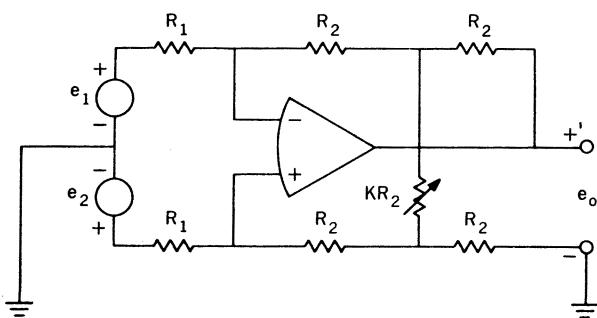


FIGURE 1. Simple differential amplifier. A—Zero source impedance. B—Unbalanced source impedance.

FIGURE 2. Simple, adjustable-gain differential amplifier.



The resistor ratios, R_2/R_1 and R_4/R_3 , must be carefully matched in order to insure the rejection of common-mode signals. The value of these resistor ratios sets the gain for differential signals. These equations illustrate the performance of the circuit when dealing with zero source impedances and nonzero common-mode signals. For zero source impedance the gain is determined solely by the feedback resistors and, if these resistors are matched in pairs as indicated, common-mode signals are rejected completely. Actually, of course, the operational amplifier has been assumed ideal in having infinite input impedance, infinite gain, and infinite common-mode rejection. If these factors are given real values and their effects evaluated, it will be found that the finite input impedance of the operational amplifier and its inherent finite common-mode rejection will place limits on the overall

common-mode rejection of the closed-loop differential amplifier. The finite open-loop gain will limit the gain accuracy of the overall circuit.

Figure 1(B) illustrates a model for unbalanced source impedances and their interactions with the finite resistances of the amplifier feedback network. An analysis similar to that for the circuit of Fig. 1(A) yields

$$e_o = e_{cm} \left[\frac{R_2(R_{S_1} - R_{S_2})}{(R_1 + R_{S_1})(R_3 + R_{S_2} + R_4)} \right] + \left(\frac{R_2}{R_1 + R_{S_1}} \right) \left[\frac{1 + (R_1 + R_{S_1})/R_2}{1 + (R_3 + R_{S_2})/R_4} e_2 - e_1 \right]$$

Note that if the source impedances are nonzero but equal, the only effect is a gain error due to the source loading. However, if the source impedances are also unequal, the common-mode rejection is degraded.

Input bias currents (I_{B1}, I_{B2}) and input voltage offset (V_{os}) of the operation amplifier will cause dc offset errors at the output of the differential amplifier circuit. Bias current (I_{B2}) from the noninverting side of the operational amplifier flows through the parallel combination of R_4 and R_3 to create a dc error voltage at the noninverting input terminal. This dc voltage effectively adds to the offset voltage of the operational amplifier and is amplified by the factor, $(R_2 + R_1)/R_1$. Bias current (I_{B1}) from the inverting input of the operational amplifier flows principally through resistor R_2 and causes an output offset adding to the other two components to give the total dc offset error of

$$E_{os} = V_{os} \left(\frac{R_2 + R_1}{R_1} \right) + I_{B1} \left(\frac{R_3 R_4}{R_3 + R_4} \right) \left(\frac{R_2 + R_1}{R_1} \right) - I_{B2} R_2$$

Tracking between the two bias currents reduces the bias current induced error term by as much as a factor of 10.

The principal limitations of this circuit are its low input impedance and the difficulty of varying the gain. The input impedance, of course, is determined by the feedback and input resistors. If these resistors are made large in order to increase the input impedance, the dc errors due to bias currents will be proportionately increased, thus placing an upper limit on the feasible values of input impedance. The gain of the differential amplifier can be changed only by varying the ratios of the feedback resistors. Because of the necessity for maintaining the equality of the resistive ratios, it is quite difficult to vary the gain continuously. Gain steps can be achieved if the common-mode rejection is carefully adjusted at each gain setting.

The differential amplifier circuit of Fig. 2 is a similar type of circuit, with the added feature of a gain vernier that allows the gain to be continuously varied without affecting the common-mode rejection of the circuit. The output voltage is

$$e_o = 2 \left(1 + \frac{1}{K} \right) \frac{R_2}{R_1} (e_2 - e_1)$$

Note, however, that this circuit requires four matched resistors of value R_2 and two matched resistors of value R_1 . The gain is an inverse function of the setting of the vernier potentiometer and, as such, is highly nonlinear. The potentiometer can, however, provide approximate

linearity over limited ranges. The circuit still suffers from the limitations of low input impedance. The dc offset errors are much the same as those for the circuit of Fig. 1.

Differential dc amplifiers using more than one operational amplifier.^{1,3} The circuit of Fig. 3 provides another low-impedance alternative to those of Figs. 1 and 2. The two amplifiers required operate in the inverting mode and need not have a noninverting capability. Thus they can be chopper-stabilized amplifiers for low drift or may be field-effect transistor (FET) input types, which may have rather poor linearity when used noninverting. The output voltage is

$$e_o = \frac{R_2}{R_1} (e_2 - e_1)$$

The gain can be easily varied, in steps or continuously, by changing the value of R_2 , without affecting the common-mode rejection properties. Good common-mode rejection requires four closely matched resistors of value R_1 . Note that the dc offset error is approximately four times that of a single amplifier, if it is assumed that offset errors add, as given by the expression

$$\begin{aligned} E_{os} &= \left(1 + 2 \frac{R_2}{R_1}\right) V_{os2} + 2 \frac{R_2}{R_1} V_{os1} \\ &= \left(2 + 4 \frac{R_2}{R_1}\right) V_{os} \text{ (worst case)} \end{aligned}$$

Since the common-mode rejection of the operational amplifiers is not a factor, the common-mode rejection of the closed-loop amplifier can be trimmed to quite high values by simply allowing a small amount of adjustability of one of the R_1 resistors. The common-mode voltage capability of the circuit is limited only by the output voltage capability of the unity gain inverter. This capability can be increased by making the gain of amplifier 1 less than unity. The gain of amplifier 2 must then be increased accordingly, however, thereby increasing the output offset error.

Another differential dc amplifier circuit using two operational amplifiers is shown in Fig. 4. This circuit provides the high input impedance lacking in the circuits discussed up to now. For this circuit,

$$e_o = \left(1 + \frac{R_4}{R_3}\right) (e_2 - e_1) \quad \text{if } \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

Again, equality of the two resistor ratios is required if the circuit is to reject common-mode signals. The operational amplifiers, since they operate in the noninverting mode, must have good common-mode properties. The input impedance at each terminal of the differential amplifier is simply the common-mode input impedance of the operational amplifiers. This can be quite large ($10 \text{ M}\Omega$ and up) depending on the type of operational amplifier used. For fixed gains, or gain steps, the circuit is quite useful, but it is not feasible for continuously variable gain. Also, since the input voltage of the upper amplifier must be less than $R_1/(R_1 + R_2)$ times the output saturation voltage, the common-mode voltage range is very limited at low values of overall gain. This is not considered a serious limitation, since such amplifiers are usually used at gains of 10 or greater.

The differential dc amplifier circuit of Fig. 5 overcomes most of the weaknesses of the circuits discussed up to this

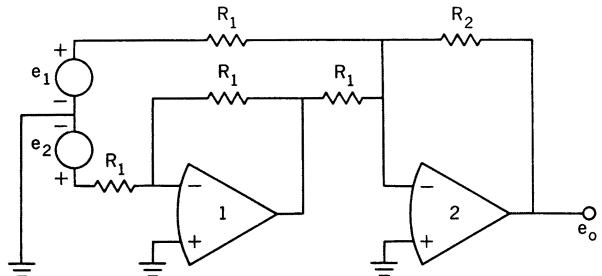


FIGURE 3. Differential dc amplifier using inverting operational amplifiers.

FIGURE 4. High-input-impedance differential amplifier.

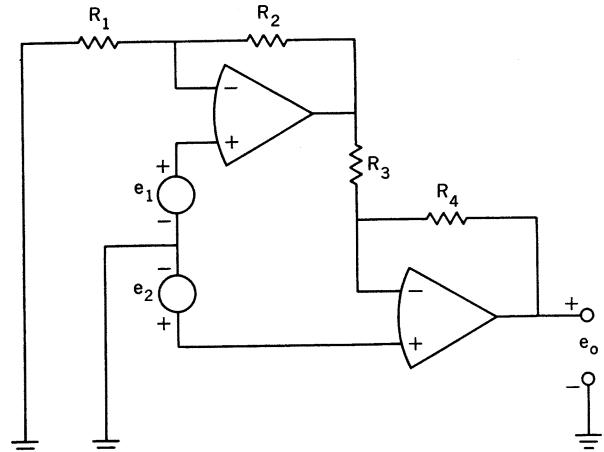
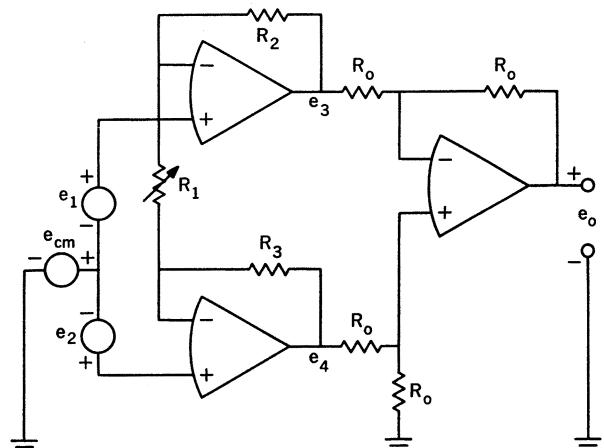


FIGURE 5. High-input-impedance adjustable-gain differential amplifier.



point. Analysis of the circuit yields the following equations:

$$e_3 = \left(1 + \frac{R_2}{R_1}\right) e_1 - \frac{R_2}{R_1} e_2 + e_{cm}$$

$$e_4 = \left(1 + \frac{R_3}{R_1}\right) e_2 - \frac{R_3}{R_1} e_1 + e_{cm}$$

$$e_o = e_4 - e_3$$

If $R_2 = R_3$, then the output voltage is

$$e_o = \left(1 + \frac{2R_2}{R_1}\right)(e_2 - e_1)$$

The two input amplifiers constitute a differential buffer amplifier with a gain of $1 + (2R_2/R_1)$ for differential signals, and unity gain for common-mode signals. The non-inverting configuration of these input amplifiers insures high input impedance at both inputs. The gain is easily varied by a single resistor R_1 . The effect of mismatch in resistors R_2 and R_3 is simply to create a gain error without affecting the common-mode rejection of the circuit. The resistors R_o of the output amplifier must be accurately matched, or trimmed, to insure the rejection of common-mode signals at this point. This final amplifier acts simply as a differential-input/single-ended-output converter. Feedback impedances in both stages can be relatively low in value to minimize the effects of bias current, since these feedback elements do not affect the input impedance of the differential amplifier. Usually, all of the gain of this differential amplifier is in the input stage, thus insuring that only the offset voltages of these two operational amplifiers are significant in determining the output offset. Since the output voltage offset is proportional to the difference of the voltage offsets of these two amplifiers, it is desirable to use amplifiers whose voltage offsets tend to track with temperature. Such techniques are the basis for some low-drift differential-amplifier modules. The bias currents of these input amplifiers will flow through the impedance of the source, and will thus generate additional offset voltage, which will appear at the output of the differential amplifier amplified by the differential gain factor. The use of amplifiers with FET input stages will greatly reduce this effect.

Bridge amplifiers¹

Probably the most common use for a differential dc amplifier is in amplifying the output signal from a transducer bridge, such as a strain gage. The most straightforward way of doing this is with one of the high-impedance amplifiers discussed in the previous section. Such a strain-gage bridge, with one active bridge arm, is shown in Fig. 6. The following equations describe its operation:

$$e_2 = V \frac{R}{2R + \Delta R} \quad e_1 = \frac{V}{2}$$

$$e_2 - e_1 = -\left(\frac{V}{4}\right) \frac{\delta}{1 + (\delta/2)}$$

where $\delta = \Delta R/R$. Then

$$e_o = K(e_2 - e_1) = -\left(\frac{KV}{4}\right) \frac{\delta}{1 + (\delta/2)}$$

$$\text{or} \quad e_o \approx -KV \frac{\delta}{4} \quad \text{if } \delta \ll 1$$

The output signal is a linear function of the variation of the active element only for small percentage changes in the element. If larger changes are to be measured, the exact equation must be used and a conversion or linearization must be performed at some point in the data-gathering process.

It is sometimes desirable to use an amplifier less complex than the fully developed differential instrumentation amplifier for amplifying the output signal from a bridge.

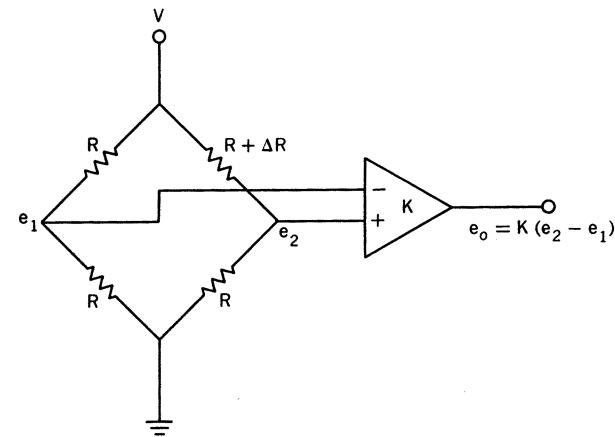
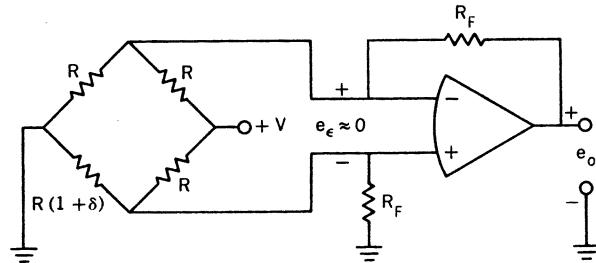


FIGURE 6. Bridge amplifier.

FIGURE 7. Bridge-type current amplifier.



There are several such circuits that use only a single operational amplifier, such as the one shown in Fig. 7. This circuit forces the differential output voltage of the bridge to be zero, since opposite sides are connected directly to the inputs of an operational amplifier with feedback. Thus the amplifier is used to measure the current flowing into the bridge under short-circuit conditions. The resulting output voltage is

$$e_o = \frac{R_F}{R} \left(\frac{\delta}{1 + \delta} \right) \frac{V}{\left(\frac{2 + \delta}{1 + \delta} + \frac{R}{R_F} \right)}$$

If $\delta \ll 1$ and $R_F \gg R$, this equation reduces to the approximate form

$$e_o \approx V \left(\frac{\delta}{2} \right) \frac{R_F}{R}$$

Note that here again the equation for the output voltage of the bridge amplifier is a nonlinear function of the variation of the active bridge element, but for small deviations the nonlinearity is negligible. For the simplified, approximate form of the equation, it has also been assumed that the values of resistance in the bridge are much smaller than the resistors R_F . The bridge resistance appears in the gain equation, thus requiring that the values of the bridge elements be insensitive to temperature in order that the gain of the amplifier be stable with temperature. If the assumption that R_F is much greater than the nominal bridge resistance applies, there is no loading effect.

The dc offset voltage generated at the output of the bridge amplifier as a result of the input offset voltage

and bias currents of the operational amplifier is given by

$$E_{OS} = V_{OS} \left(\frac{2R_F + R}{R} \right) + (I_{B2} - I_{B1})R_F$$

where I_{B1} and I_{B2} are input bias currents. The main advantage of this circuit is its simplicity. It does require an amplifier with reasonably good common-mode rejection.

Where the rejection of common-mode noise signals is not a problem, the half-bridge measuring circuit of Fig. 8 is sometimes used. Here, also, the output of the bridge is connected directly to the input terminal of the operational amplifier as is the feedback through R_F . Since the other input of the operational amplifier is held at ground potential, the output of the half-bridge is held at zero voltage, and the amplifier responds to the short-circuit output current

$$e_o = -iR_F = -V \frac{R_F}{R} \left(\frac{\delta}{1 + \delta} \right)$$

If $\delta \ll 1$,

$$e_o \approx -V \left(\frac{R_F}{R} \right) \delta$$

Because the amplifier does operate single-ended, the amplifier used can be chopper-stabilized for lowest possible drift and dc offset errors. Also, the maximum voltage supplied to the bridge, or half-bridge, is not limited by common-mode voltage limitations of the operational amplifier, as it is in those circuits that use the noninverting input of the operational amplifier. Thus, it is possible to increase the sensitivity of the bridge by increasing the supply voltage within the limitations of the bridge elements and the ability of the amplifier to supply the current flowing through the feedback resistor.

The major drawback of the half-bridge circuit is its inability to reject noise pickup, as is normally accomplished by the differential type of bridge amplifier. Consequently, the noise and ripple of the half-bridge supply must be very low and all wiring must be kept short and well-shielded. As in the previous bridge amplifier, the gain is a function of the bridge elements. This can be a serious drawback if the bridge elements are sensitive to environmental factors other than the one that it is desired to measure. The output dc offset voltage of the half-bridge amplifier is given by the expression

$$E_{OS} = V_{OS} \left(1 + \frac{2R_F}{R} \right) - I_{B1}R_F$$

where I_{B1} is the input bias current.

Figure 9 illustrates another bridge amplifier using a single operational amplifier in the inverting mode. Thus it is once again possible to use a single-ended chopper-stabilized amplifier with its attendant low drift. The amplifier output voltage is

$$e_o = V \left(1 + \frac{R_F}{R_1} \right) \frac{\delta}{4[1 + (\delta/2)]}$$

which, for $\delta \ll 1$, reduces to

$$e_o \approx V \left(1 + \frac{R_F}{R_1} \right) \frac{\delta}{4}$$

Another advantage of this circuit, not shared by the preceding two, is that the gain is not dependent upon the

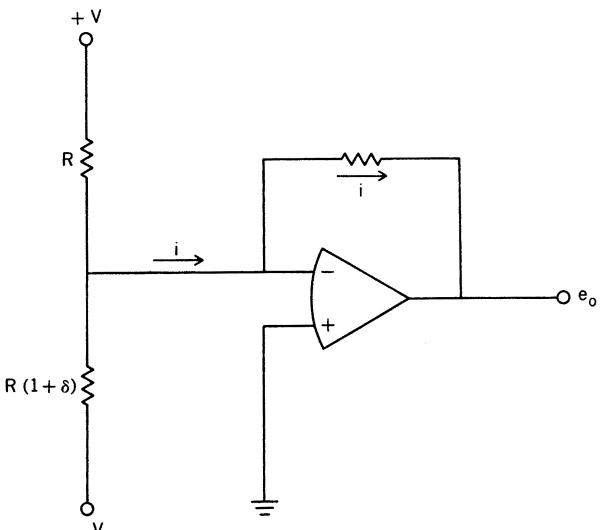
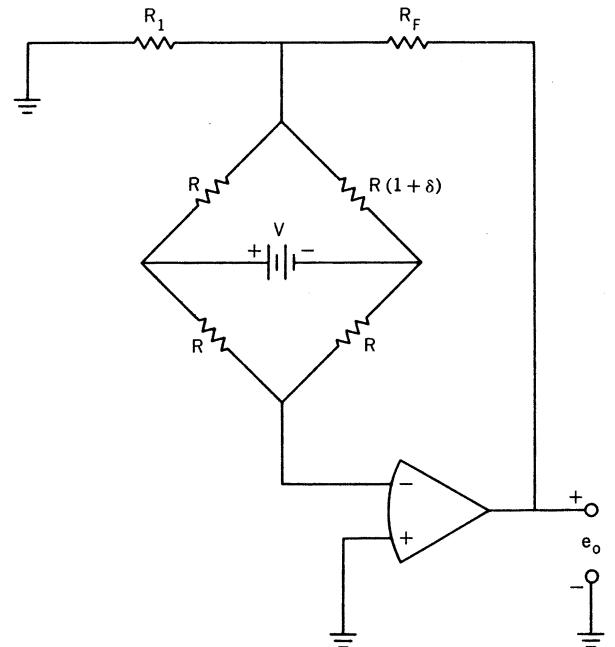


FIGURE 8. Half-bridge current amplifier.

FIGURE 9. Inverting bridge amplifier.



absolute value of the bridge resistors. The output voltage is proportional to the open-circuit voltage of the bridge since the input to the amplifier draws negligible signal current. The inverting input of the operational amplifier is maintained at virtual ground by the high open-loop gain. Since the gain is a function of R_F and R_1 , it can be varied easily with either resistor. A small-valued potentiometer can be added in series with either resistor for calibration purposes. This type of bridge amplifier, which can be very accurate, is recommended when it is necessary to detect very small bridge signals. The primary disadvantage is that a floating bridge supply is required. Since it uses a single-ended amplifier it does not have the common-mode-rejection capabilities of the true differential amplifier. However, careful shielding and filtering to remove noise can help to eliminate this prob-

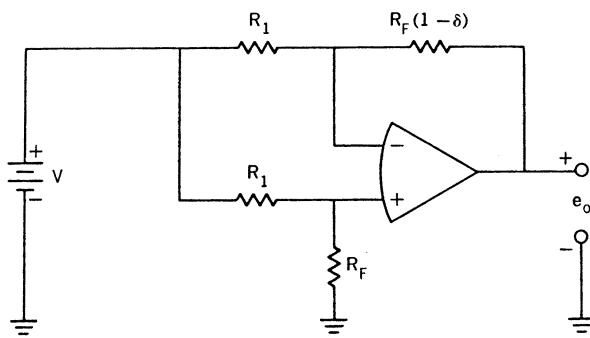


FIGURE 10. Wide-deviation bridge amplifier.

FIGURE 11. Analog integrator.

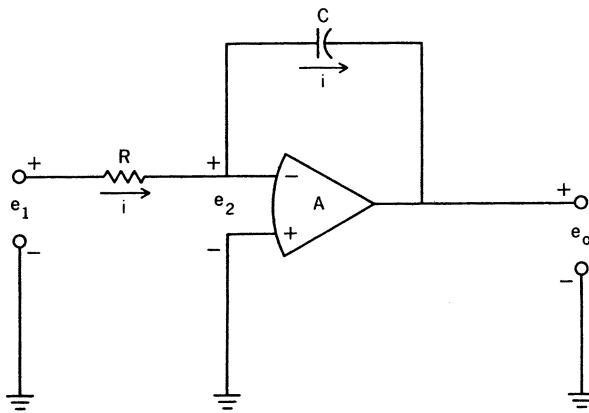
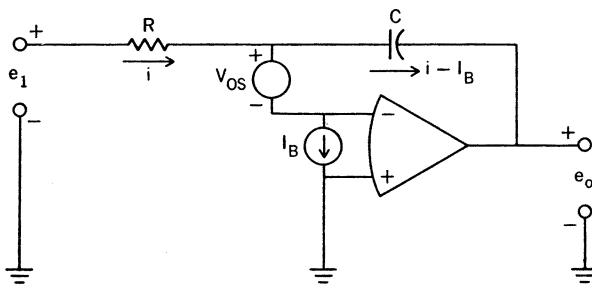


FIGURE 12. Effects of offset voltage and bias current in integrator circuit.



lem. The output offset voltage as a function of input offset voltage and bias currents is similar to that of the inverting amplifier circuit; that is,

$$E_{OS} = \frac{R_F + R_1}{R_1} (V_{OS} - I_{B1}R) - I_{B1}R_f$$

The final bridge-amplifier circuit to be discussed is that given in Fig. 10, in which the output voltage is directly proportional to the transducer deviation even for large fractional changes in the active element; that is,

$$e_o = -V \left(\frac{\delta R_F}{R_1 + R_F} \right)$$

This particular circuit should be used whenever the deviation of the active element is large enough that the linear approximations made in the previous bridge equations are no longer valid. Examples are thermistors,

semiconductor strain gages having high gage factors, etc. The bridge elements must be so matched that the two input resistors are equal and the active element is equal to the value of R_F when the bridge is at null. Calibration is difficult since it requires the trimming of two values of resistance to maintain null while varying sensitivity.

Analog integrators⁴⁻⁶

The analog integrator is extremely useful in computing, signal-processing, and signal-generating applications. It uses an operational amplifier in the inverting configuration, as shown in Fig. 11. The equations of operation are derived assuming an ideal operational amplifier of gain A . These are

$$\frac{e_1 - e_2}{R} = i$$

$$e_2 - e_o = \frac{1}{C} \int_0^t i dt = \frac{1}{RC} \int_0^t (e_1 - e_2) dt$$

$$e_2 = -\frac{e_o}{A}$$

If $A \rightarrow \infty$, then $e_2 \rightarrow 0$, and

$$e_o = -\frac{1}{RC} \int e_1 dt$$

As in the inverting amplifier, the summing point is held at a virtual ground by the high gain of the amplifier and its feedback network. Since no current flows into the input terminal of the operational amplifier, all of the input current, $i = e_1/R_1$, is forced to flow into the feedback capacitor, causing a charge voltage to appear across this element. Because one end of the capacitor is tied to the virtual ground point, the output voltage of the amplifier equals the capacitor-charging voltage. The overall integrator circuit has the low output impedance normally associated with a feedback amplifier.

The dc offset and bias current of the analog integrator are taken into account in the more realistic model of Fig. 12. Because these dc errors exist, the output of the integrator now consists of two components: the integrated signal term and an error term

$$e_o = -\frac{1}{RC} \int e_1 dt + \frac{1}{RC} \int V_{OS} dt + \frac{1}{C} \int I_B dt + V_{OS}$$

The error term itself is made up of a component due to the input offset voltage and another due to the input bias current. The integral of the dc offset voltage results in a ramp voltage, a linearly increasing term whose polarity is determined by the polarity of the input offset voltage. In addition to this ramp-voltage error, the input offset voltage creates an output offset voltage equal to it in value. The bias current flows almost entirely through the feedback capacitor, charging it in ramp fashion, similar to the ramp voltage resulting from the input offset voltage. These two ramp-voltage errors will continue to increase until the amplifier reaches its saturation voltage or some limit set by external circuitry. These error components usually set the upper limit on feasible length of integration time. The error component caused by bias current can be minimized by increasing the capacitance of the feedback element. This can be done only by de-

creasing the value of the input resistor, if a specific value of the RC time constant is to be achieved. A lower limit usually exists on R because of current limitations and loading of the input signal source.

The effects of bias current can be reduced by inserting a resistance R between the noninverting input of the amplifier and ground. This equalizes the resistances at the two inputs and changes the effects of bias current to that of offset (difference) current. Thus, in the equation for output voltage, the bias current I_B should be replaced by the offset current I_{OS} if the compensating resistor is used. The error ramp due to voltage offset is fixed by the chosen value of RC time constant.

To realize the performance possibilities of an operational amplifier as an integrator, a feedback capacitor must be selected with a dielectric leakage current that is less than the bias current of the amplifier. Polystyrene and Teflon are usually the best choices for the ultimate in long-term integrating accuracy. If shorter integration times are required, the requirements on capacitor quality can accordingly be relaxed. Mylar capacitors may then prove satisfactory, as will silver-mica types if small values of capacitance, corresponding to high-speed integration, are to be used.

The choice of the type of amplifier is also governed by the length of computing time and the desired accuracy. Chopper-stabilized amplifiers are usually used for long-term integrators because of their superior long-term dc stability. FET amplifiers are used for medium-length integration because of their low bias current. Amplifiers with bipolar transistor input stages may be used in very-short-term integration, such as in signal generation (sweep generation, triangle waves, etc.).

If the finite gain and bandwidth are taken into account, their effects on the integrator response function may be evaluated. The open-loop frequency response of the amplifier is approximated by a single pole located at $1/\tau_o$, and a low-frequency gain of A_o .

The resulting integrator response function is

$$\frac{E_o}{E_1}(s) \approx \frac{-A_o}{\left(\frac{\tau_o}{A_o}s + 1\right)(A_o RC s + 1)}$$

if $A_o \gg 1$ and $A_o RC \gg \tau_o$. This function has two poles on the real axis—as opposed to the ideal integrator function, which has a single pole at the origin. In Fig. 13 the frequency response of this approximate integrator is compared with the response of an ideal integrator, along with an open-loop frequency response of the operational amplifier. Note that the response of the real integrator departs from the ideal response only at the extremes of frequency. At low frequencies, the departure is attributable to the finite gain of the operational amplifier; at high frequencies, to the finite amplifier bandwidth.

The transient response of the integrator (Fig. 14) is studied by calculating the response to a step function. The response of an ideal integrator to a step function $-E/s$ would be a linear ramp voltage increasing to infinity. The step response of the practical integrator is a close approximation of this ramp throughout most of the signal range:

$$e_o(t) = A_o E \left[1 - \frac{e^{-t/A_o RC}}{1 - (\tau_o/A_o RC)} + \frac{e^{-t/\tau_o}}{(A_o RC/\tau_o) - 1} \right]$$

In order to compare the ideal and real responses it is necessary to examine the responses for very small and for very large times. For small values of time,

$$e_o(t) \approx E \left(\frac{t}{RC} + \frac{\tau_o}{RC} + \frac{e^{-t/\tau_o}}{RC/\tau_o} \right)$$

For large values of time the response is approximately

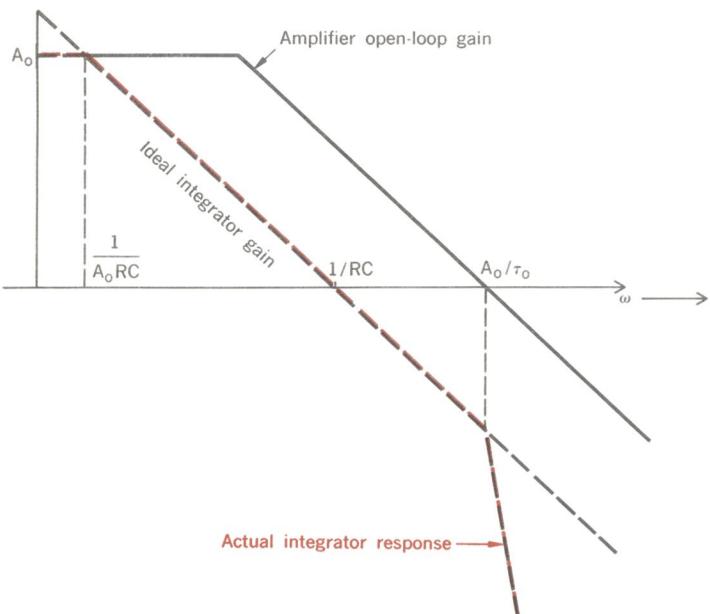
$$e_o(t) = A_o E (1 - e^{-t/A_o RC})$$

For small values of time the principal error effect is caused by the finite bandwidth, which causes a time-lag error in the actual response. For large values of time the output signal would approach an exponential with time constant $A_o RC$ and final value $A_o E$. For accurate computation, the integration should be terminated at time much less than $A_o RC$ and output amplitude much less than $A_o E$.

Figure 15 illustrates the switching techniques used to initiate and terminate the period of the integration. This integrator circuit has three modes. The first of these is RESET, in which the initial conditions are established by placing an initial charge on the capacitor. This is done by closing switch S_1 to allow the output voltage to rise to the negative of V_{IC} . If switch S_1 is then opened and S_2 is closed, the circuit begins integration of the input signal e_1 , beginning at the value $-V_{IC}$. This is the second or INTEGRATE mode. If both switches are held open, the output voltage will hold its latest value and will not respond to input or initial condition voltages. During this HOLD mode, the only discharge of the capacitor is that resulting from the bias current of the amplifier and dielectric leakage in the capacitor. Since electronic switch modules are commonly used for the mode-control function in place of the simple switches shown, any leakage current flowing from these switches must be added to the amplifier bias current in calculating the decay of the capacitor voltage during HOLD or during the INTEGRATE mode.

Although the analog integrator is a linear device, its maximum rate of change of output signal can lead to

FIGURE 13. Bode plots for amplifier and integrator. (Actual integrator response shown in color.)



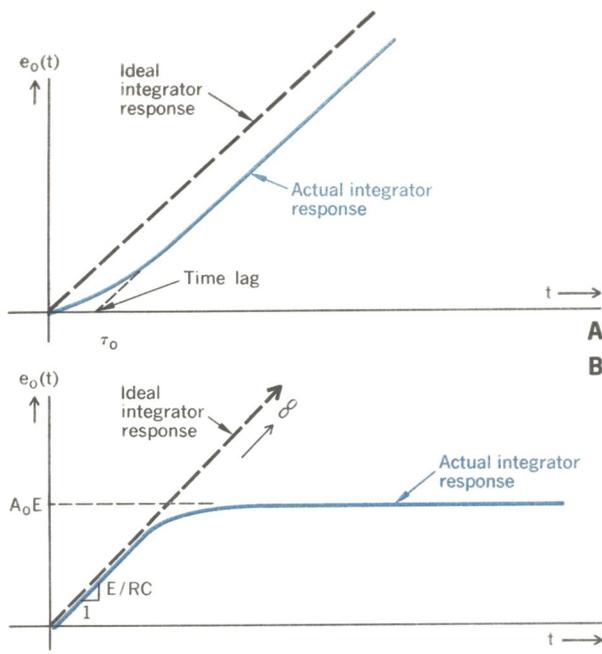


FIGURE 14. Integrator step-response curves A—For small values of time. B—For large values of time.

FIGURE 15. Three-mode integrator.

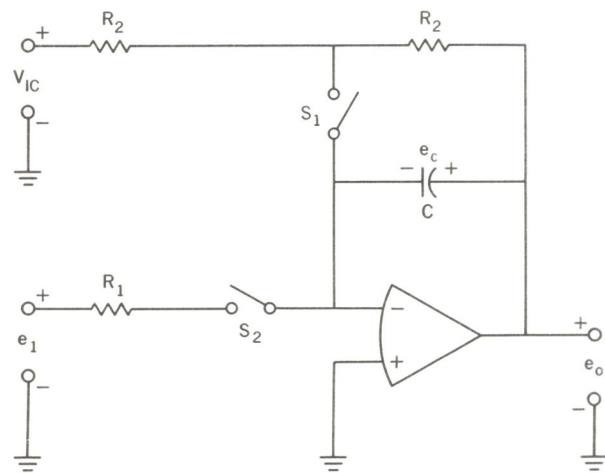
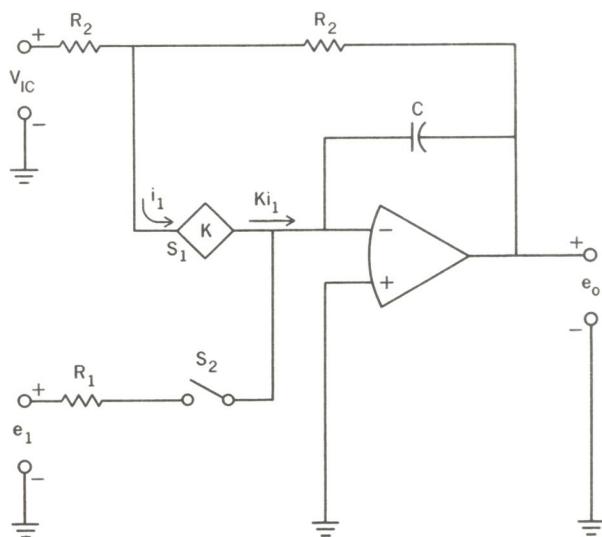


FIGURE 16. Current-amplifying switch used for reset of integrator circuit.



slew-rate distortion for signals of relatively high frequency and large amplitude. The inherent slew-rate limit of the operational amplifier places one of these limitations on the operation. However, another limitation, usually much more restrictive, is that placed on the rate of change of capacitor voltage by the output-current limits of the amplifier. The expression for this is

$$\left(\frac{de_c}{dt} \right)_{\max} = \left(\frac{de_o}{dt} \right)_{\max} = \frac{I_{\text{lim}}}{C}$$

where I_{lim} is the output-current limit.

The time required for the amplifier to reset to initial conditions is limited by the RC time constant of the RESET network and also by the slew rate achievable in the closed-loop circuit. If a reset switch that has a large current gain factor is used, the reset time can be considerably reduced. The use of such a switch is illustrated in Fig. 16, where the circuit is shown in the RESET state. Analysis of the circuit yields the equation for the output voltage,

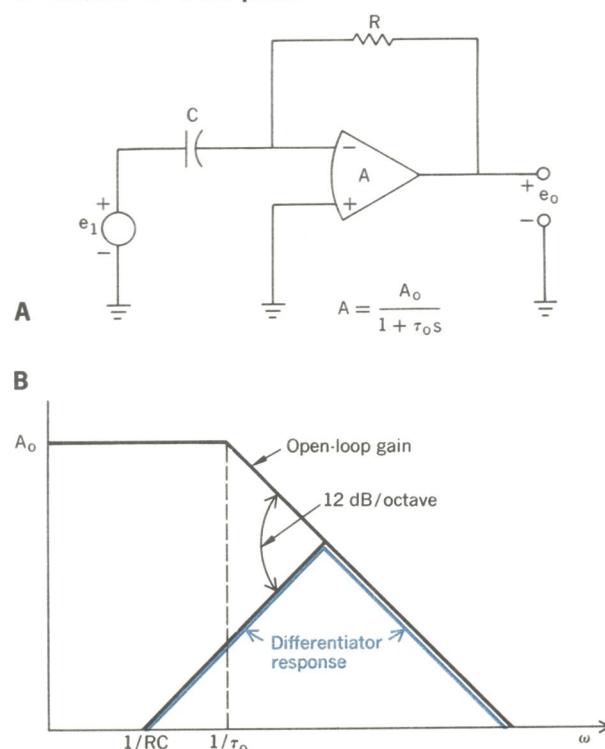
$$e_o = -e_i(1 - e^{-Kt/R_2C})$$

This is again the equation of an exponentially increasing voltage. Here, however, the time constant is R_2C/K , reduced by a factor equal to the current gain of the switch. The reset time can potentially be reduced by the factor K if the operational amplifier and switched current amplifier do not reach their current limits, thus limiting the slew rate. Maximum current is required at $t = 0$, the initiation of the RESET mode.

Differentiators^{1,2,7}

By interchanging the resistor and capacitor of an integrator circuit we obtain the inverse function, differentiation. However, as will be shown, the differentiator

FIGURE 17. Differentiator using operational amplifier. A—Circuit. B—Bode plots.



circuit, shown in Fig. 17(A), has some troublesome properties. If the usual single-pole open-loop gain function is assumed for the amplifier, the transfer function of the differentiator circuit may be reduced to

$$\frac{e_o}{e_i} = \frac{-RCs}{1 + \frac{1}{A_o}(\tau_o + RC)s + \frac{RC\tau_o}{A_o}s^2}$$

This transfer function has the form

$$H(s) = \frac{-H_0 s}{1 + \frac{\alpha}{\omega_n} s + \frac{s^2}{\omega_n^2}}$$

where

$$\omega_n^2 = \frac{A_o}{RC\tau_o}$$

$$\text{and } \alpha \text{ (damping factor)} = \sqrt{\frac{(\tau_o + RC)^2}{RC\tau_o}} \frac{1}{A_o} \ll 1$$

Thus the damping factor α is very small, indicating a lightly damped circuit response and complex poles near the $j\omega$ -axis. Such a response would also be indicated by the 12-dB/octave rate of closure of the Bode plots; see Fig. 17(B). Thus the differentiator circuit, as shown, has a tendency toward instability. If the amplifier open-loop gain has an attenuation rate of greater than 6 dB/octave over a portion of its Bode plot, the circuit may well oscillate. Another problem with this differentiator circuit is its high gain at high frequencies. This allows the high-frequency components of amplifier noise to be amplified even though the signal may not have high-frequency components. Thus the high-frequency output noise may obscure the differentiated signal.

The modified differentiator circuit of Fig. 18(A) is usually preferred as a means of eliminating the problems of the simpler circuit. Two additional real poles are introduced by use of R_1 and C_F . This creates a very stable system and reduces the high-frequency noise. The poles are placed sufficiently high in frequency to prevent significant phase-shift error in the signal-frequency range. The modified frequency response is shown in Fig. 18(B).

Line-driving amplifiers

One of the primary areas of application for the operational amplifier is that of buffering between a signal source and the desired load. Usually the signal source is very limited in power, has relatively high internal impedance, and is of a low level. The load is relatively low in impedance (possibly capacitive) and requires high-level signals. Thus the amplifier must provide impedance buffering, signal scaling, and power gain. Needless to say, it must be stable under the desired conditions of loading and feedback, and must have sufficient gain and bandwidth to insure accurate response to input signals. A typical example of such an application is the line-driving amplifier.

When data signals must be transmitted over long signal lines from a remote measuring station, the line-driving amplifier is usually required. Figure 19 illustrates a simulated load of this type. The capacitance is that of a shielded cable and may be as little as a few picofarads or as much as several microfarads. If the output impedance of the amplifier is considered, the equation for effective open-loop gain $A'(s)$ becomes

$$A'(s) = A(s) \frac{R_p}{R_p + R_o} \left(\frac{1}{1 + R_q C_L s} \right)$$

where

FIGURE 18. A—Modified differentiator with improved noise and stability. B—Modified frequency response.

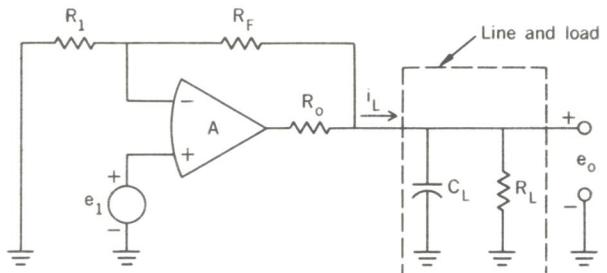
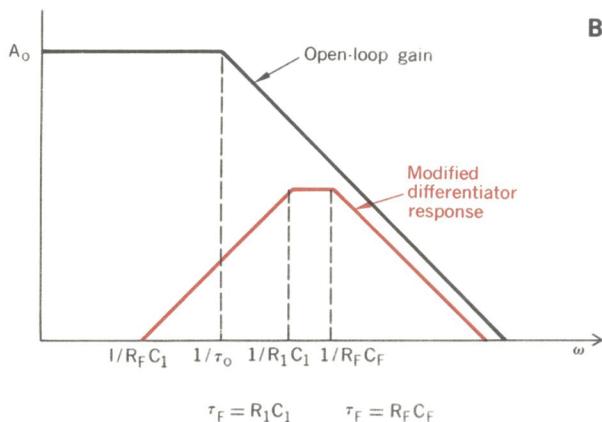
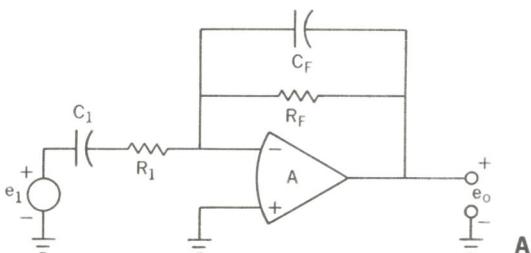
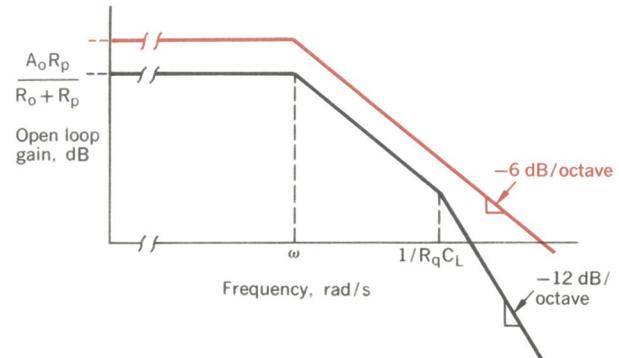


FIGURE 19. Line-driving amplifier.

FIGURE 20. Effect of loading on open-loop gain.



$$R_p = \frac{1}{\frac{1}{R_F} + \frac{1}{R_L}} \quad R_q = \frac{1}{\frac{1}{R_F} + \frac{1}{R_L} + \frac{1}{R_o}}$$

where $A(s)$ is the unloaded open-loop gain and R_o is the dynamic output impedance of the operational amplifier. If $A(s)$ is approximated by a single-pole transfer function,

$$A(s) = \frac{A_o}{1 + (s/\omega_o)}$$

then the effective (loaded) open-loop gain becomes

$$A'(s) = \frac{R_p}{R_p + R_o} \left[\frac{A_o}{1 + (s/\omega_o)} \right] \frac{1}{1 + R_q C_L s}$$

A Bode plot of this transfer function, for $s = j\omega$, is shown in Fig. 20, along with a plot of the unloaded open-loop gain. Note that the effect of the resistive loading is to reduce the open-loop gain, lowering the entire curve. Thus, resistive loading alone reduces the unity-gain bandwidth and will consequently reduce closed-loop bandwidth by the same factor. This bandwidth reduction factor is extremely important for fast line-drivers since the very low impedance of the line can severely degrade the bandwidth unless the operational amplifier has very low output impedance. The capacitive component of load impedance introduces another pole in the gain function at $s = -1/R_q C_L$. This causes an additional "break" in the frequency response and a rolloff of -12 dB/octave above the frequency $\omega = 1/R_q C_L$. If the closed-loop gain curve intersects this section of the effective open-loop gain curve, the amplifier will be marginally stable with unacceptable transient response.

There are a number of techniques for dealing with the problems of loading. The most satisfactory of these is to choose an amplifier with very low open-loop output impedance, or to create one by adding a power-booster stage to an available operational amplifier. This will reduce the gain and bandwidth loading factors caused by the load resistance and will increase the frequency at which the additional pole occurs. The higher in frequency this pole occurs, the more stable the closed-loop response will be. The power output stage also supplies the current necessary to meet the condition

$$(i_L)_{\max} = C_L \left(\frac{de_o}{dt} \right)_{\max}$$

As an example, the amplifier must be capable of supplying 63 mA to the capacitive load if $C_L = 10\,000 \text{ pF}$ and the output voltage is a 10-volt sine wave at 100 kHz.

AC-coupled feedback amplifiers^{1,2}

Although the operational amplifier is designed to amplify dc signals, it has a rather broad frequency response and is consequently quite useful for strictly ac signals. The feedback network can be tailored for exactly the desired passband. One of the simplest ac amplifiers is that shown in Fig. 21(A), where the closed-loop gain is given by

$$\frac{E_o}{E_1}(s) = -\left(\frac{R_F}{R_1}\right) \frac{s}{s + (1/R_1 C_1)}$$

The dc gain is zero, whereas the high-frequency gain approaches $-R_F/R_1$. The lower cutoff frequency is

$$f_c = \frac{1}{2\pi R_1 C_1}$$

The dc output offset voltage E_{os} is equal to the dc input offset voltage plus the dc offset voltage generated by the input bias current flowing through R_F .

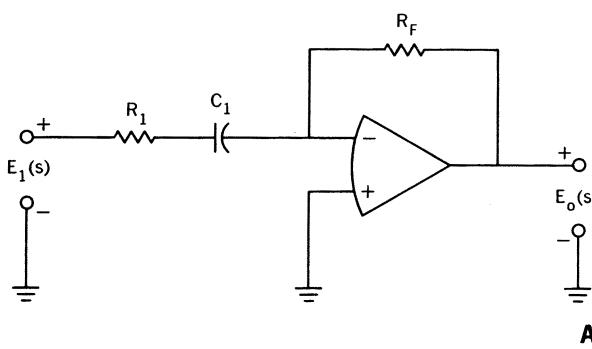
$$E_{os} = V_{os} \times 1.0 + I_{B1} R_F$$

A noninverting ac amplifier is shown in Fig. 21(B). The response is given by

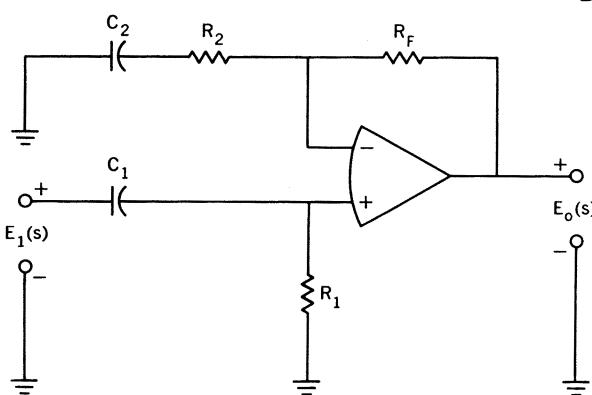
$$\frac{E_o}{E_1}(s) = \frac{s}{s + (1/R_1 C_1)} \left[\frac{(R_2 + R_F)C_2 s + 1}{R_2 C_2 s + 1} \right]$$

Both circuits of Fig. 21 have relatively low input impedance above the cutoff frequency, determined by the

FIGURE 21. Typical ac-coupled feedback amplifiers. A—Inverting circuit. B—Noninverting circuit.

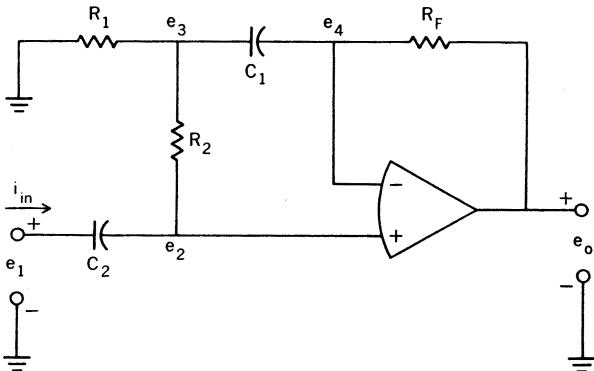


A



B

FIGURE 22. Bootstrapped ac amplifier.



resistors denoted R_1 in both cases.

The circuit of Fig. 22 is an ac amplifier whose input impedance is "bootstrapped" to a high value. Resistor R_2 provides a decoupling for dc input signals. However, for high-frequency signals the voltage across R_2 becomes very small. Consequently, very little current flows through R_2 , and the effective input impedance is very high.

The analysis of the circuit is greatly simplified if it is assumed that $e_2 = e_4$ as $A \rightarrow \infty$. Then we may write the equations

$$\frac{e_1 - e_2}{X_2} = \frac{e_2 - e_3}{R_2}$$

$$\frac{e_0 - e_2}{R_F} = \frac{e_2 - e_3}{X_1}$$

$$\frac{e_2 - e_3}{R_2} + \frac{e_2 - e_3}{X_1} = \frac{e_3}{R_1}$$

where $X_1 = \frac{1}{j\omega C_1}$ and $X_2 = \frac{1}{j\omega C_2}$

If these equations are solved for e_2 , the input impedance may be calculated from

$$Z_{in} = \frac{e_1}{i_{in}} = \frac{e_1 X_2}{e_1 - e_2}$$

which yields

$$Z_{in} = X_2 + R_2 + R_1 + \frac{R_1 R_2}{X_1}$$

As the frequency increases, X_1 and X_2 approach zero and the input impedance becomes very large. As frequency

increases still further, the open-loop gain decreases and the condition $e_2 = e_4$ is no longer enforced. The input impedance then decreases.

Differential ac amplifiers are also easily realized through the use of operational amplifiers. Two examples are shown in Fig. 23. In Fig. 23(A) a simple dc decoupling is introduced into the familiar differential dc amplifier circuit. The circuit of Fig. 23(B) provides high input impedance while decoupling dc signals in the second stage. The dc offset voltages of the first-stage amplifiers are removed by the capacitive coupling. The dc offset voltage of the second-stage amplifier is multiplied by the dc gain, 1.0.

Voltage-to-current converters^{1,3}

In applications such as coil-driving and transmission of signals over long lines, it is sometimes desirable to convert a voltage to an output current. With operational amplifiers this is quite easily done. Several realizations of the voltage-to-current converter will be examined in this section.

The simplest V -to- I converters are those for floating loads. The circuits of Fig. 24 are the prime examples of this type. Figure 24(A) illustrates a simple inverting circuit. The input current is given by $i_1 = e_1/R_1$, since R_1 is terminated at the virtual ground of the summing junction. This same current flows through the feedback load impedance Z_L in the feedback loop. The current i_1 is independent of the value of Z_L . Both the signal source and the operational amplifier must be capable of supplying the desired amount of load current. The circuit of Fig. 24(B) operates in the noninverting mode and, hence, presents

FIGURE 23. Differential ac amplifiers. A—Simple one-amplifier circuit. B—High-input-impedance circuit.

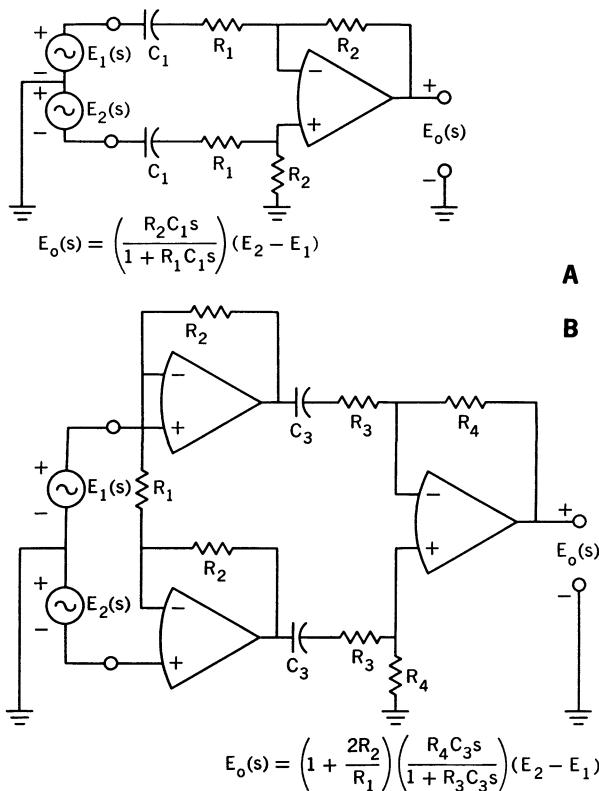
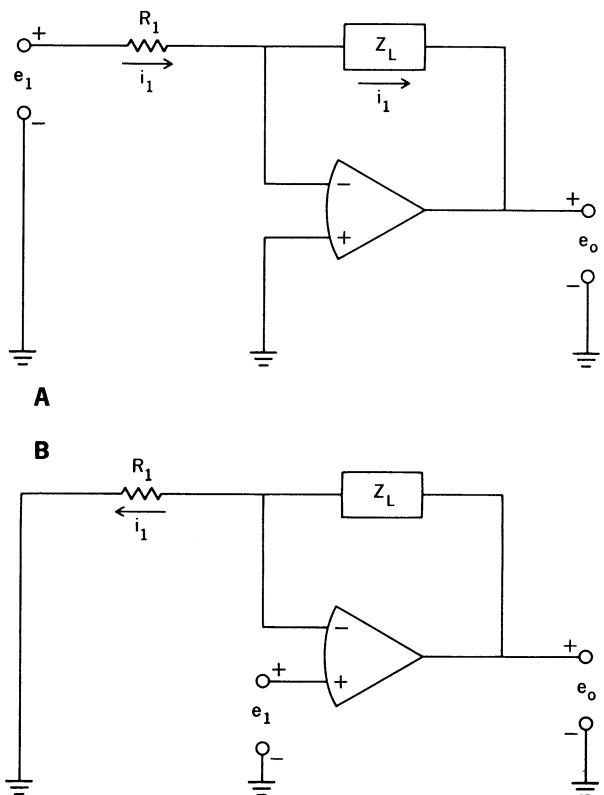


FIGURE 24. V-to-I converters, floating loads. A—Inverting amplifier type. B—Noninverting amplifier type.



a high impedance to the driving source. The current is again given by the equation $i_L = e_1/R_1$ and, again, i_L is the load current. Very little current, however, is required from the signal source because of the high input impedance of the noninverting amplifier.

Another V -to- I converter for a floating load is shown in Fig. 25. In this case most of the current is provided by the amplifier and only a small portion by the signal source. Analysis of the circuit yields the following equation for load current:

$$i_L = \frac{e_1}{R_1} \left(1 + \frac{R_2}{R_3} \right)$$

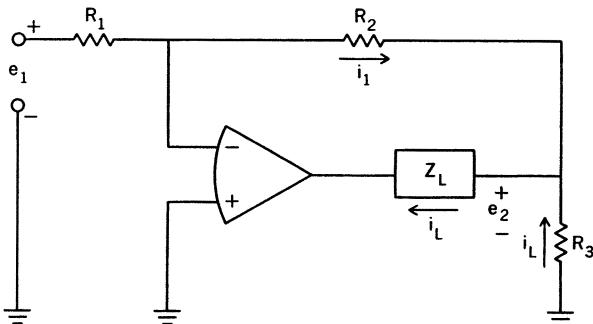


FIGURE 25. Current-amplifying circuit.

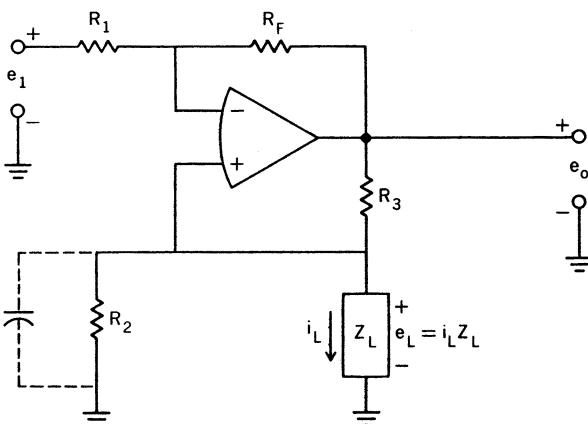
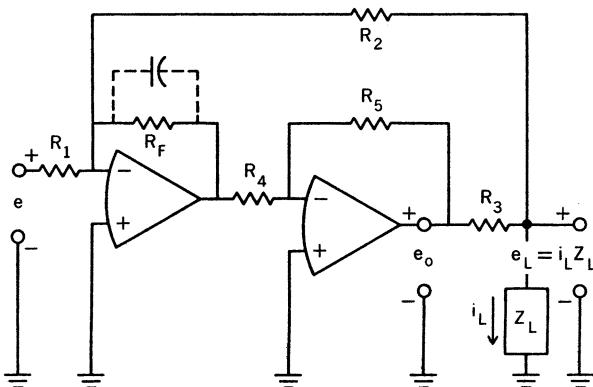


FIGURE 26. Voltage-to-current converter, grounded load.

FIGURE 27. Two-amplifier voltage-to-current converter, grounded load.



Resistor R_3 provides a convenient means for scaling the current. Resistor R_1 can be made relatively large to minimize the loading of the signal source. The amplifier must be capable of providing all of the current to the load and must also be capable of an output voltage equal to

$$(e_o)_{\max} \approx (i_L)_{\max}(Z_L + R_3)$$

For loads grounded on one side there are also circuits that give V -to- I conversion. The single-amplifier circuit of Fig. 26 acts as a current source controlled by e_1 ; i.e.,

$$i_L = -\frac{e_1}{R_2} \quad \text{if } \frac{R_3}{R_2} = \frac{R_F}{R_1}$$

If these ratios of resistances are matched, the circuit will function as a true source of current with very high internal impedance. A mismatch of the ratios will be seen as a decreased internal impedance of the current source. Fluctuations in effective load impedance will then cause fluctuations of the output current. The operational amplifier for the circuit of Fig. 26 must have an output voltage range sufficient to provide the maximum load voltage plus the voltage drop across R_3 . Normally, R_1 and R_2 will be chosen to draw small currents and R_F and R_3 will be made small to minimize voltage drops.

The circuit of Fig. 27 utilizes two inverting amplifiers to drive a current into a grounded load. This current is given by the expression

$$I_L = E_1 \frac{\frac{R_5 R_F}{R_4 R_1}}{R_3 + Z_L \left(1 + \frac{R_3}{R_2} - \frac{R_5 R_F}{R_4 R_2} \right)}$$

If resistors are selected so that

$$1 + \frac{R_3}{R_2} = \frac{R_5 R_F}{R_4 R_1}$$

$$\text{then } i_L = \frac{e_1}{R_3} \left(\frac{R_5 R_F}{R_4 R_1} \right)$$

In particular, if

$$R_1 = R_F = R_4 = R_5$$

$$\text{then } i_L = \frac{e_1}{R_3} \quad \text{and} \quad R_2 = R_F - R_3$$

If R_1 is large, very little current is drawn from the signal source and very little flows through the feedback elements. Then the output voltage is given by

$$(e_o)_{\max} \approx (i_L)_{\max}(Z_L + R_3)$$

Note that, in the circuits of Figs. 26 and 27, when the load is open-circuited the positive feedback is equal to the negative feedback. This is equivalent to an open-loop condition. The stabilizing capacitors shown by dashed lines are therefore desirable to prevent excessive noise and possible oscillations. Figure 28 illustrates a modified form of the two-amplifier V -to- I converter that provides the additional feature of very high input impedance. The expression for output current as a function of input voltage is

$$i_L = \frac{e_1 \frac{R_5}{R_4} \left(1 + \frac{R_F}{R_2} + \frac{R_3}{R_2} \right)}{R_3 + Z_L \left(1 + \frac{R_3}{R_2} - \frac{R_5 R_F}{R_2 R_4} \right)}$$

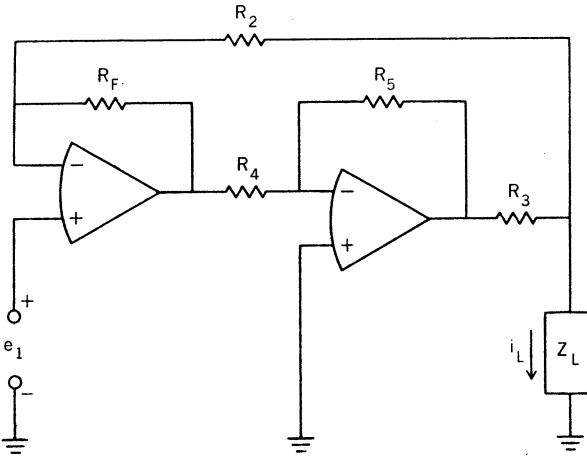


FIGURE 28. Buffered V-to-I converter, grounded load.

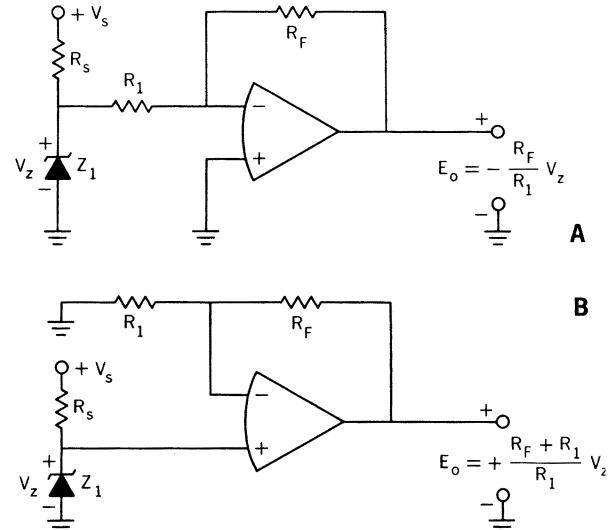
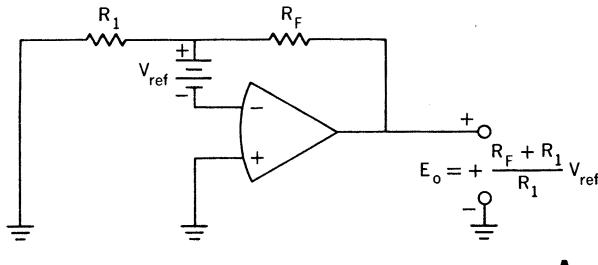
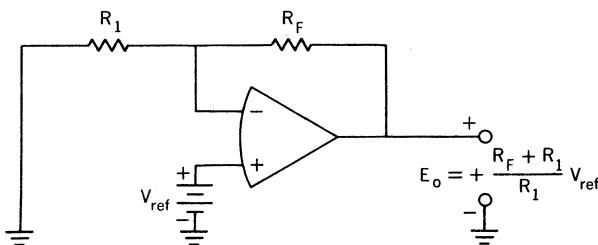


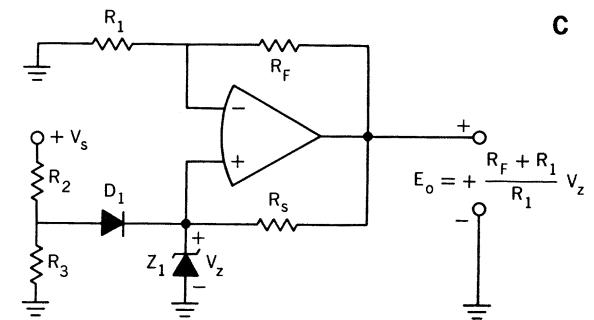
FIGURE 29. Reference-voltage sources. A—Single-ended circuit. B—Noninverting circuit.



A

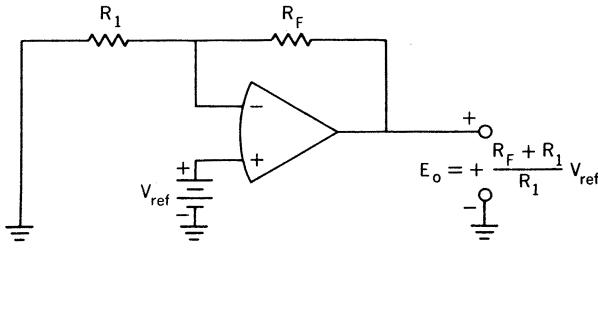


B



C

FIGURE 30. Zener reference sources. A—Inverting. B—Noninverting. C—Noninverting with regulated Zener drive.



If we again select resistors such that

$$1 + \frac{R_3}{R_2} = \frac{R_5 R_F}{R_2 R_4} \quad \text{and} \quad R_F = R_4 = R_5$$

$$\text{then } i_L = \frac{2e_1 R_F}{R_2 R_3} \quad \text{and} \quad R_2 = R_F - R_3$$

Reference-voltage sources and regulators¹⁻³

Because of its high input impedance and easily adjustable gain, the operational amplifier may be used as a reference-voltage source with very low output impedance and substantial output-current capability. Two circuits for use with standard cells are shown in Fig. 29. In both instances the output voltage is given by

$$E_o = V_{\text{ref}} \left(1 + \frac{R_F}{R_1} \right)$$

The circuit of Fig. 29(A) can be used with single-ended amplifiers (such as chopper-stabilized types), as well as with those having a differential input. The circuit of

Fig. 29(B) is used if the reference source or cell must be grounded on one side. The only current drawn from the cell is the input bias current of the amplifier plus a term given by

$$I_{\text{in}} = \frac{E_o}{A R_{\text{in}}} = \frac{V_{\text{ref}} \left(1 + \frac{R_F}{R_1} \right)}{A R_{\text{in}}}$$

where R_{in} is the differential input impedance of the operational amplifier. This component of current is negligible in comparison to bias current for most amplifiers. The reference voltage cell is, for all practical purposes, isolated from any load being driven. The effective output impedance, R_{out} , is given by

$$R_{\text{out}} = \frac{R_o}{A \beta}$$

$$\text{where } \beta = \frac{R_1}{R_1 + R_F}$$

and R_o is the open-loop output impedance.

The load regulation is therefore given by

$$\text{Regulation (percent)} = \frac{R_o}{A \beta R_L} \times 100$$

where R_L is the minimum load impedance.

Similar circuits for use with Zener diodes are shown in Fig. 30(A) and (B). The loading conditions on the Zener diodes are constant and the load regulation is the

same as derived for the circuits of Fig. 29. Regulation with respect to the input voltage V_s depends upon the dynamic resistance of the reference Zener diode Z_1 . The circuit of Fig. 30(C) further reduces this regulation due to input voltage by providing the output reference voltage as the source for the Zener diode current. The dc voltage V_s now functions only as a "start-up" voltage through the network of R_2 , R_3 , and D_1 .

Voltage regulators

Any one of the voltage references described in the preceding section may be considered a voltage regulator, with extremely tight regulation characteristics. Where higher output currents are required, a power booster can be added, inside the feedback loop. However, in speaking of voltage regulators, it is more usual to consider operation from a single source of unregulated dc voltage, rather than the dual supplies tacitly assumed in the reference-voltage circuits. Figure 31 shows such a regulator. The amplifier, which normally operates on dual power supplies of opposite polarity, is biased for operation on a single unregulated power supply. The negative supply terminal is grounded and the noninverting input is biased at the Zener voltage. The Zener diode Z_1 operates at constant load current, since the output current is provided by the transistor Q_1 . If the amplifier has a minimum (balanced) supply rating of $\pm V_m$, then V_s must be larger than $2V_m$. Similarly, if $\pm V_M$ is the maximum (balanced) supply rating, V_s must not exceed $2V_M$. The amplifier will saturate as the output voltage approaches either supply voltage. This determines the limit on output, whereas the common-mode voltage range sets the lower limit on Zener voltage.

Although the amplifier may have an internal current limit, the resistor R_p is required to protect against short circuit in this type of regulator. This is because a short circuit to ground is equivalent to a short circuit to the negative supply. This causes a power dissipation equal to twice that of a short circuit to ground when operating on balanced dual supplies. Thus the internal protection may not be sufficient. The value of R_p should be chosen to limit the amplifier short-circuit current to approximately half the internal current-limit value when the output is at positive saturation voltage. The resistor R_s provides current-limiting to protect Q_1 .

The load regulation of this type of regulator can exceed 0.01 percent, since the effective output impedance is very low. The line regulation is increased beyond that of the Zener by using the output voltage as excitation for the Zener.

Current amplifiers

Current amplifiers, or current-to-voltage converters, are realized very simply by the use of operational amplifiers. An ideal current source has infinite output impedance and an output current that is independent of load. Photocells and photomultiplier tubes are basically current sources with an output impedance that is finite but very large. For small load impedances, the output impedance may be considered infinite.

The current-to-voltage converter of Fig. 32 presents almost zero load impedance to ground because the inverting input appears as a virtual ground. The input current, however, flows through the feedback resistor, generating an output voltage

$$e_o = -i_s R_F$$

The actual input impedance Z_{in} of the current-to-voltage converter, taking into account the finite gain A and differential (open-loop) input impedance Z_{id} , is

$$Z_{in} = \frac{Z_{id}}{1 + \frac{Z_{id}}{R_F}(1 + A)} \approx \frac{R_F}{1 + A}$$

The lower limit on measurement of current input is determined by the bias current of the inverting input. For greatest resolution, FET or varactor bridge amplifiers are usually employed.

The gain of the amplifier for dc offset voltage and noise voltage is given by

$$\frac{R_F + R_s}{R_s} \approx 1.0 \quad \text{since } R_s \gg R_F$$

Although errors resulting from these parameters are very small, current noise can be a factor because of the very large impedances. Since most such measuring circuits are used for very-low-frequency signals, it is usual to parallel R_F with a capacitor C_F to reduce the high-frequency current noise. Output impedance of the current-to-voltage converter is very low because of the nearly 100 percent feedback.

Charge amplifiers

Some transducers, such as capacitance microphones and some types of accelerometers, operate on the principle of conversion of the measurement variable into an equivalent charge. The equivalent circuit of such a trans-

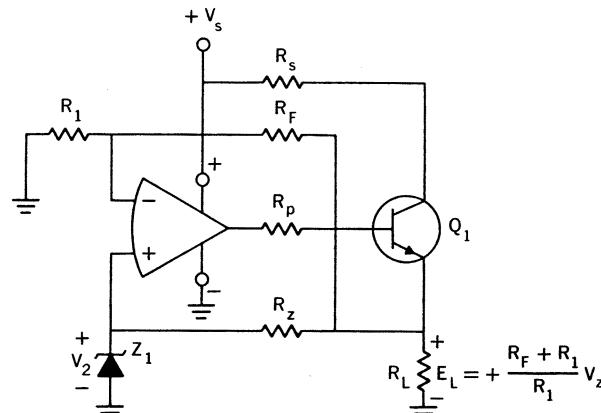
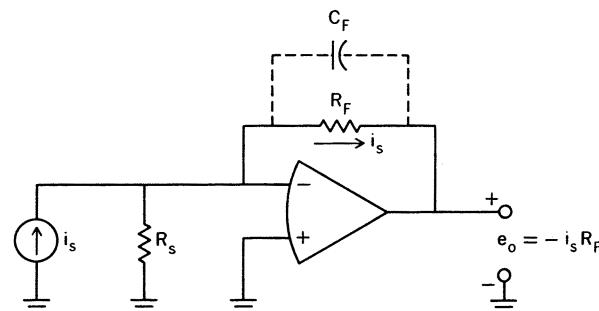


FIGURE 31. Voltage regulator.

FIGURE 32. Current amplifier (I-to-V converter).



ducer may be represented by a battery and capacitor in series, as shown in Fig. 33(A). As the capacitance varies, the charge also changes, according to the equation

$$\Delta q = \Delta C_1 E$$

When the transducer is connected to the inverting input of an operational amplifier, as in Fig. 33(A), this charge flows into the feedback capacitor C_F . The resultant change in charge on C_F generates an output voltage

$$e_o = -\Delta C_1 \frac{E}{C_F}$$

Since the operational amplifier requires a dc path from each input to common (for bias-current flow), it is necessary to insert the resistor R_1 . In the absence of this resistor, the capacitors will build up a dc charge until the output voltage reaches saturation. This resistor limits the lower cutoff frequency of the charge amplifier. For stabilization purposes, and sometimes for protection of

the amplifier input stage, it is also desirable to insert the series resistor R_1 . This resistor limits the upper response frequency as shown in Fig. 33(B).

The gain, or sensitivity, of the charge amplifier in its passband is given by

$$\frac{e_o}{\Delta C_1} = -\frac{E}{C_F}$$

and can be varied only by changes in C_F . It is usually desirable to use a small value of C_F consistent with the desired frequency response and a reasonable value of R_F . Because of their high input impedance, low bias current, and wide bandwidth, FET amplifiers are usually the first choice for charge amplification.

Another common form of charge amplifier is shown in Fig. 34. Here the amplifier operates as a noninverting buffer with gain. Charge flows into, and out of, capacitor C_2 as the capacitance of the transducer varies. Once again these capacitance variations are converted into voltage variations at the amplifier output. An amplifier with an FET input stage is usually required in this circuit; it also minimizes the bias and noise currents. Resistor R_B provides the dc path for this bias current and limits the low-frequency response of the circuit.

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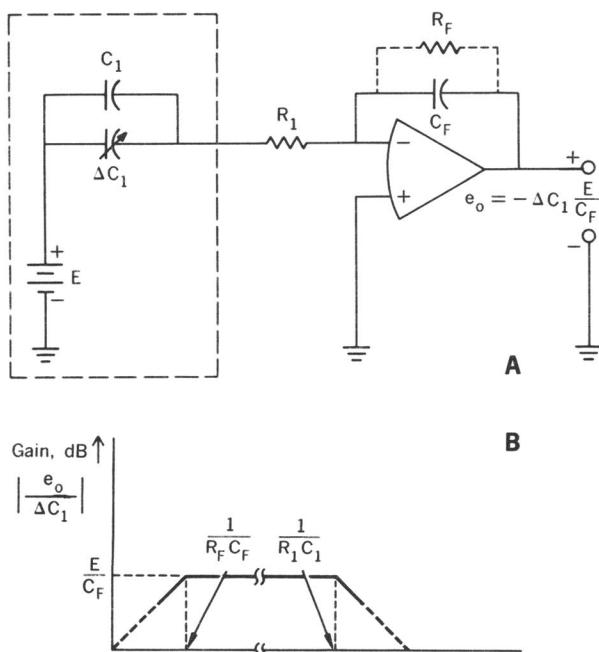
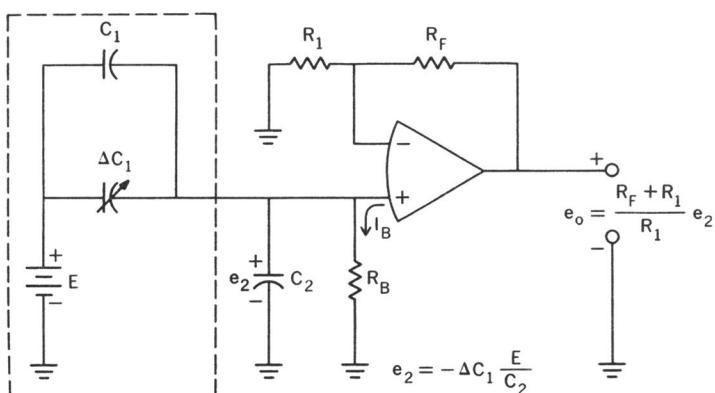


FIGURE 33. Charge-amplifier operation. A—Typical circuit. B—Frequency response.

FIGURE 34. Charge-amplifier circuit in which amplifier operates as a noninverting buffer with gain.



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