ETH

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Institut für Integrierte Systeme

Integrated Systems Laboratory

SEMESTER PROJECT AT THE DEPARTMENT OF
INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

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PULPino implementation in 65nm CMOS

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1 Introduction

At the Integrated Systems Laboratory (IIS) we have been working on a Parallel Ultra-Low Power Processor (PULP) System for the past two years[1]. Throughout the project we have worked on different processor cores. For the first few designs, the original or1k code from the opensource project was used[2]. We then heavily modified this core and improved its IPC (instructions per clock) close to its optimum value of 1. In a next step we started a new implementation from scratch, and called this implementation Or10n[3]. This core has been the main processor core used in PULP projects.

The RISC-V[4] effort started also during this time and is being driven by the Computer Science Division of the EECS Department at the University of California, Berkeley. At the moment, this instruction set architecture (ISA) is very popular in academic circles, so much so that several members of the Open RISC projected have stated that they would stop working on the OpenRISC project and concentrate on RISC-V.

For this reason, we have also investigated the possibility to have a 32-bit version of the RISC-V architecture and during a recent Master Thesis we have developed RI5CY, our own implementation of the RISC-V32 architecture that is reaching a level of maturity close to that of the latest Or10n cores. This core has attracted much attention, also from the lowrisc project[5] of the Cambridge University with which we have a close collaboration.

From the start the intention was to make the entire PULP project open, and provide everyone access to high-quality processor complete with all support (tool flow, debugging, FPGA and ASIC mapping scripts). Until now, we have been unable to rollout a release mainly due to lack of experience in large open projects, and the state of the documentation. As a first step we have decided to release PULPino, a single core processor that uses the same cores we have developed, together with a selected set of peripherals. The release is expected within 2015 and should also contain an FPGA mapping to the popular ZED platform which will allow many people to start using it.

This project has attracted considerable attention, and we have been asked whether or not the processor would support operating systems. In several instances a desire to run FreeRTOS[6] as well as sel4[7] was stated.

2 Project Description

The goal of this project is to implement the first ASIC version of PULPino in UMC65 CMOS process, and to make the necessary changes to the system to run FreeRTOS and/or Sel4. The group is already working on a PULPino release (for FPGA) and the goal is to work together to adapt and extend the PULPino so that it can also support the FreeRTOS and/or sel4. This will at the very least require a timer unit that needs to be added to the system, but may also require some additional changes such as support for supervisor mode commands etc. The tape-out is scheduled to coincide with the student tape-out early in January 2016.

We will join the Orconf conference in October in Geneva[8], to present the PULPino project to a wider audience, and we expect to get some more feedback from the community in general on this topic. Following this conference, and time permitting, we might wish to integrate the ideas from this meeting into the current project as well.

3 Goals

First and foremost, the goal of this project, is to learn and experience the design process for a digital ASIC. At the end of the project a chip in UMC65 will be taped out. We expect that the manufactured chip:

- Uses the latest PULP core either Or10n or RI5CY.

- Be able to boot from an external EEPROM like other PULP systems

- Run an operating system (FreeRTOS, sel4 or other) and a demo application on it.

- Have a basic set of interfaces (SPI, GPIO)

We would like that this work complements our current PULPino project. Furthermore, it would be good if the result of this project could be done in a way that will benefit future collaborations with our partners, specifically ACP which has an interest in running OsmocomBB on FreeRTOS and Simless (part of the LowRISC project) that wants to develop a security module based on a core running sel4.

4 Project Realization

4.1 Project Plan

Within the first month of the project you will be asked to prepare a project plan. This plan should identify the tasks to be performed during the project and sets deadlines for those tasks. The prepared plan will be a topic of discussion of the first week's meeting between you and your advisers. Note that the project plan should be updated constantly depending on the project's status.

4.2 Meetings

Weekly meetings will be held between the student and the assistants. The exact time and location of these meetings will be determined within the first week of the project in order to fit the students and the assistants schedule. These meetings will be used to evaluate the status and progress of the project. Beside these regular meetings, additional meetings can be organized to address urgent issues as well.

4.3 HDL Guidelines

Since most of the PULP project is written in System Verilog, it is strongly suggested to use System Verilog for this project as well. However, any other HDL can also be used if there are strong arguments to use them.

Adapting a consistent naming scheme is one of the most important steps in order to make your code easy to understand. If signals, processes, and entities are always named the same way, any inconsistency can be detected easier. Moreover, if a design group shares the same naming convention, all members would immediately *feel at home* with each others code. At the IIS we make use of the naming convention proposed by the Microelectronics Design Zentrum [9]. The PULP code uses a similar but slightly different style. Thus, try to maintain the PULP naming convention in order to create readable and maintainable HDL code. Note that there might still be some legacy code which may not be compatible to the naming convention. It is not the goal of this work to re-write and adapt all code to a common naming convention, but the newly developed code should be compatible, and the top-level interfaces to legacy code should be adapted to be compatible to the rest of the system.

4.4 Report

Documentation is an important and often overlooked aspect of engineering. One final report has to be completed within this project.

The common language of engineering is de facto English. Therefore, the final report of the work is preferred to be written in English. Any form of word processing software is allowed for writing the reports, nevertheless the use of LaTeX with Tgif[1] or any other vector drawing software (for block diagrams) is strongly encouraged by the IIS staff.

Final Report The final report has to be presented at the end of the project and a digital copy need to be handed in. Note that this task description is part of your report and has to be attached to your final report.

4.5 Presentation

There will be a presentation (15 min presentation and 5 min Q&A) at the end of this project (usually last Thursday of the semester) in order to present your results to a wider audience. The exact date will be determined towards the end of the work.

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[1] Tgif is a simple vector drawing software, quite useful for drawing block diagrams. For further information about Tgif we refer to `http://bourbon.usc.edu:8001/tgif/index.html` and `http://www.dz.ee.ethz.ch/en/information/how-to/drawing-schematics.html`.

References

[1] PULP home page: `http://pulp.ethz.ch`

[2] Opencores website: `http://opencores.org`

[3] Or10n project website: `http://iis-projects.ee.ethz.ch/index.php/Ultra-low_power_processor_design`

[4] The RISC-V website: `http://riscv.org`

[5] The LowRISC website: `http://www.lowrisc.org`

[6] The FreeRTOS website: `http://www.freertos.org`

[7] The Sel4 website: `https://sel4.systems`

[8] The ORconf2015 website: `openrisc.io/orconf`

[9] The EDA www page (ETH Zurich internal) `http://eda.ee.ethz.ch` and VHDL naming conventions: `http://eda.ee.ethz.ch/index.php/Naming_Conventions`

[10] H. Kaeslin. "Top-Down Digital VLSI Design, 1st Edition From Architectures to Gate-Level Circuits and FPGAs". *Morgan Kaufmann*, 2014.

Zurich, September 15, 2015   Prof. Dr. Luca Benini