University of Chinese Academy of Sciences

Verification & Implementation of SoC Design

Low Power Design Technology

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Low Power Design

- **Low Power Design in Advanced Nodes**
- Low Power Design and Its Verification
- Implementation of Low Power Design
- Power Integrity and Power Analysis
- Summary

Focused Technologies at 2X-nm Process Nodes

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Node	32/28nm	22/20nm	16/14nm
Intel	2007 “GL”; 45/32nm HkMG	Ivy Bridge: 22nm Tri-Gate (5/2/11)	IUV for 11nm? 5-7nm node
TSMC	3D IC on 28nm (6/4/12); CoWos	10/09/12: 20nm ready for IC Design	10nm FinFET by 2015
IBM	“GF” 32 nm HkMG; SOI (1/10/12)	SOI	T.O. 10/30/12: FinFET, ARM CM0, EDI
GF	“GF” 32nm for HkMG SOI (1/10/12)		
SMIC	2012: 28nm	?	FinFET ?
Tech	GF/GL; 3D IC; HkMG; SOI; CoWos	Tri-Gate; DPT; 3D IC (stkd); SOI	IUV, 18” wafer FinFET / ArF 100W 200W/cm^2

Semiconductor manufacturing processes

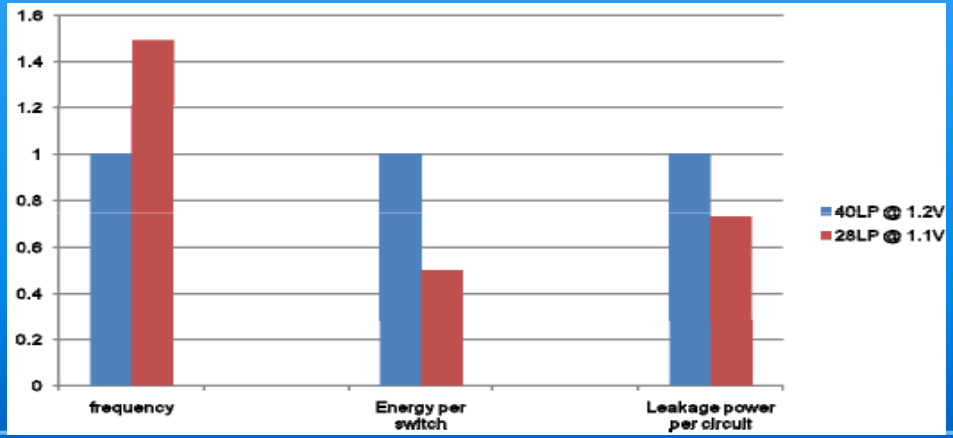
10 µm — 1971
3 µm — 1975
1.5 µm — 1982
1 µm — 1985
800 nm — 1989
600 nm — 1994
350 nm — 1995
250 nm — 1997
180 nm — 1999
130 nm — 2002
90 nm — 2004
65 nm — 2006
45 nm — 2008
32 nm — 2010
22 nm — 2012
14 nm — est. 2015
10 nm — est. 2017
7 nm — est. 2020
5 nm — est. 2022

Half-nodes

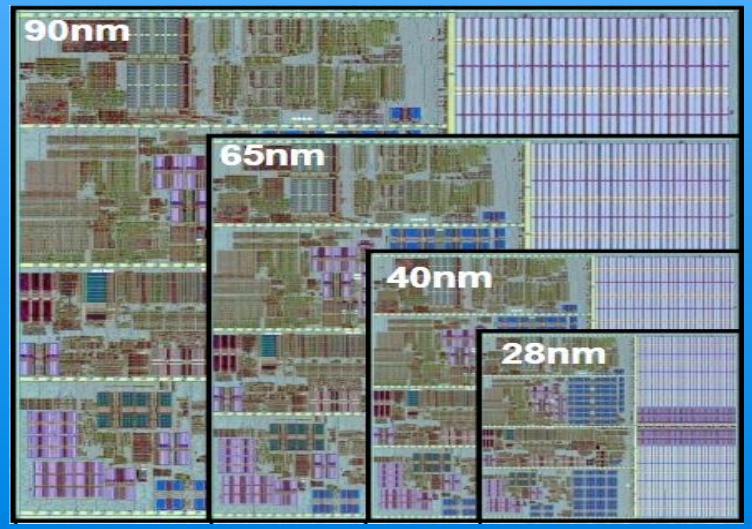
V • T

28nm Provide Area And Power Advantages

- 28nm value proposition (relative to 40nm)
  - ~100% density increase
  - Up to 50% increased speed

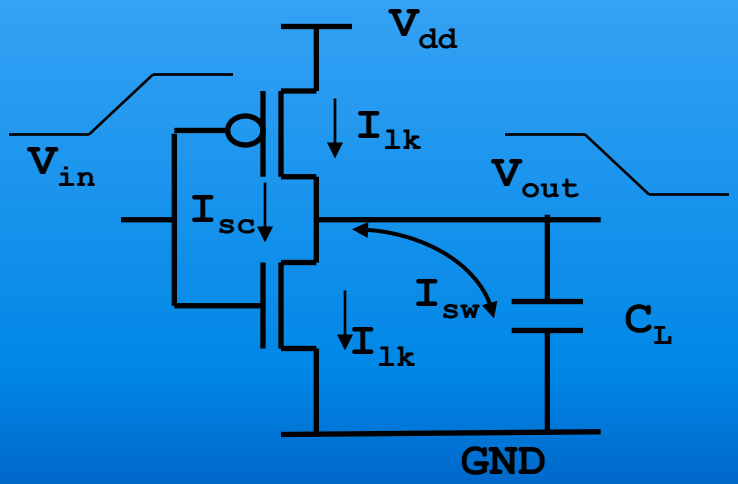


Source: GlobalFoundries



CMOS Power Dissipation

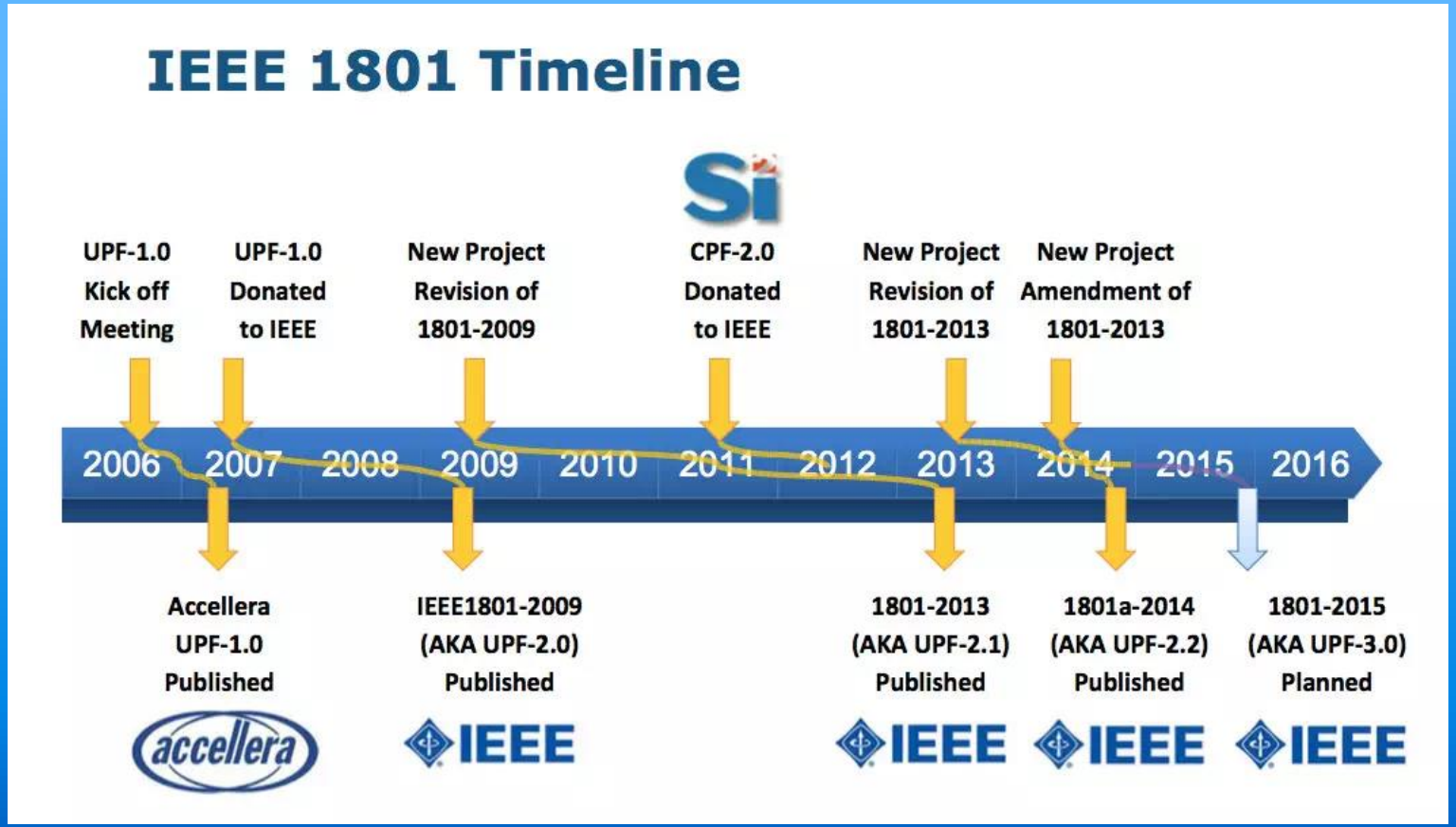
- **Dynamic Short-circuit Power**
  - Due to direct current path from V_{dd} to ground during output switching
  - $I_{sc} \propto$ input_slew/C_L
- **Dynamic Switching Power**
  - Due to charge/discharge of load cap
  - $P = 0.5*C_L*V_{dd}^2*TR$
    - TR is the net Toggle Rate, which is toggle count/ns
- **Static Leakage Power**
  - Due to subthreshold leakage from V_{dd} to GND



Power Tradeoffs with A CPF-Based Methodology

Power reduction technique	Power Savings	Timing penalty	Area penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Area optimization	Small	-None-	n/a	-None-	Low	-None-	Low
Multi-Vt optimization	Medium	Little	Little	-None-	Low	-None-	Low
Clock gating	Medium	Little	Little	-None-	Low	Low	Medium
Multi-supply voltage	Large	Some	Little	Medium	Low	Low	Medium
Power shut-off	Huge	Some	Some	Medium	Medium	Medium	Medium
Dynamic & Adaptive Voltage Frequency Scaling	Large	Some	Some	Medium	Medium	Medium	Medium

IEEE1801 and CPF/UPF

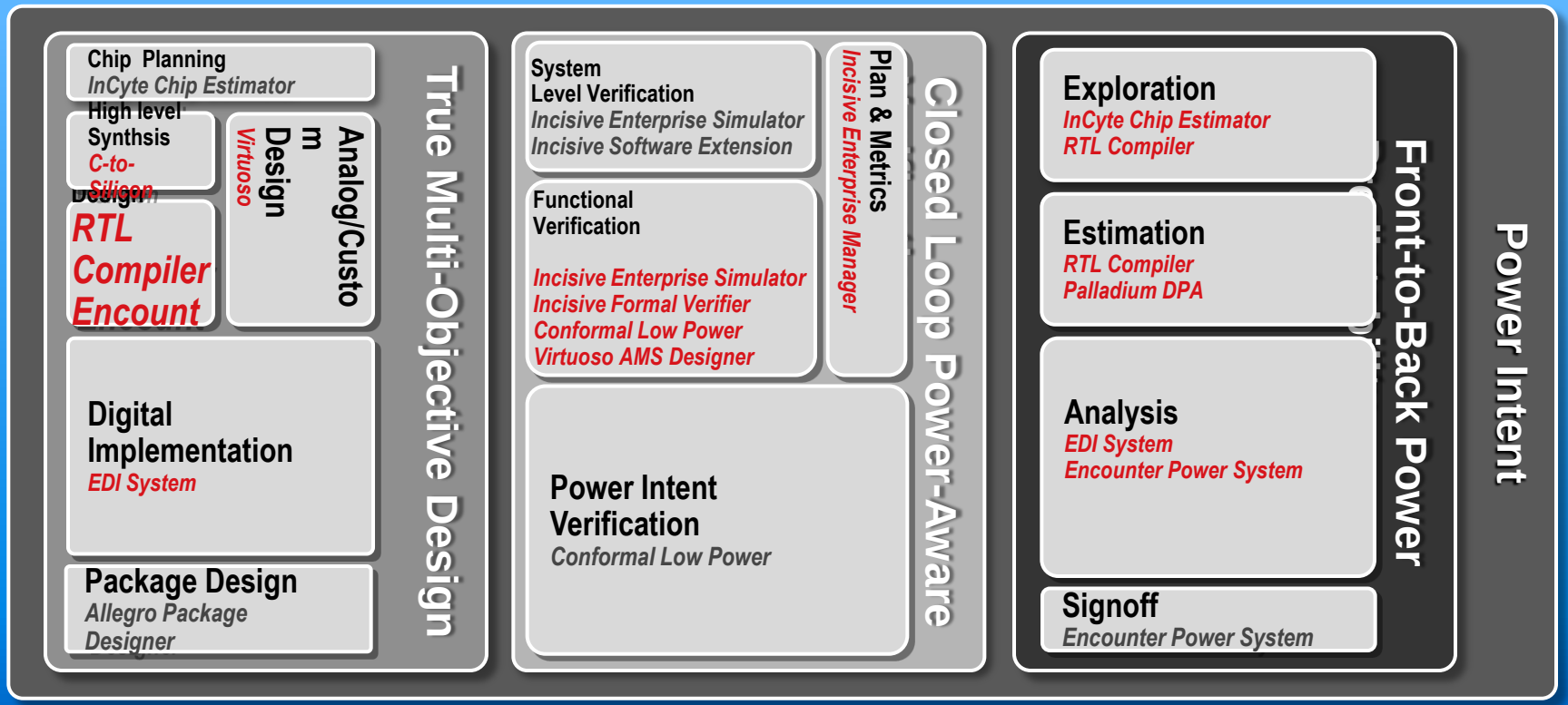


Low Power Design

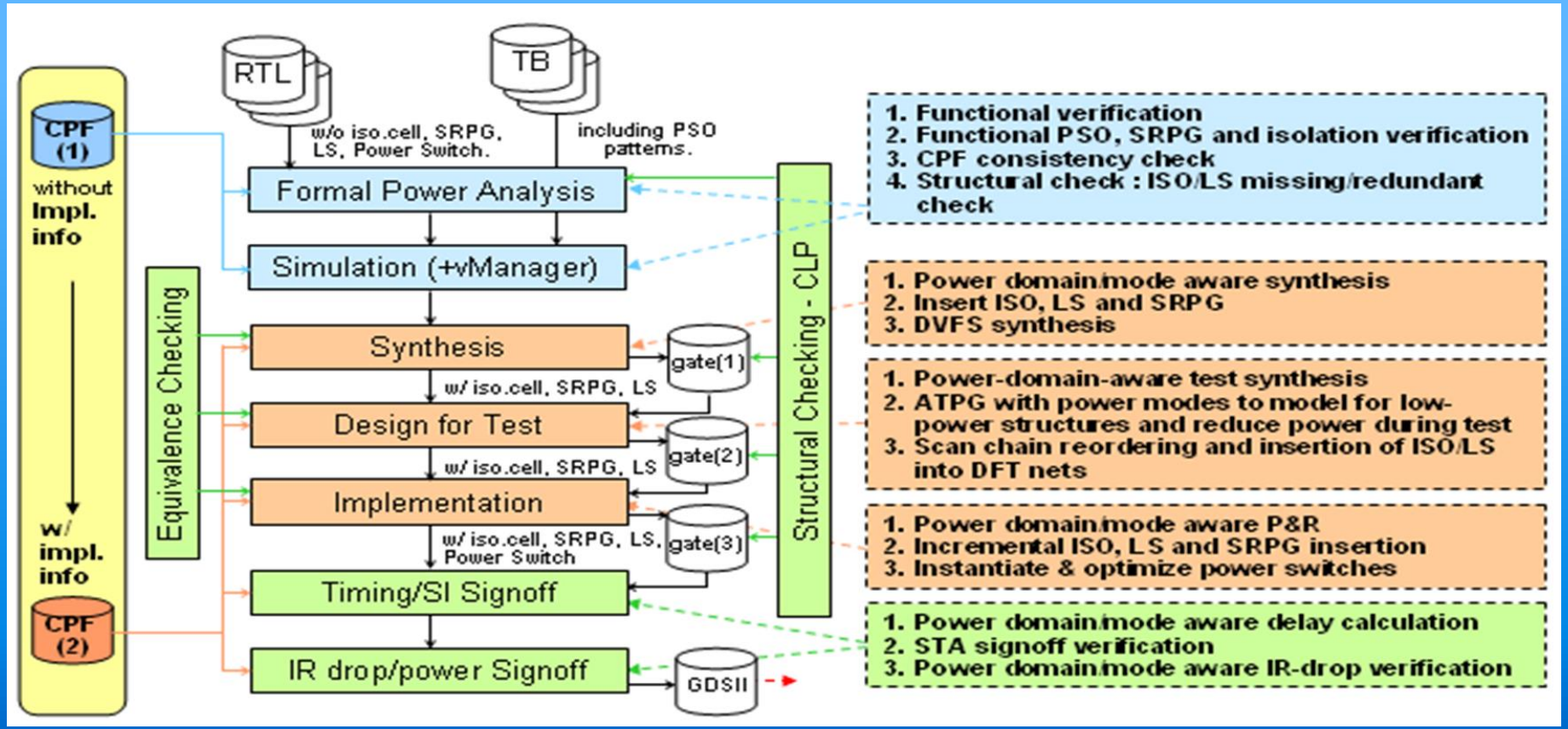
- Low Power Design in Advanced Nodes
- **Low Power Design and Its Verification**
- Implementation of Low Power Design
- Power Integrity and Power Analysis
- Discussion

Products & Flows

The Advanced Technology for Power-Aware Design

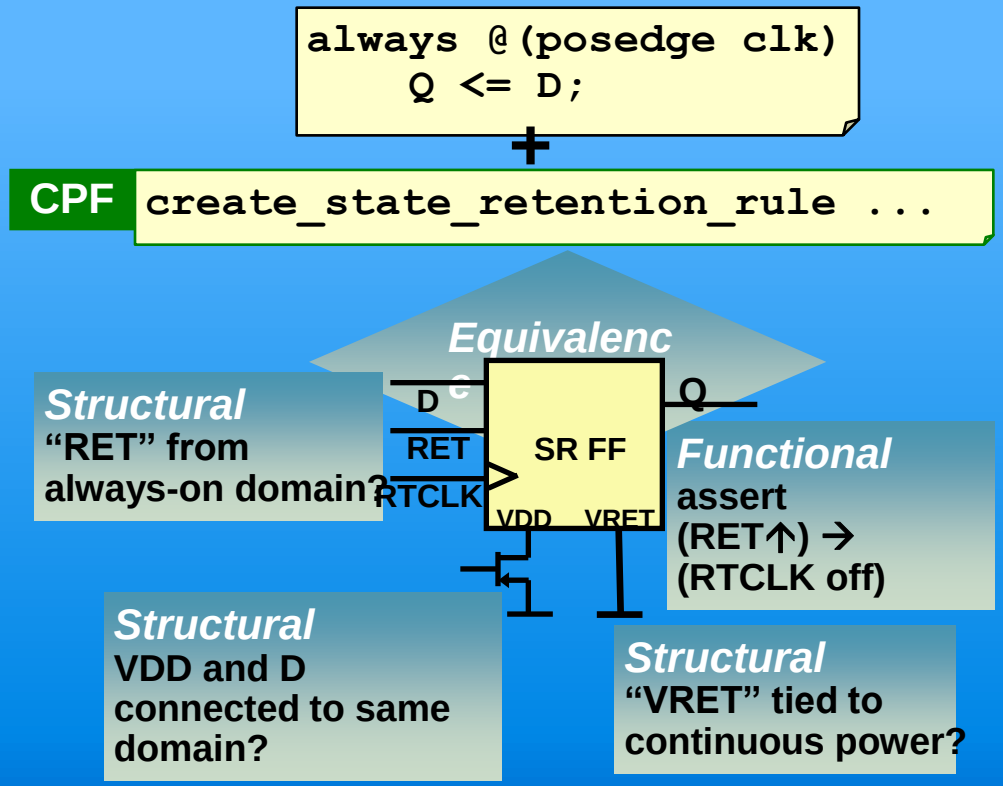


From Simulation to Sigoff using CPF



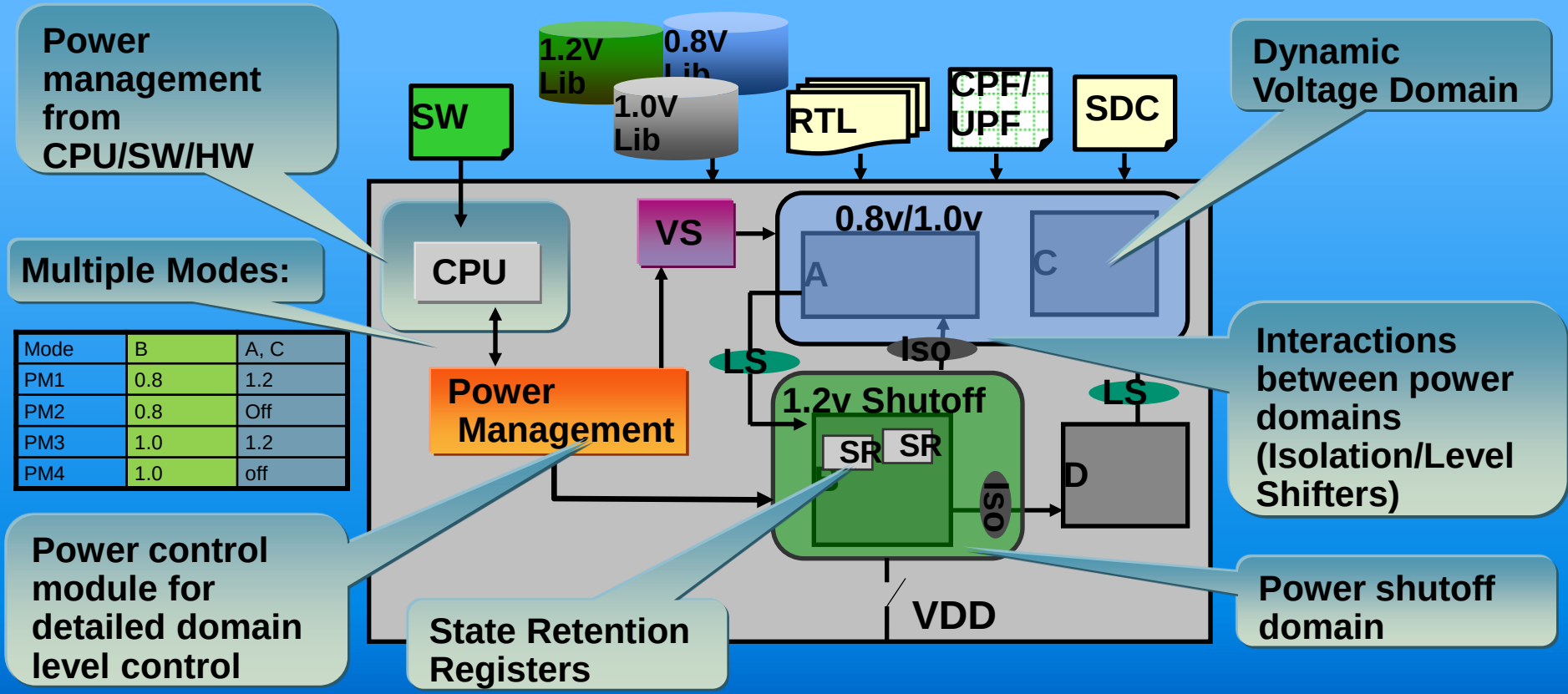
Front-End: Formal Verification
Conformal® Low Power

- Checks CPF quality and consistency
- Power domain aware equivalence checking verifies:
  - Low power optimizations
  - State retention mapping
  - Power domain states and boundaries
- Structural and Rule checks ensure:
  - Proper insertion of low power cells
  - Proper connectivity of low-power cells
  - Consistency with CPF
- Functional checks formally validate:
  - Isolation function
  - State retention function
  - Detect leakage paths across power domain boundaries



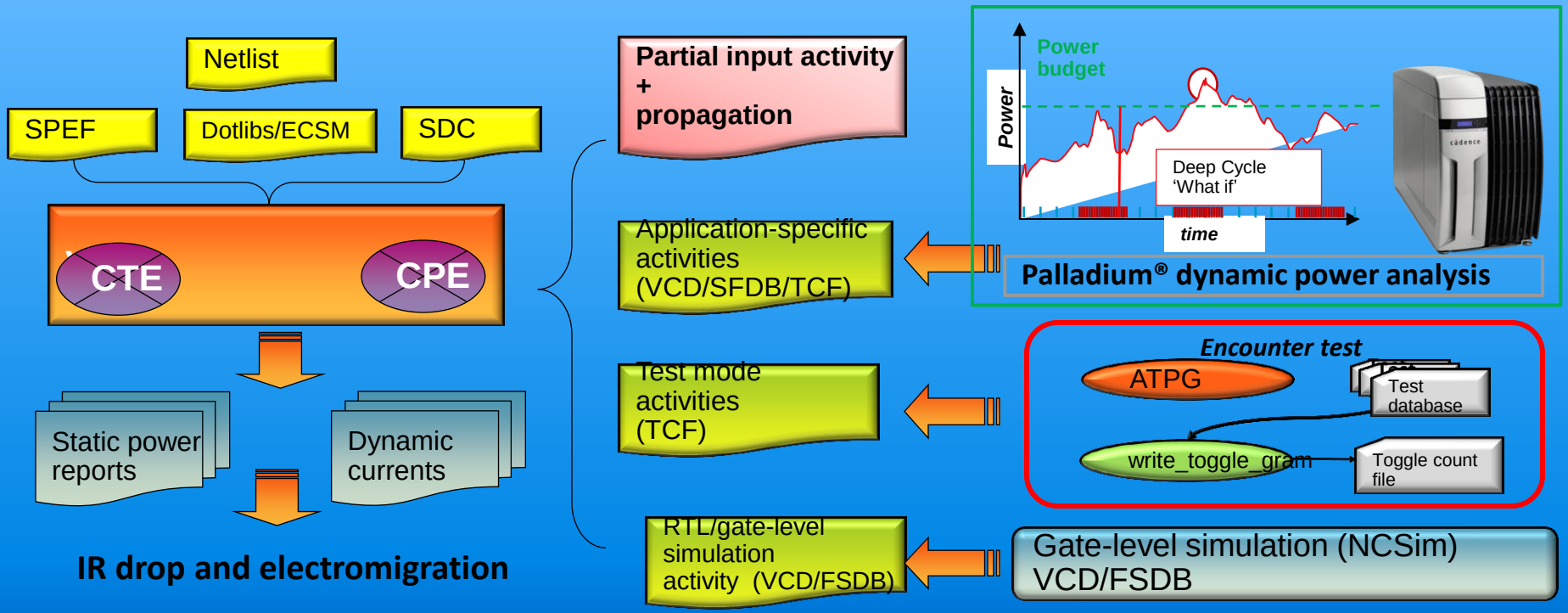
Ensures correct implementation of advanced low-power techniques

Low Power Design



Activity and Accurate Power Calculation

Design concern: *How to get realistic power estimates for my design?*



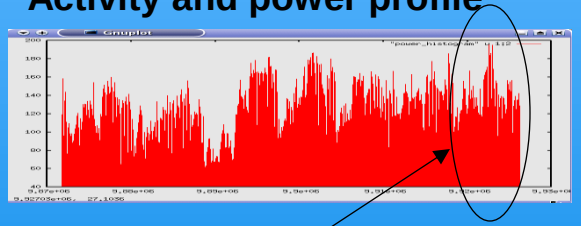
Accurate activity information enables accurate static and dynamic power estimation.

Cycle-Accurate Power Estimation Vector Profiler

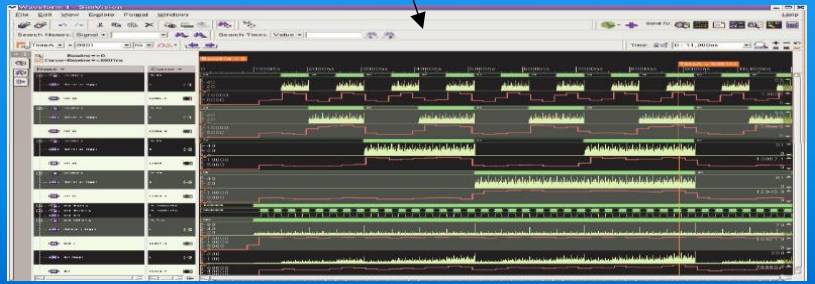
Design concern: *How do I find highly active events that can cause timing or functional failures due to high power and IR drop?*

- Integrated in the Common Power Engine (CPE)
  - Identifies worst-case windows for dynamic -power and IR-drop calculation
  - Uses event-based peak-power profiling with small resolution (1 ps) and high performance
  - Reports toggle counts or calculated power spanning the whole vector
  - Reports toggle counts or calculated power in a user-defined window
  - Reports profile for total, switching, internal, or leakage
- Flexibility enables reporting per-power net.
- Efficiency to profile huge files.
- Supports VCD and FSDB simulation data formats.
- Graphical display of VCD, activity, and power histograms in SimVision.

Activity and power profile



Identify high activity and power cycles for detailed static and dynamic analysis



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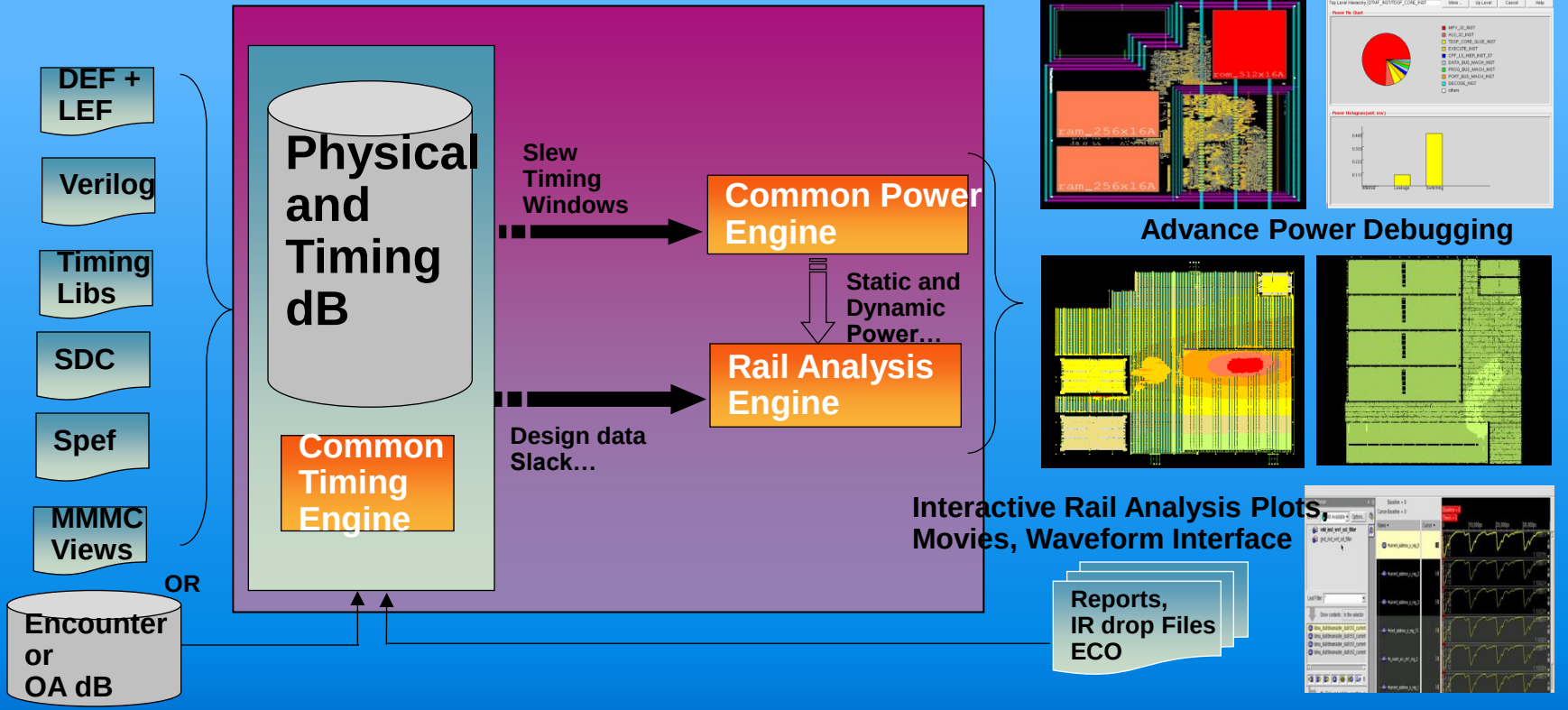
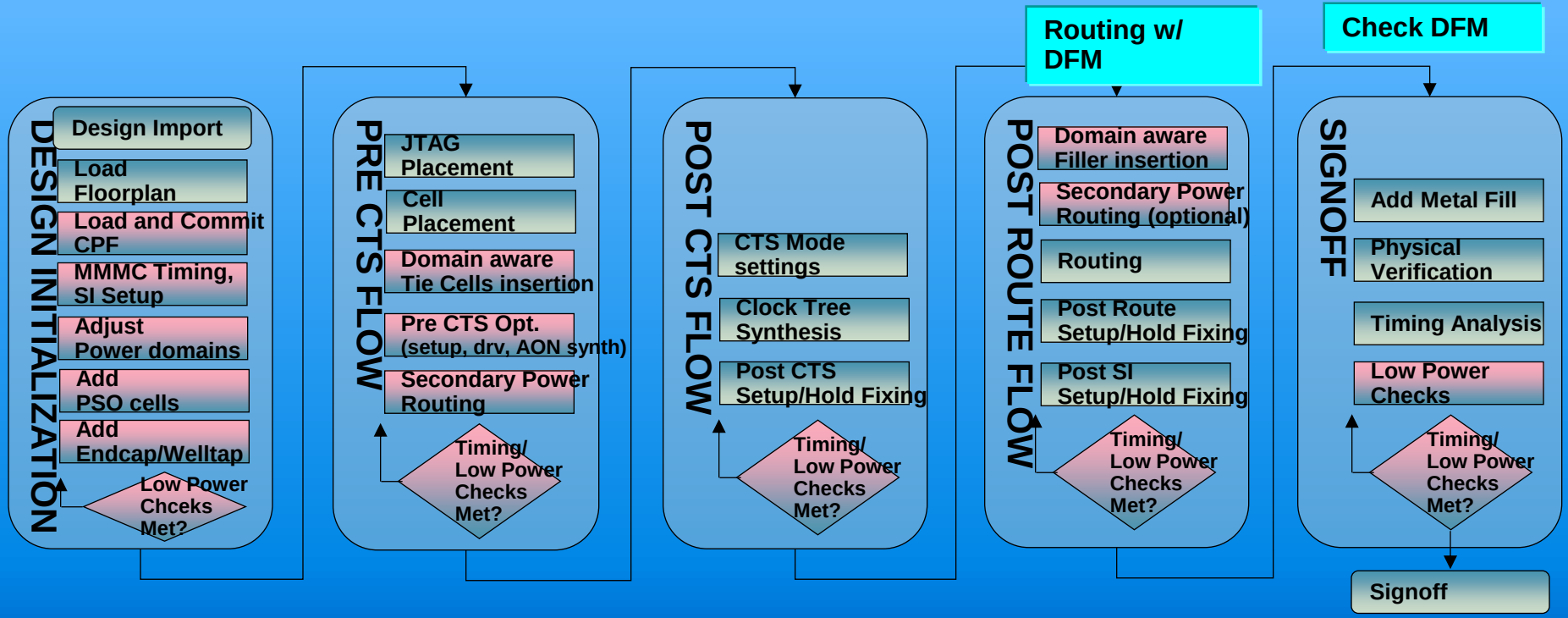
Low Power Design System

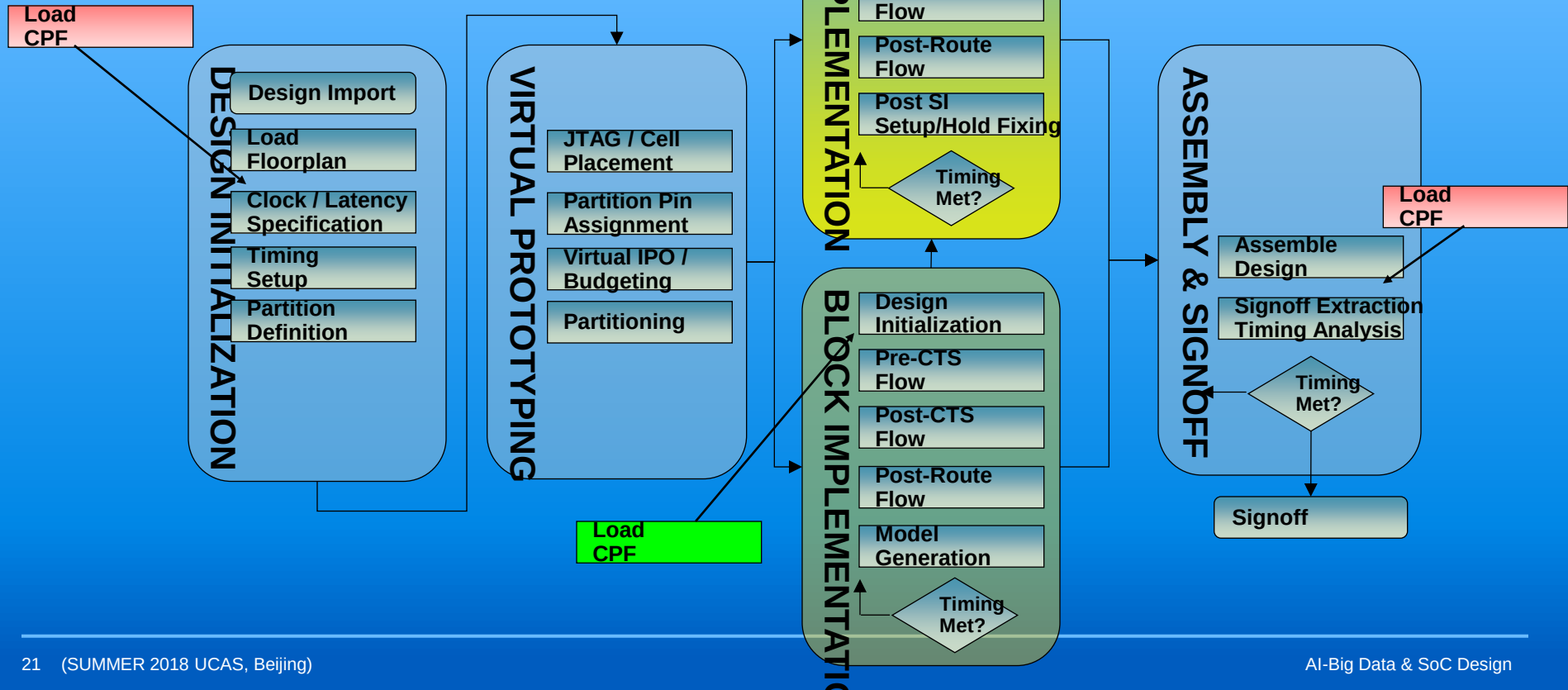


Low Power Design Flow



Hierarchical Flow w/ CPF

(single-pass ILM and Black Box)



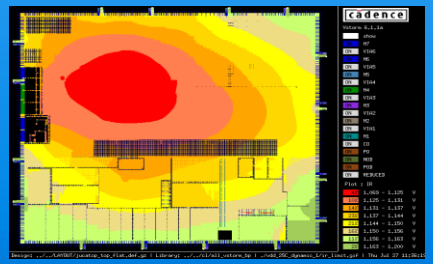
Decap Analysis and Optimization

- Decoupling capacitance on power grid helps in reducing dynamic IR drop.
- Adding decoupling cells on power grid increases overall design leakage power.
- At 65 nm, and below, leakage power component can be as high as 50 percent of total power.

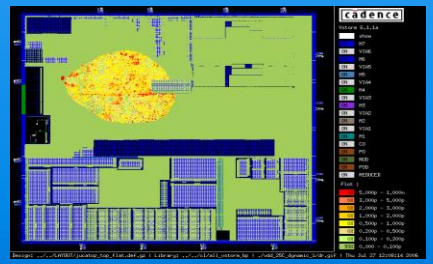
Design concern: *How to manage leakage power and dynamic IR drop in the design?*

Power planning → **Powerv grid optimization** → **Signoff**

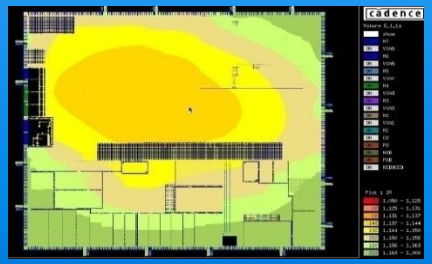
- **Power planning**: Area-based decap estimation; Rule-based decap insertion
- **Powerv grid optimization**: Placement-aware decap optimization; Timing and Leakage aware decap optimization
- **Signoff**: Decap removal



1. Set IR-drop limit.



2. Calculate additional decap required.



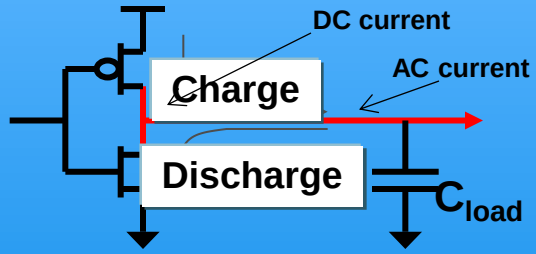
3. Validate IR drop using what-if analysis.

4.Implement in an EDI System.

Design change in EDI System

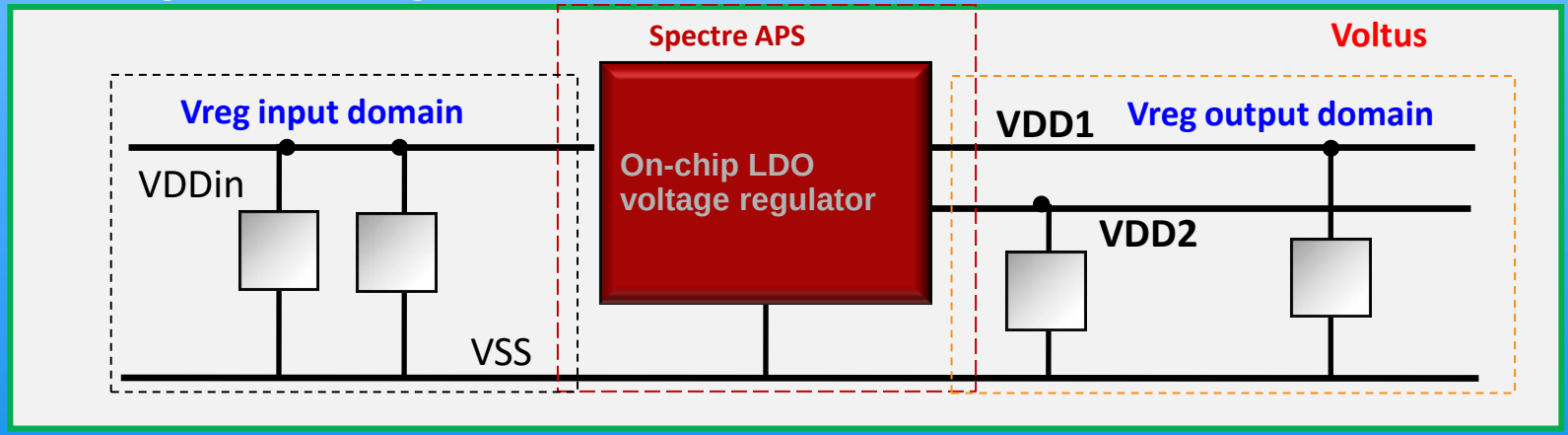
Power and Signal Electromigration

- **Power electromigration**
  - Supports power electromigration during IR-drop analysis
  - Supports Blech-length, MTTF, variable width models and RMS AC EM analysis and models.
  - Supports electromigration models embedded inside QRC technology file
- **Signal electromigration**
  - Supports AC (Joule heating) and DC (hot-carrier injection) signal electromigration analysis.
  - Supports frequency-based DC electromigration templates in liberty (frequency limits based on input slew and output load).
  - SPICE correlation within 5 percent when ECSM models are used for Irms current waveform computation.
  - *Irms* computed for each wire segment considering downstream capacitance to avoid false electromigration violations.
  - Automatic fix is available through the EDI System.



On-Chip Low Dropout Voltage Regulator

- Stabilizing local voltage



- Power-integrity analysis challenges
  - Nonlinearity of low dropout (LDO) due to transistors, BJTs, and so on
  - Linearity of power-grid RC network
- Voltus technology advantages: APS + Voltus co-simulation
  - Nonlinear devices in LDOs: Spectre APS
  - Linear power grid: Voltus
  - Quick convergence at partition boundaries

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Power Integrity Analysis in a Typical Design Flow

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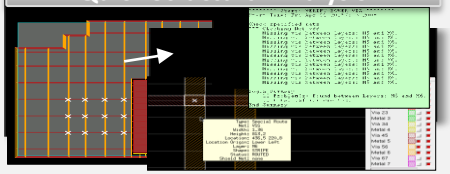
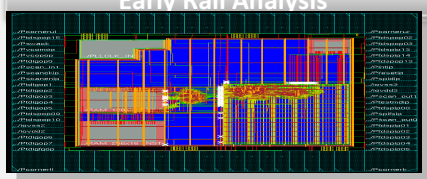
Quick Structural Analysis



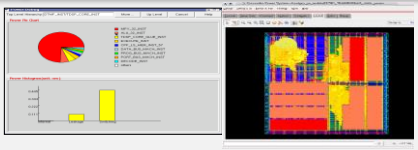
- Quick sanity check and analysis on input data
- Identify gross design issues
- Connectivity check, such as missing via report

Early Rail Analysis



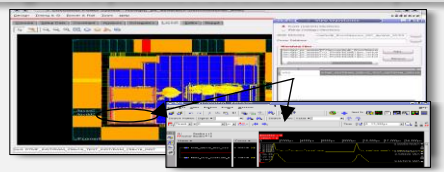
- Assessing power routing schemes at floorplan stage
- Fast power-grid rail resizing
- What-if analysis for power-grid optimization

Signoff Static Power & Rail Analysis



- Static power analysis: leakage, internal, and switching power
- Static rail analysis to check IR-drop and electromigration violations on power-grid; power switch analysis

Signoff Dynamic Power & Rail Analysis



- Dynamic power analysis: vector based or vectorless
- Dynamic power analysis for decap optimization, power switches optimization, power shutoff analysis

Power Integrity Solution

IR drop and electromigration

Power calculation

Decap power switch

IR-aware STA

Early rail analysis

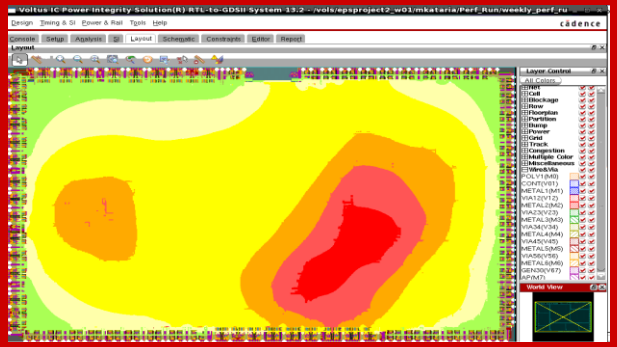
Chip-PKG-PCB

Performance

Integration

Capacity

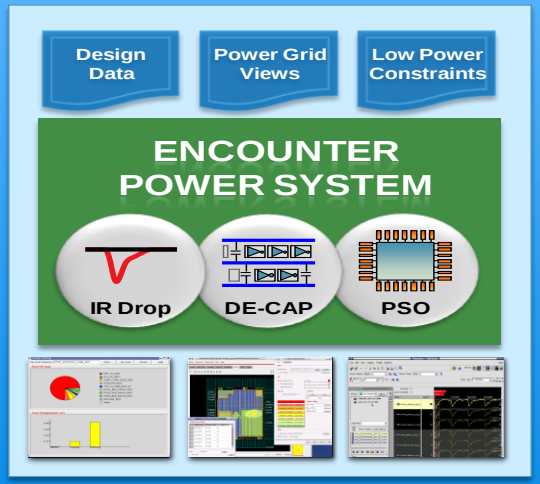
Accuracy



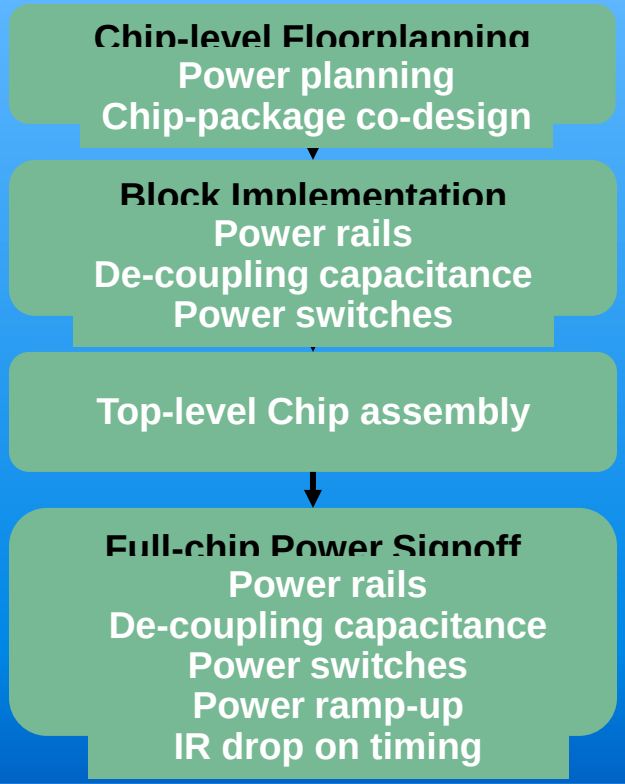
Comprehensive static and dynamic power analysis

- **Complete full chip power analysis**
  - Highest capacity and performance
  - Flat, hierarchical, hybrid power/IR drop
  - Static, dynamic, vector, vectorless, CPF-driven
  - Gate-level, instance, pwr grid, GUI debug
- **Integrated with EDI System and ETS**
  - Better convergence and productivity
  - Early rail analysis, power network optimization, decap opt, power switch opt
  - Full physical/logical/analysis, rapid ECOs
  - Sign-off quality timing and power analysis built-in
  - Power impacts on delay/timing/skew/clock
- **Advanced technologies**
  - Easy to generate library models with transistor-level accuracy
  - Thermal, variation aware, EM, ESD, DFM
  - Statistical leakage power analysis
- **Certified for Signoff**
  - Qualified for signoff at all nodes by TSMC, SMIC, IBM, Chartered, Samsung, etc.
  - Certified by all major ASIC and IP providers

Reference Flow 11

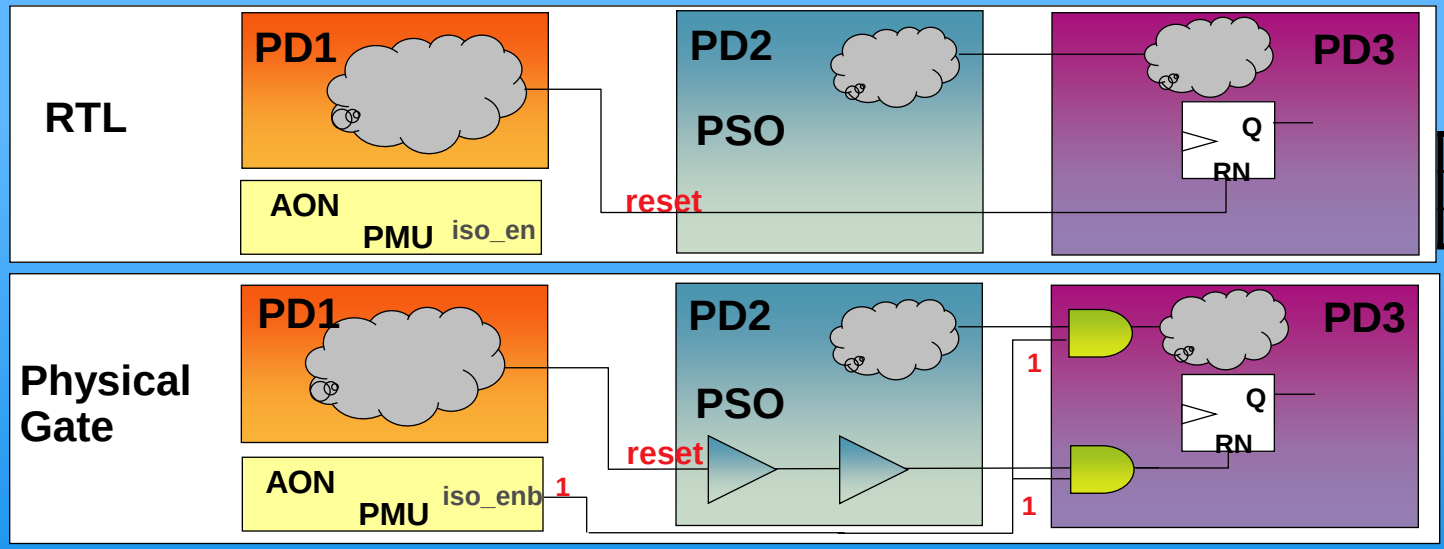


Signoff Flow Chart for Low Power Design



- Early planning stages (early rail analysis)
  - Validate chip-level power delivery
  - Optimize power-grid design (grid, tree …)
  - Estimate de-coupling capacitance
- Block implementation
  - Optimize and validate power-grid within block
  - Results drive block-level optimization
    - De-coupling capacitance
    - Power switches
- Full-chip signoff
  - Most accurate analysis includes full details
  - STA drives vectorless dynamic analysis
  - Validates all aspects of power delivery

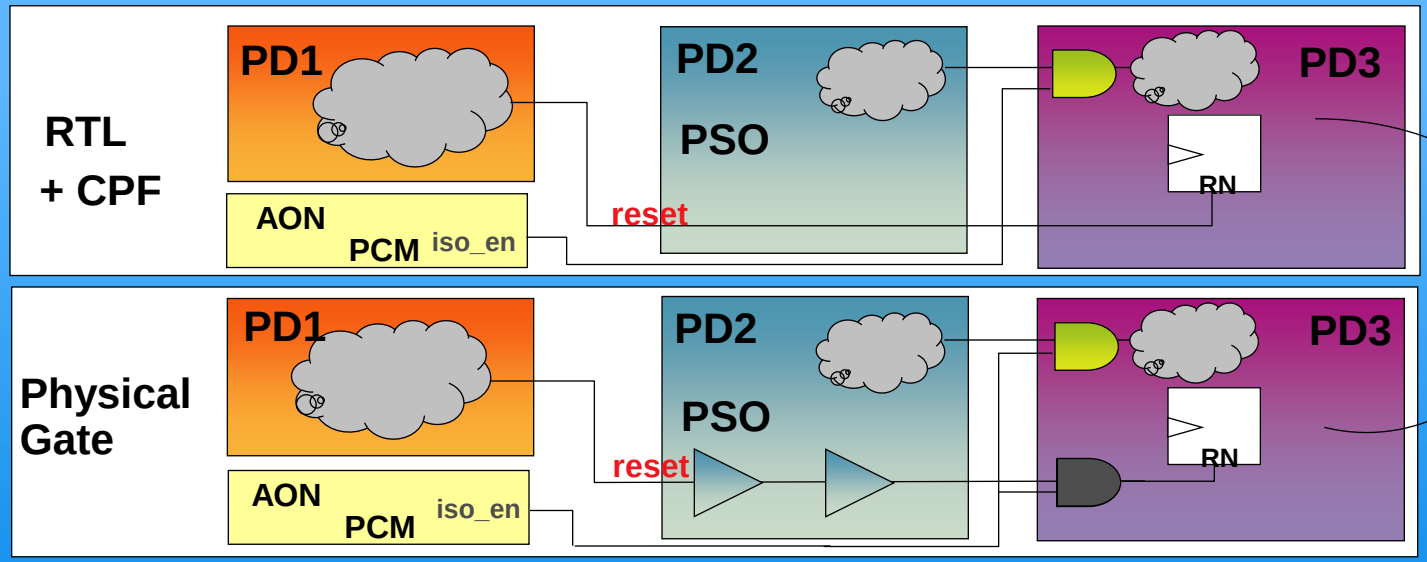
Ad-hoc Equivalence Checking



Mode	PD1	PD2	PD3
PM1	1.0	1.0	1.0
PM2	1.0	0.0	1.0

- RTL does not have low power logic inserted
  - `create_isolation_rule r1 -from PD2 -to PD3 -isolation_condition {i_pmu/iso_enb} -isolation_output low`
- Place and Route Step
  - Buffers inserted on reset line in PD2; Isolation inserted in PD3 based on CPF isolation rule
- Ad-hoc EC
  - iso_en='1' signal to disable isolation logic; Reports design is equivalent
- In fact, it is not equivalent because reset behavior changes when PD2 is off and PD3 is on
  - Feedthrough reset signal should not be isolated

Power Aware Equivalence Checking



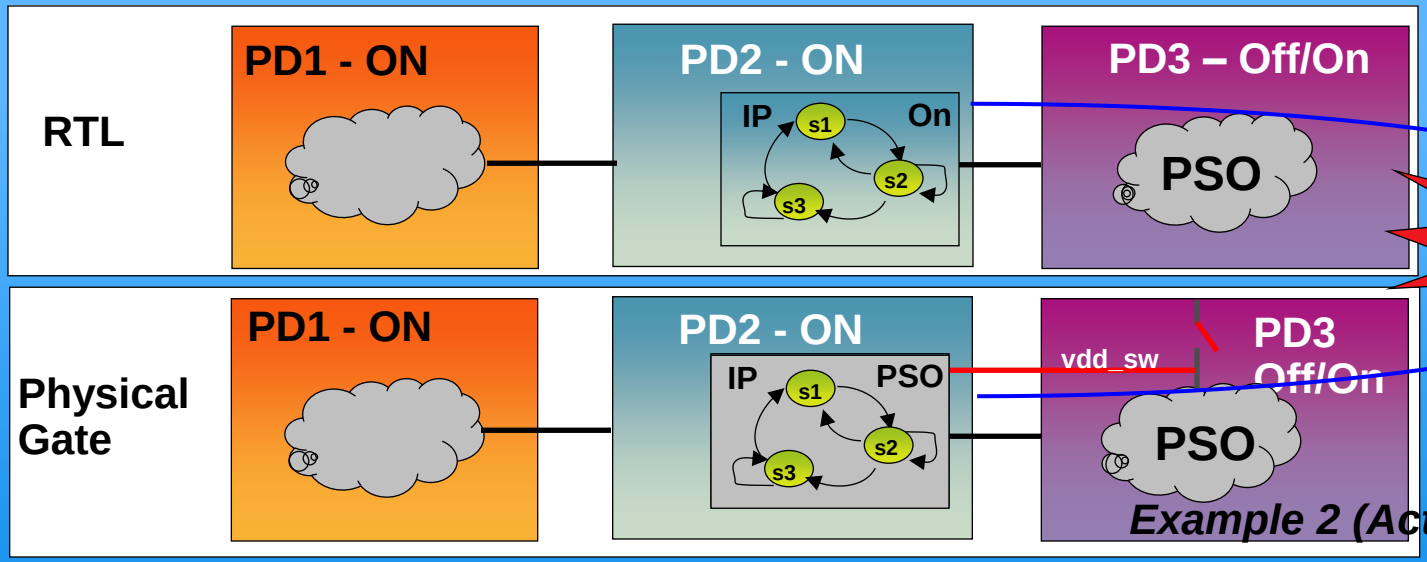
Mode	PD1	PD2	PD3
PM1	1.0	1.0	1.0
PM2	1.0	0.0	1.0

- EC tool inserts isolation logic per isolation rule

```
create_isolation_rule r1 -from PD2 -to PD3 -isolation_condition {i_pmu/iso_enb} \
-isolation_output low
```

- Place and Route Step
  - Buffers inserted on reset line in PD2; Isolation inserted in PD3 based on CPF isolation rule
- RTL2Gate CLP EC reports design is non-equivalent

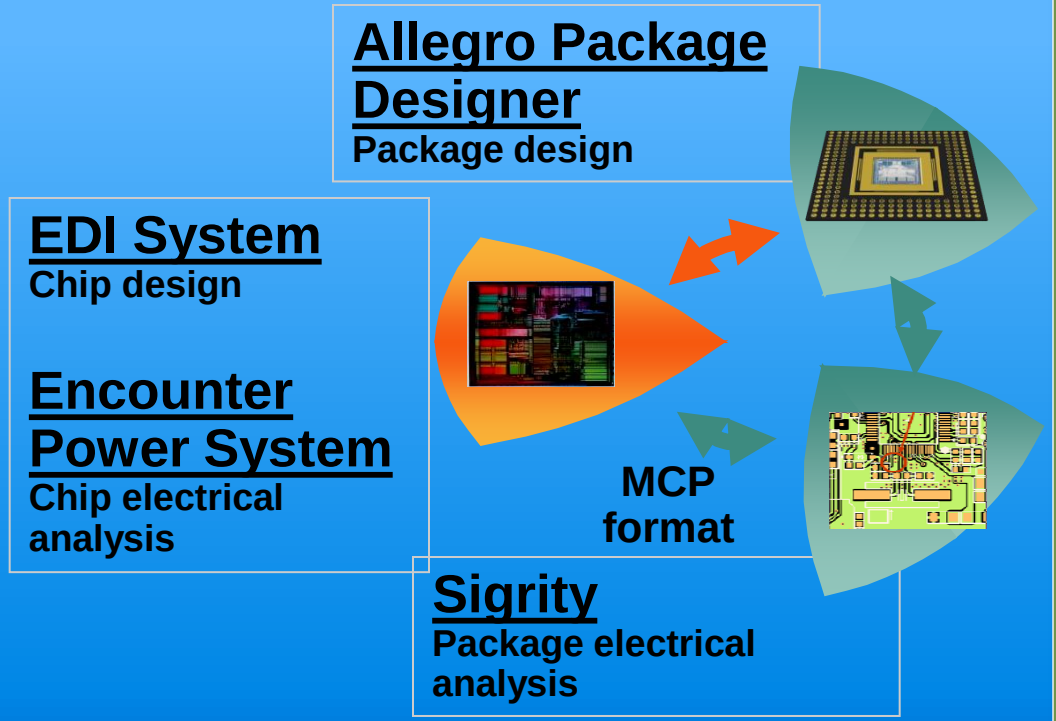
The Need For Domain Aware Equivalence Checking



Mode	PD1	PD2	PD3
PM1	1.0	1.0	1.0
PM2	1.0	1.0	0.0

- IP block in PD2 was connected incorrectly to PD3 switchable power net *vdd_sw* during PnR instead of PD2 primary power net
- When PD3 is shut off, registers in IP block will lose state in silicon
- Domain Aware equivalence checking finds this problem
  - Customer used Ad-hoc equivalence checking flow did not run CLP EC

Cadence Chip-Package Co-Design



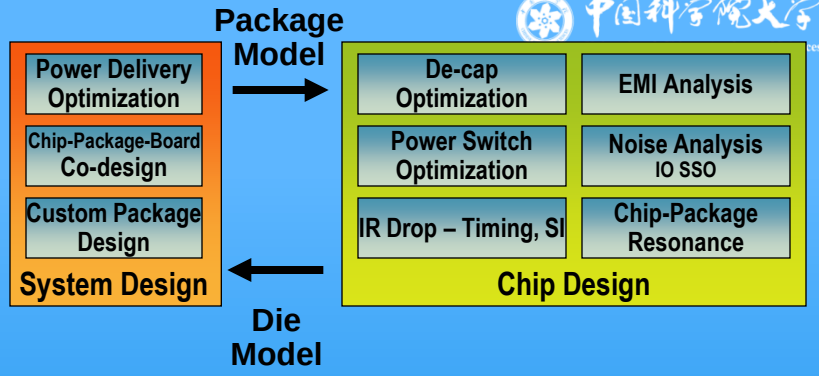
Chip-Package-Board data transfer using Model Connection Protocol (MCP) format (open format based on SPICE)

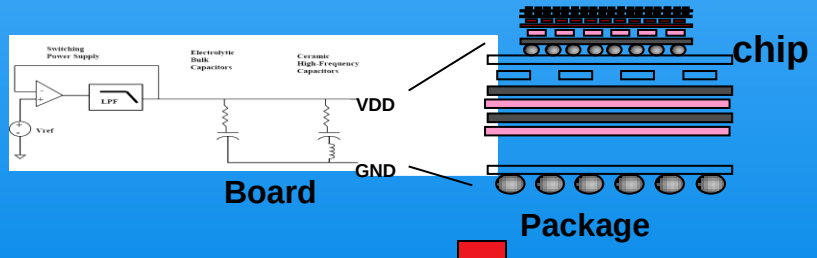
- **Power delivery management**
  Ensures clean power from source, through board, package, die and down to transistors
- **Signal Integrity management**
  Ensures signals from/to chip-package-board arrive in time and without loss of integrity
- **Noise management**
  Ensures on-chip noise sources do not negatively impact end-application function (IR drop, IO SSO, block power up …etc…)
- **Thermal and power management**
  On-chip thermal hotspots, which must be efficiently dissipated through package/board

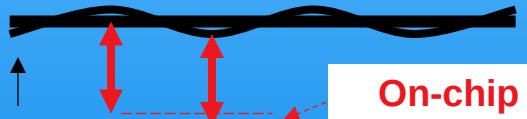
Chip-Package Co-design

Die and package models

- Chip design
  - Package model ➔ accurate on-chip analysis
- **Package design**
  - **Die model ➔ optimize the package**

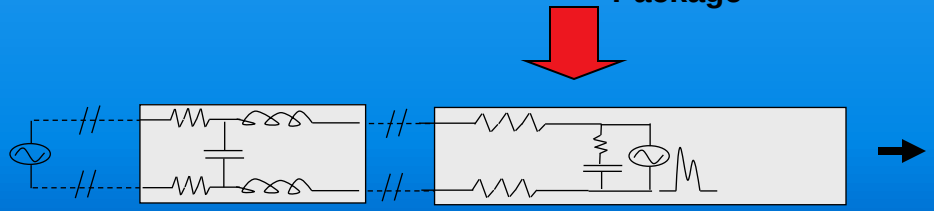


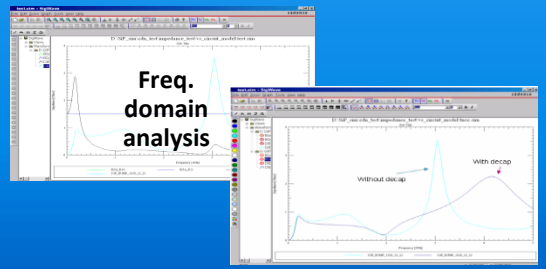




di/dt event

On-chip IR drop increased by resonance



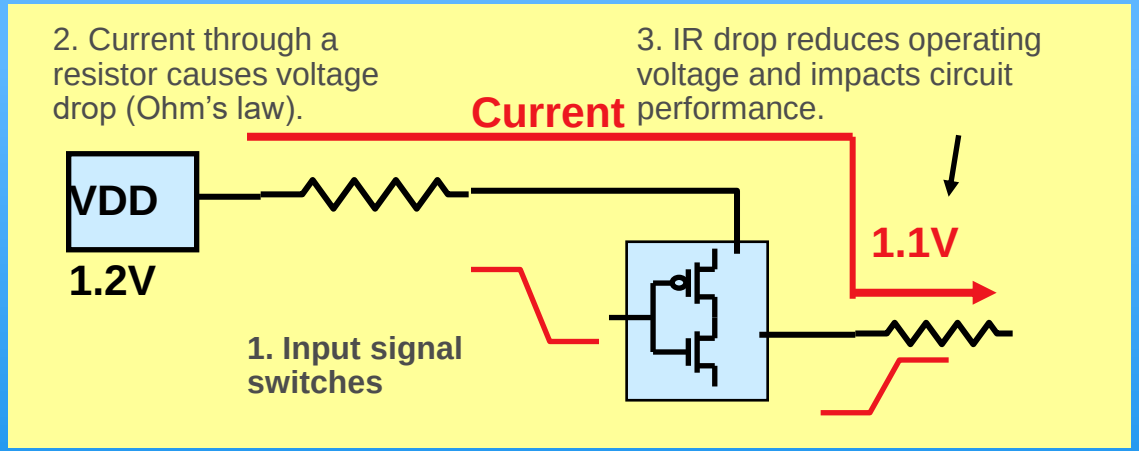


Low Power Design

- Low Power Design in Advanced Nodes
- Low Power Design and Its Verification
- Implementation of Low Power Design
- Power Integrity and Power Analysis
- Discussion

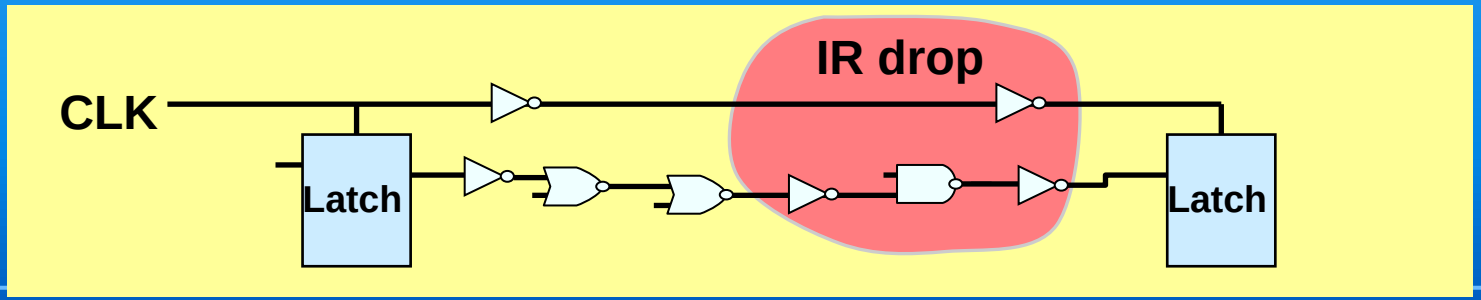
IR Drop Impacts Timing Unpredictably

- **IR-drop impact on timing**
  - IR drop can lead to timing violations caused by skew introduced on both signal nets and clock nets.
  - IR drop typically increases delay, but in some situations can decrease delay.

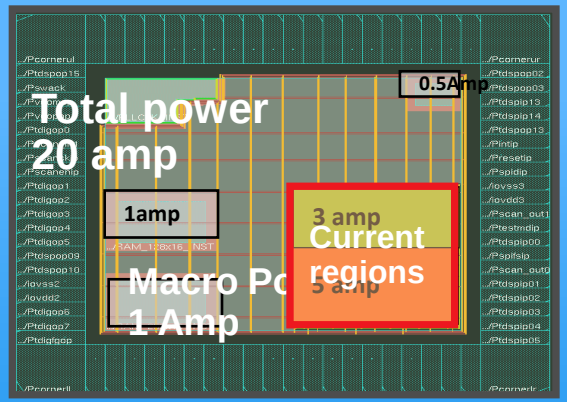


Impact is design dependent

- Clock skew increases more than signal skew (hold-time violations).
- Signal skew increases more than clock skew (setup-time violations).

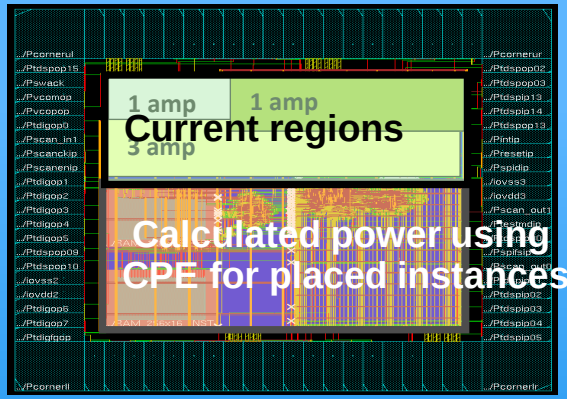


Early Rail Analysis: Static Power and Rail Analysis



Floorplanning and power-planning stage

- Imagine power distribution using current regions.
- Apply current sinks interactively on the desired layer.
- Estimate IR drop and optimize power pads location.
- Refine power grid using EDI.



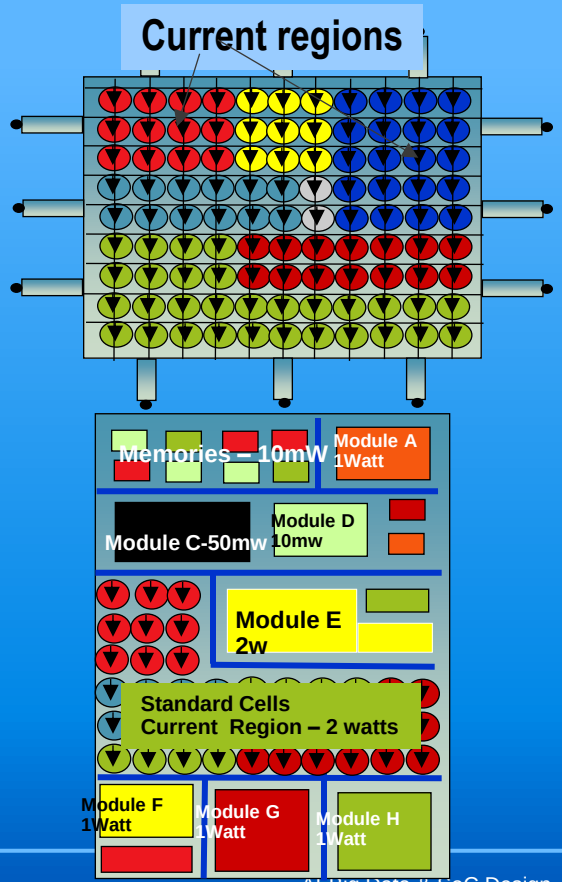
Placement and routing stage

- Imagine power distribution using current regions (unplaced).
- Calculate power using Common Power Engine (placed region).
- Virtual power-grid connectivity to placed instances.
- Scale currents for hierarchy and placed macros.
- Power gate analysis and optimization with ECO.
- Optional power-grid libr support (w/ Voltus license).
- Refine placement and power grid using EDI.
- Refine power pad placement based on IR drop.

Early Rail Analysis: Dynamic Analysis Feature List

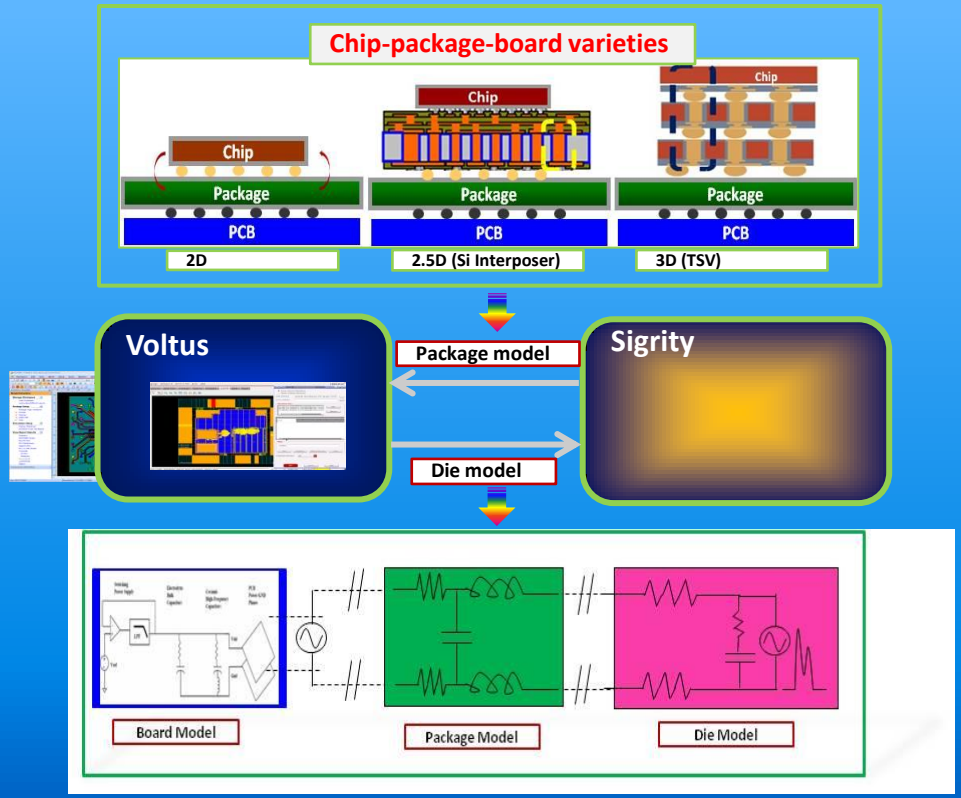
- Voltus rail analysis engine and Voltus power engine integration
- Uses EDI native extractor for fast power-grid extraction
- Available with EDI L license
- Checks out Voltus license when running dynamic early rail analysis

- Dynamic analysis supports:
  - Package analysis and die model generation
  - Decap analysis and ECO
  - Power gate steady-state analysis and ECO
  - Dynamic PWL current regions with intrinsic and loading capacitance specification
  - Estimated loading capacitance and gate capacitance in a region
  - Multi-threaded solver in local mode
  - On-chip voltage regulator
  - CPF



Chip-Package-Board Co-simulation

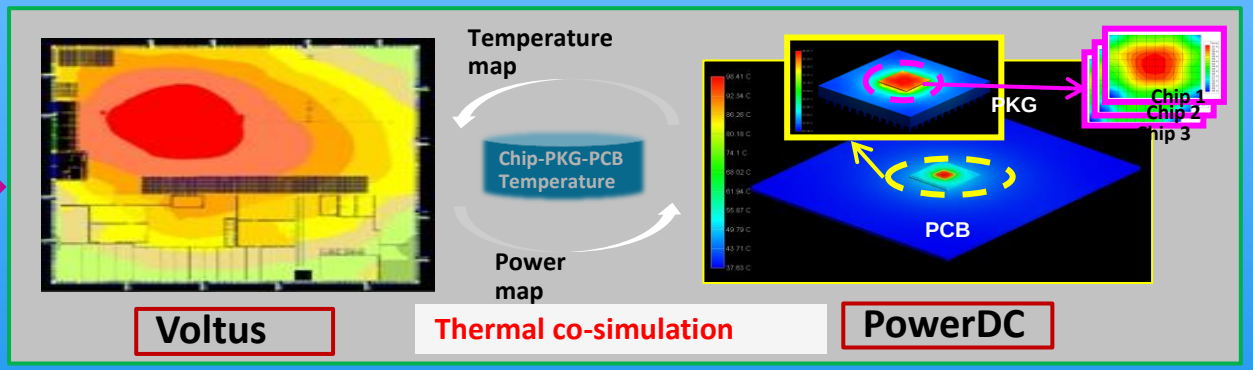
Integrated Voltus and Sigrity design flows



- Sigrity package model generation
  - XtractIM: broadband SPICE format
  - PowerSI: S-parameter format
- Voltus die model generation
  - Broadband SPICE format
  - Frequency and time domains
  - Single-port and N-port (up to 100s)
- Sigrity MCP interface
  - Model Connection Protocol
  - Name- based or location-based
- Complete power integrity solutions
  - Chip: Voltus + package model
  - System: PowerDC + die model

Electrical-Thermal Co-simulation

TSMC 3DIC reference flow



- Thermal runaway
  - Positive feedback among chip's Temperature, leakage, and power dissipation
  - Temperature dependent IR-drop and electromigration
- Thermal simulation in Voltus + PowerDC
  - Voltus output: temperature and location dependent Power Map file.
  - PowerDC computes detailed temperature distribution for Chip-PKG-PCB (T vs. time).
  - Voltus reads back temperature map file for EMIR convergence.
  - Thermal view available in 2D and 3D.