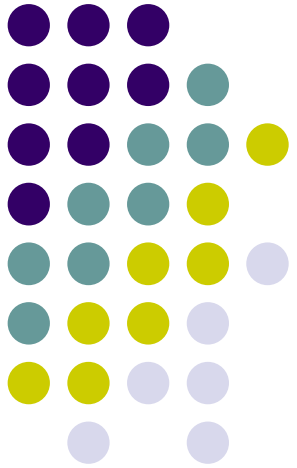
# 超大规模集成电路基础

# Fundamental of VLSI

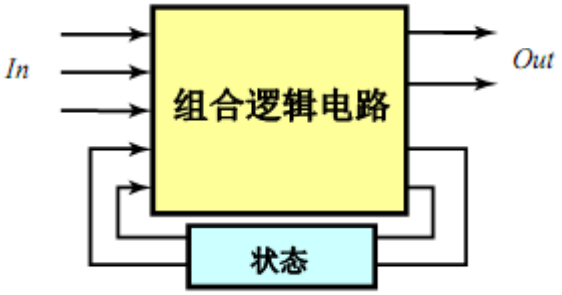
## 第六章 CMOS 组合逻辑电路设计



# 组合逻辑与时序逻辑

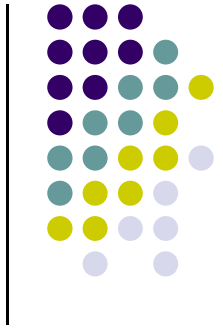
- 组合逻辑电路
  - 电路的输出信号是电路的输入信号的逻辑关系表示
- 时序电路
  - 电路的输出信号不仅决定于当前的输入信号，而且还决定于先前的输入信号


组合逻辑电路




时序电路

# 逻辑门



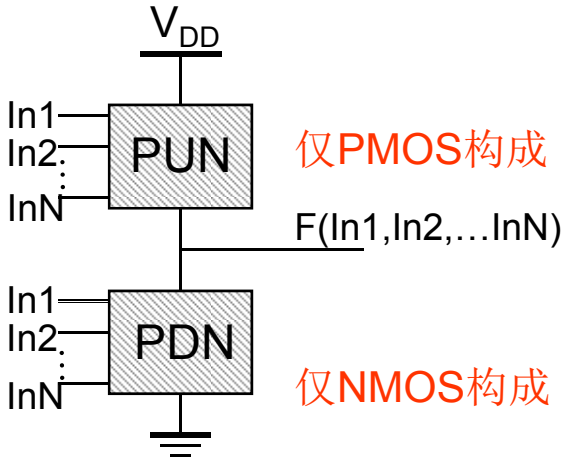
- 逻辑门
  - 由器件组合而成，实现一个特定逻辑函数的电路
- 评价逻辑门的设计指标
  - 面积
  - 速度
  - 能量
  - 功率
  - 抗噪声能力

# 静态互补CMOS电路

- 静态互补CMOS电路
  - 由静态CMOS反相器扩展而成的电路
- 静态互补CMOS电路特点
  - 每个门的稳态输出总是通过低阻连至$V_{DD}$和GND
  - 稳态时，门的输出值总是由电路所实现的布尔函数决定
  - 与动态电路相反，动态电路的信号是暂时存储在电路节点电容上的

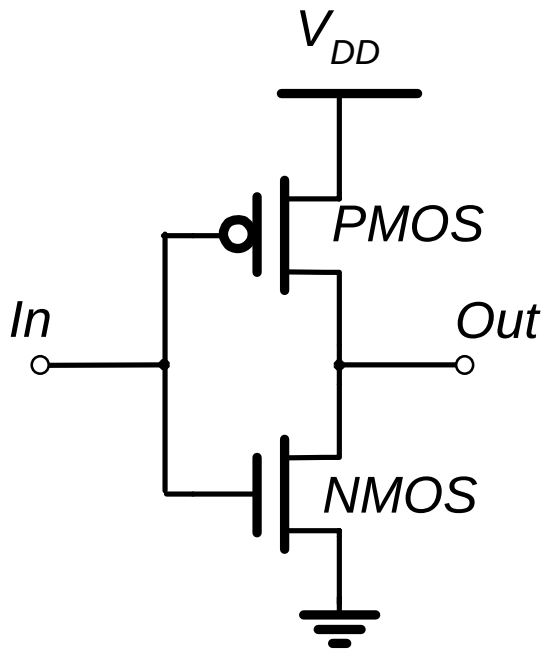
# 静态互补CMOS电路

- 静态互补CMOS门是上拉网络（PUN）和下拉网络（PDN）的组合
  - PUN网络：当输出意味着逻辑1时，把输出和$V_{DD}$之间建立通路
  - PDN网络：当输出意味着逻辑0时，把输出和GND之间建立通路
  - PUN和PDN网络以互相排斥的方式工作的，即在稳定状态下两个网络只有一个导通



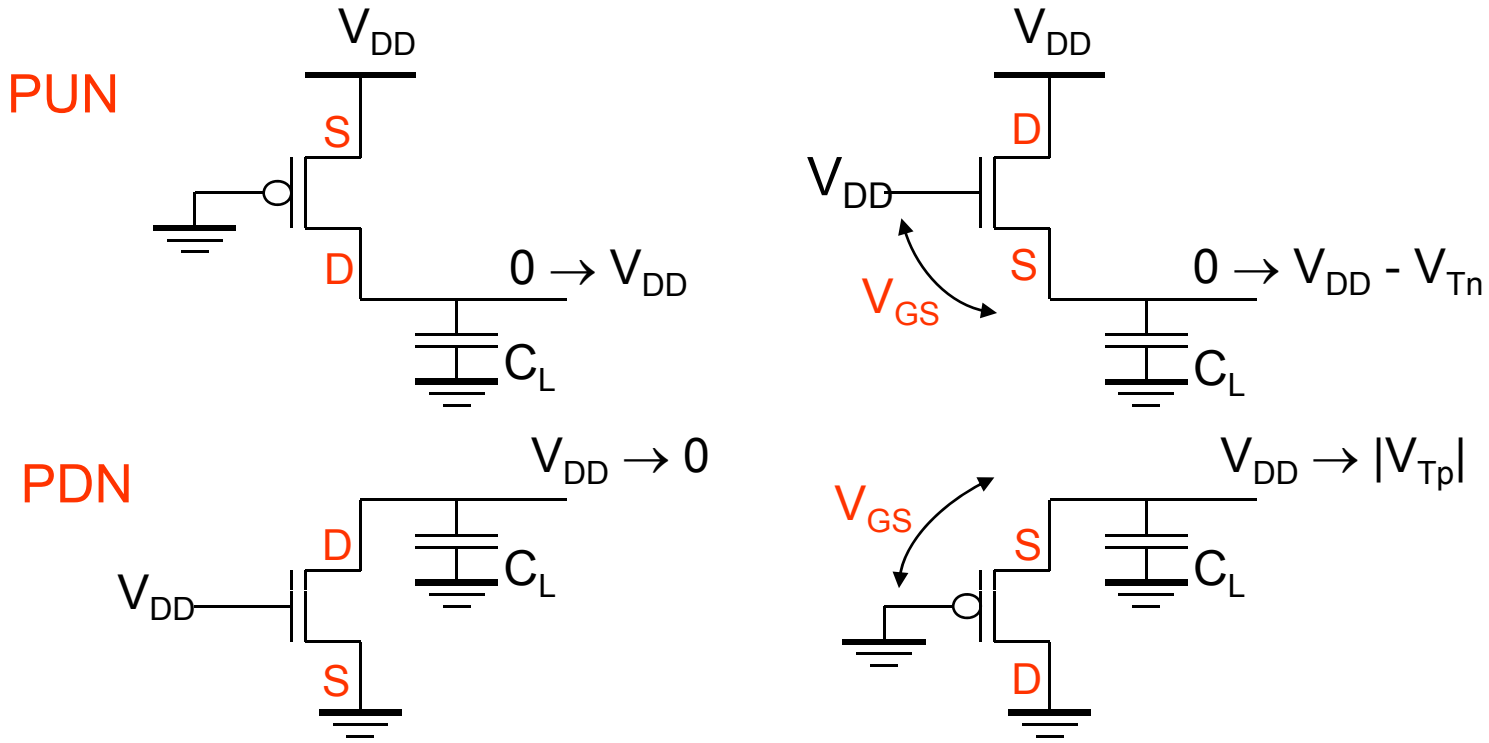
# 静态互补CMOS电路

- 晶体管可以看成由栅信号控制的开关
  - NMOS：
    - 栅控制信号高，开关闭合
    - 栅控制信号低，开关断开
  - PMOS：
    - 栅控制信号高，开关断开
    - 栅控制信号低，开关闭合



# 静态互补CMOS电路

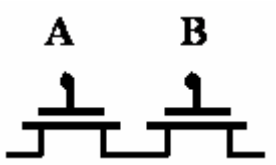
- 阈值损失
  - PDN由NMOS构成，NMOS产生强0
  - PUN由PMOS构成，PMOS产生强1



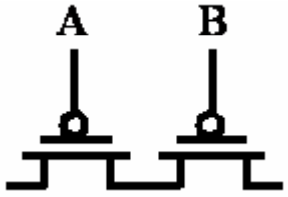
# 静态互补CMOS电路

- 静态互补CMOS逻辑功能实现规则

晶体管串联

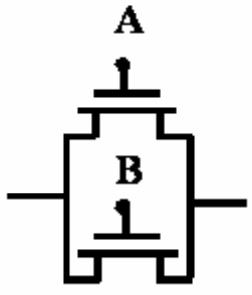



$A \bullet B = 1$ 导通

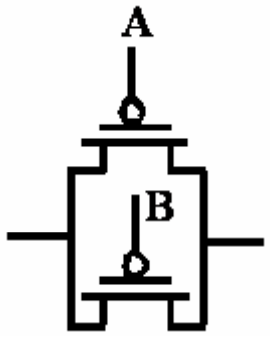



$\overline{A} \bullet \overline{B} = 1$ 导通

晶体管并联




$A + B = 1$ 导通




$\overline{A} + \overline{B} = 1$ 导通

# 静态互补CMOS电路

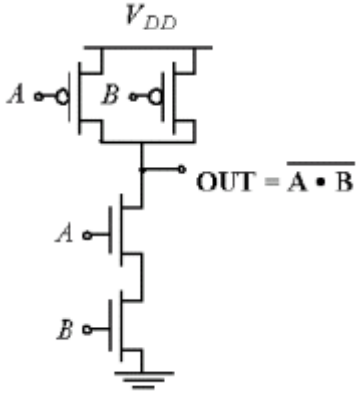
- De Morgan定理

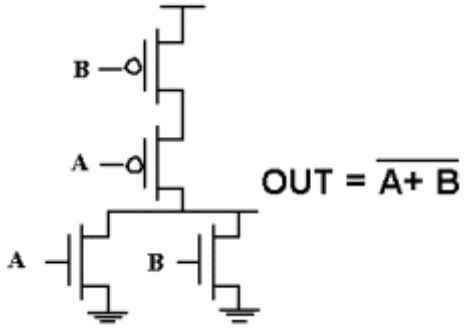
$$\overline{A} \bullet \overline{B} = \overline{A + B} \qquad \overline{A} + \overline{B} = \overline{A \bullet B}$$

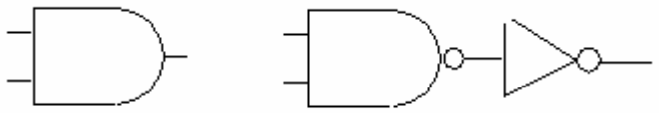
- 静态互补CMOS电路的对偶关系
  - PUN网络并联的晶体管相应于PDN网络串联的晶体
  - 反之亦然

| PUN | PDN |
|---|---|
| $\overline{A} \bullet \overline{B}$ | $A + B$ |
| $\overline{A} + \overline{B}$ | $A \bullet B$ |

- 互补门的本质是反向的



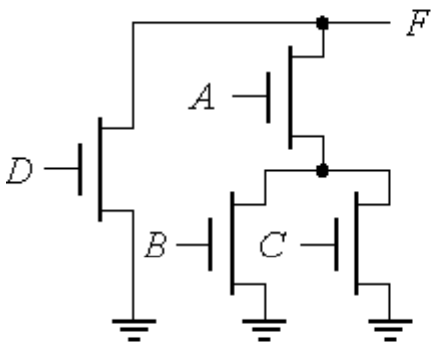



$AND = INV(NAND)$

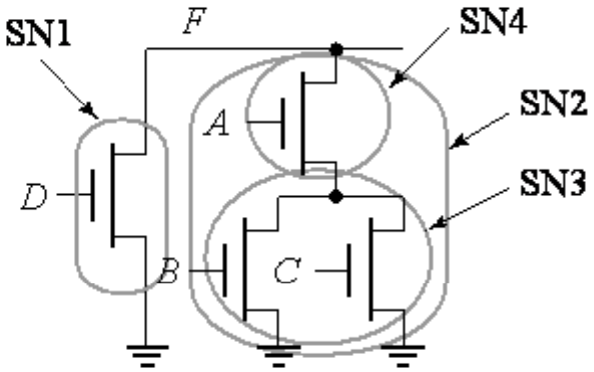
# 静态互补CMOS电路

- 构建CMOS复合门

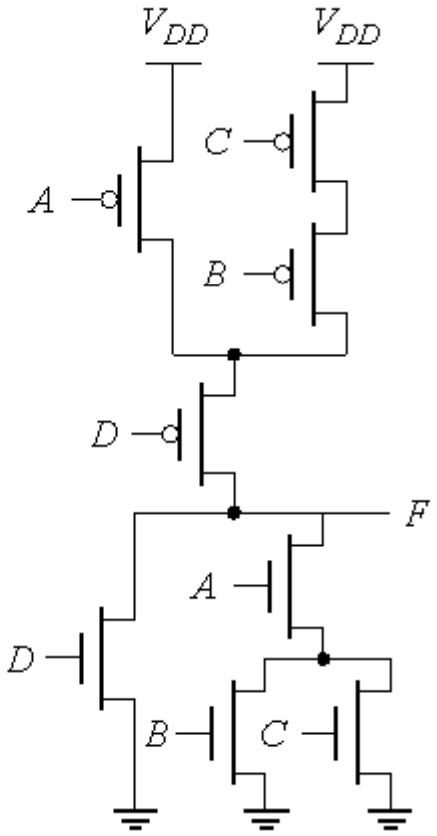
$$OUT = \overline{D + A(B + C)}$$




(a) PDN



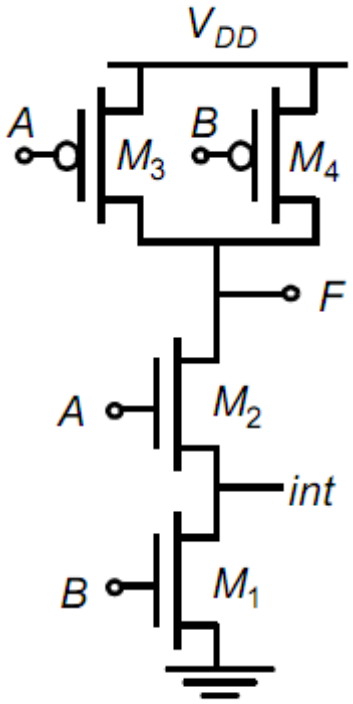

(b)通过识别电路中层次关系的子网络推导出PUN

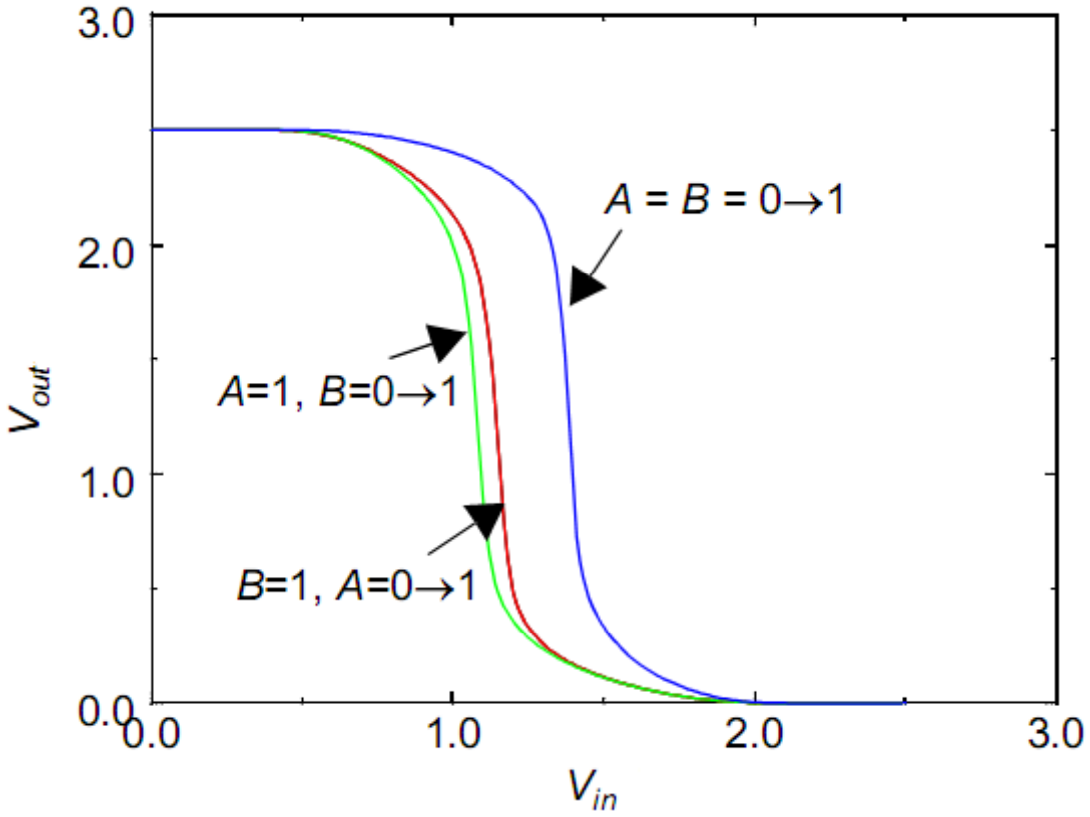



(c)完整的互补CMOS电路

# 静态互补CMOS电路

- 静态特性
  - 集成了静态CMOS反相器的所有优点
  - VTC如输入信号的模式有关

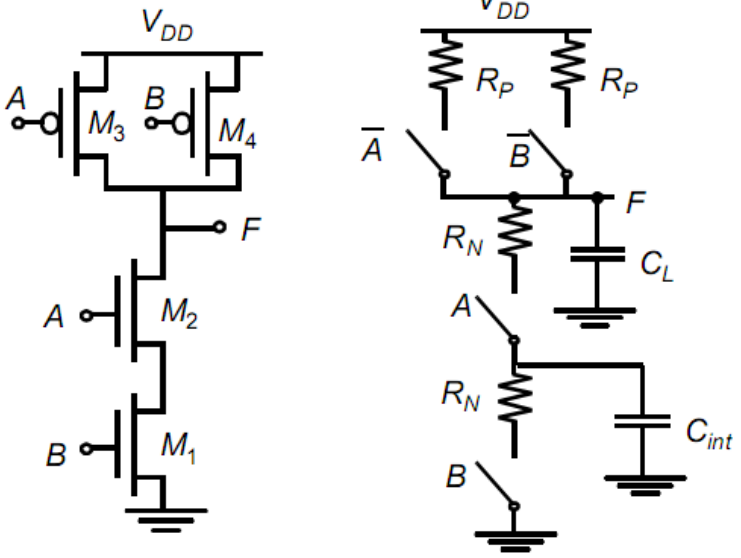


# 静态互补CMOS电路

- 动态特性
  - 延时与输入信号的模式有关
  - $t_{pLH}$ $A=1\rightarrow 0$ *and* $B=1\rightarrow 0;\ t_{pLH}=0.69(R_p/2)C_L$

    $A=1\rightarrow 0$ *or* $B=1\rightarrow 0;\ t_{pLH}=0.69R_pC_L$
  - $t_{pHL}$ $A=0\rightarrow 1$ *and* $B=0\rightarrow 1;\ t_{pHL}=0.69(2R_N)C_L$

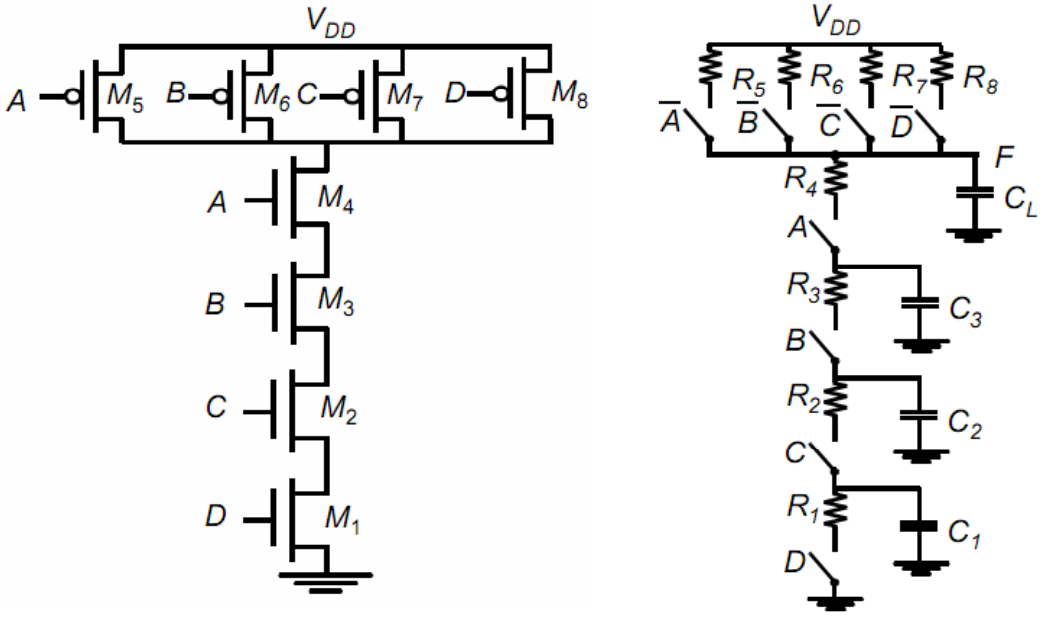


# 静态互补CMOS电路

- 动态特性
  - 考虑内部节点电容的分布式RC模型
    - 四输入NAND门的Elmore传播延时

$$t_{pHL} = 0.69\left(R_1C_1 + \left(R_1+R_2\right)C_2 + \left(R_1+R_2+R_3\right)C_3 + \left(R_1+R_2+R_3+R_4\right)C_L\right)$$

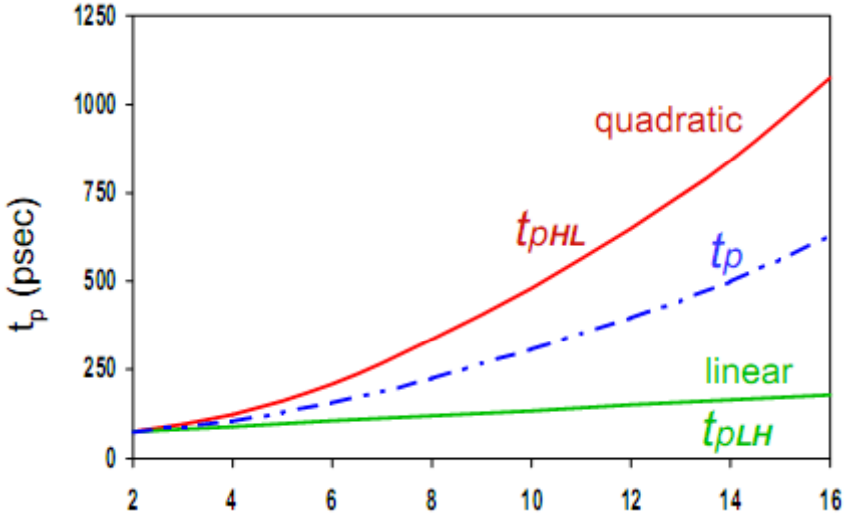
$$t_{pHL} = 0.69R_N\left(C_1 + 2C_2 + 3C_3 + 4C_L\right)$$



# 静态互补CMOS电路

- 动态特性
  - 考虑内部节点电容的分布式RC模型
    - 扇入影响
      - N个输入需要2N个晶体管
      - 由高至低本征延时最坏情况是扇入数的二次函数

$$t_{pHL} = 0.69R_N\left(C_N + 2C_N + \cdots + NC_N\right) = 0.69R_N C_N \frac{N\left(N+1\right)}{2}$$



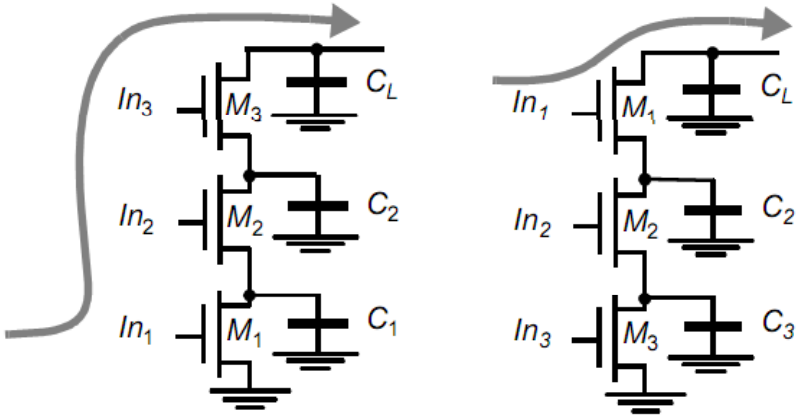
# 静态互补CMOS电路

- 动态特性
  - 大扇入时的设计技术
    - 调整晶体管尺寸
    - 逐级加大晶体管尺寸

$$t_{pHL} = 0.69\left(R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + (R_1+R_2+R_3+R_4)C_L\right)$$

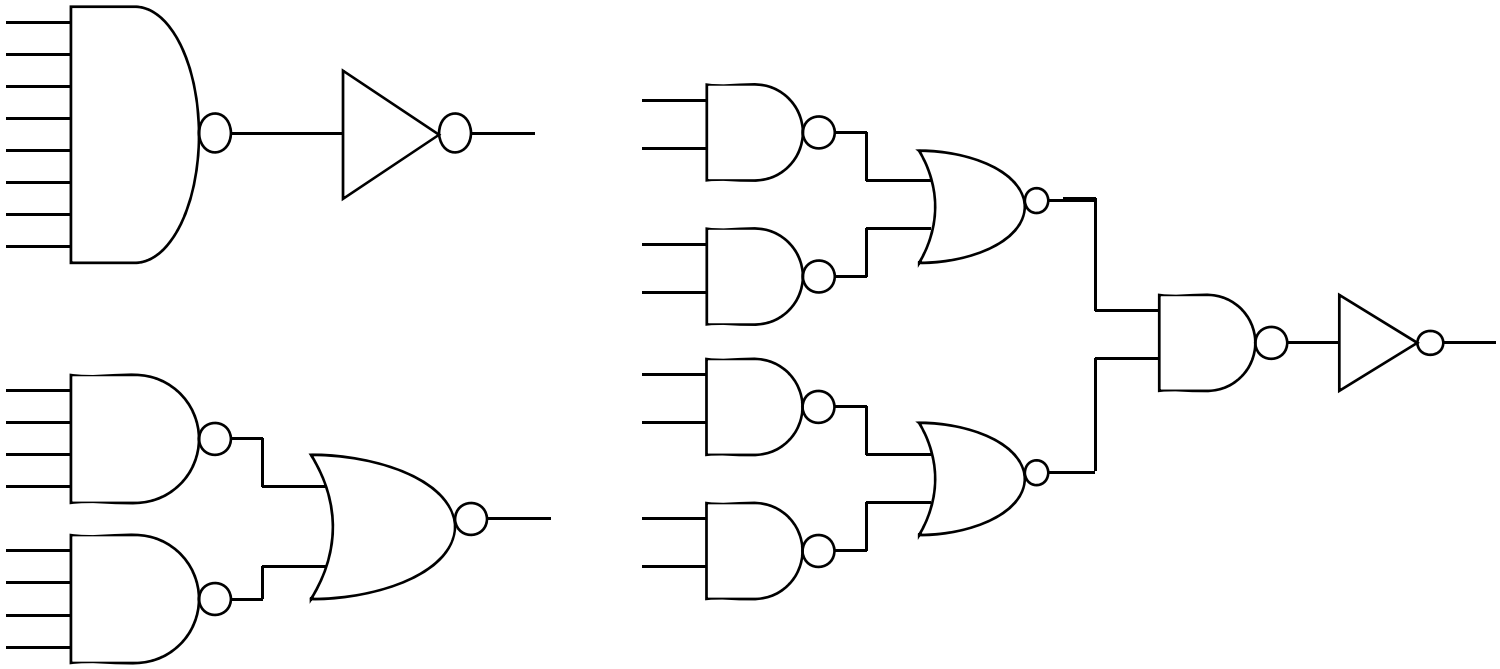
$$R_1 < R_2 < R_3 < R_4$$

    - 重新安排晶体管次序
      - 使关键路径上的延迟最低
      - In1为关键信号
      - In2=1，In3=1，In1: 0->1



# 静态互补CMOS电路

- 动态特性
  - 大扇入时的设计技术
    - 重组逻辑结构



# 静态互补CMOS电路

- 组合逻辑电路中的性能优化

$$t_p = t_{p0}\left(1+\frac{C_{ext}}{\gamma C_g}\right) = t_{p0}\left(1+\frac{f}{\gamma}\right)$$

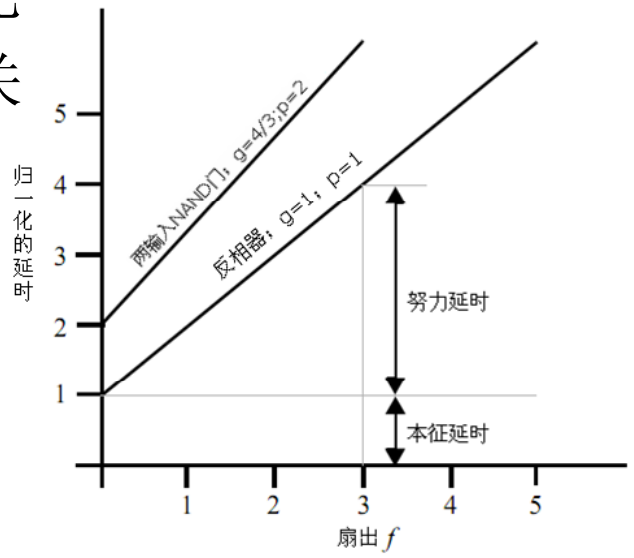
考虑复合门情况修改为

$$t_p = t_{p0}\left(p+gf/\gamma\right)$$

p代表该复合门和简单反相器的本征延时比

g称为逻辑努力，只与电路的拓扑结构有关

h=gf称为门努力



# 静态互补CMOS电路

- 组合逻辑电路中的性能优化

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{p0} \sum_{j=1}^{N} \left( p_j + \frac{f_j g_j}{\gamma} \right)$$

求$t_p$关于$C_{g,j}$的导数可得最小延时的约束条件

$$C_{g,j+1} / C_{g,j} = C_{g,j} / C_{g,j-1}$$

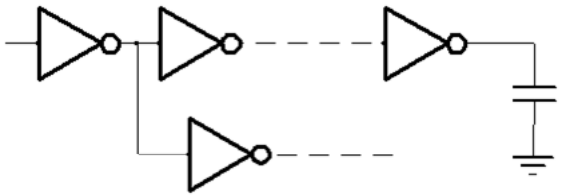
$$f_1 g_1 = f_2 g_2 = \cdots = f_N g_N$$

路径逻辑努力：沿电路中一条路径的总逻辑努力可以通过把这条路径上所有门的逻辑努力相乘求得

$$G = \prod_{1}^{N} g_i$$

逻辑门的分支努力

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$



路径分支努力

$$B = \prod_{1}^{N} b_i$$

# 静态互补CMOS电路

- 组合逻辑电路中的性能优化

  路径逻辑努力与各级电器努力和分支努力间的关系

$$F = \prod_{1}^{N} \frac{f_i}{b_i} = \frac{\prod f_i}{B} \qquad b = \frac{C_{on-path} + C_{off-path}}{C_{gin}}$$

  总路径努力

$$H = \prod_{1}^{N} h_i = \prod_{1}^{N} g_i f_i = GFB$$

  使路径延时最小的门努力为：

$$h = \sqrt[N]{H}$$

  通过该路径的最小延时为：

$$D = t_{p0}\left(\sum_{j=1}^{N}\left(p_j + \frac{N\sqrt[N]{H}}{\gamma}\right)\right)$$

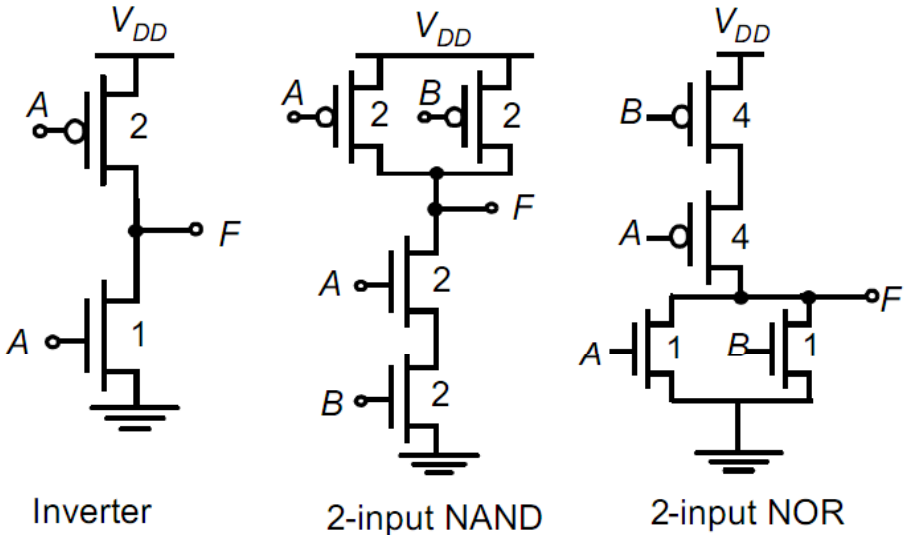
  逻辑链中各门的尺寸确定

$$g_2 s_2 C_{ref} = \left(\frac{f_1}{b_1}\right) g_1 s_1 C_{ref} \qquad s_i = \frac{g_1 s_1}{g_i} \prod_{j=1}^{i-1}\left(\frac{f_j}{b_j}\right)$$

# 静态互补CMOS电路

- 复合门的逻辑努力

| Gate Type | Number of Inputs | | | |
|---|---|---|---|---|
| | 1 | 2 | 3 | n |
| Inverter | 1 | | | |
| NAND | | 4/3 | 5/3 | (n+2)/3 |
| NOR | | 5/3 | 7/3 | (2n+1)/3 |
| Multiplexer | | 2 | 2 | 2 |
| XOR | | 4 | 12 | |




Inverter　　2-input NAND　　2-input NOR

# 静态互补CMOS电路

- 组合逻辑电路中的性能优化
  - CMOS逻辑门中的功耗
    - 动态功耗

$$\alpha_{0\to1} C_L V_{DD}^2 f$$

    - 开关活动性$\alpha_{0\to1}$与逻辑电路拓扑结构的静态部分和电路时序特性的动态部分有关

$$\alpha_{0\to1} = p_0 p_1 = p_0(1-p_0)$$

假设输入是独立并且均匀分布的

$$\alpha_{0\to1} = \frac{N_0}{2^N}\frac{N_1}{2^N} = \frac{N_0\left(2^N - N_0\right)}{2^{2N}}$$

$$\alpha_{0\to1} = \frac{N_0}{2^N}\frac{N_1}{2^N} = \frac{N_0\left(2^N - N_0\right)}{2^{2N}} = \frac{3\left(2^2 - 3\right)}{2^4} = \frac{3}{16}$$

两输入NOR门真值表

| *A* | *B* | *Out* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

# 静态互补CMOS电路

- 组合逻辑电路中的性能优化
  - CMOS逻辑门中的功耗

    如果输入服从某种统计特性

    两输NOR入门，令$p_a$和$p_b$为输入A和B分别等于1的概率，并且输入A和B不相关，则输出节点为1的概率为

$$p_1 = (1-p_a)(1-p_b)$$

    因此，由0至1的翻转的概率为：

$$\alpha_{0\to1} = p_0 p_1 = \left(1-(1-p_a)(1-p_b)\right)(1-p_a)(1-p_b)$$

| | $\alpha_{0\to1}$ |
|---|---|
| **AND** | $(1-p_A p_B)p_A p_B$ |
| **OR** | $(1-p_A)(1-p_B)[1-(1-p_A)(1-p_B)]$ |
| **XOR** | $[1-(p_A+p_B-2p_A p_B)](p_A+p_B-2p_A p_B)$ |

# 静态互补CMOS电路

- 组合逻辑电路中的性能优化
  - CMOS逻辑门中的功耗
    - 考虑信号间的相关性

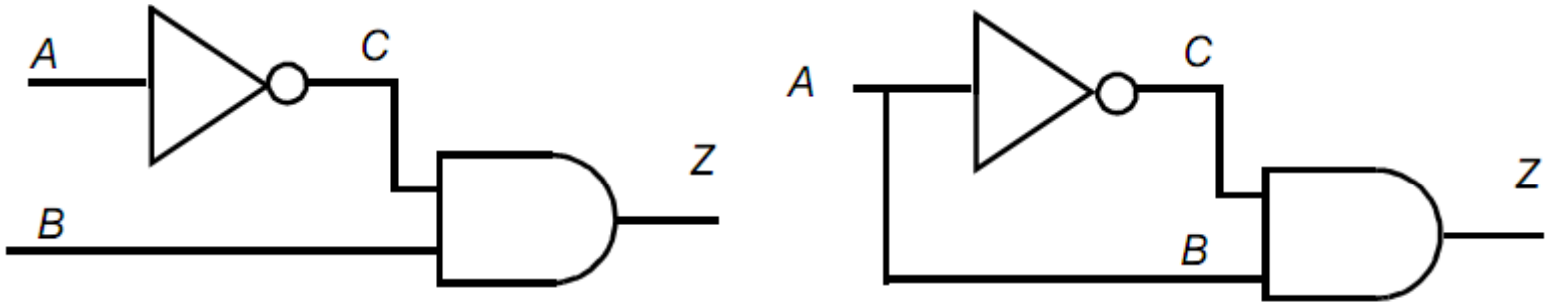
      AND门的输出翻转概率，假设输入信号是独立的

      $$\alpha_{0\to1} = (1 - p_a p_b)\, p_a p_b = (1 - 1/2 \cdot 1/2)\, 1/2 \cdot 1/2 = 3/16$$

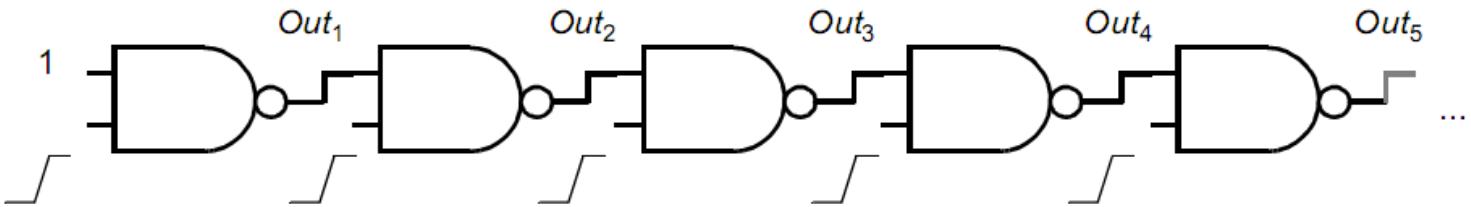
      如果输入信号是相关的，则需使用条件概率计算

      $$p_Z = p(Z = 1) = p(B = 1, C = 1)$$

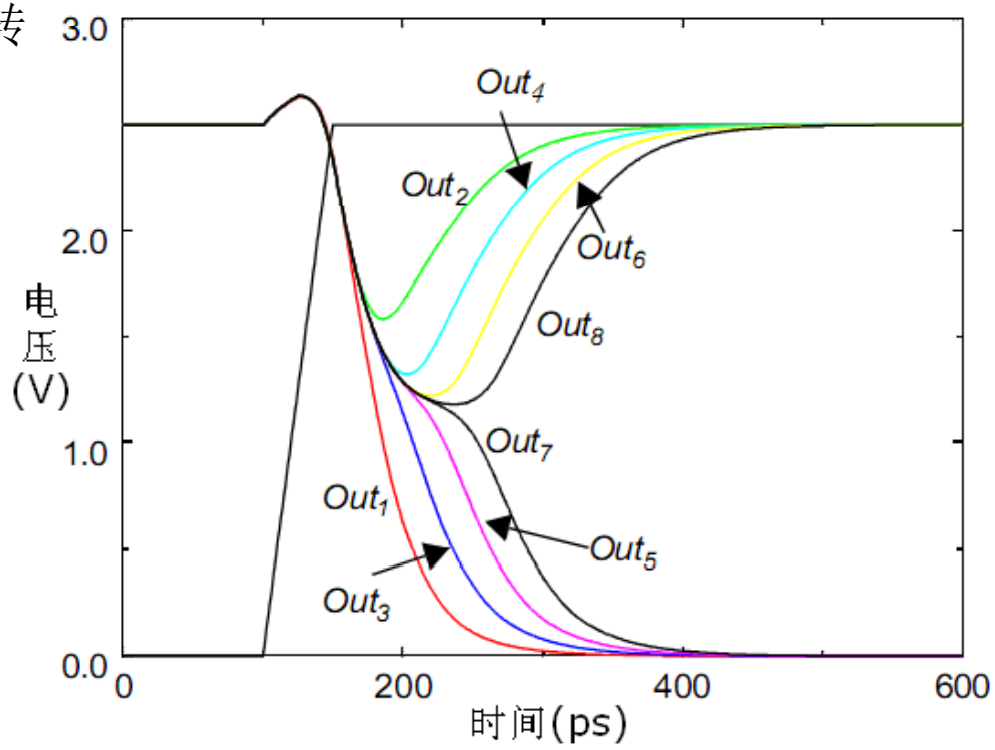
      $$p_Z = p(C = 1 \mid B = 1)\, p(B = 1)$$



# 静态互补CMOS电路

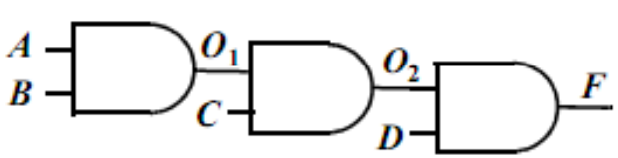


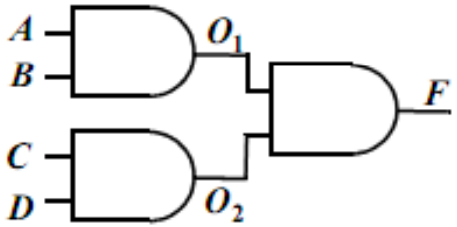

- 动态或虚假翻转
  - 毛刺：在一个周期内一个节点在稳定到正确的逻辑电平之间可以出现多次翻转



# 静态互补CMOS电路

- 组合逻辑电路中的性能优化
  - 降低开关活动性的设计技术
    - 逻辑重组 $F = ABCD$



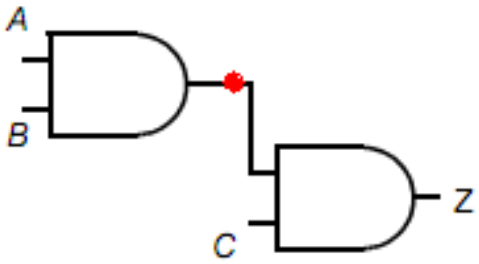



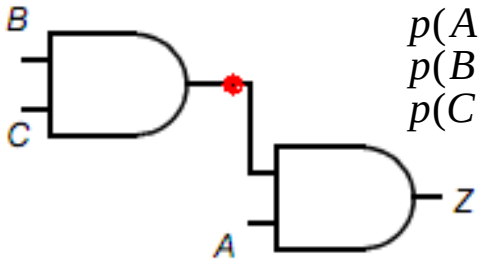

$$p_1(a,b,c,d) = \frac{1}{2}$$

| | $O_1$ | $O_2$ | $F$ |
|---|---|---|---|
| $p_1$ (chain) | 1/4 | 1/8 | 1/16 |
| $p_0$ = 1-$p_1$ (chain) | 3/4 | 7/8 | 15/16 |
| $p_{0\to1}$ (chain) | 3/16 | **7/64** | 15/256 |
| $p_1$ (tree) | 1/4 | 1/4 | 1/16 |
| $p_0$ = 1-$p_1$ (tree) | 3/4 | 3/4 | 15/16 |
| $p_{0\to1}$ (tree) | 3/16 | **3/16** | 15/256 |

# 静态互补CMOS电路

- 组合逻辑电路中的性能优化
  - 降低开关活动性的设计技术
    - 输入排序



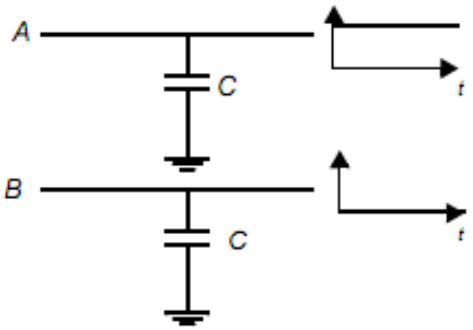

$p(A=1)=0.5$
$p(B=1)=0.2$
$p(C=1)=0.1$

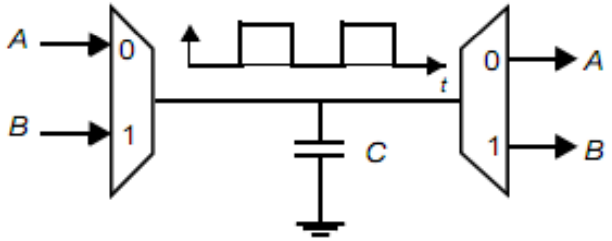
$(1-0.5\times0.2)(0.5\times0.2)$
$=0.09$

$(1-0.2\times0.1)(0.2\times0.1)$
$=0.0196$

# 静态互补CMOS电路

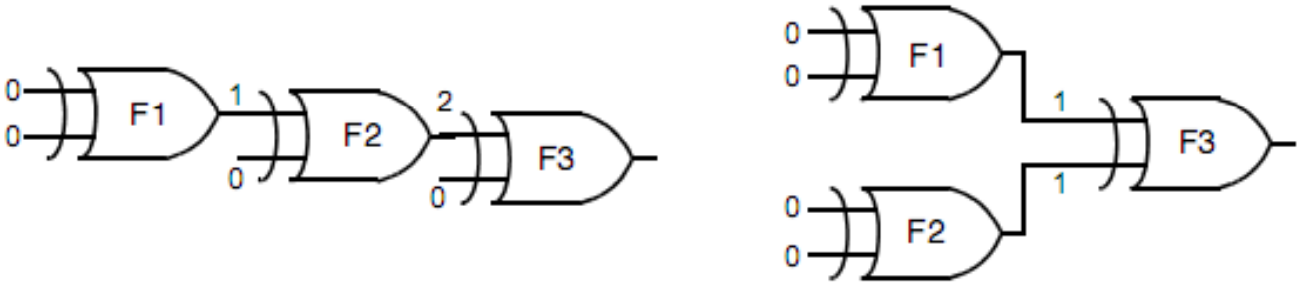
- 组合逻辑电路中的性能优化
  - 降低开关活动性的设计技术
    - 分时复用资源
      - 减少面积
      - 增加功耗



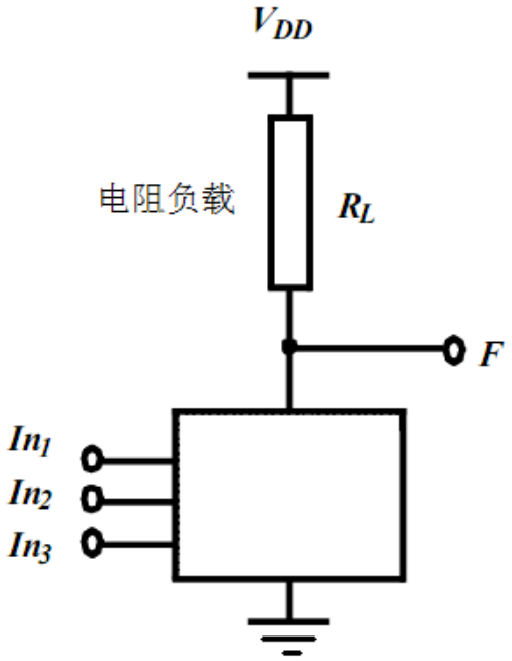
# 静态互补CMOS电路

- 组合逻辑电路中的性能优化
  - 降低开关活动性的设计技术
    - 通过均衡信号路径来减少毛刺



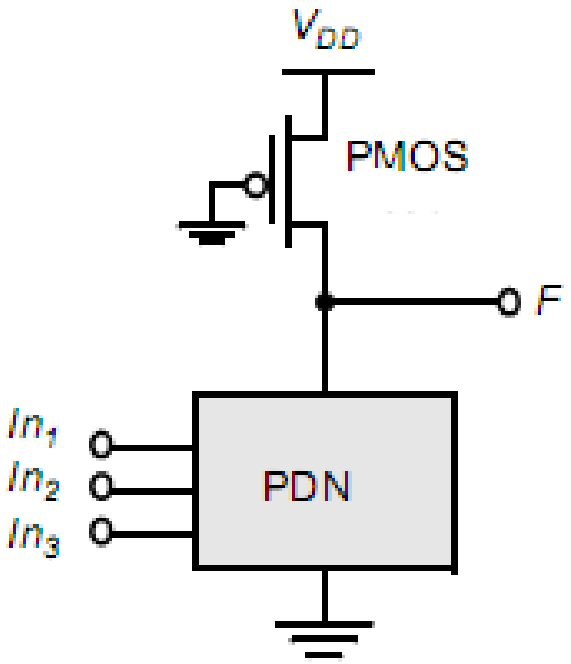
# 有比逻辑

- 有比逻辑由一个有源下拉（上拉）网络连到一个负载器件上构成
  - N个晶体管+负载
  - $V_{OH}=V_{DD}$
  - $V_{OL}=（V_{DD}R_{PDN}）/（R_{PDN}+R_L）$
  - $t_{pHL}\neq t_{pLH}$，$t_{pLH}=0.69R_LC_L$
  - 有静态功耗




有比逻辑门

# 有比逻辑




- 伪NMOS门
  - 晶体管数目N+1
  - 额定输出高电压$V_{DD}$
  - 额定输出低电压不是0

$$k_n\left(\left(V_{DD}-V_{Tn}\right)V_{OL}-\frac{V_{OL}^2}{2}\right)+k_p\left(\left(-V_{DD}-V_{Tp}\right)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)=0$$

$V_{OL}$可近似为

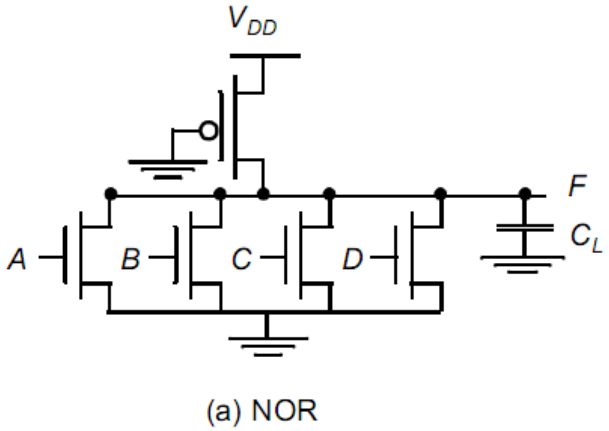
$$V_{OL}\approx\frac{k_p\left(V_{DD}+V_{Tp}\right)V_{DSATp}}{k_n\left(V_{DD}-V_{Tn}\right)}\approx\frac{\mu_p W_p}{\mu_n W_n}V_{DSATp}$$

静态功耗

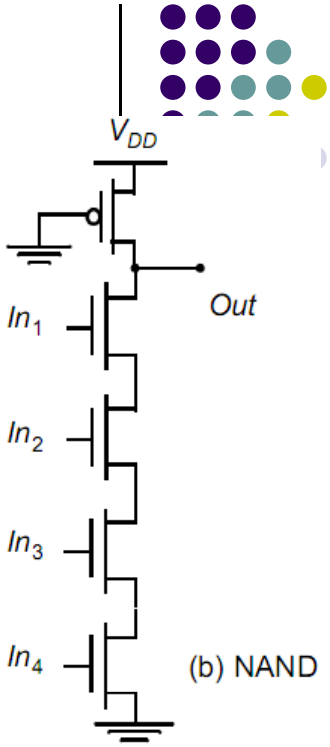
$$P_{low}=V_{DD}I_{low}\approx V_{DD}\left|k_p\left(\left(-V_{DD}-V_{Tp}\right)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)\right|$$

# 有比逻辑

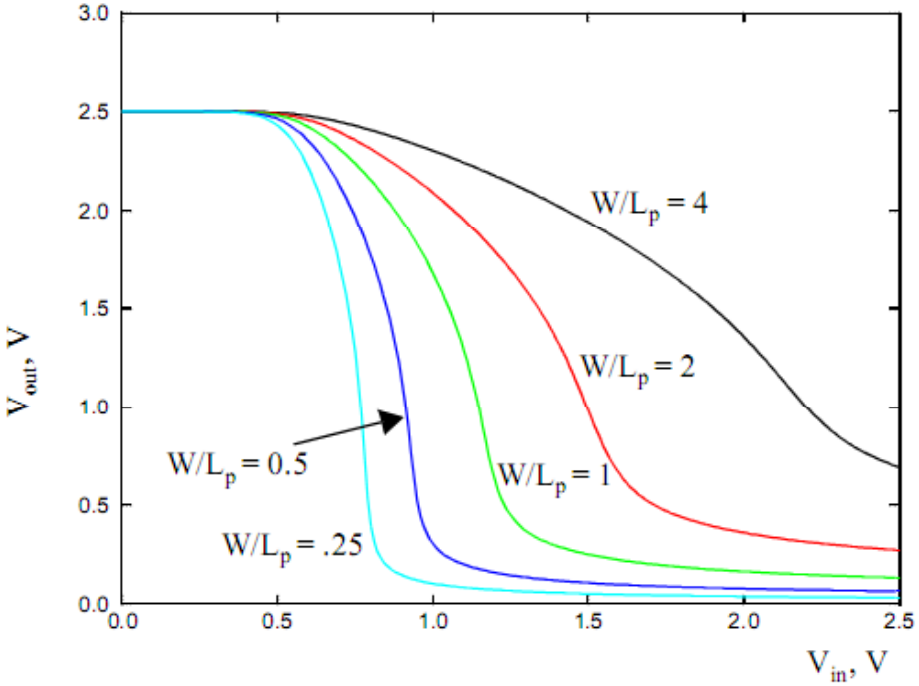
- 伪NMOS门
  - 静态功耗较大
  - 适于大扇入电路




(a) NOR



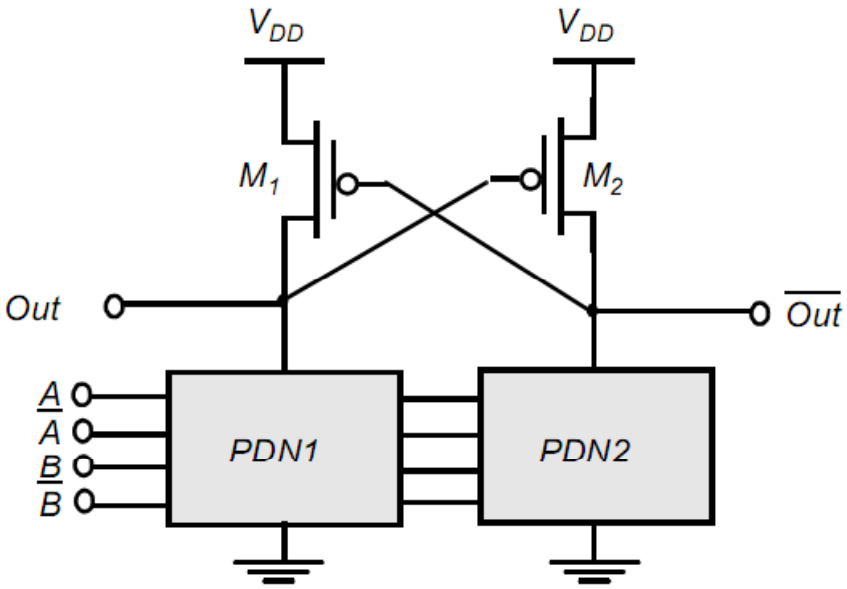

(b) NAND

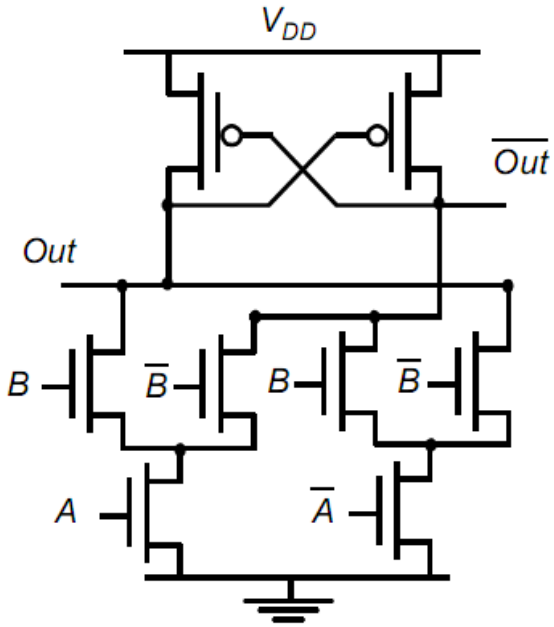



| Size | $V_{OL}$ | Static Power Dissipation | $t_{plh}$ |
|---|---|---|---|
| **4** | 0.693V | 564µW | 14ps |
| **2** | 0.273V | 298µW | 56ps |
| **1** | .133V | 160µW | 123ps |
| **0.5** | 0.064V | 80µW | 268ps |
| **0.25** | 0.031V | 41µW | 569ps |

# 有比逻辑

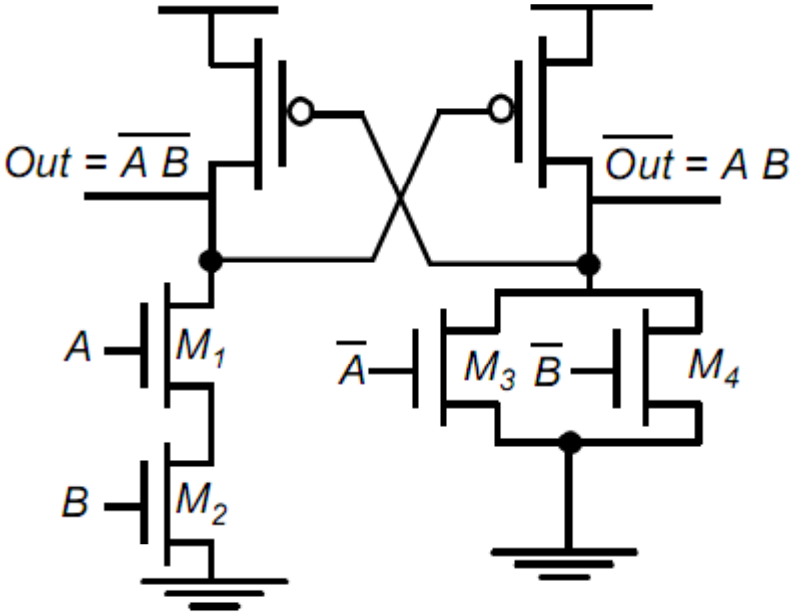
- 差分串联电压开关逻辑（DCVSL）
  - 可以完全消除静态电流和提供电源轨线至电压摆幅的有比逻辑
    - 差分逻辑：每个输入都具有互补形式
    - 正反馈：通过正反馈将不需要的负载器件关断

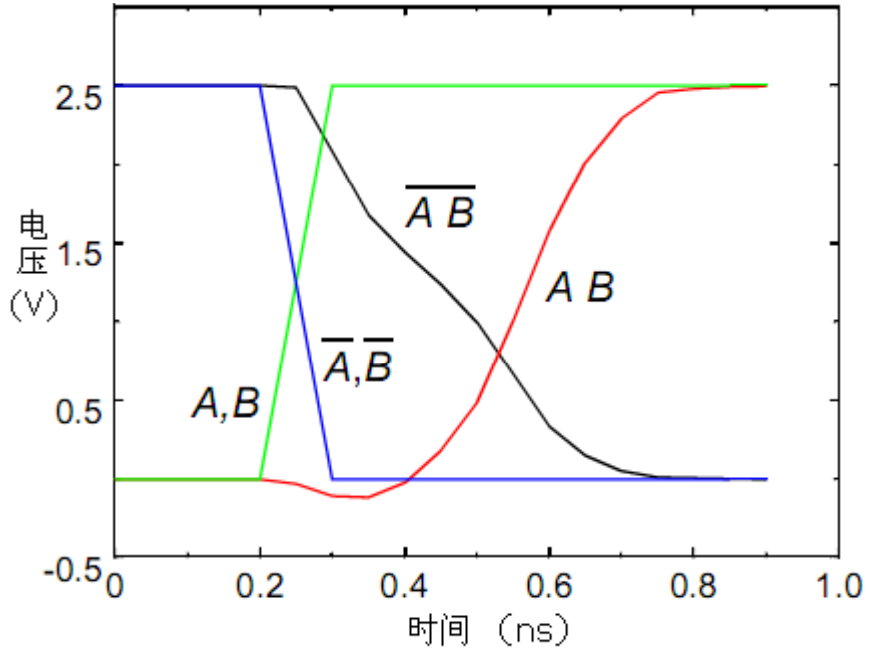


# 有比逻辑

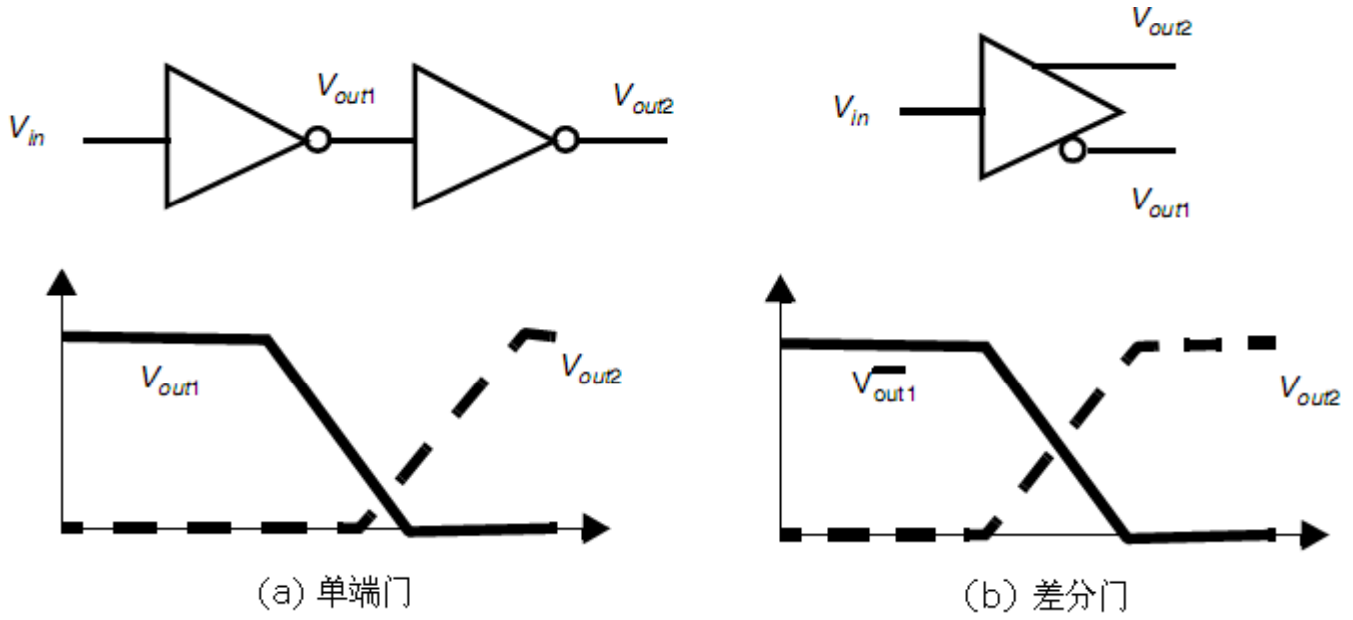
- 差分串联电压开关逻辑（DCVSL）
  - 信号延迟



# 有比逻辑

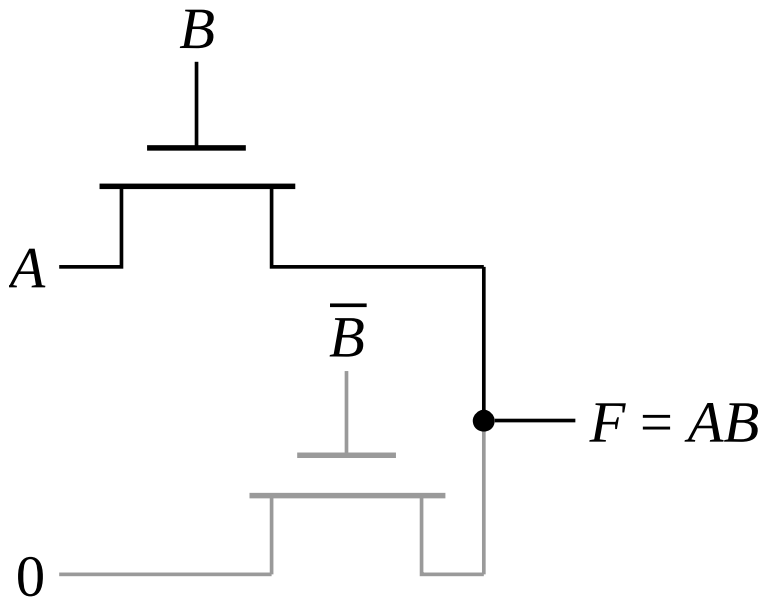
- 差分串联电压开关逻辑（DCVSL）
  - 设计考虑
    - 同时产生互补信号
    - 导线数量加倍，使设计电路十分复杂




(a) 单端门　　(b) 差分门

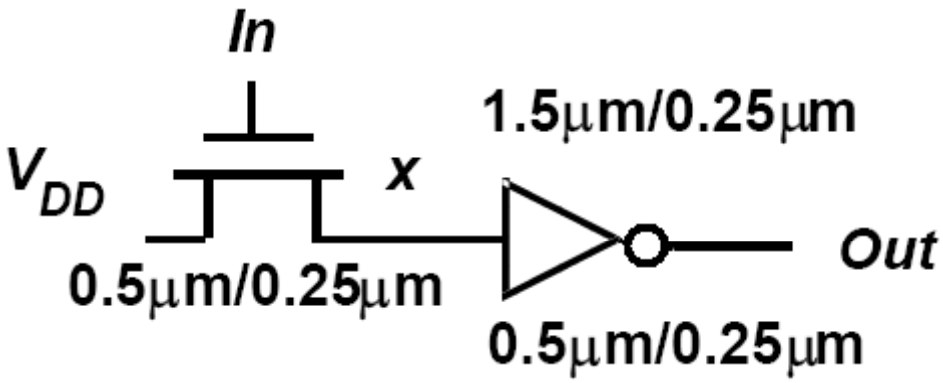
# 传输管逻辑

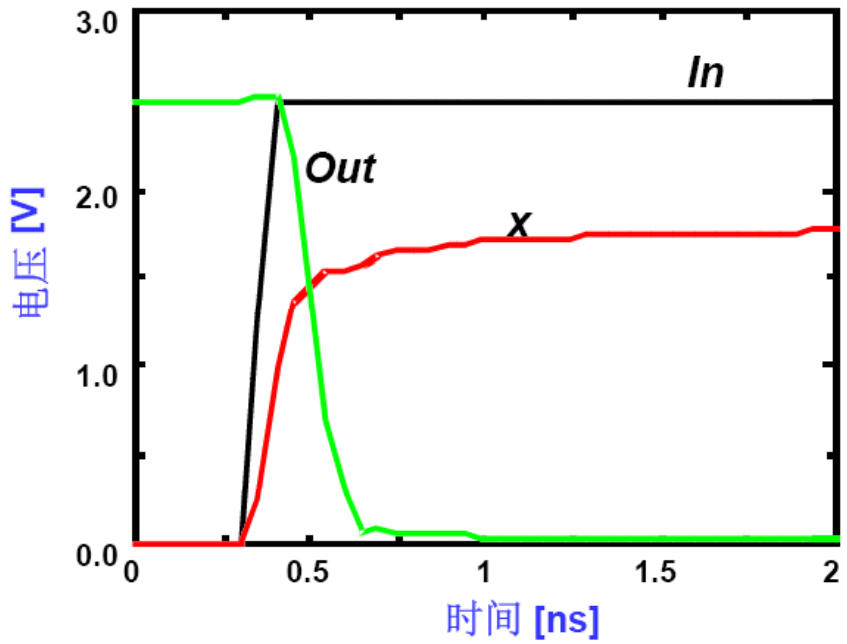
- 传输管逻辑允许原始输入驱动栅端和源-漏端来减少实现逻辑所需要的晶体管数目
- 前面介绍的逻辑门只允许驱动晶体管的栅端

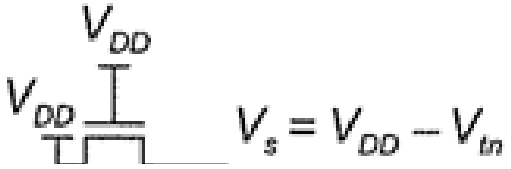


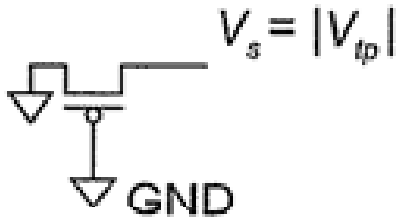
# 传输管逻辑

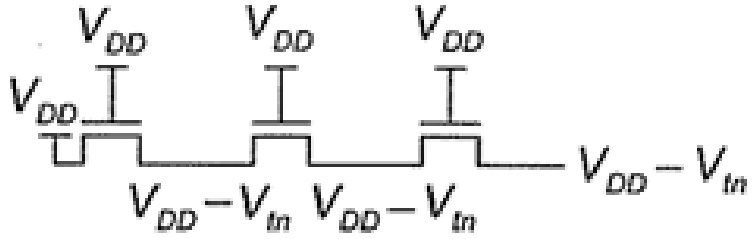
- 传输管的电压摆幅

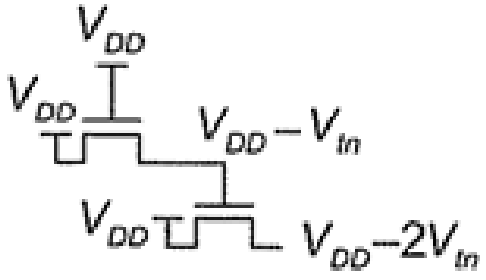


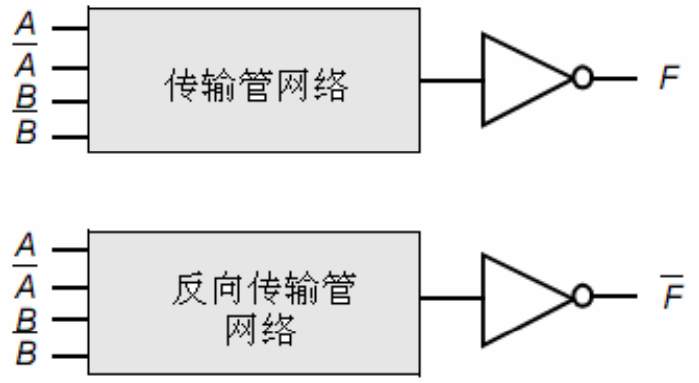



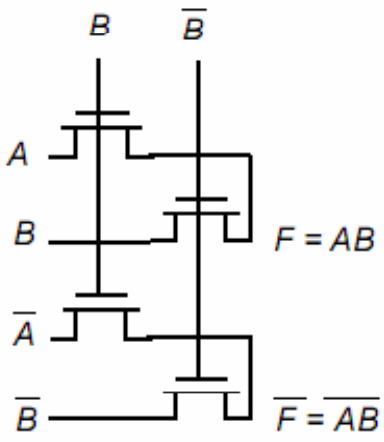



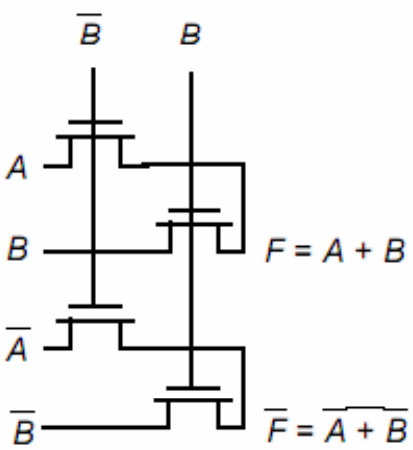
# 传输管逻辑

- 差分传输管逻辑
  - 互补传输管逻辑（CPL）
    - 电路简单，功耗低
    - 输出节点总是连至$V_{DD}$或GND
    - 设计具有模块化特点

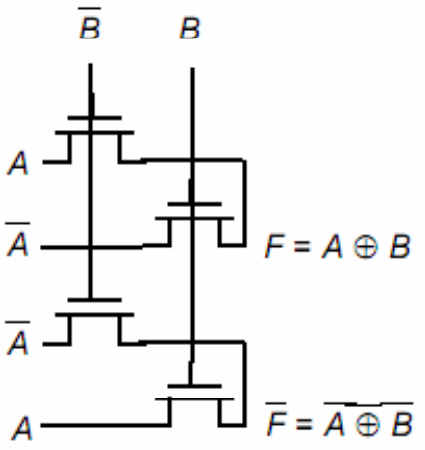



AND/NAND



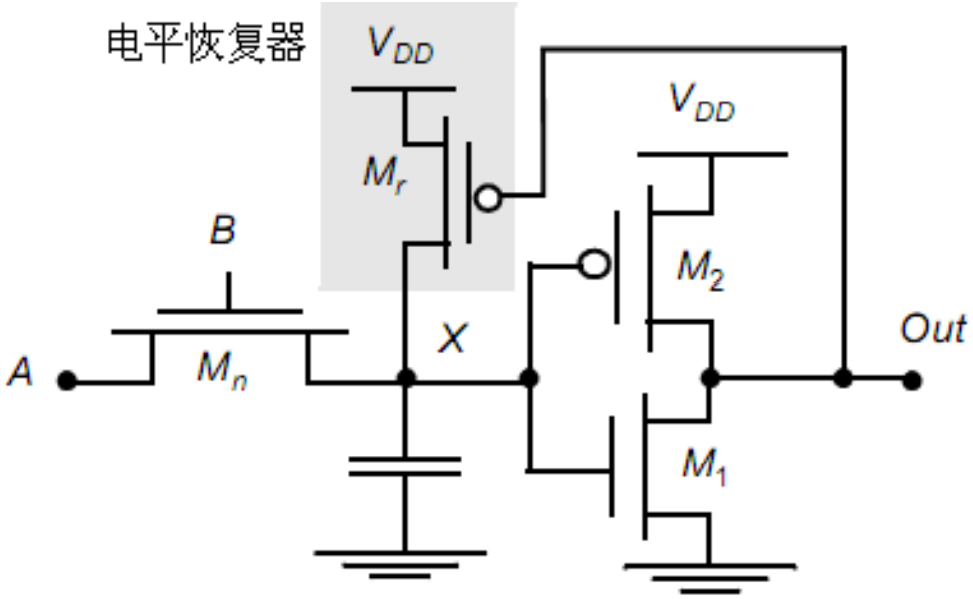

OR/NOR

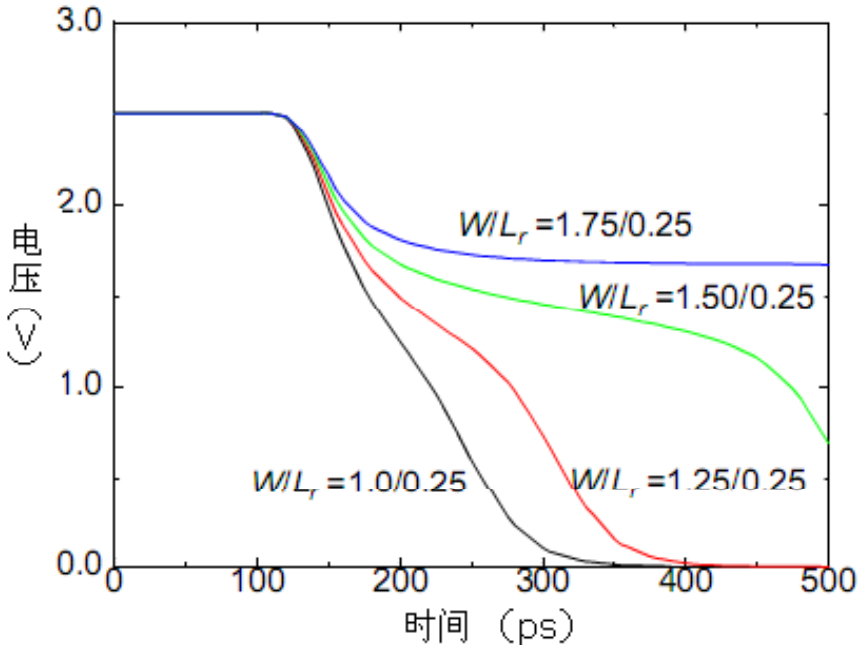



XOR/NXOR

# 传输管逻辑

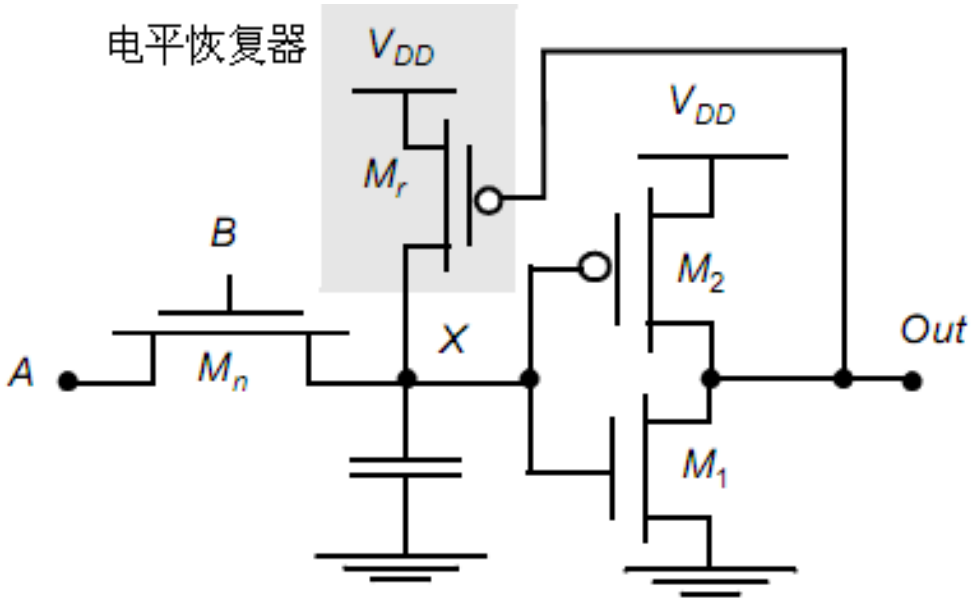
- 稳定有效的传输管设计
  - 电平恢复
    - 无静态功耗
    - 有比电路

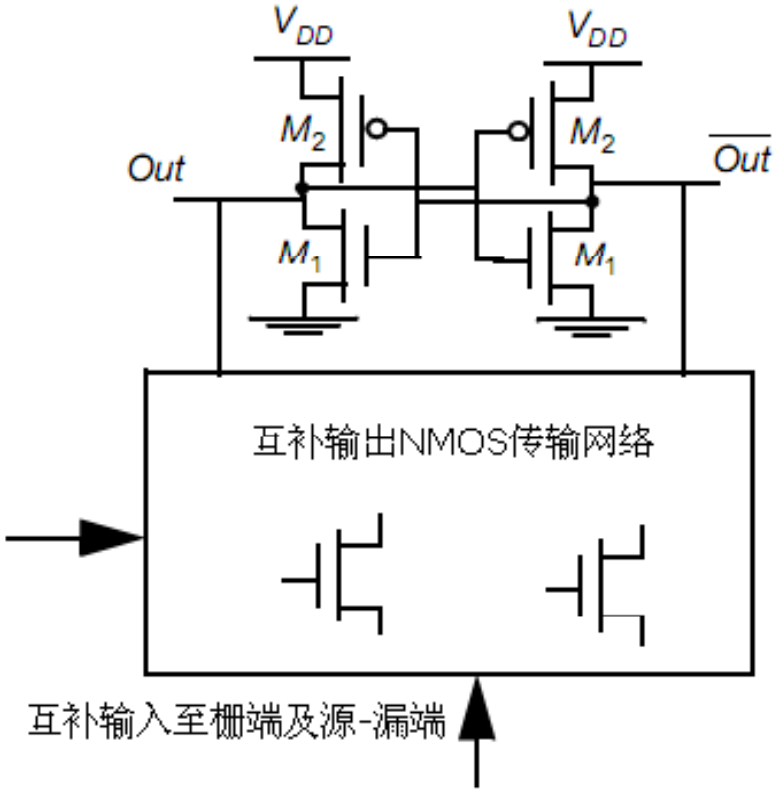


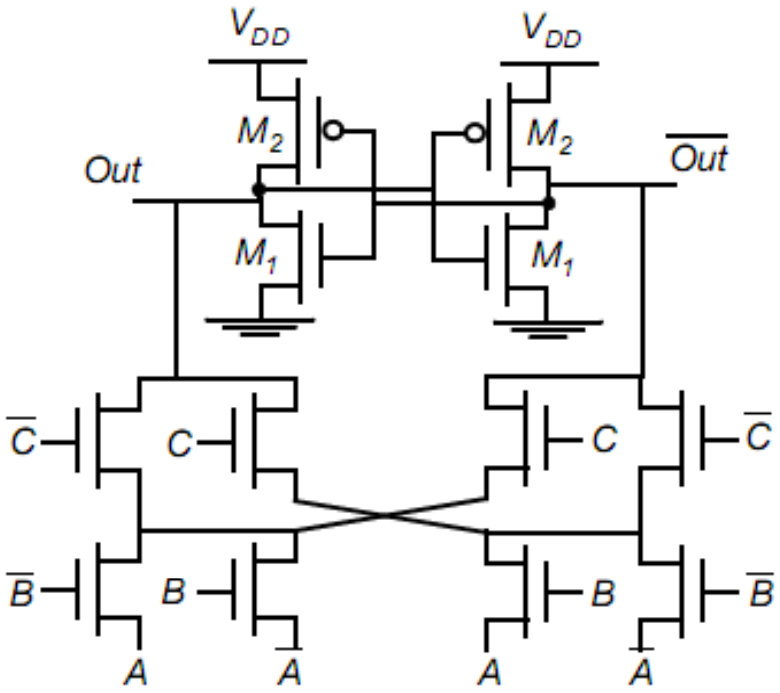



# 传输管逻辑

- 稳定有效的传输管设计
  - 电平恢复
    - 影响器件切换速度

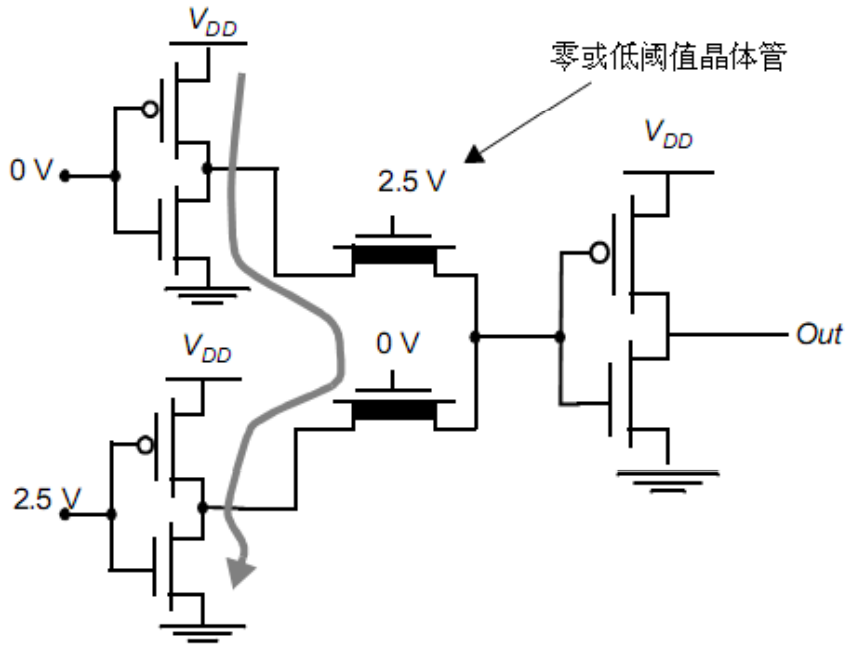


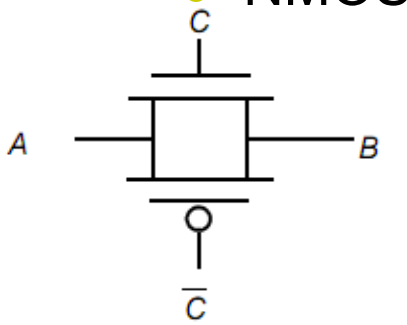
# 传输管逻辑

- 稳定有效的传输管设计
  - 多种阈值晶体管
    - 传输管NMOS采用零阈值器件实现
    - 非传输管的器件都用标准的高阈值器件实现
    - 器件的体效应仍然会阻止全摆幅达到$V_{DD}$
    - 采用零阈值器件会增加功耗

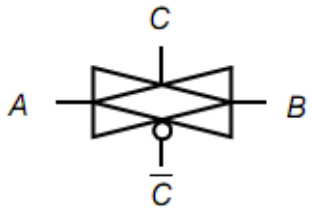


# 传输管逻辑

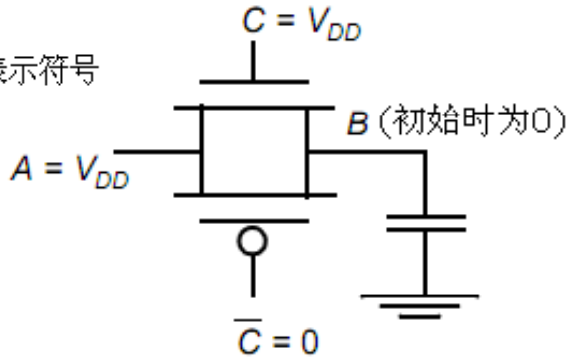
- 稳定有效的传输管设计
  - 传输门逻辑
    - 由一个NMOS器件与一个PMOS器件并联构成
    - NMOS器件用于下拉，PMOS器件用于上拉



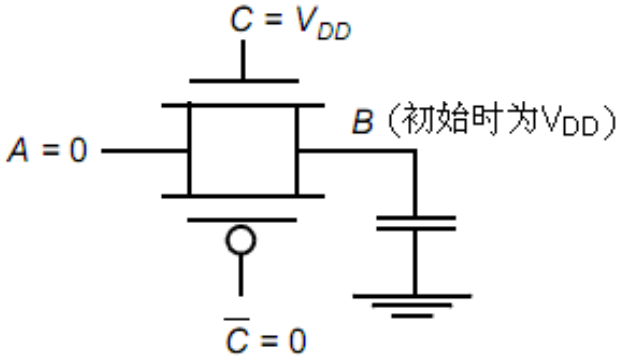
(a) 电路



(b) 表示符号



(a)充电节点B

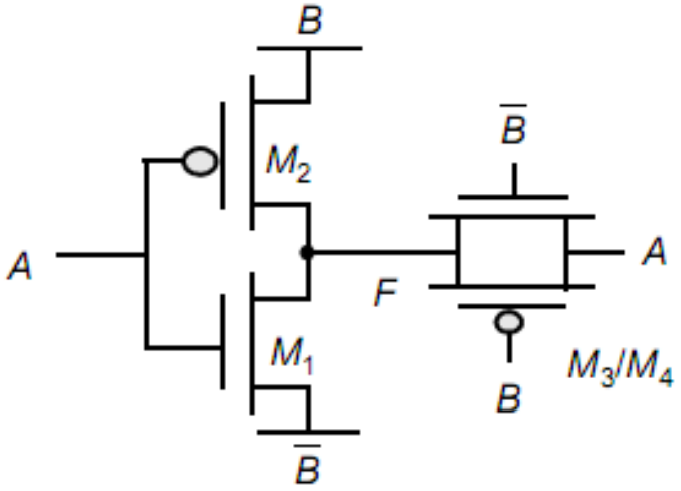


(b)放电节点B

# 传输管逻辑

- 稳定有效的传输管设计
  - 传输门逻辑

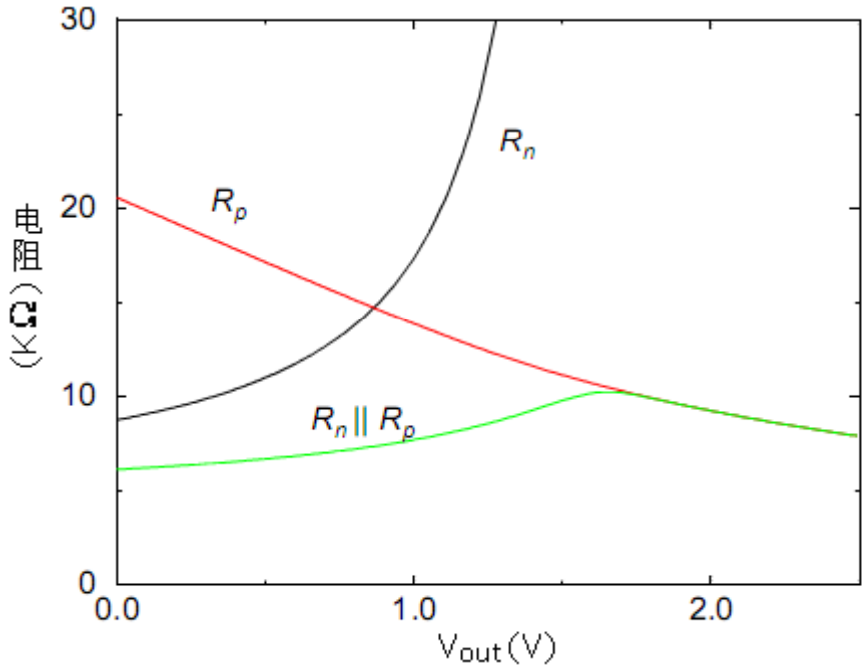
$$F = \overline{A}B + A\overline{B}$$

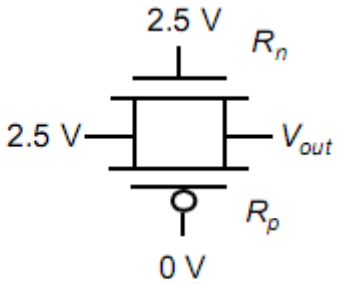



XOR传输门

# 传输管逻辑

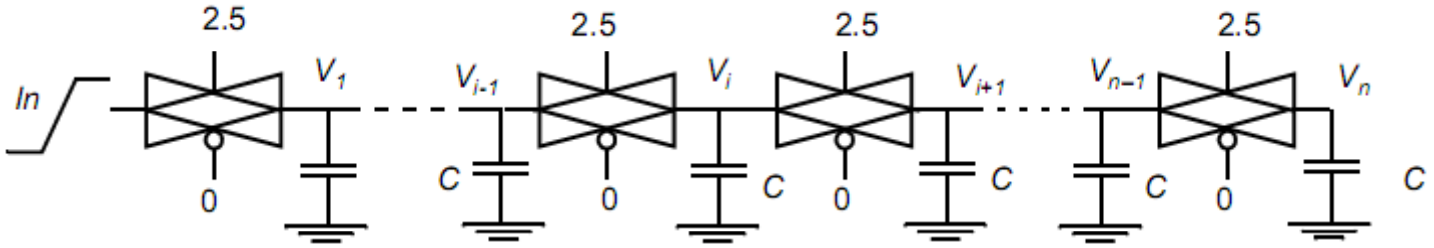
- 传输管和传输门逻辑的性能



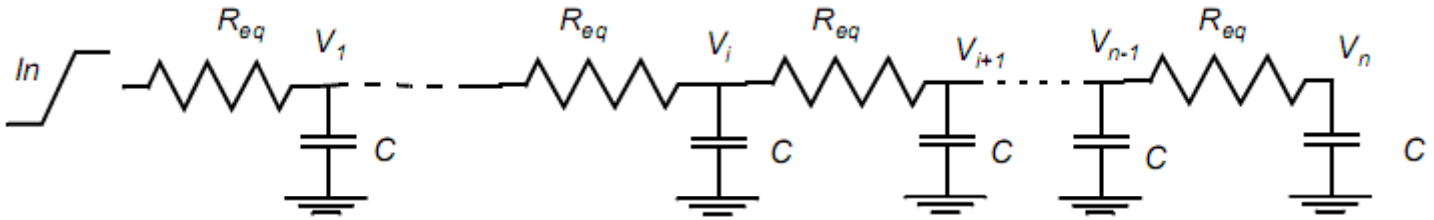



# 传输管逻辑

- 传输门链的延时




(a) 传输门链



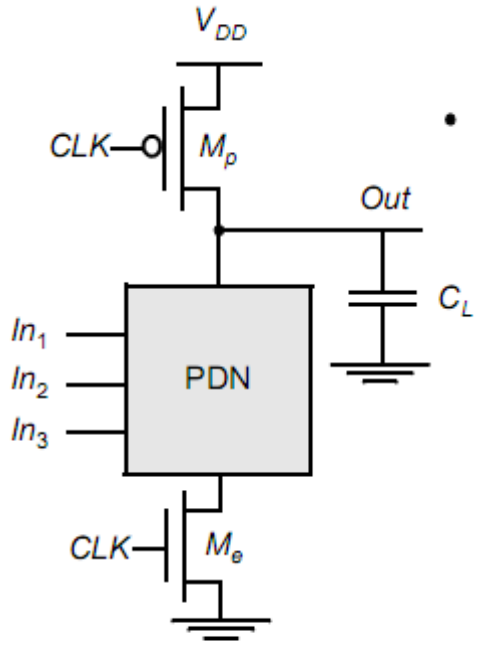

(b) 等效的RC网络

$$t_p(V_n) = 0.69\sum_{k=0}^{n} C\,\mathrm{R}_{eq}\,k = 0.69C\,\mathrm{R}_{eq}\,k\,\frac{n(n+1)}{2}$$

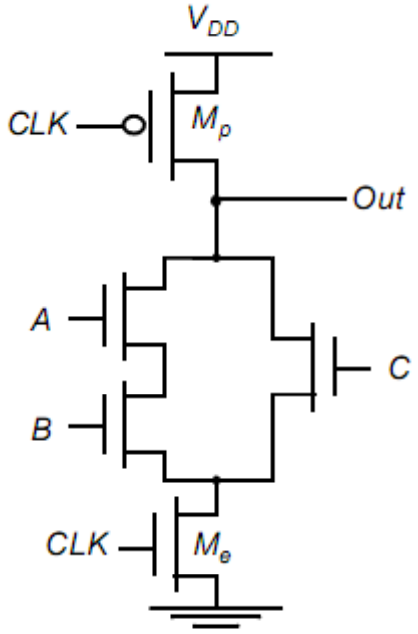
# 动态CMOS设计

- 动态逻辑：基本原理
  - 两个工作阶段，由时钟信号决定
    - 预充电
    - 求值

$$Out = \overline{CLK} + \overline{(A \cdot B + C)} \cdot CLK$$




(a) n型网络

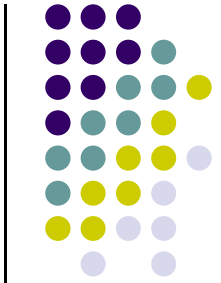



(b) 举例

# 动态CMOS设计

- 动态逻辑门对输入和输出的要求
  - 一旦动态门的输出被放电，它直到下一个充电阶段之前不可能再次被充电
  - 动态门的输入在求值期间最多只能有一次过渡
  - 求值期间或求值之后输出可以处于高阻态，求值之后的状态存放在$C_L$上

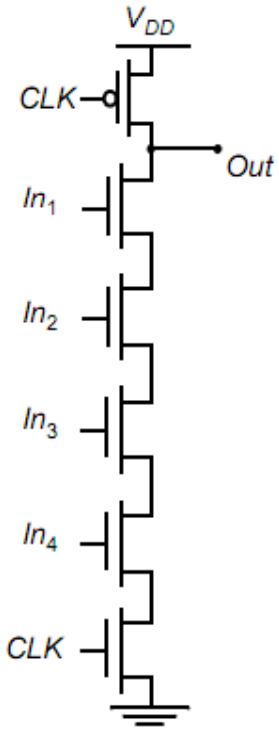
# 动态CMOS设计

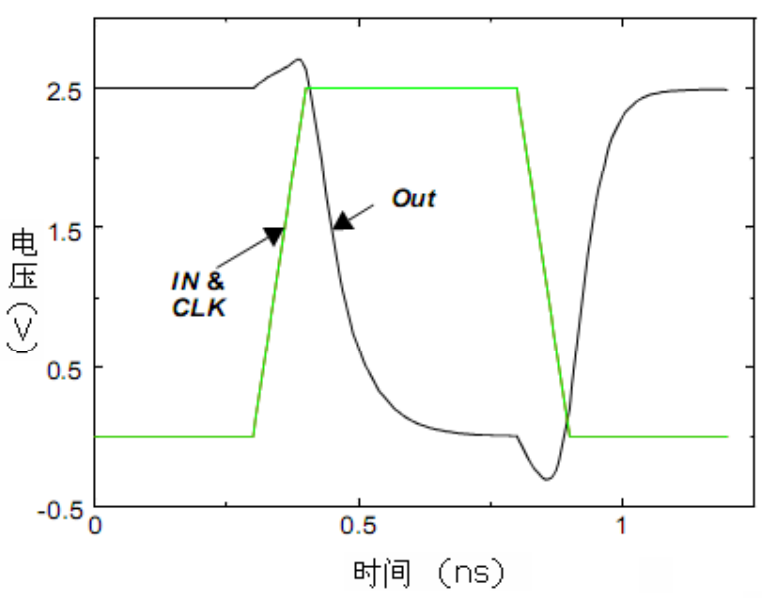


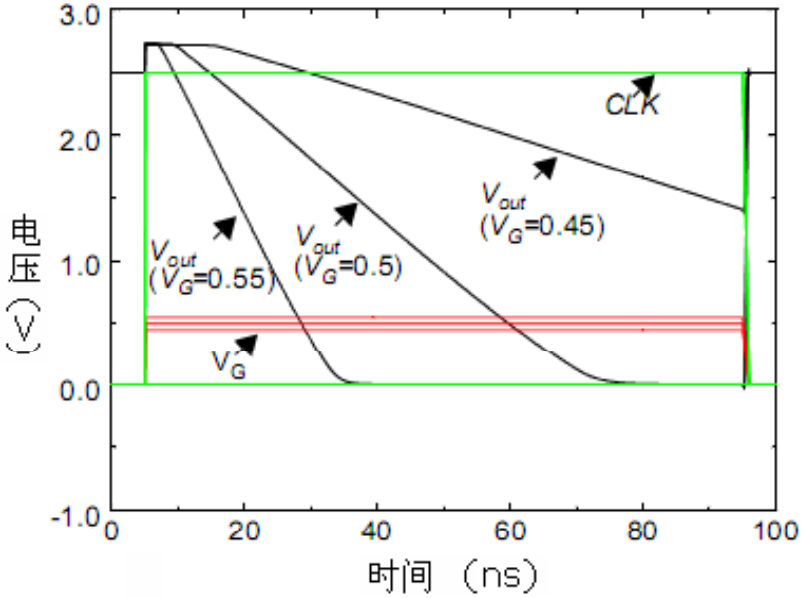
- 动态逻辑门的重要特性
  - 逻辑功能由NMOS下拉网络实现
  - 晶体管数目（对于复杂门）明显少于静态情况：为N+2
  - 是无比的逻辑门
  - 动态逻辑门只有动态功耗
  - 动态逻辑门具有较快的开关速度
    - 减少了每个门的晶体管数目
    - 下拉器件只对负载电容放电

# 动态CMOS设计

- 动态逻辑的速度和功耗

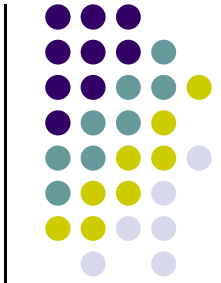



| 晶体管数 | $V_{OH}$ | $V_{OL}$ | $V_M$ | $NM_H$ | $NM_L$ | $t_{pHL}$ | $t_{pLH}$ | $t_{pre}$ |
|---|---|---|---|---|---|---|---|---|
| 6 | 2.5 V | 0 V | $V_{TN}$ | 2.5-$V_{TN}$ | $V_{TN}$ | 110 psec | 0 nsec | 83psec |

# 动态CMOS设计



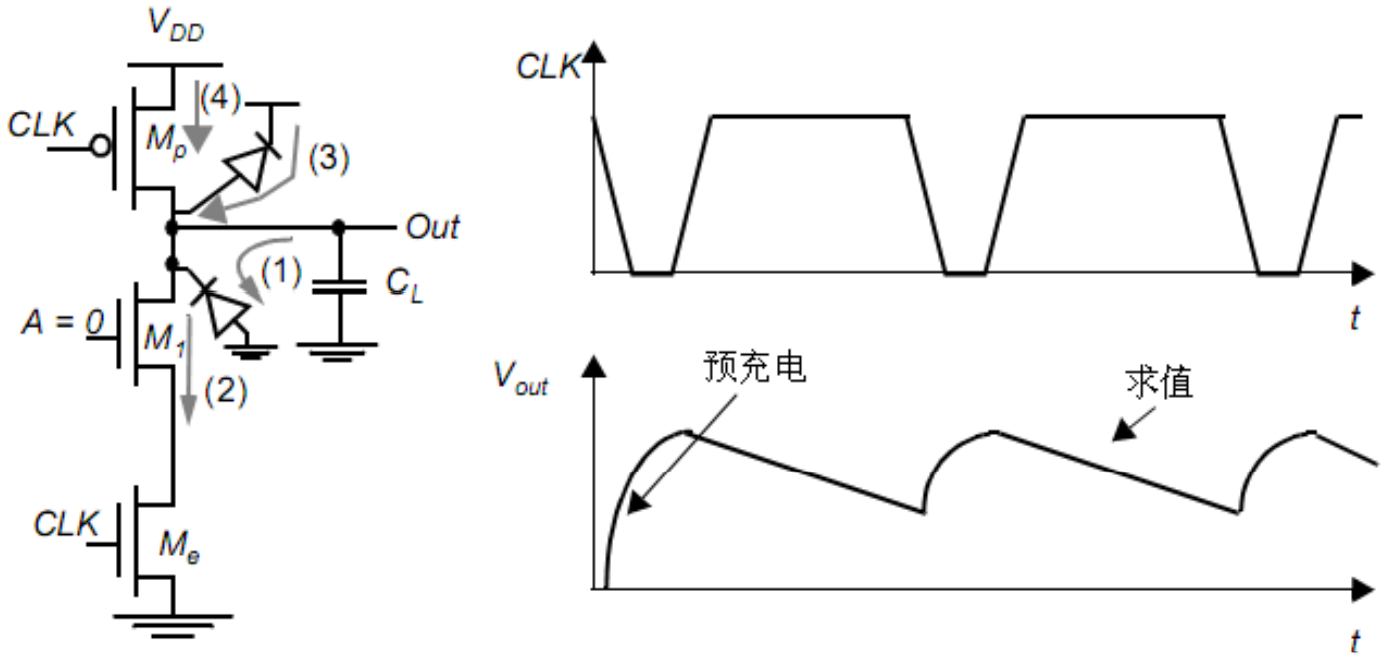
- 动态逻辑的速度和功耗
  - 实际电容较少
  - 动态门每个时钟周期只有一次翻转
  - 动态门不存在短路功耗

  - 动态逻辑时钟功耗可以很大
  - 动态门使用晶体管数目并不是最少的
  - 当增加抗漏电器件时可能会有短路功耗存在
  - 由于周期性的预充电和放电操作，动态逻辑通常表现出较高的开关活动性 $a_{0\to1} = p_0$

    对于均匀分布输入的N个输入门的翻转概率为：$a_{0\to1} = \frac{N_0}{2^N}$

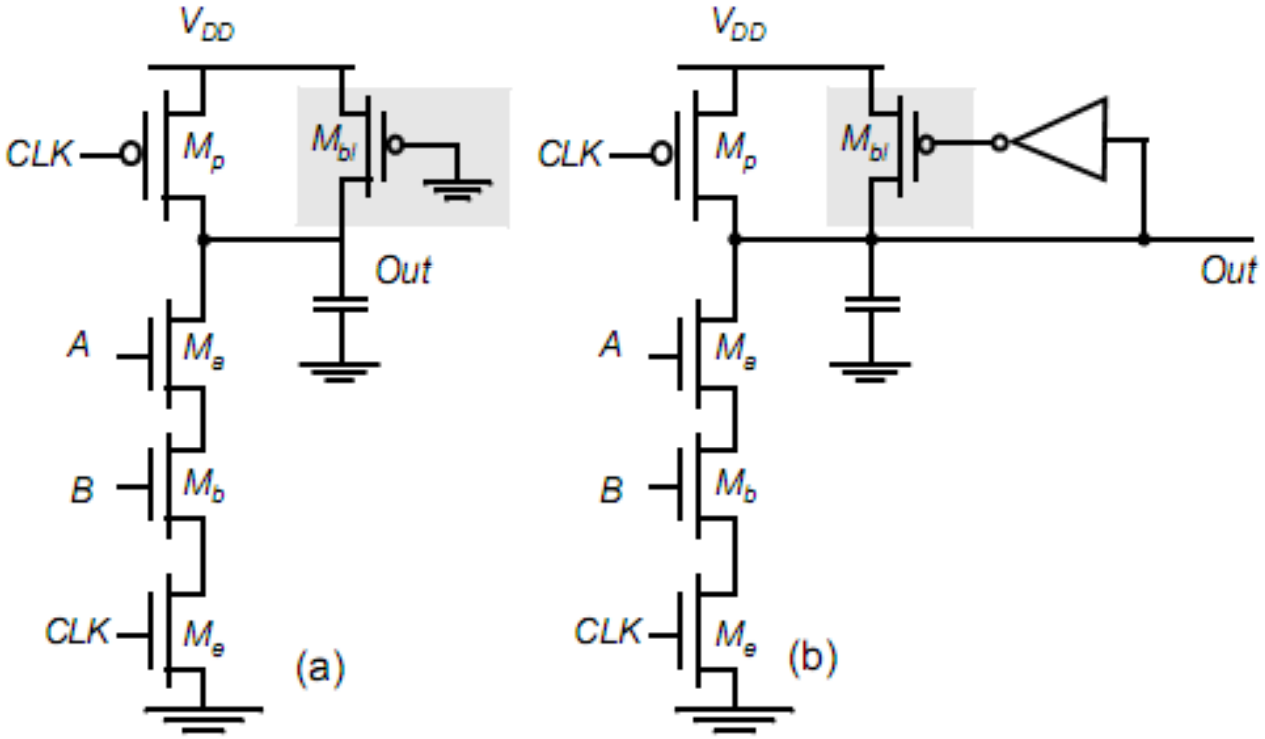
# 动态CMOS设计

- 动态设计中的信号完整性问题
  - 电荷泄露



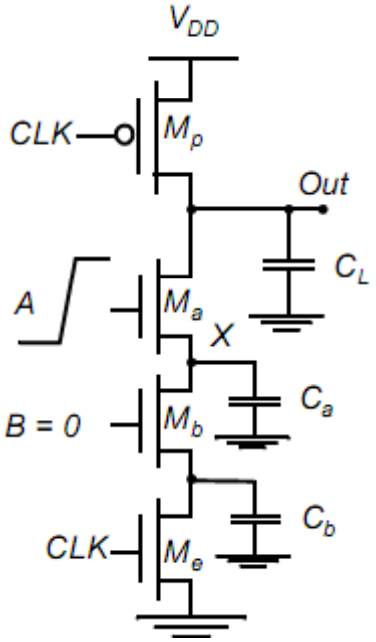
# 动态CMOS设计

- 动态设计中的信号完整性问题
  - 电荷泄露
    - 增加泄露晶体管



# 动态CMOS设计

- 动态设计中的信号完整性问题
  - 电荷分享




$$C_L V_{DD} = C_L V_{out} + C_a \left[ V_{DD} - V_{Tn} \left( V_X \right) \right]$$

或

$$\Delta V_{out} = V_{out} + \left( -V_{DD} \right) = -\frac{C_a}{C_L} \left[ V_{DD} - V_{Tn} \left( V_X \right) \right]$$

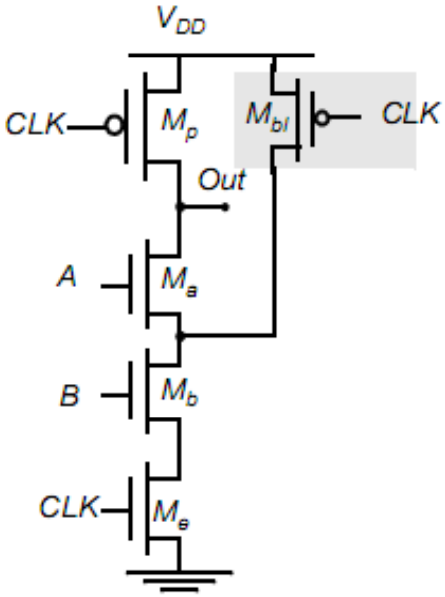
$$V_{DD} C_L = V_{out} C_L + V_X C_a$$

$$\Delta V_{out} = -V_{DD} \left( \frac{C_a}{C_a + C_L} \right)$$

边界条件 $\frac{C_a}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}}$

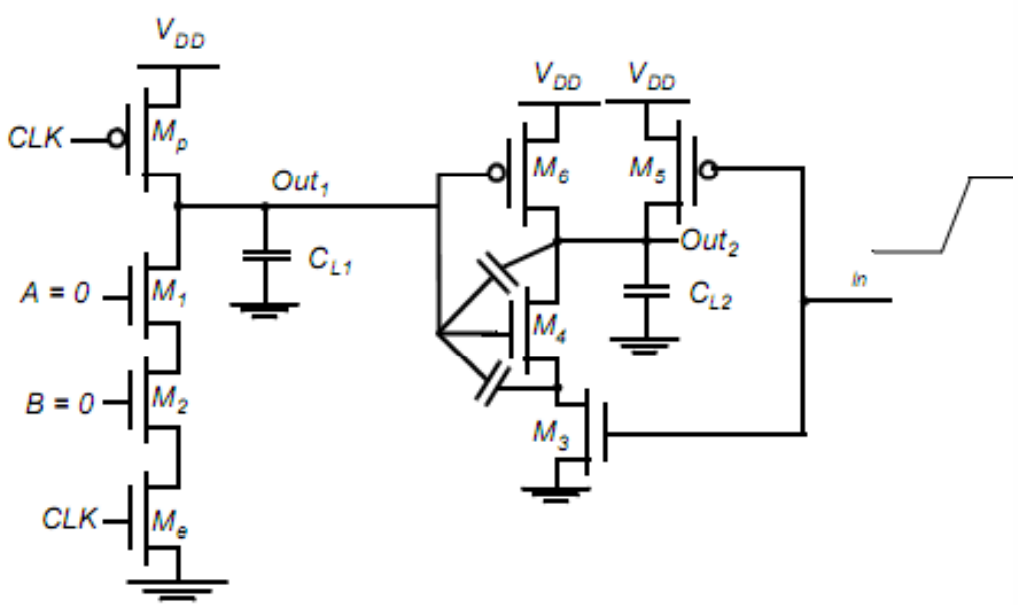
$\Delta V_{out} < V_{Tn}$

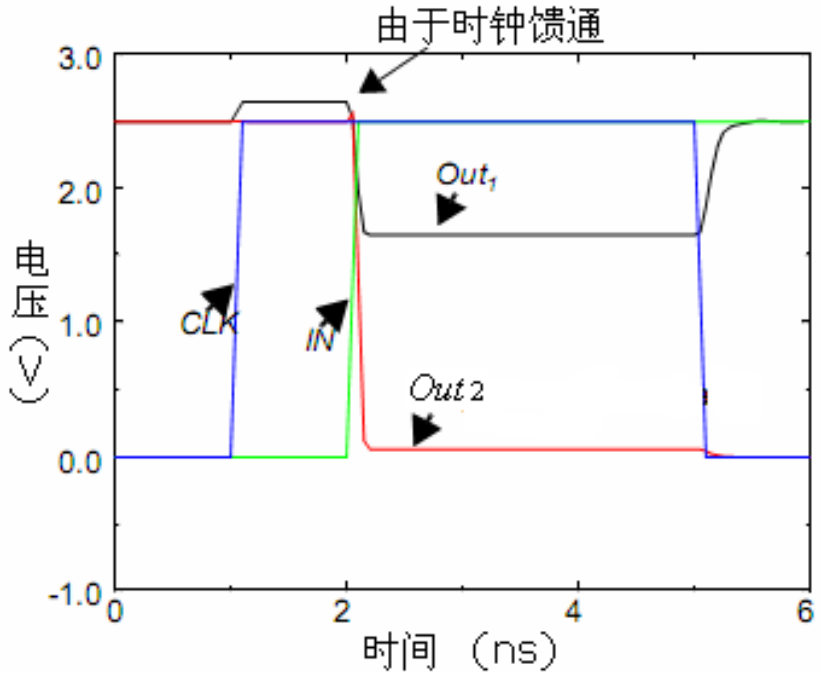
$\Delta V_{out} > V_{Tn}$



# 动态CMOS设计

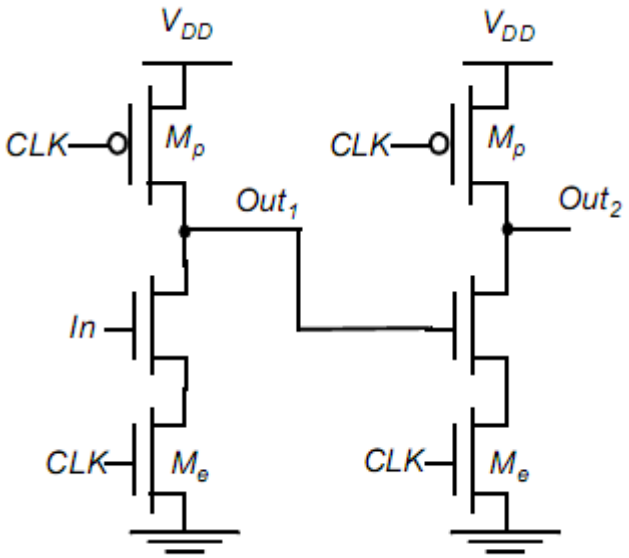
- 动态设计中的信号完整性问题
  - 电容耦合
  - 时钟馈通

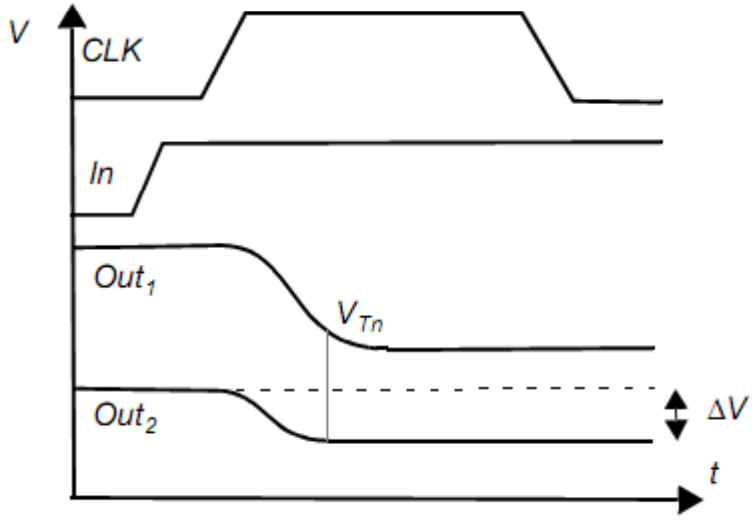


# 动态CMOS设计

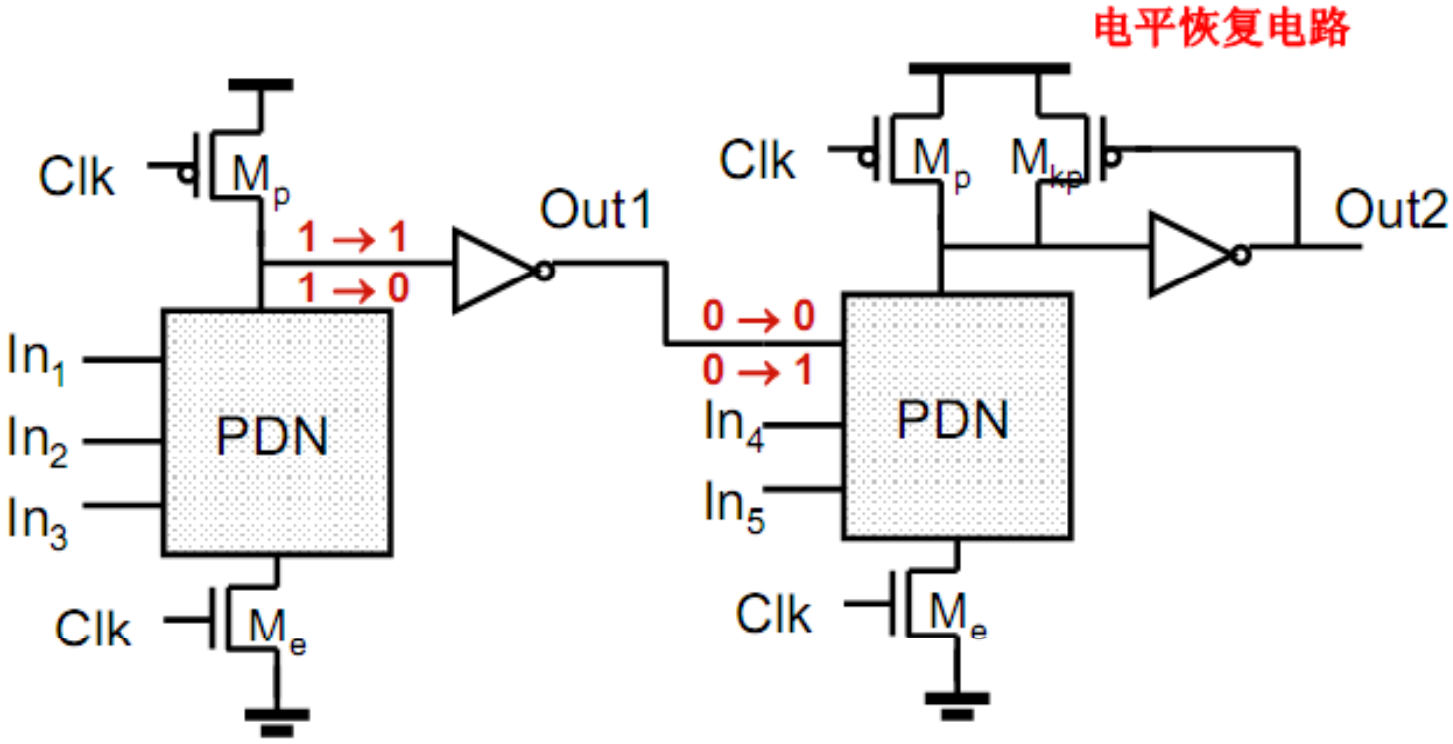
- 串联动态门
  - 上一级的信号延迟导致下一级的电荷流失



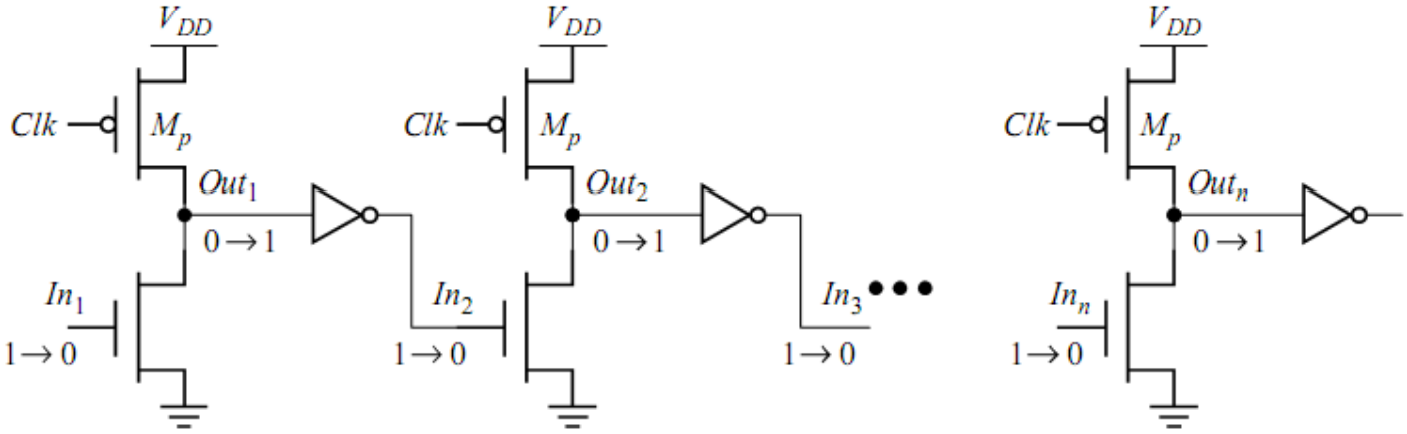
# 动态CMOS设计

- 多米诺逻辑
  - 动态逻辑+反相器



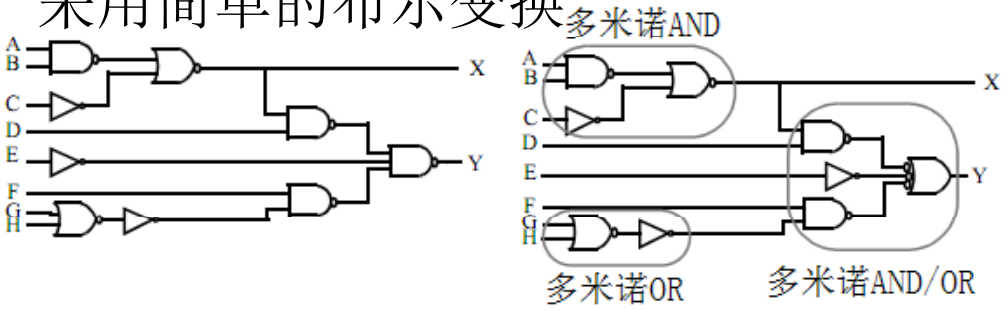
# 动态CMOS设计

- 多米诺CMOS特点
  - 只能实现非反向逻辑
  - 有非常高的速度，只有上升延时，而下降延时为零
- 无求值管多米诺
  - 信号传播延迟，预充电产生竞争，导致静态功耗

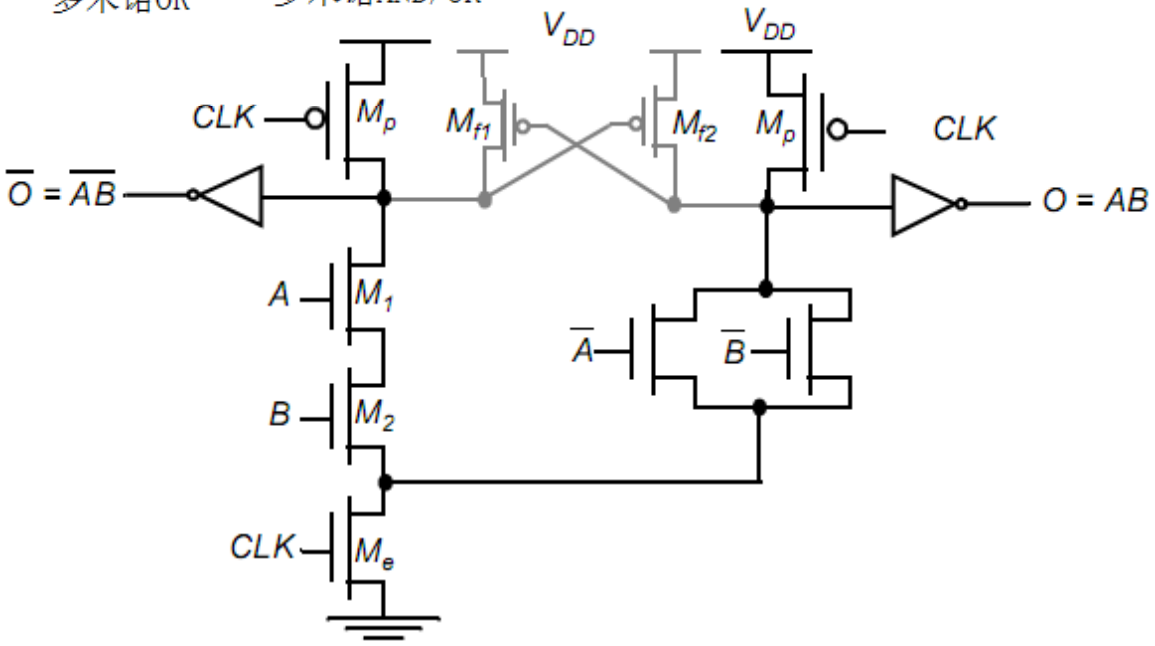


# 动态CMOS设计

- 多米诺逻辑非反向问题
  - 采用简单的布尔变换

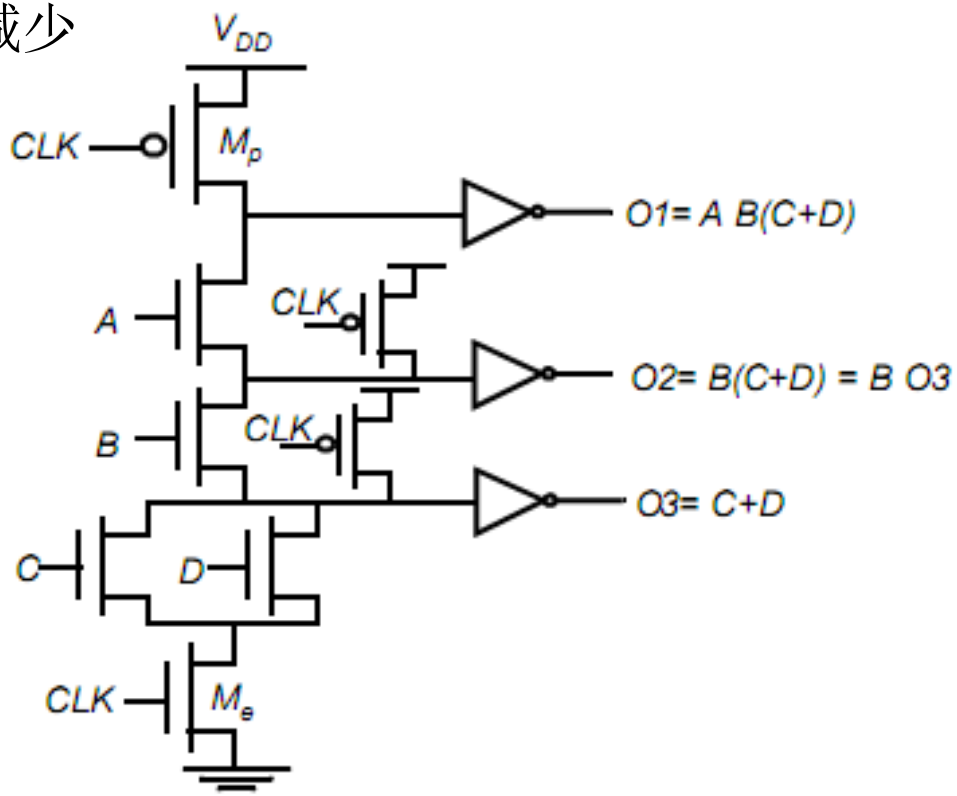



  - 采用差分逻辑
    - 双轨多米诺



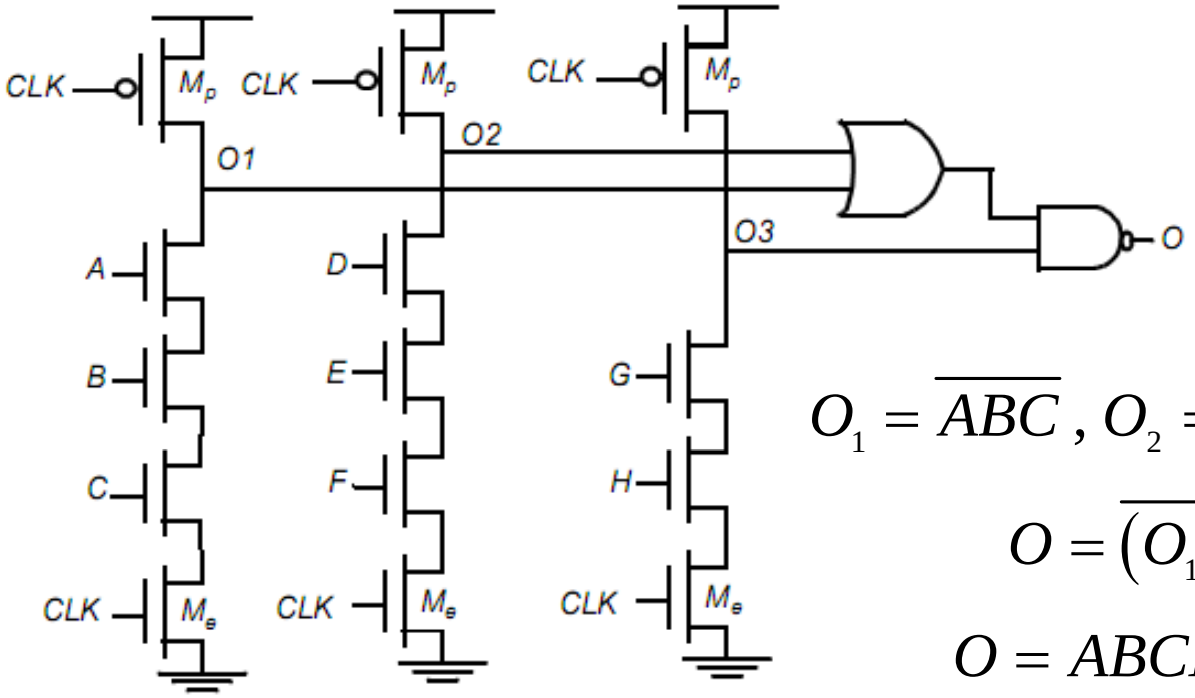
# 动态CMOS设计

- 多米诺逻辑门的优化
  - 多输出多米诺
    - 求值晶体管数目减少
    - 扇出数目减少



# 动态CMOS设计

- 多米诺逻辑门的优化
  - 组合多米诺




$$O_1 = \overline{ABC}\,,\ O_2 = \overline{DEF}\,,\ O_3 = \overline{GH}$$

$$O = \overline{(O_1 + O_2)O_3}$$

$$O = ABCDEF + GH$$

# 动态CMOS设计

- np-CMOS