

课程作业 (Coursework)

- 1 **课程得分** (Score Percentiles): Class Attendance (20%), Completion of Course Report (80%). *The final scores is reported to the office of school's administration.*
- 2 **课程作业截止时间** (Due Date of Coursework): Friday, July 9, 2018.
- 3 **课程作业形式**: 研究文章或者研究报告(**Option 1**: Research Paper, **Option 2**: Research Report)。

4 研究文章或者研究报告写作模板:

Option 1: Research Paper (in concise style) should contain 3-5 pages, you may use the sample paper “CSTIC_2017_Symposium_9-16_Cheng_Hu2.pdf” as a reference. The Paper can be written in either English or in Chinese.

Option 2: Research Report (in loose style) can contain 6-10 pages, you may use the sample paper “CSTIC_2017_Symposium_9-16_Cheng_Hu2.pdf” as a reference. The Report can be written in either English or in Chinese.

5 研究文章或者研究报告格式:

Paper Title, Author(s) Names and Affiliations: paper or report title should be related to current course, i.e. “SoC Design in AI-Big Data Era and/or related applications”, see “Recommended class project titles” below. Don’t forget to write your name(s) and affiliation(s), as well as your communication address.

Abstract: provide a short abstract paragraph. List of key words is optional.

Paper or Report style and format: it is recommended to follow the reference template (Research_paper_template1.doc or Research_paper_template2.doc) which is provided with this document. See also the above sample paper “CSTIC_2017_Symposium_9-16_Cheng_Hu2.pdf” for your writing reference.

Note: *If 2-3 people work in a group, the roles and contributions from each individual must be claimed and stated to receive their credits.*

6 研究文章题目:

- A Study of “XNN” Algorithm and Its {System Architecture | Verilog Coding | Verification and} Design Implementation.

- Architecture Design and Verification of a {AI chip, IoT chip or MCU or SoC}
- Design and Integration of {RapidIO IP} in {Communication SoC}, in relation to a potential Application of Big Data scenario
- [*Synchronous/ Asynchronous*] Clock Tree Synthesis and Design Performance
- A low power SoC design for IoT fitting on NB-IoT (LPWAN)
- Low Power Design and Low Power Verification in {*SoC/Communication Chip*}
- Comparison of 28nm Design between Bulk CMOS and FD-SOI Technologies
- Integration of {3D | HBM | eFlash | SDD} in an {AI | Big Data | Data Center} Chip Design
- A Study of {ESD Models} and Design-For-Reliability

7 研究报告题目:

- Overview of SoC Design Features in {AI Application | Big Data Era}
- Review of Types of Architecture Design (CPU/GPU/DSP/ASIC/FPGA) for AI Applications
- IPs in a SoC design for IoT wearable/SmartHome/SmartCity
- EDA flow for a neuromorphic based SoC design containing CPU/GPU/DSP etc
- Comparison of 28nm Design between Bulk CMOS and FD-SOI Technologies
- ASIC Design methodology using TPU Flow2 with FPGA+CPU
- {Ionizing Radiation} Induced Reliability Issues in FPGA Designs
- An Overview of {*HBM / HPC / Cambricon*} SoC Design Features used in AI-Big Data Era （大数据时代{*HBM / HPC / Cambricon*}系统芯片设计特点回顾，选择 1-2 点深入讨论）
- Verification Methodology of IP in SoC Design (系统芯片设计中 IP 的验证方法介绍)
- 当代系统芯片设计中 IP 类型特点及其应用
- IBM 云计算中的 Power 芯片先进技术的集成
- Fabless SoC 设计与制造(非 IDM 设计公司模式)
- Progress in Studies of Formal Equivalence Checking
- Progress in Studies of Placement Algorithms (SAT)
- 布线算法研究的进展讨论
- {*Ionizing Radiation*} Induced Reliability Issues in FPGA Designs

8 作业提交

Email to (收件人): czchen126@126.com, CC: sunny_alice@126.com

Email Subject (邮件主题): **Title** of the report, **Name** of the contact author.

9 参考文献 (Sample References)

1. Chen, C. -Z. and Hu, D.Y., 2017, Geometry Effect with Respect to ESD and Radiative Charged Particles in SoC. Semiconductor Technology International Conference (CSTIC), 2017 China. (March 12-13, 2017, Shanghai.) **IEEE Conference Publications**, <http://ieeexplore.ieee.org/document/7919894/> (**pp. 1-3**, DOI: 10.1109/CSTIC.2017.7919894)
2. 翻译《数字模拟混合信号集成电路设计方法学指导》, 科学出版社(2015 年 1 月, ISBN 978-7-03-041959-0) 陈春章 何乐年 李智群 艾霞 等译
3. 专著《数字集成电路物理设计》, 科学出版社出版(2008 年 8 月, ISBN 978-7-03-022031-8) 陈春章 艾霞 王国雄 著

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撰写时间: 2018 年 3 月