University of Chinese Academy of Sciences

Verification & Implementation of SoC Design

SI-STA in Advanced SoC Design

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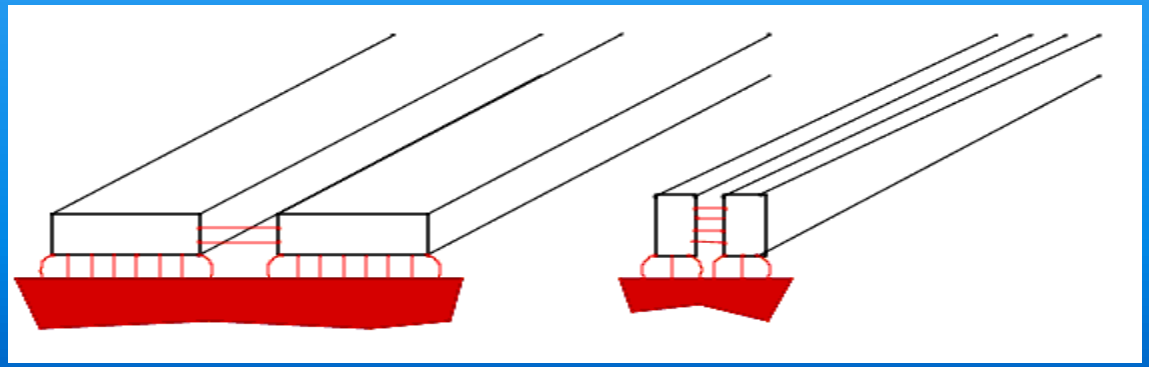
SI and SSTA in SoC Design

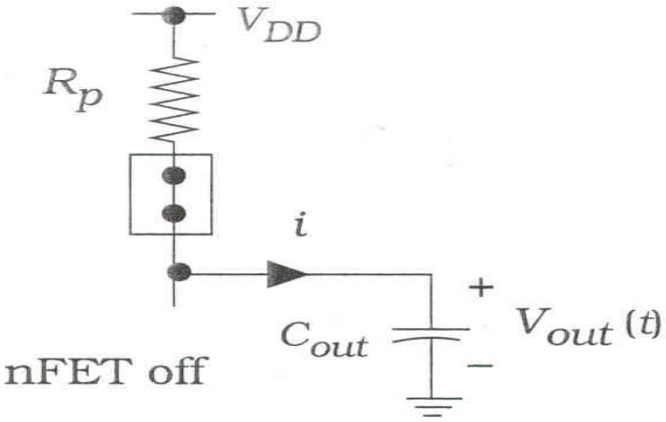
- SI and STA
- STA and SSTA
- MMMC
- OCV and AOCV
- Discussion

Significance of SI

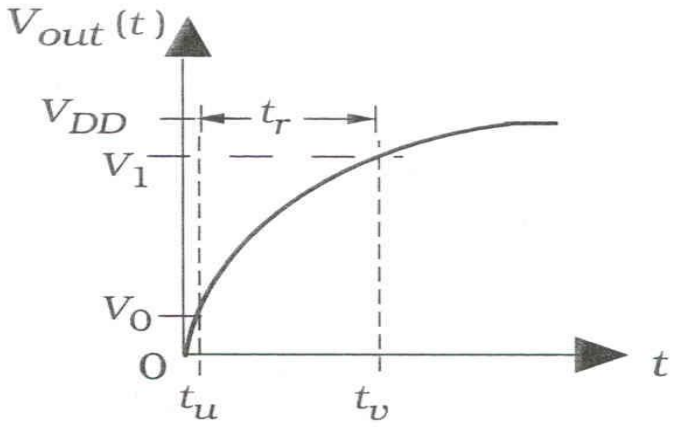
- Noise has become a significant problem for UDSM designs
- Noise can cause timing problems, functional failures and poor yields
- SI Analysis helps cell based designers achieve functional first pass silicon with the desired performance



Rise Time for MOS Gate (Inverter)

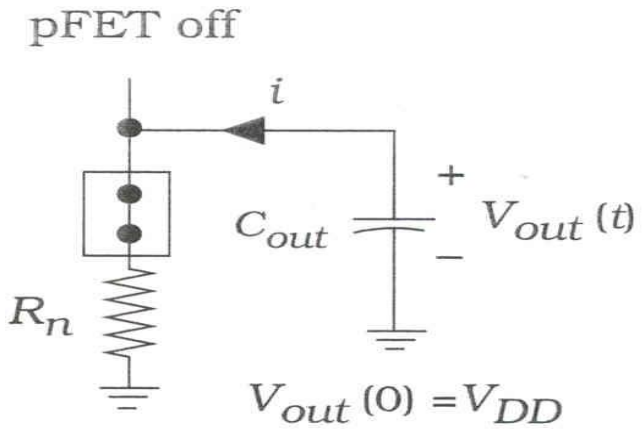


(a) Charge circuit

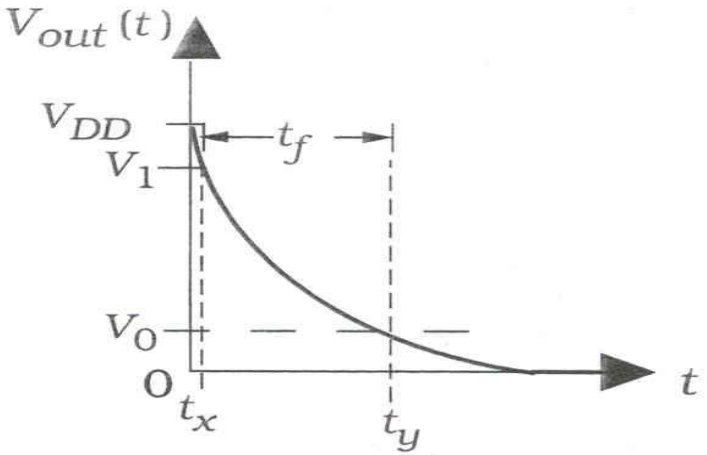


(b) Output waveform

Fall Time for MOS Gate (Inverter)



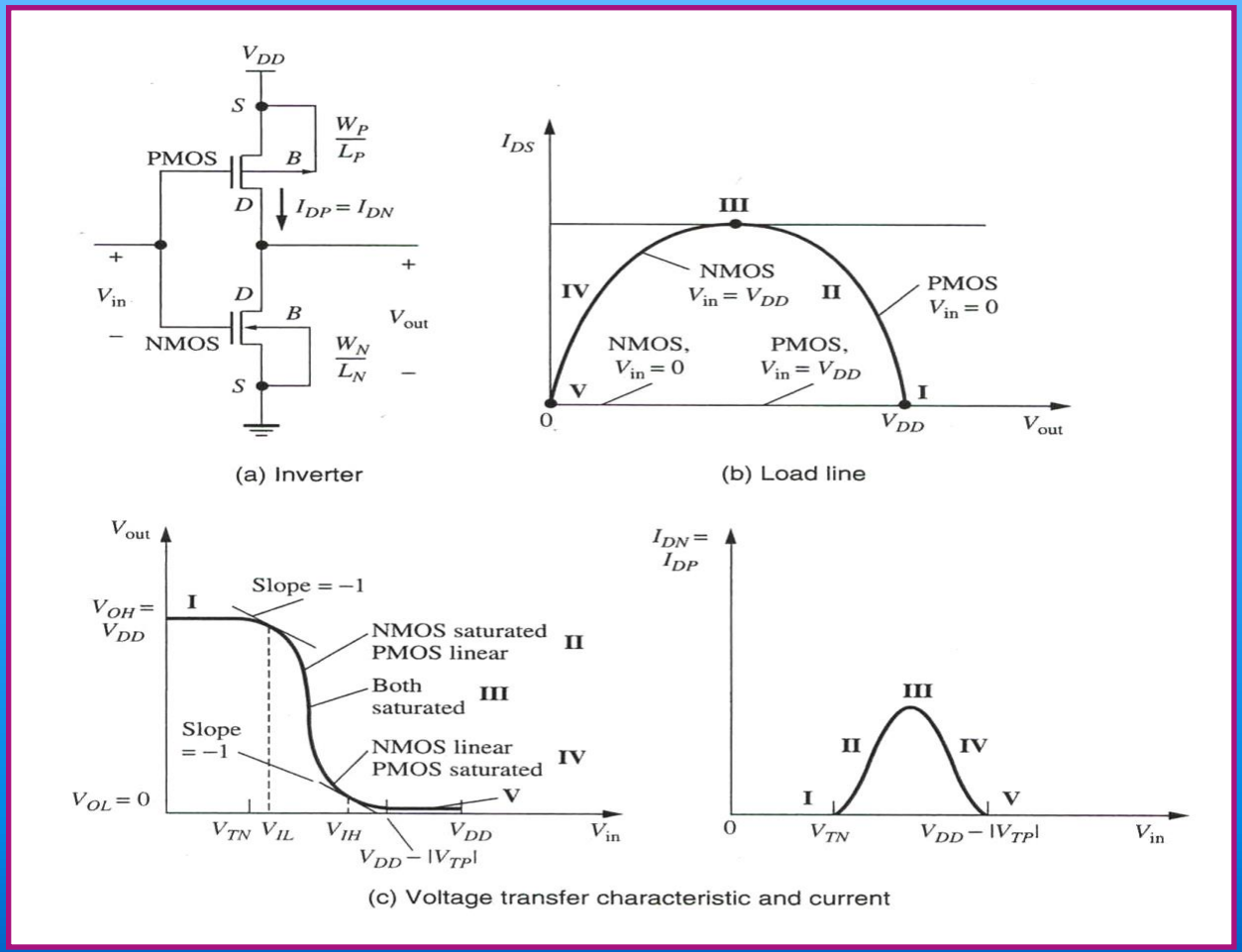
(a) Discharge circuit



(b) Output waveform

MOS Inverter

- $V_{in} \rightarrow V_{out}$
- a) Inverter
- b) Load Line
- c) Voltage & Current

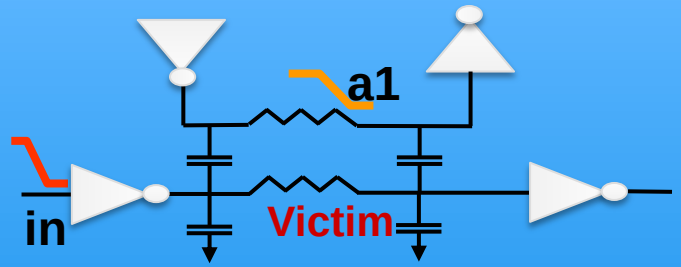


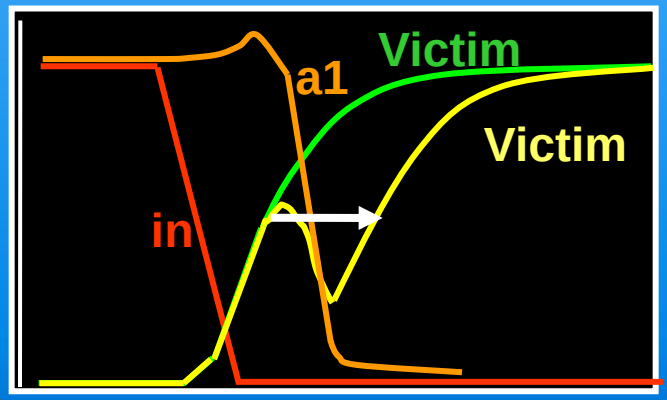
Cross-Coupling Effects

Impact of Noise on Delay

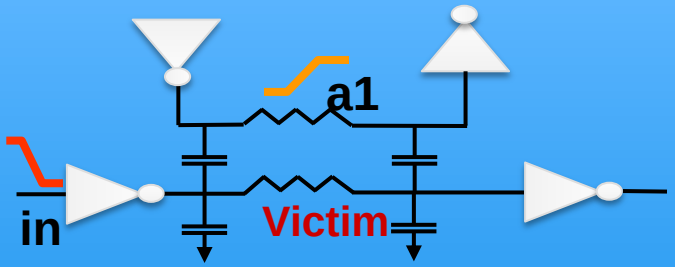
Coupling noise can impact max and min delay

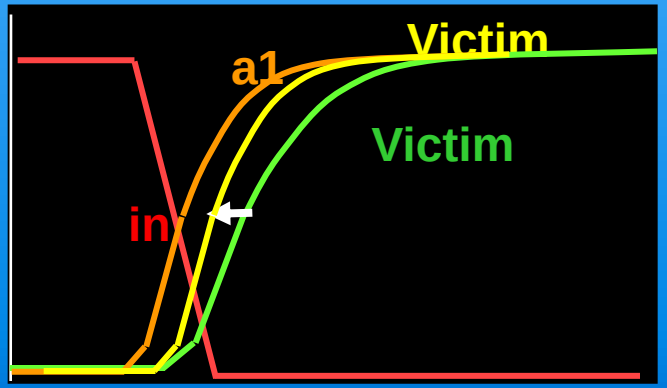
- Crosstalk or noise, can increase or decrease delay and cause setup or hold failures





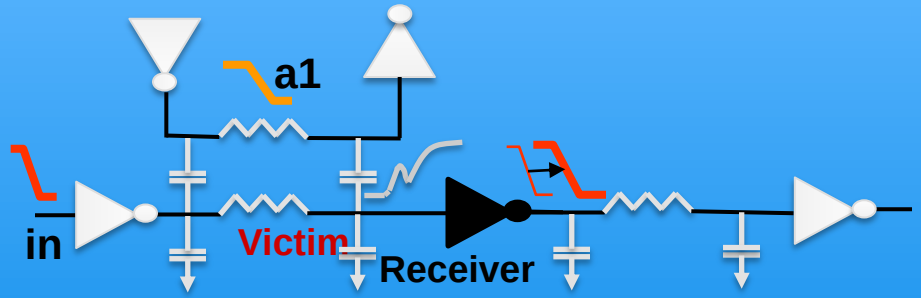
Crosstalk increases delay

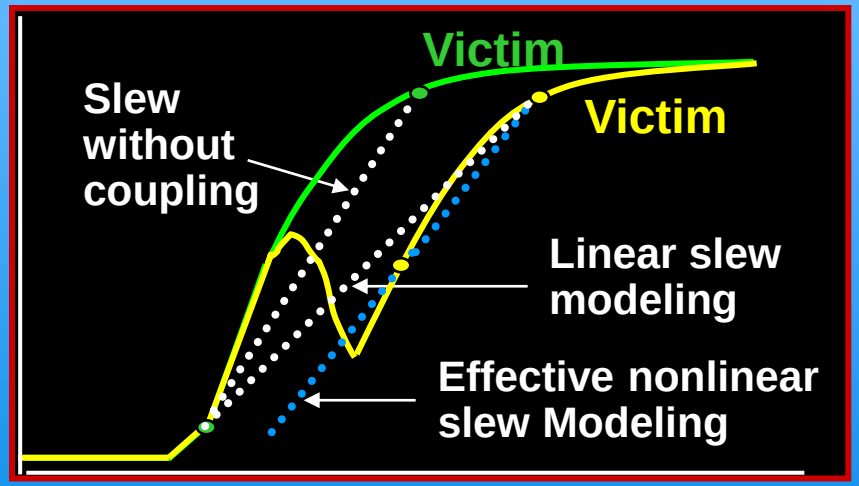




Crosstalk decreases delay

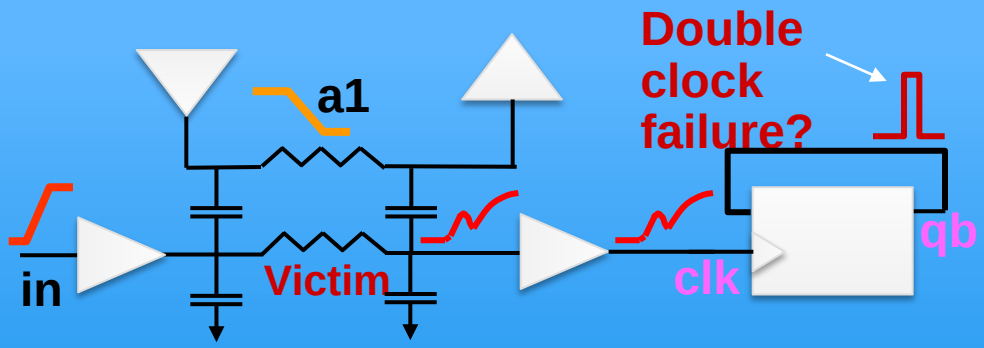
The Impact of Noise on Slew



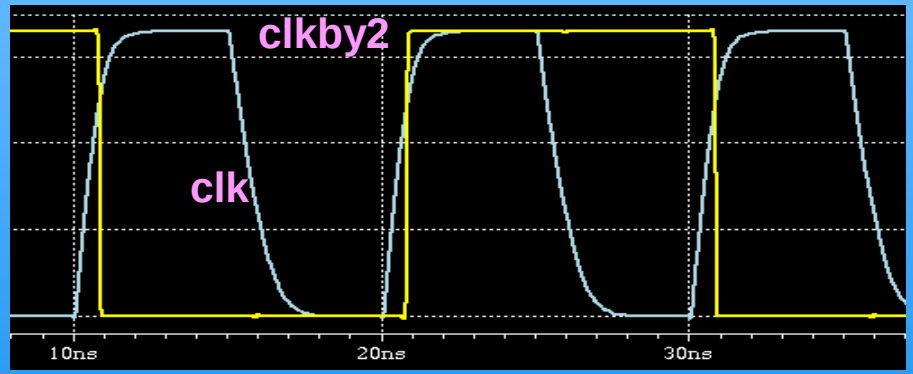


- Noise impacts victim slew.
- Victim slew changes impact receiver delay.

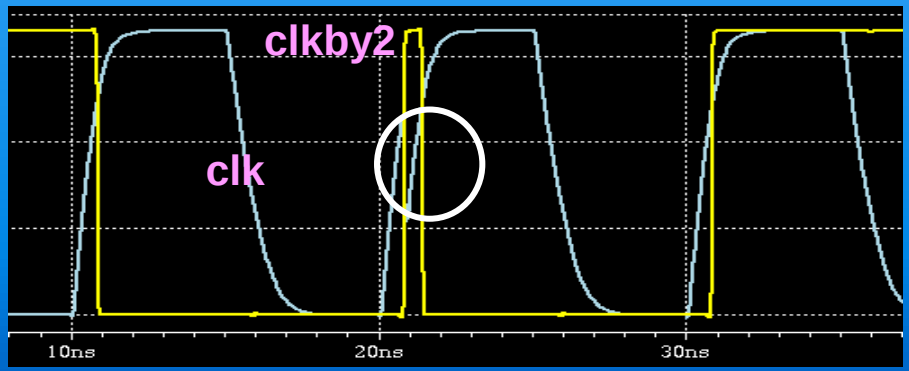
Double-Clocking Noise



Without crosstalk



With crosstalk



Crosstalk noise during a clock transition can cause double-clocking.

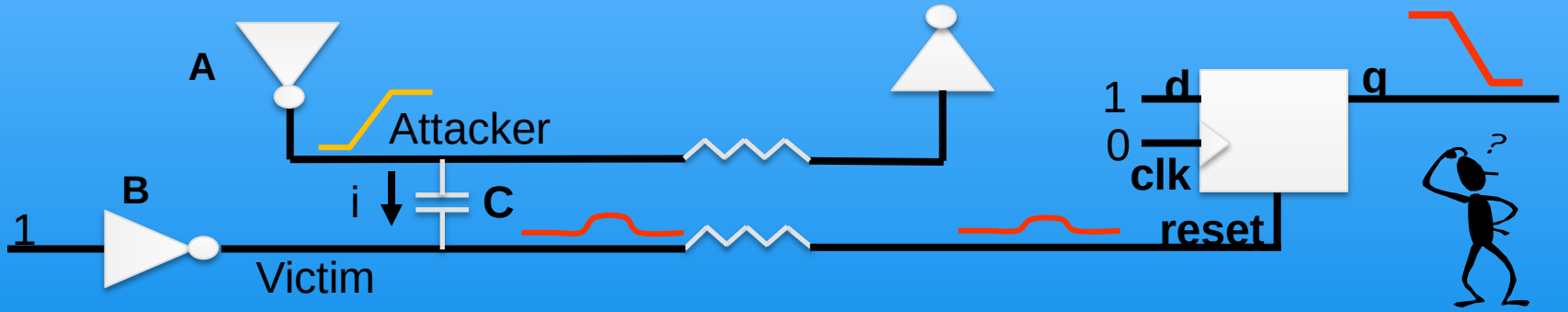
Use unique glitch and SI delay controls for a more detailed analysis of clocks.

Report the SI impact on clocks, sorted by

- Noise, SI delay, SI slew
- Opposite or zero slope

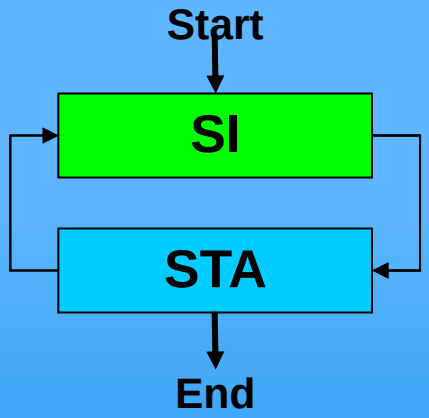
Impact of Noise on Functionality

- Coupling noise can cause functional failures.



i=Cdv/dt Slew rate and C set glitch current.
Load impedance sets glitch voltage.

SI Analysis Flow



Timing Library (.lib)
Timing-constraint file
Verilog
Tcl command file
Noise library(.cdB)
SPEF

SDF
Noise Abstract (XILM)
Timing windows

STA Tool

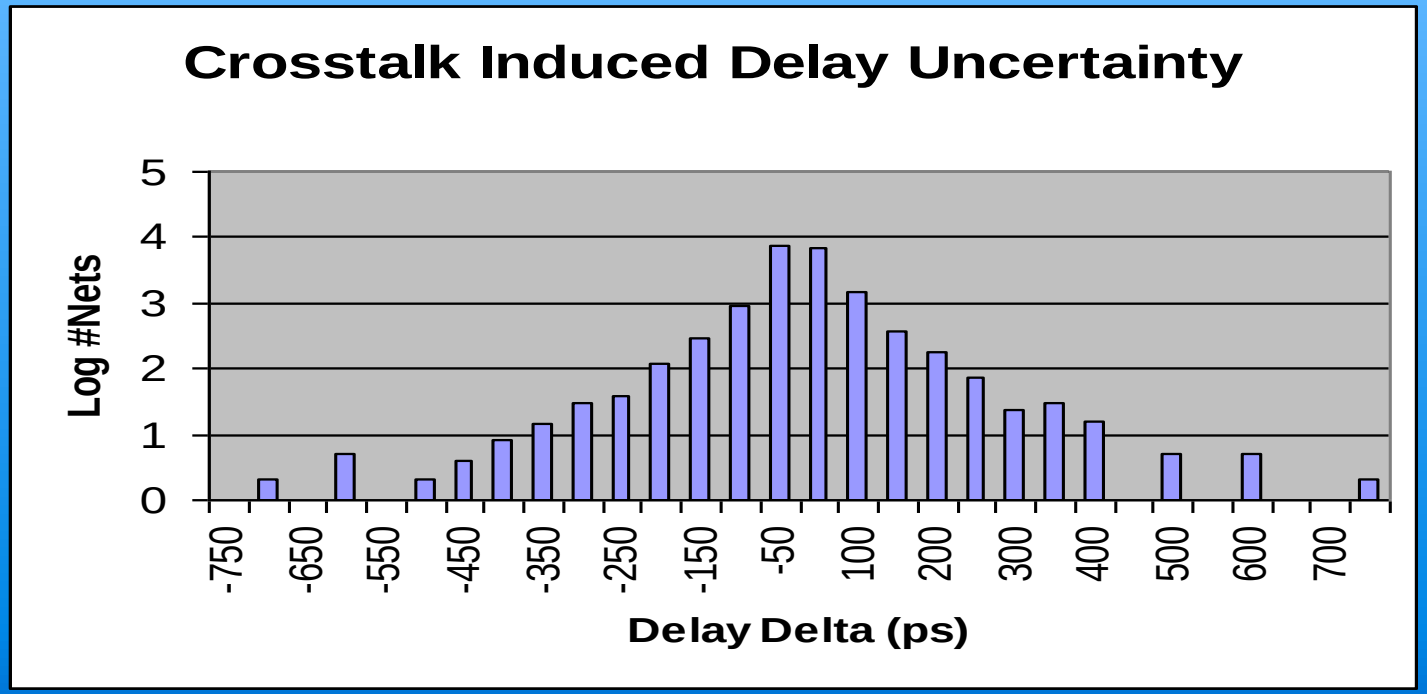
Schematic and physical layout for cross-probing
Histograms, Waveforms

Crosstalk reports
Delay uncertainty
ECO repair file
Incremental SDF

Required Inputs
Optional Inputs
Graphical
Outputs

Cross-Coupling Effects

Impact of Noise on Delay: example of 0.18 um design



Noise Library

- The Concept: Unity Gain Point (UGP)
  - UGP is the point where the slope of Vout Vs. Vin reaches 1 for the first time The .lib and BSIM4 models
- The .lib, BSIM4 and cdb file
- Characterization

Comparison of Noise Library Models

Noise Library Form	Format	Content	Details	Application	Conversion
cdB	bin	[1]Transistors	Noise thres, I/O pin cap, holding R	[1]Std cell, memory	TLF/.lib -> cdB
UDN	bin	Cell-level view	Black box, core of ECHO	Analog, RF	
ECHO	bin	Cells, [2]CCC and R/C network	Tolerance, holding R	[1]Std cell, [2]DSP	ILM -> XILM, ECHO
Stamp	Language			Std cell	Stamp -> cdB
ILM/XILM	SPEF, Verilog	Timing & noise	Tolerance, holding R	Std cell	

SI and SSTA in SoC Design

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Statistical STA started at 65nm

SI and SSTA

- SI is NOT “seen” in FED or system verification
  - SI started to be an issue at 180nm
  - SI may become problematic at block adjesent boundaries
  - SI analysis in hirarchical/partitioned design is a challenge!
- SSTA was expected to be “serious” problem at 65nm
  - Foundry process technology advancement
  - DFM and CMP procedures helps a lot
  - New challenges in 10nm with FinFET and SOI

Statistical Static Timing Analysis

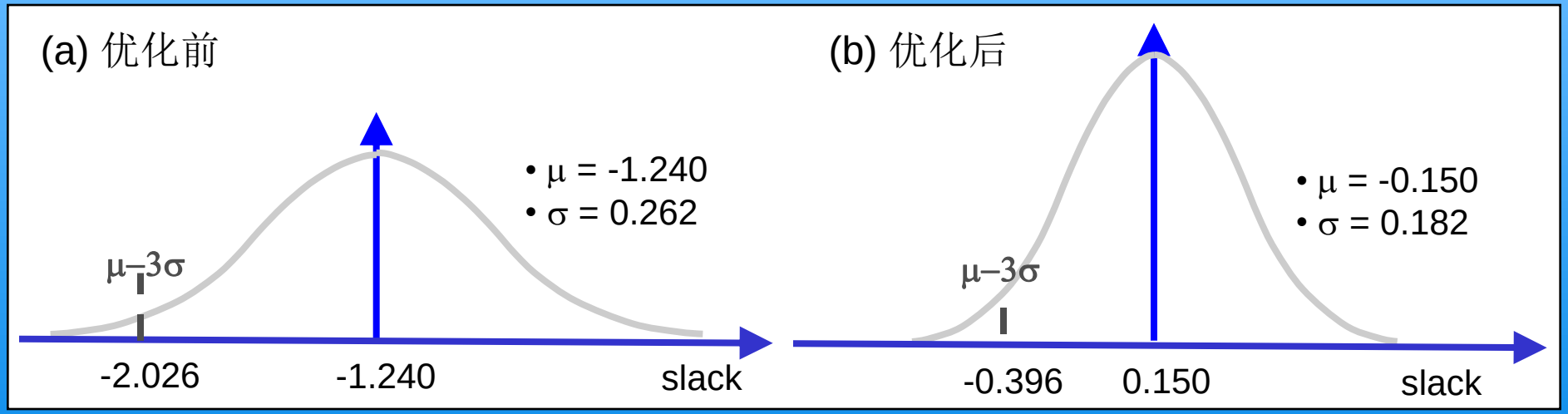
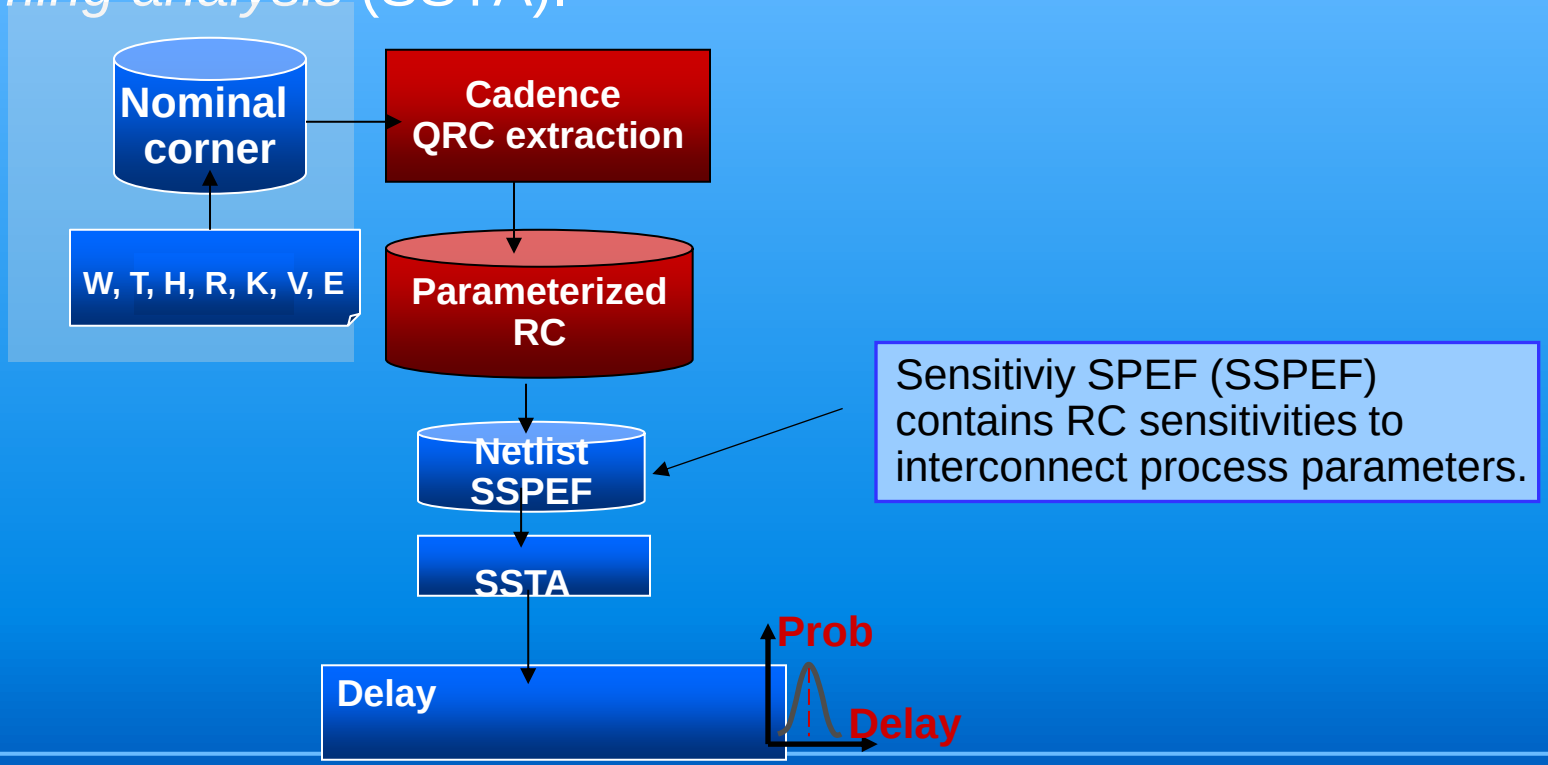


图6-37 用SSTA对某65nm设计进行优化处理前后的结果

(a) 用SSTA计算出的误差均值 μ =-1.240，标准误差 σ =0.262，其分布范围($\mu \pm 3\sigma$)较宽；(b) 优化后再用SSTA计算出的误差均值 μ =+0.150，标准误差 σ =0.182，其分布范围($\mu \pm 3\sigma$)变窄，并往坐标右方正值区域移动。

Sensitivity Extraction Plus Statistical STA

- Use *sensitivity extraction* in combination with *statistical static timing analysis* (SSTA).



SI and SSTA in SoC Design

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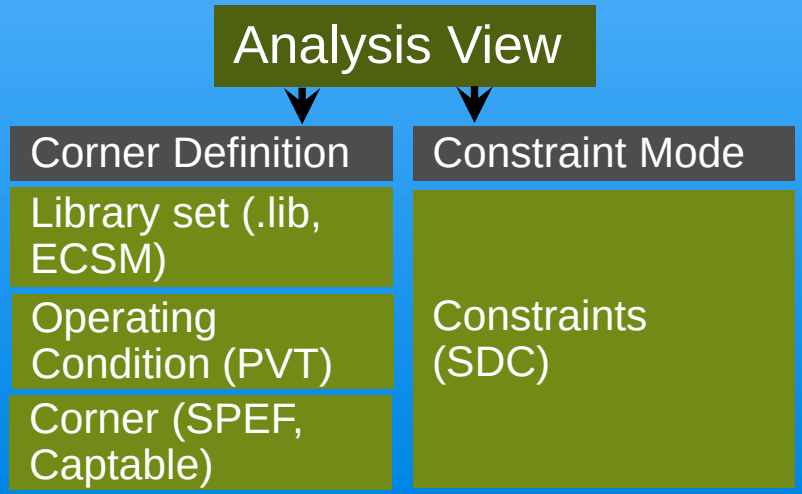
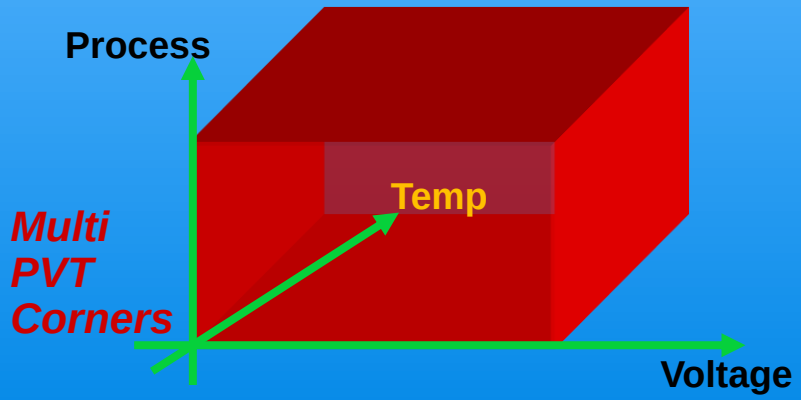
How MMMC Technology Works

View 1	View 2	View 3	View 4
Functional mode	Functional Mode	Functional Mode	Test Mode
FF corner	SS corner	TT corner	SS Corner

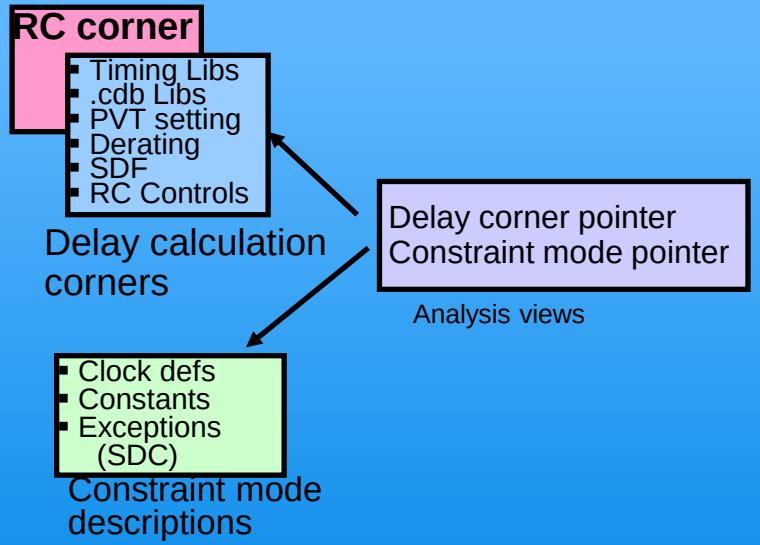




Concurrent analysis/optimization after views are set up

Definitions of Views, Corners, Modes etc

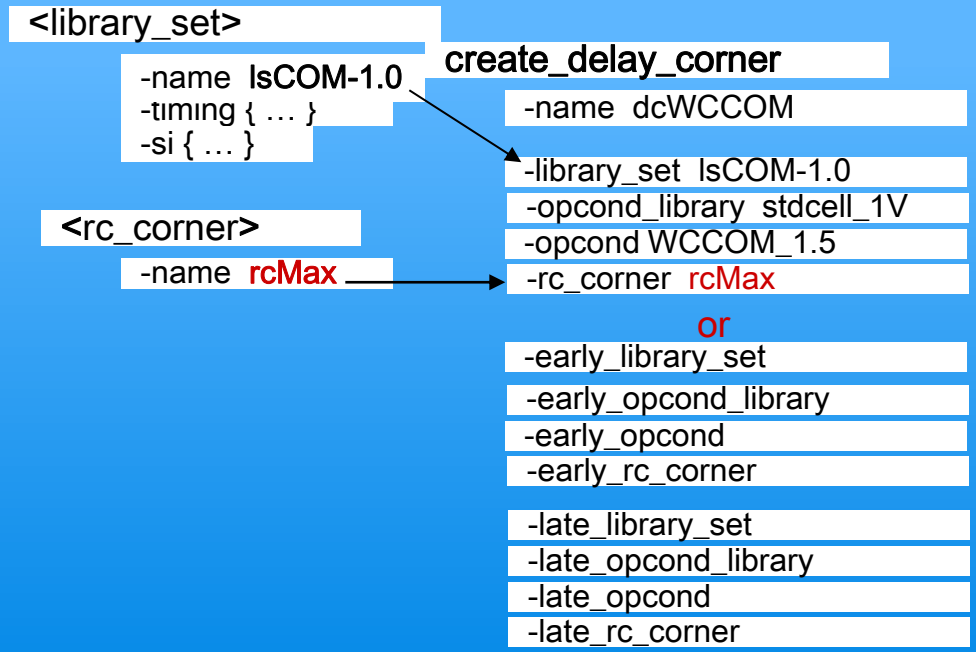
- MMMC uses a hierarchical approach so that you can assemble the appropriate information.
- Each top-level set of criteria is called an *analysis view*. Each view is composed of two pieces:
  - A corner, which describes all the information used to compute delays
  - A mode that describes the functional information used to drive the analysis



Modes and corners can be reused to create many different view variations.

Analysis and optimization work on the current set of active analysis views.

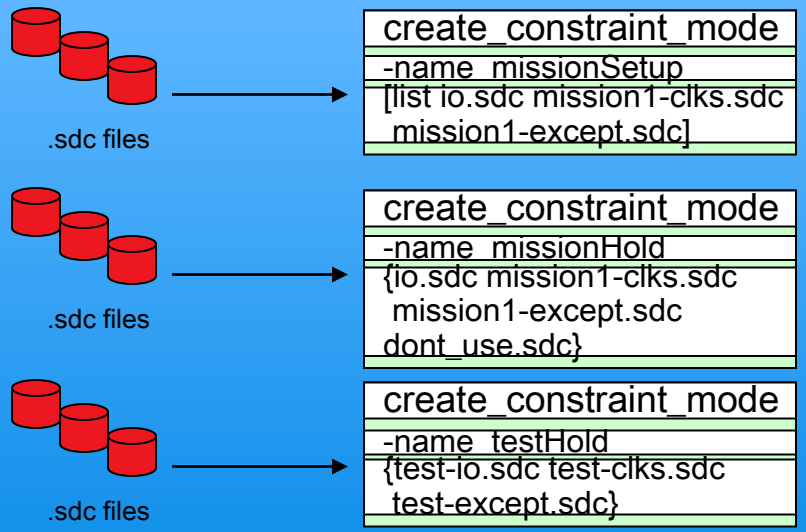
Corners for Delay Calculation




```
create_delay_corner -name dcWCCOM -library_set
lsCOM-1V
          -opcond_library stdcell_1V -opcond
WCCOM -rc_corner rc-cworst
```

- Delay calculation corners (*delay_corner*) provide all the information necessary to control delay calculation at a specific corner.
- The *delay_corner* controls
  - Library set selection
  - Operating condition (PVT point)
  - Selection of the RC corner
- The *delay_corner* can contain separate sections to control MSV domains in the design.
- The *create_delay_corner* command is used to define a delay calculation corner.
- The *update_delay_corner* command is used to update some attributes and to define MSV power domains.

Modes in SDC

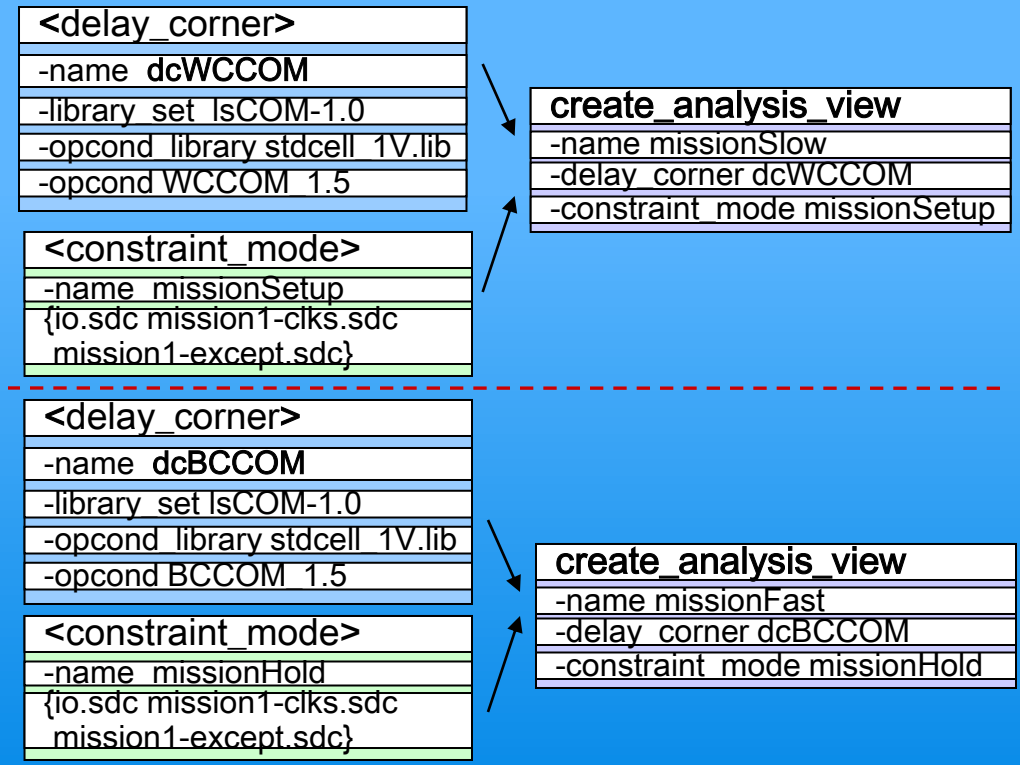


- Use the *create_constraint_mode* command to associate a Tcl list of SDC files with a named mode.
- SDC files can be shared by many different modes.
- A mode defines one of possibly many different functional, test behaviors, or DVFS modes of a design.
- SDC files contain conditional constraints that make each mode unique.

```
create_constraint_mode -name
missionSetup \
          [list io.sdc mission1-
clks.sdc mission1-except.sdc]
```

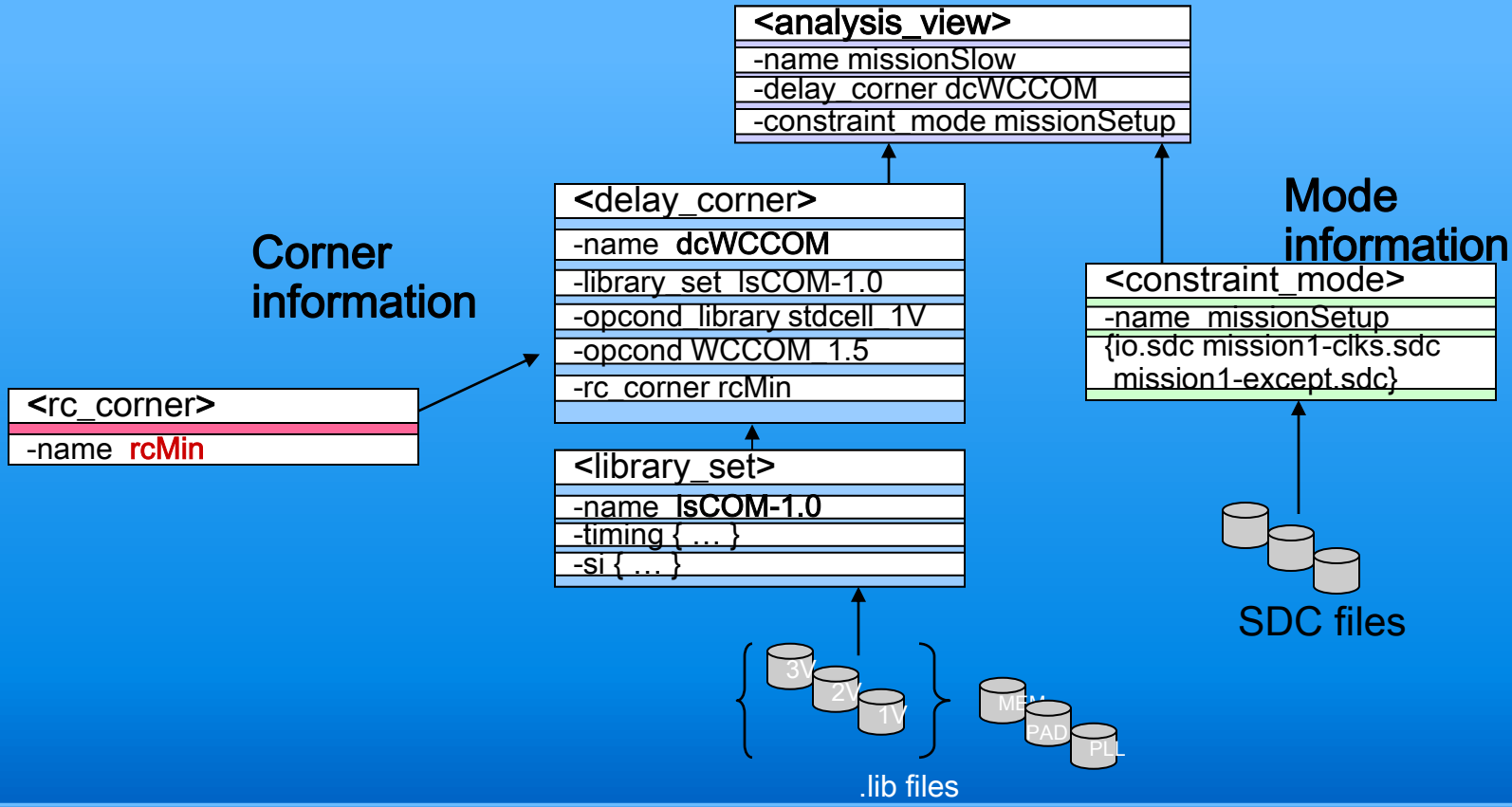
Views for Analysis

- An analysis view
  - Has all the information to control a given MMMC analysis
  - Contains a delay calculation corner and a constraint mode
- The *create_analysis_view* command is used to build a top-level association of a delay calculation corner with a constraint mode.




```
create_analysis_view -name missionSlow
\
        -delay_corner dcWCCOM \
        -constraint_mode missionSetup
```

Analysis in Combined View



MSMV Requirements

- CPF is required for any MSMV flow, to support both timing and power
- The CPF must define the power domain names etc

SI and SSTA in SoC Design

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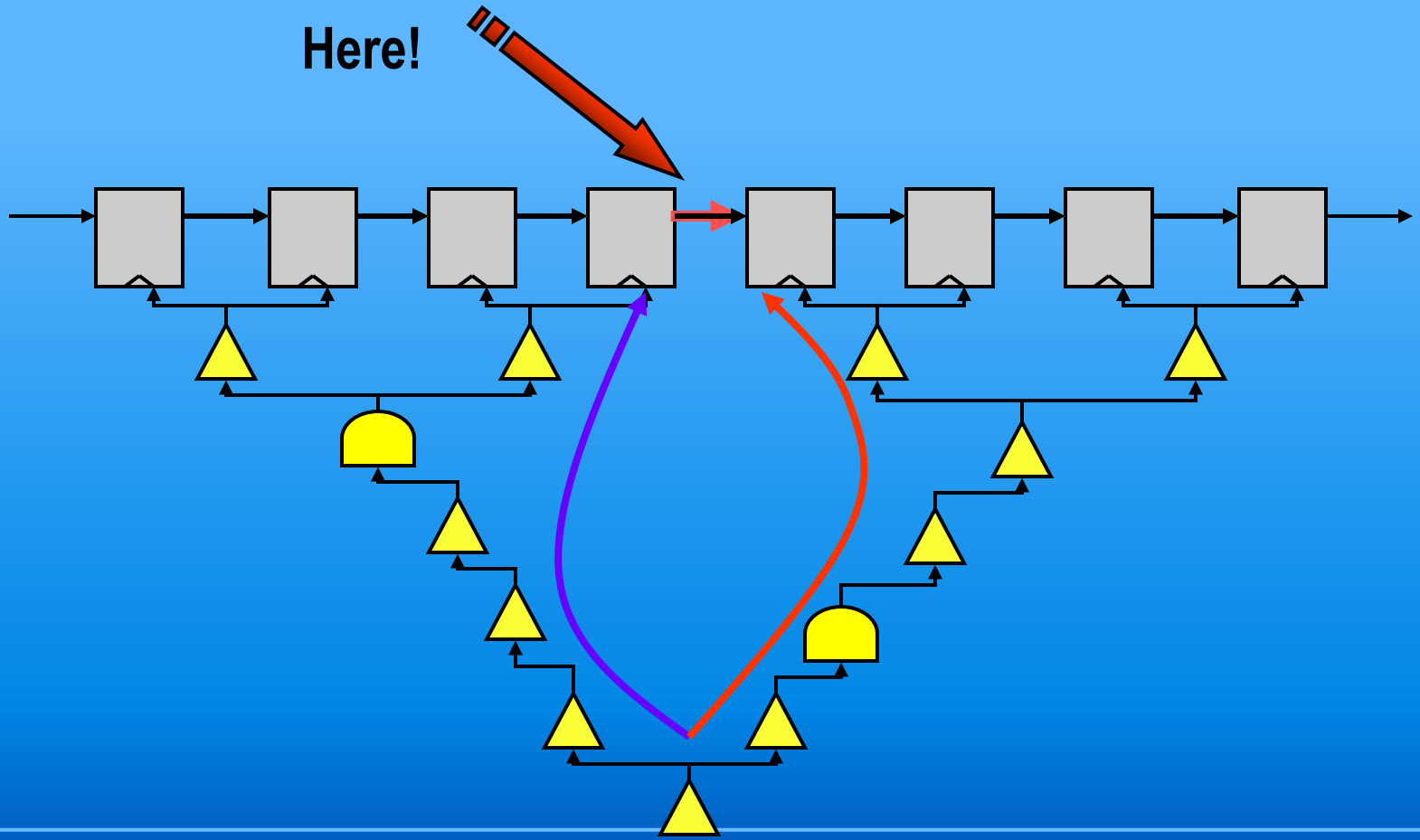
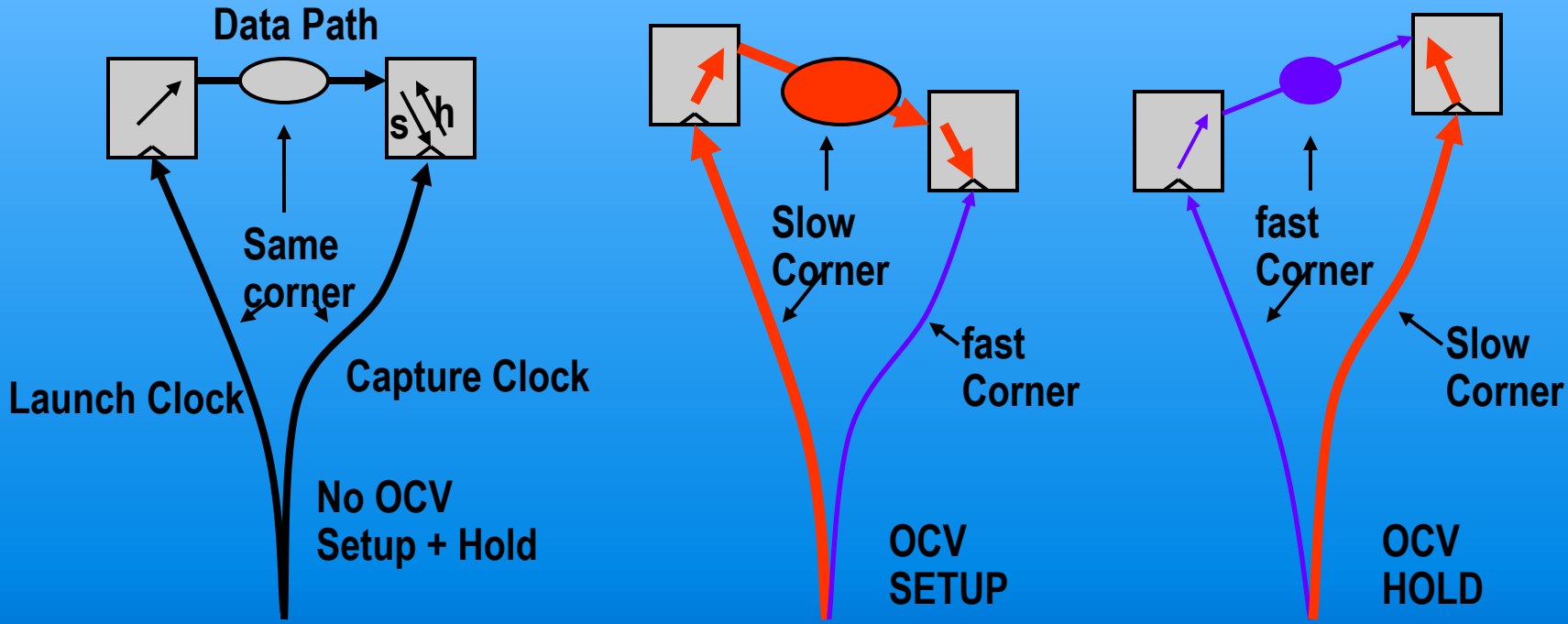
Where it hurts?



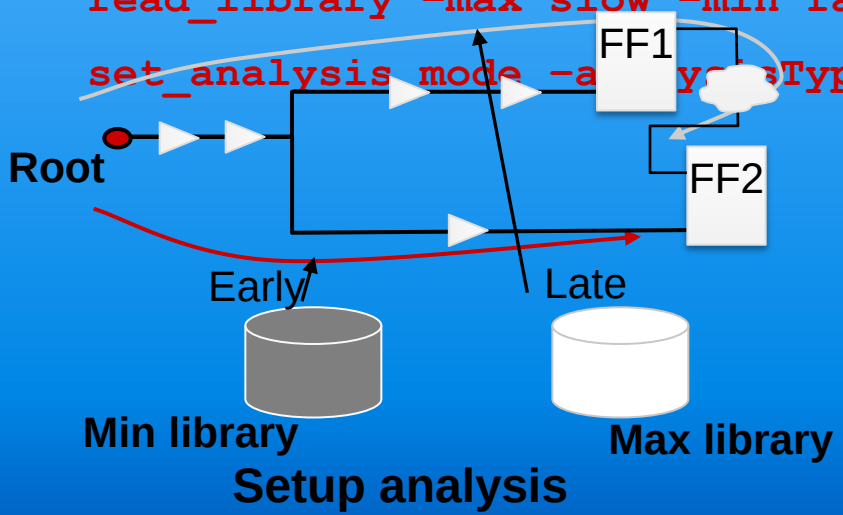
OCV Analysis

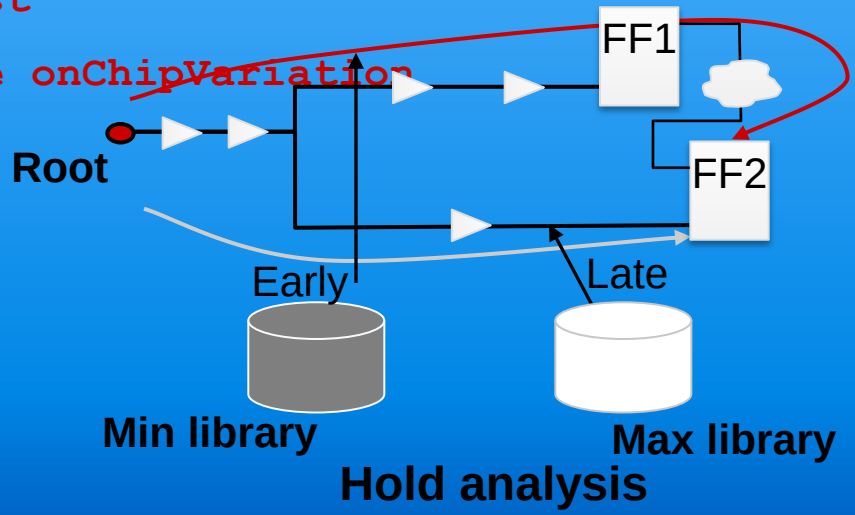


On-Chip Variation Analysis Mode

- In the on-chip variation analysis mode, the software calculates the delay for one path based on the maximum operating condition while calculating the delay for another path based on the minimum operating condition for setup and hold checks.

```
read_library -max slow -min fast
set_analysis_mode -analysisType onChipVariation
```



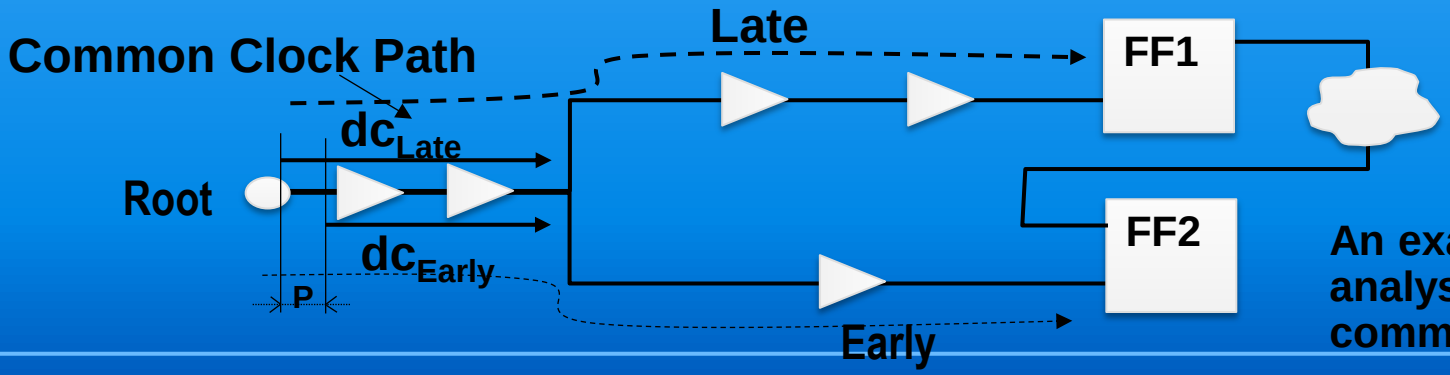


Clock Reconvergence Pessimism Removal

- To account for clock reconvergence pessimism removal (CRPR) in a common clock path or reconvergent clock path, use the following:

```
set_analysis_mode -checkType setup -cppr setup
```

  - The common part of the clock path cannot physically have a different timing in late and early analyses.
  - Considering a different delay implies a pessimism that is the difference of delay between late and early analyses on the common clock path.
  - The pessimism: P = dcLate – dcEarly
  - New slack = slack(w/o CRPR) + P



An example of setup analysis with a common clock path

Launch and Latch Clock Paths

Setup check:

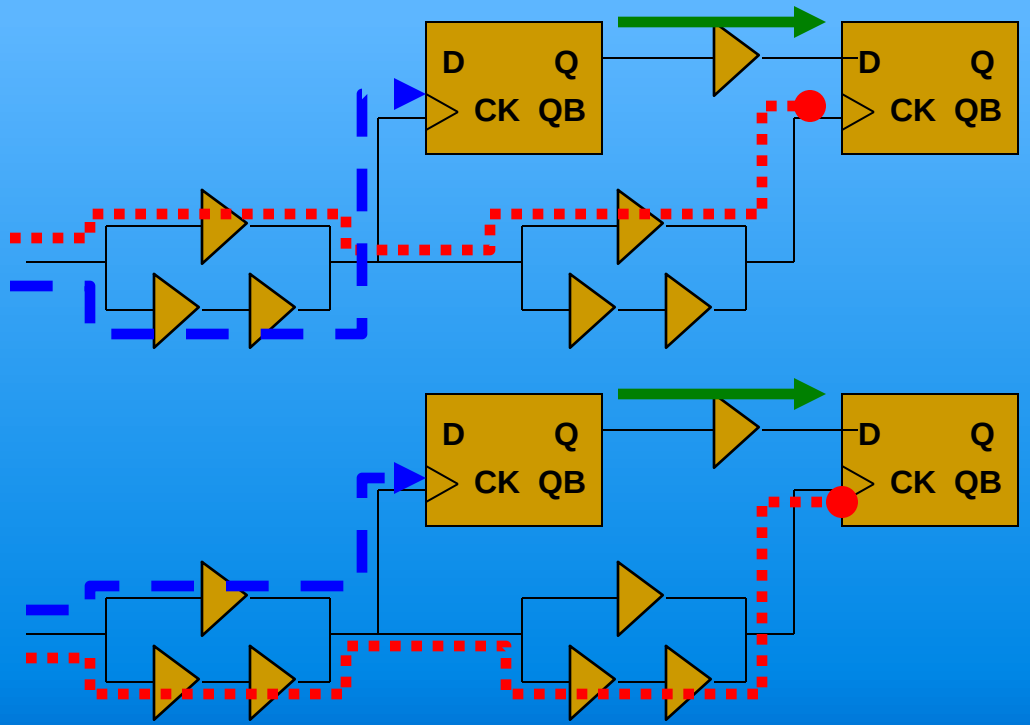
Launch clock: longest path

Latch clock: shortest path

Hold check:

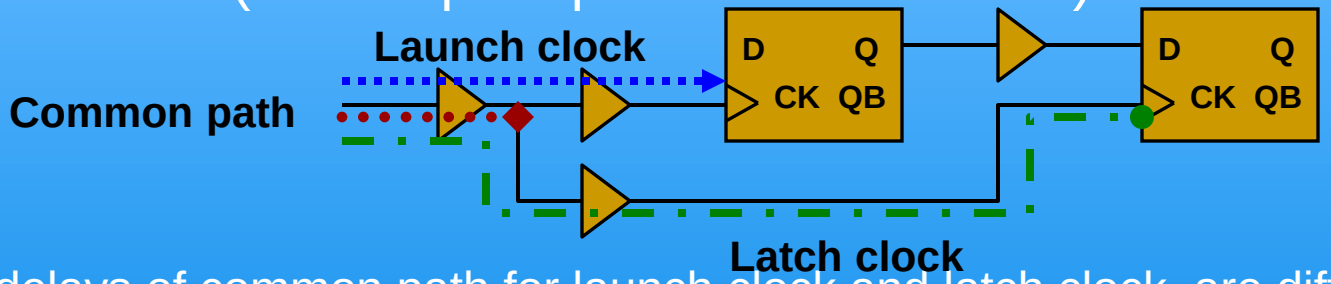
Launch clock: shortest path

Latch clock: longest path



CPPR and CRRP

- PT: CRPR (clock reconvergence pessimism removal)
- STA: CPPR (“clock” path pessimism removal)



- The delays of common path for launch clock and latch clock are different.
  - Consider real physical behavior, the delay variation of common path for launch and latch clock is almost 0(ignorable).
- CPPR is a technique to get more accurate slack by removing the delay variation of common clock path.
  - Setup: CPPR = MAX (launch-delay(common path) – latch-delay(common path), 0).
  - Hold: CPR = MAX (latch-delay(common path) – launch-delay(common path), 0).

Path-Based Analysis (PBA) and AOCV

The MMMC SignOff ECO feature supports timing optimization in Path-Based Analysis including the SI mode.

The different types of Path-Based Analyses supported are

- ✓ **aocv: Re-timing the timing critical paths using the LOCV derating factors**
- ✓ **path_slew_propagation: Re-timing the timing critical paths using the actual slews for the path**
- ✓ **aocv_path_slew_propagation: Combining the re-timing with aocv + path_slew_propagation**
- ✓ **waveform_propagation: Re-timing taking the waveform effect during delayCal into consideration**

	Hold fixing in PBA (path_slew_propagation) vs. GBA	
	Gain in added area	Gain in number of inserted buffers
Design 1	4.7%	4.3%
Design 2	0.4%	0.45%
Design 3	2.3%	2.8%
Design 4	5.7%	6.6%

Applying Path-Based Analysis lets you remove some timing pessimism and leads the tool to fix only the real timing violations.

SSPEF Sample (Decoupled Mode)

- //CDN *SENSITIVITY_VARIABLES
- //CDN *1 METAL_1 "M0" "T" -24.000000 43.099998
- //CDN *2 METAL_1 "M0" "W" -12.000000 11.900000
- //CDN *3 METAL_2 "M1" "T" -34.099998 58.799999
- ……
- //CDN *SENSITIVITY_COMPOSITE
- //CDN *1 (2 1)
- //CDN *2 (4 3)
- //CDN *3 (6 5)
- …
- //CDN *10 (3 4 20 21 22 23)
- ……
- *D_NET *140220 90.6436

Nominal RC

- *CONN
- *P REG_ADDR[5] O *C 640.12 0.14
- *I *1407:Z O *C 202.48 48.06 *D BUFFD6

- *CAP
- 0 REG_ADDR[5] 2.8377 //CDN *10 3f 9.42863e-05 2.04546e-05 0.000156954 -7.2902e-06 0.000149454 -5.24042e-05
- 1 *1407:Z 0.0583986 //CDN *10 3f 9.42863e-05 2.04546e-05 0.000156954 -7.2902e-06 0.000149454 -5.24042e-05

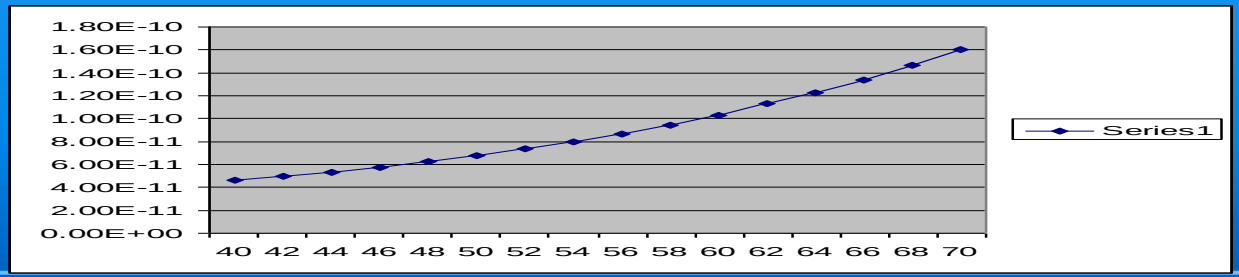
- *RES
- 0 *140220:7 *140220:9 46.3421 //CDN *3 3 -0.165899 -0.326531
- 1 *140220:8 *140220:7 49.3521 //CDN *3 3 -0.165899 -0.326531
- 2 *140220:10 *140220:8 49.2599 //CDN *3 3 -0.165899 -0.326531
- 3 *140220:9 *140220:11 17.624 //CDN *3 3 -0.0665585 -0.131004

SI and SSTA in SoC Design

- SI and STA
- STA and SSTA
- MMMC or MCMM
- OCV and AOCV
- Discussion

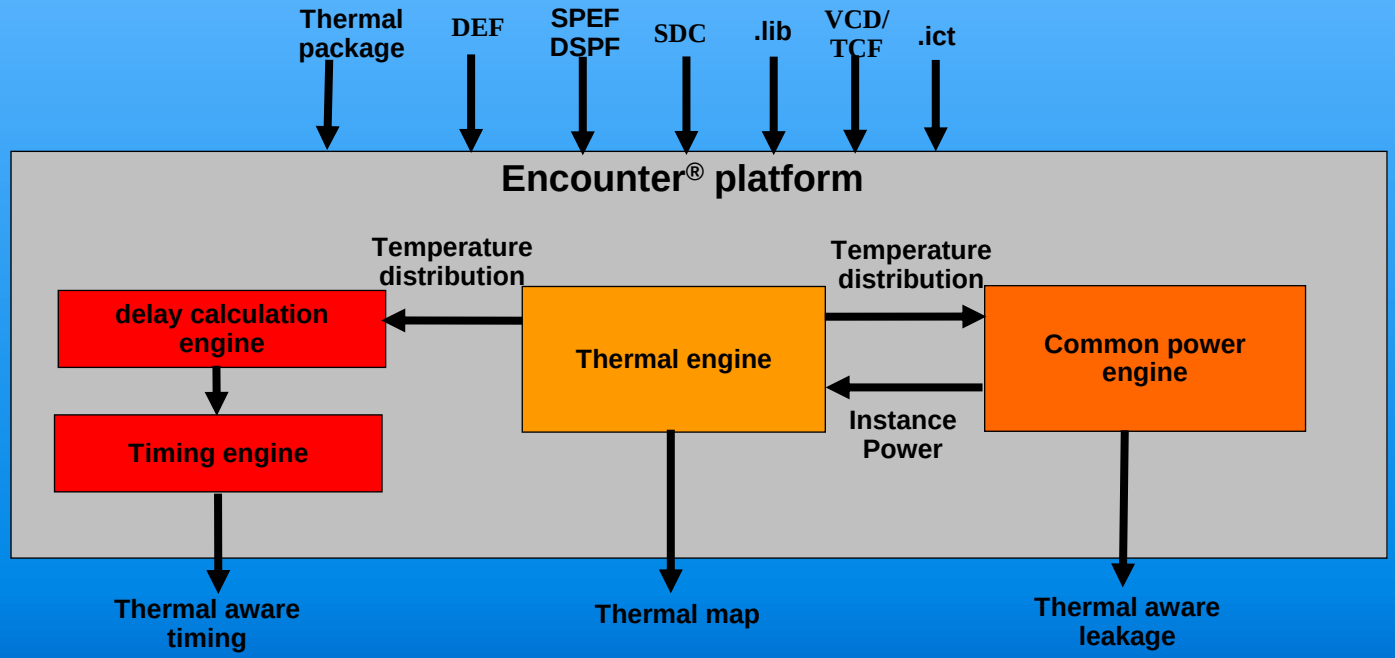
Thermal Analysis

- Transistor efficiency is a function of its temperature
- Temperature gradients can effect performance of analog circuits.
- Understanding the temperature on your chip is important
- Thermal analysis flow requires the following inputs to generate the thermal map file
  - Design data, Instance power file, Technology information
  - Thermal package information, Ambient temperature



Thermal Analysis Flow

- Example



Q&A, Discussion

- Which should be analyzed first, STA or SI? Why?
- Is SSTA related to DFM?
- Is MMMC related to Reliability or Yield?
- Discuss the difference between OCV and AOCV