University of Chinese Academy of Sciences

SoC Design with Advanced Technology

FD-SOI, FinFET, Quantum & Beyond

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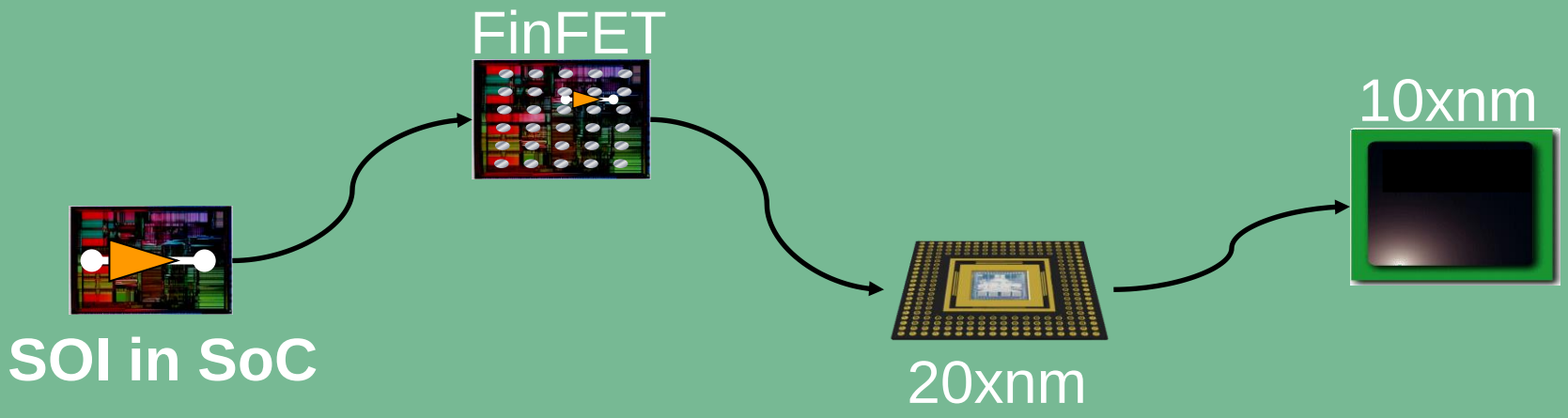
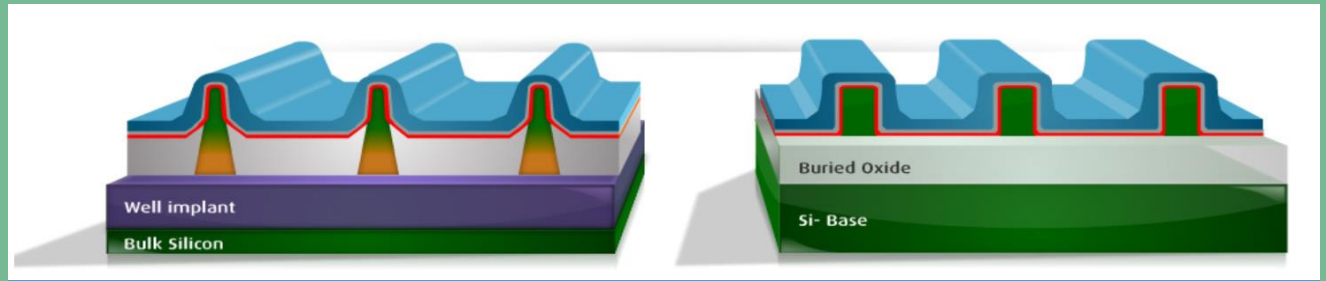
June 25-29, 2018

中国科学院大学2018年夏季

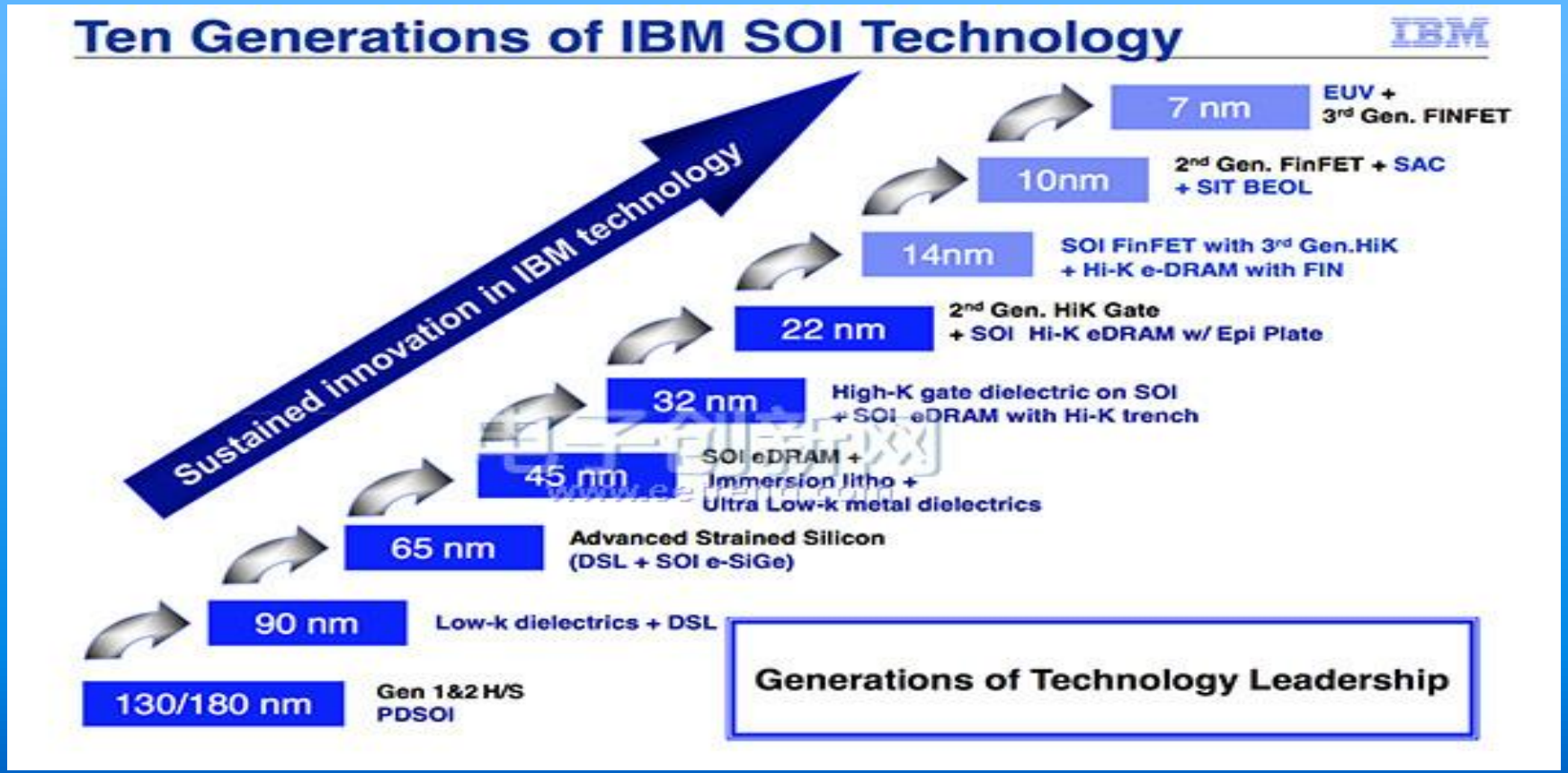
Advanced Technology in SoC
From Planar (2D) to 3D





Bulk FinFET Definition **Fins on Oxide Definition**

SOI Tech at IBM



Intel vs TSMC and Samsung

Intel	TSMC		Samsung	Others
??	28		32	
28	20?			
22	16|16+	~19	14	
14	10			
13	7			

	Intel	TSMC	Samsung	Intel
Process Name	22nm HP	16nm FF+	14nm FF	14nm HP
Supply Voltage (Vdd)	0.75V	0.75V	0.8V	0.7V
Minimum Gate Length	26nm	30nm	20nm	20nm
Contacted Gate Pitch	90nm	90nm	78nm	70nm
Minimum Metal Pitch	80nm	64nm	64nm	52nm
HD SRAM Cell Size	0.092um2	0.070um2	0.064um2	0.050um2
Apple A9 Die Size	Not applicable	104.5mm2	96mm2	Not applicable
Volume Production	**2Q12**	**3Q15**	**1Q15**	**4Q14**

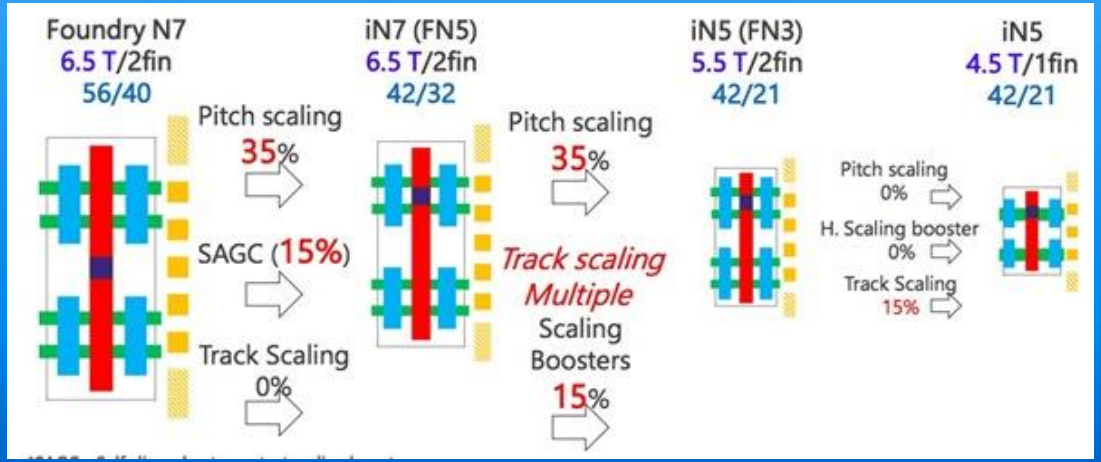
Minimum Feature Size

	Intel 22 nm	Intel 14 nm	TSMC 16 nm	Samsung 14 nm
Transistor Fin Pitch	60 nm	42 nm	48 nm	48 nm
Transistor Gate Pitch	90 nm	70 nm	90 nm	84 nm
Interconnect Pitch	80 nm	52 nm	64 nm	64 nm
SRAM Cell Area	.1080 um^2	.0588 um^2	.0700 um^2	.0645 um^2
			S.-Y. Wu 2014 IEDM p. 48	T. Song 2014 ISSCC p. 232

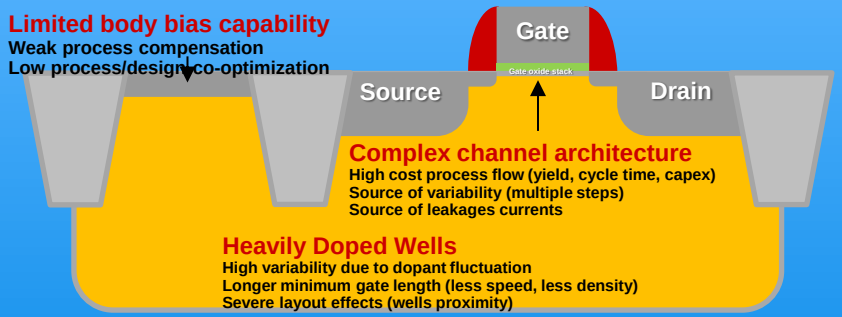
Intel has developed a true 14 nm technology with good dimensional scaling

The Industry First 3nm Tape Out (02/28/18)

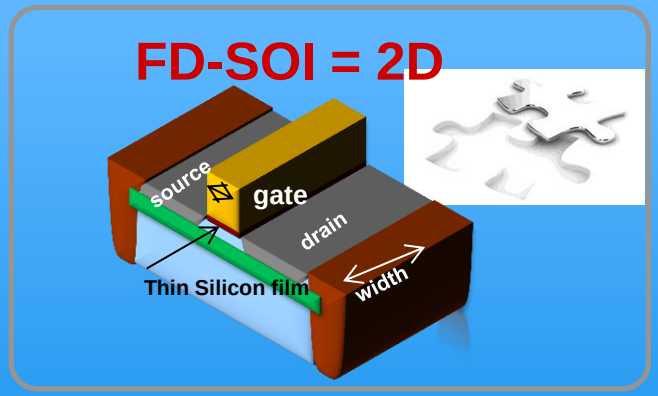
- (2015 5nm Tape Out)
- EUV (Extreme ultraviolet) and 193i (193 immersion lithography technology)
- 64-bit CPU (FinFET, 21nm routing pitch)

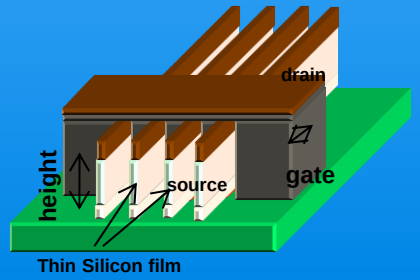


FD-SOI vs Bulk CMOS



Depleted devices deliver improved electrostatic control and device scalability





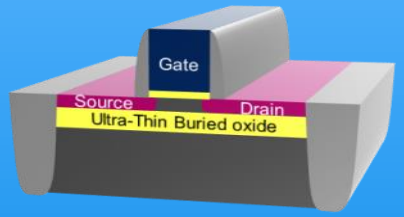
FinFET = 3D

Efficient FD-SOI Transistors

- FD-SOI enables better transistor electrostatics
  - Enabling faster operation at low voltage, leading to better energy efficiency
  - Improving transistor behavior, especially at low supply, enabling ultra-low-voltage operation
  - Reducing transistor variability sources
- FD-SOI has a shorter channel length
  - 28nm FD-SOI is in reality a **24nm** technology!
- FD-SOI has lower leakage current
  - Lower channel leakage current
    - Carriers efficiently confined from source to drain
  - Thicker gate dielectrics, leading to lower gate leakage
  - Enabling ultra low power SRAM memories
  - Leakage current is less sensitive to temperature with FD-SOI

FD-SOI is Simpler

- FD-SOI significantly reduces the process complexity



28nm FD-SOI

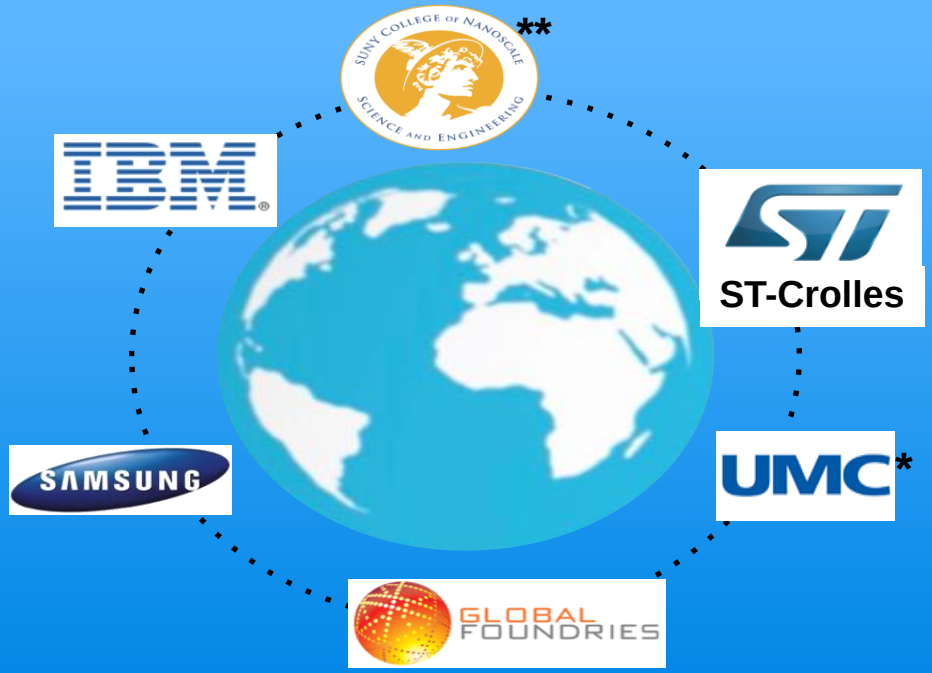
38 Masks

For 8 Metal Layers

28nm Bulk LP: 45 Masks

28nm Bulk G mobile: >48 Masks

SOI and ISDA



ISDA Members:

IBM, AMD/GF, FSL, IFN,

NEC, Samsung, STM, Toshiba

SOI vs Bulk CMOS

- **FD-SOI**
- **PD-SOI**

Proposed RM of FD-SOI Technology

- Extending 28nm to below
- UTBB FD-SOI

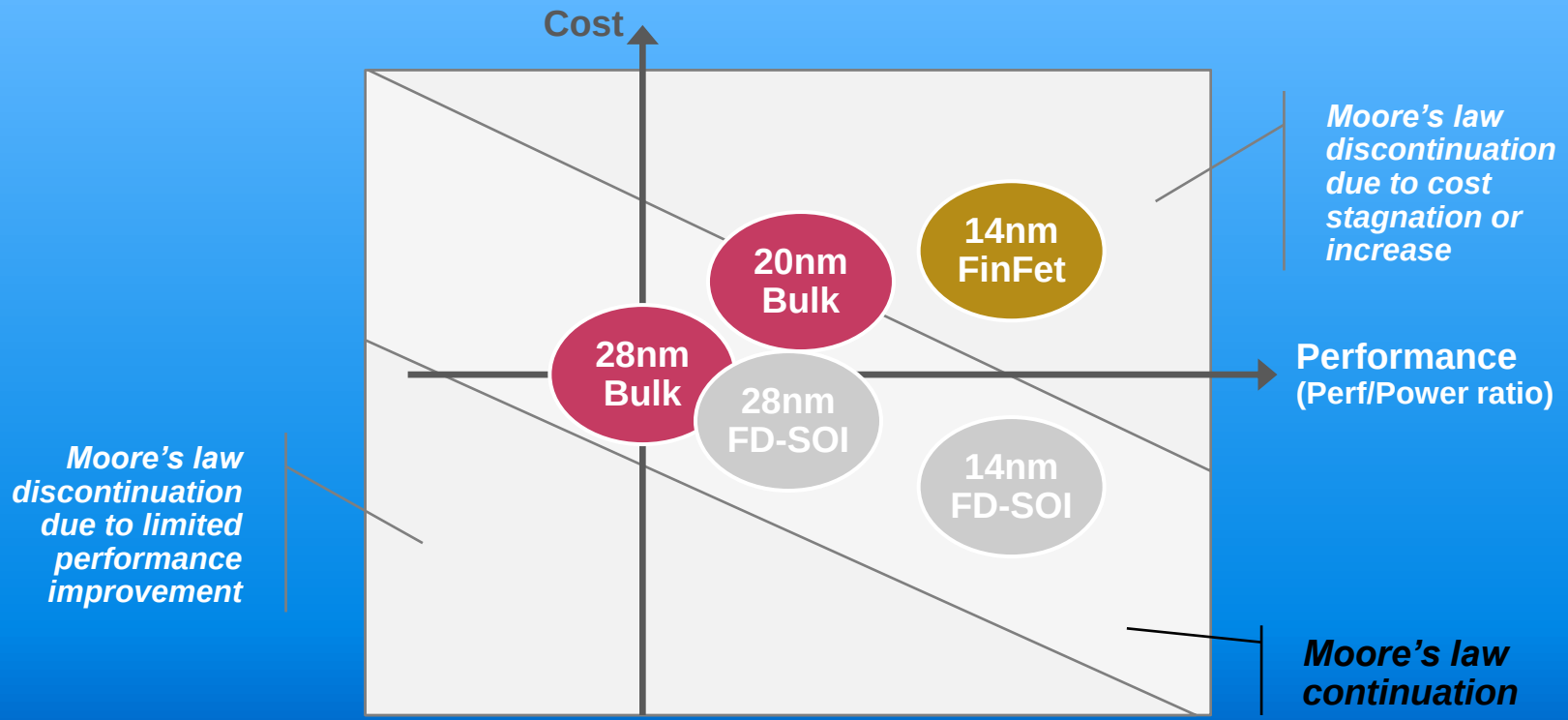
LEVERAGE DEVELOPMENT ECOSYSTEM IN GRENOBLE/FRANCE AREA

10nm FD-SOI 2017

14nm FD-SOI 2015

28nm FD-SOI 2012

Moore’s law on Planar Technology



Smart Cut™ Technology

- Soitec, Bernin, Grenoble
  - Patent # US5374564
- CEA-Leti

Studies on FD-SOI

- SOI Consortium

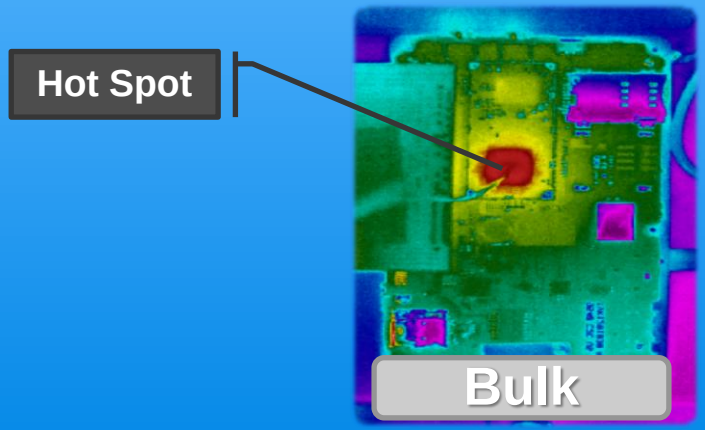
PRESENTATIONS

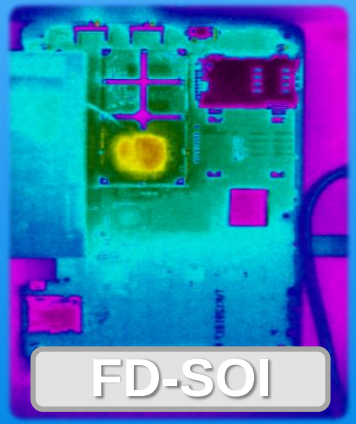
Feb. 15, 2011	Evaluation of Fully-Depleted SOI for next generation Mobile Consumer Chips [Horacio Mendez, Executive Director, SOI Industry Consortium]
Jan. 28, 2010	SOI – The next five years: The critical role that SOI will play in the semiconductor market EuroSOI 2010 – Grenoble, France [Horacio Mendez, Executive Director, SOI Industry Consortium]
Jul. 28, 2009	SOI – Integrated Technology, IP and Design Flow for Customer Success 46th Design Automation Conference – San Francisco, CA, USA [Gordon Starkey, IBM Systems & Technology Group; David Desharnais, Group Marketing Director, Cadence Design Systems; Tom Lantzch, VP Marketing, ARM]
Jul. 28, 2009	Low-Power Design with Material Impact on Silicon-on-Insulator Technology 46th Design Automation Conference – San Francisco, CA, USA [Horacio Mendez, Executive Director, SOI Industry Consortium]
Jul. 28, 2009	The Truth About Power and Process Technology 46th Design Automation Conference – San Francisco, CA, USA [Horacio Mendez, Executive Director, SOI Industry Consortium]
Apr. 9, 2009	SOI technology & emerging applications [Horacio Mendez, Executive Director, SOI Industry Consortium]

Comparison on FD-SOI and Bulk CMOS

Cooler Smartphone can be used for longer time

Running applications simultaneously on both L8540 & L8580 platforms configured with same settings (max 1.85GHz). Monitoring temperature and power consumption for the digital part





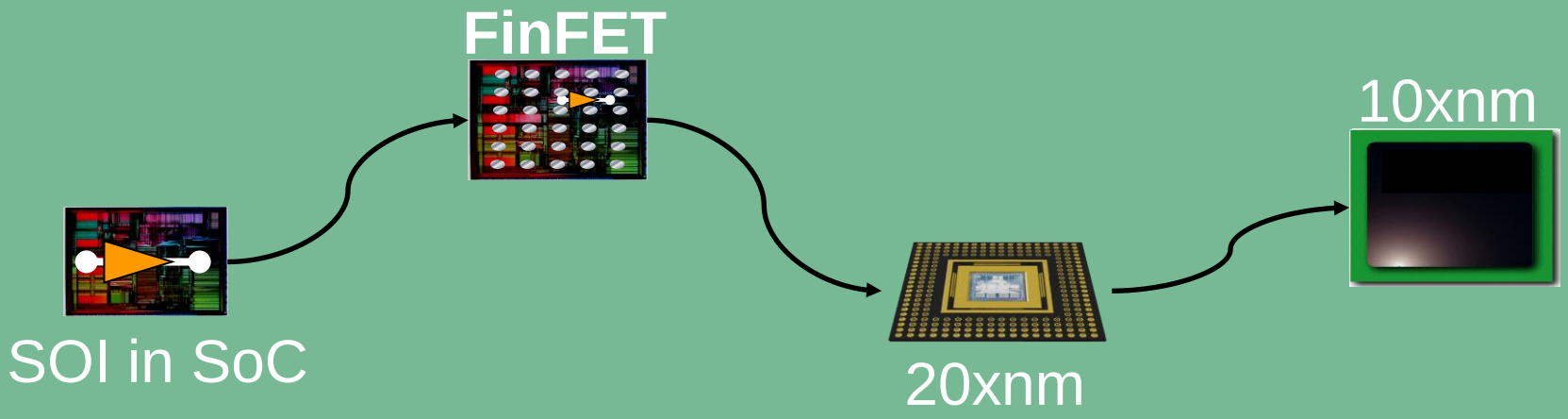
NovaThor BY ST-ERICSSON

ST-Ericsson NovaThor L8580
FD-SOI is Cooler than Bulk Technology

BSIM SOI Modeling

- BSIMSOI is a SPICE compact model for SOI (Silicon-On-Insulator) circuit design. This model is formulated on top of the BSIM3 framework. It shares the same basic equations with the bulk model so that the physical nature and smoothness of BSIM3v3 are retained. It’s already being used in production by major semiconductor companies such as IBM and AMD. BSIMSOI was selected by TechAmerica Compact Model Coalition (CMC) as the standard SOI MOSFET model in December 2001.

Advanced Technology in SoC
FinFET

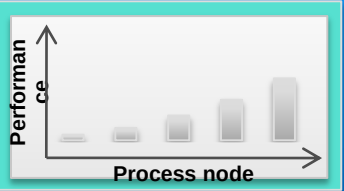


"FinFET; Tri-Gate Transistors; Multigate-FET"

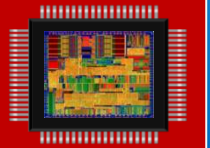
SoC Design at Advanced Process Node

	65nm	40nm	28nm	20nm	14nm
Power, Performance, Area	✓	✓	✓	✓	✓
Signal Integrity	✓	✓	✓	✓	✓
Severe Process Variation		✓	✓	✓	✓
CMP and Litho		✓	✓	✓	✓
Device Stress			✓	✓	✓
Double/Multi-Patterning				✓	✓
New Devices e.g. FinFET					✓

3-5 GHz SoCs



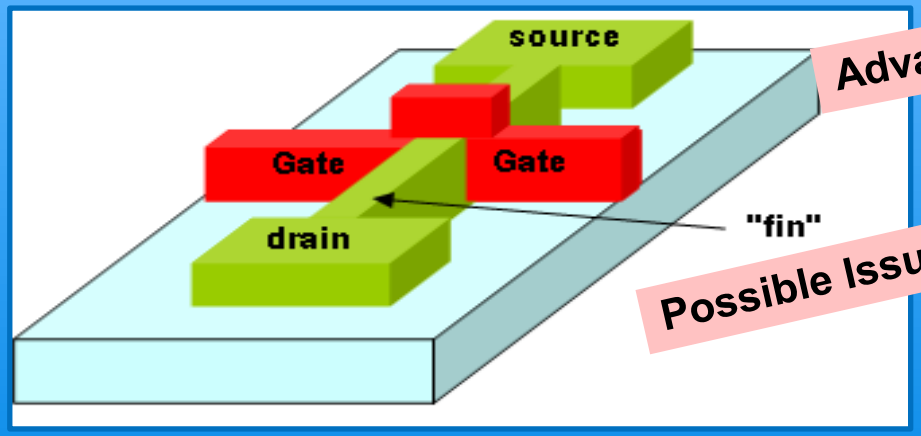
150+ Million Instance Designs



Custom-digital integration, low power design

More Moore – Miniaturization

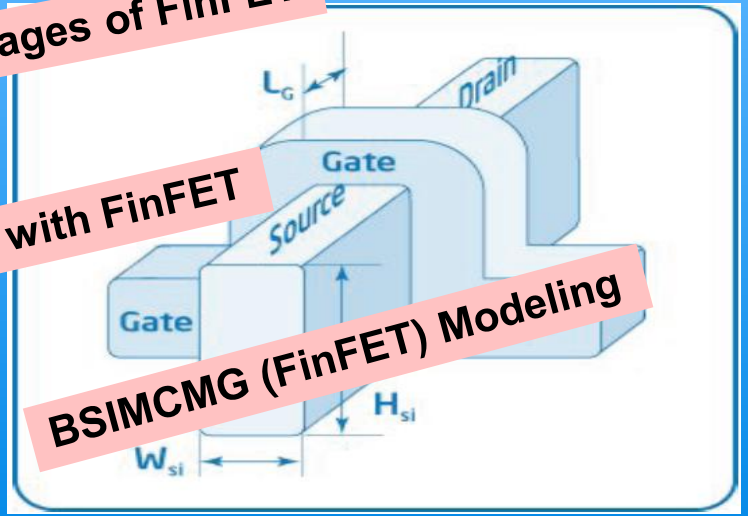
Beyond CMOS at 14nm & Below



Advantages of FinFET

Possible Issues with FinFET

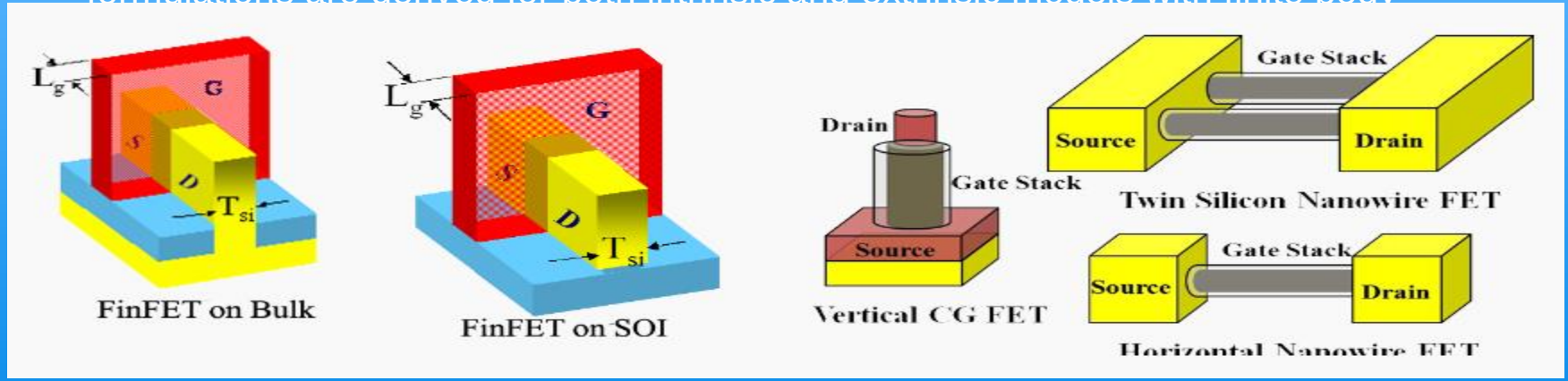
BSIMCMG (FinFET) Modeling



FinFET, by Chenming Hu (UCB), IEDM, 1999
Other names: TriGate, MuGFET, FlexFET, GAAFET

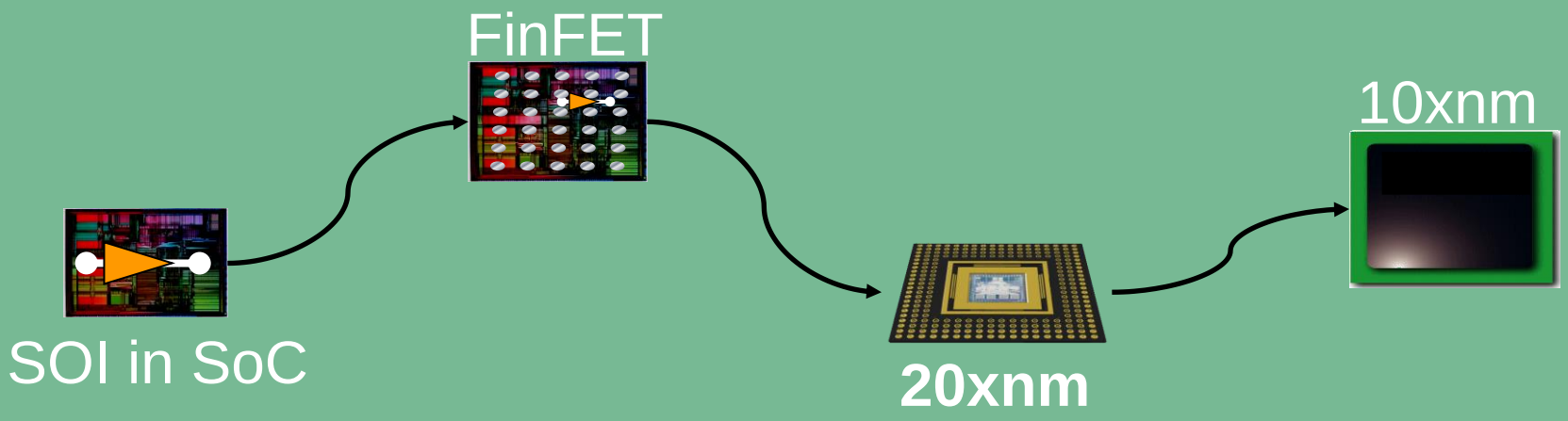
Compact Modeling

- BSIM-CMG is a compact model for the class of common multi-gate FETs. BSIM-CMG has been implemented in Verilog-A. Physical surface-potential-based formulations are derived for both intrinsic and extrinsic models with finite body



subsequent I-V formulation automatically captures the volume inversion effect. Analysis of the electro-static potential in the body of MG MOSFETs provided the model equation for the short channel effects (SCE). The extra electrostatic control from the end-gates (top/bottom gates) (triple or quadruple-gate) is also captured in the short channel model.

Advanced Technology in SoC
20xnm

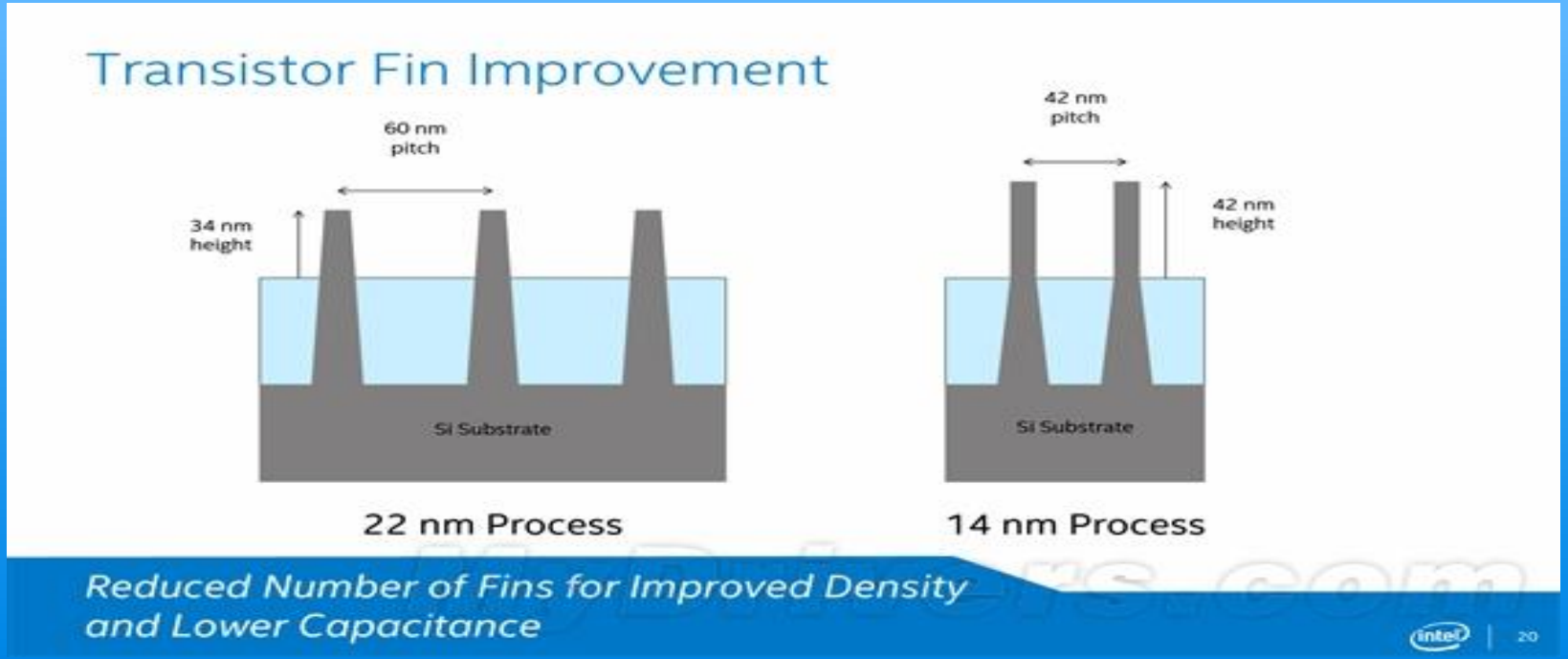


“28/22/20nm”

Memory Patents (20xnm …)

- DRAM
- SRAM
- NAND Flash
- Storage (25% Patents): 美光（Micron）、三星电子（Samsung Electronics）、东芝（Toshiba）、IBM和英特尔（Intel）
- DRAM: Conversant、高通（Qualcomm）、Rambus、Round Rock Research

FinFET at Intel



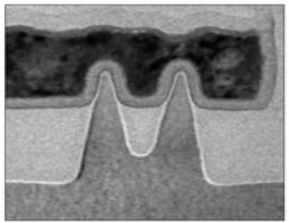
FinFET Process Technology Transition

Minimum Feature Size

	22 nm Node	14 nm Node	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80 nm	52 nm	.65x

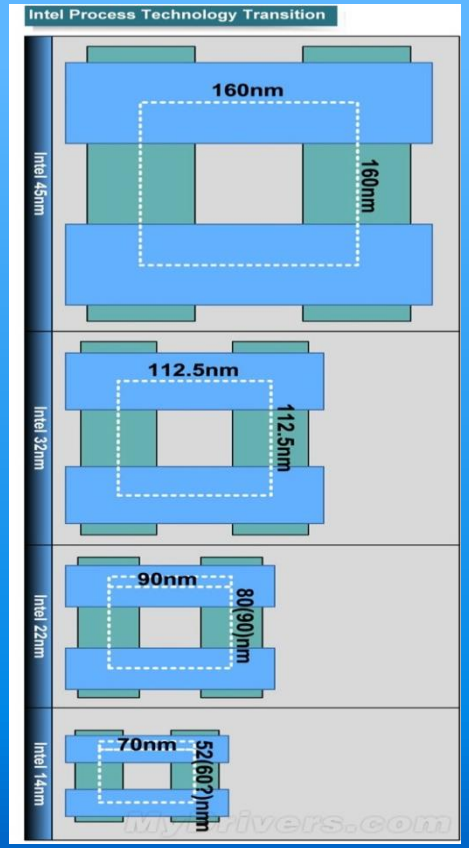
Intel Has Developed a True 14 nm Technology with Good Dimensional Scaling

Transistor Fin Improvement

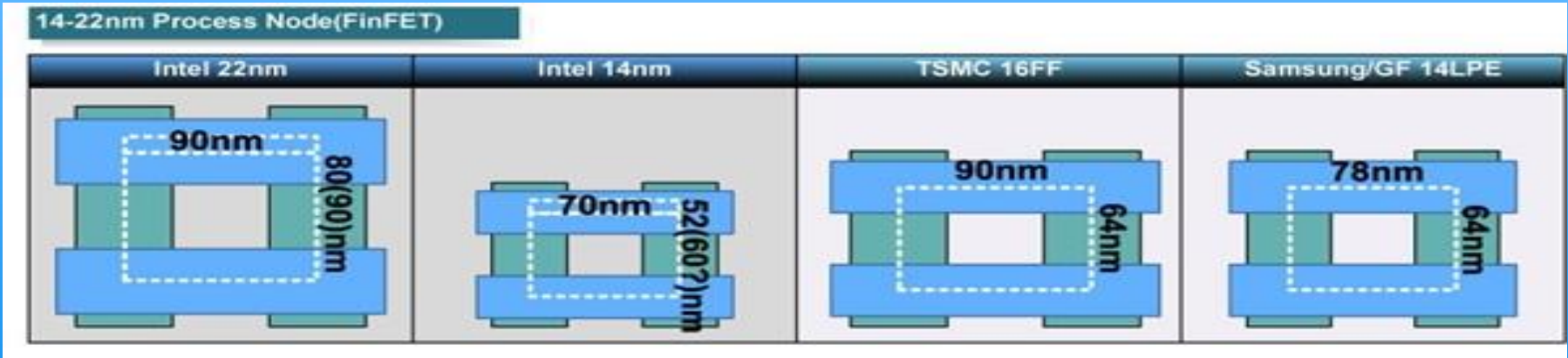


22 nm 1st Generation Tri-gate Transistor

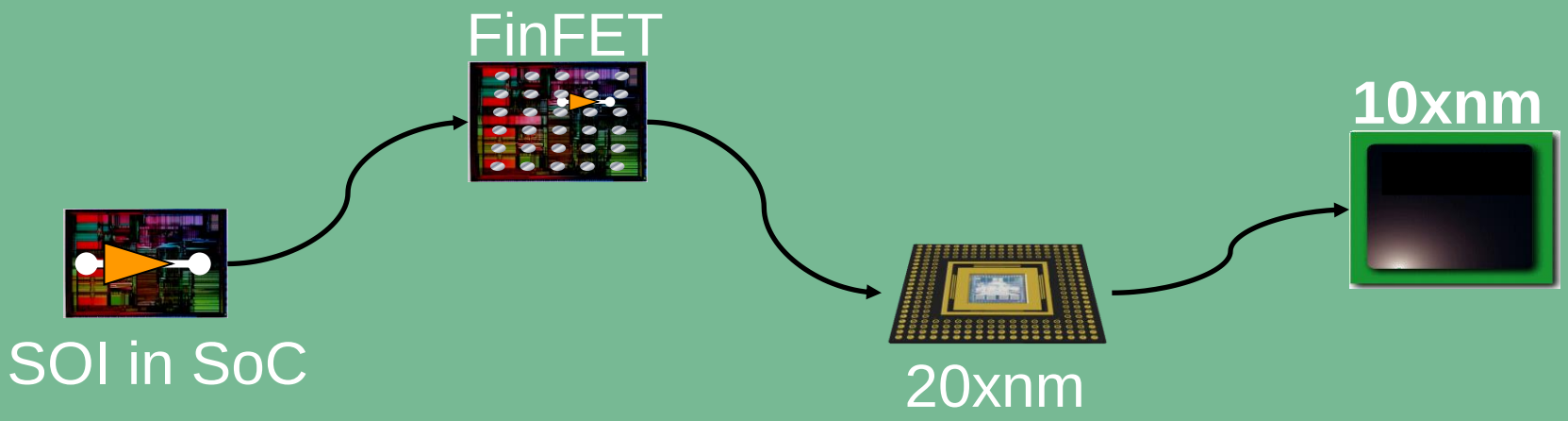
14 nm 2nd Generation Tri-gate Transistor



FinFET at Various Foundries



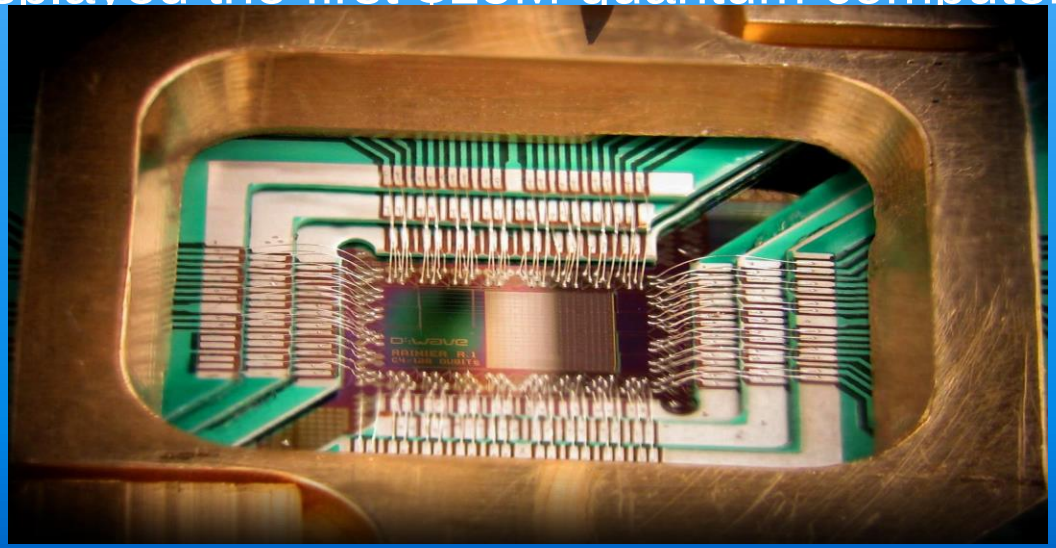
Advanced Technology in SoC
10nm



“16/14/10nm”

Quantum Computing

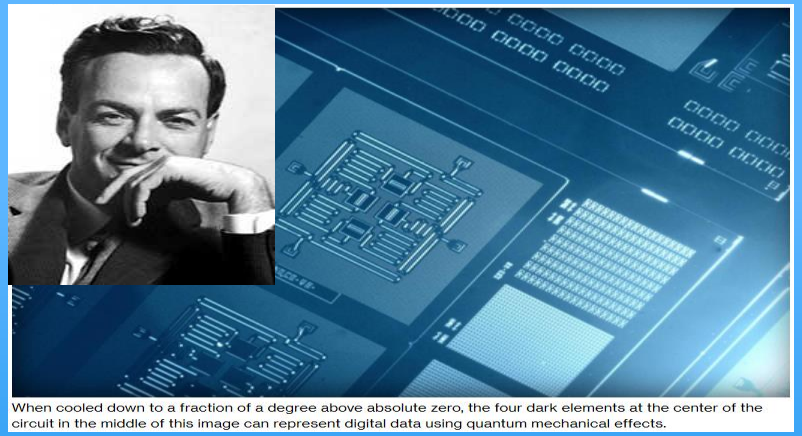
- Theoretical model: quantum Turing machine
- quantum bits (qubits)
- 2015 NASA displayed the first $15M quantum computer



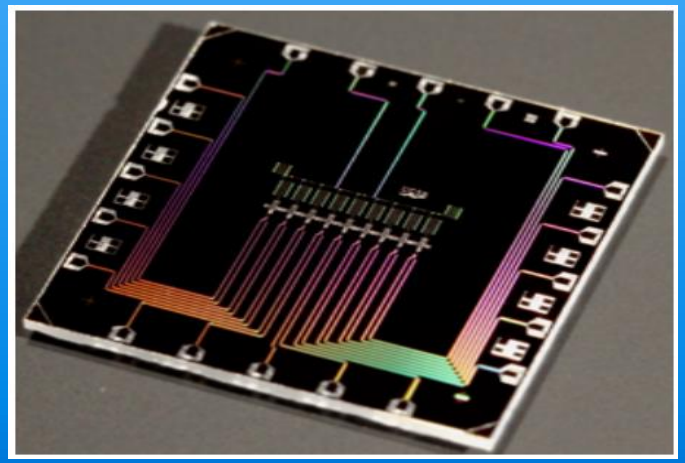
Quantum Computer

- Copenhagen
  - Digital, Analog, MS
  - PLL/DLL
- Quantum Computer
- Richard Feynman 1981

- Quantum Computer Design
  - IBM, Google, UCSB: *qubits*



When cooled down to a fraction of a degree above absolute zero, the four dark elements at the center of the circuit in the middle of this image can represent digital data using quantum mechanical effects.



Researchers from Google and the University of California, Santa Barbara, used this chip to demonstrate a crucial method needed to make quantum computers reliable.

IBM Quantum Experience (QX)

- **Quantum computing**
  - Quantum circuit, quantum (logic) gate:
    - to work a small number of *qubits*
  - Unitary Matrices: $2^n x 2^n$
- **From 5-qubit to 50-qubit**

TSMC Top10 2018

	eFlash	MRAM	RRAM
Cost	$$$	$$	$
Read perf.	1X	1X	1X
Read Power	0.77	2	1.2
uA/MHz/bit			
Write perf.	1X	3X	
Cycles	100K	>1M	10K

MRAM qualification for the Automotive platform is underway -- *"We will provide a feasibility assessment on MRAM for Automotive in 2H'18."*

More than Moore

- CNT
- Graphene
- Spintronics

Biochip