CLASS PROJECT REPORT 2018 (6/25-6/29)
高级强化课（雁栖湖校区）课程编号:
课程名称: 大数据时代的系统芯片设计 (主讲教师: 陈春章)

Score Percentiles and Due Date of Project Report or Review Paper:

1. Score Percentiles

   Class Attendance (20%); Completion of Project Report or Review Paper (80%)

2. Due Date of Project Report (option 1) or Review Paper (option 2):

   Monday, July 9, 2018 (chose Option 1 or Option 2)

Contents of Report (option 1) or Paper (option 2):

1. Option 1: Class Project Report should contain a total of 5,000-15,000 words (12-30 pages), in either English or Chinese. You may use the sample paper "CSTIC_2017_Symposium_9-16_Chen_Hu2.pdf" as a reference.
2. Option 2: Class Review Paper (concise format) should contain 3-4 pages, in either English or Chinese. You may use the sample paper "CSTIC_2017_Symposium_9-16_Chen_Hu2.pdf" as a reference.
3. Title and affiliations: report or paper title should be related to current course, i.e. "SoC Design in Big Data Era and/or AI related applications", see "Recommended class project titles" below. Don't forget to write your name(s) and affiliation(s), as well as your communication address.
4. Abstract: provide a short abstract paragraph. List of key words is optional.
5. Report or paper style and format: though not strictly required or defined, it is recommended to follow the reference template (Research_paper_template1.doc or Research_paper_template2.doc) which is provided with this document. See also the above sample papers for your writing reference.
6. If 2-3 people work in a group, the role and contribution must be claimed for each individual for the work to have contributed.

Recommended class project report or review paper titles - Select one of the following topics (or create your own topic) within the class scope:

- An Overview of {*HBM* | *HPC* | *Cambricon*} SoC Design Features used in AI-Big Data Era

  （大数据时代{*HBM* | *HPC* | *Cambricon*}系统芯片设计特点回顾，选择 1-2 点深入讨论）

- Design and Integration of *{PCIe | RapidIO | DDR4}* in *{HPC | Communication SoC}*, in relation to a potential Application of AI-Big Data scenario
- Architecture Design and Verification of a *{SmartHome IoT Chip or SoC}*
- Verification Methodology of IP in SoC Design

  (系统芯片设计中 IP 的验证方法介绍)
- 当代系统芯片设计中 IP 类型特点及其应用
- IBM 云计算中的 Power 芯片先进技术的集成
- Existing Verification Methodologies and their Applications
- Fabless SoC 设计与制造(非 IDM 设计公司模式)
- Progress in Studies of Formal Equivalence Checking
- Progress in Studies of Placement Algorithms (SAT)
- 布线算法研究的进展讨论
- Low Power Design and Low Power Verification in *{SoC|Comunication Chip}*
- *[Synchronous| Asynchronous]* Clock Tree Synthesis and Design Performance
- Comparison of 28nm Design between Bulk CMOS and FD-SOI Technologies
- A Study of *{ESD Models}* and Design-For-Reliability
- *{Ionizing Radiation}* Induced Reliability Issues in FPGA Designs