University of Chinese Academy of Sciences

Verification & Implementation of SoC Design

Physical Implementation of SoC Design

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Physical Design of SoC

- **Design Preparation**
- **Placement and Its Algorithm**
- **CTS and Performance**
- **Routing and Its Algorithm**
- **Signoff**

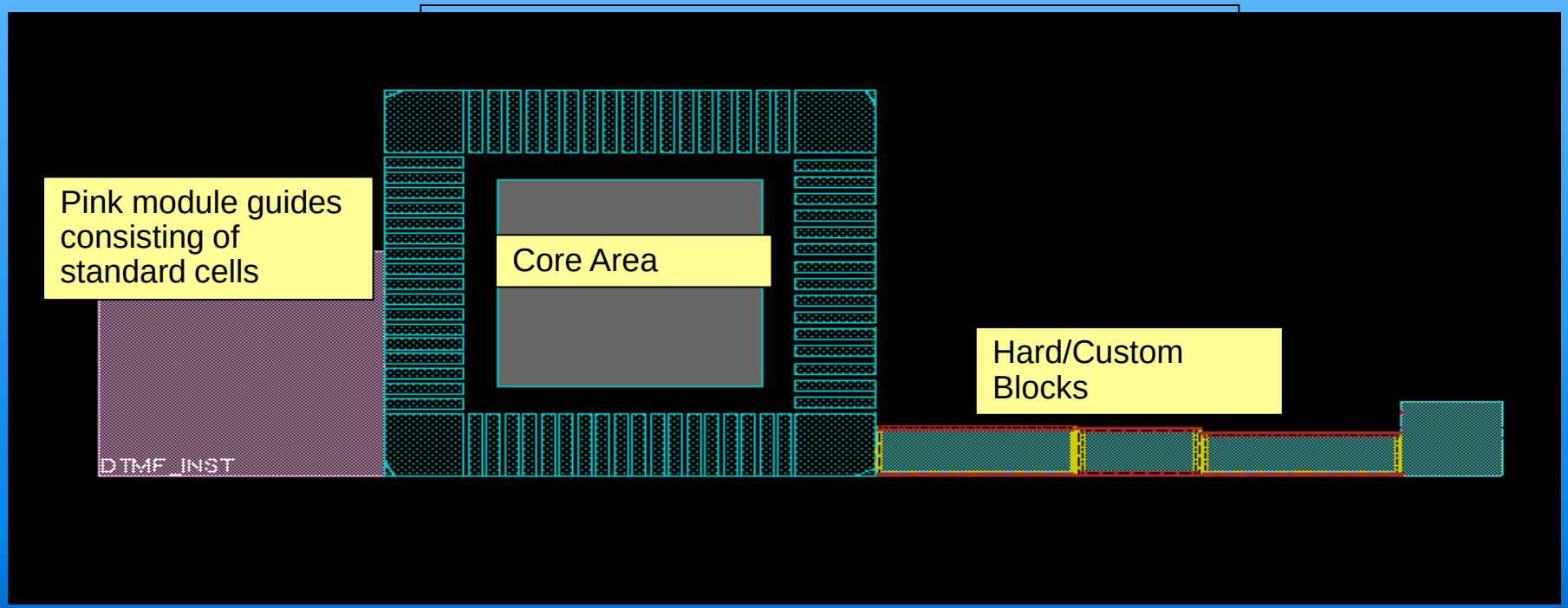
PLACEMENT OF IC DESIGN

- Physical Design Flows
- Library Data Preparation
- Design Data Preparation
- Floor Plan & Power Plan
- **Placement**
- Hierarchical Partition
- Clock Tree Synthesis
- Routing
- RC Extraction & DC
- Static Timing Analysis
- In Placement Optim
- Power Analysis
- Signal Integrity Analysis
- Engineering Change Order
- Chip Assembly

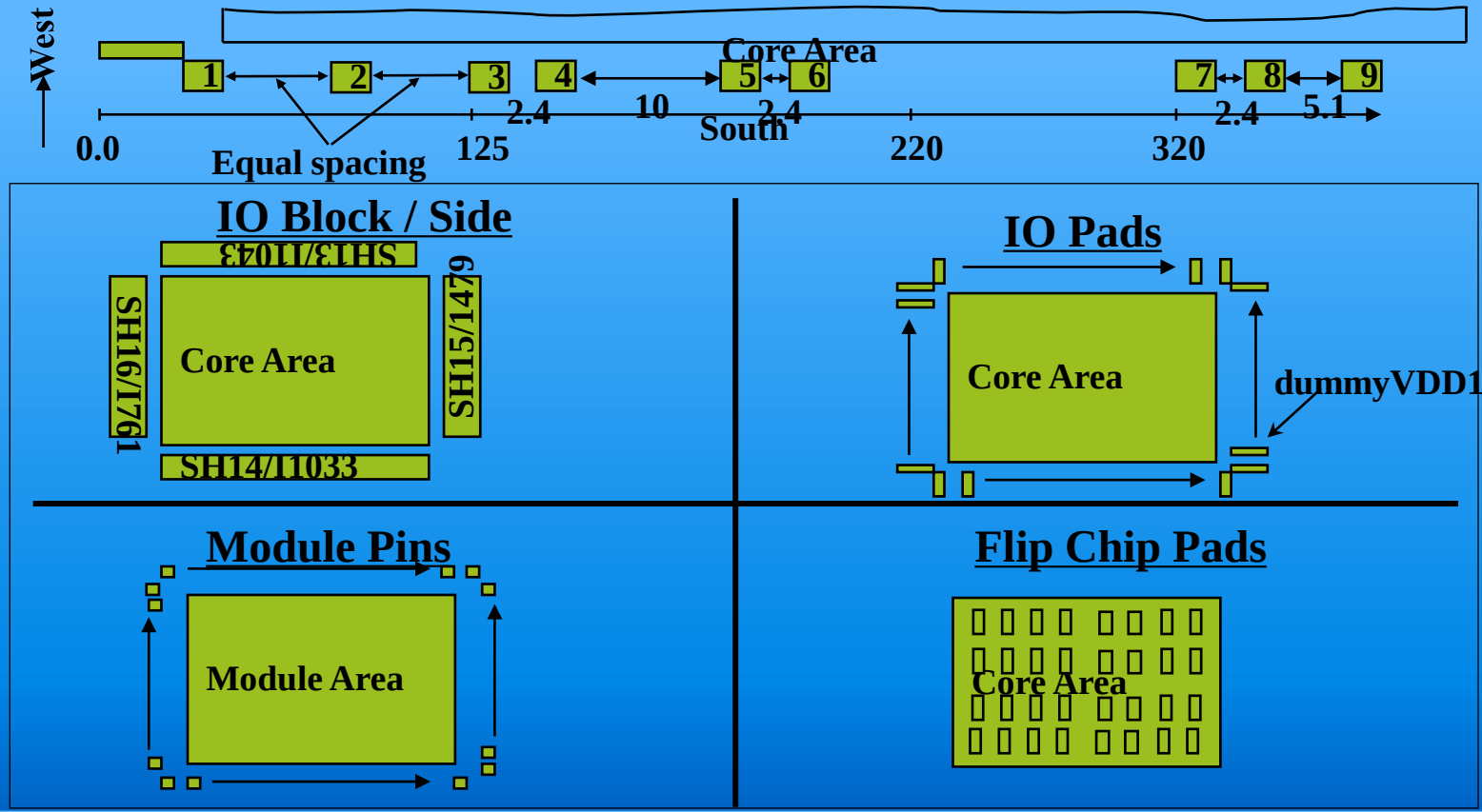
- Placement Essential
  - Goals and Objectives
  - Algorithms
  - Basic Features and Options
- Timing-Driven Placement and Constraints
  - I/O and Block Placement
  - Standard Cell Placement
  - Area Placement
  - Incremental Placement
  - ECO Placement
  - SDF, GCF and SDC
- JTAG and Scan Chain Placement
  - Boundary Scan and JTAG Pre-placement
  - Scan Chain Detachment
  - Scan Chain Reattachment

Floorplan and Placement

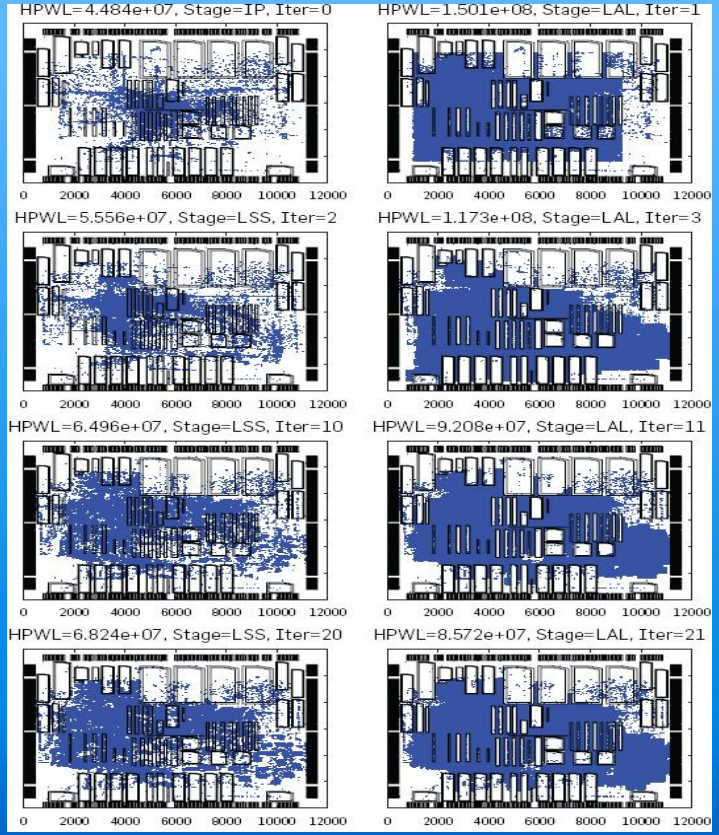
Example



I/O Types


West
1
2
3
4
5
6
7
8
9
Core Area
0.0
Equal spacing
125
2.4
10
2.4
South
220
320
2.4
5.1
IO Block / Side
SH13/I1043
SH16/I761
Core Area
SH15/1479
SH14/I1033
IO Pads
Core Area
dummyVDD1
Module Pins
Module Area
Flip Chip Pads
Core Area

Description of Placement Algorithm



- The problem
  - The problem in simple statement: connect a collection of sites by a "good" network.
- The example
  - To connect components of a VLSI circuit by networks of wires, in a way that
  - uses little surface area on the chip,
  - draws little power, and
  - propagates signals quickly.

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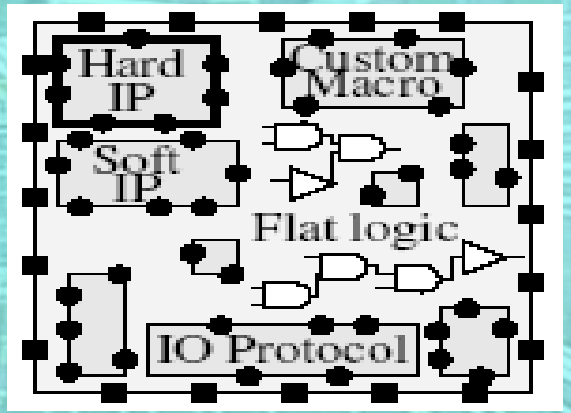
Algorithm of Placement

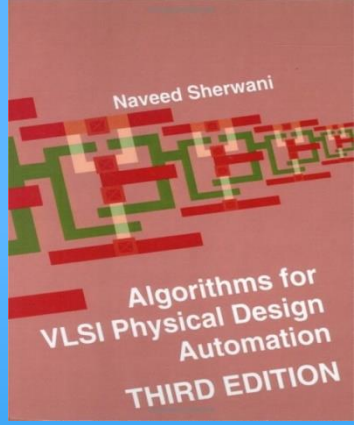
PLACEMENT OF IC DESIGN

Constructive Placement
Iterative Placement
Annealing Placement
Partitioning Placement



Studies of Placement

- Placement of Algorithm, Naveed Ahmed Sherwani,
  - **Algorithms for VLSI Physical Design Automation**,
  - pp219-244. (3rd ed., 1998. ISBN-10: 0792383931)



Let us formally state the placement problem. Let $B_1, B_2, \ldots, B_n$ be the blocks to be placed on the chip. Each $B_i, 1 \leq i \leq n$, has associated with it a height h_i and a width w_i. Let $\mathcal{N} = \{N_1, N_2, N_3, \ldots, N_m\}$ be the set of nets representing the interconnection between different blocks. Let $\mathcal{Q} = \{Q_1, Q_2, \ldots, Q_k\}$ represent rectangular empty areas allocated for routing between blocks. Let L_i denote the estimated length of net N_i, $1 \leq i \leq m$. The placement problem is to find iso-oriented rectangles for each of these blocks on the plane denoted by $\mathcal{R} = \{R_1, R_2, \ldots, R_n\}$ such that

1. Each block can be placed in its corresponding rectangle, that is, R_i has width w_i and height h_i,
2. No two rectangles overlap, that is, $R_i \cap R_j = \phi$, $1 \leq i, j \leq n$,
3. Placement is routable, that is, $Q_j, 1 \leq j \leq k$, is sufficient to route all the nets.
4. The total area of the rectangle bounding $\mathcal{R}$ and $\mathcal{Q}$ is minimized.
5. The total wirelength is minimized, that is, $\sum_{i=1}^{m} L_i$ is minimized. In the case of high performance circuits, the length of longest net $\max\{L_i \mid i = 1, \ldots, m\}$ is minimized.

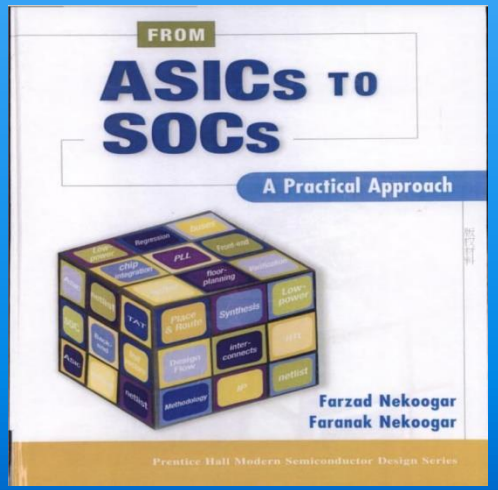
Classification of Placement Algorithms

- Simulation Based Placement Algorithm
  - Annealing;
  - Evolution;
  - Force-Directed;
  - Sequence-Pair Technique
- Partitioning Based Placement Algorithm
  - Breuer's Algorithm
  - Terminal Propagation Algorithm
- Other Placement Algorithm
  - Cluster Growth;
  - Quadratic Assignment
  - Resistive Network Optimization
  - Branch-and-Bound Technique

Amoeba Placement for Gigantic Design

- Algorithm
  - United States Patent 6249902
  - Design hierarchy-based or partitioning based placement
  - Cluster placement

- From ASICs To SoCs
  - By Nekoogar & Nekoogar, 2003.
  - Ch. 4, p99-100
  - Modern Physical Design Techniques
  - ISBN 0-13-033857-5



Studies of Place and Route

- UCB
- UCSD VLSI CAD Lab, Andrew Kahng
  - Physical, Placement, modeling, DFM, ITRS, Adaptive, 3D IC
- UCLA CMOS Lab, Jason Woo
  - S-D Electrostatic Coupling; Channel Transportation; Para. RC, Quantum Effects; Planar Double-Gate, Graphene Based Devices, SOI
- Univ. of Michigan, Dennis Sylvester
- Univ. of Minnesota, VLSI Res. Lab

Studies of Place and Route

- Tsinghua University, Dept. Computer & Tech.
  - Xianlong Hong, Yici Cai
    - Wire-length Driven Legalization Algorithm for Large-scale ASIC
- Fudan University,
  - Pushan Tang, Xuan Zeng
    - A novel simulated annealing based FPGA placement algorithm

Physical Design of SoC

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CLOCK TREE SYNTHESIS

- Physical Design Flows
- Library Data Preparation
- Design Data Preparation
- Floor Plan & Power Plan
- Placement
- Hierarchical Partition
- **Clock Tree Synthesis** ←
- Routing
- RC Extraction & DC
- Static Timing Analysis
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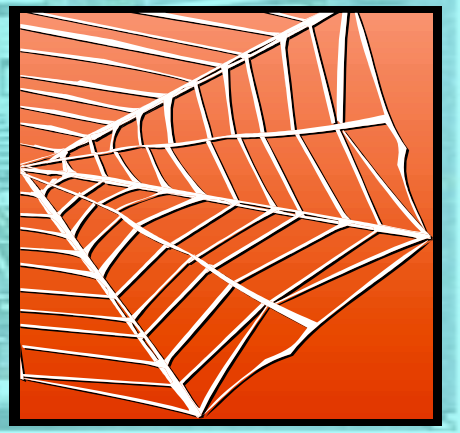
- Engineering Change Order
- Chip Assembly

- Clock Generation and CTS
- CTS Implementation
  - Concepts and Terminology
  - Goals and Objectives
  - Features
  - Implementation
- Types of Clock Tree
- Scan Reordering



Concepts of CTS

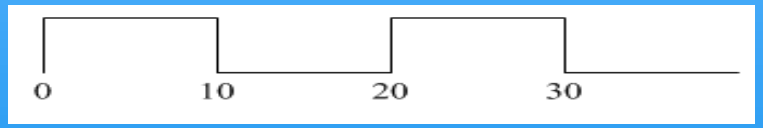
- Constraints and Terminology
  - design constraints, CTS constraints
  - clock, period, waveform, duty cycle, rise, fall, edge-triggered
  - skew, useful skew, delay, latency, jitter, transition
  - exceptions: false path, multi cycle
  - synchronization, synchronized clock and asynchronized
  - R-2-R and latch-based

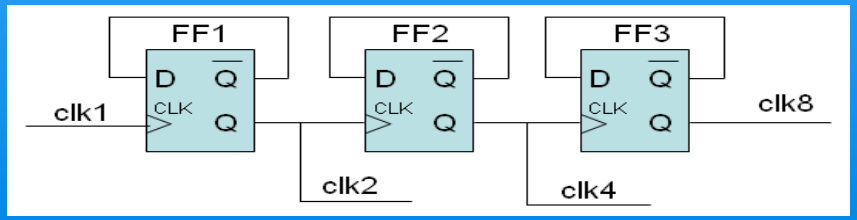
Clock Generation and CTS

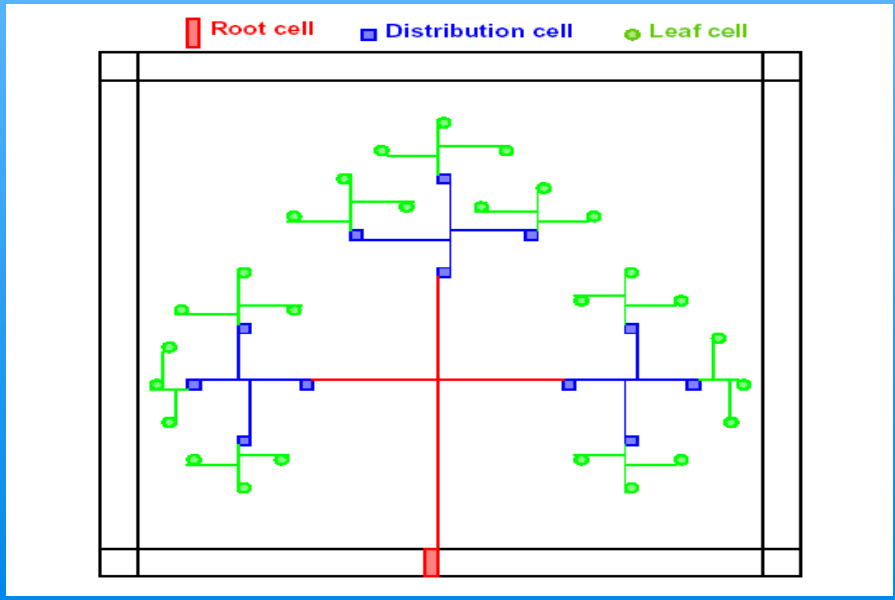
- Clock and Clock Generation
  - Defined in timing constraint file
- Clock distribution system
  - Insertion delay: the difference in time between an active clock edge at the input pin of the clock and the same edge arriving at a load
  - Skew: the difference in time between an active edge clock edge arriving at a load and the same edge arriving at a different load
- Goal is to minimize both insertion delay and skew
  - Use clock buffer (designed for clock tree)
  - Widen routing wire
  - Balance clock tree

Clock Generation and Clock Tree

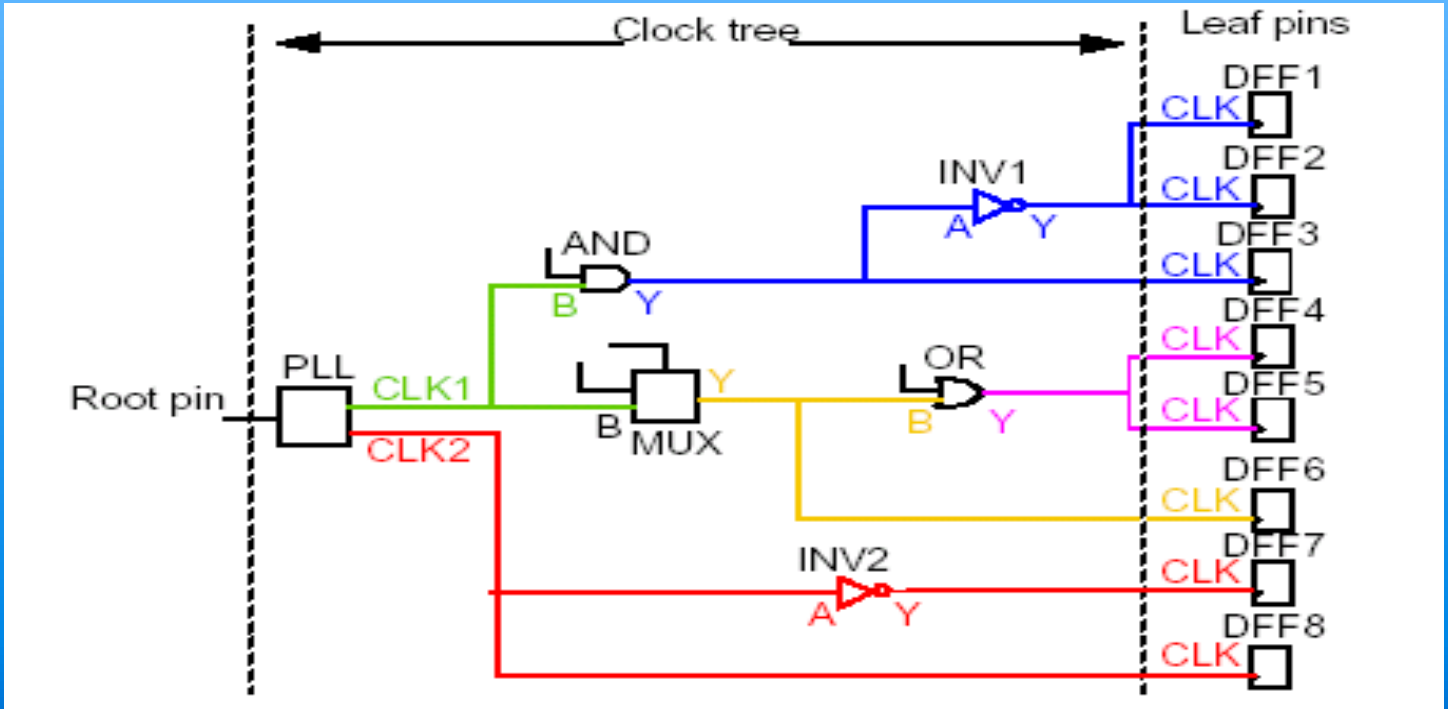
```
create_clock -period 20 CLK
```





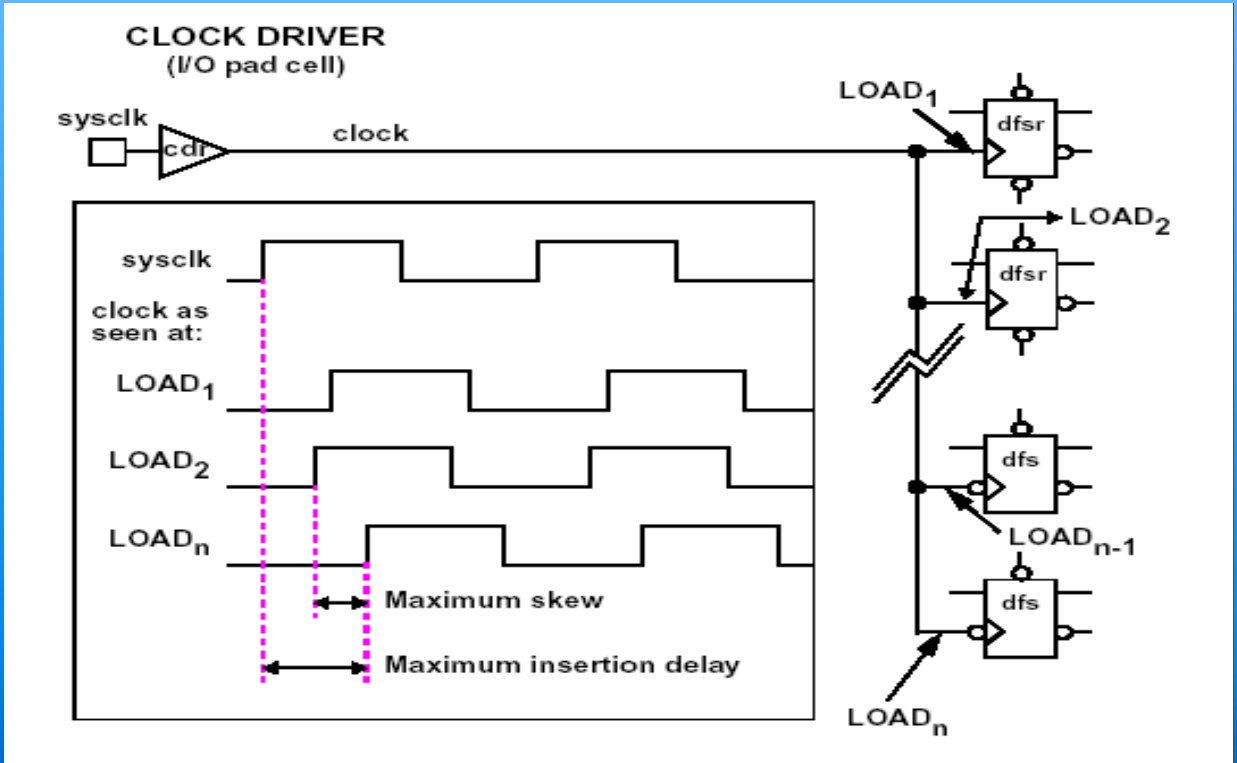


Clock Trees are Sequential Circuits



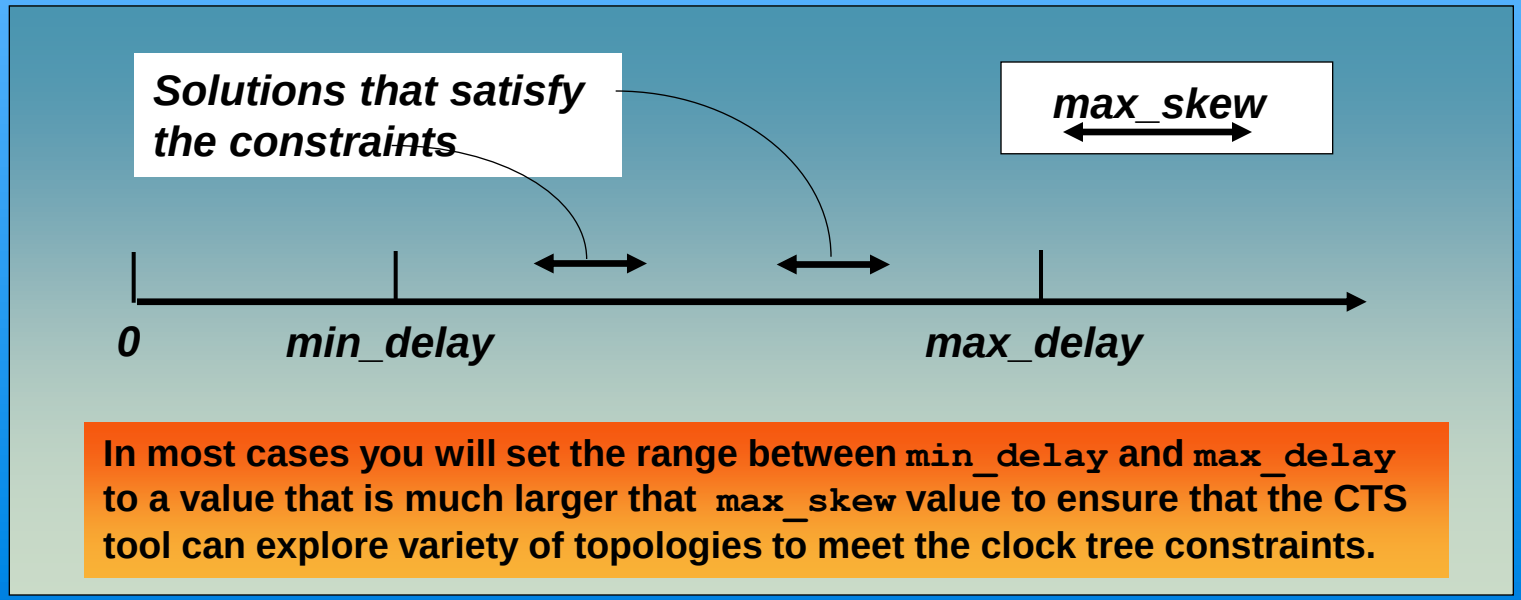
Clock Tree Synthesis

Clock Trees are Sequential Circuits



CTS Goals

Clock Skew is the Main Concern in CTS



In most cases you will set the range between `min_delay` and `max_delay` to a value that is much larger that `max_skew` value to ensure that the CTS tool can explore variety of topologies to meet the clock tree constraints.

Sequential and Synchronous

- Sequential Circuits
  - All sequential circuits have one property in common:
  - a well-defined ordering of the switching events must be imposed if the circuit is to operate correctly
- Synchronous System
  - Most of the current sequential circuits belong to the class of the synchronous systems – which means that the latching of data into the memory elements is orchestrated by a number of globally distributed clock signals

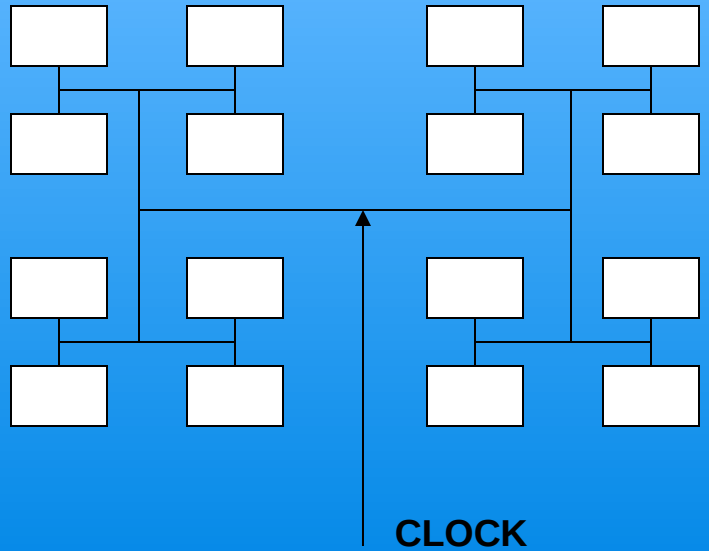
Asynchronous Clocks

- As “self-timing” is to becoming a mainstream design at high speed, distributing such clock is exceedingly difficult
- Advanced “asynchronous design innovation” techniques and implementation methodologies are needed
- Such candidates could be fully “asynchronous designs” or “islands of synchronous units” connected by an asynchronous network

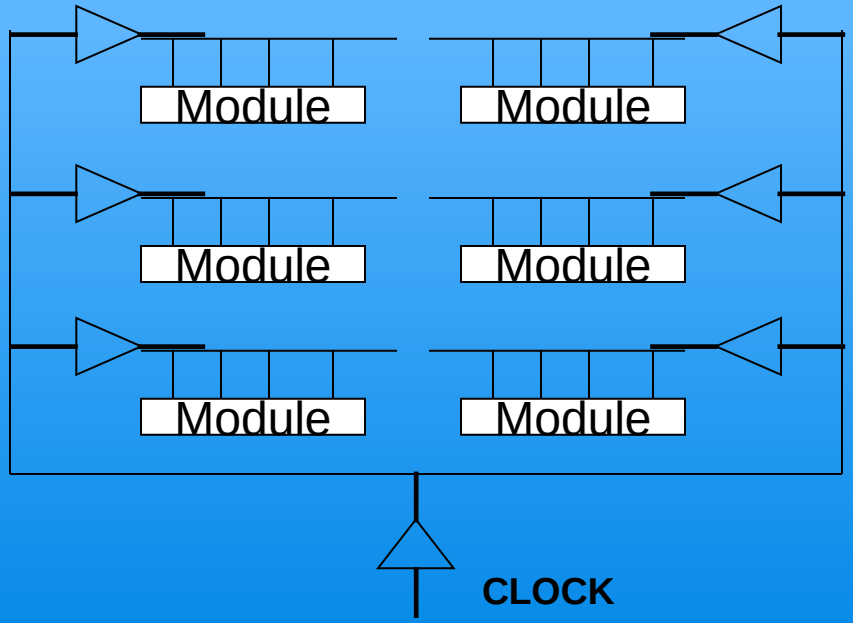
Types of Clock Tree Synthesis

- H-tree clock-distribution network
  - Clock signal delay is equal
  - + 0 skew; - small tree only
- Balanced Tree
  - Ex: 2-level clock-distributed buffering
  - + small skews; - harder to interface the absolute clock delays in different chips and boards
- Clock Tree Mesh (comb, fish-bones or spine)
  - + achieving good skew for large trees; - manual and experience dependent, increased power consumption
- Clock Tree Synthesis / Generation
  - + automatic generation; - requires understanding and experienced manipulations

H-Tree Clock Buffering



Example of a H-tree clock-distribution

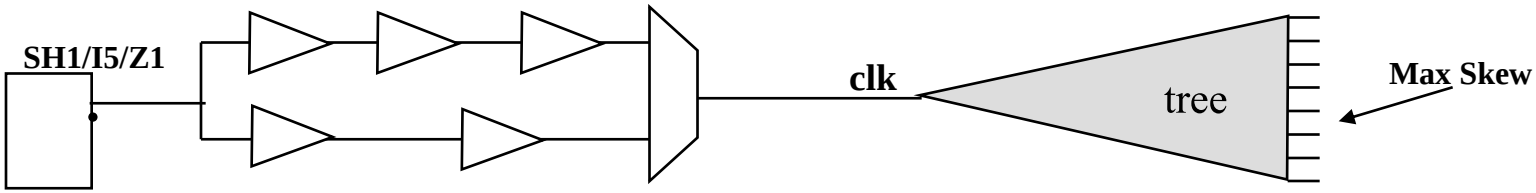


A clock-distribution network using
Two-level distributed buffering

Auto CTS Features:

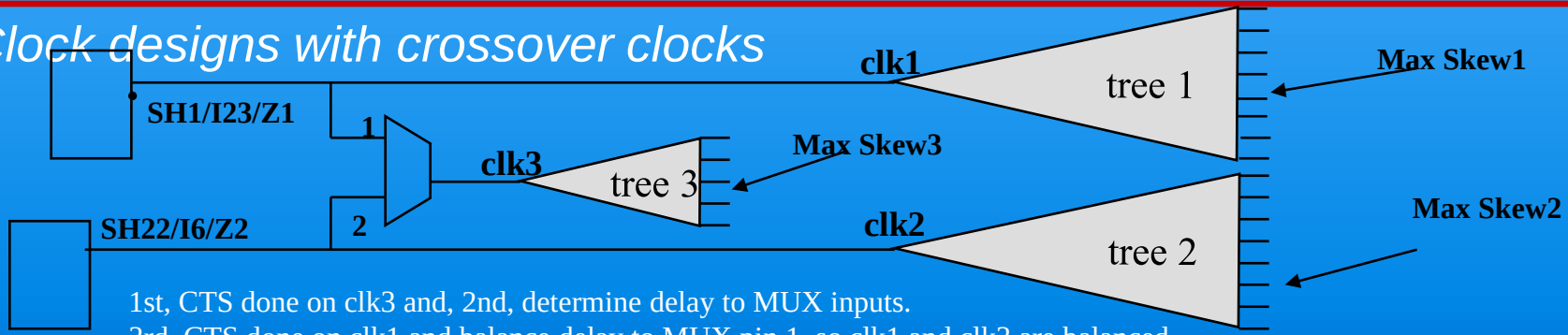
Re-convergent and Crossover Clocks

Clock designs with self-reconvergent



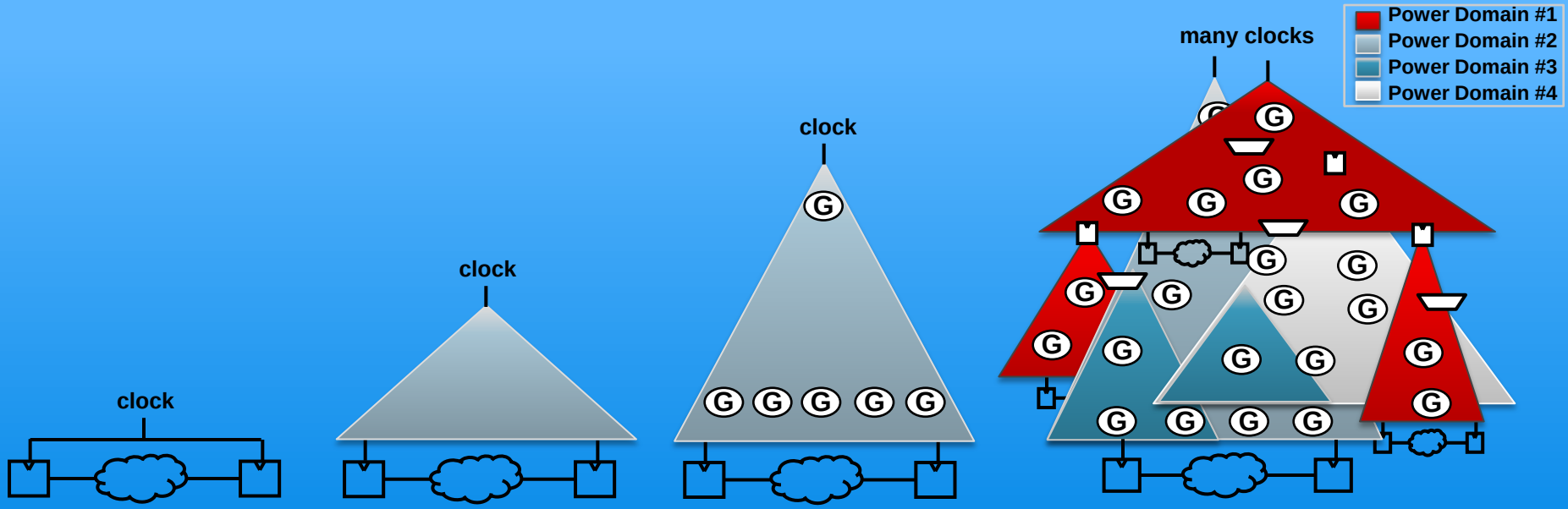
1st, CTS is done on clk and, 2nd, determine delay to MUX inputs.
3rd, balance clock paths to MUX inputs.

➢*Clock designs with crossover clocks*



1st, CTS done on clk3 and, 2nd, determine delay to MUX inputs.
3rd, CTS done on clk1 and balance delay to MUX pin 1, so clk1 and clk3 are balanced.
4th, CTS done on clk2 and balance delay to MUX pin 2, so clk2 and clk3 are balanced.
5th, optionally, use clock grouping to balance all three clocks.

Clocking Crisis in High Performance Design



30 years ago
Clocks just a wire
CTS didn't even exist

20 years ago
Clocks need amplification
CTS is born

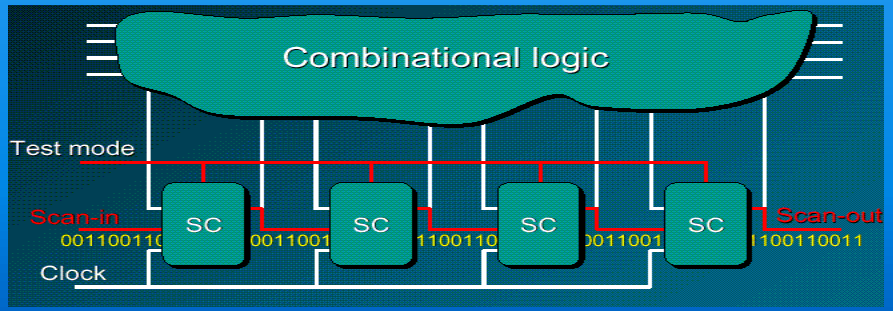
10 years ago
Clock power and latency
start to get out of hand

Modern nanometer SoC design
Clocks look more like
logic than clocks!

Scan Chain Implementation

Detaching and Reordering

- Creation of scan chain
  - are used to increase the testability of ASICs
  - introduce new nets, and sometimes cells to the design
  - Created during logic synthesis, in DEF format
- Input
  - To load / delete / re-order:
  - scan info in DEF, TDF, or FE Tcl format
- Reordering Requirements
  - Placed and CTS completed db
- Output
  - To save / display:
  - scan info in DEF or TDF format



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ROUTING OF IC DESIGN

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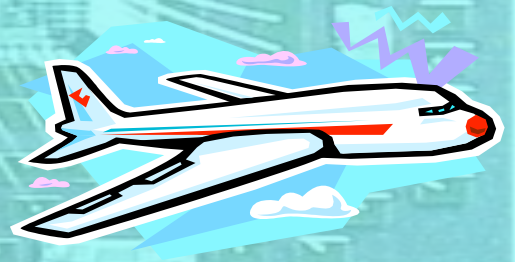
- Global Routing
- Detailed Routing
- Special Routing
- Trial Routing and Virtual Routing
- Nano Routing
- X (Diagonal) Routing



Concepts of Routing

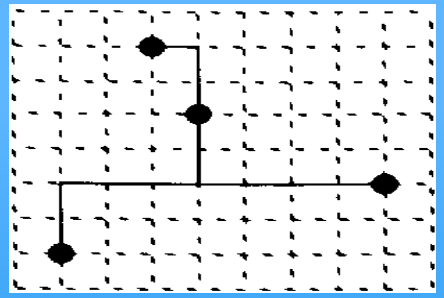
ASIC Routing and Manhattan Routing

- *Route, Router, Routing and Routability*
  - *Routing track, resource, congestion, density, cost function*
  - *Global (loose), detailed (local, final), special routing*
- *ASIC Routing*
  - *Channel routing (GA or FPGA)*
  - *Channel-less routing*
- *Manhattan Routing*
  - *One-way streets*
  - *Orthogonal*
  - *Euclidean (diagonal)*

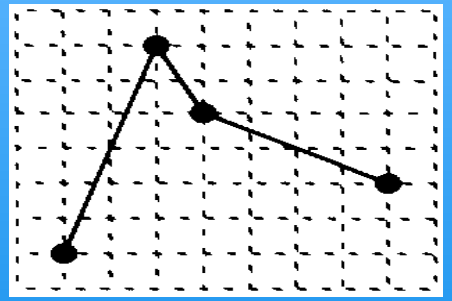
Routing Tasks

- Global routing
  - Guide the detailed router in large design
  - May perform quick initial detail routing
  - Commonly used in cell-based design, chip assembly, and datapath
  - Also used in floorplanning and placement
- Detail routing
  - Connect all pins in each net
  - Must understand most or all design rules
  - May use a compactor to optimize result
  - Necessary in all applications

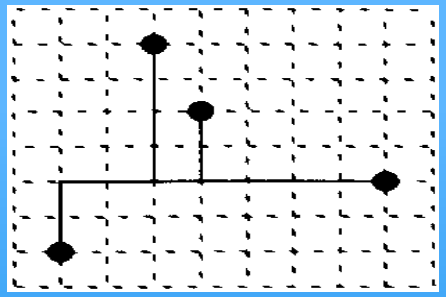
Multi-terminal Nets: Different Routing Options



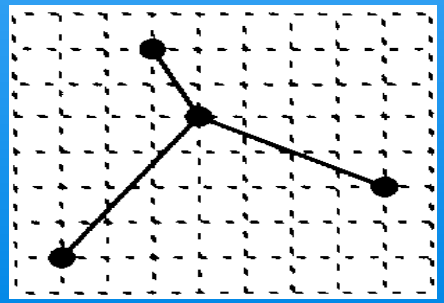
(a) Steiner Tree (14)



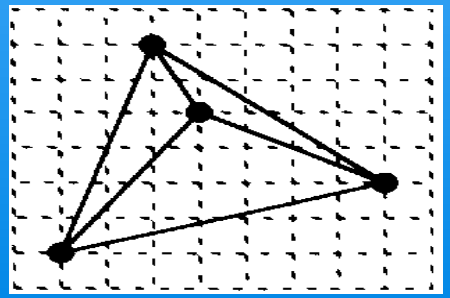
(d) Chain (17)



(b) Steiner Tree with Trunk (15)



(c) Minimum Spanning Tree (16)



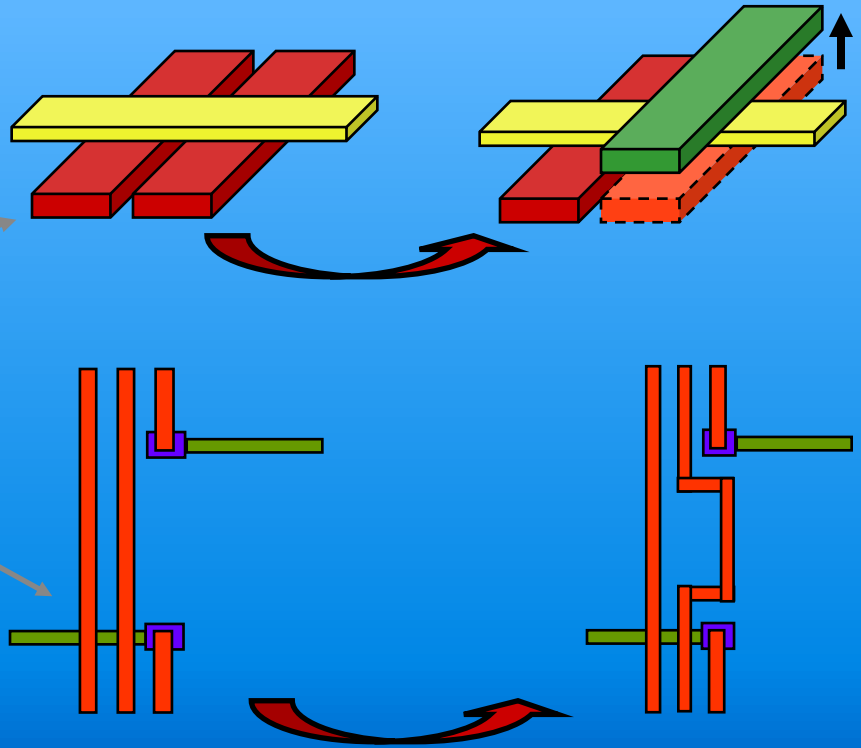
(e) Complete Graph (42)

Cost is determined by routing model

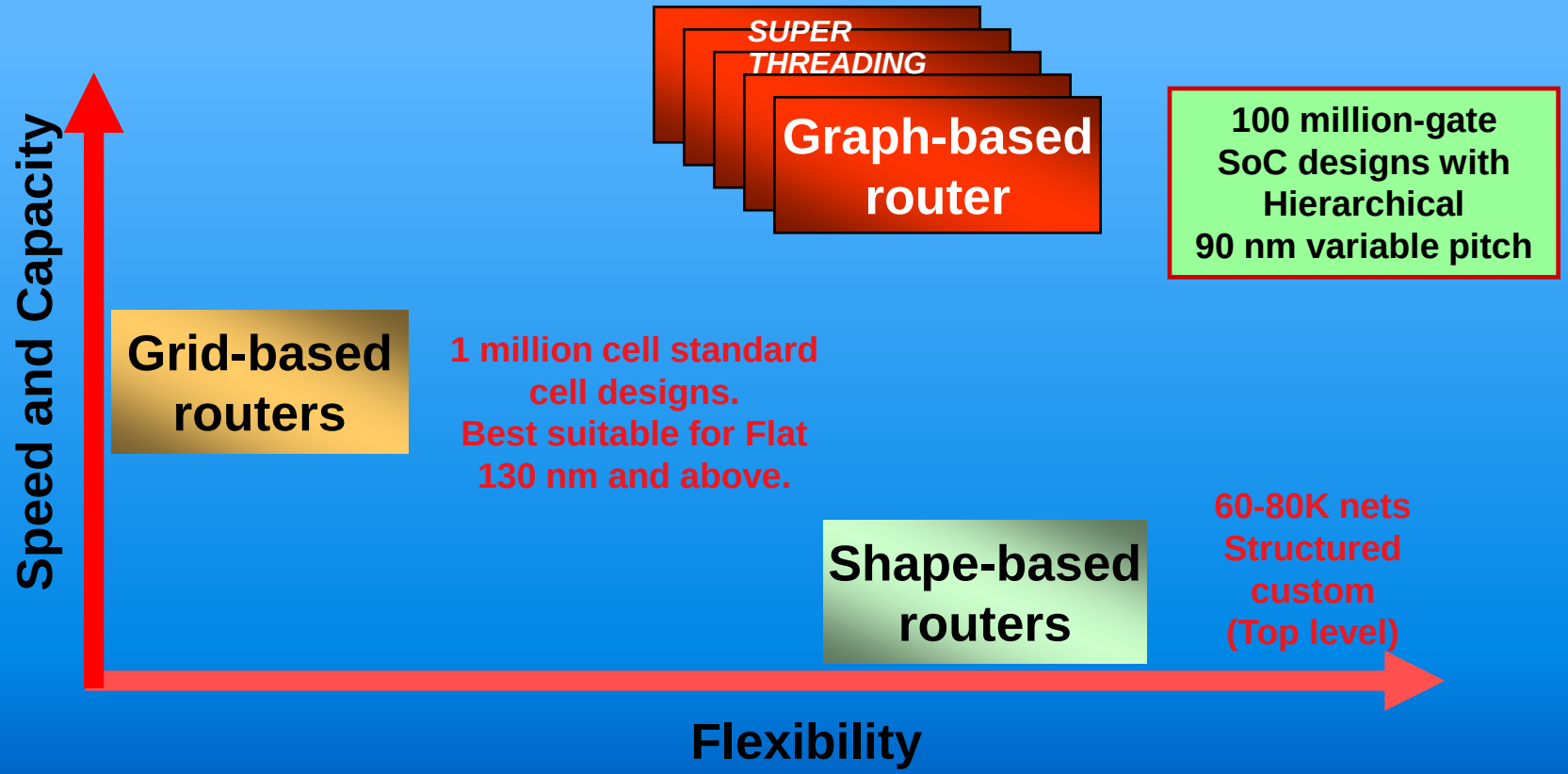
Crosstalk Avoidance during Routing

wide wire, double spacing and shielded routing

- Balances
- SI/Timing/Routability
  - Wire spacing
  - Net ordering
  - Wire topology control
  - Layer selection to reduce coupling
  - Layer selection to reduce resistance
  - Minimizing parallel long wires
  - Shielding
  - Buffer insertion



Routing Technologies



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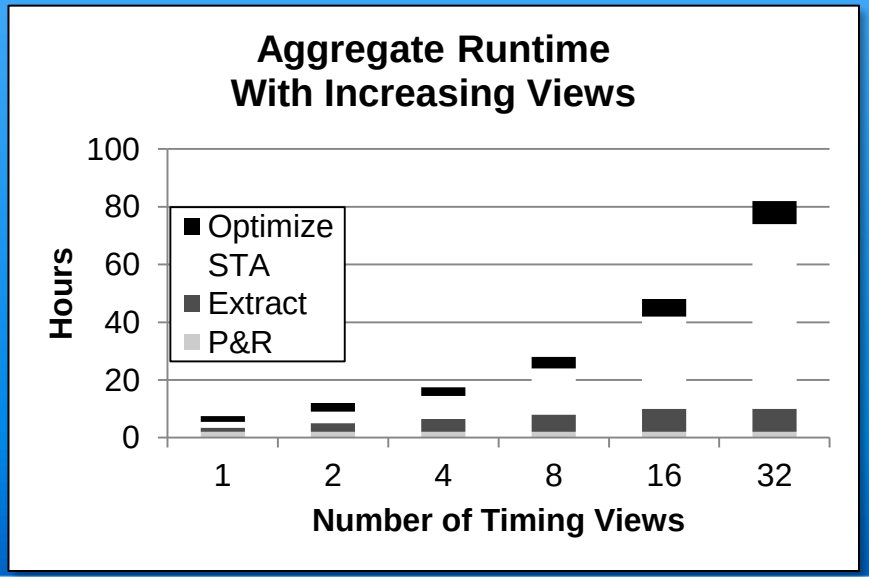
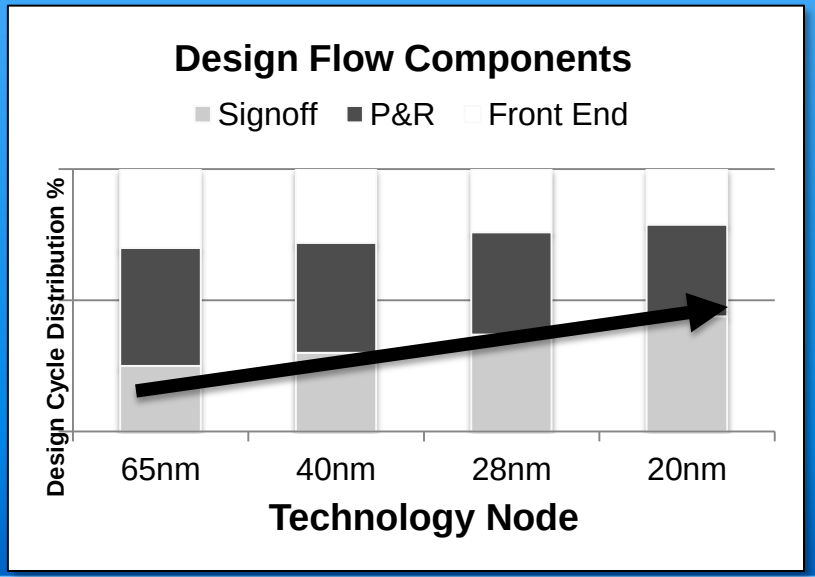
Timing Signoff and Closure Trends

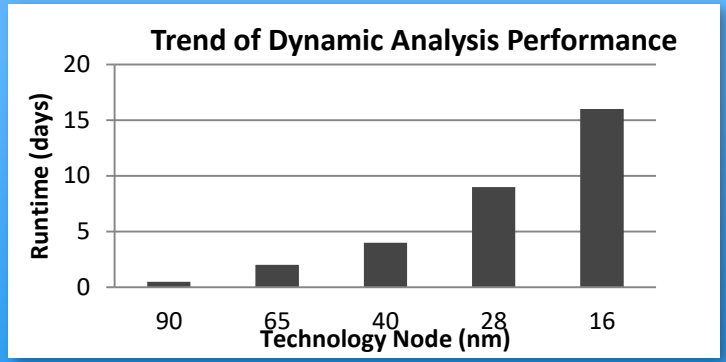
- Time to closure increasing due to:
  - Design size and complexity
  - Signoff modes and corners
  - Margins required for variation

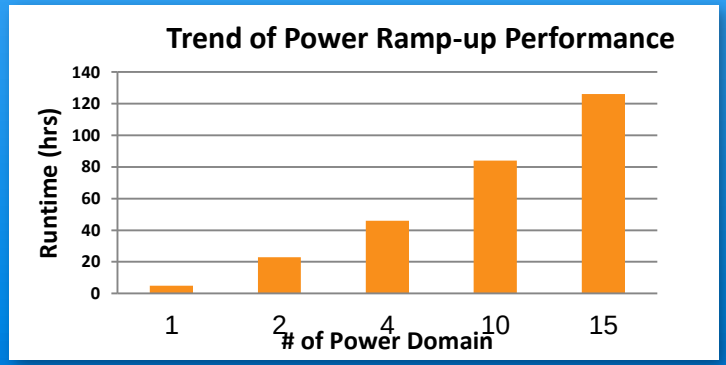




Power Solutions Have not Kept Pace with Designer's Requirements

- Time Required for Power Analysis is Increasing due to
  - Growing design complexity and size
  - More complex analysis requirements
- Current Solutions don't Consider the Impact of Power on Timing Closure
- New Challenges in 3DIC Technology
  - Thermal breakdown
  - Complete power integrity analysis from chip to package to system



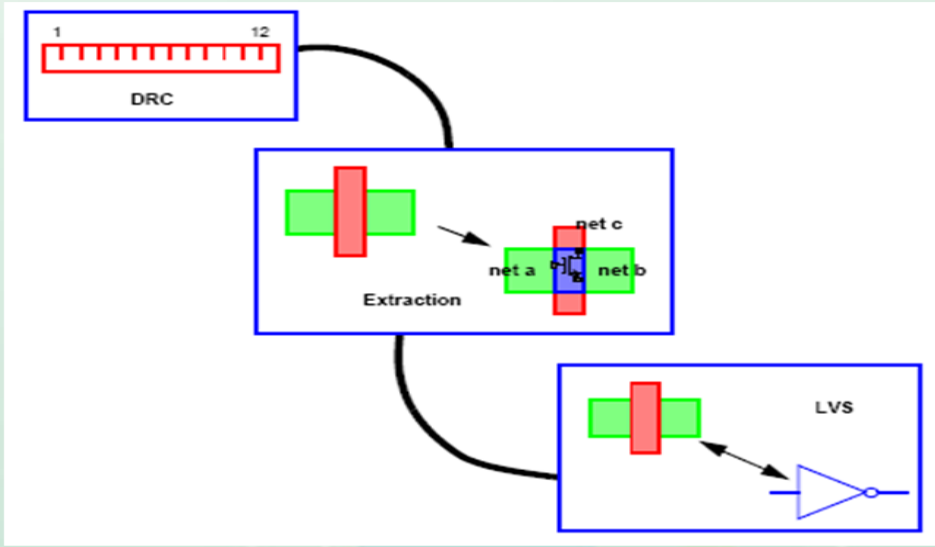


Designers Require New Technologies for Power Signoff

20nm Implementation and Signoff Physical Verification

Physical Implementation | Physical/DFM Signoff | Tapeout

- **Basic Concepts**
  - Design rule checks (DRC)
  - Layout versus schematic (LVS)
- Verification Methods
  - DRC, LVS, ERC,
  - SVL, LVL, LPE
- Tools
  - Dracula, Diva, Assura,
  - Calibre, Hercules, PVS



used in Virtuoso custom design

SUMMARY

- Placement algorithm
  - Standard cell based design
  - Block based design
- Clock Tree synthesis – propaged
  - Clock Tree topology
  - Min. skew or zero skew
- Global/Detailed routing
  - Routing algorithm
  - SI-aware
- Signoff for Timing, Power and DFM