University of Chinese Academy of Sciences

# Verification & Implementation of SoC Design

## *SPICE and Library for SoC Design*

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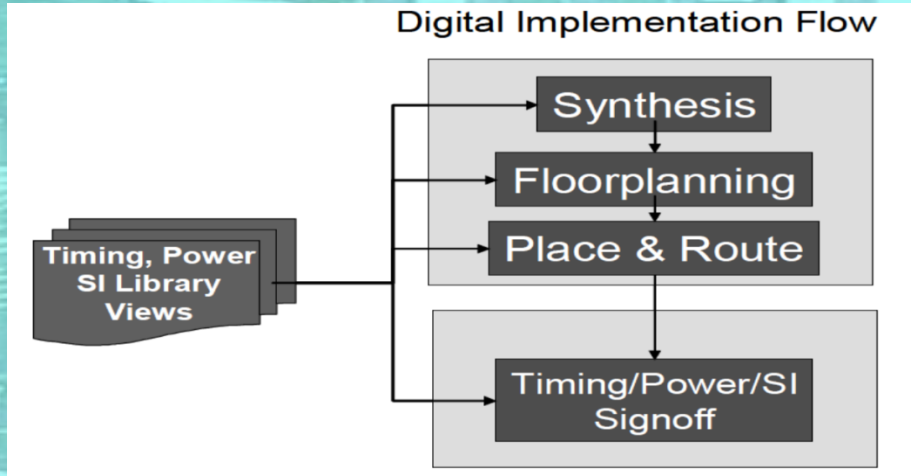
# *Library of SoC Design*

- **Physical Library**
- **Timing Library**
- **Device Modeling and SPICE Models**
- **Advanced Devices**
- **Discussion**

# Role and Importance of Library

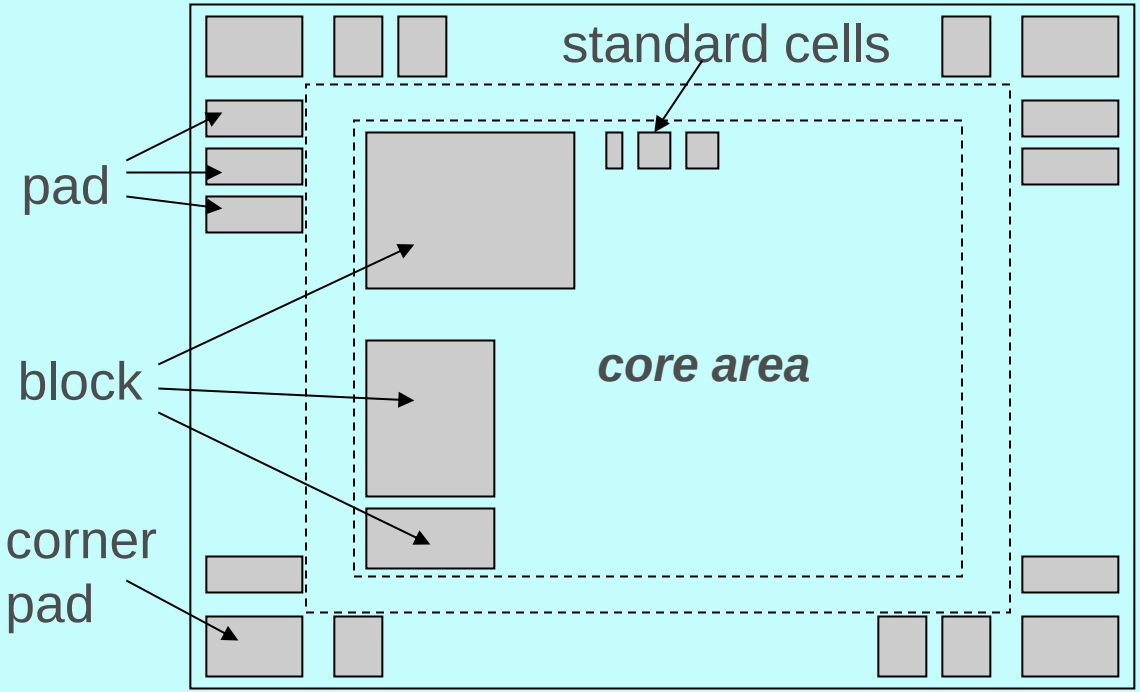
# Physical Library Data

Libraries used in SoC Design
Physical Library
Types of Cells used in Digital Design



# LEF: Library Exchange Format

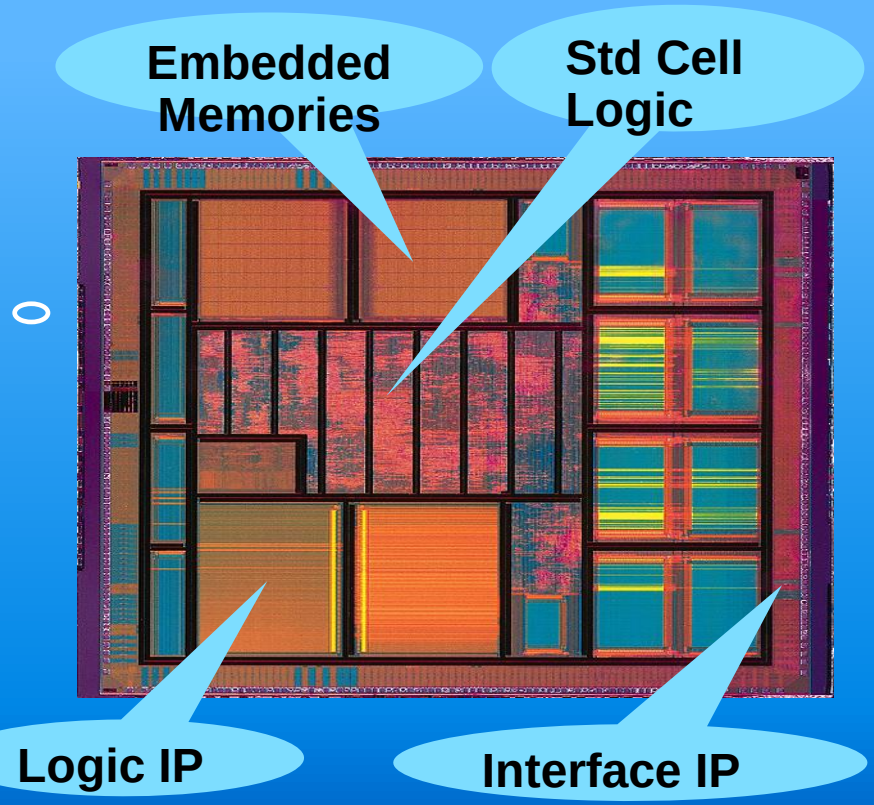
*Cadence Original, Industry Standard*



# Libraries used in an SoC Design

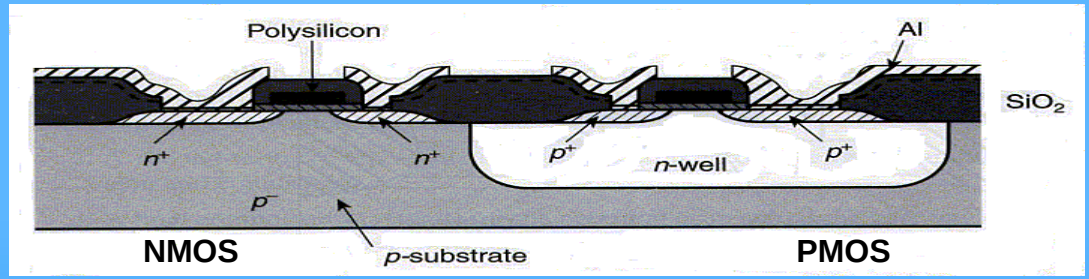
Electrical view for all IP blocks

- Logic and I/O cells (GPIO, PCI, SSTL, PECL etc.)
- Embedded Memory (SRAM, ROM, Register files, CAM etc.)
- Custom digital blocks (COT, datapath etc.)
- Interface IP and analog blocks (USB, SerDes, DDR etc)

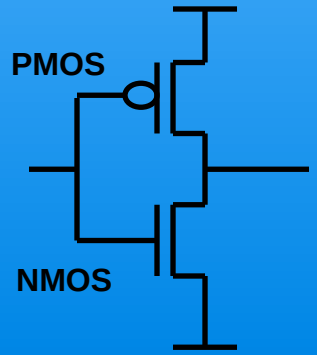


# CMOS Device

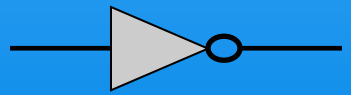
- A CMOS logic gate
- An Inverter
- Silicon
- Many details …



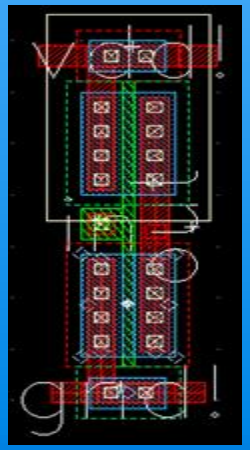

Cross section of CMOS




*Schematic*



*Symbol*



*Layout: GDSII*

*Physical Library (LEF)*

*Timing Library (.lib /TLF)*

*Noise Library (cdB)*

*Power Library (PGV)*

# LEF: Technology Data

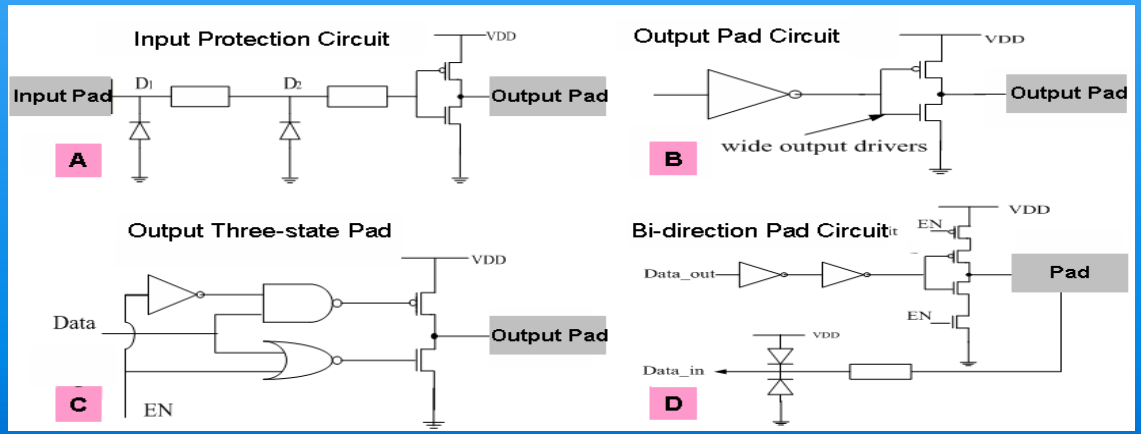
- Header and basic Information
- Routing Information
  - Routing metal layers, thickness, width, spacing, pitch
  - Connecting and cut layers, vias
  - Stacking and spacing
  - Wide wire, via arrays, via generation rules etc
- Minimum Pitch (SITE)

**LEF v5.6 Technology Syntax**

```
[VERSION statement]
[BUSBITCHARS statement]
[DIVIDERCHAR statement]
[UNITS statement]
[MANUFACTURINGGRID statement]
[USEMINSPACING statement]
[CLEARANCEMEASURE statement ;]
[PROPERTYDEFINITIONS statement]
[LAYER (Nonrouting) statement
 | LAYER (Routing) statement] ...
[SPACING statement ]
[MAXVIASTACK statement]
[VIA statement] ...
[VIARULE statement] ...
[VIARULE GENERATE statement] ...
[NONDEFAULTRULE statement] ...
[SITE statement] ...
[BEGINEXT statement] ...
[END LIBRARY]
```

# Physical Data: I/O Pad Cell Layout

- **Layout of I/O (Pad) Cell**
  - Standard height or multiple heights (ex. staggered I/O)
  - Most I/O Pad are the same height
  - Signal Pad and Power/Ground Pad Cells

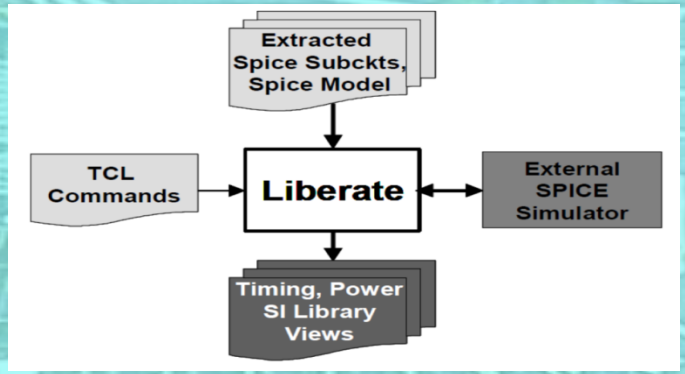


# SPICE & Library

- Physical Library: LEF
- Timing Library: Delay, Noise, IR and EM
- Device Modeling and SPICE Models
- Advanced Devices
- Discussion

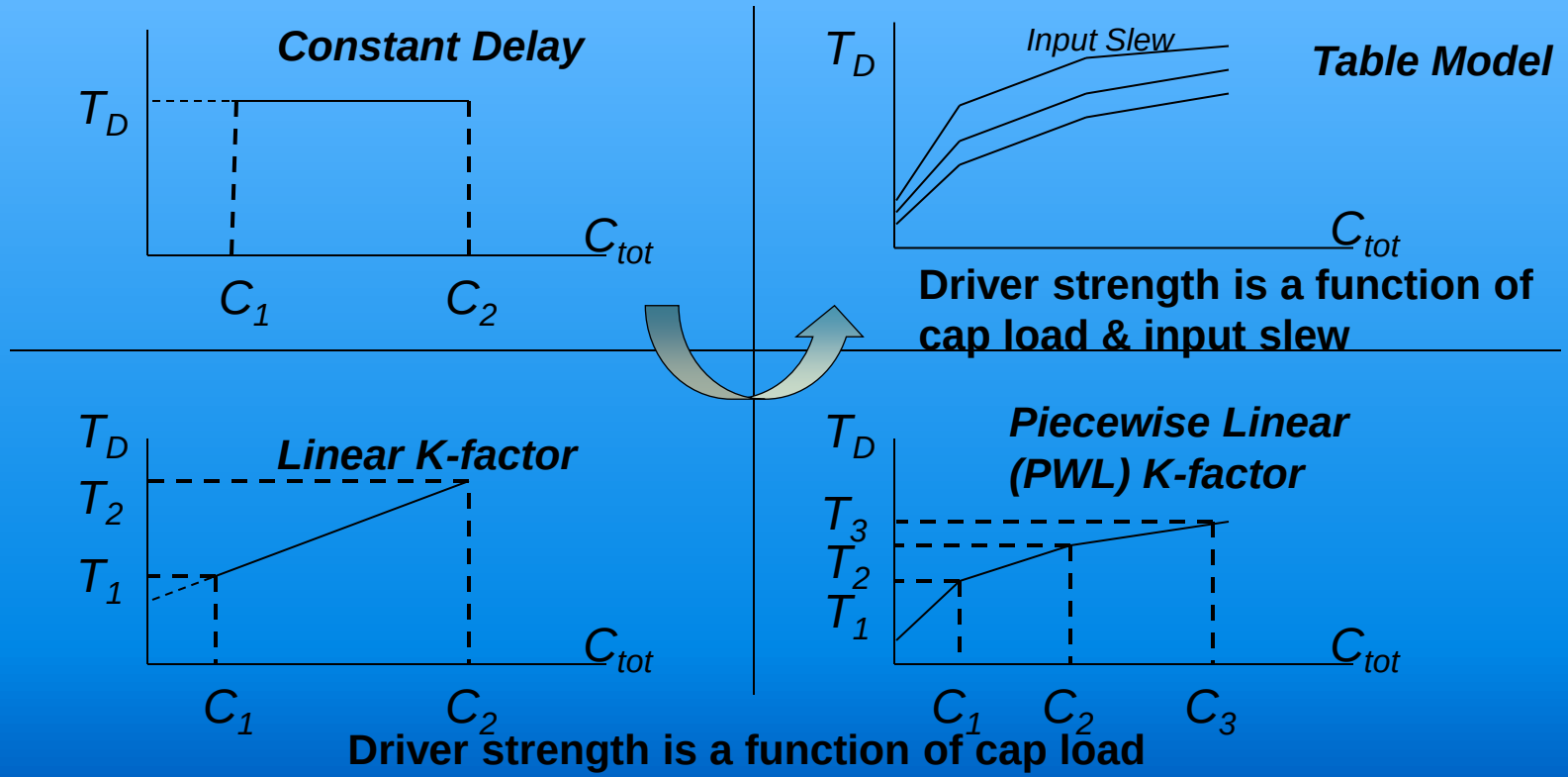
# Device Modeling and SPICE Models

Gummel–Poon Model
Doide Model & SPICE Models
PVT and Corners

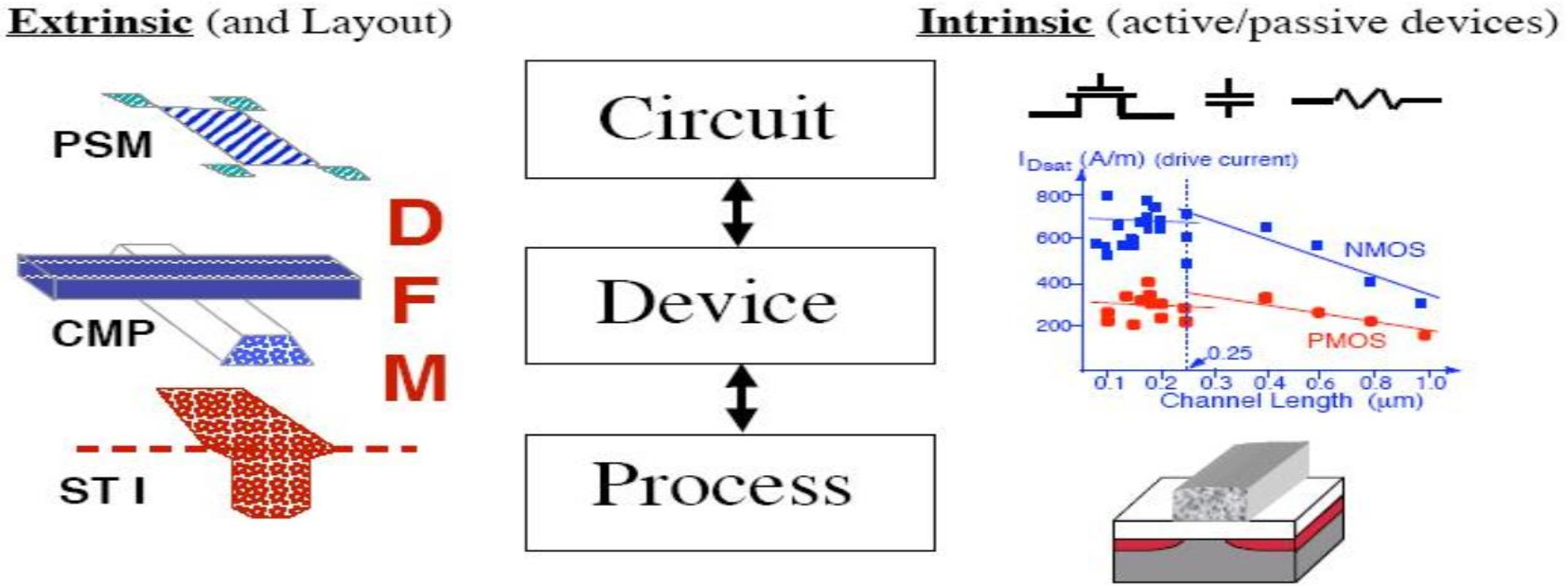


# Library Characterization: Timing Models

*Timing Delay as a Function of …*



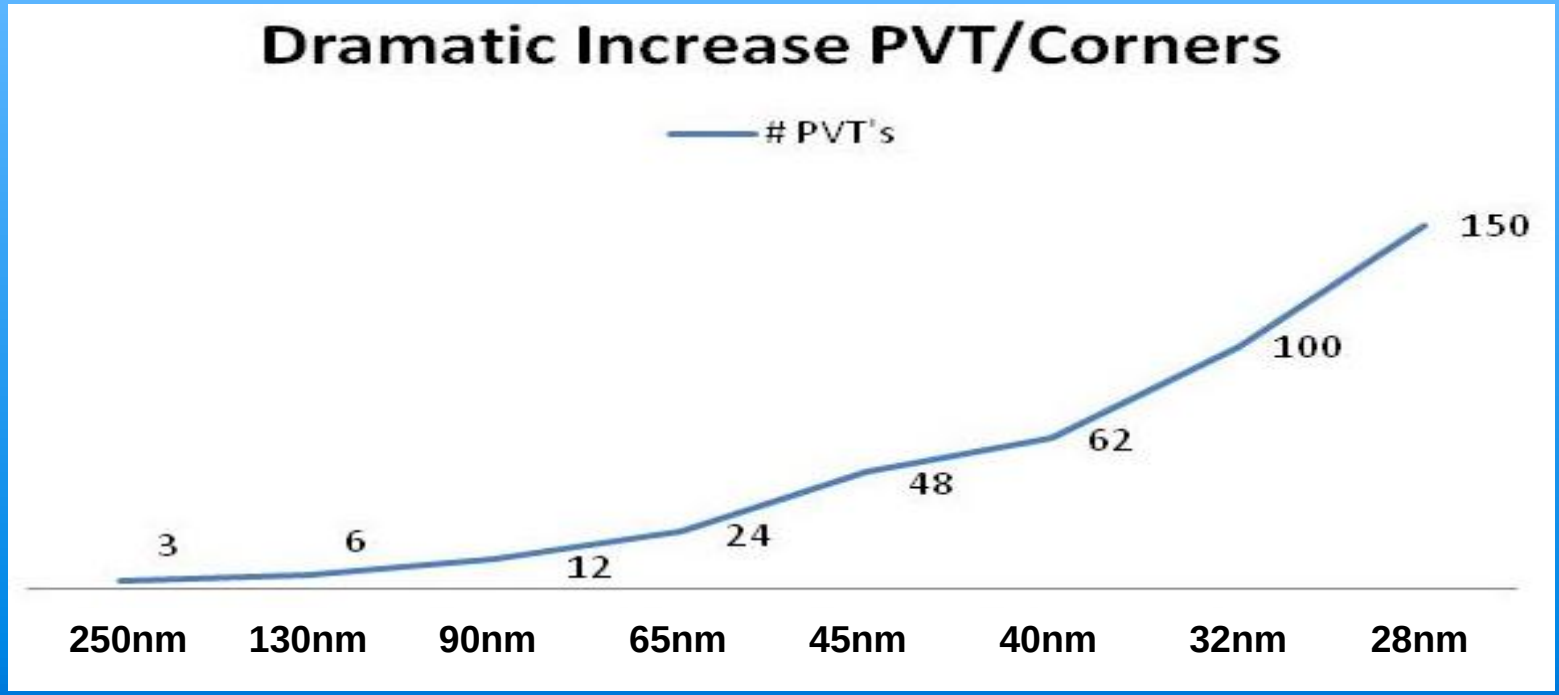
# Semiconductor Device Modeling




*Left side icons show typical manufacturing issues; right side icons reflect MOS scaling results based on TCAD. (Prof. Robert Dutton)*

# Addressing fundamental IP challenges

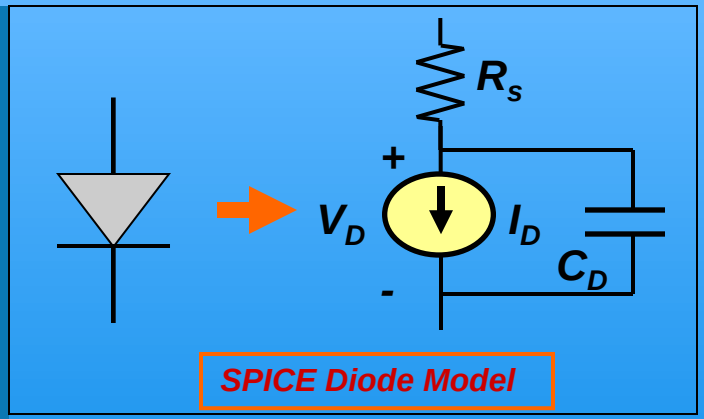
*Increased number of PVT/Corners in design flows*



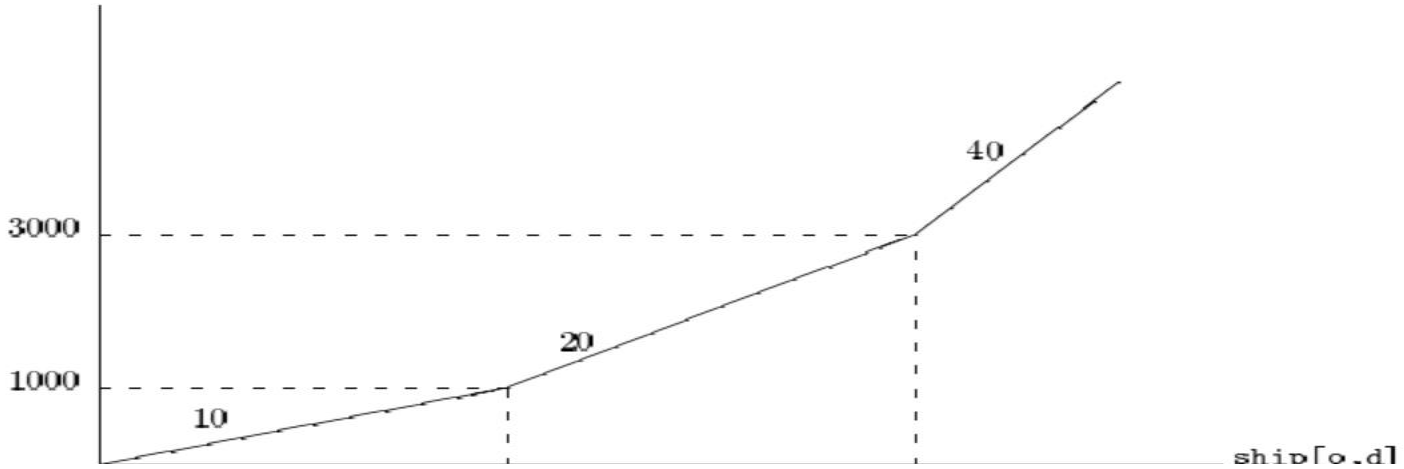
# The Simulation Programs:

*The SPICE Model*

- The SPICE Model – UCB
  - The most successful simulation program
- Good Simulation Program for
  - Better accuracy or computational
    - efficiency and robustness
- The Basic Diode SPICE Model
  - $I_D$: nonlinear current source
  - $C_D$: nonlinear capacitance



# PWL




Above: piecewise{10 -> 100;20 -> 200;40} ship[o][d];

In general:

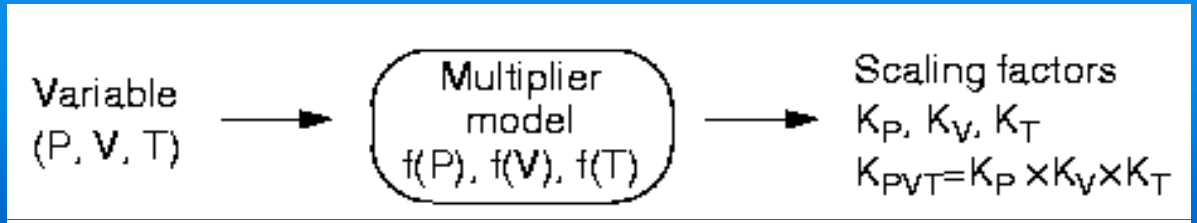
```
piecewise(i in 1..n)
        { slope[i] -> breakpoint[i];
        slope[n+1];
} ship[o][d];
```

*Reference: IBM OPL (optimum programming language)*

# Conditions of Characterization

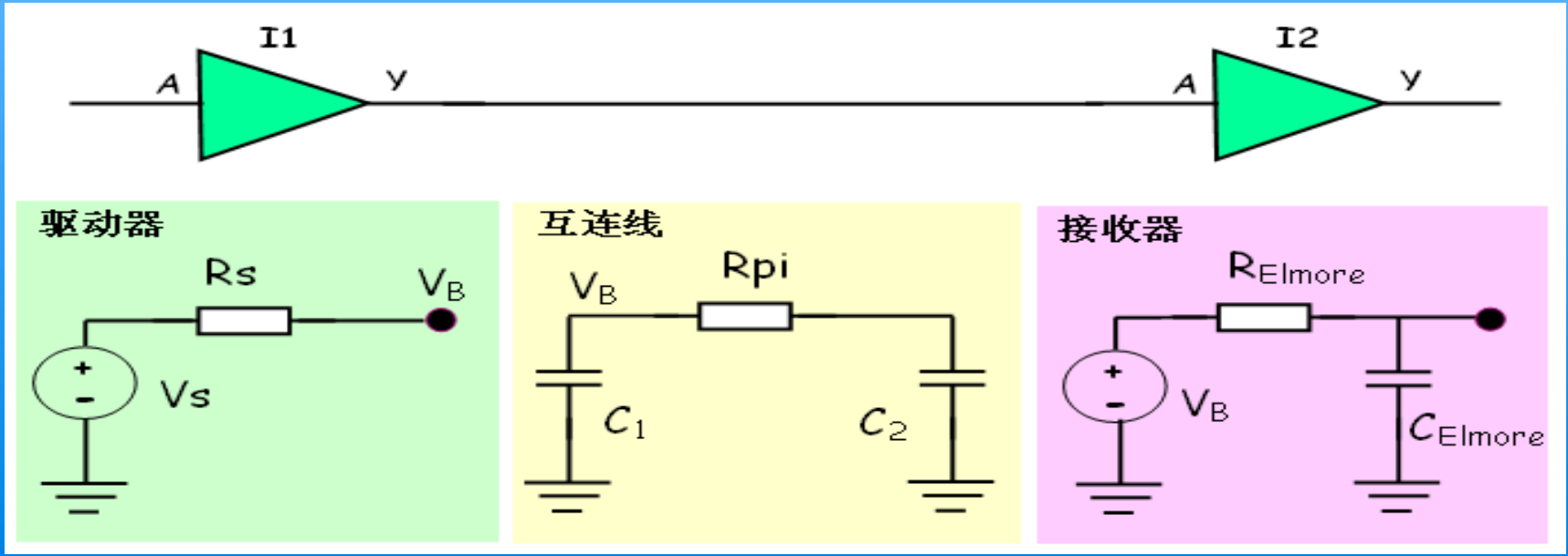
*PVT (Process, Voltage, Temperature) Derating*

- PVT
  - Process, Voltage, Temperature
- Corners
  - worst, typical, best; slow, typical, fast; TT, SS, FF (tt, ss, ff)
- Derating
  - |30%-70%|=40%, then 2X in .lib or derate is 0.5x,
  - versus |10%-90%|=80%




Actual cell delay = Original delay x $K_{PVT}$

# Timing Model – Driver and Receiver



# Delay Models for LC

- **NLDM (***Non-Linear Delay Model, 1997, Synopsys***)**

$$V_{out} = Z(s) \cdot V_S / [Z(s) + R)]$$

- **SPDM (***Scalable Polynomial Delay Model, 2000, SNPS***)**

$$\chi^2 = \sum_{i=1}^{N} \left(\frac{Y_i - y_i}{\sigma_i}\right)$$

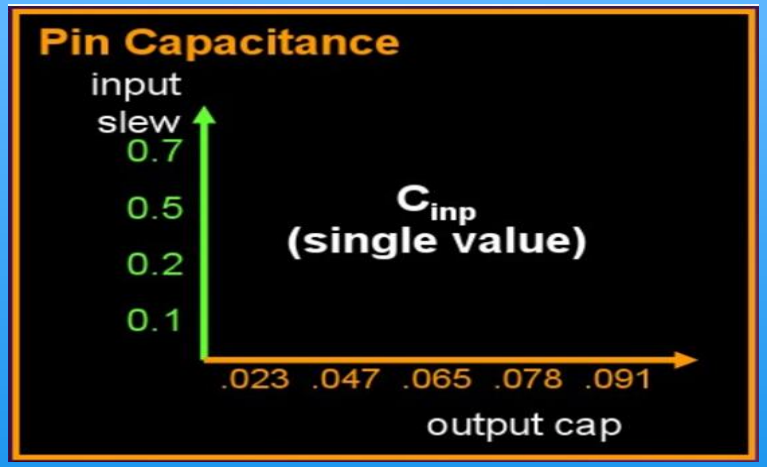
- **ECSM (***Effective Current Source Model, 2001, Cadence***)**

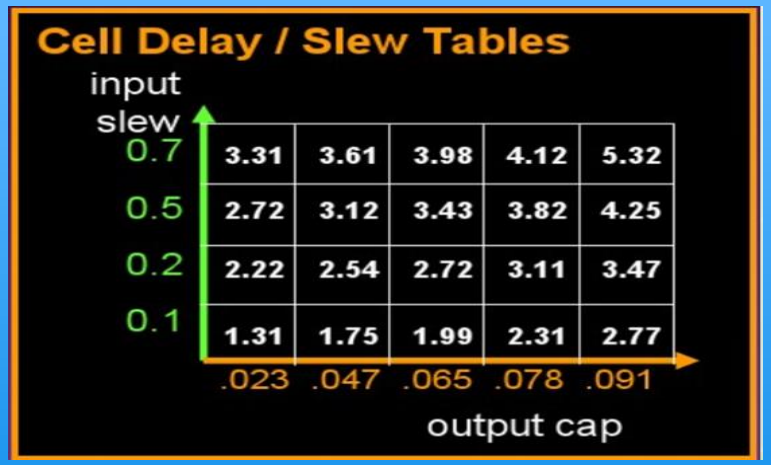
$$I_{out}(t_1, t_2) = \frac{\int_{t_1}^{t_2} I_{out}(t)dt}{t_2 - t_1} = C_{load} \frac{\int_{t_1}^{t_2} V_{out}(t)dt}{t_2 - t_1}$$

- **CCS Model (***Composite Current Source Model, 2004, Synopsys***)**

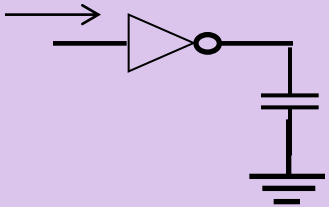
# Library Characterization using NLDM

*Timing only*




**Measure current and voltage at input pin for receiver model**

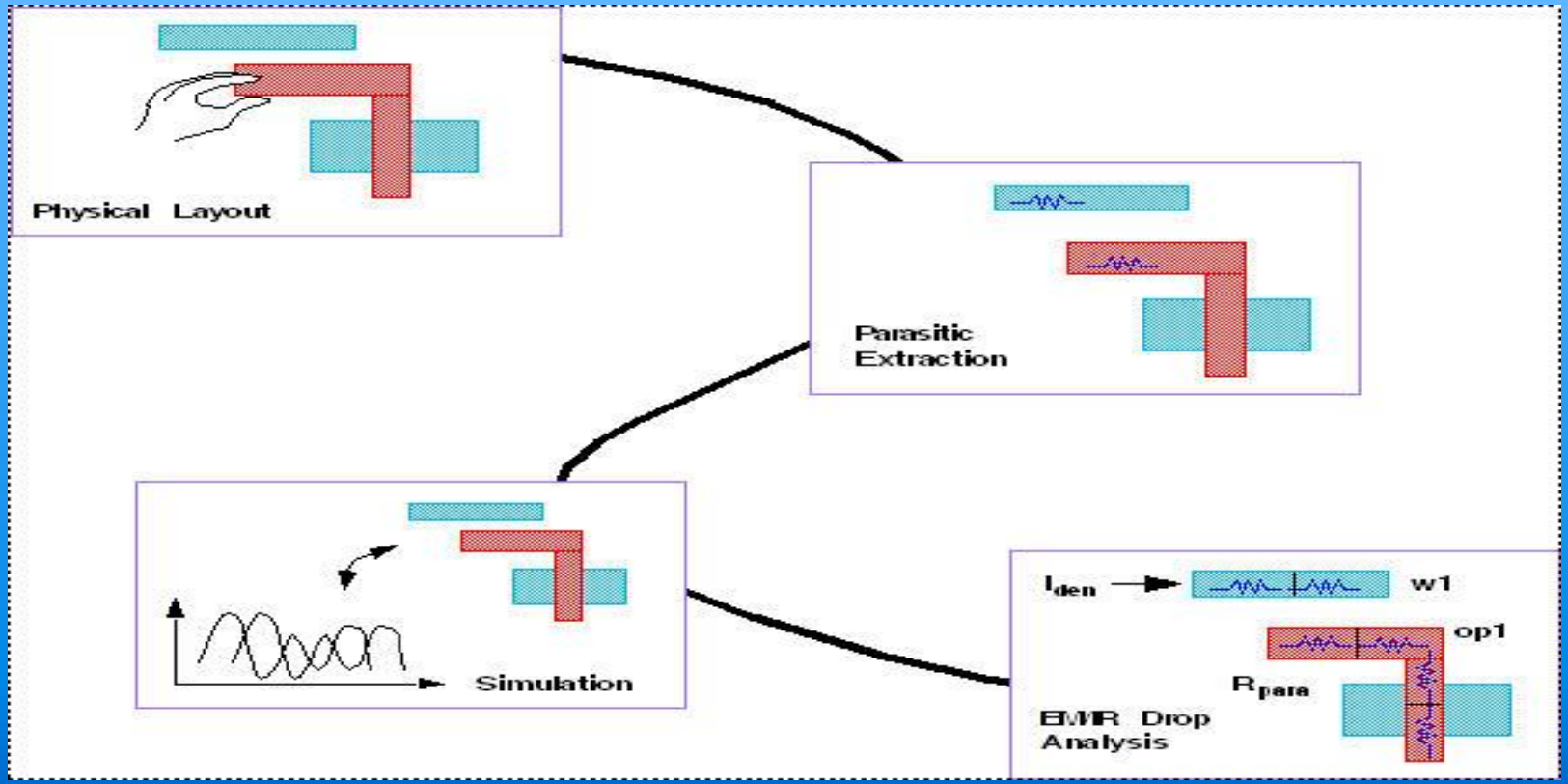


**Measure cell delay and output slew**

# Tasks of Library Characterization
## Timing, Noise, Power

| Feature | Goals |
|---|---|
| **Standard cells** | **Delay is the key** |
| **Multi-bit Cells, Memory** | full automatic vector generation for up to 8 bits (extending to 64 bits in 13.1) |
| **EM** | To support EM characterization with increased automation |
| **Leakage characterization** | leakage is not prone to oscillation and extended simulation duration times making it more accurate and more efficient, it also considers all output states |
| **Delay characterization** | **To** consider all internal states in sequential cells resulting in a more worst-case Clk->Q delay– over 40% difference seen in a commercial complex flop |
| **Constraint characterization** | **C**onstraint characterization vector generation considers all the states of internal nodes not just a single state like the competition and hence finds more worst-case values. Liberate supports “minimize D->Q” to include the “degrade” effect on Clk->Q arc a potential source of optimism in static timing analysis. |
| **I/O cells** | **To** permit per arc low level control for characterizing complex cells without needing to define a “logic function” for each arc. It can generate CCSN for I/Os. **Liberate + Spectre APS** offers the best accuracy/performance for complex I/Os. |

# Electromigration and IR Drop Overview



# SPICE & Library

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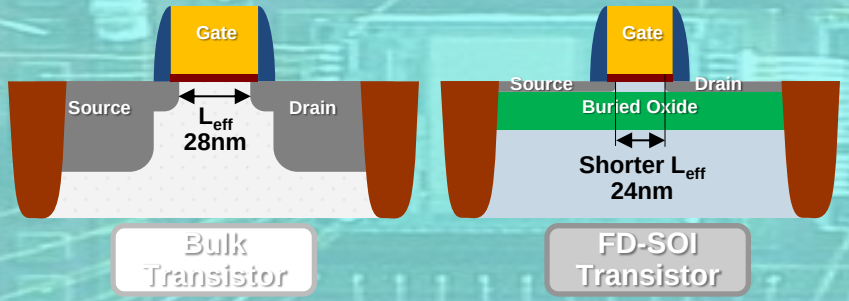
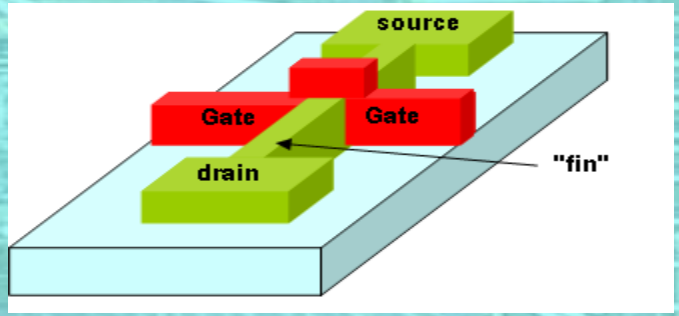
# BSIM MOSFET MODEL

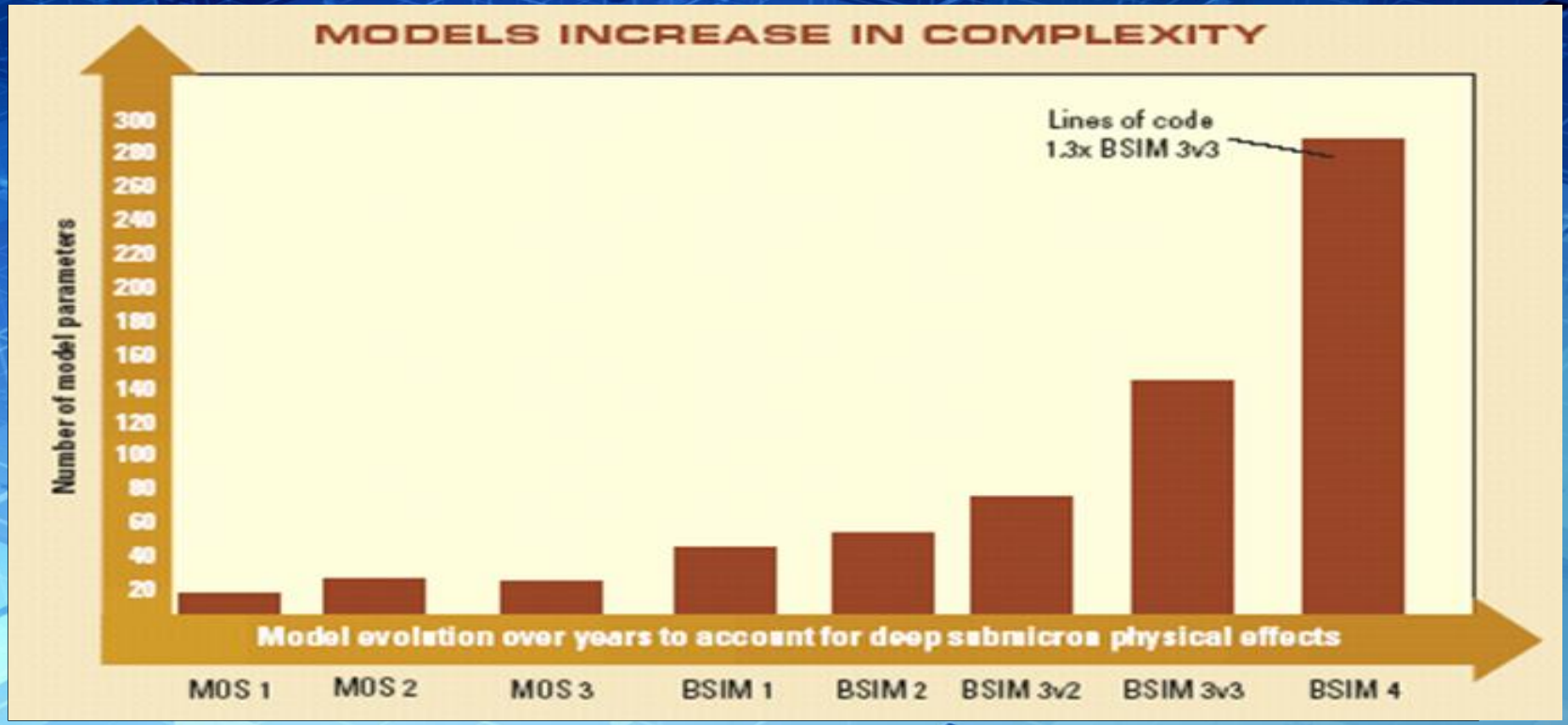


# Device Modeling and Simulation

*Meet Shrink, Processing Challenges*

***We need mathematicians!***



# Generations of SPICE Models

表2-7 SPICE模型特征与应用范围 (2008)

| SPICE Level | 年代 | 模型特征 | 应用范围 |
|---|---|---|---|
| 第一代<br>SPICE Level 1 | 1968 | Shichman-Hodges模型(电流-电压平方率特性) | 适用于精度要求不高的长沟道MOS晶体管 |
| SPICE Level 2 | 1970 | 二维解析模型(考虑MOS器件二阶效应), Gummel-Poon模型 | 适用于BJT |
| SPICE Level 3 | 1979 | 半经验短沟道模型 | 适用于MOS晶体管，>0.9 um |
| 第二代<br>SPICE Level 28,<br>BSIM1 | 1987 | 半经验式，适合DSM设计的(短沟道)模型 | 适用于数字和模拟设计，0.3—0.5 um |
| SPICE Level 39,<br>BSIM2 | 1989 | 半经验式，适合DSM设计的模型 | 适用于MOS晶体管，> 0.2 um |
| 第三代<br>SPICE Level 49,<br>BSIM3v3 | 1995 | S/D 电阻, W/L | 适用于MOS晶体管，0.18 um |
| BSIM4v6 | 2001 | 考虑到栅极泄漏, 非对称S/D电流分布 | 适用于130 nm，90 nm，65 nm |
| PSP Model | 2006 | 表面电势模型 | 适用于 90 nm，65 nm，45 nm |

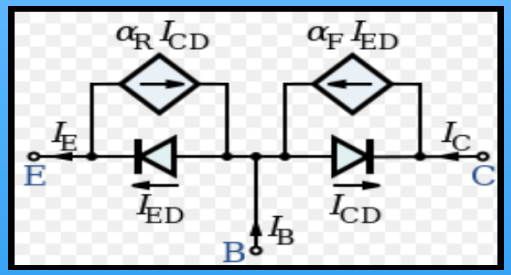
# SPICE and BSIM models from UCB (as of 2015)

- SPICE1 (Laurence Nagel/Prof. Donald Pederson, 1973, UCB, Fortran)
- SPICE2 (Stable release, 1975, Fortran)
- SPICE3 (Thomas Quarles/Prof. A. Richard Newton, 1989, C)
- **BSIM3 (BSIM3v3), for DSM**
- **BSIM4**, used for 0.13um, 90nm, 65nm,
  - **extended to 45/40nm, 23/28nm and 22/20nm**
- **BSIM6**, for RF/analog
- **BSIMSOI**, based on BSIM3, used by IBM, AMD
- **BSIMCMG**, for common multi-gate or FinFET
- BSIMIMG, for independent multi-gate, the latest
  - ex. ind. double-gate (ultra-thin body) & BOS SOI transistors (UTBB)

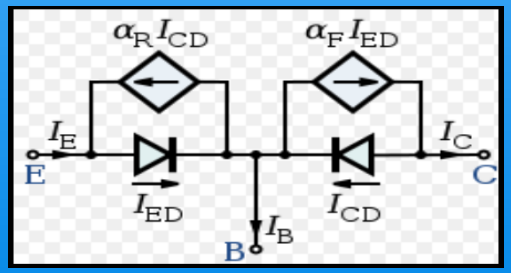
# BSIM4 – Basic Effects modeled in

- Short and narrow channel effects on threshold voltage
- Non-uniform doping effects
- Mobility reduction due to vertical field
- Bulk charge effect
- Carrier velocity saturation
- Drain induced barrier lowering (DIBL)
- Channel length modulation (CLM)
- Substrate current induced body effect (SCBE)
- Parasitic resistance effects
- Quantum mechanic charge thickness model

# Ebers-Moll Model (BJT, ?1987)
# Gummel–Poon Model (BJT, 1970)

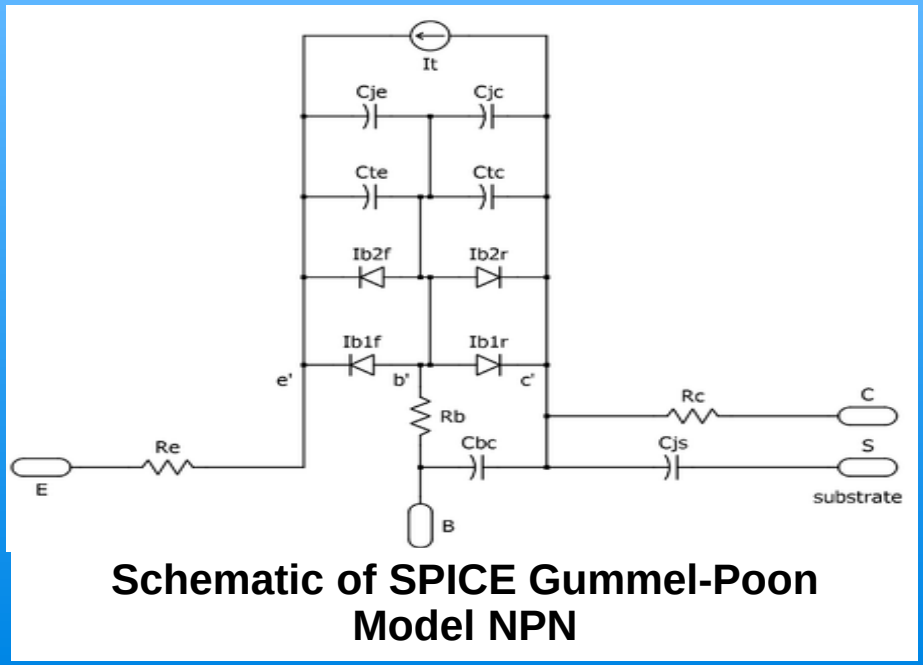



**Ebers–Moll Model for an NPN transistor.**




**Ebers–Moll Model for an PNP transistor.**

*E-M model: EM1,EM2,EM3. More Complex, for big DC signal*




**Schematic of SPICE Gummel-Poon Model NPN**

*G-P model: good physics; simple math; high resolution*

# Final Expression of Vth

$$V_{th} = V_{th0} + K_1\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right) - K_2 V_{bseff}$$

$$+ K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + \left(K_3 + K_{3b} V_{bseff}\right)\frac{T_{ox}}{W'_{eff} + W_0}\Phi_s$$

$$- D_{VT0w}\left(exp\left(-D_{VT1w}\frac{W'_{eff} L_{eff}}{2 l_{tw}}\right) + 2exp\left(-D_{VT1w}\frac{W'_{eff} L_{eff}}{l_{tw}}\right)\right)\left(V_{bi} - \Phi_s\right)$$

$$- D_{VT0}\left(exp\left(-D_{VT1}\frac{L_{eff}}{2 l_t}\right) + 2exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi} - \Phi_s\right)$$

$$- \left(exp\left(-D_{sub}\frac{L_{eff}}{2 l_{t0}}\right) + 2exp\left(-D_{sub}\frac{L_{eff}}{l_{t0}}\right)\right)\left(E_{ta0} + E_{tab} V_{bseff}\right) V_{ds}$$

# SPICE & Library

- Physical Library: LEF
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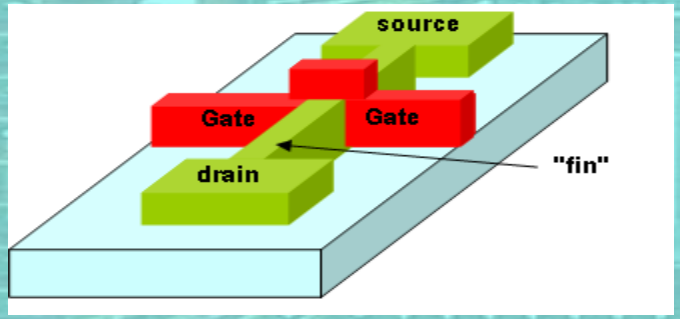
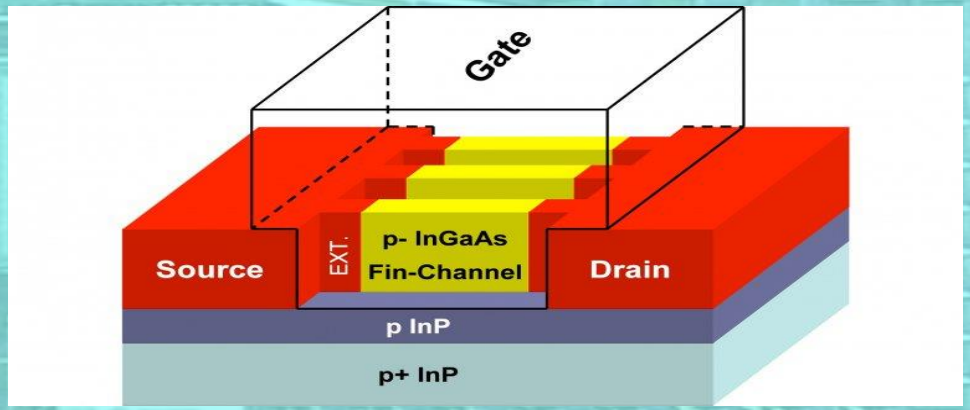
# Why FinFET?

## The gate controls a thin body from more than one side

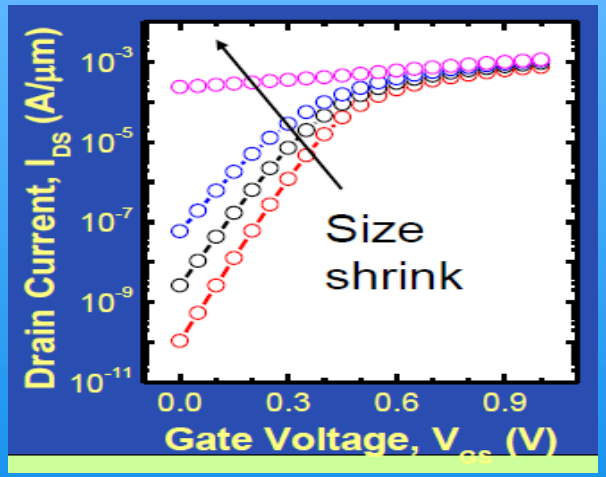


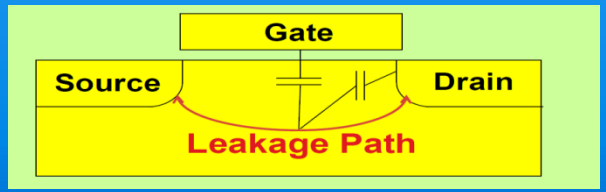




- Thin body
- Gate fully control
- Suppress leak and SCE

# Problem with MOSFET Shrinking

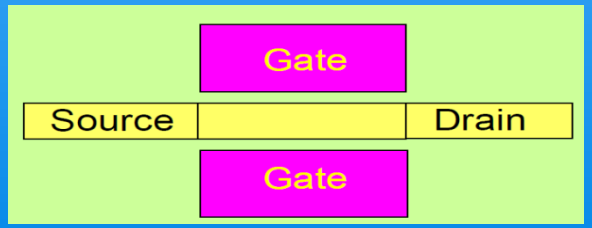
- Off-state Leakage
  - Sub-threshold swing limitation
  - Punch-through
- Strong short channel effect
  - DIBL, Vth,
- Strong variation (Vth and Swing)
  - Sensitive to channel length
  - Sensitive channel doping
  - Low yield and high design cost
- Reliability
  - HCI, NBTI, PBTI, TDDB, …
- Electron transportation scattering
  - High channel doping
  - High vertical electric field

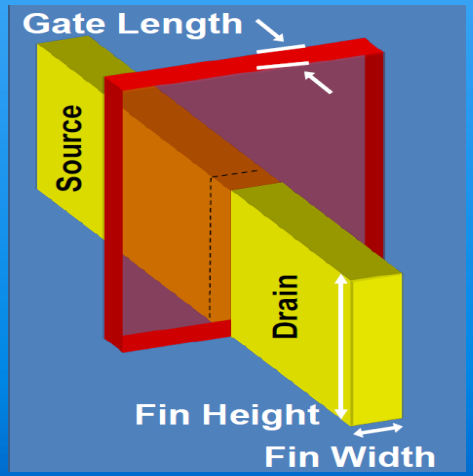


# BSIMCMG

- FinFET
  - To cover: geometry, bias, temperature, DC,
  - AC, RF, and noise characteristics
- Compact Modeling for Circuit Simulation



# SPICE & Library

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- **Timing Library:** Delay, Noise, IR and EM
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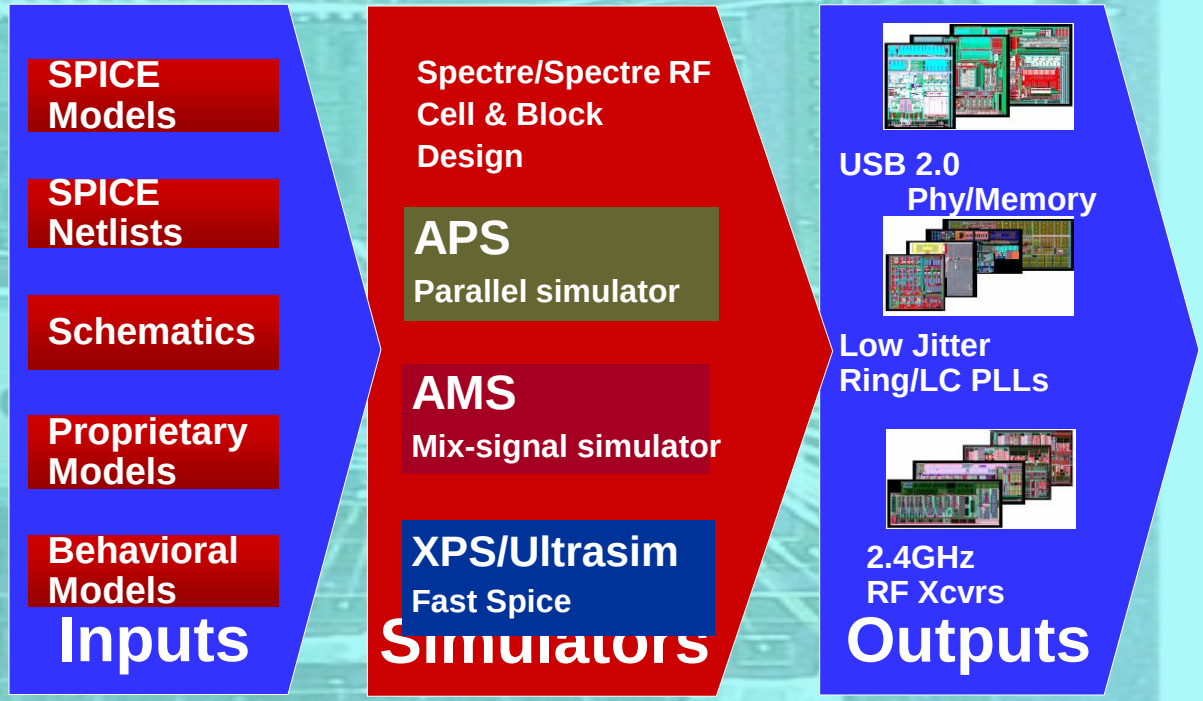
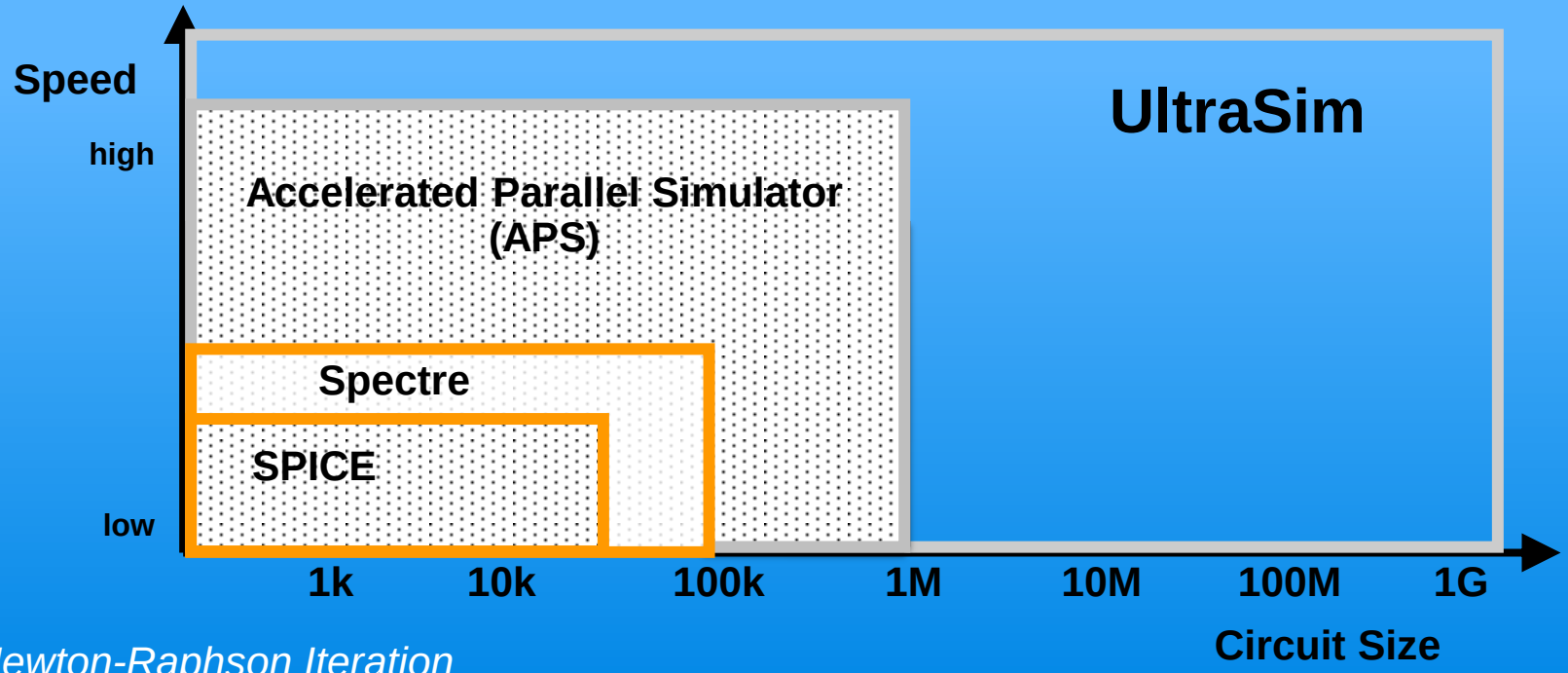
# Analog Simulation

## *Multi-mode Simulation Solution*

- Single solution for all simulation needs: analog, RF, AMS & full-chip
- Shared technology enables common device models, equations and consistency in results between simulators
- Maximize your investment with the token licensing model

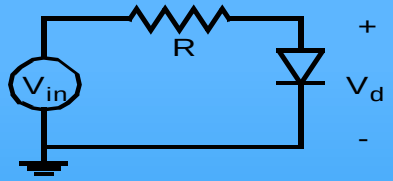


# Evaluating Simulator Speed and Capacity



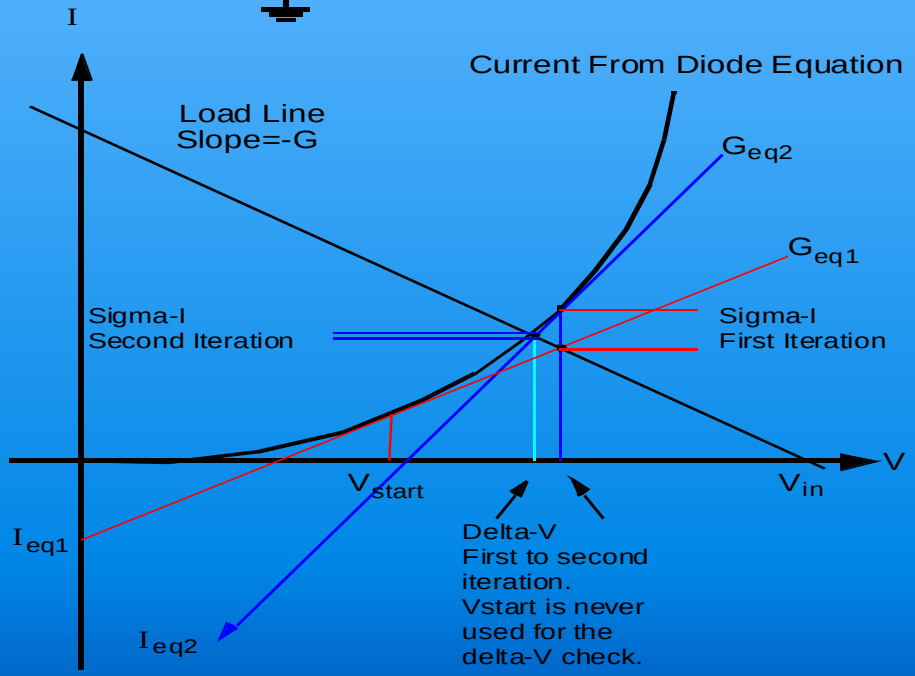

*Newton-Raphson Iteration*
*Monte Carlo*
*MMSIM*
*IO-SSO*

# Understanding the Newton-Raphson Iteration Method




**Diode Equation**

$Id = Is\ (e^{Vd/n*Vt} - 1)$



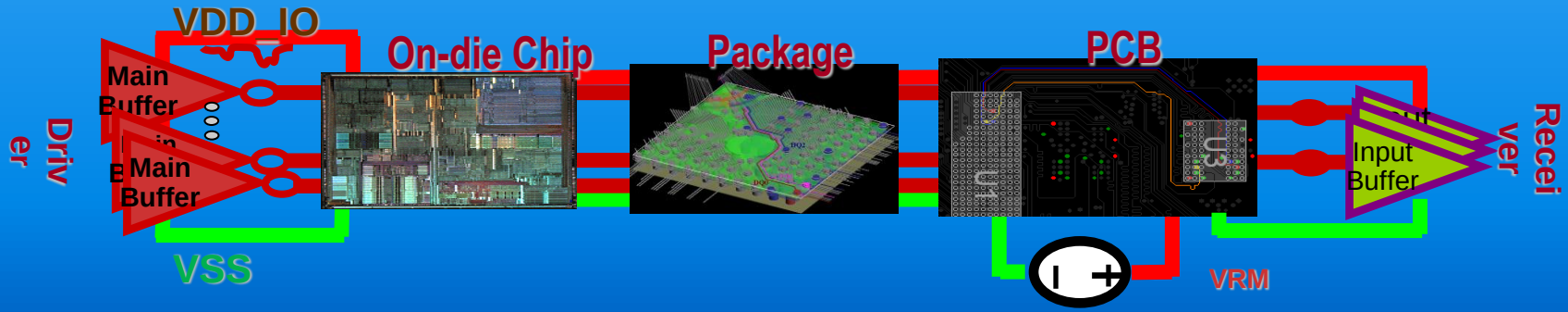

To accurately represent the tangent, both the slope ($G_{eq}$) and the intercept ($I_{eq}$) are needed. This preserves the diode terminal characteristics at only the point where the tangent is taken. The device current and the tangent are supplied by the device model.

On the third iteration, delta-V and sigma-I would be very small, and the linear solution would be very close to the nonlinear solution.

# Who cares about IO-SSO?

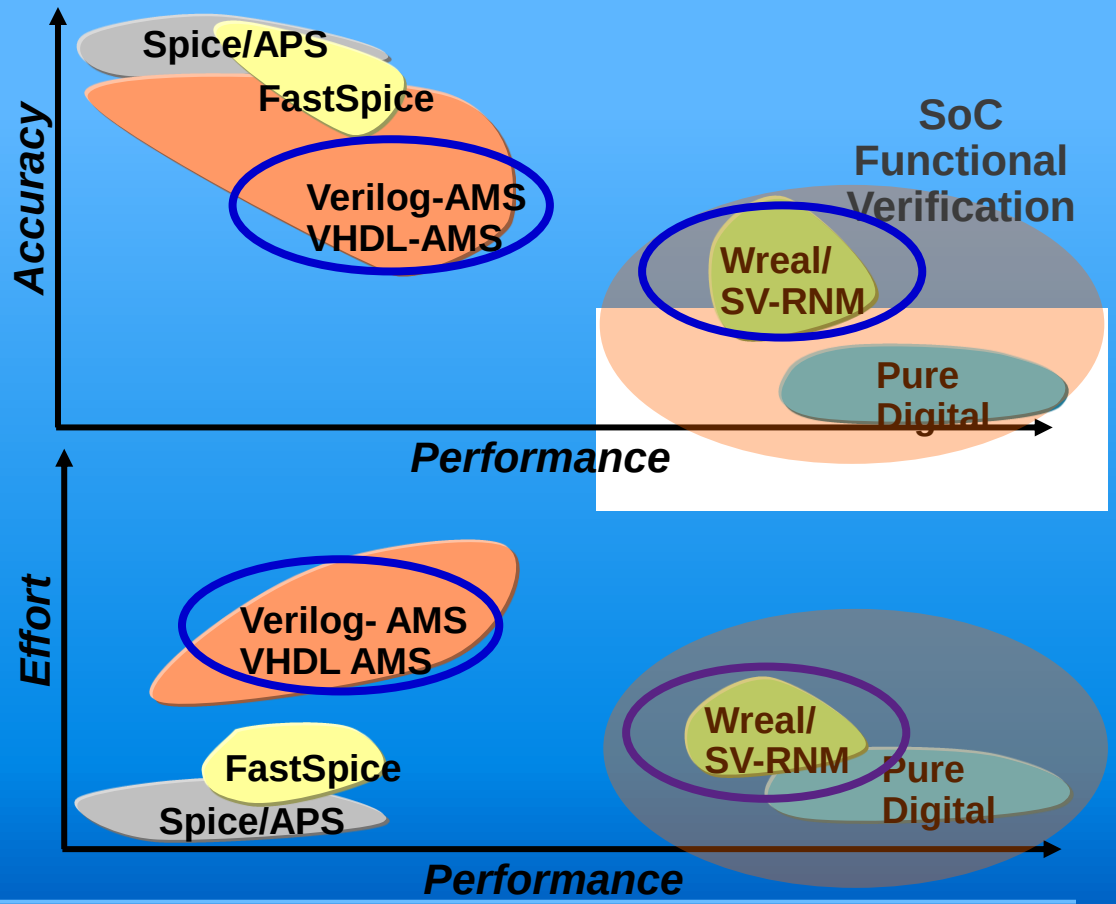
*Who are the target users for IO-SSO analysis?*

- Memory Interface Designers
  - ***IO Chip Designer*** (SoC with DDR interface or memory provider companies – Examples: Micron, nVidia, AMD, etc)
    - IO-SSO Analysis Suite Opportunity
  - IC Package Designer (Allegro Sigrity Power-Aware SI opportunity)
  - PCB Designer (Allegro Sigrity Power-Aware SI opportunity)



# Choose Real Number Modeling for Performance

- **Model analog block operation as discrete real data**
  - Signal flow based modeling approach
- **Key advantages of RNM**
  - Discrete solver only
  - Very high simulation performance
  - Event driven or sampled data modelling of analog operation
  - No analog solver, no convergence problems!
  - Can be written by analog designers and/or digital verification engineers
- **RNM languages include**
  - Verilog-AMS (wreal), VHDL
  - SystemVerilog, ***e***



# Summary

- Physical Library – LEF
  - Physical, std Cells, I/O (ESD),
  - Antenna Cell (PID/ESD)
- Timing Library - .lib (TLF)
  - Device Modeling & SPICE models
  - Delay Models – NLDM, ECSM, CCS
  - Noise, power
- Simulation and Timing
  - Analog/RF/AMS
  - Accuracy and Speed
  - I/O SSO