University of Chinese Academy of Sciences

Impact of Big Data on SoC Design

IP Design and SoC Integration

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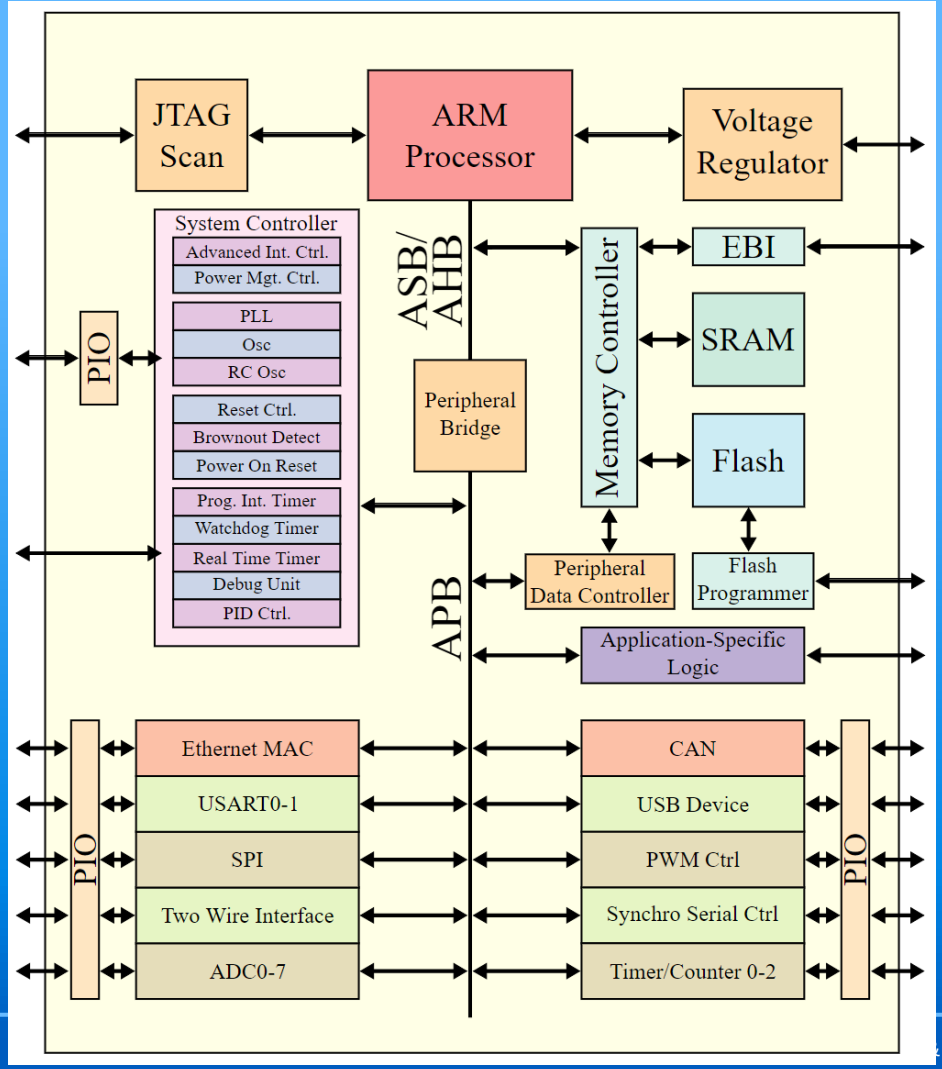
IP Design and SoC Integration

- **IP Verification and Design**
- **Common & General Purpose IPs**
- **Analog IP and Digital IP**
- **High-Speed IP**
- **Applications and Discussion**

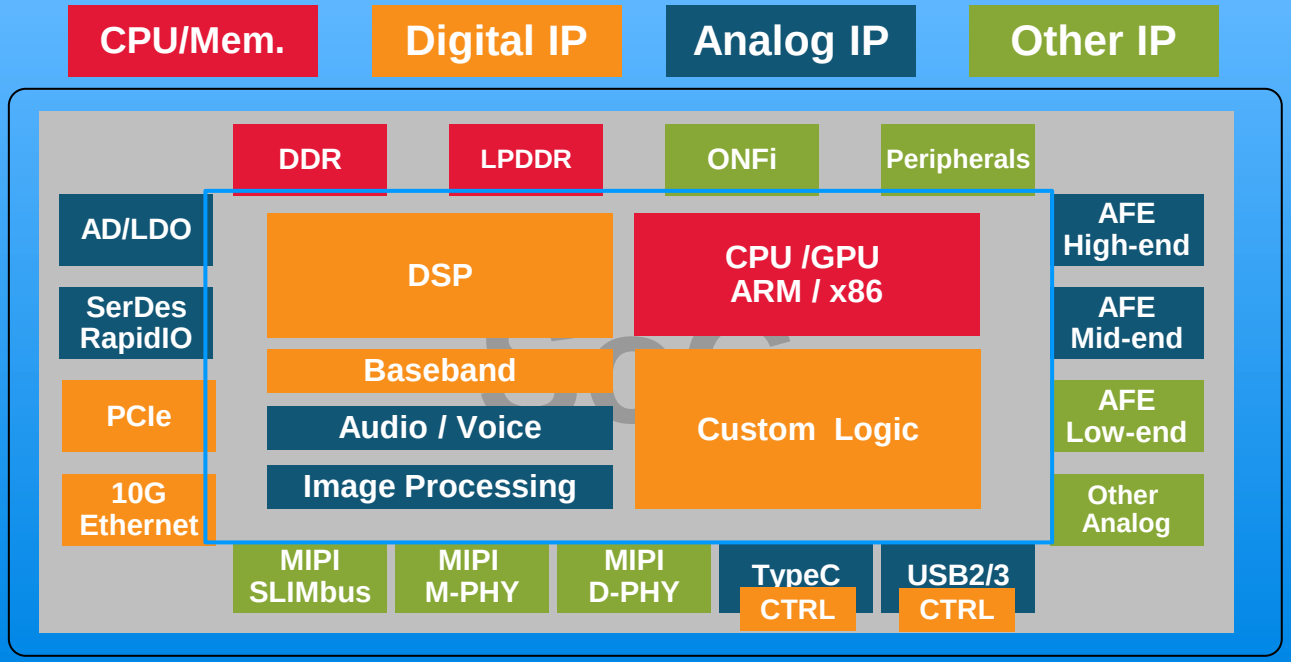
Ref: *List of Semiconductor IP Vendors*

Contents in a SoC

- CPU
- Memory
- Logic
- I/O
- IP



More IPs are being Integrated in SoC Designs

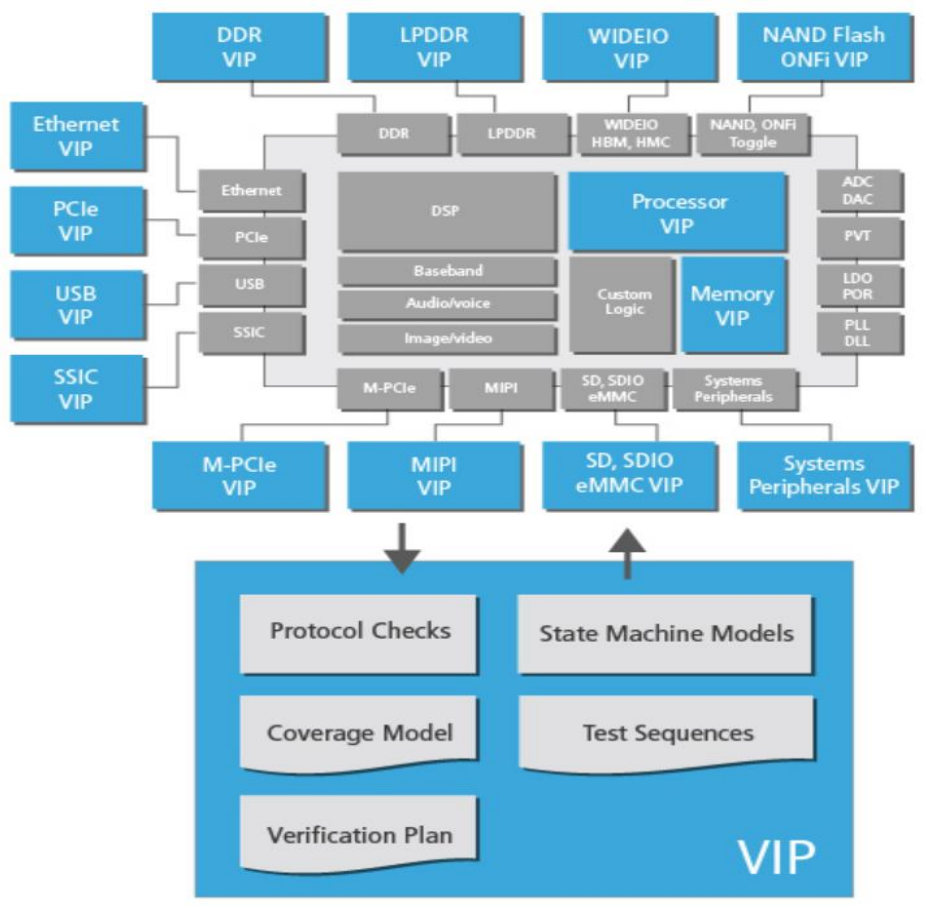


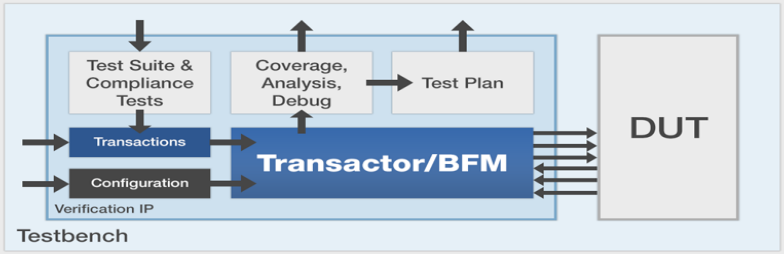
Increased SoC Designs in the Products

Types of IP Designs

- Design type
  - Digital, Analog, MS
  - ex. DSP, PLL/DLL
- Function type
  - **Lib./Module**
  - **Emb./Ext. Mem.**
  - Conn./Interface
  - MCU (IoT)
  - DSP (data)
  - CPU/GPU etc

Verification IP and Design IP





PROTOCOL SUPPORT

- AMBA ACE
- AMBA AHB
- AMBA APB
- AMBA AXI3
- AMBA AXI4
- AMBA CHI
- eDP 1.3
- Ethernet
- HDMI
- I2C
- I2S
- JTAG
- MIPI CSI-2
- MIPI DigRFv4
- MIPI DSI
- MIPI LLI
- MIPI MPHY
- MIPI UNIPRO
- PCI Express
- SAS
- SmartCard
- SPI
- SPI4-2
- UART
- USB High Speed + OTG
- USB Super Speed
- VByOne

MEMORY MODELS

- AHB Slave
- AXI Slave
- DDR2
- DDR3
- DDR4
- eMMC 4.5
- GDDR5
- HMC
- I2C EEPROM
- LPDDR2
- LPDDR3
- LPDDR4
- ONFI 2.1 NAND Flash
- SAMSUNG NOR Flash
- SDCard
- SPANSION NOR Flash
- SPI NOR Flash

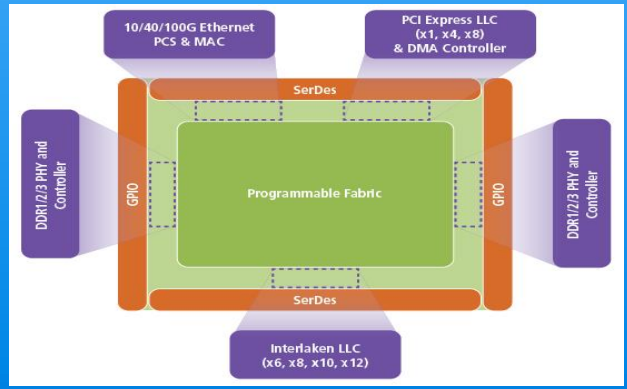
RESOURCES

MIPI LLI Verification using Questa Verification IP
JOURNAL ARTICLE

New School Thinking for Fast and Efficient Verification Using EZ-VIP
ON-DEMAND WEB SEMINAR

Soft IP and Hard IP

- Soft IP
  - RTL codes to be sythsized
  - To match on target library
  - Needs to go through hardening process
- Hard IP
  - IP block or hardened
  - Fixed size and performance
  - Usually use “as is”



Processor IP - ARM Architecture

ARM architectures

Architecture	Bit width	Cores designed by ARM Holdings	Cores designed by third parties	Cortex profile	References
ARMv1	32/26	ARM1			
ARMv2	32/26	ARM2, ARM3	Amber, STORM Open Soft Core[33]		
ARMv3	32/26	ARM6, ARM7			
ARMv4	32/26	ARM8	StrongARM, FA526		
ARMv4T	32	ARM7TDMI, ARM9TDMI			
ARMv5	32	ARM7EJ, ARM9E, ARM10E	XScale, FA626TE, Feroceon, PJ1/Mohawk		
ARMv6	32	ARM11			
ARMv6-M	32	ARM Cortex-M0, ARM Cortex-M0+, ARM Cortex-M1		Microcontroller	
ARMv7-M	32	ARM Cortex-M3		Microcontroller	
ARMv7E-M	32	ARM Cortex-M4, ARM Cortex-M7		Microcontroller	
ARMv7-R	32	ARM Cortex-R4, ARM Cortex-R5, ARM Cortex-R7		Real-time	
ARMv7-A	32	ARM Cortex-A5, ARM Cortex-A7, ARM Cortex-A8, ARM Cortex-A9, ARM Cortex-A12, ARM Cortex-A15, ARM Cortex-A17	Krait, Scorpion, PJ4/Sheeva, Apple A6/A6X	Application	
ARMv8-A	64/32	ARM Cortex-A53, ARM Cortex-A57,[34] ARM Cortex-A72[35]	X-Gene, Nvidia Project Denver, AMD K12, Apple A7/A8/A8X, Cavium Thunder X [36][37][38]	Application	[39][40]
ARMv8.1-A	64/32	No announcements yet		Application	
ARMv8-R	32	No announcements yet		Real-time	[41][42]

IP Design & SoC Integration

- IP Verification & Design: Hard IP and Soft IP
- **Common & General IPs: Standard Cells, I/O, Memory**
- Analog IP & Digital IP: Interface & Interconnect Bus
- High-Speed IP: RF and Giga-bit data
- Discussion: Applications

Library Cells

- Layout
  - Extract, Abstract, Connectivity, GDSII (CIF), LEF
- Types of Cells [Physical shapes]
  - Standard Cells
  - I/O Pad Cells
  - Block “Mega” Cells: COT, Memory Cells, IP
- Other Types of Cells (no timing info)
  - Corner Cells
  - Filler Cells
  - Tie-Hi Cell, Tie-Lo Cell
  - Antenna Cells
  - Dummy Cells
- DSM and nm Cells
  - Decap cells
  - Low leakage cells (MSV)
  - Level Shifter Cells
  - Well-Tap Cells

表2- 5标准单元逻辑电路两大类型：组合逻辑电路和时序逻辑电路

组合逻辑电路类型

类 型	种 类	特 征
互补型	PUN，PDN	设计简单，用于静态
反向型	INV，NAND，NOR	NAND 快于 NOR
非反向型	BUF，AND，OR	
其它	MUX，XOR，TBUF，AOI/OAI	逻辑关系复杂

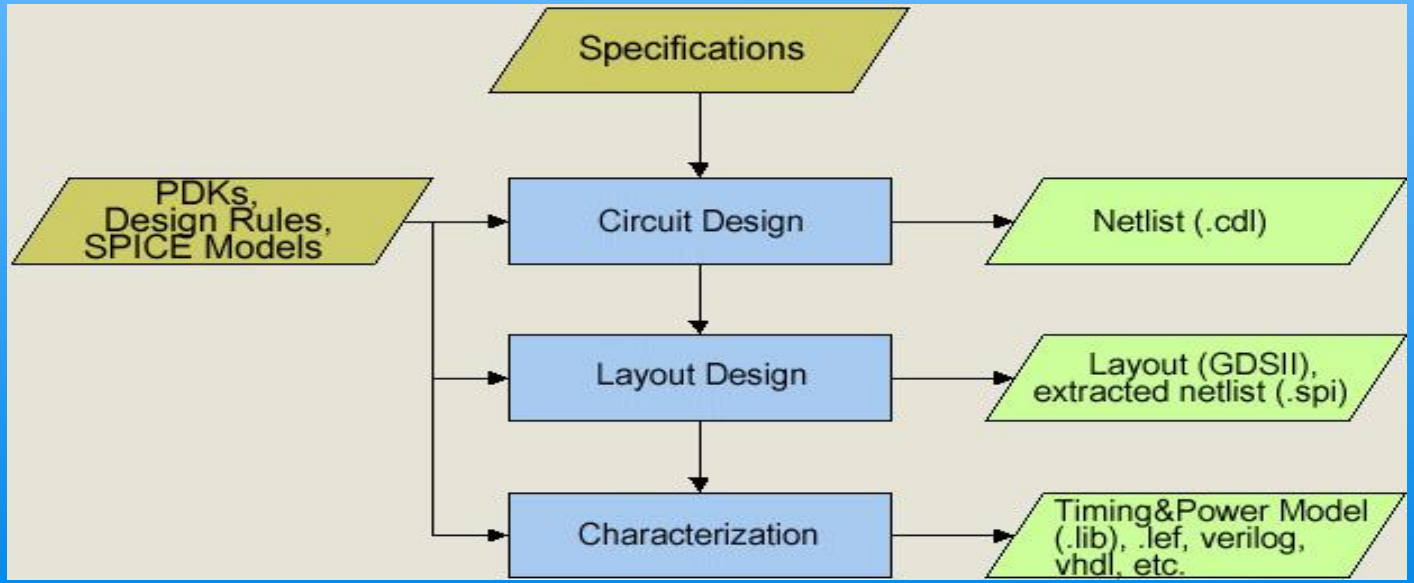
时序逻辑电路类型

类 型	种 类	特 征
锁存器	Latch（例如：DLatch）	电平驱动，时序复杂
寄存器类	flip flop，register（例如：DFF），counter，memory （ROM，RAM）	前沿驱动，时钟控制

Types of Library Cells

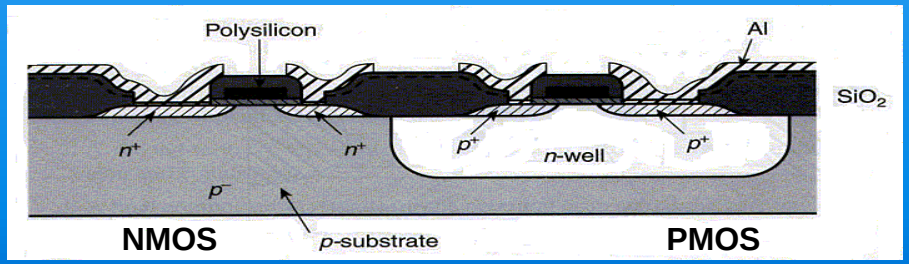
um/nm	0.5	0.35	0.25	0.18	130	90	65
Standard Cells	100	150	200	500	1000	1000	1000
I/O, Blocks	yes	yes	yes	yes	yes	yes	yes
Antenna Cells	-	-	-	yes	yes	yes	yes
Decap Cells	-	-	-	yes	yes	yes	yes
Low Leakage	-	-	-	yes	yes	yes	yes
Level Shifter	-	-	-	-	yes	yes	yes
SRPG, Well-Tab	-	-	-	-	-	yes	yes

Standard Cell Design Flow



Standard Cell Structure

- **MOS Structure Capacitance**
  - $C_g = C_{ox} A = C_{ox} W L$
  - $A = W L$, The Active Gate Area
- Channel Capacitance
- Junction Capacitances



Cross section of CMOS

Standard Cell Layout

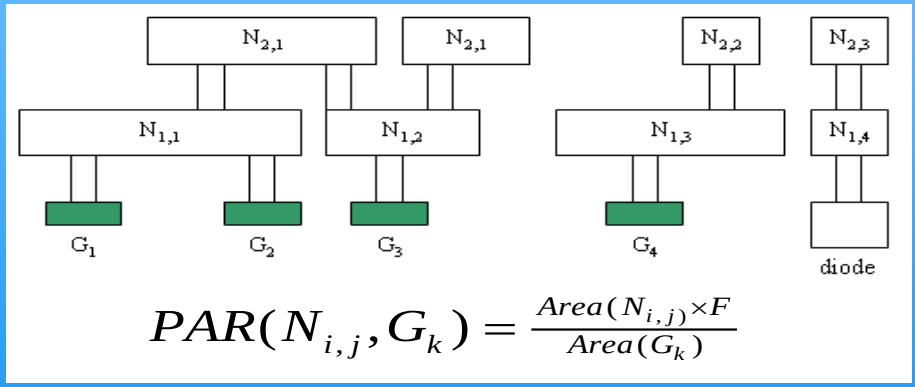
e.g. Inverter Layout

- **Combinational logic cells**
  - **INV, BUF, TR (Transmission Gate)**
  - **NAND, AND**
  - **NOR, OR**
- **Complex logic cells**
  - **AOI (AND-OR-INV)**
  - **OAI (OR-AND-INV)**
  - **AOAI (AND-OR-AND-INV)**
  - **OAOI (OR-AND-OR-INV)**
- **Sequential logic cells**
  - **Registers, F/F**

Physical Data

Layout of Other Cells (no timing info)

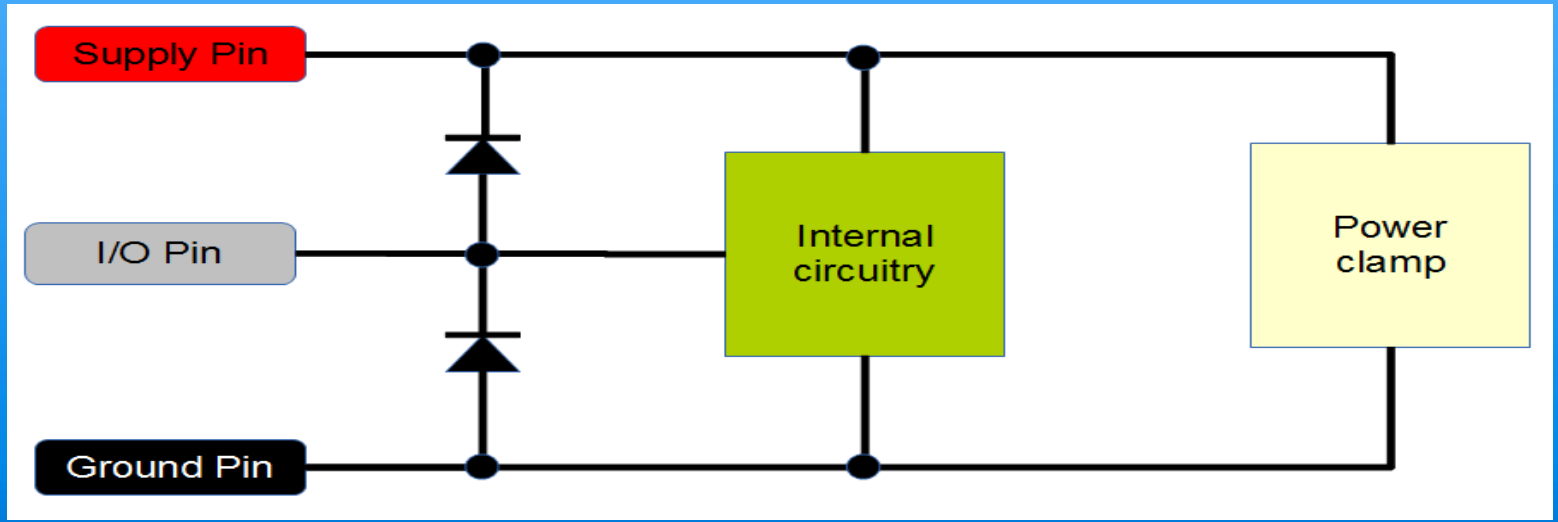
- **Antenna Cells**
  - diodes
- Corner Cells
  - contain VDD/VSS;
  - no signal pins
- Filler Cells:
  - standard core filler and I/O filler cells;
  - contain VDD/VSS, no signal pins;
  - contain substrate layers
- Cover Macro and Dummy Cells
  - Preview, Gate Array



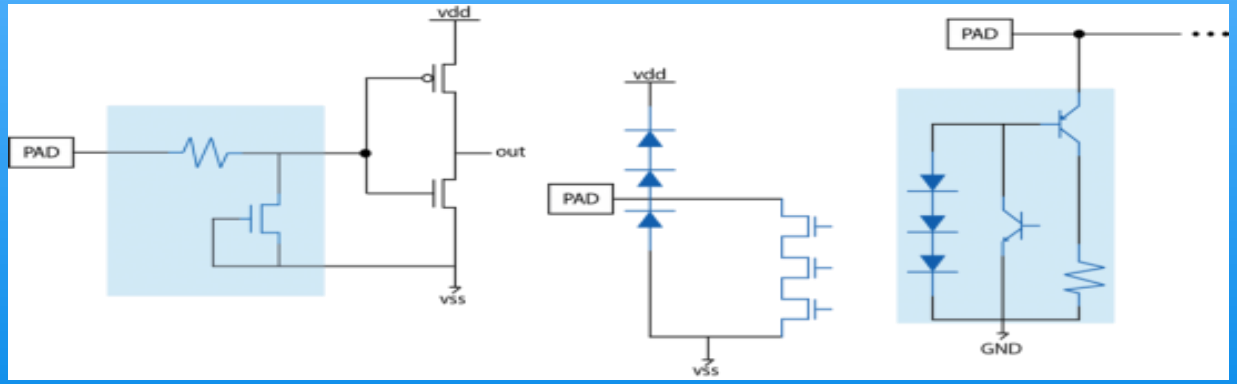
$$PAR(N_{i,j}, G_k) = \frac{Area(N_{i,j}) \times F}{Area(G_k)}$$

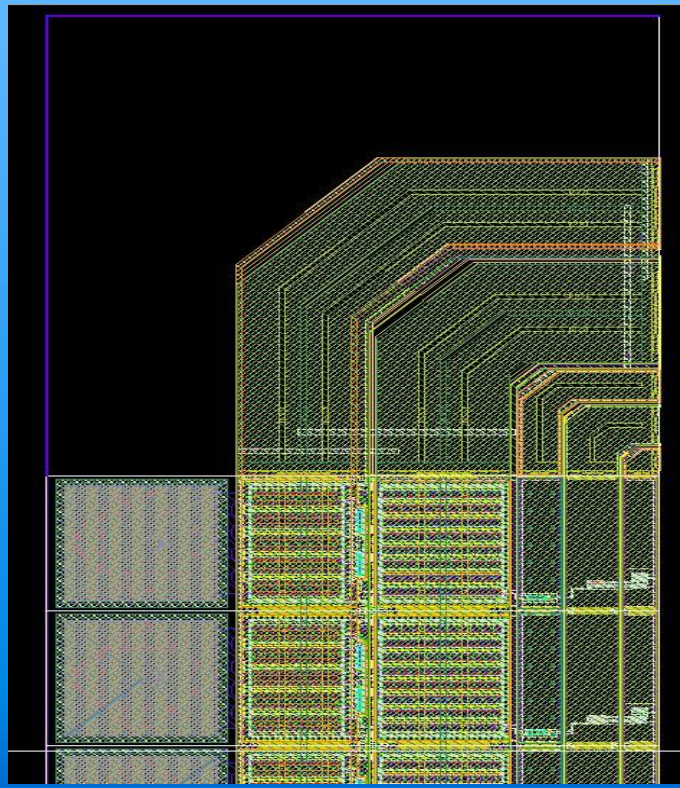
I/O Pad Design

- Type: Input, Output, In/Out (Tri-state)
- ESD Models: HBM, MM, CDM

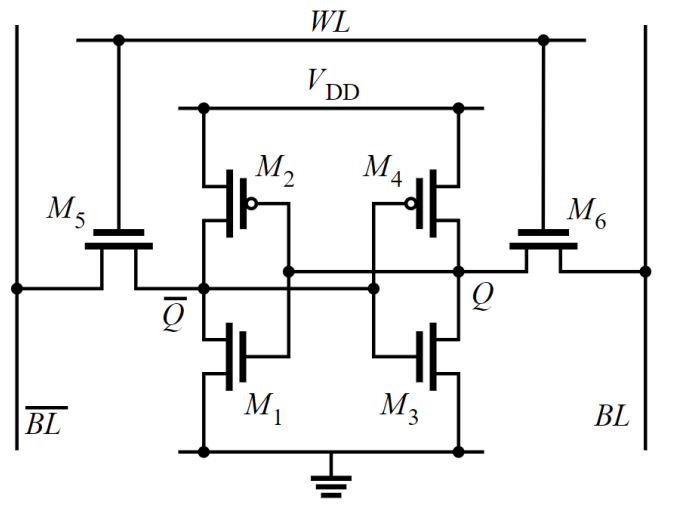


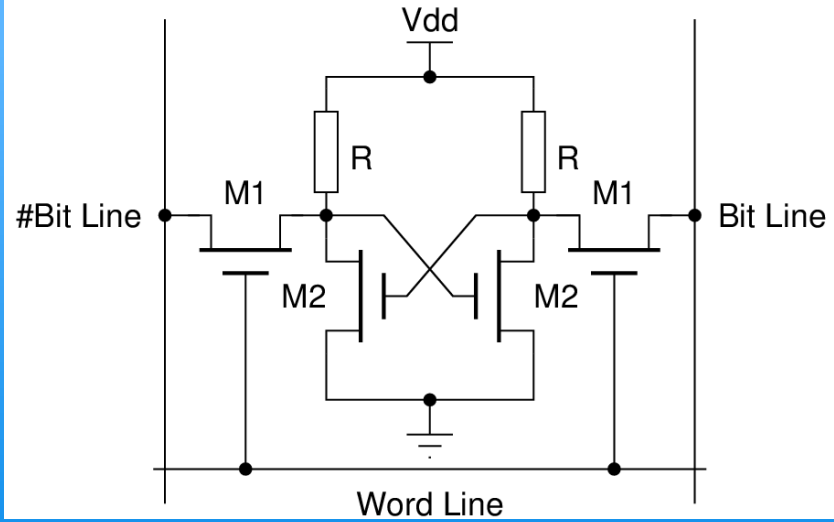
ESD Protection in I/O Pad





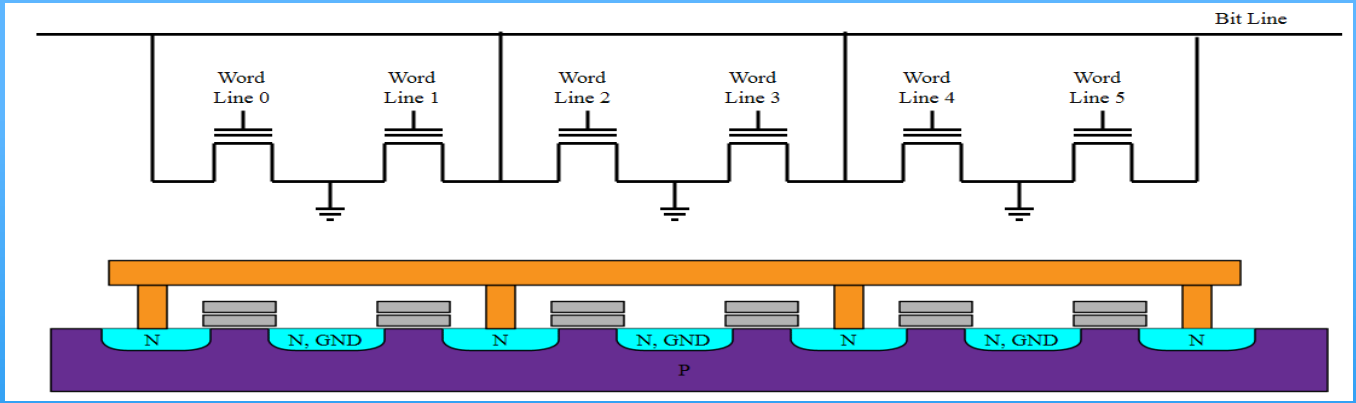
SRAM



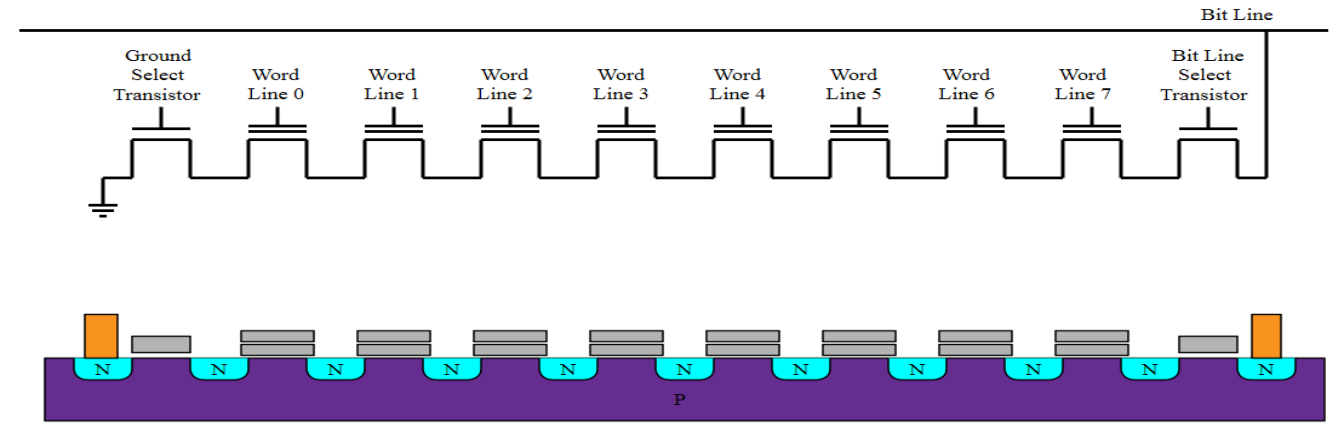


6T-SRAM and 4T+2R SRAM

Flash Structure – NOR, NAND



NOR flash memory wiring and structure on silicon

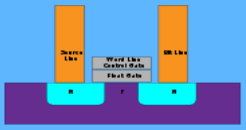


NAND flash memory wiring and structure on silicon

Memory Design - DDRx/LPDDRx

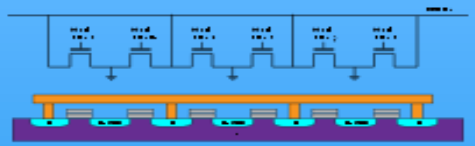
- Volatile
  - RAM: DRAM(DDR SDRAM)/SRAM
- Non-volatile
  - ROM: PROM/EPROM/EEPROM
  - NVRAM: Flash/nvSRAM/FeRAM/…
- Mobile DDR & Low Power Application
  - Hard Block vs Soft Block

Memory Design – Flash and SSD

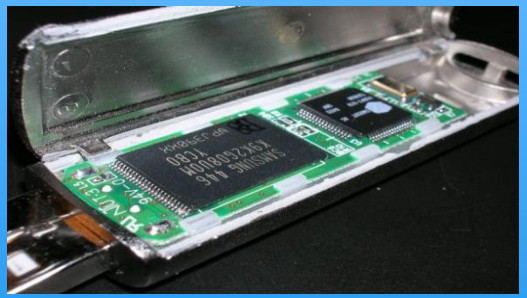


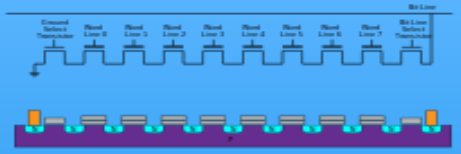
A flash memory cell

- NVRAM Flash Memory: NOR/NAND

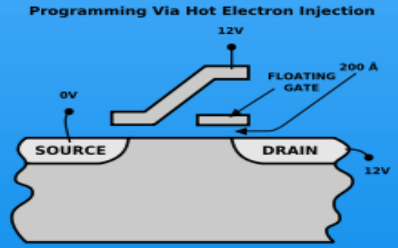


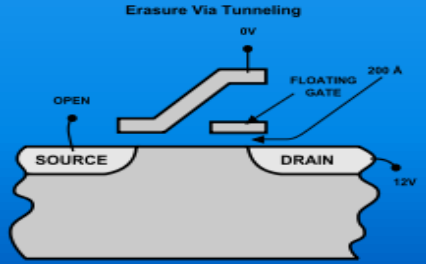
NOR flash





NAND flash





IP Design & SoC Integration

- **IP Verification & Design:** Hard IP and Soft IP
- **Common & General IPs:** Standard Cells, I/O, Memory
- **Analog IP & Digital IP:** Interface & Interconnect Bus
- **High-Speed IP:** RF and Giga-bit data
- **Discussion:** Applications

PLL, Phase-locked loop

- A control system - output signal whose phase is related to that of an input signal
- An electronic circuit consisting of a variable frequency oscillator and a phase detector
- Bringing the output signal back toward the input signal for comparison is called a feedback loop

- Variations
  - APLL, DPLL, ADPLL, SPLL, NPLL

ADC and DAC

- Concept
  - Resolution
  - Accuracy
  - Jitter
  - Sampling rate
- Types of ADC
  - SAR ADC
  - Pipeline ADC
  - Sigma-delta ADC
  - Applications
    - Medical
    - Industry control
    - Automotives
    - Communications
    - Instrumentations

Other Typical A/D

- MIPI, Mobile Industry Processor Interface (Alliance)
  - 2003: ARM, Intel, Nokia, Samsung, STM and TI
- Audio Codec
  - SW to compress/decompress digital audio data; high-fidelity
  - HW to encode/decode with ADC/DAC, e.g. used in sound cards
- AFE
  - a set of analog signal conditioning circuitry that uses sensitive analog amplifiers, often Op Amp, Filters, st ASICs
  - TI, Atmel, ADI
- PLC (Power-line communication) Chip
  - narrowband PLC (3-500kHz, up to 100 kbps, km range)
  - broadband PLC (1.8-250MHz, 100s Mbps, shorter range)

RF, EHF and mmW

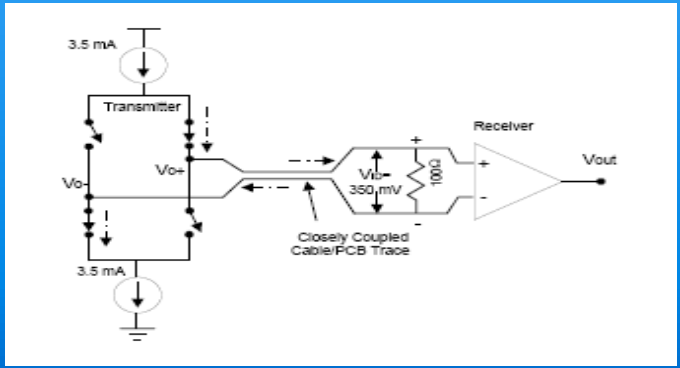
- LNA, Low noise amp.
- Mixer
- VCO
- PLL
- Bluetooth, V4.2 (2014)
  - PANs, 2.4-2.485GHz
- ZigBee
  - 0.784-2.4GHz
  - 20-250kbps, 10-100m
- NFC
  - 13.56MHz, 106-424kbps
  - card emul.,R/W; p2p
- EHF, Extremely high freq.
  - 30-300 GHz [10-1mm Wave]
  - 57-64 GHz: O_2 res./ 77 GHz
- 60 GHz/WiGig Gbps Data
  - Wi-Fi 802.11ad, V band, 7Gbps
  - 5G mobile phones
- 0.1-10 THz NDE tech

- GPS, USA, 1.57542/1.22760 GHz
- BEIDOU ,China
- IRNSS, Indian
- Galileo, European
- GLONASS, Russion

LVDS, Low-voltage differential signaling

Introduced in 1994, a tech standard: RX/TX

- it specifies electrical characteristics of a
  - differential, serial communications protocol
- low power, low V and high speed
- widely used in many areas: digital, IoT



General Purpose External Connection BUS

Full-featured USB 3.1 type-C cable wiring

Type-C plug 1		Type-C cable			Type-C plug 2	
Pin	**Name**	**Wire color**	**Name**	**Description**	**Pin**	**Name**
Shell	Shield	Braid	Shield	Cable external braid	Shell	Shield
A1, B1, A12, B12	GND	Tin-plated	GND_PWRrt1 GND_PWRrt2	Ground for power return	A1, B1, A12, B12	GND
A4, B4, A9, B9	V_{BUS}	Red	PWR_V_{BUS}1 PWR_V_{BUS}2	V_{BUS} power	A4, B4, A9, B9	V_{BUS}
B5	V_{CONN}	Yellow	PWR_V_{CONN}	V_{CONN} power	B5	V_{CONN}
A5	CC	Blue	CC	Configuration channel	A5	CC
A6	Dp1	White	UTP_Dp	Unshielded twisted pair, positive	A6	Dp1
A7	Dn1	Green	UTP_Dn	Unshielded twisted pair, negative	A7	Dn1
A8	SBU1	Red	SBU_A	Sideband use A	B8	SBU2
B8	SBU2	Black	SBU_B	Sideband Use B	A8	SBU1
A2	SSTXp1	Yellow *	SDPp1	Shielded differential pair #1, positive	B11	SSRXp1
A3	SSTXn1	Brown *	SDPn1	Shielded differential pair #1, negative	B10	SSRXn1
B11	SSRXp1	Green *	SDPp2	Shielded differential pair #2, positive	A2	SSTXp1
B10	SSRXn1	Orange *	SDPn2	Shielded differential pair #2, negative	A3	SSTXn1
B2	SSTXp2	White *	SDPp3	Shielded differential pair #3, positive	A11	SSRXp2
B3	SSTXn2	Black *	SDPn3	Shielded differential pair #3, negative	A10	SSRXn2
A11	SSRXp2	Red *	SDPp4	Shielded differential pair #4, positive	B2	SSTXp2
A10	SSRXn2	Blue *	SDPn4	Shielded differential pair #4, negative	B3	SSTXn2

** Wire colors for differential pairs are not mandated*

通用外设连接总线　　USB 2.0/3.0/3.1　　*USB Type-C (Lightning)*

I/O and Interfaces

- Logic I/O
- I2C
- GPIO
- USB, Type-C
- HTMI/DP
- RapidIO
  - Logic, Trans,
  - Physical : PHY (PCS/PMA, MII)
- PCIe
- Ethernet

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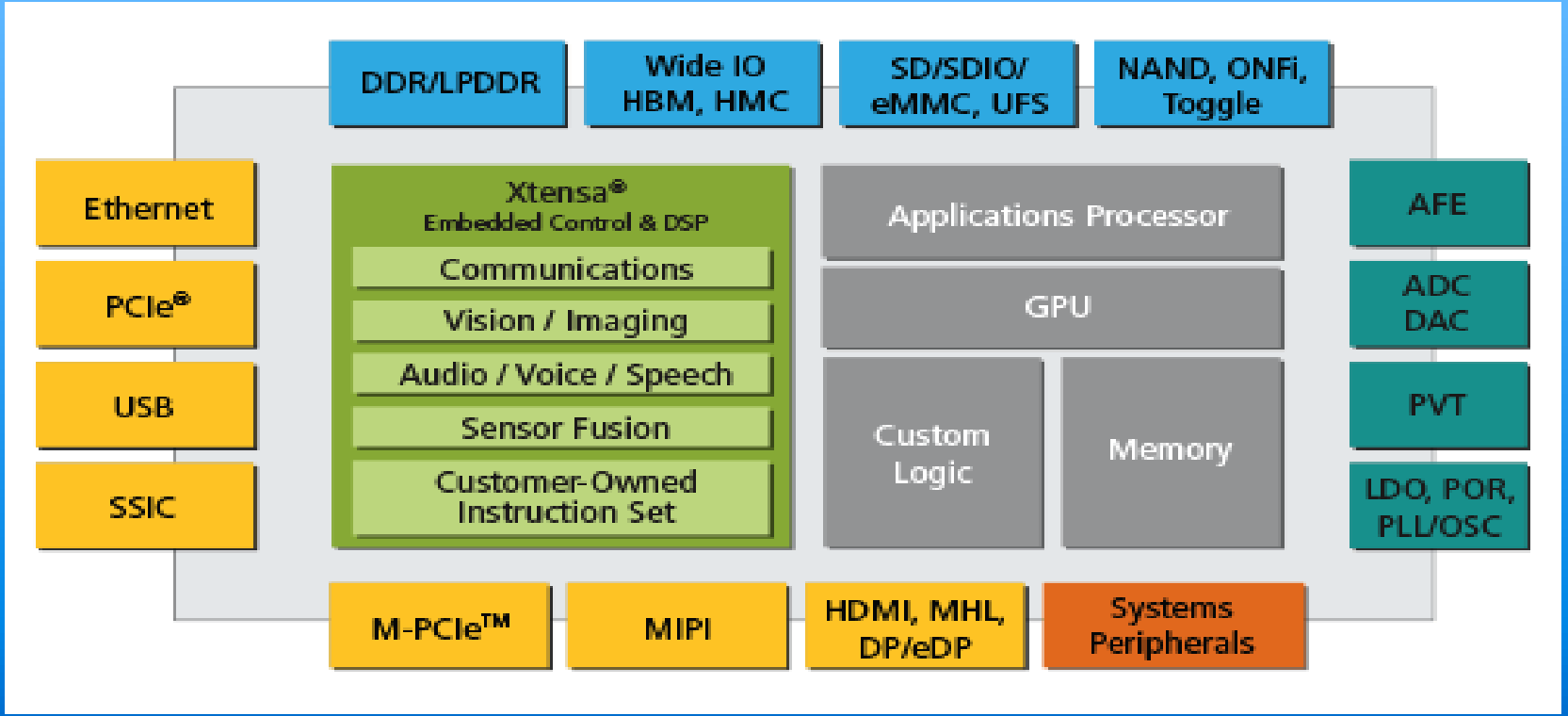
Design IP for Advanced SoC

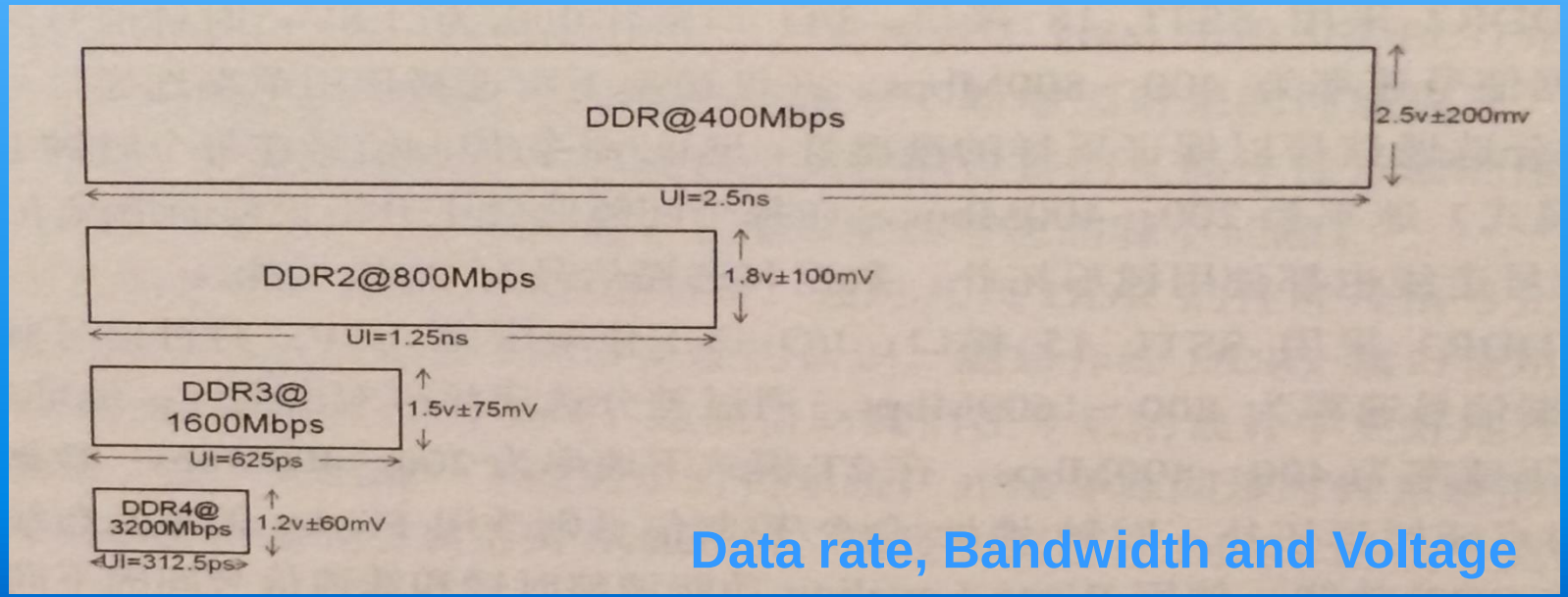


High-Speed IP Technology

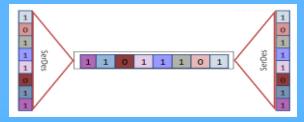
- 6Gb/s SATA
  - SATA 1.0: 1.5Gb/s, 150MB/s
  - SATA 2.0: 3Gb/s, 300MB/s
  - SATA 3.0: 6Gb/s, 600MB/s
  - SATA 3.1
  - SATA 3.2: 16Gb/s, 1969MB/s
- 10GbE
  - IEEE 802.3ae-2002
- Optical fiber over SONET/SDH
- Ethernet family of LAN tech
  - 10Mb/s, 100Mb/s,
  - 1Gb/s, 10Gb/s
  - 25Gb/s, 40 & 100Gb/s
  - 400Gb/s & 1Tb/s

High-Speed DDRx BUS

- DDR = DDR SDRAM
- DDR1, DDR2, LPDDR2, DDR3, LPDDR3, DDR4

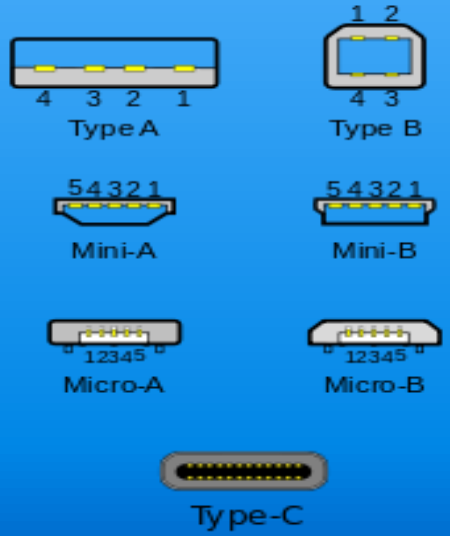


SerDes and USB



- 4 Architectures
  - Parallel clock SerDes
  - Embedded clock SerDes
  - 8b/10b SerDes
  - Bit interleaved SerDes
- Key Parameters
  - Inputs and Outputs
  - Rates and Test functions
  - Clock functions
  - Power, temperature

- Reliability
- USB 1.x/2.0/3.0/3.1
- USB Type-C

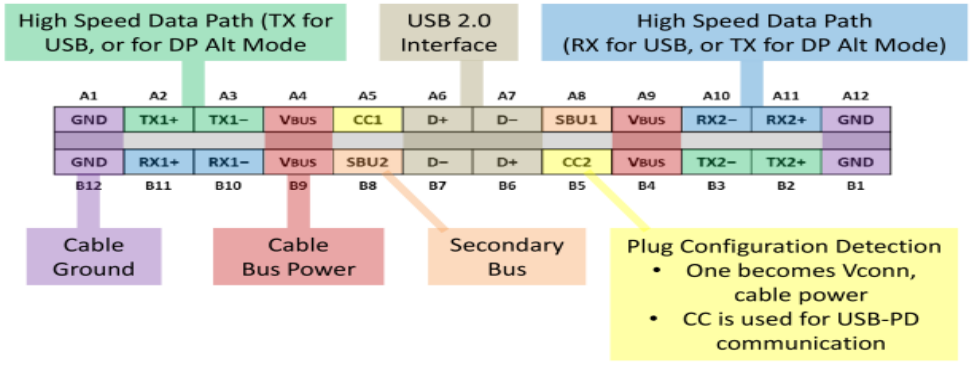


USB Type-C

- 24 pin, Spec 1.0, Aug. 2014
- replacing various Type-B and Type-A connectors …
- True Plug'n Play; 10 Gbps, up to 100W!

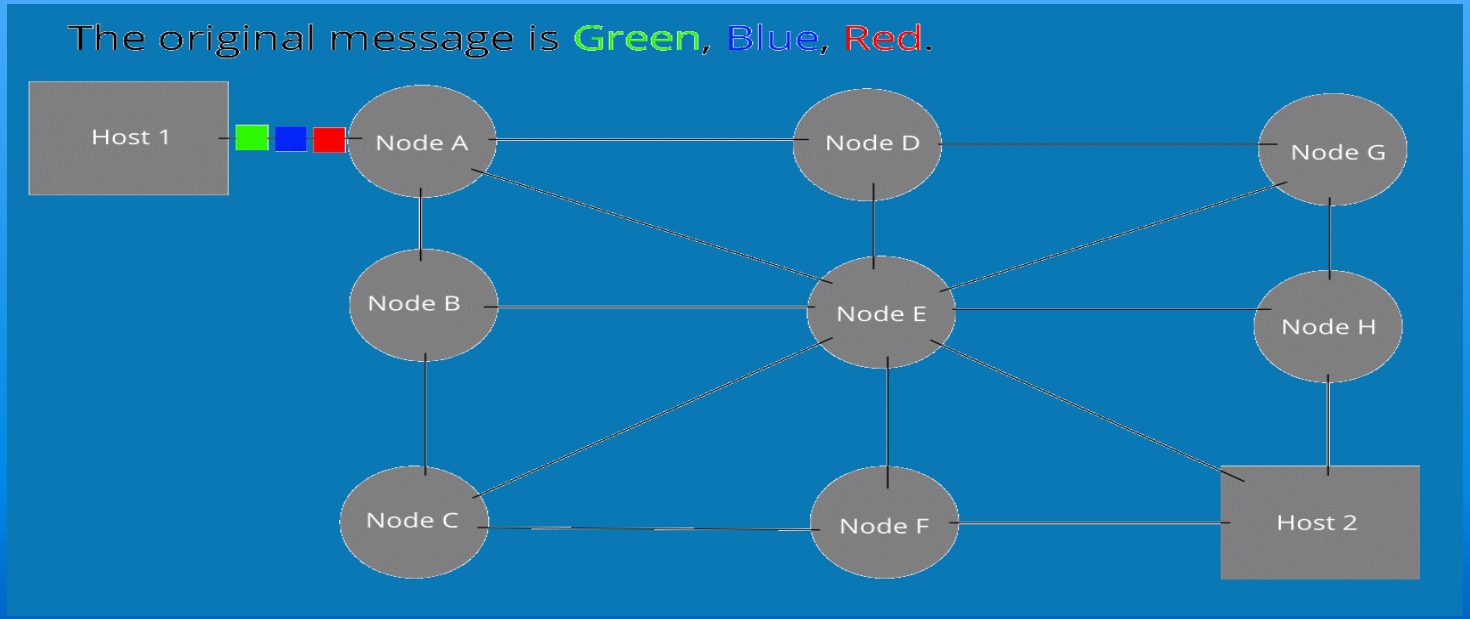
USB Type-C Receptacle Pins

Pins defined for system or device receptacle



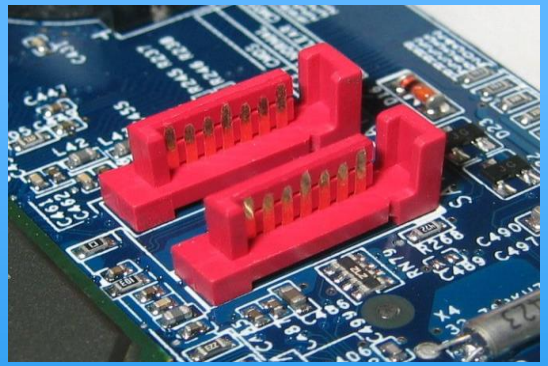
RapidIO

- SerDes and PCS
- DDRx

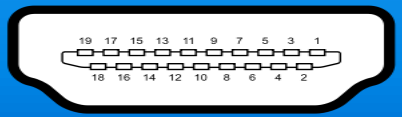


Interface IPs

- SATA
  - 1.0/2.0/3.0
- PCIe
  - 1.0a/1.1/2.0/2.1
  - 3.x/4.0



- HDMI
  - 1.0-1.2/1.3/1.4/2.0
- DP by VESA
  - 1.0-1.1/1.2/1.3
  - VGA, DVI,
  - FPD-Link

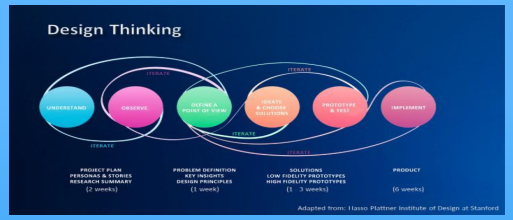


IP Design & SoC Integration

- **IP Verification & Design:** Hard IP and Soft IP
- **Common & General IPs:** Standard Cells, I/O, Memory
- **Analog IP & Digital IP:** Interface & Interconnect Bus
- **High-Speed IP:** RF and Giga-bit data
- **Discussion:** Applications

IP Design and Silicon Proven

- **Design IP**
  - IP Design Houses
  - EDA Vendors
- **Verification IP**
  - EDA Vendors
  - Self Development
- **Soft IP and Hard IP**
  - ARM
  - Distributors
- **Silicon Proven IP**
  - T.O. and Tested
  - Many Adoptions



Summary and Discussion

- Advantages/disadvantages btw/ Hard/Soft IP
- Standard IP – types of
- Analog/Digital IP – to buy or to design?
- RF/High-Speed, which one is harder to design?
- SoC and IP Design Integration