University of Chinese Academy of Sciences

Impact of Big Data on SoC Design

CPU Architecture in SoC Design

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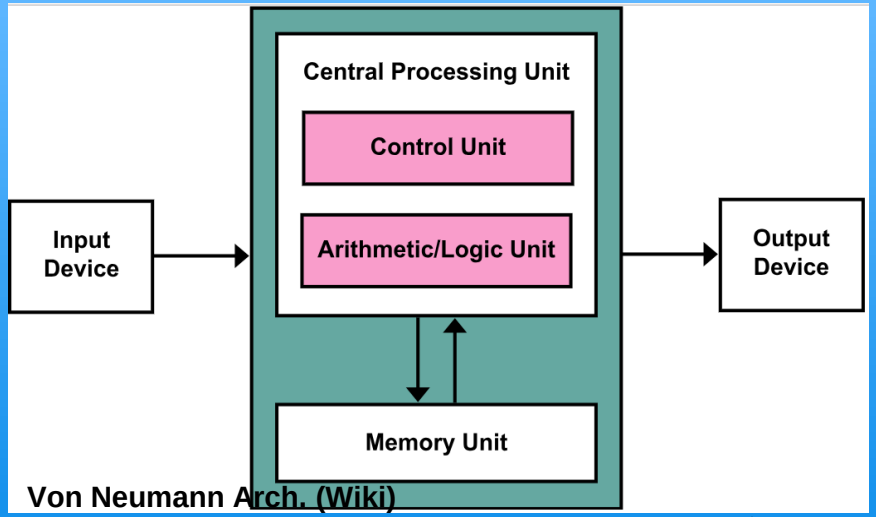
CPU Architecture in SoC Design

University of Chinese Academy of Sciences

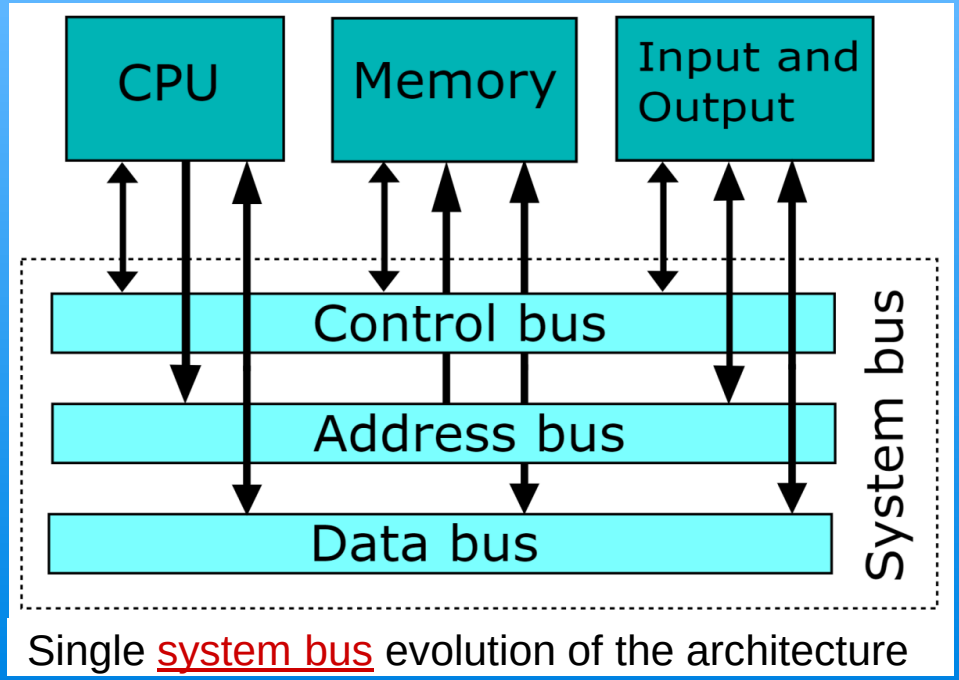
- **CPU and ISA**
- CPU in Servers & PCs
- CPU in HPC (AI-Big Data) & Mobiles
- OS and Co-Design of HW/SW
- Discussion

Von Neumann Architecture & Its Improvement



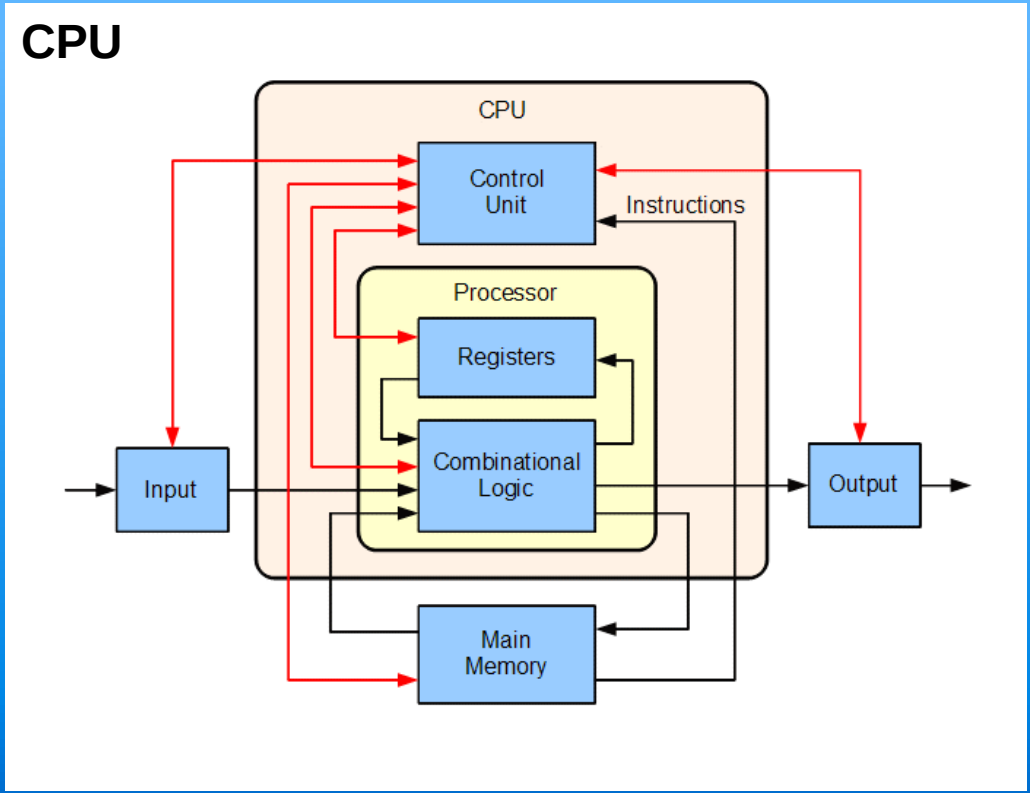
Von Neumann Arch. (Wiki)

Original Von Neumann Arch
is developed to
Single System Bus Arch



Single system bus evolution of the architecture

Central Processor Unit & Its Variants



CPU
Central Processing Unit

MCU
Microcontroller Unit

MPU
Microprocessor Unit

DSP
Digital Signal Processor

Various CPU Architectures

- CISC, RISC, RISC-V
  - CSIC (Complex Instruction Set Computer)
  - RISC (Reduced Instruction Set Computer)
- CISC: x86 and IA-64
- RISC:
  - POWER/ PowerPC
  - MIPS
  - UltraSPARC
  - ARM
  - Other CPUs

19th C.: "difference engine" by Babbage, read, store, calculate, output
1943-45, Colossus Computer, ele.+mech. Alan Turing cryptanalysis → Enigma
ENIAC (1946-1955), by J Mauchly & J Eckert 18000 tubes, 140 kW, 30t… (U Penn)
1952, von Neumann joined on EDVAC
1953, IBM 701
1957, DEC PDP-1
1964, IBM-360

List of Architectures and a Comparison

- X86/ IA-64
- POWER/ PowerPC
- MIPS
- ARM
- UltraSPARC
- C-SKY/ Loongson, PKU, VIA, Shuguang (*Sugon*), …

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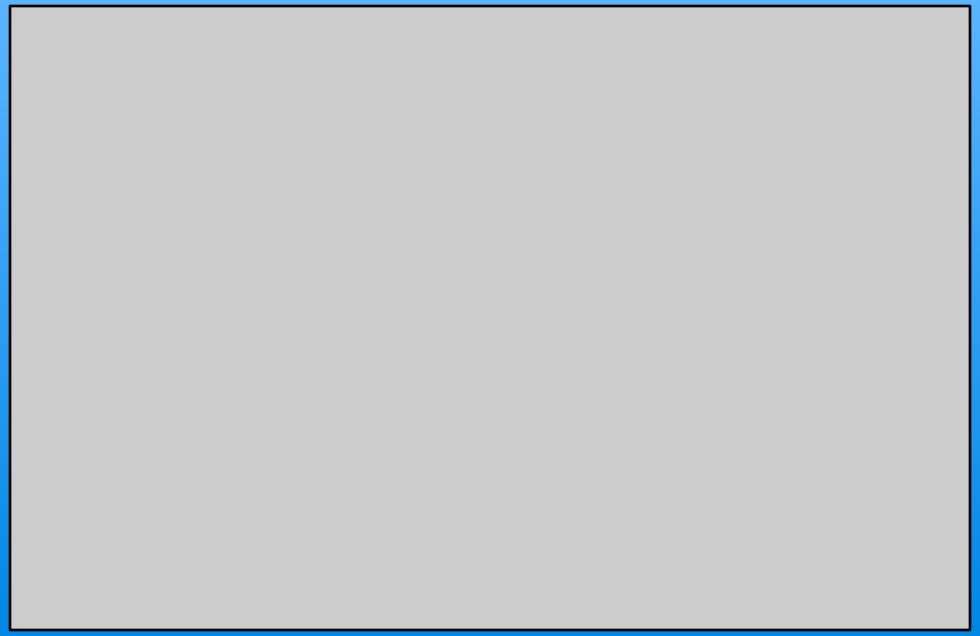
Intel’s x86

- 8086
- IA-64 (EPIC)

Components in System-on-Chip

- CPU
- Memory
- I/O (of SoC)
- Logic & IP



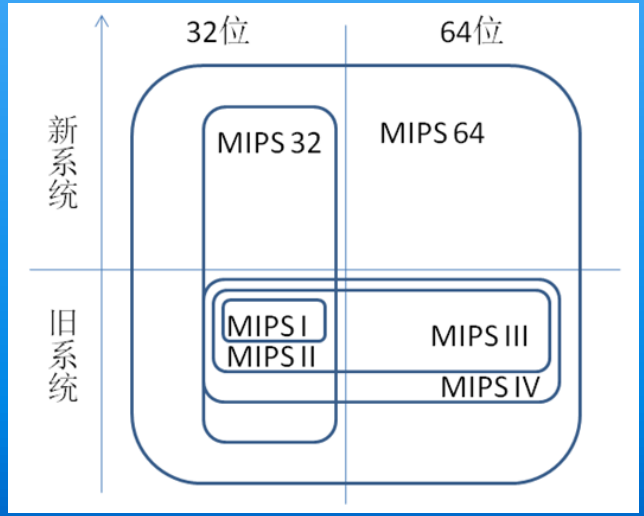
IBM’s POWER

- POWER
  - RS/6000 (CISC)
  - POWER, PowerPC, Power ISAs
- PowerPC

- AIM Alliance
- Power.org

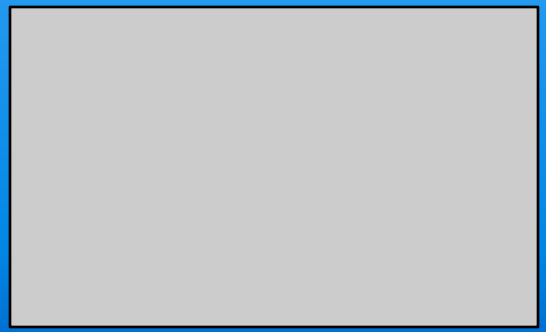
MIPS

- 1984, MIPS estab. John Hennessy
- 1992, SGI (Silicon Graphics Inc.) merger
- 1998, MIPS IPO, spun off from SGI
- 2013, Imagination
- 2017, Tallwood
- 2018, Wave Computing



*Architecture of Microprocessor

- Tested with VHDL Simulation
- Random Logic Architecture (MSPARC)
- Micro-code, Pipelined Structure and Conflicts
- Cache
- Virtual Memory
- Superscalar



ARM

- Architecture
  - Armv7-A/R/M
  - Armv8-A/R/M
- BUS
  - AMBA/2/3/4/5
  - ASB,APB;
  - AHB;
  - AXI,ATB;
  - AXI4,ACE;
  - CHI

架构名称	技术特征	应用场合	处理器案例
Armv7-A	A32(32b), T32(32b,16b混合)	(1~4)多核设计	Cortex-A5/A7/A9/A15/A17 (A8: 单核)
Armv7-R	32b	高新能应用	Cortex-R4/R5/R7
Armv7-M	32b	低功耗场合	Cortex-M0/M0+/M3/M4/M7
Armv8-A	32b/64b	Smartphones	Cortex-A53/A57/A72
Armv8-R	32b	MMU，MPU	Cortex-R 系列
Armv8-M	32b (16b)	MCU/IoT	Cortex-M0/M0+/M3/M4/M7/M

发布年代	版本	新增总线/接口	英文全名	应用举例
1996	AMBA	ASB, APB	Advanced System Bus, and Advanced Peripheral Bus	
1999	AMBA2	AHB	High-performance Bus	A7, A9, Cortex-M系列
2003	AMBA3	AXI, ATB	Advanced Extensible Interface, Advanced Trace Bus	Cortex-A 系列, 包括 Cortex-A9
2010/11	AMBA4	AXI4, ACE	Advanced Extensible Interface 4, AXI Coherency Extensions	Cortex-A 系列, 包括 Cortex-A7/15
2013	AMBA5	CHI	Coherent Hub Interface	支持(验证)VIP, SystemVerilog语言等

Server CPUs

- Server and CPU Providers in C20
  - SUN/ Solaris, IBM/ AIX, HP/
  - UNIX
- Server and CPU Providers in C21
  - Linux/Inter, IBM/POWER
  - Linux

Multi-thread multi-CPU

Computer Farm and Supercomputer

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Summit (supercomputer) by IBM

- Summit at ORNL
  - June 8, 2018 at ORNL
  - Clock: 200 *PFLOPS*
  - 9216 *POWER9* 22-core CPUs
  - 27,648 Nvidia *Tesla V100* GPUs
  - Power: 15 MW
  - Storage: 250 PB
  - Purpose: Sci. Research

- Design
  - Each node: >500GB coherent HBM, plus DDR4
  - 800GB of NVRAM
  - Nvidia's *NVLink*
  - *HSA* model

- *Blue Gene*

Blue Gene by IBM

- Blue Gene at ORNL
  - Blue Gene/L, /P, /Q
  - All nodes on 1 SoC (except ext. DRAM of 512 MB)
  - 2009 Nat Medal Tech & Inno
  - *Ended on 2015?*
- History
  - 1999, $100M, 5-yr (at T.J. Watson Res. Ctr.)
  - Parallel computing for study of protein folding
- 2004: 70.72 TFLOPS (16-rack x 1024 compute nodes)
- 2004-2007 at LLNL (104-rack) 478 TFLOPS

- *Also see Summit*

Systems and Operating Systems by IBM

- Systems
  - System I, System p, Power Systems servers, & BlueGene
  - Power Mac, iBook, eMac…
  - GameCube, Wii, Xbox 360…
- OS
  - Linux
    - Red Hat, SUSE, Ubuntu
  - AIX (Unix)
  - IBM i, …
- Other OS
  - Linux from various vendors
  - FreeBSD
- Historical OS
  - Mac OS from Apple
  - OpenSolaris from Sun
  - Windows NT from MS (till W2k)
  - *HP-UX (Unix)*
- *iOS, Android*

Types of System Bus in SoC Design

- **CoreConnect Bus** (IBM for PowerPC)
  - No-fee, no-royalty, used by >1500 companies
- **AMBA Bus** (1996, Arm)
  - 1996 AMBA1 (ASB/APB);1999 AMBA2 (AHB);2003 AMBA3 (AXI/ATB);
  - 2010-2011 AMBA4 (AXI4, ACE); 2013 AMBA 5 (CHI)
- **Wishbone Bus** (Open Source, OpenCores)
  - Defines 8, 16, 32, 64-bit Bus
- **OCP (Open Core Protocol) Bus**
  - Neither Altera nor Xilinx supports this protocol

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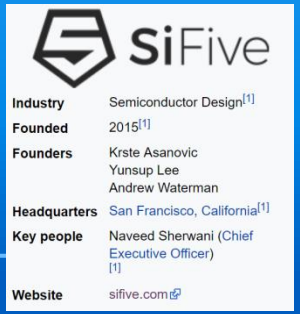
OS

- Unix
- Linux

- iOS
- Android

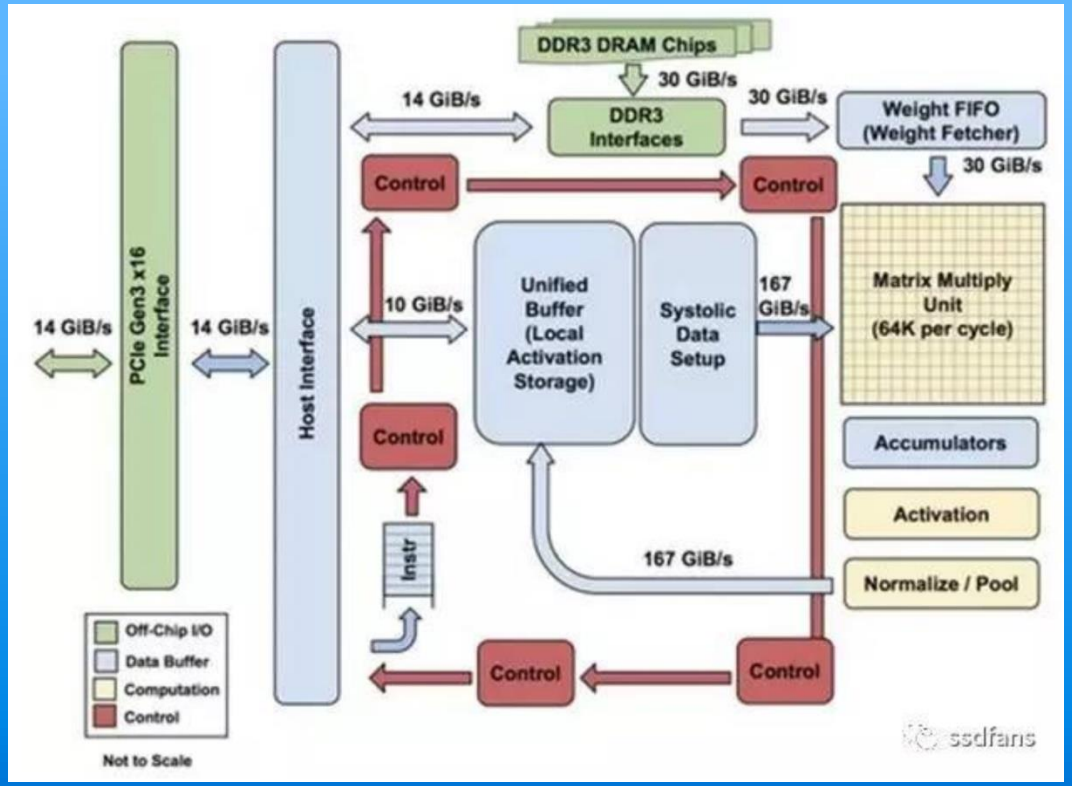
RISC-V

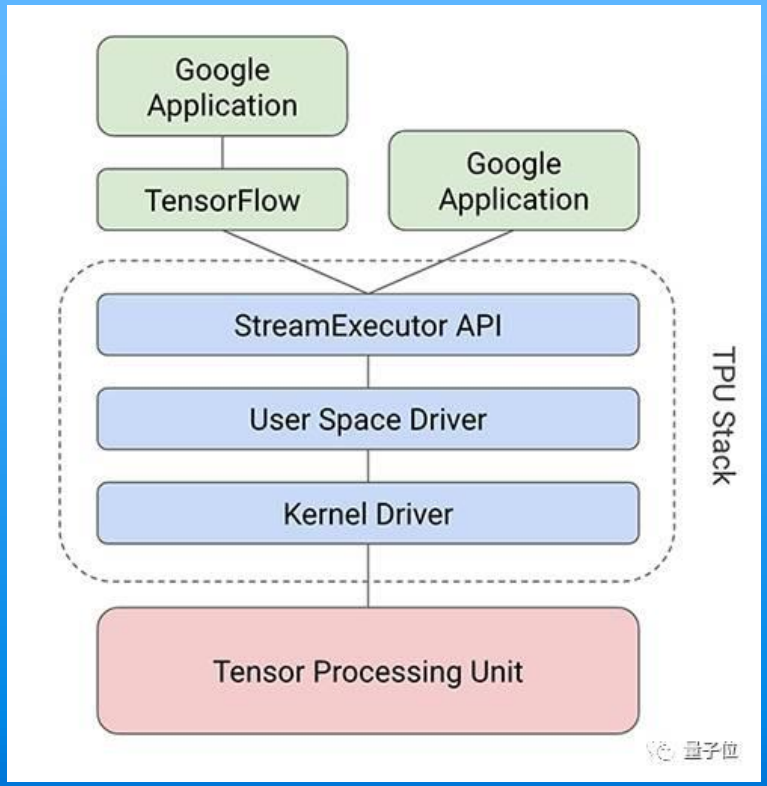
- An Open ISA: 32b, 64b,128b; v2.2/2017 (2010- , UCB)
  - Prof Krste Asanovic (UCB), Martin Fink (WD);
  - RISC-I, -II, -III aka SOAR, -IV aka SPUR, -V aka Raven-1
  - 28nm FDSOI 2011
- A partial list of orgs. support the RISC-V Foundation:
  - AMD, HP, Huawei, IBM, Nvidia, NXP, QCOM, WD, SiFive …
- SiFive (2015-), 2017 First SoC/RISC-V/64b



RISC-V

TPU Architecture and the TensorFlow





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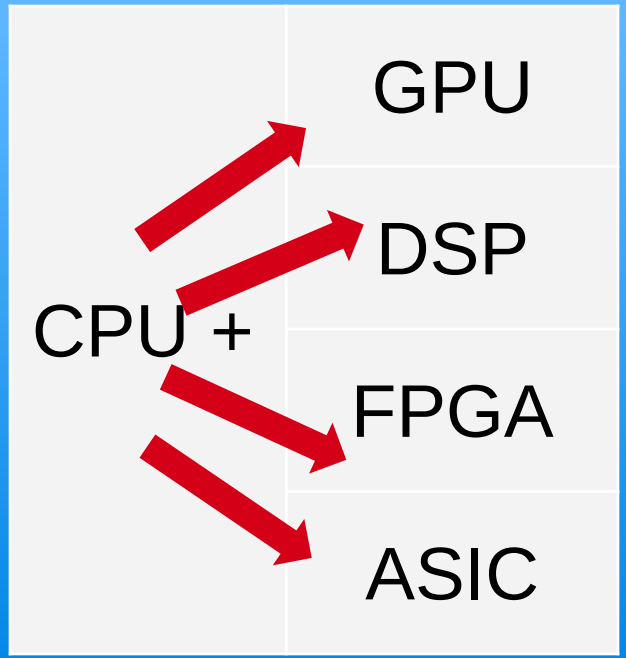
AI-Chip and HSA

- CPU + GPU
  - GPU by Nvidia (GeForce), AMD, Intel, ARM etc
  - SW: CUDA (Nvidia), OpenVX (Intel), OpenCL
- CPU+ DSP
  - DSP from Cadence; SW/OS
- CPU+FPGA
  - eFPGA, reconfig FPGA, FPGA/ASIC
- CPU+ASIC
  - Customized ASIC



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    - Sixth Edition, 2017

Summary

- Turing 2017, John Hennessy & David Patterson
  - https://mp.weixin.qq.com/s/xLDKSgRmPcJ-eHRxF9b_SA