University of Chinese Academy of Sciences

Verification & Implementation of SoC Design

DFT and LEC

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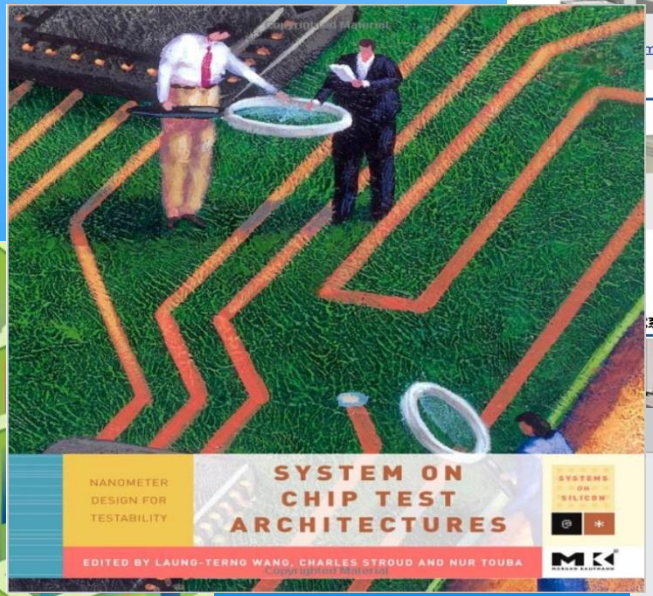
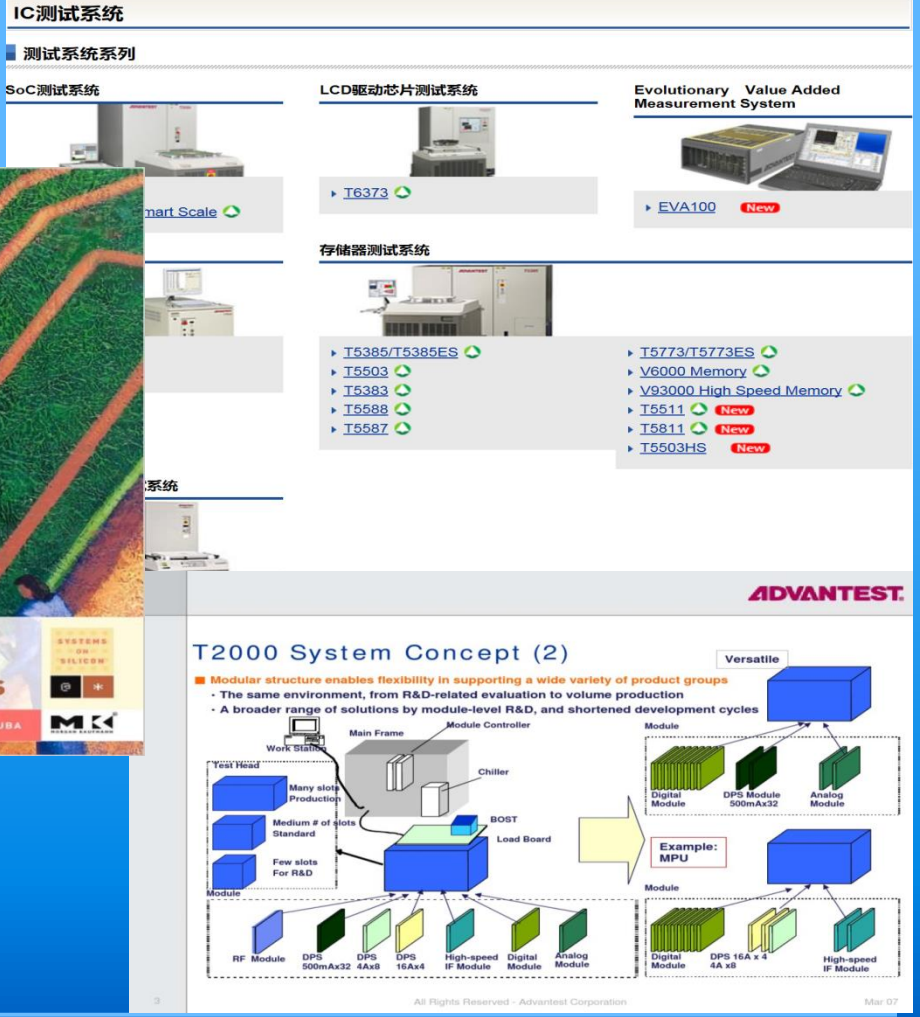
Product Chain of SoC Design

- **Background of DFT**
- **Scan Chain and Scan Insertion**
- **BIST and ATPG/ MBIST**
- **Formal (Conformal) and LEC**
- **Discussion**

DFT and ATE


NANOMETER DESIGN FOR TESTABILITY
SYSTEM ON CHIP TEST ARCHITECTURES
EDITED BY LAUNG-TERNG WANG, CHARLES STROUD AND NUR TOUBA


DESIGN FOR TESTABILITY
VLSI TEST PRINCIPLES AND ARCHITECTURES
Edited by: LAUNG-TERNG WANG CHENG-WEN WU XIAOQING WEN


IC测试系统
测试系统系列
SoC测试系统
LCD驱动芯片测试系统
Evolutionary Value Added Measurement System
T6373
EVA100 New
存储器测试系统
T5385/T5385ES
T5503
T5383
T5588
T5587
T5773/T5773ES
V6000 Memory
V93000 High Speed Memory
T5511 New
T5811 New
T5503HS New
ADVANTEST
T2000 System Concept (2)
Modular structure enables flexibility in supporting a wide variety of product groups
· The same environment, from R&D-related evaluation to volume production
· A broader range of solutions by module-level R&D, and shortened development cycles
Versatile
Example: MPU
All Rights Reserved - Advantest Corporation
Mar 07

Design For Test Introduction

- Testing is an experiment to determine if something works correctly. The system is exercised and the response is analyzed to find out whether the system behaves correctly.
- Incorrect behavior of digital designs can be caused by the following:
  - Incorrect specification or incorrect design
    - Functional defect => logical fault => faulty behavior
    - Can be detected by functional testing/verification
  - The device is built improperly
    - Manufacturing defect => physical fault => faulty behavior
    - Can be detected by manufacturing test patterns

Fault Modeling

- Physical defects are modeled as logical or timing failures. Fault models are used as an abstract of the physical defect. They have the following benefits
  - Fault models allow mathematical treatment
  - They reduce the complexity of the test problem
  - One fault model can represent several physical defects
  - Using fault models, faults can be enumerated
  - Most faults models are technology independent
  - Stuck-at is the most prevalent fault model

Controllability and Observability

- To test for stuck-at faults, the fault needs to be activated and the effect needs to be observed.
  - to activate a "*s-a-0/s-a-1*" fault, a logical 1/0 value needs to be generated at the node to be tested
  - to observe a fault, the logical difference between faulty and good circuit needs to be observed (also called Boolean difference)
- Controllability is the ability to establish logical values at specific nodes
- Observability is the ability to observe logical values at specific nodes

DFT and Design for Reliability

- Fault Coverage Driven
  - *Reliability in relation to Yield and Testing Coverage*
  - Emphasize the importance of “Y-T” relationship
  - Controlled/Alleviated RMA Task
- Engage DFT at Early Stage, Combining DFY Tactics
- Guided with Defect Level, DL

$$DL = 1 - Y^{(1-T)}$$

DL: probability of shipping a defect chip,

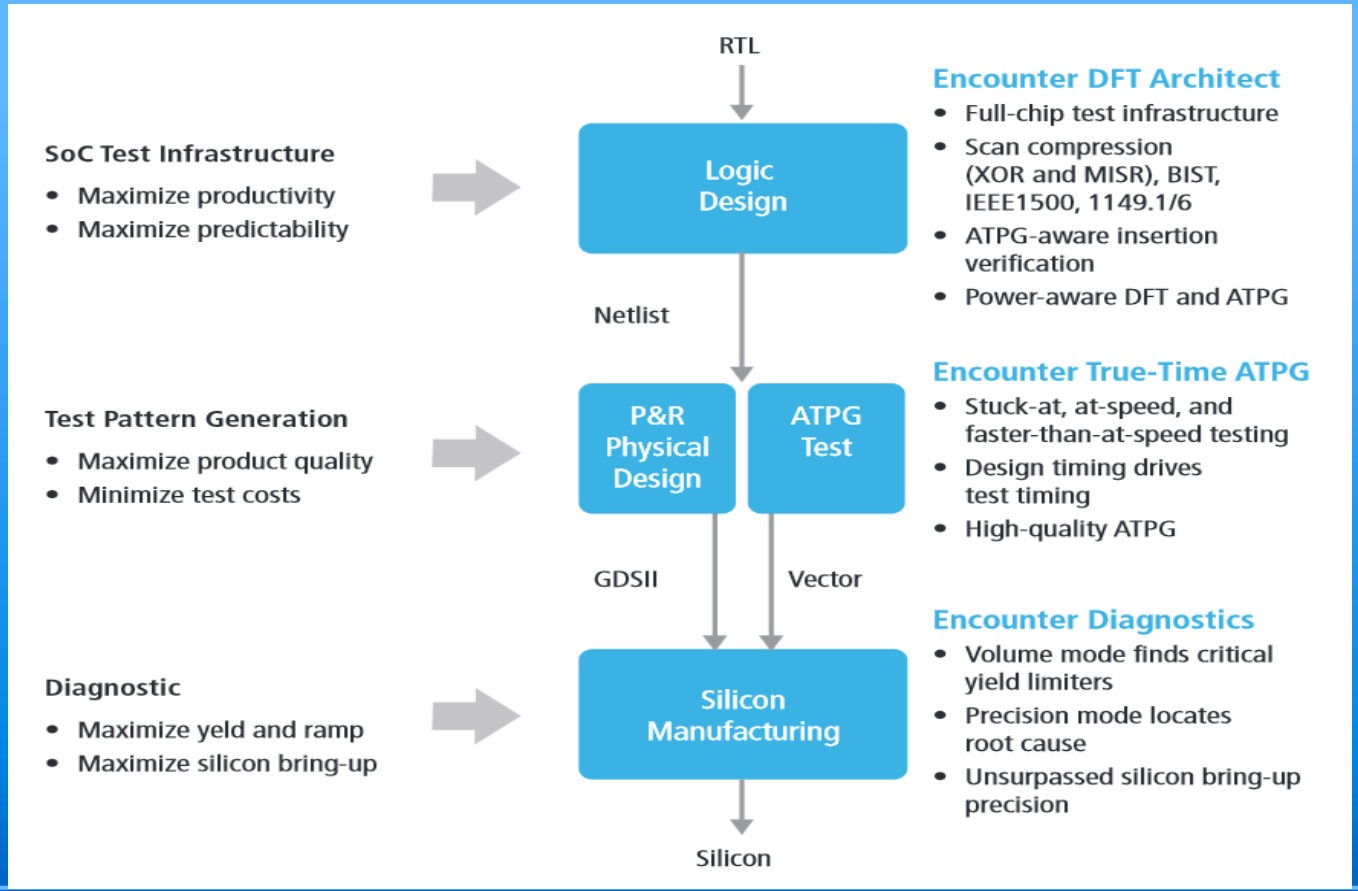
Y, yield, T: test (fault/defect) coverage

Ex. Y=96%, T=98% → 500ppm

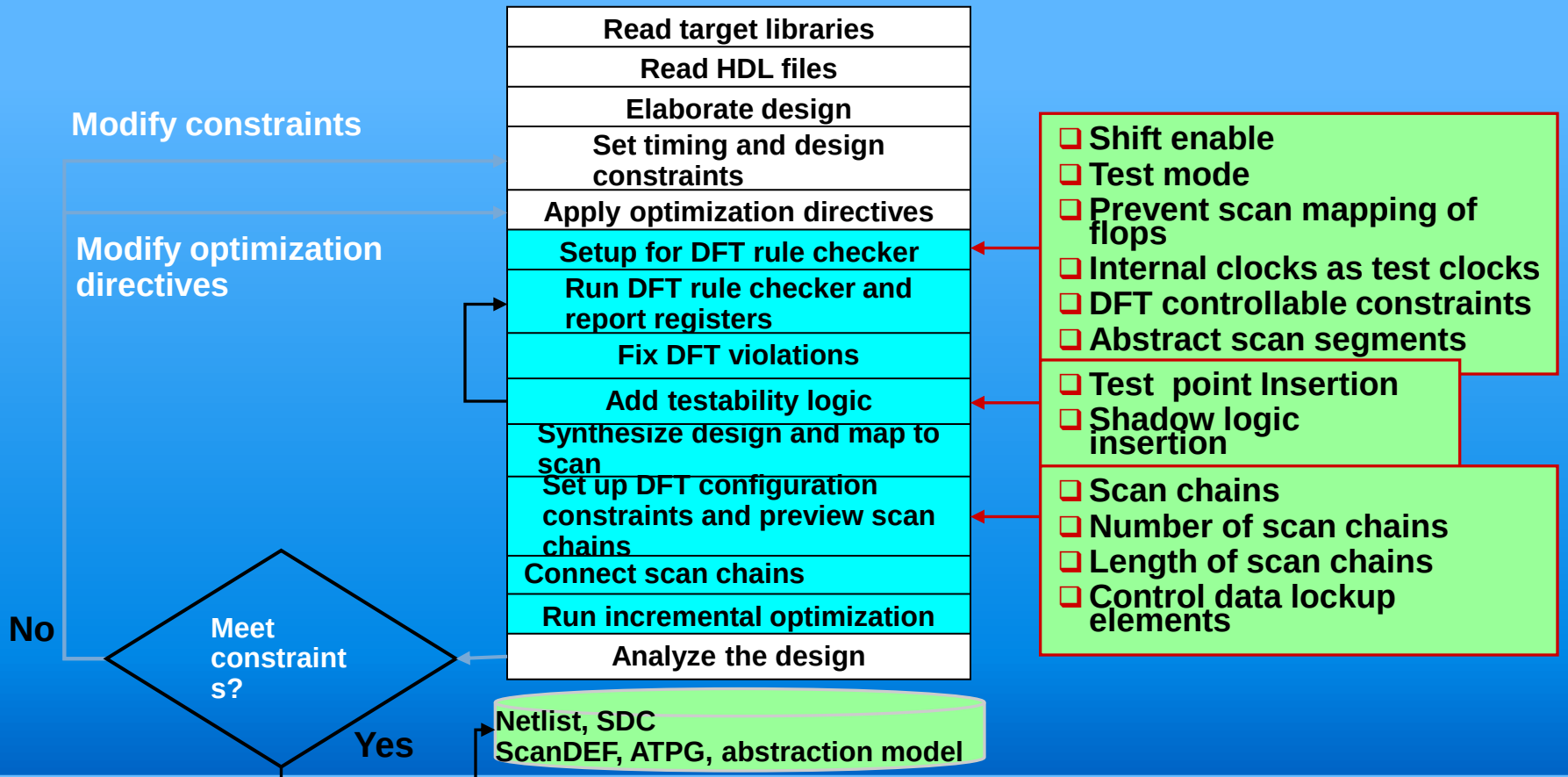
(→ < 500/200/100/10ppm)

- ** In-House Technology on “DFT+Test”*

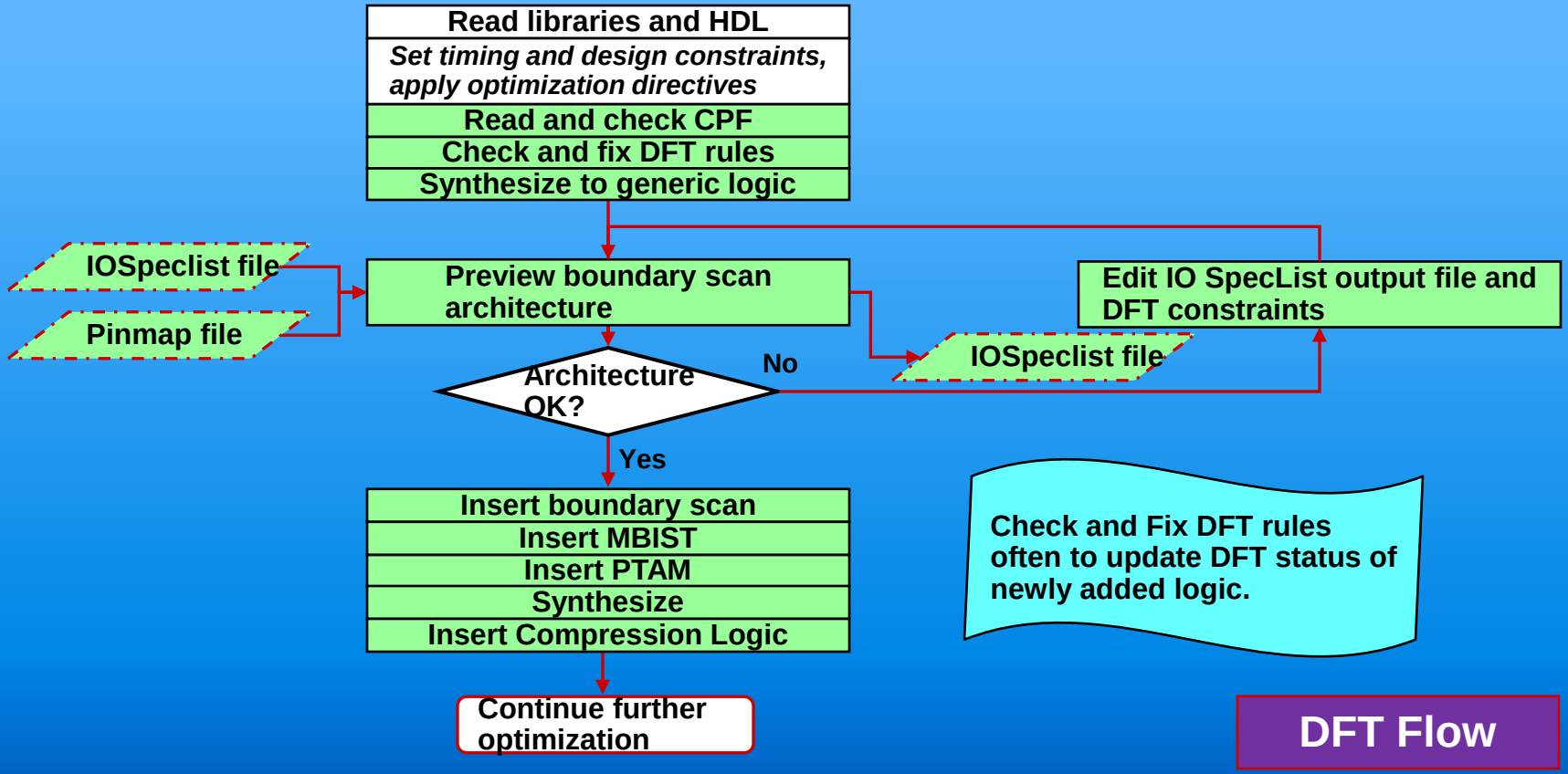
Complete DFT Solution for RTL-to-Silicon



RTL Top-down Design-for-Testability (DFT) Flow



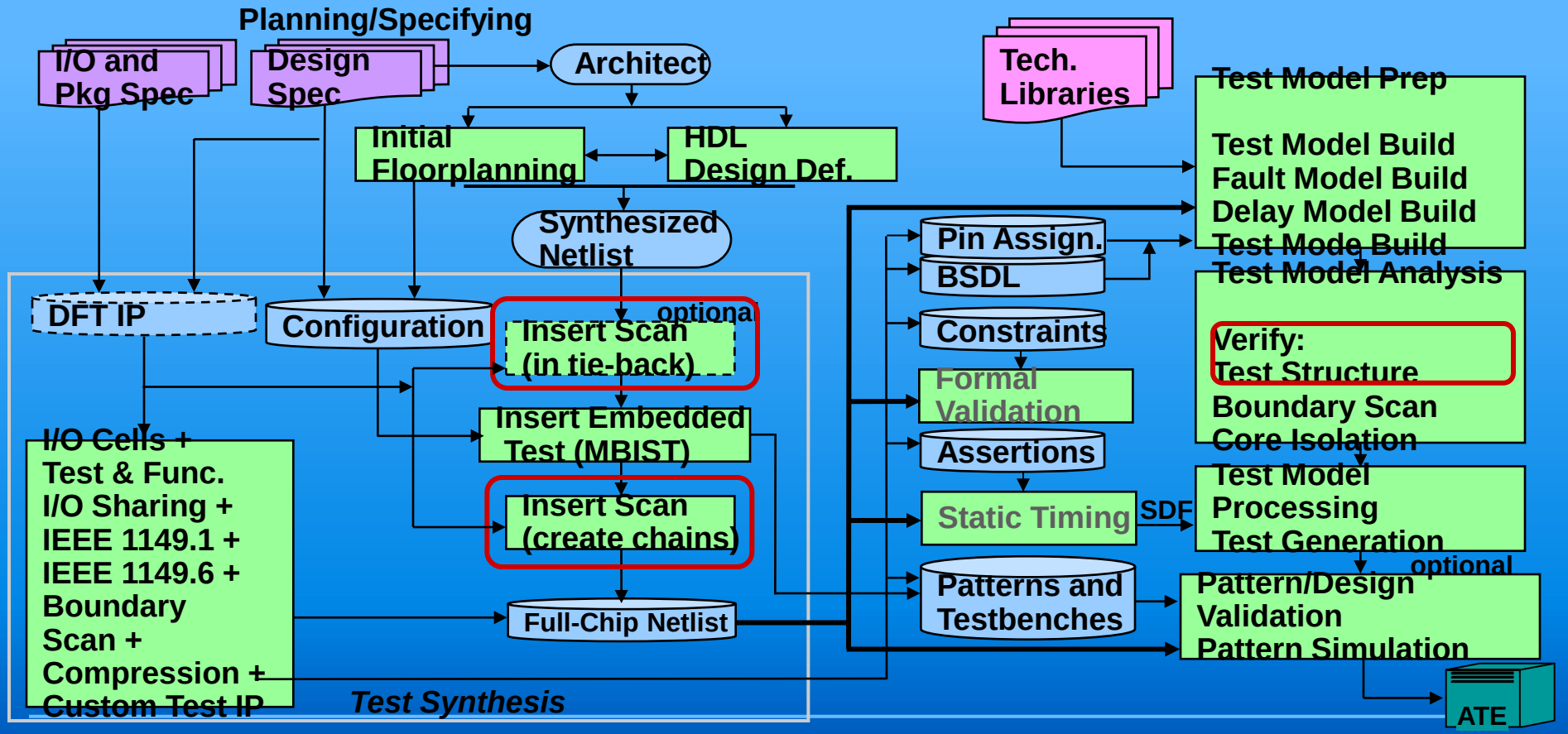
Advanced Design For Test Synthesis



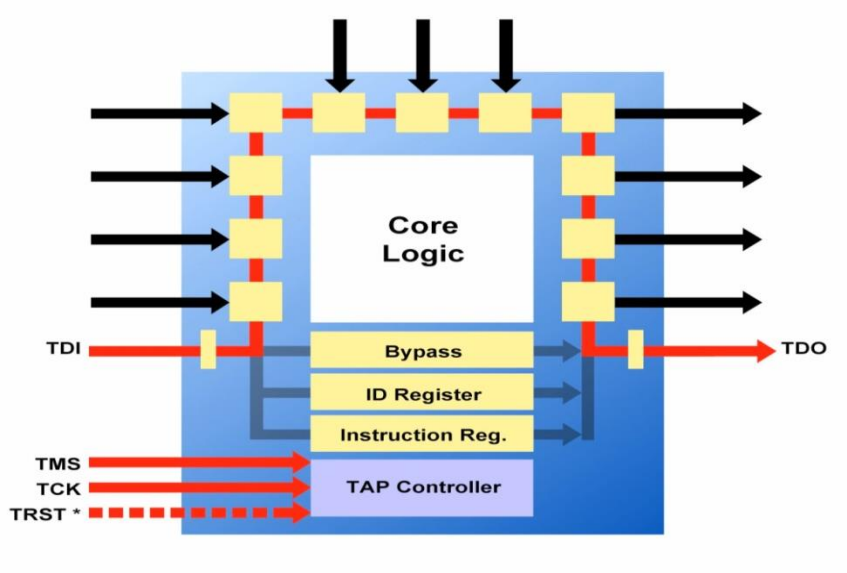
DFT & DFY

- Background of DFT
- Scan Chain and Scan Insertion
- BIST and ATPG
- Compression/Diagnosis & ATE
- Discussion

Encounter Test Synthesis Flow

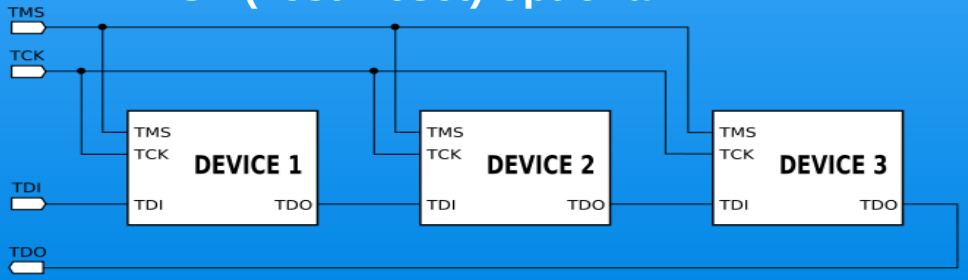


BSD and JTAG Illustrated



Daisy-chained JTAG (IEEE 1149.1)

TDI (Test Data In)
TDO (Test Data Out)
TCK (Test Clock)
TMS (Test Mode Select)
TRST (Test Reset) optional



Scan for Digital Design

- Scan Types
  - Internal Scan (Scan Chain)
  - Boundary Scan *Description* (BSD) *Language*
- Scan Chain and Scan Insertion
- DC Scan and AC Scan
  - DC Scan, to detect *stuck-at faults*, traditional
  - AC Scan, to detect *at-speed defects*
- Boundary Scan and BSDL (*Description Language*)
  - BSD is supported by JTAG
  - JTAG (Joint Test Action Group, 1985-), IEEE 1149.1-1990

Design for Test - Tips

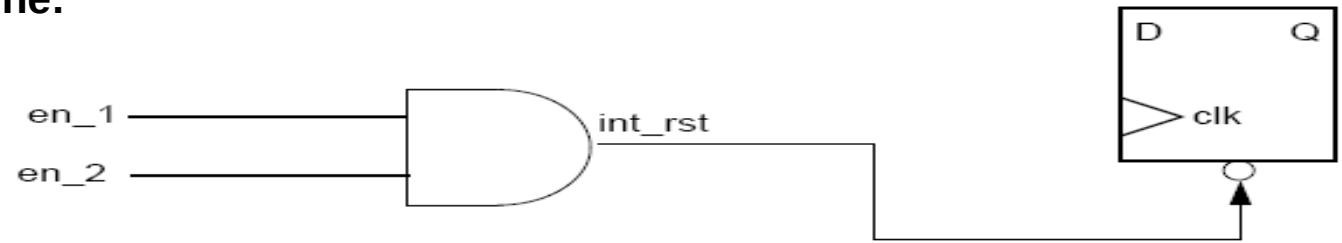
- Flip-flops must have asynchronous set or reset
- Asynchronous set/reset of the flip-flops should either be inactive during scan shift or should be directly controllable from primary port
- Clock can not be as a part of set/reset or data of a latch/flip-flop
- Either all the sets/resets should be synchronous or all should be asynchronous.
- Avoid internally generated clocks and sets/resets
- For each internally generated clock, a test clock must be present
- The clock of a flip flop be connected to one test clock, and only one, through test logic circuitry
- The enable of latch be directly controllable from the primary inputs
- Control the condition of a tri-state enable during the scan shift operation

Example Test Methodology

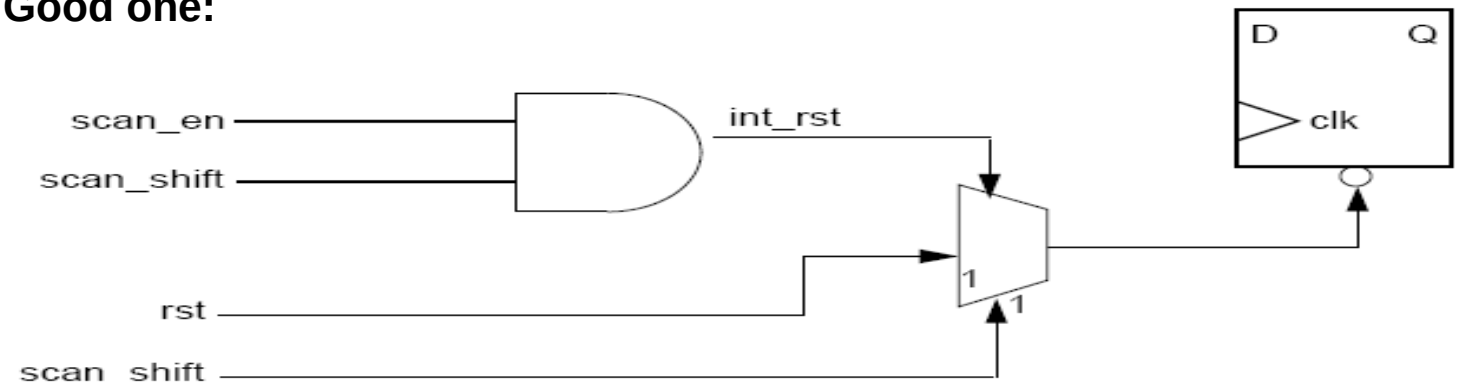
- There is NO ONE Ideal DFT solution for every design
  - Different methods are usually combined to reach testability goals
  - Example Methodology
    - Design Characteristics
      - Synchronous flip-flops based design with hard macro RAMs. No memory BIST available for RAMs. IEEE 1149.1 boundary scan logic compliance required
    - Methodology
      - Fault simulation of functional vectors exercising the RAMs. So RAMs should be modeled for fault simulation. Generate a fault list of all detected faults
      - Insert scan DFT on the non-RAM portion of the design
      - Generate functional patterns for testing the IEEE 1149.1 boundary scan logic.
      - Fault simulate 1149.1 functional test vectors. Generate a fault list of all detected faults.

Design for Test Example

Bad one:



Good one:



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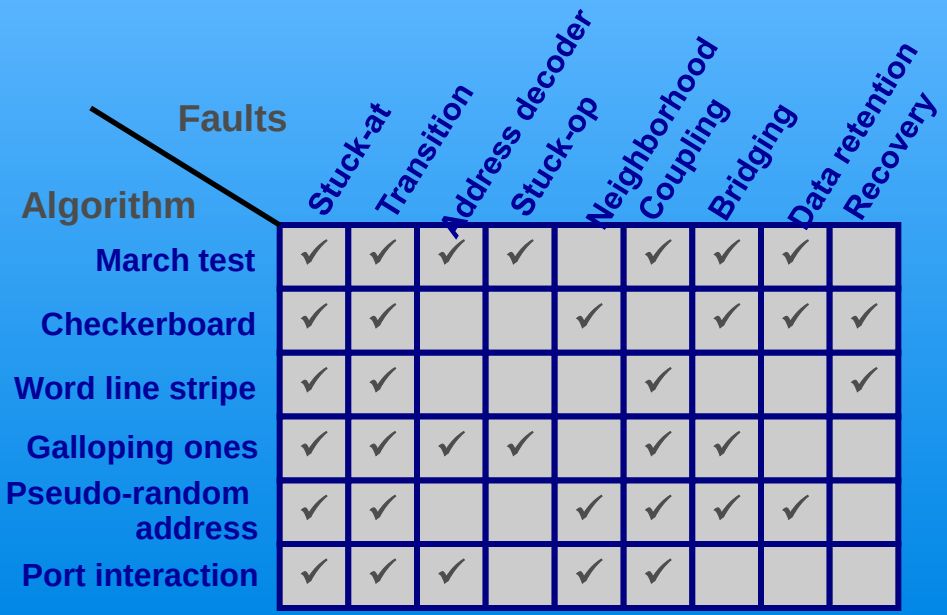
Built-In Self-Test - BIST

- **L**BIST and **M**BIST
  - Logic BIST
  - Memory BIST
- ATPG
  - Designer can write test pattern for a coverage of **70-75%**
  - ATPG can produce a coverage of **98%**

Scan DFT and ATPG

- Scan design for test (scan DFT) and automatic test pattern generation (ATPG) are currently the most popular methods to perform testing for manufacturing defects
- ATPG generation
  - *manual method;*
  - *algorithm method; and*
  - *pseudo random generation method.*
- ATPG with EDA Tool
  - can automatically generate manufacturing test patterns
- Scan DFT
  - Reduces the complexity of the test generation problem by making all/some sequential cells directly controllable and observable

Memory BIST - Flexible Memory Test



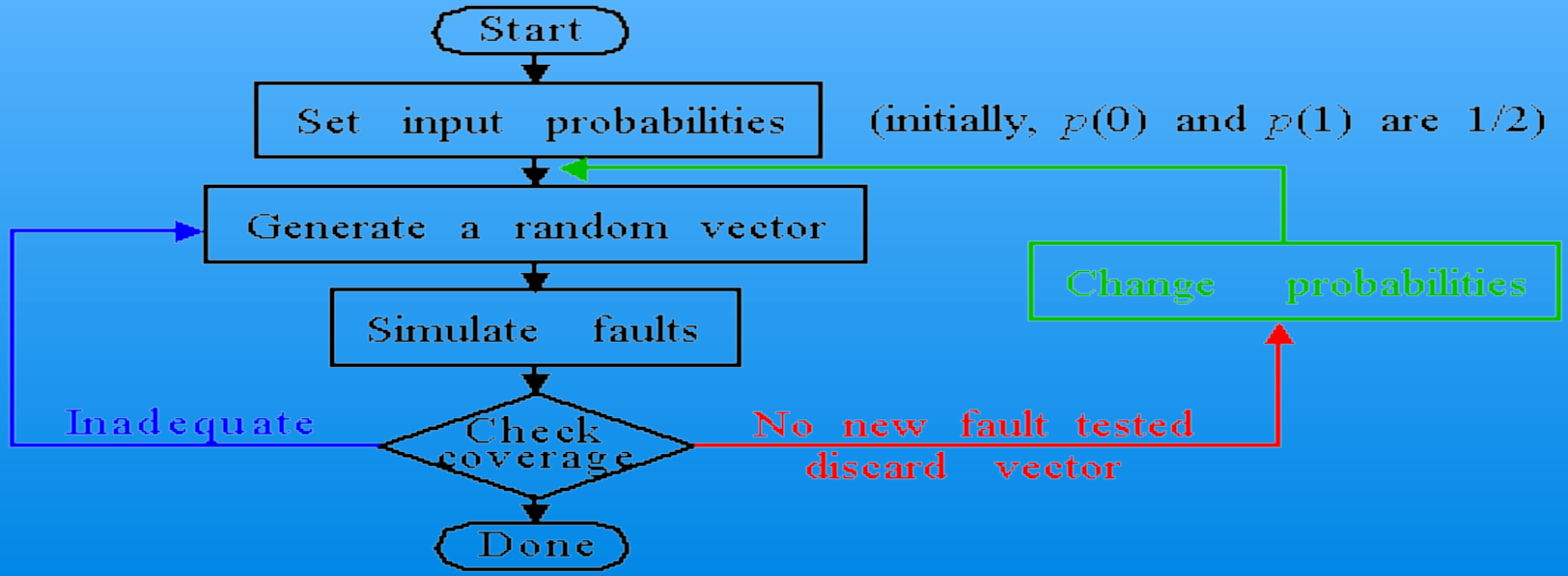
Algorithm \ Faults	Stuck-at	Transition	Address decoder	Stuck-op	Neighborhood Coupling	Bridging	Data retention	Recovery	
March test	✓	✓	✓	✓		✓	✓	✓	
Checkerboard	✓	✓			✓		✓	✓	✓
Word line stripe	✓	✓				✓			✓
Galloping ones	✓	✓	✓	✓		✓	✓		
Pseudo-random address	✓	✓			✓	✓	✓	✓	
Port interaction	✓	✓	✓		✓	✓			

Multiple Algorithms Supported

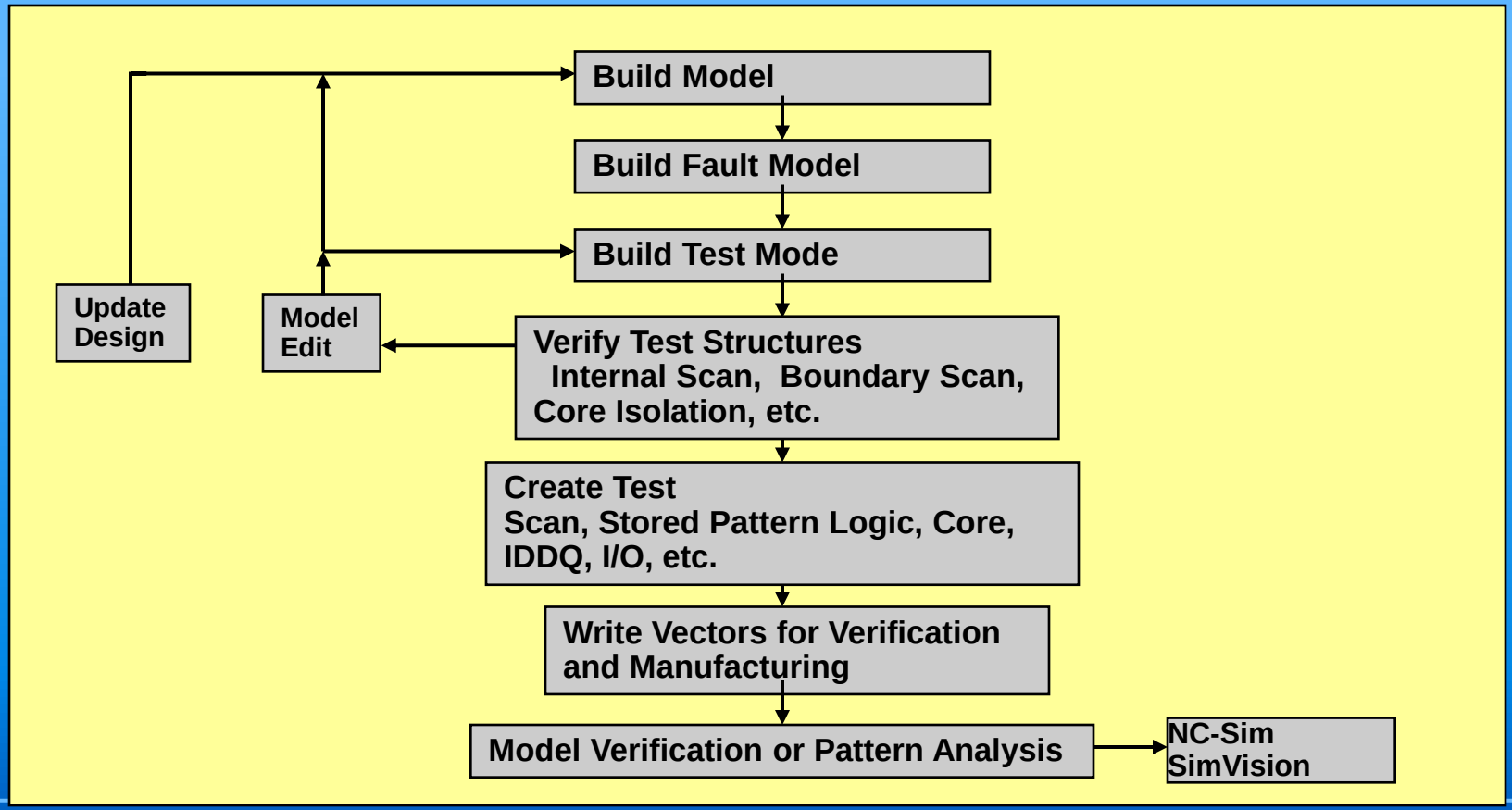
- **checkerboard** or **checkerboard_retention**
- **wordline stripe**
- **march c- enhanced** or **march lr prime**
- **pseudo-random address**
- **galloping ones**
- **port interaction**

Algorithms are runtime selectable

ATPG


Start
Set input probabilities
(initially, $p(0)$ and $p(1)$ are 1/2)
Generate a random vector
Simulate faults
Check coverage
Inadequate
No new fault tested
discard vector
Change probabilities
Done

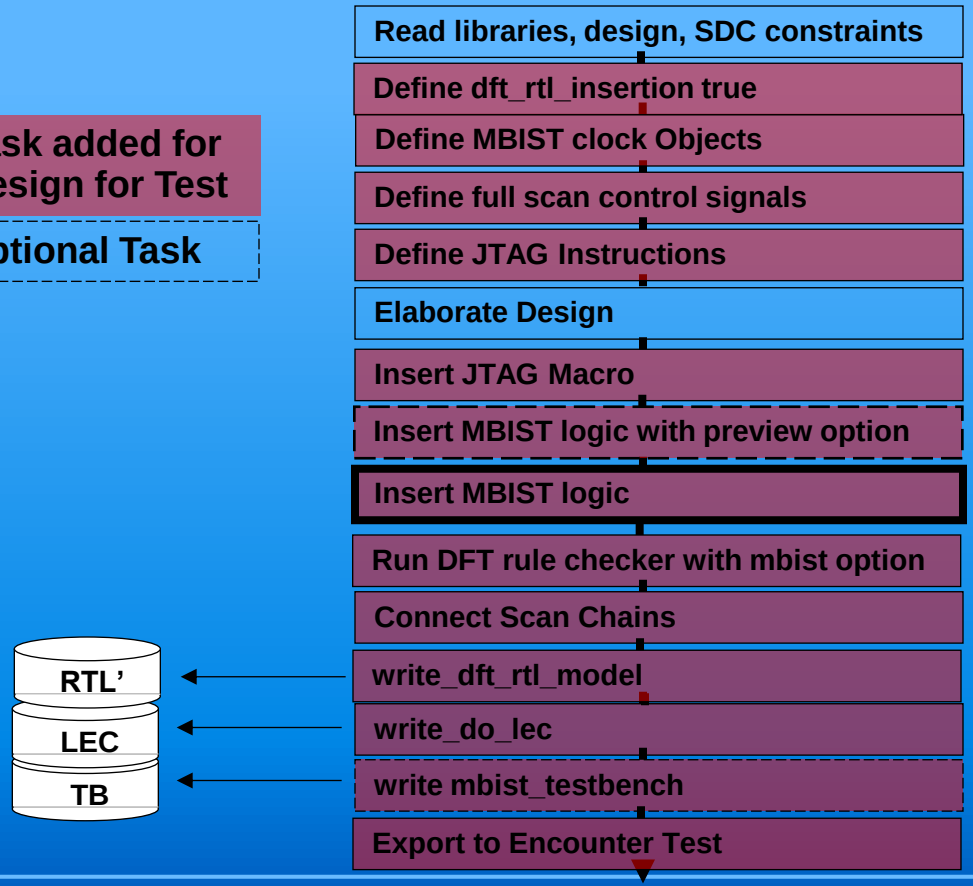
Encounter Test ATPG Process Flow



Insertion of MBIST using RC-DFT (RTL level netlist)

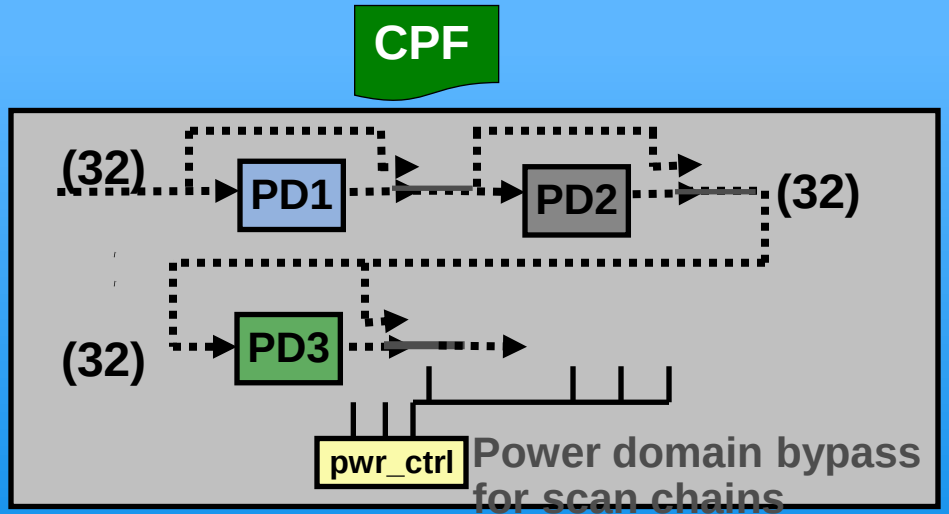
Task added for Design for Test

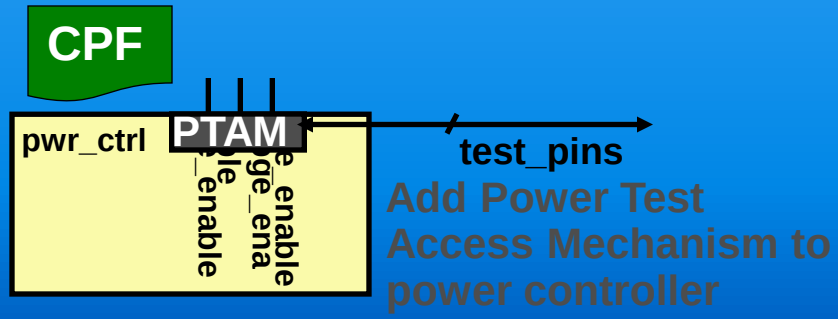
Optional Task



- Define to "True" for RTL Insertion
- Define Clocks used for MBIST
- Define MBIST Instruction
- Generates configuration file template
- Insertion based on configuration file
- Validates controllability of test signals
- Write out minimally RTL netlist
- Write out verilog testbench

Front-End: Power-Aware Test





Tester Power Consumption

Mode	Clock (MHz)	% Switch	Power (mW)
Normal	500	10~20	2.96
Scan	50	46	11.86
LP Scan	50	6	1.66

- **ATPG test coverage for low-power structures**
- **Power-aware ATPG**
  - **Minimize power during test mode by intelligent fill of test patterns**

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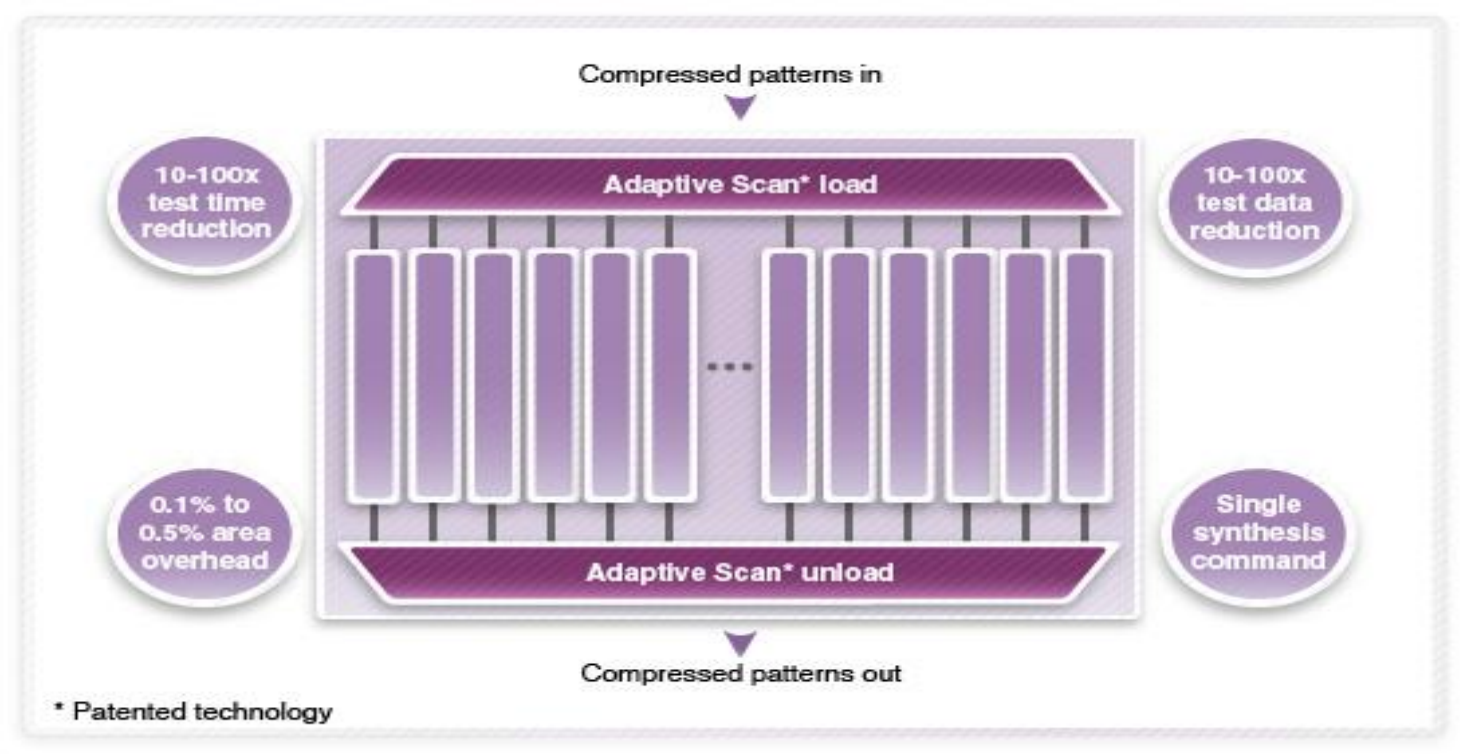
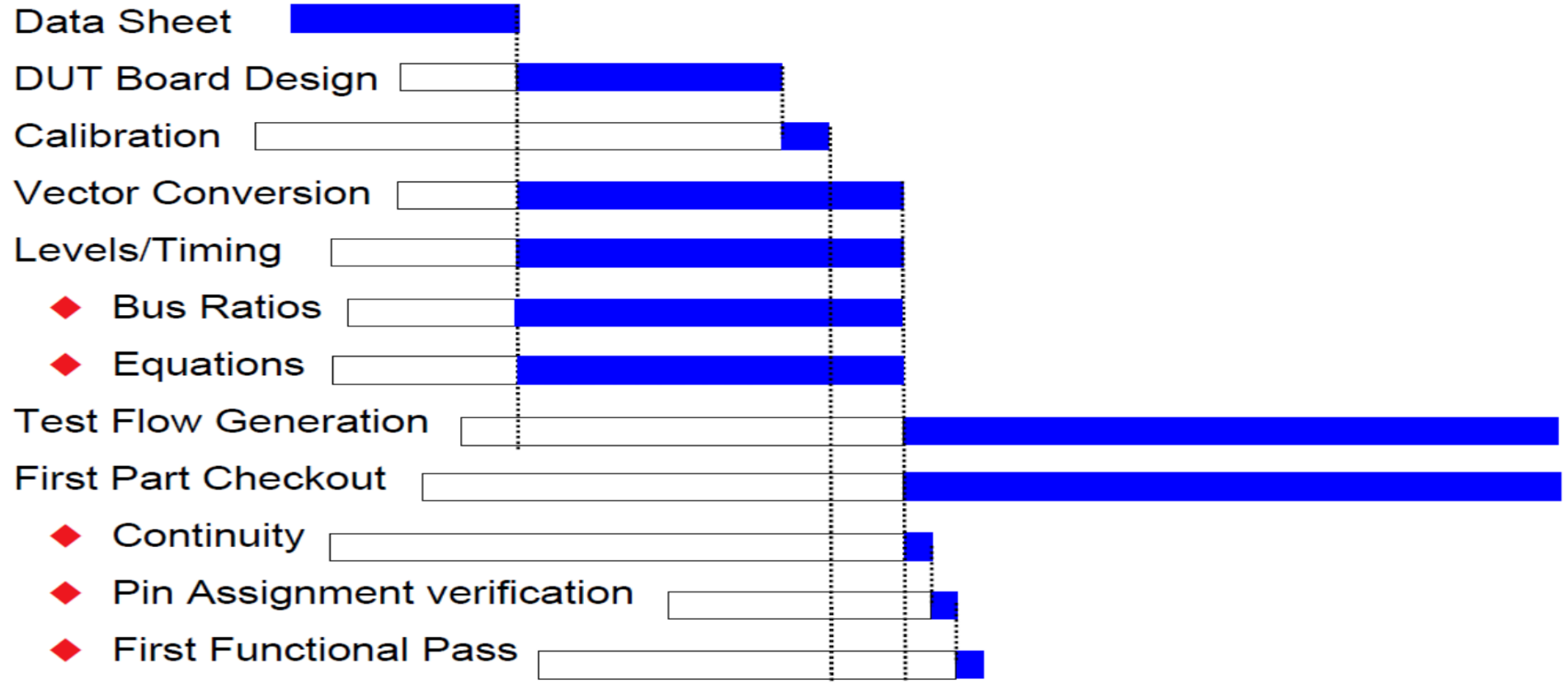
DFT Compression



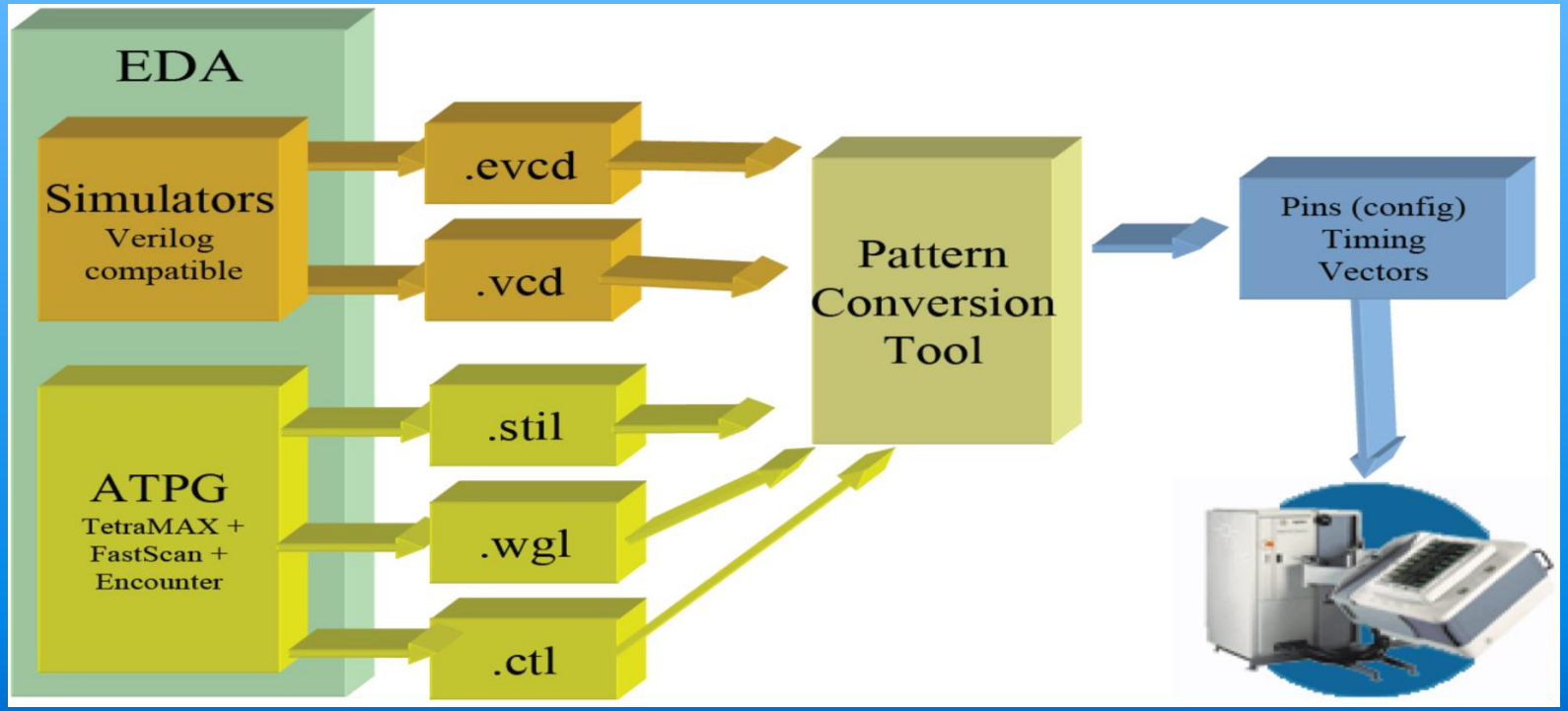
DUT Board Design

- Package type
- Pin names
- Tester configuration
- Types of tests
- Decoupling
- Power supplies
- Special tests: RF, Analog, Memory
- High speed

Test Program Generation



Vector Conversion



Installed ATE Example

Verigy 93000 PinScale test system

- Up to 3.6Gbps data rate
- 448 channels
- Mixed-Signal option
- Port Scale RF option

Advantest T2000 test system

- Up to 800Mbps data rate
- 512 channels
- Mixed-Signal option
- RF test option

Teradyne J750HD test system

- Up to 800Mbps data rate
- 256 channels
- Wafer sort toolkit

Chroma 3360P test system

- 25/50 Mbps data rate
- 256 channels
- Wafer sort orientated configuration

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Complex DFT for Large Chip at 28nm

- Diff. std. for MBIST at 28nm (increased number of fault models)
- Low power scan scheme for huge chip
- Stuck-at/AC scan (at-speed)
- DFT Compression → DFT Architecture (wrapper/partition …)
- Overall DFT for 1000+ memory blocks

DFT at 20nm

- Test for
  - short/small delay defects (SDD)
  - new memory failure mechanisms
  - test compression strategies

Test Cycle – *ITC Annual since 1998*

- Test of devices, boards and systems
- Complete cycle
  - design verification
  - design-for-test
  - design-for-manufacturing
  - silicon debug
  - manufacturing test
  - system test
  - diagnosis
  - reliability and failure analysis
    - and back to process and design improvement

Summary - *DFT/ATE - Topics of Interest*

- 3D/2.5D Test
- Adaptive Test in Practice
- ATE/Probe Card Design
- Advances in BS
- …