University of Chinese Academy of Sciences

Verification & Implementation of SoC Design

RC Extraction and Delay Calculation

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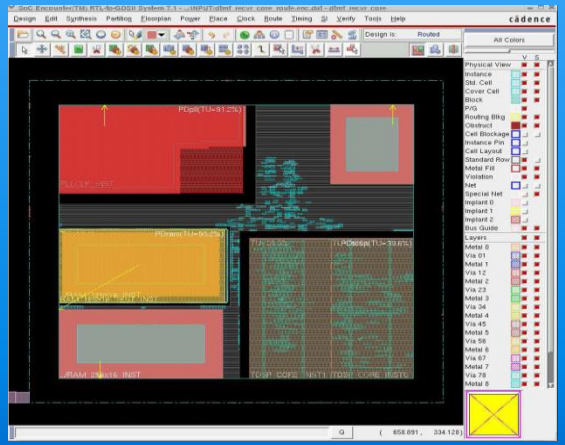
RC and DC

- **Principles of RC Extraction**
- **Types of Extraction**
- **Extraction Models**
- **Delay Calculation**
- **Discussion**

What Is Parasitic Extraction?

- It is a critical link between two domains.

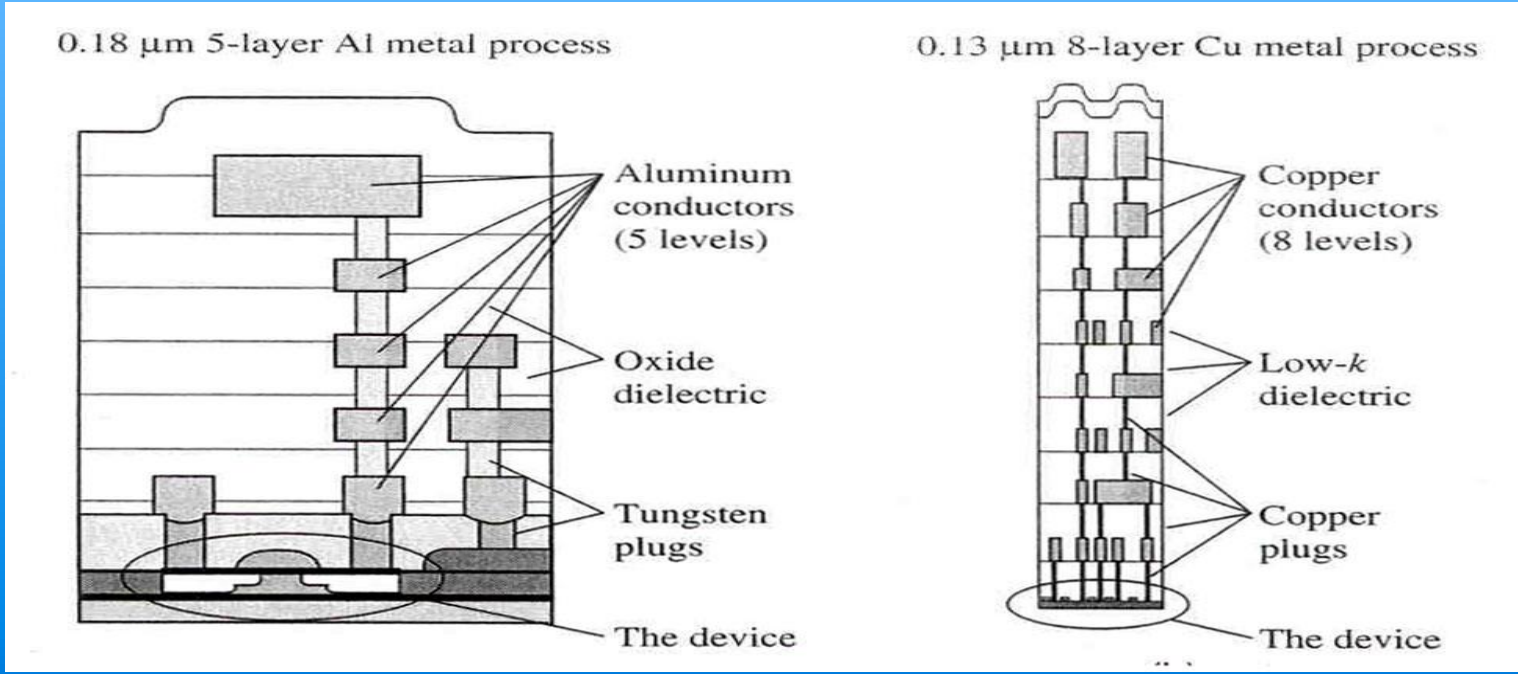
Physical domain → Extraction → **Electrical domain**



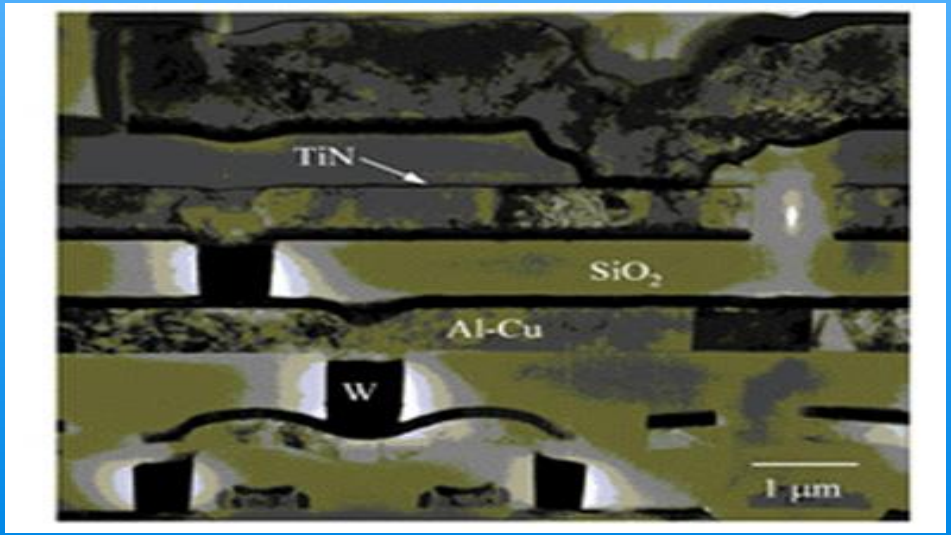
```
*D_NET *3889 0.360008
*CONN
*P port_pad_data_out[8] O *C 359.7 329
*I *3675:Y O *C 358.71 329.56 *D INVXL

*CAP
0 port_pad_data_out[8] 0.0891337
1 *3675:Y 0.115719
2 *3889:2 0.155155

*RES
0 *3675:Y *3889:2 1.52
1 port_pad_data_out[8] *3889:2 1.55214

*END
```

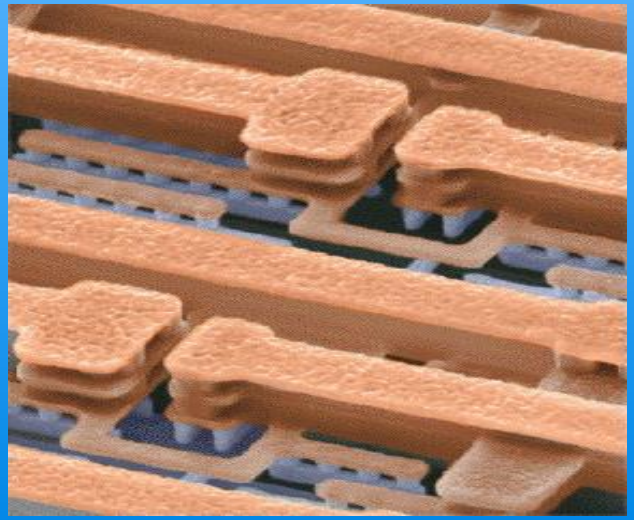
Extracted netlist

Cross-Sectional Comparison of 0.18 (Al) and 0.13 (Cu) Devices



Interconnect by SEM





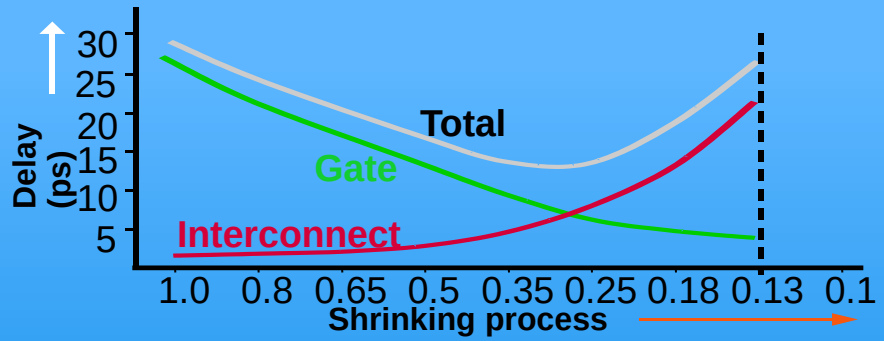
RC EXTRACTION - *SPEF FOR CROSSTALK ANALYSIS*

- Report -> RC to extract parasitic data from a routed database
  - Generate SPEF containing distributed cross-coupling information
- Why SPEF?
  - In a lumped cross-coupling model, we do not know location of violation (closer to driver or receiver?)
  - In a lumped cross-coupling model, we do not know which specific receiver is in violation, for multi-fanout nets
  - Distributed cross-coupling information in SPEF helps resolve these issues

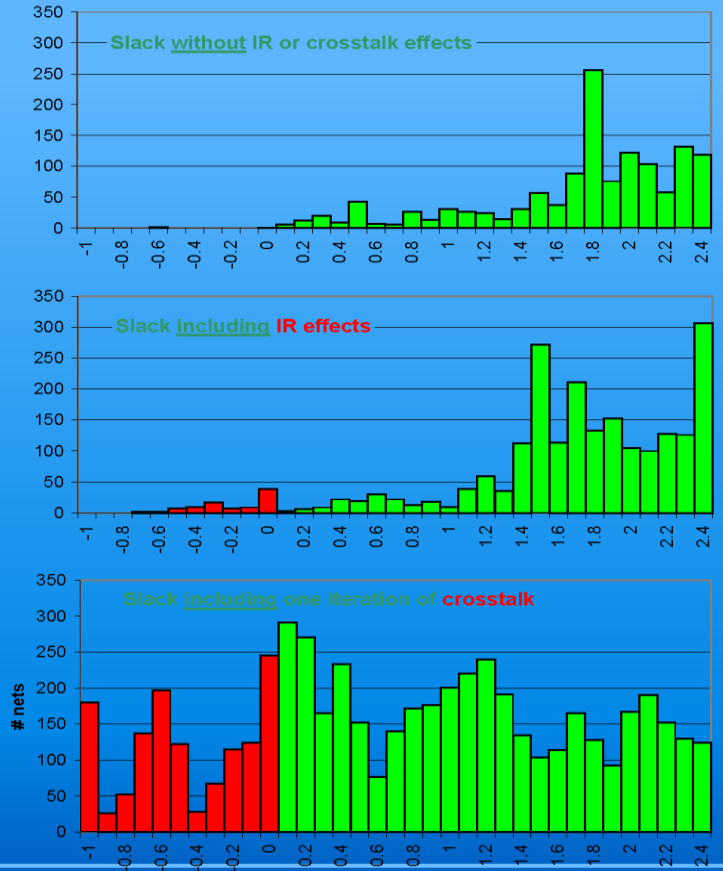
RC EXTRACTION - *LUMPED Vs. DISTRIBUTED COUPLING*

Consider the situation above. A2 clearly will have a bigger effect on the receiver of the victim than will A1. Using lumped coupling these two nets would be identical when clearly they are not.

Importance of Interconnect

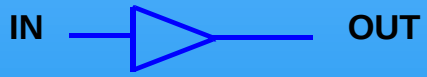


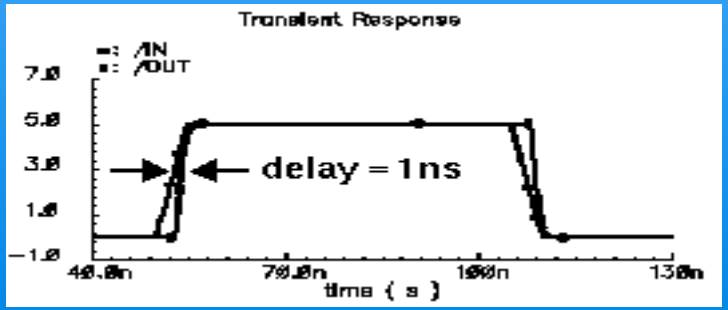
- The contribution of interconnect to the delay of signals is greater than the cell contribution at 0.18 um and below.
- Contributions of interconnect amount to 80% of the overall path delay.
- Accurate knowledge of the interconnect parasitics is a must for high-performance chip design.
- Accurate coupling capacitance extraction is a must for signal-integrity analysis.



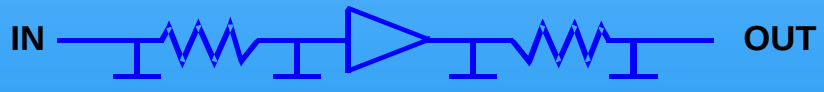
Parasitic Element Analysis

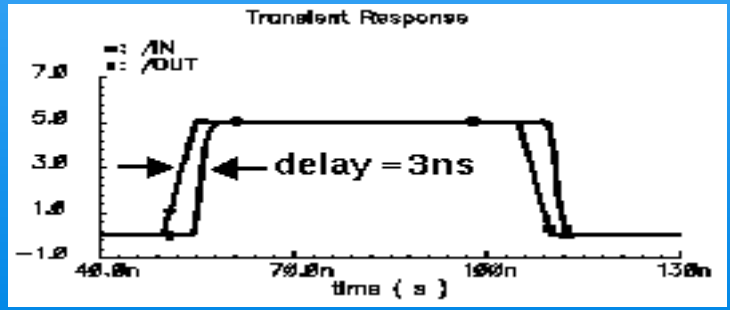
- Simulating parasitic elements as a part of the design is required to accurately model the manufactured circuit.





Results using device models only

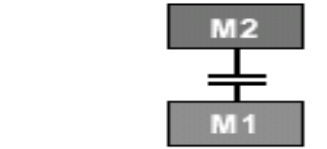




Results including parasitics

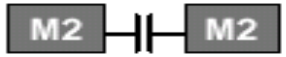
Parasitic Capacitance Components

Capacitance Models



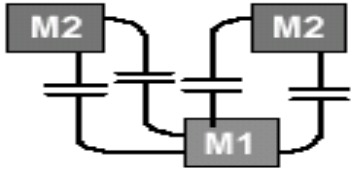
Area capacitance C_a

parallel plate or overlap capacitance



Lateral capacitance C_l

line-to-line coupling or sidewall capacitance



Fringe capacitance C_f

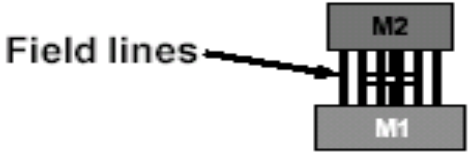
coupling between conductors in different planes (everything else)

C_{total} on any node = $C_a + C_l + C_f$

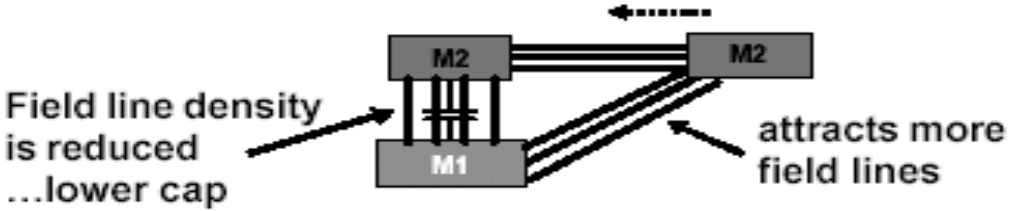
As process dimensions get smaller, lateral capacitance is becoming the more dominant of the 3 components.

Near Body Effect

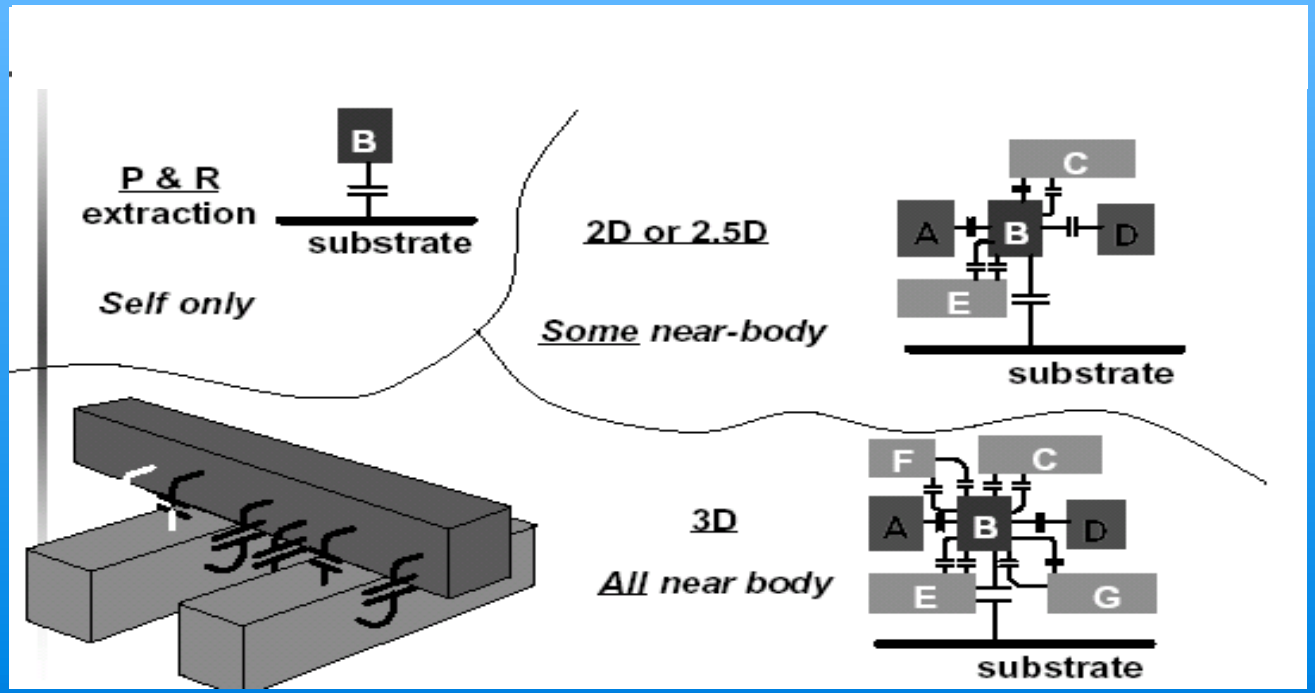
- Field line density reflects capacitance.



- Introduction of M2 causes nearbody effects



2D or 2.5D vs. 3D Extraction – Near-Body Effect



RC & DC

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- Types of Extraction
- Extraction Models
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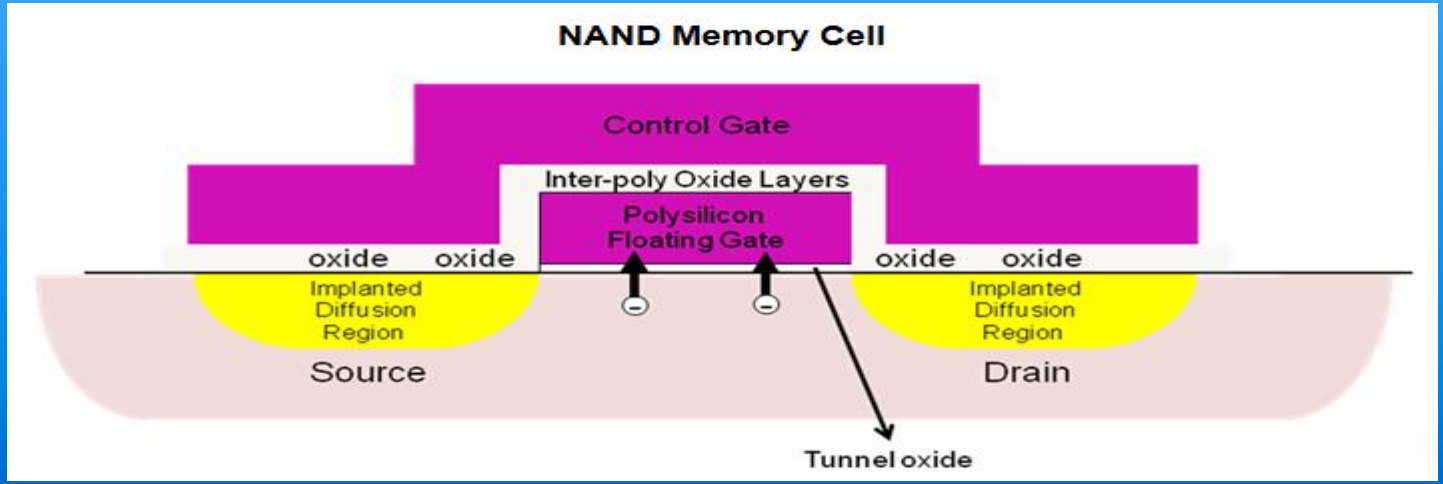
- Discussion

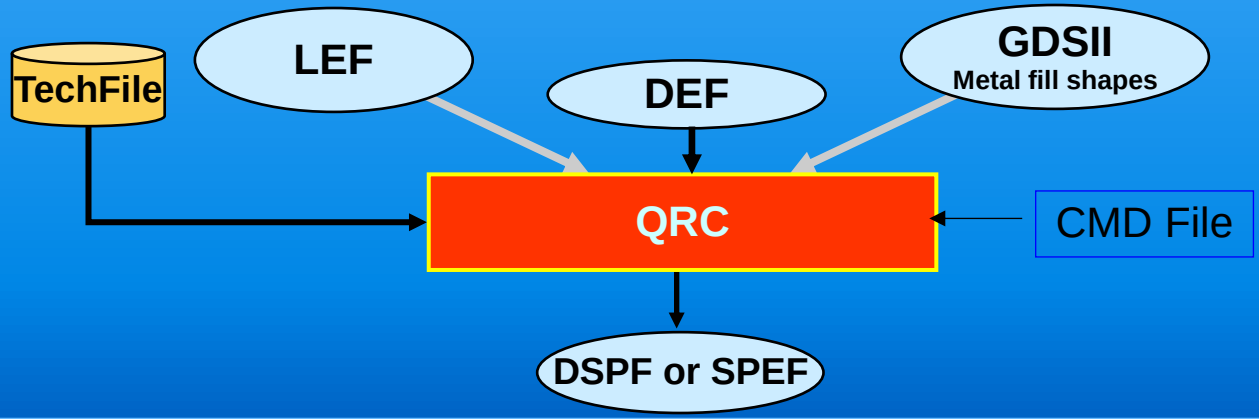
RC Extraction Levels

- Cell Level
- Transistor Level
- Substrate Level



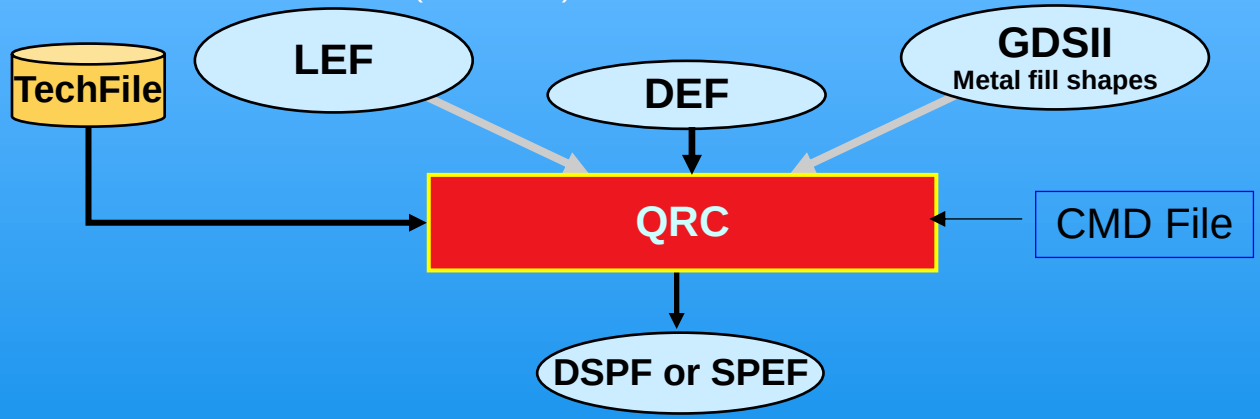
Cell Level Extraction

- Standalone with LEF and DEF flow
  - Layout design information read from DEF file.
  - Cell contents read directly from LEF.
  - Parasitic results output into DSPF or SPEF.
  - QRC can be plugged into a non-Cadence place-and-route environment.



Cell-Level Flow: QRC Standalone (continued)

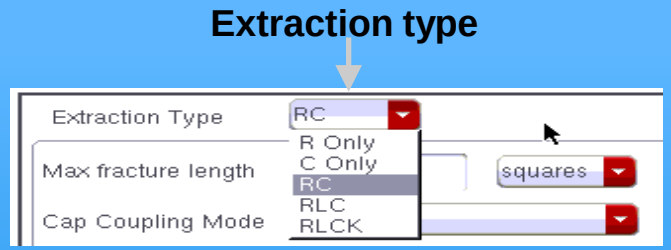
- LEF and DEF flow (continued)



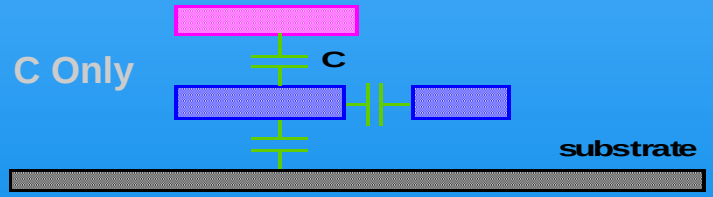
CCL Command: `input_db -type def`

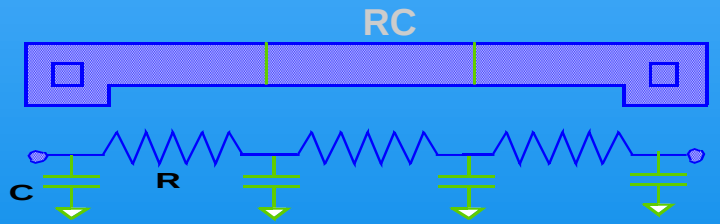
- `design_file <filename>`
- `lef_file_list <filename+> | -lef_file_list_file <filename>`
- `gds_file_list <filename+> | -gds_file_list_file <filename>`
- `libgen_library_name <filename>`

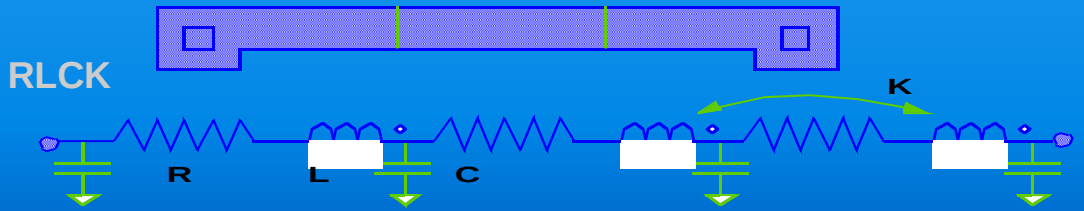
Transistor Level Extraction



Extraction tab

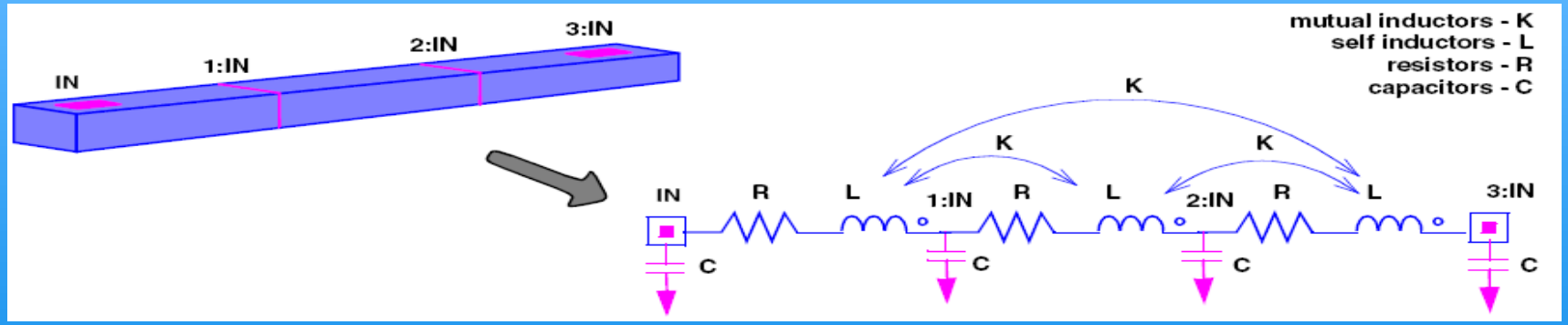


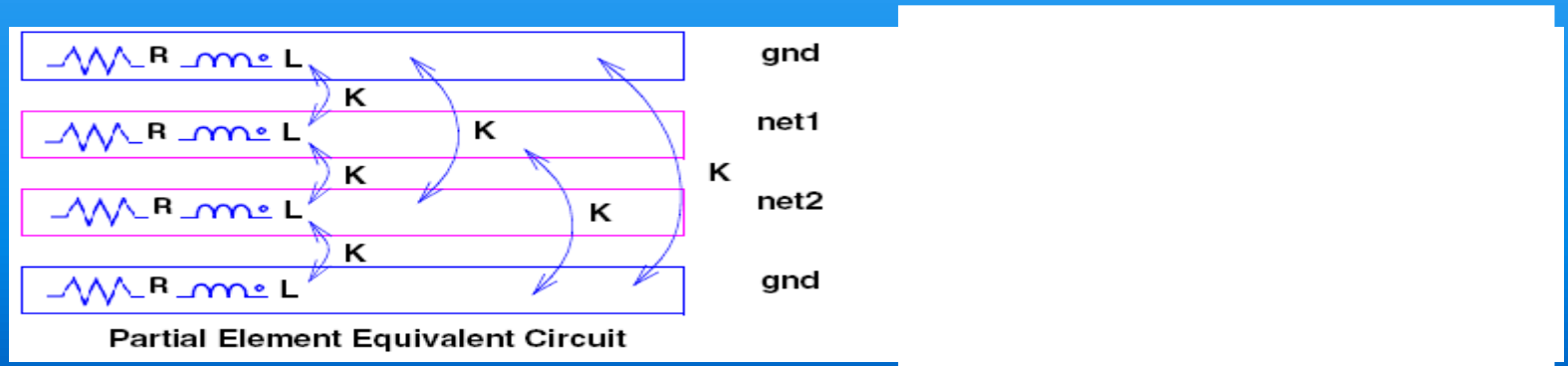




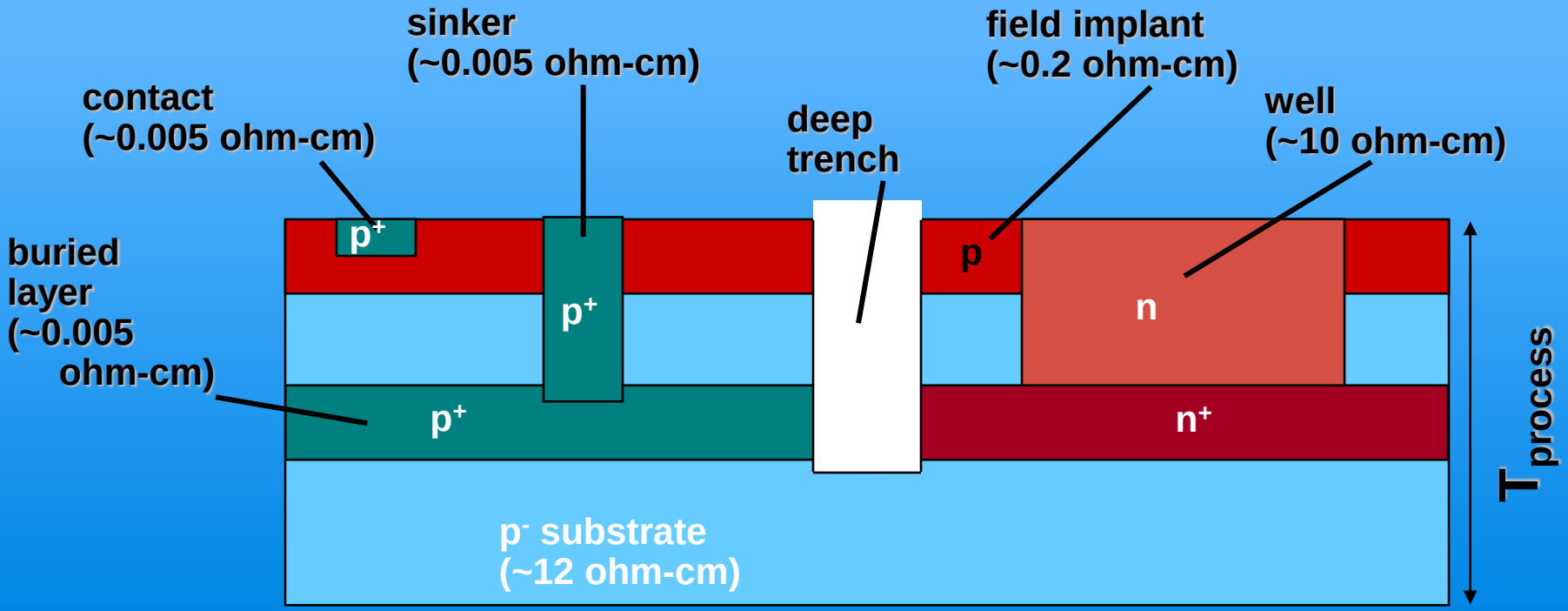
Inductance Extraction

- Physical Conductor Network Representation





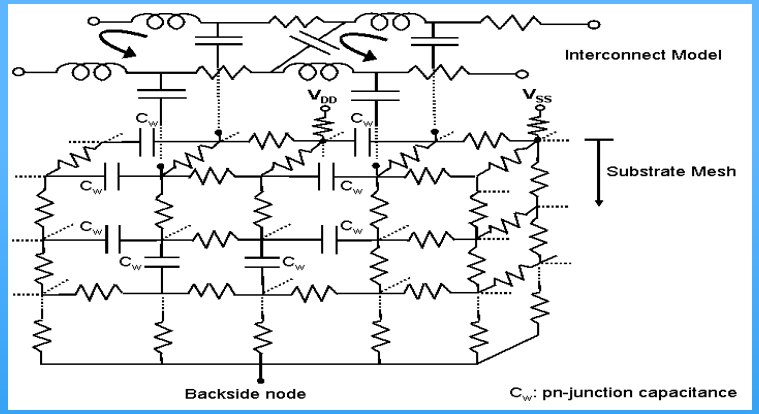
Substrate Cross-section

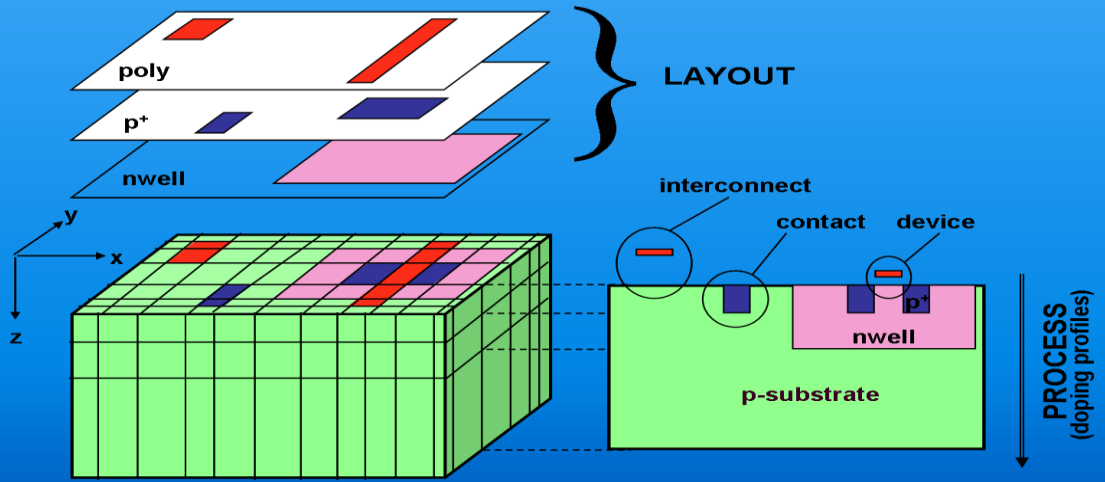


Substrate Technology File built based on process doping profiles

Substrate Extraction

- Lightly doped substrates
  - Increased sensitivity of RF designs to substrate
  - Displacement currents dominate
- Full-chip substrate extraction capability
  - Model noise injection and propagation
  - Full-chip verification
  - Mixed A/D SoC, memories, etc
  - 1M+ transistors





RC Extraction Scenario

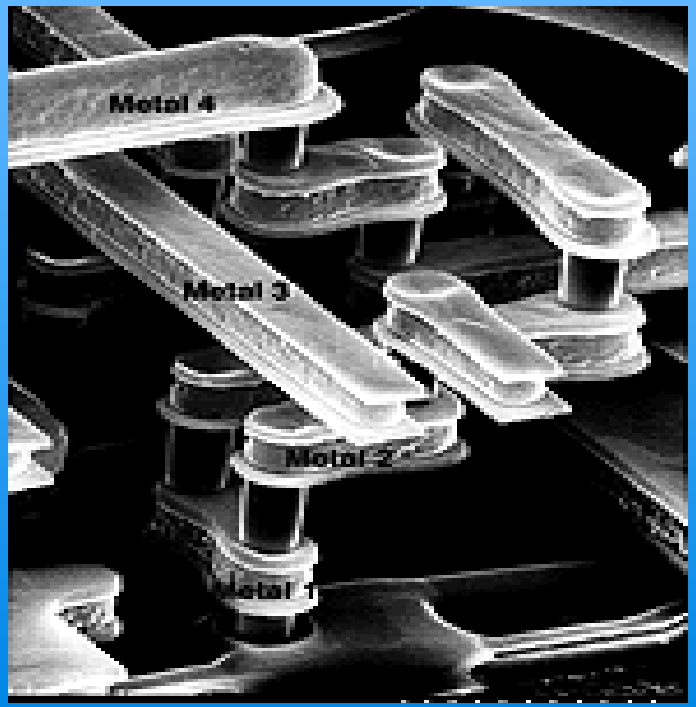


图6-2：四层互连线

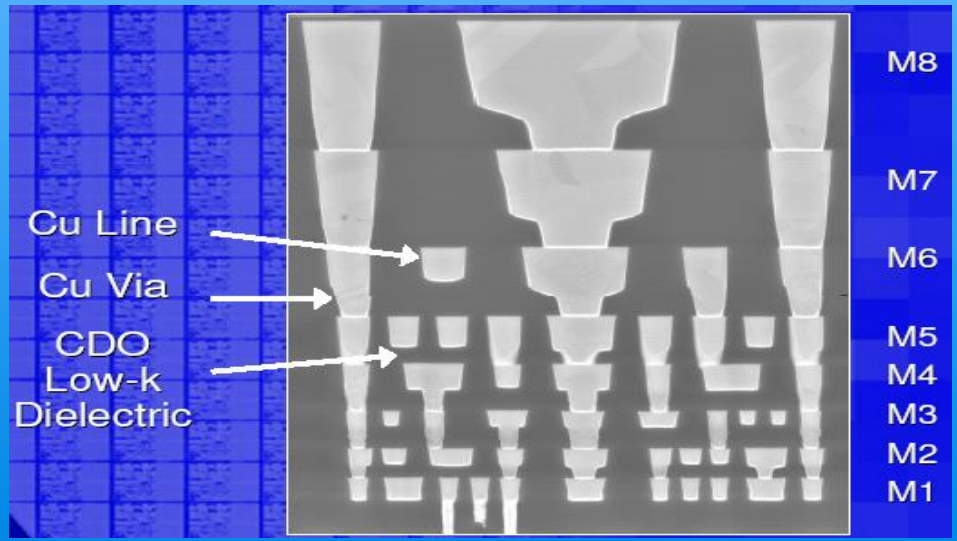


图6-3：八层互连线

R Extraction in the Interconnect

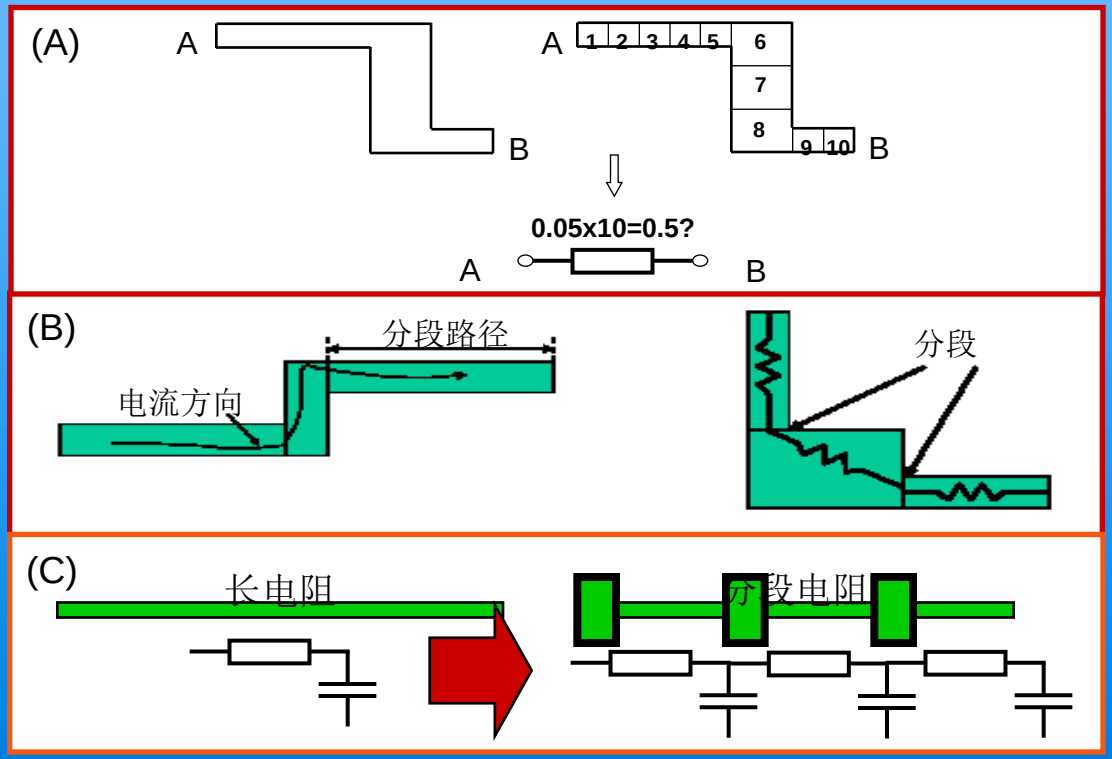


图6-8：互连线中的R提取模型

Distortion of R in the Interconnect

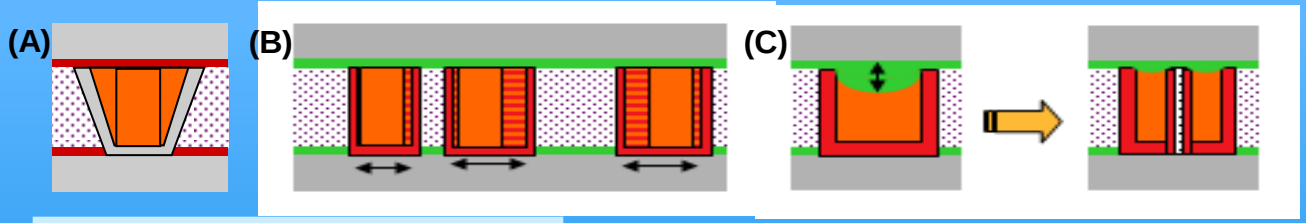


图6-9：130nm互连线中的R

表3-1 亚微米工艺中三层金属的物理参数值

0.8 μm 工艺	*H*	*T*	*W*
metal1	1.46	0.63	0.80
metal2	3.29	0.85	0.80
metal3	5.34	0.85	0.80

Classical VDMS Model

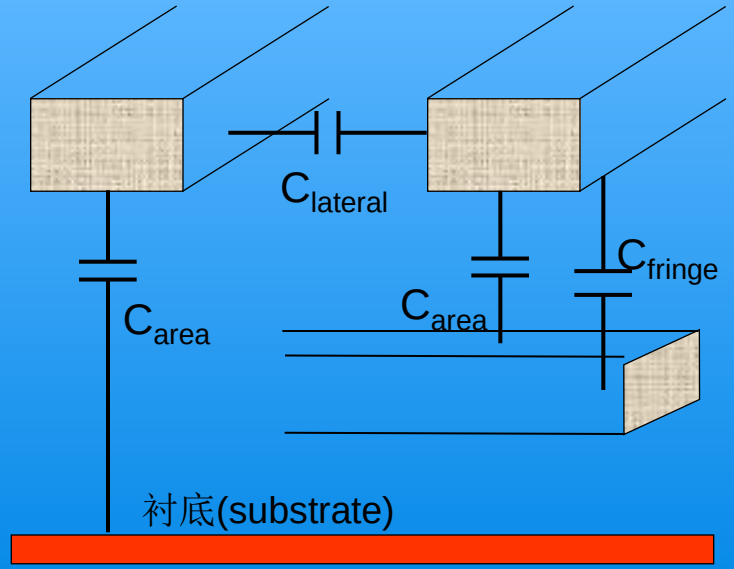


图6-10：用于互连线中C提取的平行板电容器模型和VDMF模型

Capacitance Model in DSM and Below

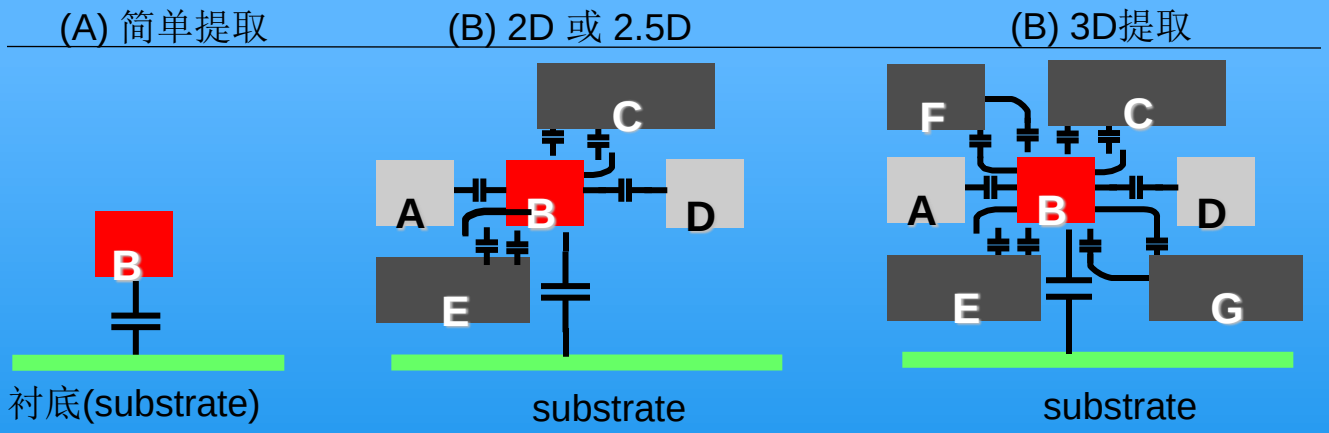


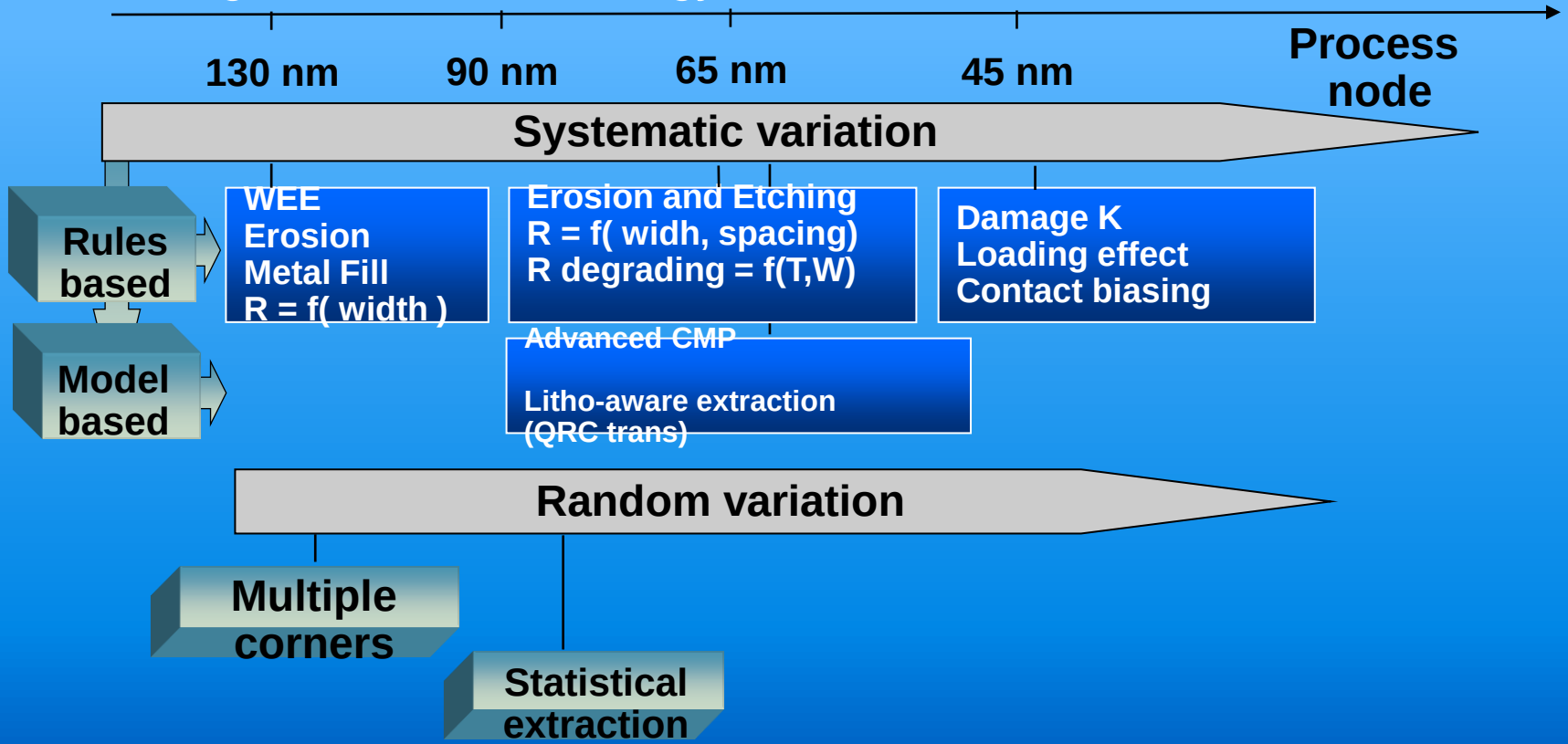
图6-11：用于亚微米的电容模型

表3-2 亚微米工艺中三层金属的物理参数值

130 nm	H	T	W
metal1	0.89	0.30	0.16
metal2	1.64	0.35	0.23
metal3	2.44	0.35	0.23

Modeling and Manufacturing Effects

- Driving extraction technology



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Wire Load Model Flow

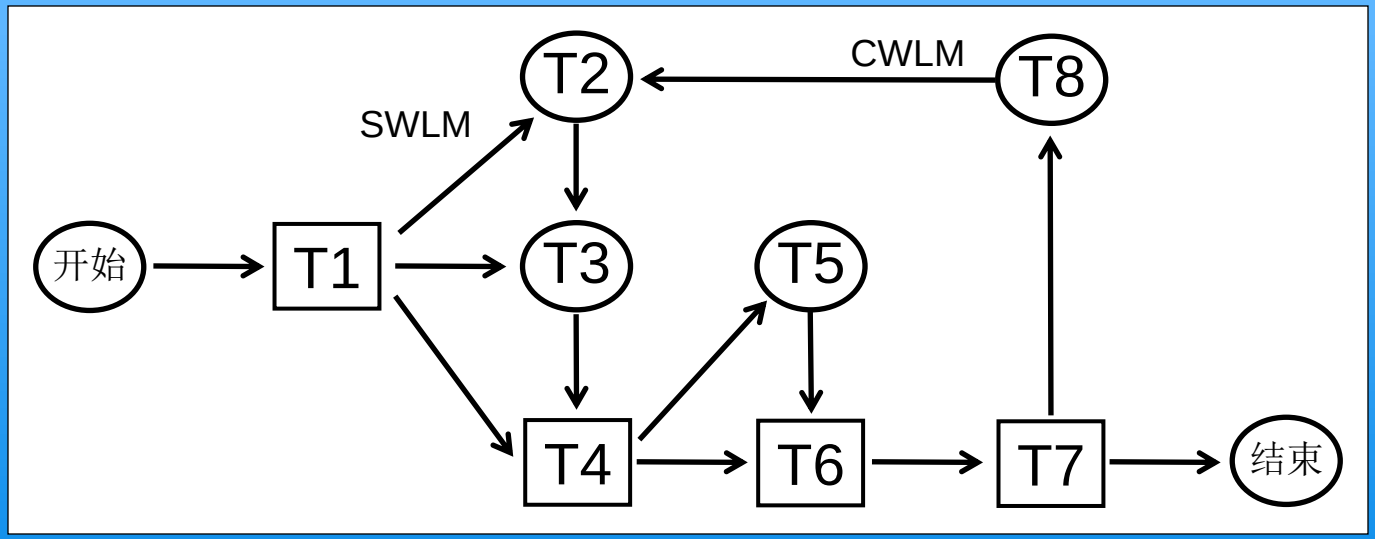


图6-4：WLM在物理实施流程中的应用

T1=synthesis, T2=read SWLM, T3=pre-placement opt, T4=placement;
T5=post-place opt, T6=global routing, T7=detail routing, T8=generate CWLM
Reference: Andrew B. Kahng and Stefanus Mantik

RC Extraction Model

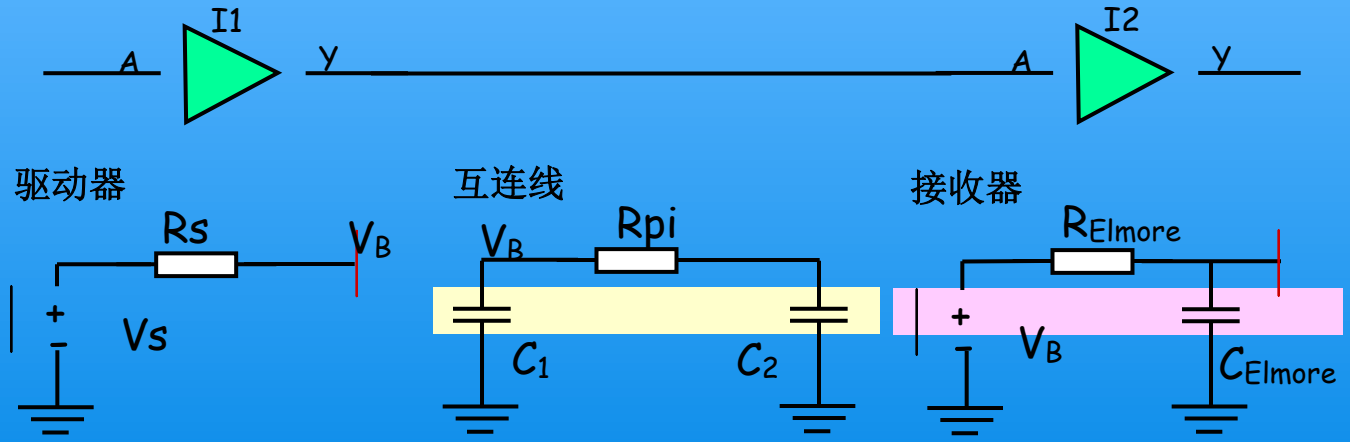


图6-5：互连线中的RC提取模型

Calculation of Parasitic Capacitance

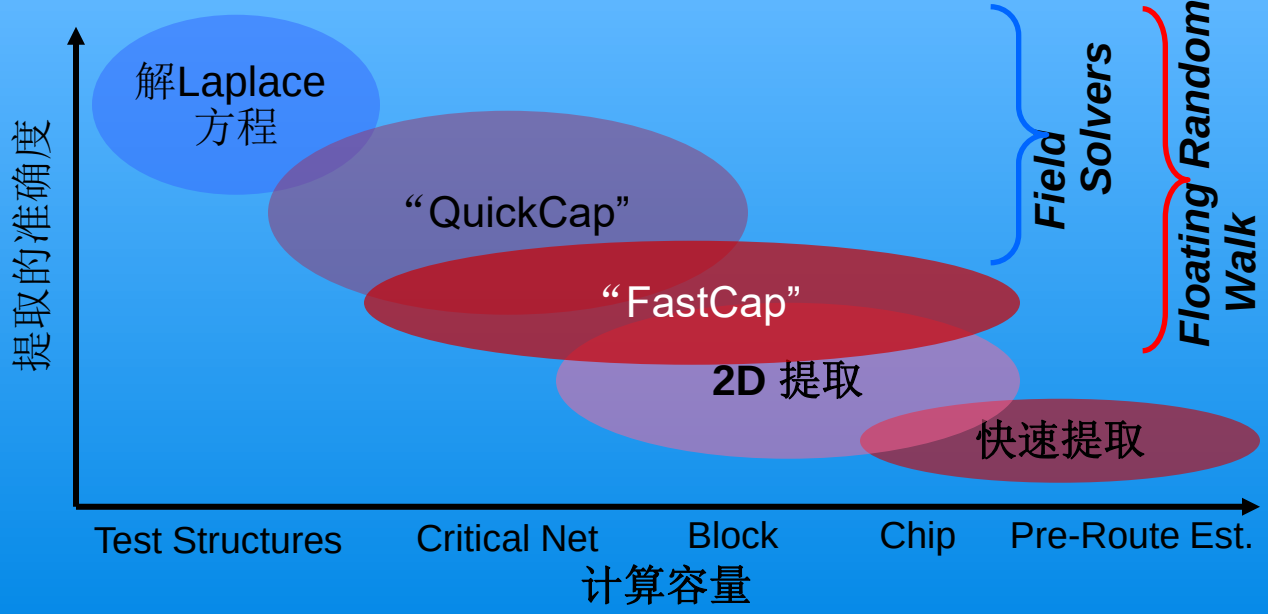


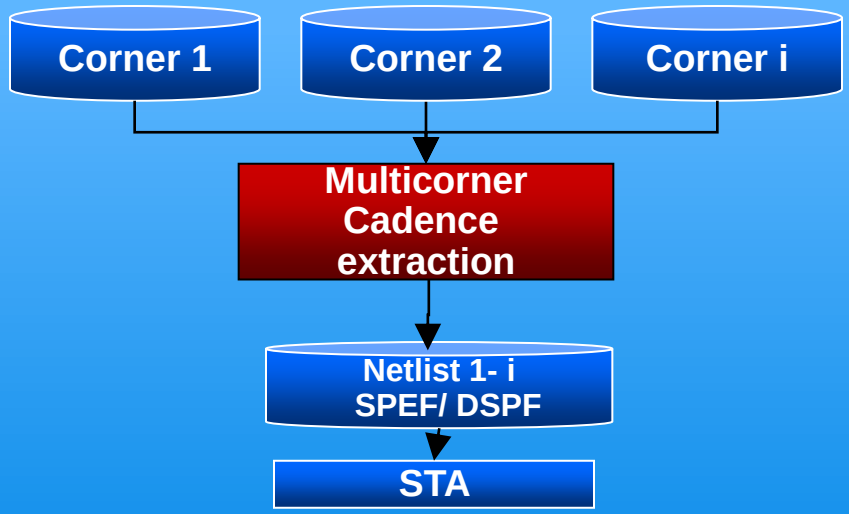
图6-12：用两维到拉普拉斯模型处理电容器计算

Multiple-Process Corner Extraction

- With the conventional extraction method, you can extract parasitics of the design with respect to each corner sequentially. For example, to extract 10 corners with the conventional method the QRC should be run 10 times.

- In MPC mode, you can extract parasitics of the design for different corners in a single extraction run with reduced turnaround time without compromising accuracy.

- In this MPC flow, the QRC runs only once and parasitic information for all process corners (tech files) is stored in multiple output files (one for each corner, in case of SPEF/DSPF output).
- Each single output file from QRC (in MPC mode) is analyzed separately by downstream tools, such as STA (static timing analysis).



- Advantages
  - Keeps traditional flows working
  - Run-time savings in extraction for multiple corners

RC & DC

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Parasitic SPF File

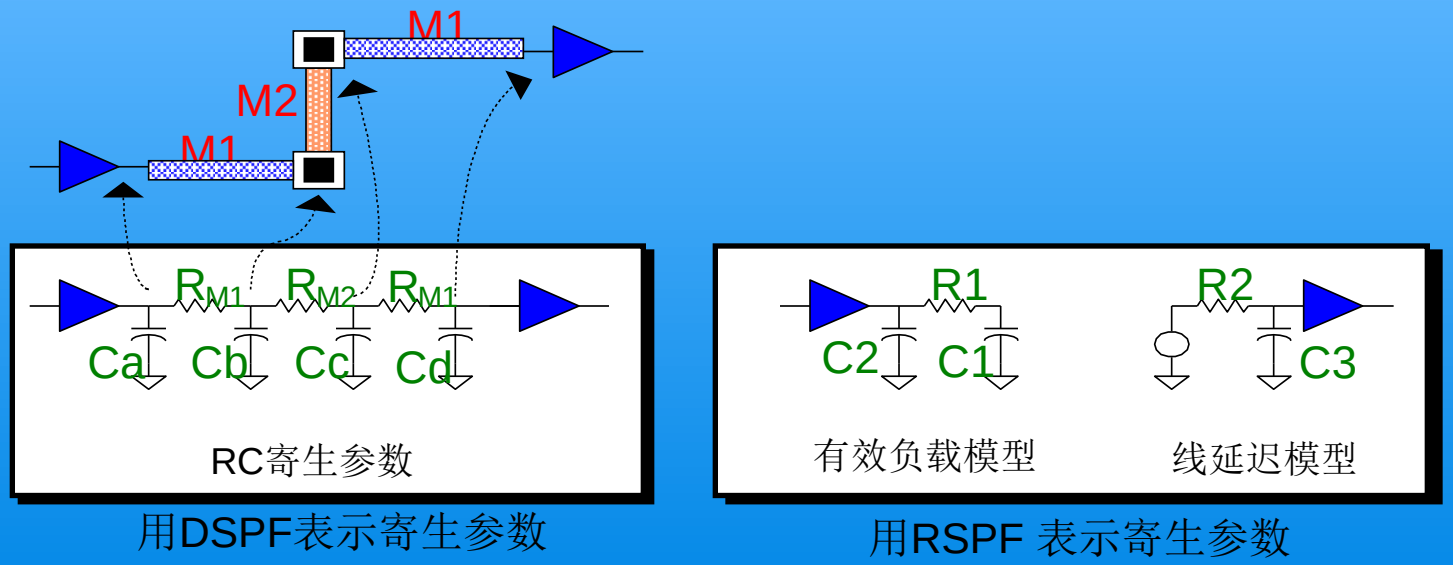


图6-14：DSPF和RSPF的应用

Parasitic SPEF File

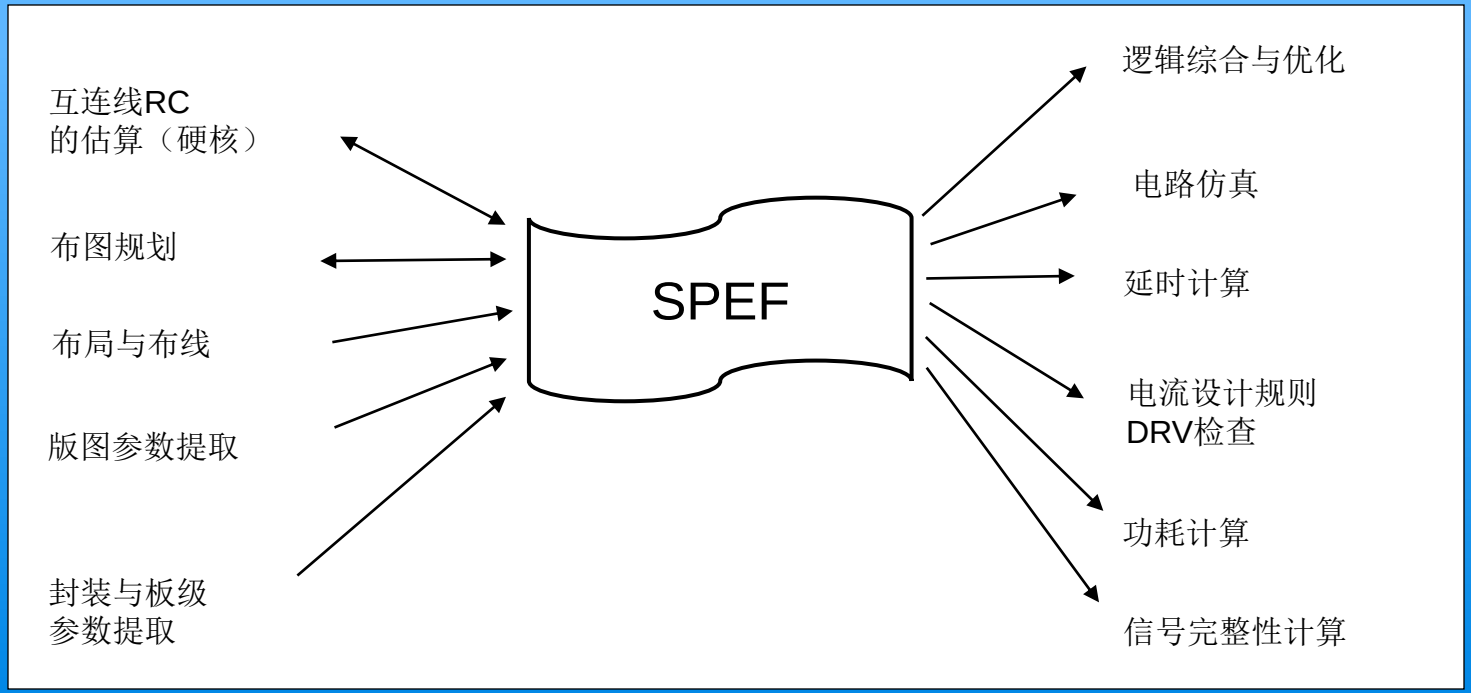
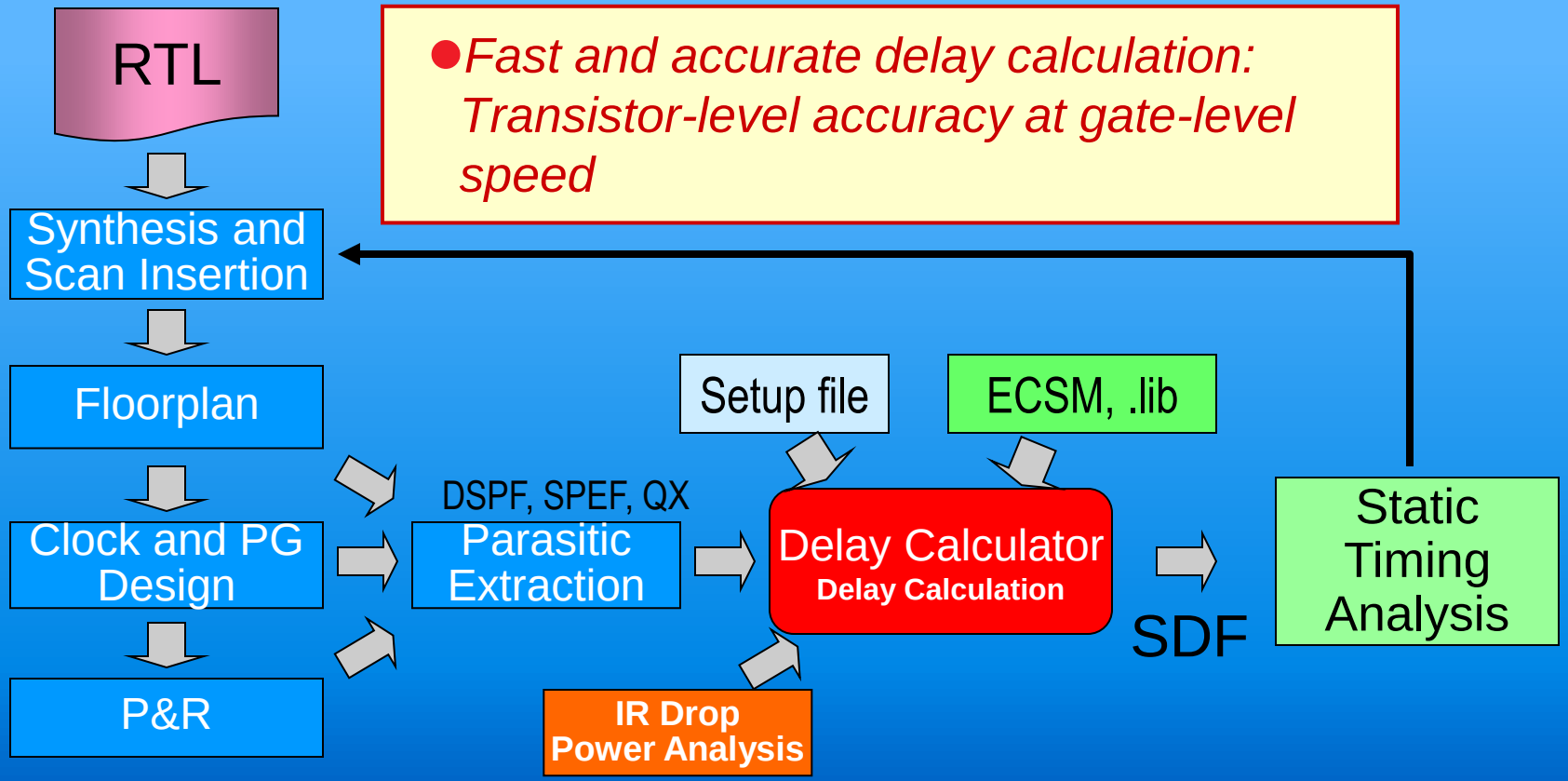


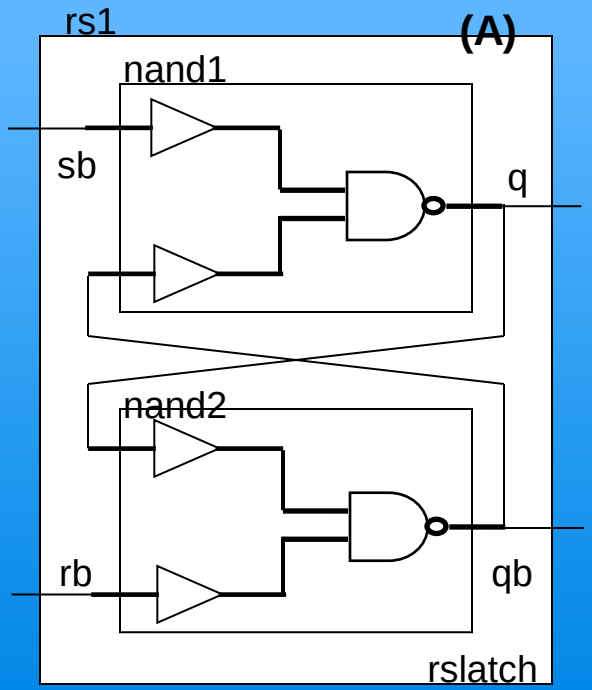
图6-15：SPEF的应用

Delay Calculation Method



- *Fast and accurate delay calculation: Transistor-level accuracy at gate-level speed*

Standard Delay SDF File



(B)

```
(CELL
(CELLTYPE “rslatch“)
(INSTANCE rs1)
(DELAY
(ABSOLUTE
(IOPATH sb q (1:3:8) (4:5:7))
(IOPATH rb q (1:3:8) (4:5:7))
(IOPATH sb qb (2:4:9) (6:8:12))
(IOPATH rb qb (2:4:9) (6:8:12))
)
)
)
```

(C)

```
(INSTANCE top)
(DELAY
(ABSOLUTE
(INTERCONNECT d1.y c.r1.a (0.01:0.02:0.03))
(INTERCONNECT d1.y c.r2.a (0.03:0.04:0.05))
(INTERCONNECT d1.y r3.a (0.05:0.06:0.07))
(INTERCONNECT b.d2.y c.r1.a (0.04:0.05:0.06))
(INTERCONNECT b.d2.y c.r2.a (0.02:0.03:0.04))
(INTERCONNECT b.d2.y r3.a (0.02:0.03:0.04))
)
)
```

图6-16：SDF中的器件延迟与互连线延迟

Application of SDF and the Flow

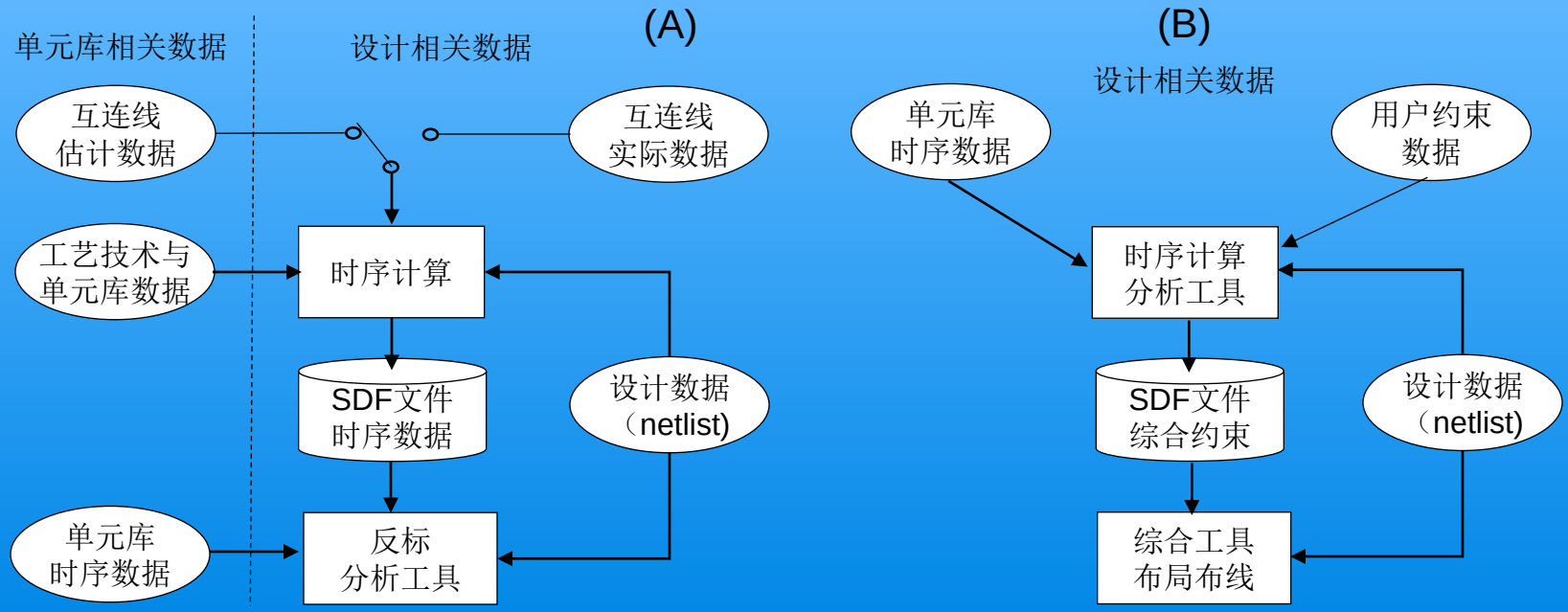


图6-17：用SDF文件作时序分析的流程图

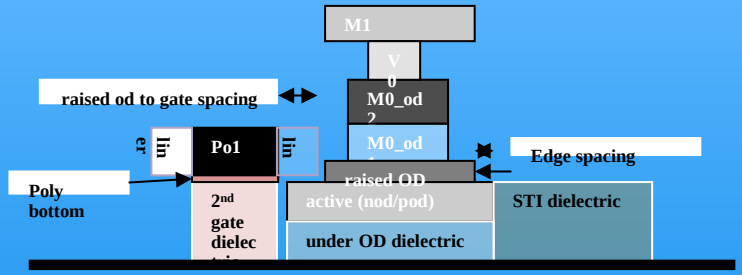
RC & DC

- Principles of RC Extraction
- Types of Extraction
- Extraction Models
- Delay Calculation
- Discussion

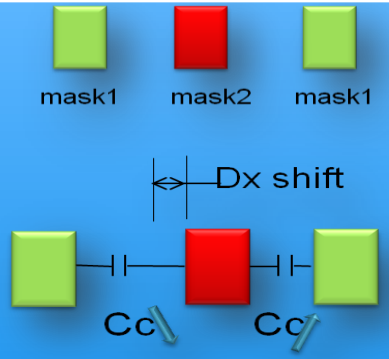
20nm Extraction, Timing and Power signoff

New extraction considerations at 20nm

2-step M0/V0, Raised source-drain with bias, 3D fringing etc



Mask-shift considerations for DPT



QRC 20nm extraction

20nm rules, litho bias/retargeting, multi-value SPEF

EPS – signoff power analysis

Multi-value SPEF support, DC/AC EM analysis

ETS – signoff timing analysis

Waveform effects, multi-value SPEF support

Summary

- Extraction Levels: Cell, Transistor, Substrate
- Parasitic Extractions: R, C, L, K
- Extraction Models
  - Device: SPICE
  - Interconnect: WLM, Field Solvers, Random Walks
- Total Delay:
  - Device Delay,
  - Interconnect Delay
- Parasitic and Delay Formats
  - SPEF, SDF