University of Chinese Academy of Sciences

Design Variations and Design for Yield

Design for Manufacturability

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June 25-29, 2018

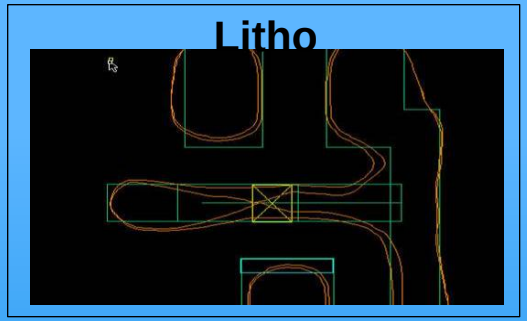
中国科学院大学2018年夏季

DFM for DFY

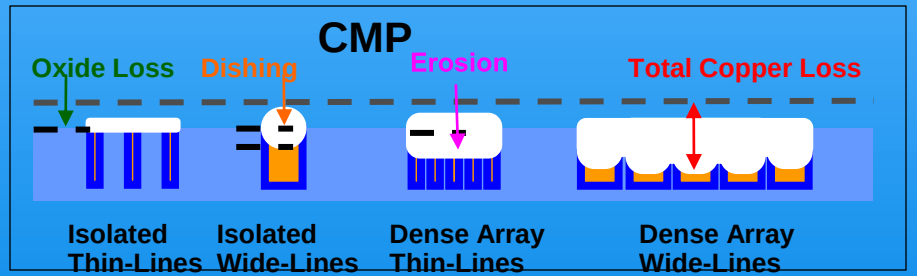
- **DFM wrt DRX**
- **CMP and DFM**
- **MPT of DFM**
- **EAD for DFM**
- **Discussion**

DFM Introduction - *What is Litho, CMP and Variability?*

- Litho
  - Problem: Specific DRC clean layout patterns cause resolution problems
  - Solution: Mandatory detection and fixing of litho hotspots from design by foundry certified litho solution



- CMP (Chemical Mechanical Polishing)
  - Problem: Copper metal erodes during manufacturing and create yield issue and impact interconnect RC
  - Solution: Mandatory detection of CMP hotspot using foundry certified CMP simulations



- Variability
  - Problem: Characteristics of devices vary with placement and density “Layout Dependent Effects (LDE)”
  - Solution: Include LDE in implementation to predict electrical variability across design by foundry certified e-DFM flows

Layout Dependent Effects		Prior to 40nm	At 40nm	28nm & Beyond
WPE	Well Proximity Effect	x	x	x
PSE	Poly Spacing Effect		x	X
LOD	Length of Diffusion	x	X	X
OSE	OD to OD Spacing Effect		x	X
LPC	Layout Patterning Check		x	x
OP/PO Density	OD/Poly Density		X	X

Design for Value*

Andrew Kahng, 2003

- Mask cost trend → **Design for Value (DFV)**

Design for Value Problem:

Given

- Performance measure *f*
- Value function *v(f)*
- Selling points f_i corresponding to various values of *f*
- Yield function *y(f)*

***Maximize* Total Design Value = Σ_i $y(f_i)*v(f_i)$**

[or, ***Minimize*** Total Cost]

- Probabilistic optimization regime

* See "Design Sensitivities to Variability: Extrapolation and Assessments in Nanometer VLSI", *IEEE ASIC/SoC Conference*, September 2002, pp. 411-415.

DFM in DSM since 2000

New Metal Density/CMP; Antenna Rules

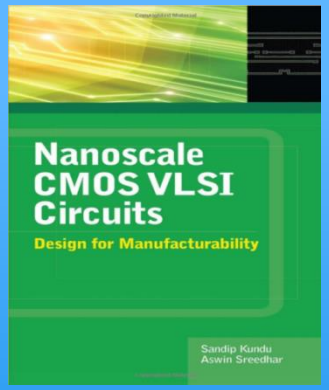
PSM, RET, and OPC

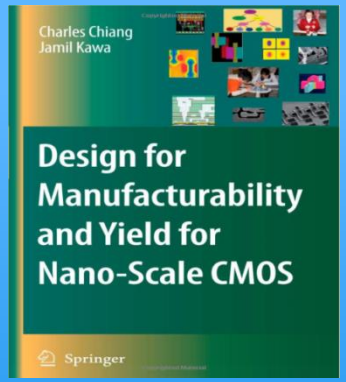
DFM in Below 20nm/FinFET

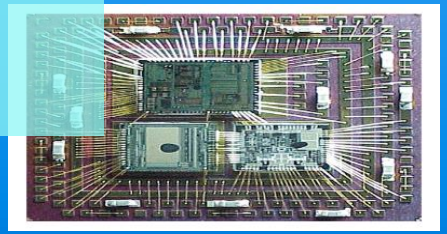
ITRS Predictions of DFM

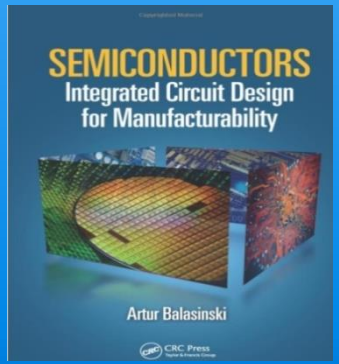
Requirements

Economic, Technologic









DFM for DFY

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- **CMP and DFM**
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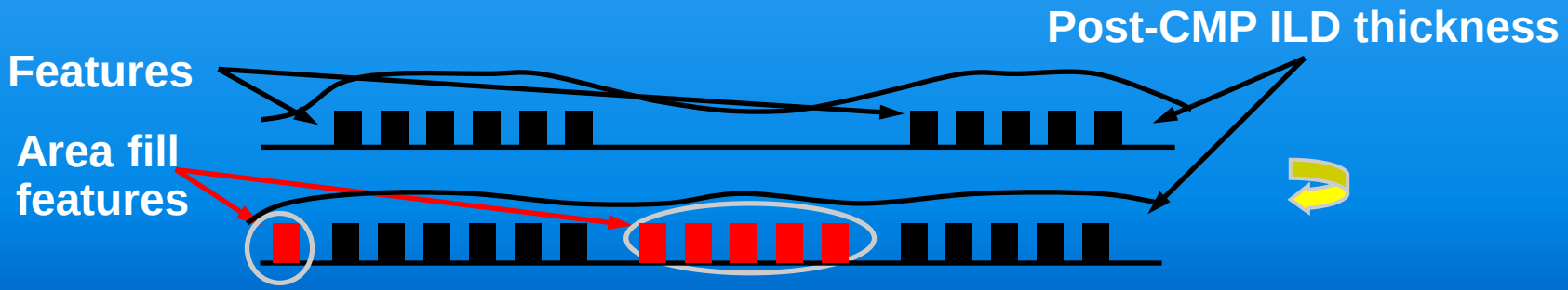
Layout Density Control

- Area fill: “electrically inactive”, floating or grounded
- Area fill insertion (and slotting)
  - Decreases local density variation
  - → Decreases post-CMP ILD erosion, conductor dishing
  - Cf. “Filling and Slotting: Analysis and Algorithms”, ISPD-98

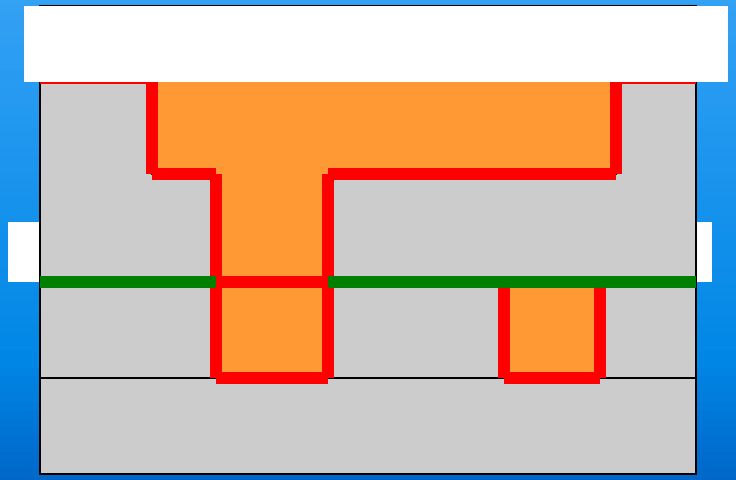


New Rule of Metal Density

- New rule: max/min metal density
  - For Cu, metals are “poured” (damascene)
  - Review of dual-damascene

Ta barrier layer
to prevent Cu from
diffusing into Si

SiN layer
for etch stop

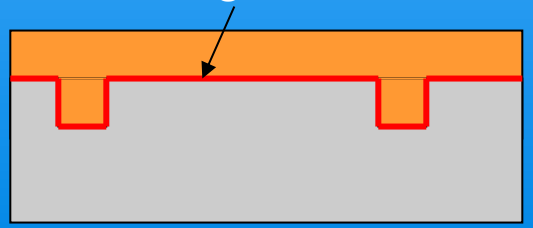


An amateur’s view of dual damascene (“via-first” variation)

Min/Max Rule of Metal Density

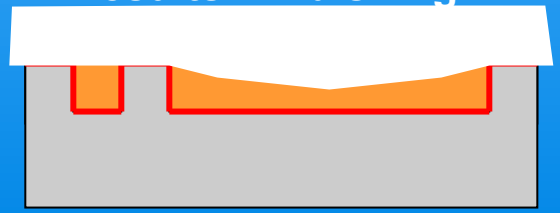
- Min rule: Ta barrier is hard to remove
- Max rule: Cu metal is much softer than Ta
- “Selectivity” of Cu is 20x higher than for Ta

Barrier tough to remove



Low density:
Mandate min. metal density

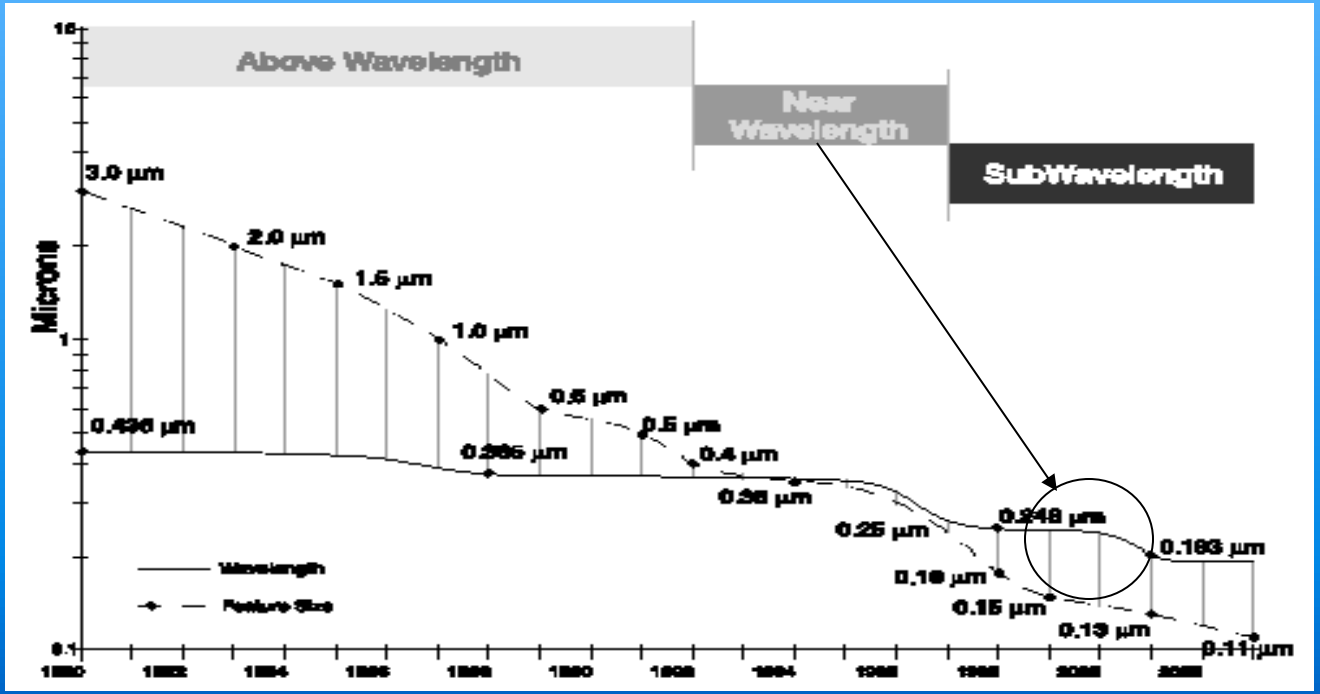
Softness of Cu results in “dishing”



High density:
Mandate max. density and width

Phase-Shifting Masks (PSM)

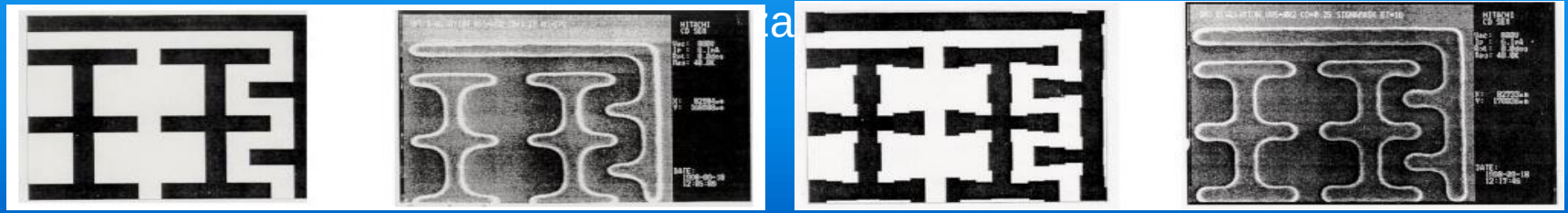
- Lithography uses (partially) coherent light
  - Wavelength today is 248nm; changes slowly



Kahng et. al., 1999 DAC

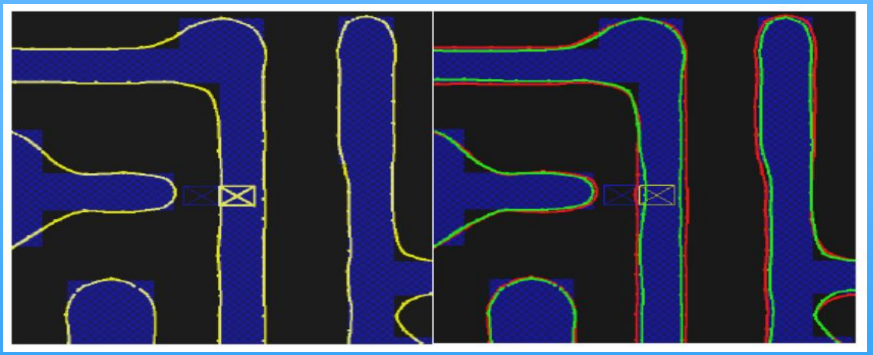
Optical Proximity Correction (OPC)

- Also known as serifs and dog-ears
  - Layout is not WYSIWYG anymore
- Patterning through a reticle is tough
  - Holes in reticle act as low-pass filter
    - Blurred edges
    - Squares in mask are blobby ovals in production
  - We can predistort the image to compensate



Schellenberg et. al., 1999 SPIE

Automated Full-Chip Hotspot Detection



SPIE 2007, Roseboom et al
Contours and Hotspots on a 65nm Metal1 Layout
(a) Contours at Nominal Conditions
(b) Contours and Hotspots at Defocus Conditions

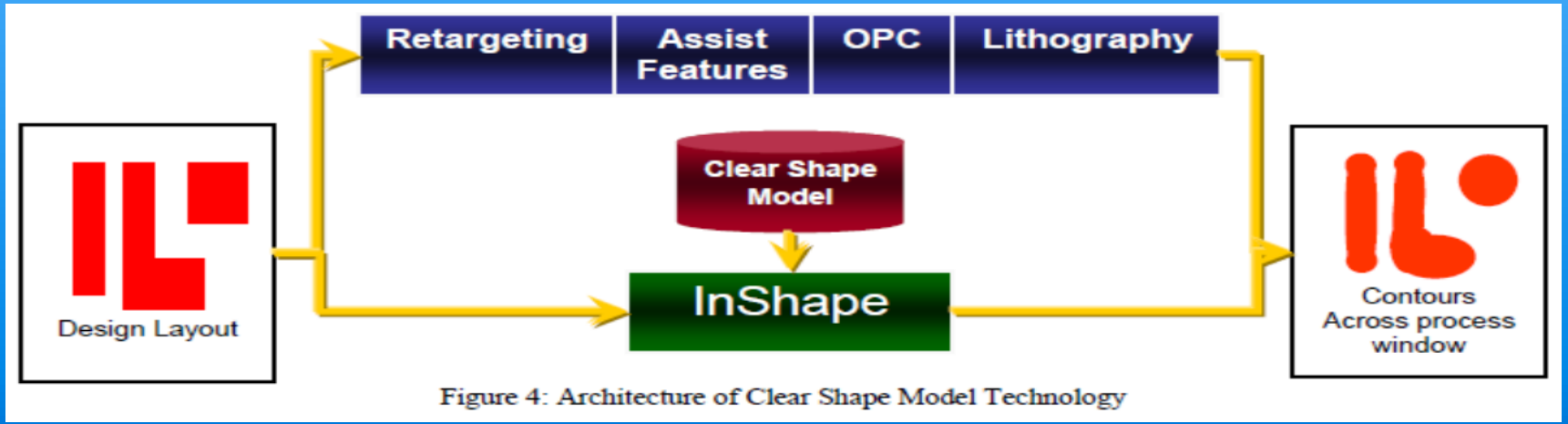


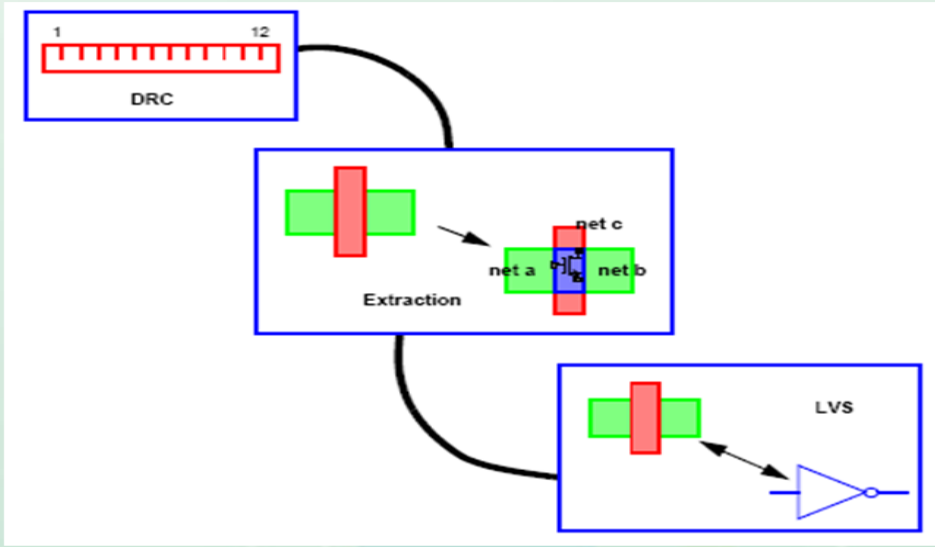
Figure 4: Architecture of Clear Shape Model Technology

SPIE 2007, Roseboom et al, Architecture of Clear Shape Model Technology for RET/OPC/ORC Manufacturing Flow

20nm Implementation and Signoff Physical Verification

Physical Implementation | Physical/DFM Signoff | Tapeout

- **Basic Concepts**
  - Design rule checks (DRC)
  - Layout versus schematic (LVS)
- Verification Methods
  - DRC, LVS, ERC,
  - SVL, LVL, LPE
- Tools
  - Dracula, Diva, Assura,
  - Calibre, Hercules, PVS



used in Virtuoso custom design

DFM for DFY

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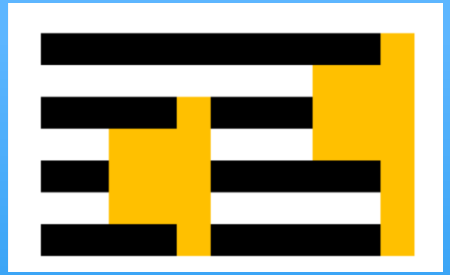
Multiple Patterning Technology in Lithography

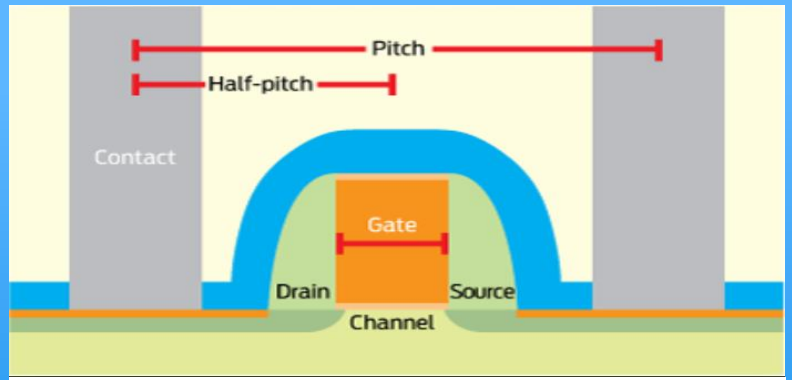
- MPT: DPT, TPT, QPT
- SADP, SATP, SAQP
- Self-aligned contact/via patterning
  - used in DRAM
- SID (*Spacer-is-Dielectric*) SADP (*to replace LELE*)
- DSA ()
- LELE
  - LELE (*Litho-Etch-Litho-Etch*), used in 20nm/14nm
  - LELELE, used in 10/7nm



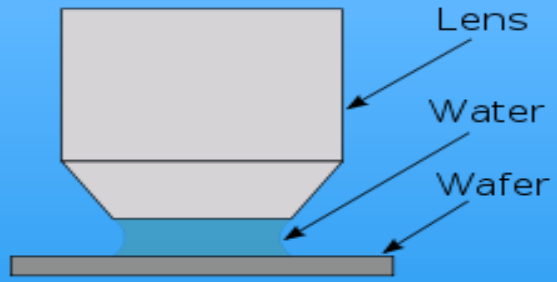
MPT and DPT Application in IC

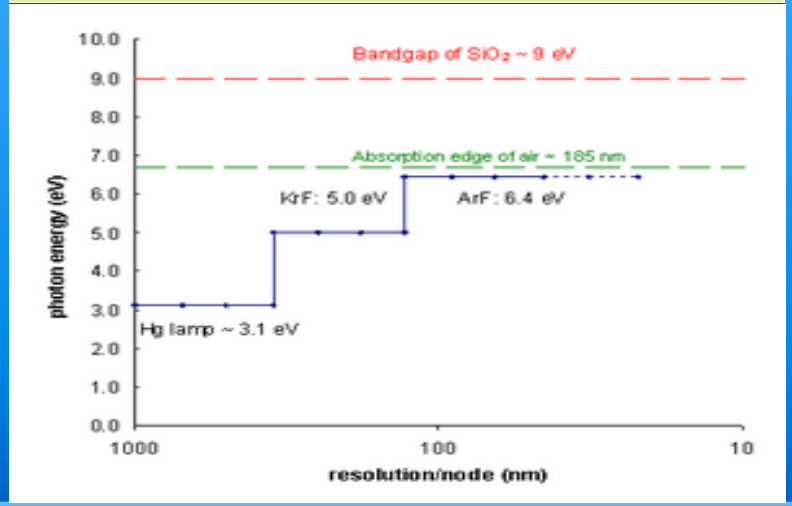
- MPT vs EUV
  - LELE – Litho-Etch-Litho-Etch (DPT)
    - 28nm-40nm, LELE with half-pitch
    - 20nm-14nm, LELE
  - SAS - Self-Aligned Spacer
    - 20nm-28nm, SAS with half-pitch
    - 10nm-14nm, SAS
  - Quadruple Patterning Technology (QPT)
    - sub-20nm, QPT with half-pitch
    - beyond 10nm, QPT
      - EUV with MPT at 7nm and beyond
      - SID (Spacer-Is-Dielectric) patterning
      - DSA (Directed self-Assembly)
- Ref.:
  - E. van Setten et al., SPIE 9661, 96610G (2015)
  - http://www.eetimes.com/document.asp?doc_id=1327919 EUV 5nm test

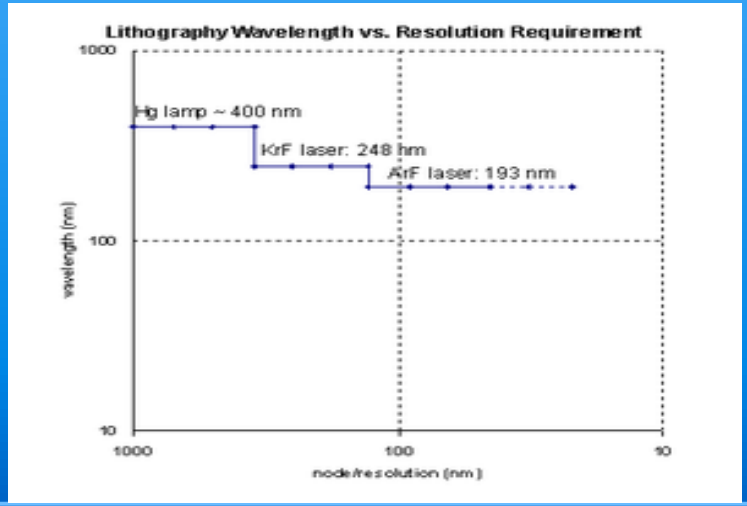
Dry UV and Immersion UV



$$CD = k_1 \cdot \frac{\lambda}{NA}$$



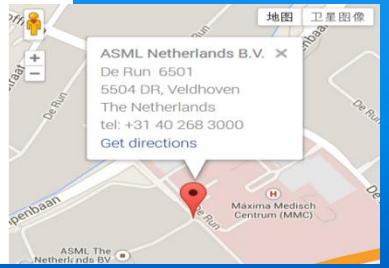




EUV (extreme ultraviolet) for 10nm

436nm → 365nm → 248nm KrF → 193nm ArF Immersion (200W/cm^2) → 13.5nm CO_2 EUV (10^{11}W/cm^2)

NXE:3300B @13.5nm, ASML/Cymer Generation 1 “” [by Cymer]
LPP (***Laser-Produced Plasma***) 55W for 43 wafer/hr in 2013;
250W for 126 wafer/hr by 2015



Chip Optimizer for DFY/DFM Solutions

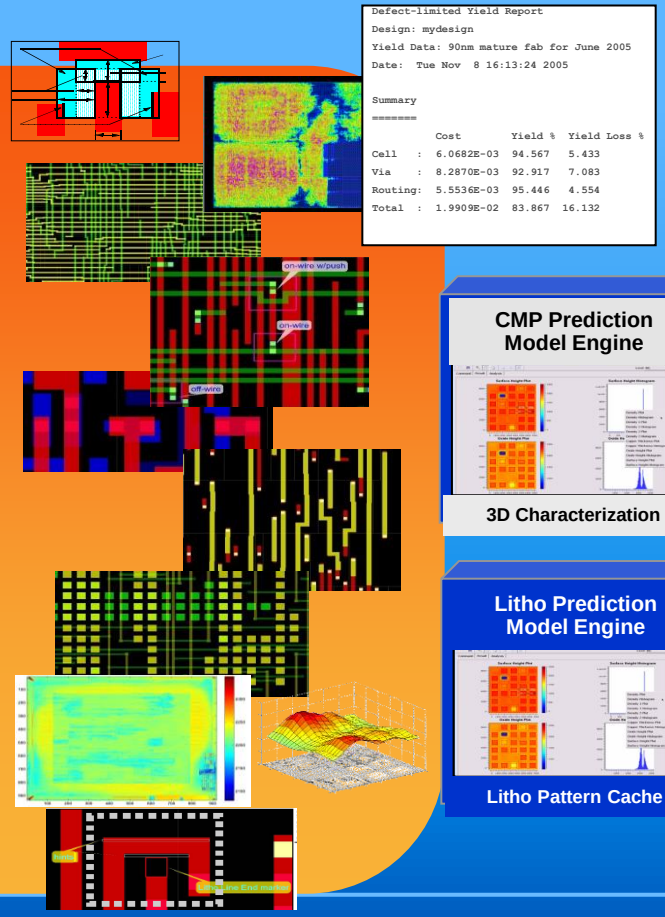
SoC Encounter

Electrically Aware (In-core QRCX & CTE)

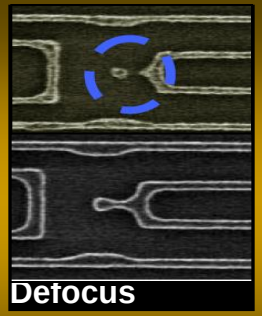
Space-based Router

Chip Optimizer

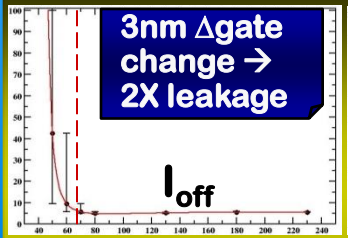
- Incremental, Automated DRC/Recommended Rule Optimization or ECO Routing
- Via Reduction
- Wire Spreading & CAA Optimization
- Wire Topology Optimization
- Via Optimization
- Wire Widening
- Pwr/Gnd Optimization
- Dummy Fill
- CMP Model-based Fill
- Incremental, Automated Litho Repair

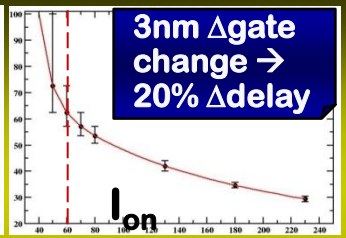


65/45 nm Design-Related Manufacturing Failures Cause Yield Loss and Respins

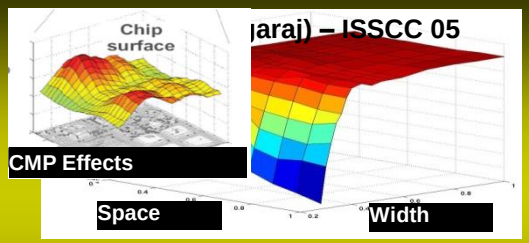


Catastrophic Failures Impact Yield





Transistor delay and leakage non-linear variation with gate length variations



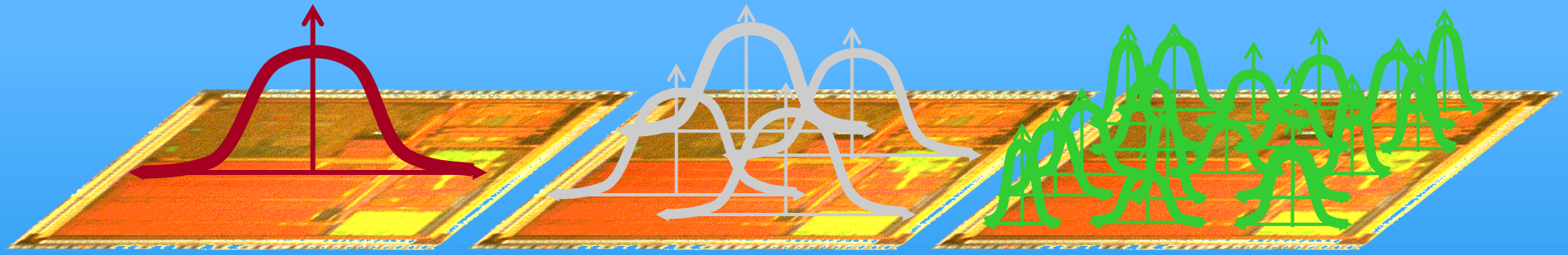
Wire Δwidth creates non-linear RC Δdelay

Manufacturing variations cause leakage and delay failures

- **DRC is not sufficient anymore**
- Risk poor utilization of process or costly re-spins
- **Need to prevent catastrophic failures 'during' design**

- ⑩ **Increased sensitivity to variations on both devices and interconnect**
- ⑩ **Current margins and rule-based method insufficient**
- ⑩ **Need silicon accurate timing and leakage analysis**

OutPerform Reduces Guard-bands and Detects New Parametric Failures



All variations – systematic, random etc., - lumped together

Table-based solutions try to account for systematic variations in interconnect

Manufacturing Integrity analysis reduces guard-bands and detects new failures

Pessimism | **Pessimism** | **Pessimism**

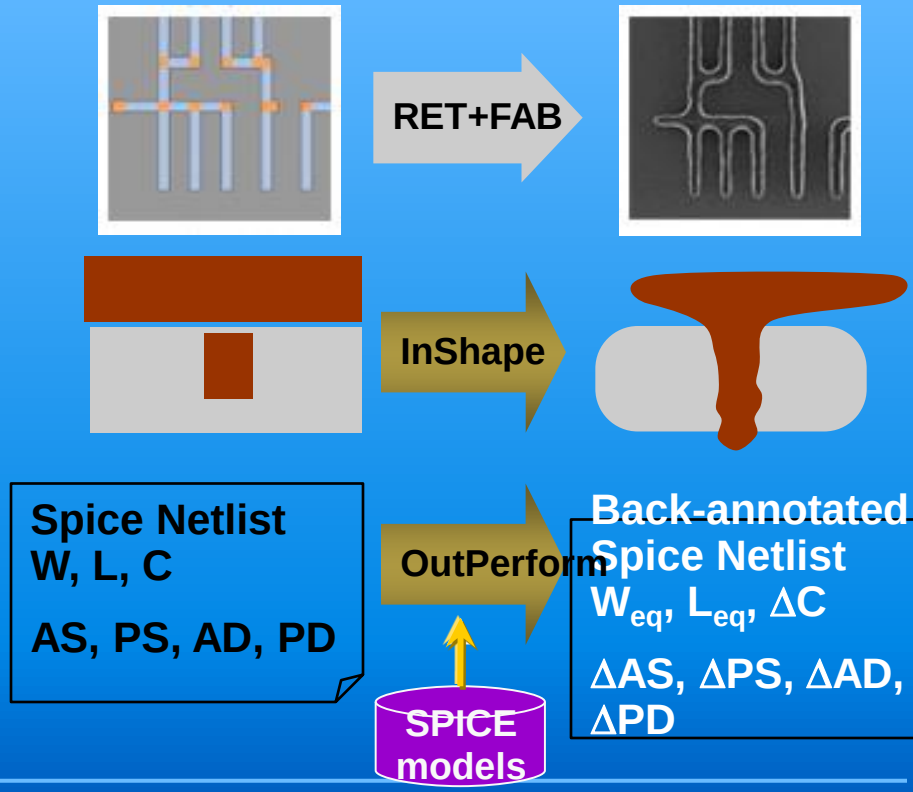
Timing/Noise/Power Checks ☆ ☆

Timing/Noise/Power Checks ☆ ☆ ☆

Timing/Noise/Power Checks ☆ ☆ ☆ ☆ ☆

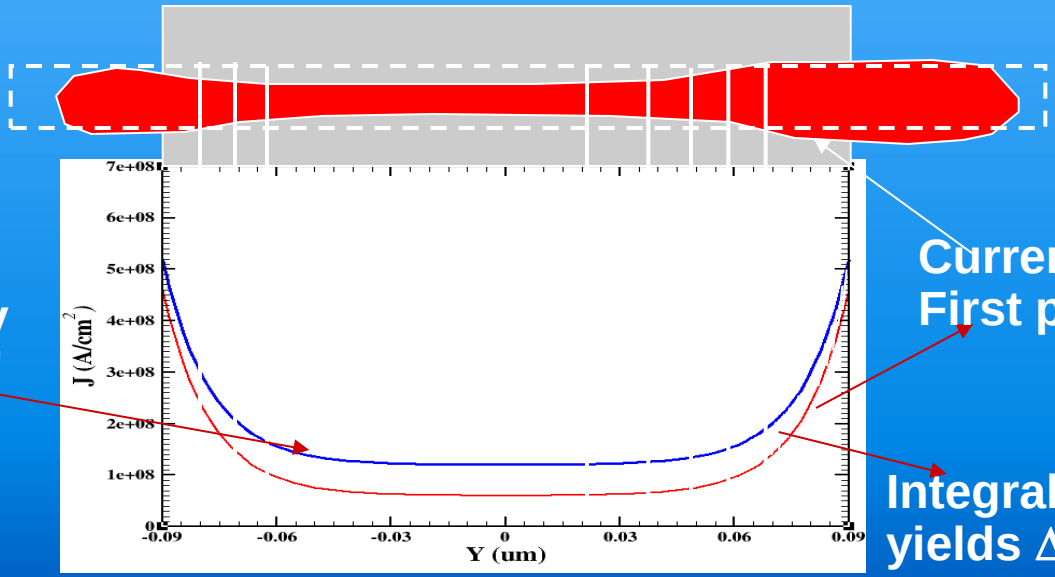
OutPerform Accounts for Manufacturing Integrity Issues on Device

- Proprietary incremental device parameter extraction algorithms
- Predict current density across channel from SPICE models and extract equivalent W/L
  - Equivalent I_{on} for delay
  - Equivalent I_{off} for leakage
- Formulated as perturbation problem
  - Back-annotated transistor SPICE netlist



Proprietary L transformation

- Current varies non uniformly over channel width
- Divide into multiple partitions across channel
- Find current for each partition
- Sum to get total current = Find L_{eff} to match current

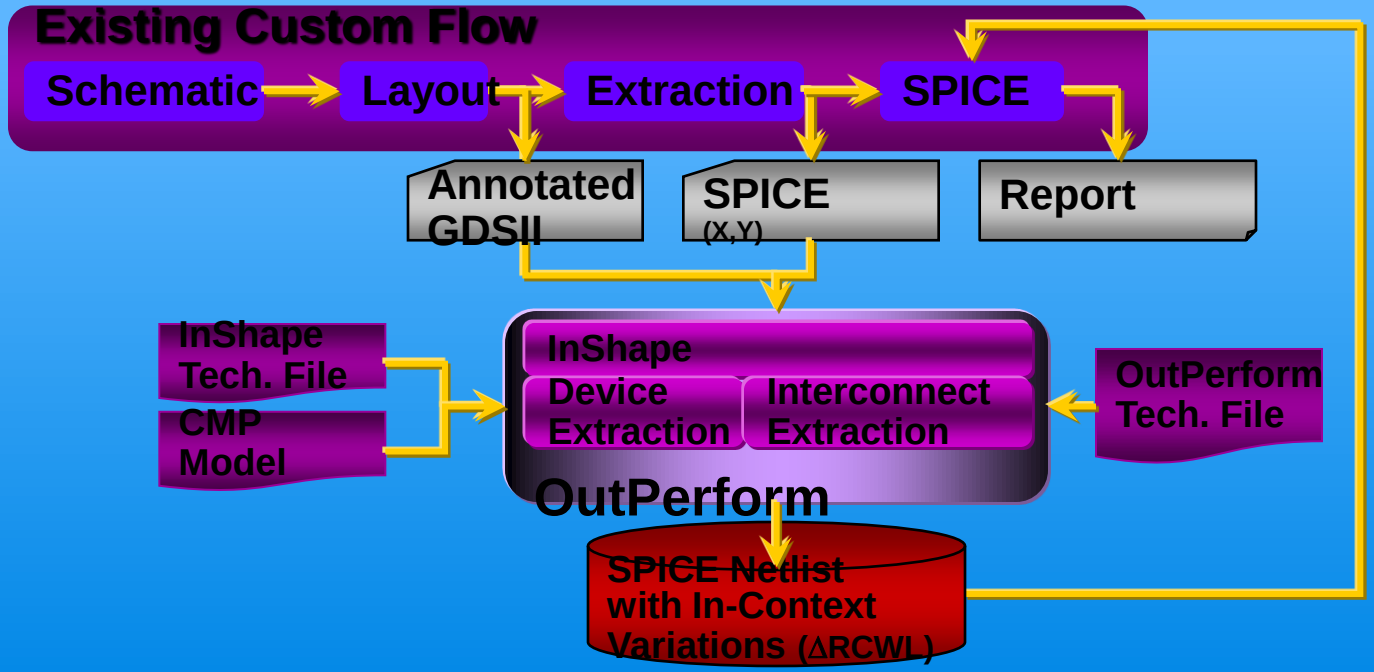


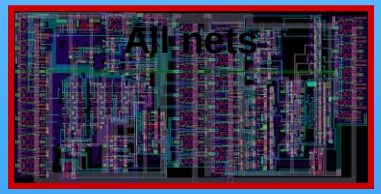
Current density for Original "L"

Current density for First partition

Integral of difference yields ΔI_{ds} for partition

OutPerform : In-Context Performance Integrity Flow In Custom Design





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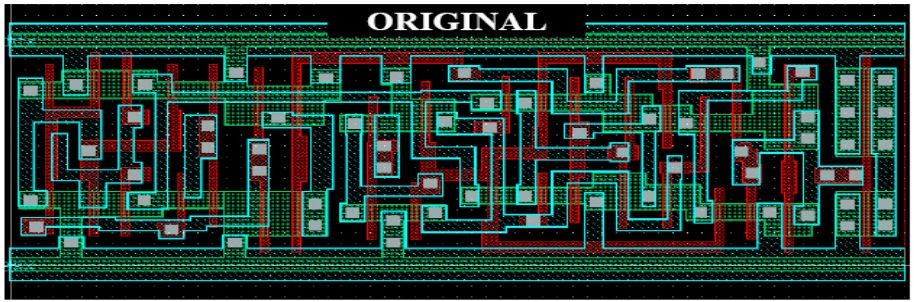
- Produce back-annotated SPICE netlist with W_{eq}, L_{eq}, ΔR, ΔC
- Predicts impact of actual silicon shapes on device and interconnect
- Simulation of back-annotated netlist in SPICE shows timing impact of manufacturing variations

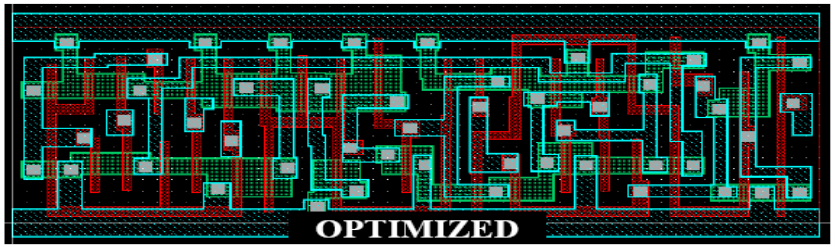
Clear Shape Enables Reduction in Area(10%), Power (up to 9%) and Leakage (up to 24%)

SPIE Advanced Lithography

Physical DFM Application for Libraries



- Used conservative design rules
- Routing grid larger than minimum routing pitch
  - Larger via enclosure and spacing rules.
- Moving L-shaped poly and diffusion away from MOS gates



- More aggressive rules enabled by:
  - Usage of model-based simulation to detect and fix hotspots
  - Process maturity

17% cell area reduction
10% block area reduction

Block	Die area reduction	Dynamic power reduction	Leakage power reduction
"A"	10.1%	5.2%	4.8%
"R"	14.0%	9.0%	24.2%

QUALCOMM CDMA Technologies

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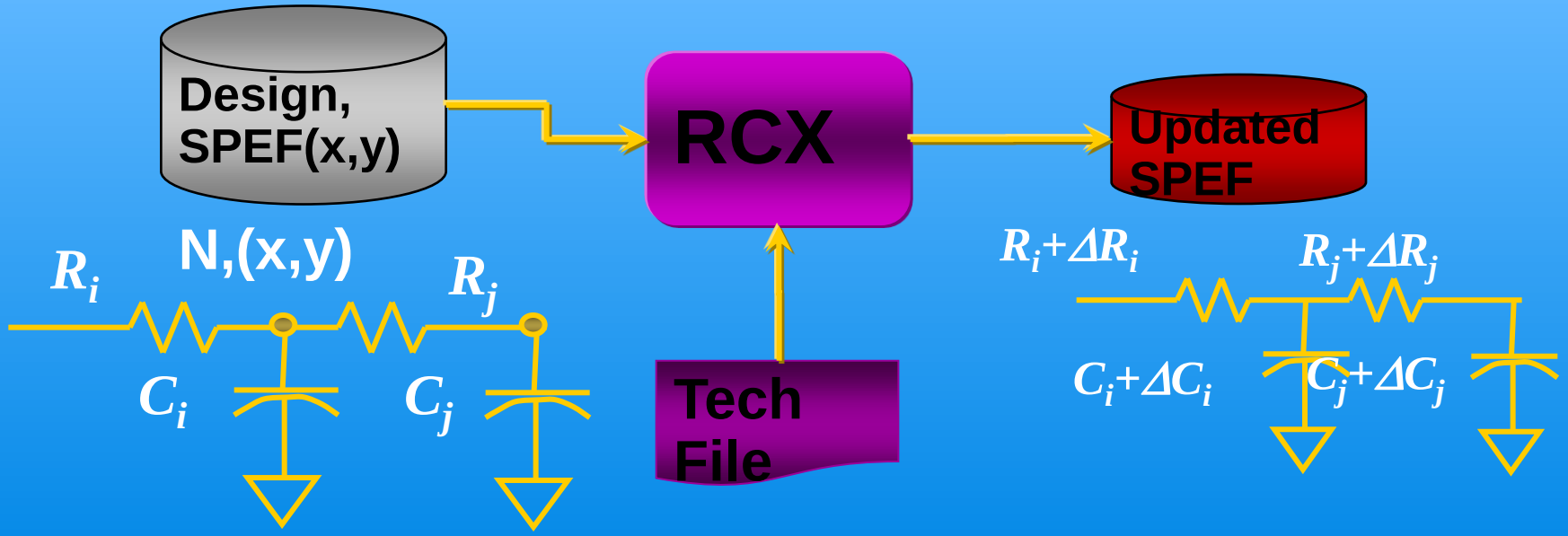
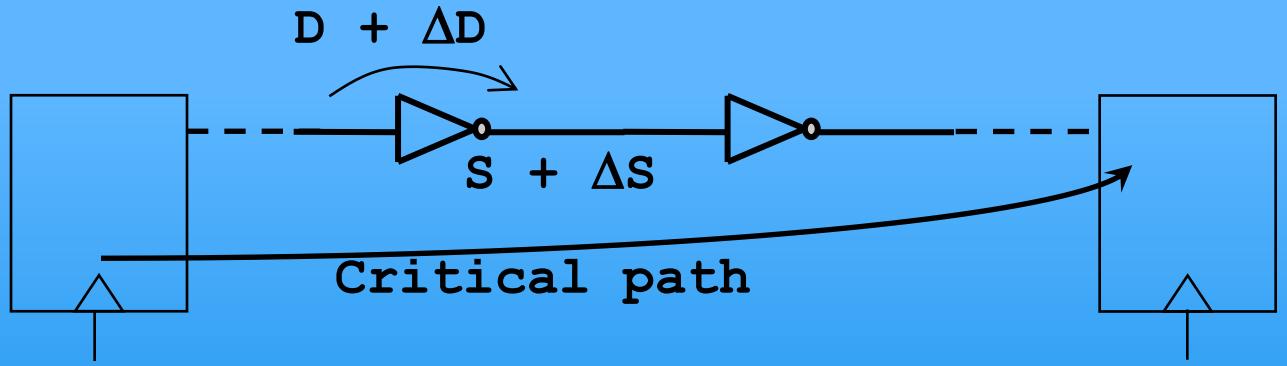
clear shape technologies

RCX – Interconnect Extraction



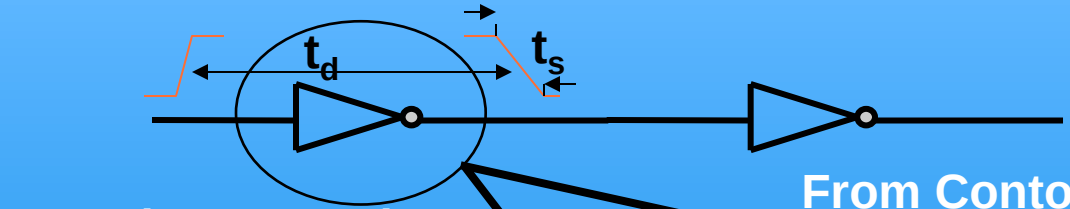
Extracts ΔR and ΔC due to shape variations and updates the original SPEF

Delay Calculation

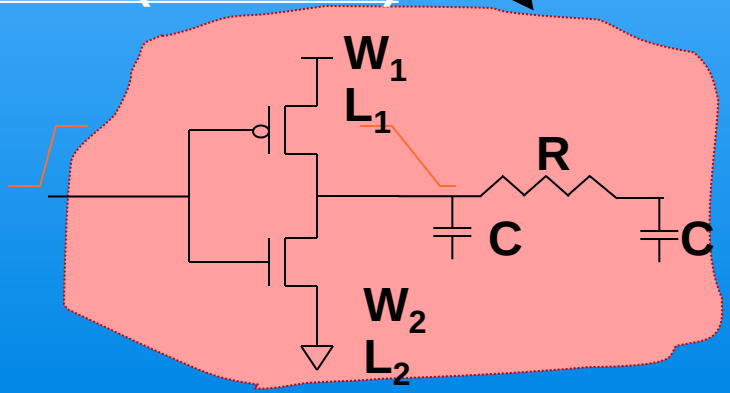


- ΔL, ΔW and ΔR, ΔC variation affects both delay and slew
- Δslew affects downstream logic delay
- Δslew and Δdelay on the clock network affects the entire design
- OutPerform takes into account the Δslew, device delta, and parasitic delta and calculates Δdelay for gates
- Δdelay for interconnect factors the Δslew and parasitic delta

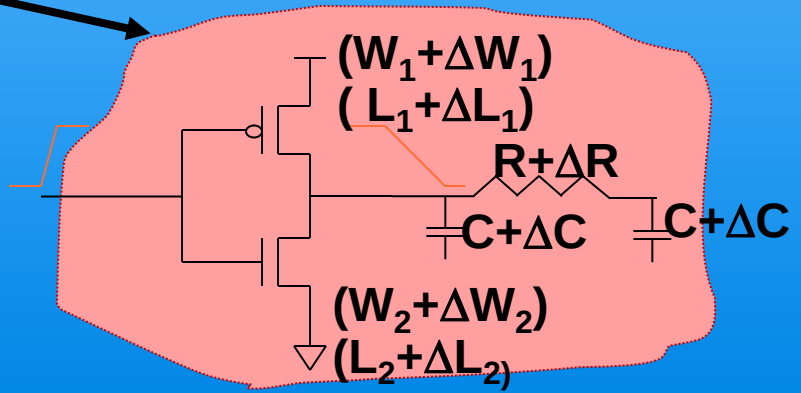
Bringing Manufacturing Variations into Timing Analysis



Worst Case (Best Case)

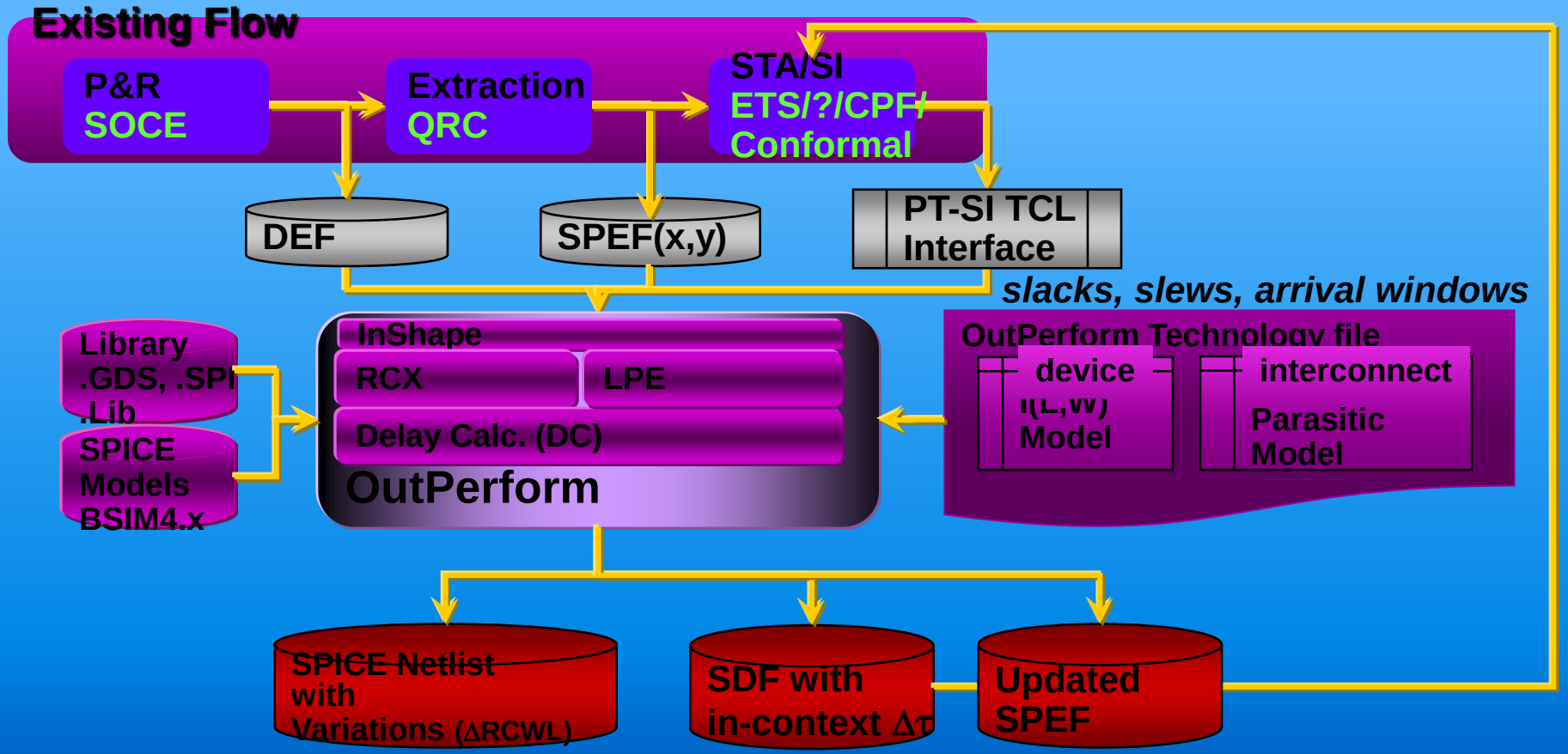


From Contours (ΔL, ΔW, ΔR, ΔC)



Simulate circuit with worst-case (best-case) parameters and contour-extracted parameters

OutPerform: Variation Analysis in ASIC flow



DFM for DFY

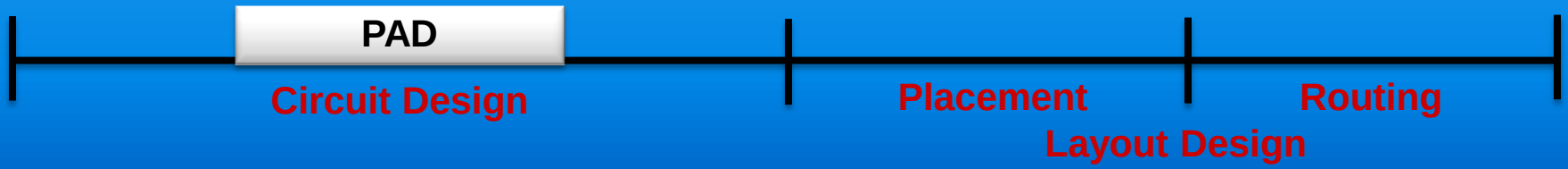
- DFM wrt **DFX**
- **CMP and DFM**
- **MPT of DFM**
- **EAD for DFM**
- **Discussion**

Definitions

- PAD = Parasitic Aware Design
- RAP = Rapid Analog Prototyping
- LDE = Layout Dependent Effects
- EAD = Electrically Aware Design
- VSE = Virtuoso Schematic Editor (CAS)
- ADE = Analog Design Environment (CAS)
- VLS = Virtuoso Layout Suite (CAS)
- PVS = Physical Verification System (SSV)
- QRC = Cadence Extraction (SSV)
- LEA = Litho Electrical Analyzer (SSV)

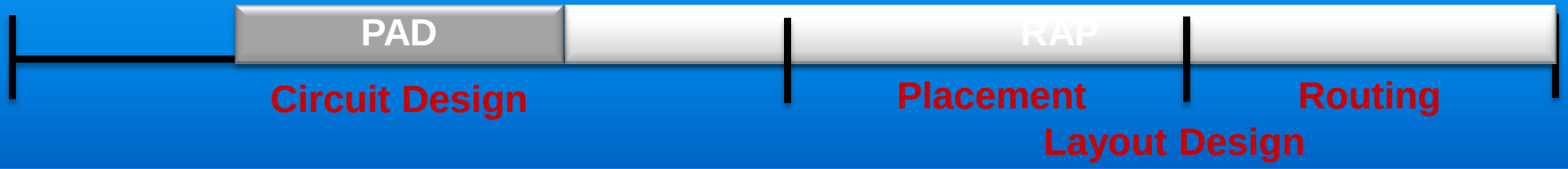
PAD

- Parasitic Aware Design
  - Allows designers to estimate parasitic effects without any layout
  - Highlights
    - Run simulations with estimated parasitics across multiple testbenches and corners
    - Perform parasitic sweeps and specify constraints (max R, max C, max Coupling C, matched C) to drive layout generation
    - Perform sensitivity analysis and Monte Carlo analysis in the presence of these parasitics



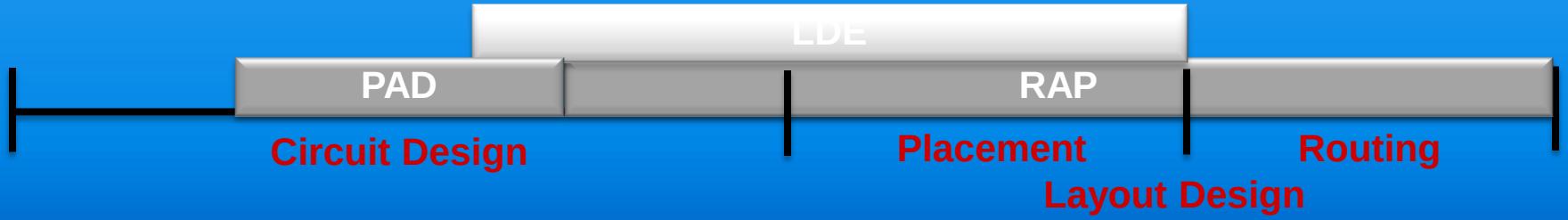
RAP

- Rapid Analog Prototyping
  - Allows designers to very quickly and automatically capture constraints for a circuit architecture
  - Constraints include
    - Module Generators – allows for highly matched array of devices with abutment, merging, guard rings etc.
    - Symmetry, Orientation, Matching etc..
  - These constraints can drive a prototype layout generation using the auto-placer and auto-router
  - *Goal is to get a layout as quickly as possible for getting access to physical effects as quickly as possible*



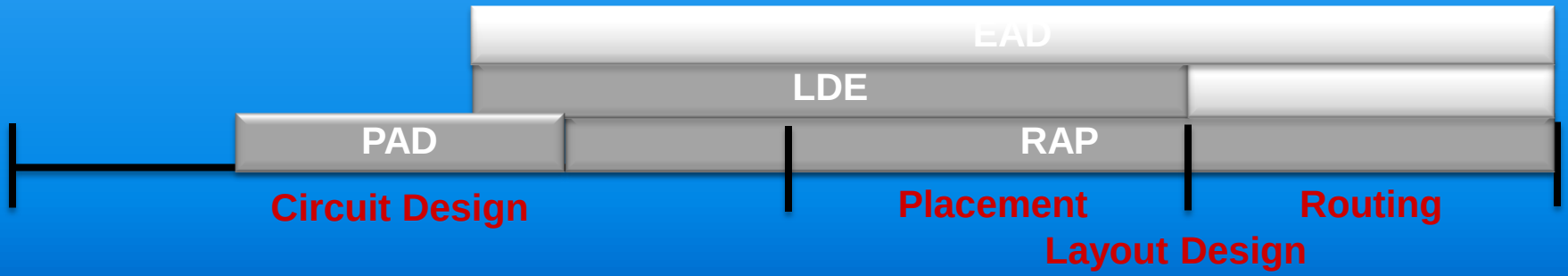
LDE

- Layout Dependent Effects
  - Circuit Designer can extract accurate LDE effects from Module Generators or a placement to re-simulate in the presence of these effects
  - Layout Engineer can perform LDE hotspot analysis in the layout during placement to identify any problem areas in your circuit
  - *Note: While RAP can provide inputs for the LDE flow, it is not a requirement for using the LDE flow*



EAD

- Electrically Aware Design
  - Supports RC extraction on interconnect
  - Supports EM analysis on interconnect while routing
    - Currents are captured during circuit design phase
  - Supports re-simulation with parasitic effects during circuit design while layout is being generated

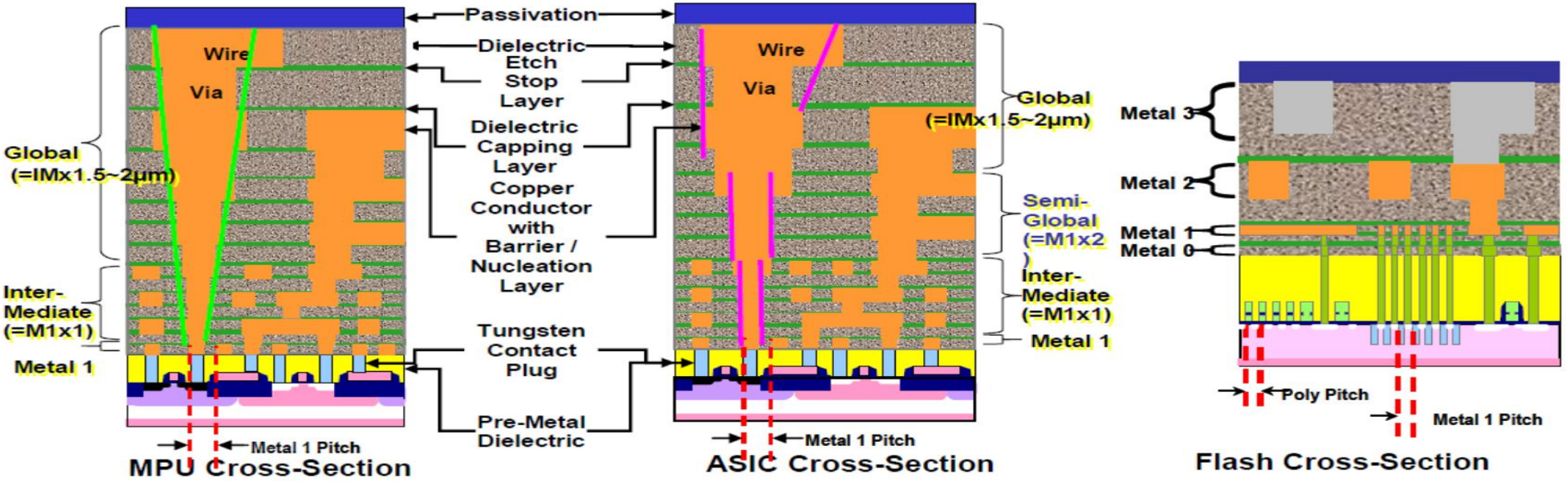


DFM for DFY

- DFM wrt **DFX**
- **CMP and DFM**
- **MPT of DFM**
- **EAD for DFM**
- **Discussion**

DFM Requirements by ITRS 2011

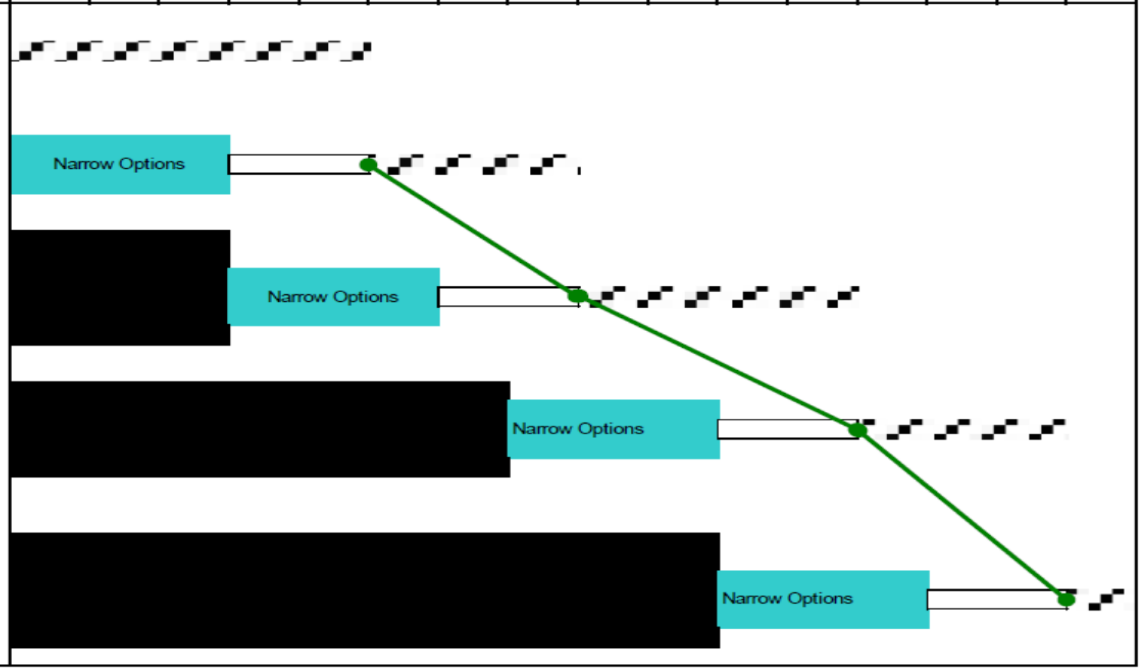
- Requirements due to fundamental economic limitations
  - Mask cost towards multi $M, for SoC innovation
- Requirements due to variability and lithography limitations



MPU and DRAM Metal Level Potential Solutions

ITRS 2013

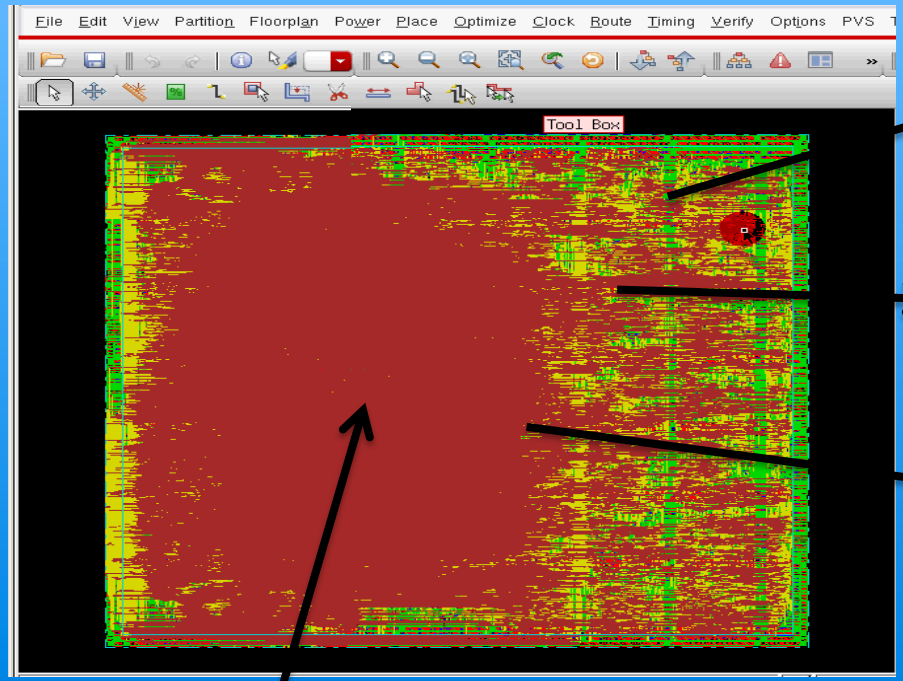
Minimum 1/2 Pitch	Production Year	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
	Minimum lithographically defined half pitch in production in nm (driven by DRAM, MPU metal)	28	26	24	22	20	18	17	15	14	13.0	11.9	10.9	10.0	8.9	8.0	7.1
30nm to 20nm	193nm DP																
< 20nm to 15nm	193nm QP EUV DSA																
< 15nm to 11nm	193 QP EUV DP EUV extension such as high NA DSA ML2 Imprint																
< 11nm to 8nm	EUV DP EUV Extension such as high NA DSA ML2 Imprint																
sub 8nm	EUV extension such as high NA and DP EUV QP DSA Extension ML2 Imprint Innovation																

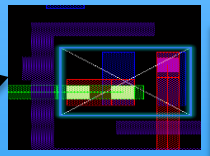


Legend indicates the time frame in which research, development, and qualification/pre-production should be taking place for a given half pitch range for the solution.

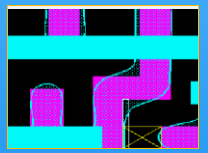
Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

Summary: In-Design DFM in Encounter Digital Implementation System

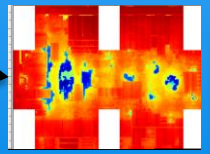




Pattern-Based DRC+



Model-Based Litho Check



Model-Based CMP Analysis

Layout Dependent Effect-Aware Placement and Timing Analysis

Summary

- DFM challenges are from
  - Increasing variability
  - Mask cost
  - Data explosion
  - Lithography hardware limitations
- They (may) impact on
  - Architecture challenges
  - Logic and circuit challenges
  - Layout and physical design challenges
  - Yield prediction and optimization as design challenges