数字电子技术作业(五)

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6.2.4 试分析图题 6.2.4 所示电路，列出状态转换表，并画出状态转换图。当输入序列A为01011011111111101,其输出序列 Z 是什么？该电路可以检测 A 的何种输入序列？

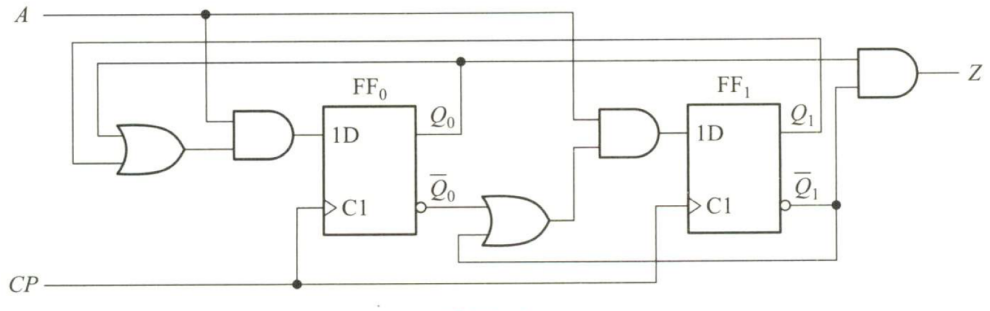


图 1: 6.2.4

解：

Step 1. 写出输出方程，激励方程，状态方程：

$$Z = Q_0\overline{Q}_1, \begin{cases} D_{FF_0} = A(Q_1 + Q_0) \\ D_{FF_1} = A(\overline{Q}_0 + \overline{Q}_1) \end{cases}, \begin{cases} Q_0^{n+1} = A(Q_1^n + Q_0^n) \\ Q_1^{n+1} = A(\overline{Q}_0^n + \overline{Q}_1^n) \end{cases}$$

Step 2. 列出状态转换表

$Q_0^nQ_1^n$	$Q_0^{n+1}Q_1^{n+1}/Z$	
	A=0	A=1
00	00/0	01/0
01	00/0	11/0
10	00/1	11/1
11	00/0	10/0

Step 3. 画出状态转换图

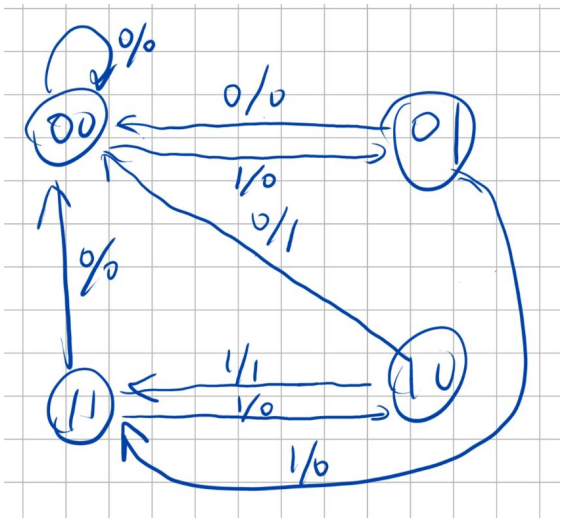


图 2: 6.2.4

输出序列为：0000 0000 0100 0101 0100，可以检测连续的三个1，若连续的三个1之后每跟着两个1就输出一个1，只要有0重新检测。

6.2.6 试分析图题 6.2.6 所示同步时序电路，写出激励方程组、状态转换方程组和输出方程，列出状态转换表并画出状态转换图。

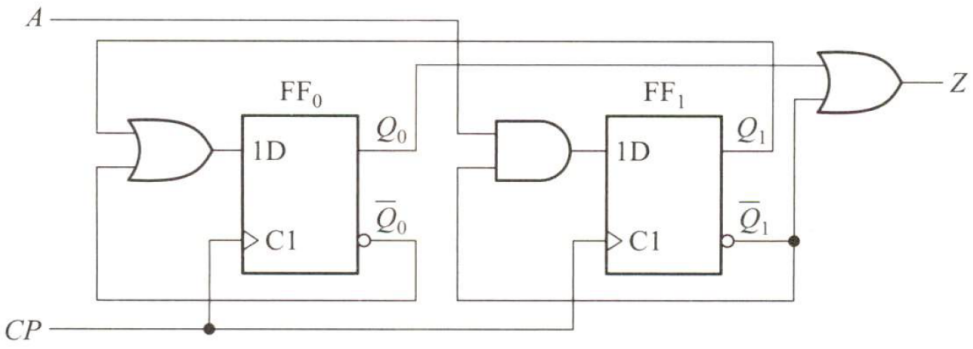


图 3: 6.2.6

解：

Step 1 写出输出方程，激励方程，状态方程：

$$Z = Q_0 + \overline{Q}_1, \begin{cases} D_{FF_0} = Q_1 + \overline{Q}_0 \\ D_{FF_1} = A\overline{Q}_1 \end{cases}, \begin{cases} Q_0^{n+1} = Q_1^n + \overline{Q}_0^n \\ Q_1^{n+1} = A\overline{Q}_1^n \end{cases}$$

Step 2 列出状态转换表

$Q_1^nQ_0^n$	$Q_1^{n+1}Q_0^{n+1}/Z$	
	A=0	A=1
00	01/1	11/1
01	00/0	10/0
10	01/1	01/1
11	01/1	01/1

Step 3. 画出状态转换图

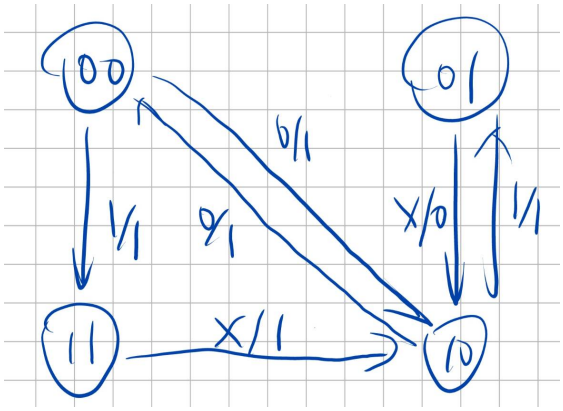


图 4: 6.2.6

6.3.5 试用下降沿触发的JK触发器和最少的门电路，实现图题 6.3.5 所示的Z_1和Z_2输出波形(要求写出Verilog程序)

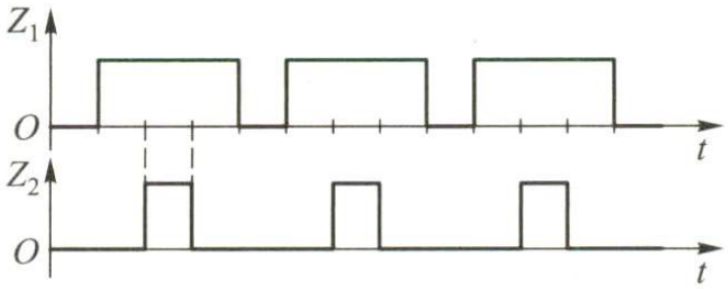


图 5: 6.3.5

解：

Step 1. 逻辑抽象

从图6.3.5所示输出波形图可以看出，对于每一个周期，可分为4个状态：$Z_2Z_1=00, Z_2Z_1=01, Z_2Z_1=11, Z_2Z_1=01$。设定为4个状态：00,01,10,11,用两个下降沿触发的 JK 触发器实现.设两个触发器的状态为 Q_1、 Q_0,输出信号为Z_1, Z_2

Step 2. 列写激励方程，输出方程

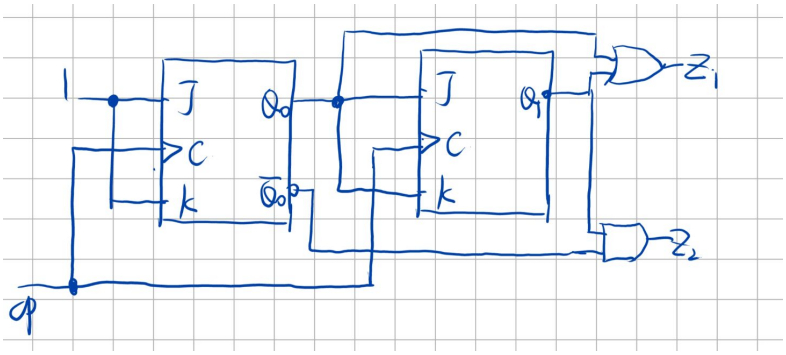
首先写出真值表：

$Q_0^nQ_1^n$	$Q_0^{n+1}Q_1^{n+1}$	Z_1Z_2	J_0	K_0	J_1	K_1
00	01	00	1	x	0	x
01	10	10	x	1	1	x
10	11	11	1	x	x	0
11	00	10	x	1	x	1

易得激励方程和输出方程：

$$\begin{cases} J_1=K_1=Q^{\check{}}0 \\ J_0=K_0=1 \end{cases}, \begin{cases} Z_1=Q_1+Q_0 \\ Z_2=Q_1\overline{Q}_0 \end{cases}$$

Step 2. 画出逻辑电路，写出Verilog语句




```
module sol(input clk,
    output reg Z_1,
    output reg Z_2);
    reg[1:0] state;
    parameter S0=2'b00, S1=2'b01, S2=2'b10, S3=2'b11
    always@(posedge clk)begin
        case(state)
            S0:begin
                state=S1;Z_1=0;Z_2=0;
            end
            S1:begin
                state=S2;Z_1=1;Z_2=0;
            end
            S2:begin
                state=S3;Z_1=1;Z_2=1;
            end
            S3:begin
                state=S0;Z_1=1;Z_2=0;
            end
            default:begin
                state=S0;
            end
        endcase
    end
endmodule
```

6.3.6 试用上升沿触发的*D*触发器设计一个1101序列检测器(序列可重复),输入为串行编码序列，输出为检出信号(要求写出Verilog程序) 解：

Step 1. 逻辑抽象

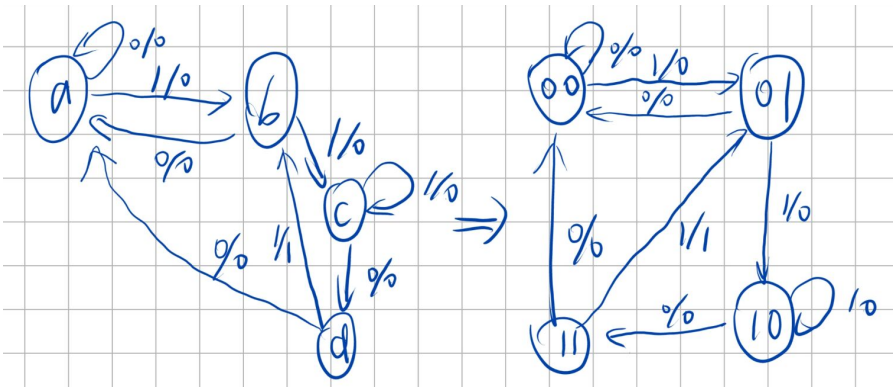
首先写出状态转换图和状态转换表

Q^n	Q^{n+1}/Y	
	$A=0$	$A=1$
a	a/0	b/0
b	a/0	c/0
c	d/0	c/0
d	a/0	e/1
e	a/0	c/0

Step 2. 状态化简

Q^n	Q^{n+1}/Y	
	$A=0$	$A=1$
a	a/0	b/0
b	a/0	c/0
c	d/0	c/0
d	a/0	b/1

Step 3. 状态分配

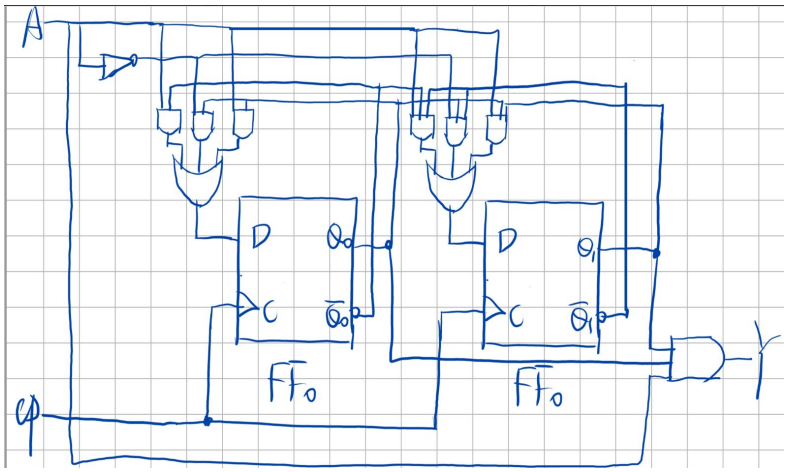


$Q_0^nQ_1^n$	$Q_0^{n+1}Q_1^{n+1}/Y$	
	$A=0$	$A=1$
00	00/0	10/0
01	00/0	10/0
10	11/0	10/0
11	00/0	01/1

Step 4. 列写激励方程，输出方程

$$\begin{cases} D_0 = A\overline{Q}_0Q_1 + \overline{A}Q_0\overline{Q}_1 + AQ_0\overline{Q}_1 \\ D_1 = A\overline{Q}_0\overline{Q}_1 + \overline{A}Q_0\overline{Q}_1 + AQ_0Q_1 \end{cases}, Y = AQ_0^nQ_1^n$$

Step 5. 画出逻辑电路，写出Verilog语句




```
module sol(input clk, input A, output reg Y);
    reg[1:0] state;
    parameter S0=2'b00, S1=2'b01, S2=2'b10, S3=2'b11
    always@(posedge clk)begin
        case(state)
            S0:begin
                if (A==0){state=S0;Y=0;}
                    else {state=S2;Y=0;}
            end
            S1:begin
                if (A==0){state=S0;Y=0;}
                    else {state=S2;Y=0;}
            end
            S2:begin
                if (A==0){state=S3;Y=0;}
                    else {state=S2;Y=0;}
            end
            S3:begin
                if (A==0){state=S0;Y=0;}
                    else {state=S1;Y=1;}
            end
        endcase
    end
endmodule
```