XR871 Datasheet

A Single-Chip Wireless MCU for Wi-Fi and Internet-of-Things Applications

Revision 1.0

May 8, 2017

Declaration

THIS DOCUMENTATION IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF XRADIO TECHNOLOGY ("XRADIO"). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF XRADIO AND GIVE CLEAR ACKNOWLEDGEMENT TO THE COPYRIGHT OWNER.

THE INFORMATION FURNISHED BY XRADIO IS BELIEVED TO BE ACCURATE AND RELIABLE. XRADIO RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE. XRADIO DOES NOT ASSUME ANY RESPONSIBILITY AND LIABILITY FOR ITS USE. NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF XRADIO. THIS DATASHEET NEITHER STATES NOR IMPLIES WARRANTY OF ANY KIND, INCLUDING FITNESS FOR ANY PARTICULAR APPLICATION.

THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. XRADIO SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. XRADIO SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.

Revision History

Version	Data	Summary of Changes
1.0	2017-5-9	Initial Version

Table 1-1 Revision History

Contents

Tables

Figures

1 Overview

1.1 General Description

XR871 is a highly integrated low-power WLAN Microcontroller System-on-Chip (SOC) solution designed for Internet of Things (IoT), Wearable equipment, Machine-to-Machine (M2M), Home automation, Cloud Connectivity and Smart Energy applications.

The XR871 application subsystem is powered by an ARM Cortex-M4F CPU that operates up to 192MHz. It supports an integrated 448KB SRAM and 64KB ROM, and a QSPI interface to external Flash. An integrated Flash Cache enables eXecute In Place (XIP) support for firmware from flash. It also includes many peripherals, including UART, I2C, SPI, I2S, DMIC, PWM, IrDA (T/R), CSI, SDIO and auxiliary ADC.

The WLAN subsystem contains the 802.11b/g/n radio, baseband and MAC that designed to meet both the low power and high throughput network application.

The SoC is designed for low-power operation and there is a separate power management unit for each subsystem. Multiple power domains and clocks can be individually shut down and the application and WLAN subsystems can be placed into low-power states, independently, to support a variety of application cases.

1.2 Features

- Package
  - 6 x 6mm 52-pin QFN package

- Power Management and Clock Source
  - Integrate high efficiency power management unit with single 2.7-5.5V power supply input.
  - Integrated DC-DC and LDOs for internal power supply
  - Separate power switches for CPU, RAM and peripherals
  - 24/26/40/52MHz source crystal clock support
  - 32KHz OSC and RC clock support

- Application Microcontroller Subsystem
  - ARM Cortex-M4F, up to 192MHz
  - Embedded 448KB SRAM and 64KB ROM
  - Supports external SPI flash with QSPI mode and eXecute In Place (XIP) on flash
  - Flash cache for XIP mode
  - Supports Secure Boot
  - Hardware Crypto Engine for Advanced Security, Including AES, DES/3DES, SHA2/MD5, CRC
  - 8-channels General Direct Memory Access(DMA) channels

- 2 Universal Asynchronous Receivers and Transmitters (UART)
- 2 Serial Peripheral Interface (SPI, boot & Application) with multi Chip-Select
- 2 General Timers, 2 alarm timers, 1 RTC and 1 watch dog
- 8 PWM and Event Capture Controllers
- 8 channels 12-bit accuracy ADC
- 1 Camera Serial Interface (CSI)
- 1 Digital Audio Controller supports PCM and IIS protocol
- 1 Digital Microphone Controller
- 1 SD/MMC/SDIO Controller for external storage
- 2 Two Wire Interface Controllers for Camera module and some other sensors control
- 1 IR receiver and 1 IR transmitter

- WLAN Subsystem

- 802.11b/g/n Radio, Baseband, Medium Access Control(MAC)
- Embedded TCP/IP Stack
- Station, AP Modes
- SmartConfig Technology for Autonomous and Fast WIFI Connections
- Security support for WEP, WPA/WPA2 personal, WPS2.0
- Industry-Standard BSD Socket Application Programming Interfaces (APIs)

- Miscellaneous
- Integrates 2Kbit eFuse to store device specific information and RF calibration data

1.3 Application

- Home Automation
- Home Appliances
- Access Control
- Security Systems
- Smart Energy
- Internet Gateway
- Cloud Connectivity
- Industrial Control
- Wearable Equipment
- Wireless Audio
- IP Network Sensor Nodes

1.4 Block Diagram

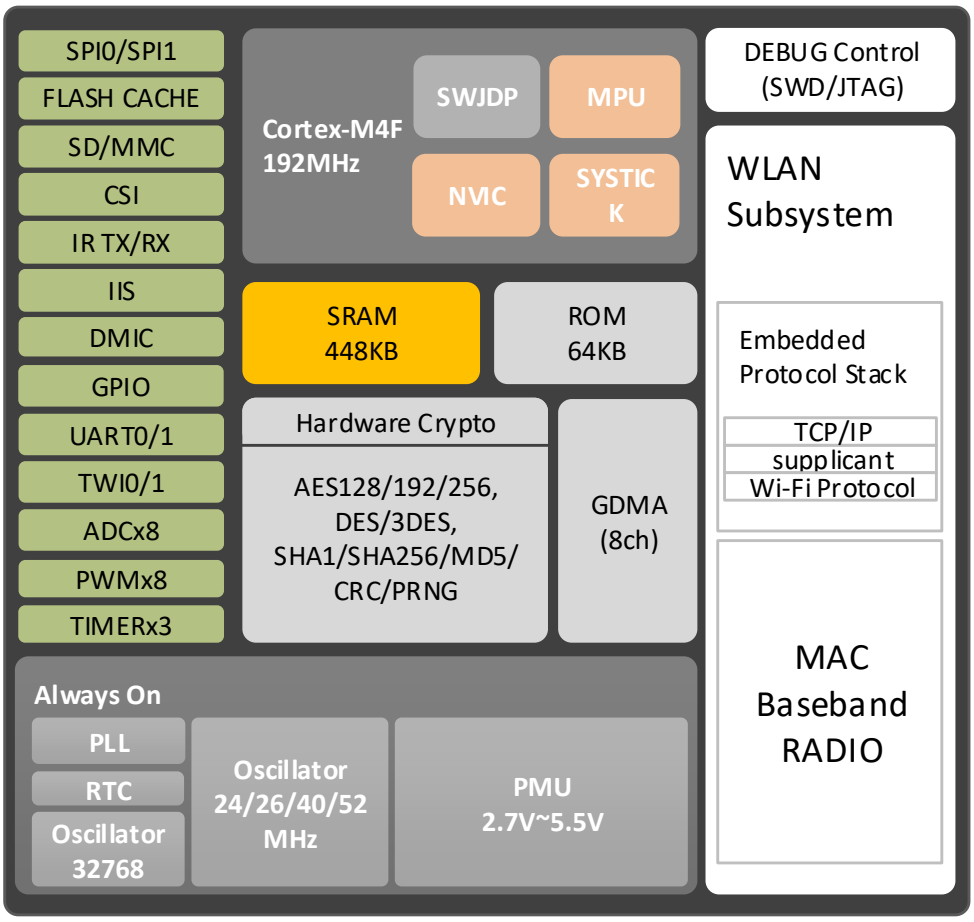


Figure 1-1 XR871 Functional Block Diagram

2 Function Description

2.1 System Overview

2.1.1 Power Management

A single 2.7 – 5.5V power supply is required for the XR871. It could be from an AC-DC converter to convert the AC voltage supply to 5V or a DC-DC converter to convert higher voltage supply to 3.3V. It could be from a battery directly too.

The Power Management Unit (PMU) contains a DC-DC, several Low Drop-out Regulators (LDOs), a highly efficient buck converter and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection, and low output noise.

The PMU integrates several LDOs for different circuits: DLDO stands for digital core LDO and the ALDO stands for Analog and RF system LDO. PLDO stands for clock generate system LDO and RLDO stands for the RTC and SLEEP system LDO. In Deep-Sleep mode, the DLDO, PLDO, RLDO can be shut down and only the RLDO is working.

There are three power domains in the system: RTC domain, SRAM domain, Digital Core domain and WIFI domain.

2.1.2 Clock

The clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based up a module's individual requirements. The system depends on, and generates two different clocks: a high frequency clock *HFCLK* and a low frequency clock *LFCLK.*

The system supports two LFCLK clock sources, the 32.768 KHz crystal oscillator and the 32.768 KHz RC oscillator. The 32.768 KHz crystal oscillator requires an external AT-cut quartz crystal to be connected to the XL1 and XL2 pins. The LFCLK clock and all of the available LFCLK sources are switched off by default when the system is powered up. The LFCLK clock can be started by selecting the preferred clock source in PRCM register. The LFCLK is used for each subsystem to achieve lower current consumption for different running mode. In addition, the LFCLK is also used in RTC circuit to achieve accuracy timing.

There is only one clock source for HFCLK, the 24MHz, 26Mhz, 40MHz or 52MHz crystal oscillator. The HFCLK is enabled automatically when the system is powered up and can be switched off when all subsystems won't use it anymore in some low power modes.

The HFCLK is used to generate the clock source for Digital PLL, which is used to generate the clock sources for Cortex-M4 core, WLAN and peripherals. There is also an Audio PLL used to generate the clock source for I2S (for external audio CODEC).

The following figure shows the clock control block diagram.

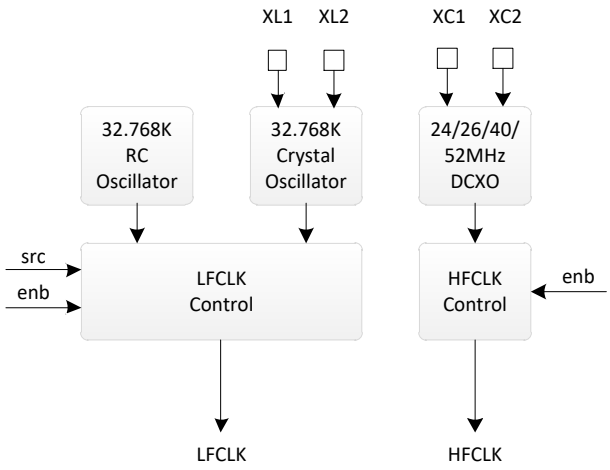


Figure 2-1 XR871 Clock Control

2.1.3 Memory Mapping

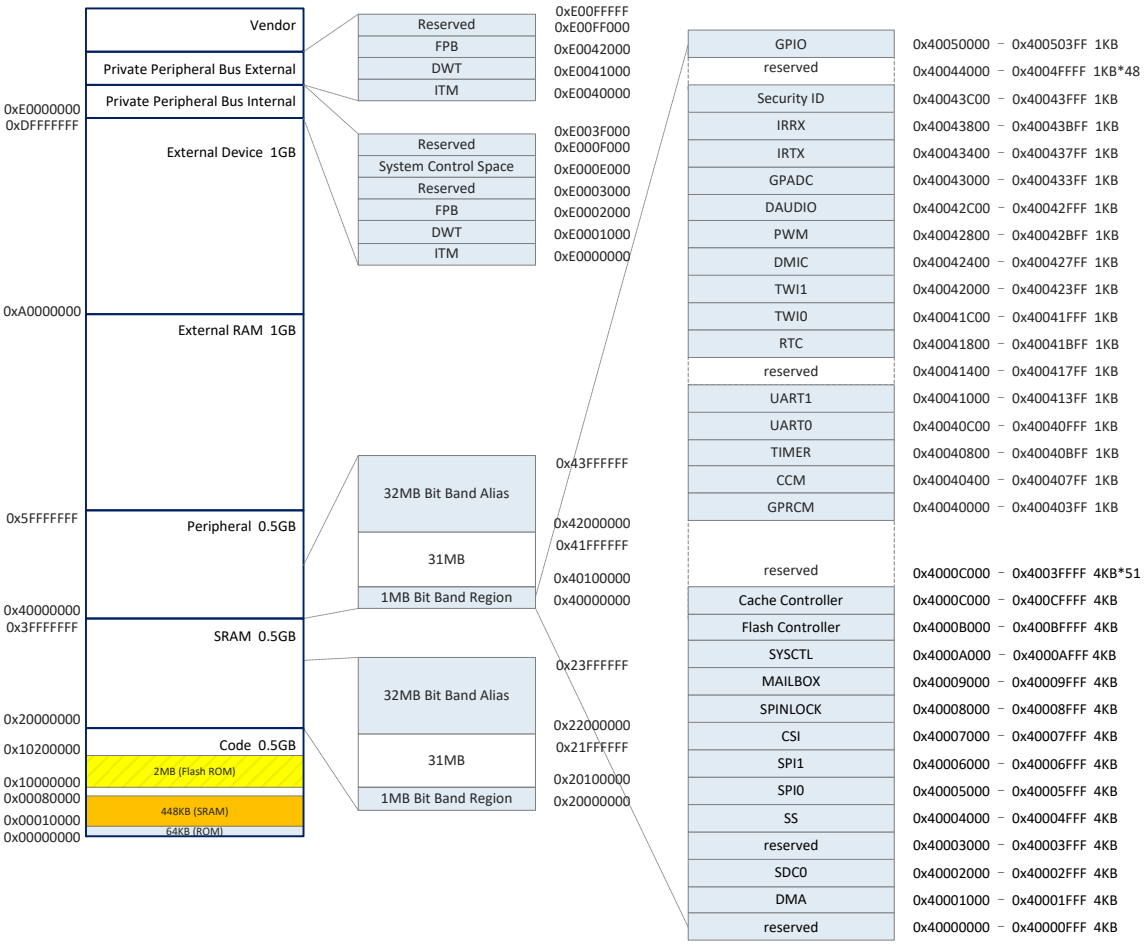


Figure 2-2 XR871 Memory Mapping

2.1.4 CPU

XR871 features an ARM Cortex-M4 processor, which is the most energy efficient ARM processor available. It supports the clock rates from 32KHz up to 192MHz. The processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption.

The ARM Cortex-M4 core has low-latency interrupt processing with the following features:

- Thump-2 instruction set for optimal performance and code size
- Handler and thread modes
- Memory Protection Unit (MPU) for memory protection features
- Floating Point Unit (FPU) to support DSP related function
- Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing
- Three Advanced High-Performance bus AHB-Lite interfaces: ICode, DCode and system bus
- Bit-band support for memory and select peripheral that include atomic bit-band write and read operations
- Wake-up Interrupt Controller (WIC) providing ultra-low power sleep mode support

2.1.5 Crypto Engine

The Crypto Engine (CE) is one encrypt/decrypt algorithms accelerator. It is suitable for a variety of applications.

Features:

- Supports AES, DES, 3DES, SHA-1, MD5, PRNG, CRC32/16, SHA256
- Supports ECB, CBC, CTR modes for AES/DES/3DES
- Supports 128-bits, 192-bits and 256-bit key size for AES
- Supports 160-bits hardware PRNG with 192-bits seed

2.2 Peripherals

2.2.1 GPIO

The XR871 GPIO unit provides as many as 31 GPIO (General Purpose IO) pins. All ports are brought out of the device using alternate function multiplexing. The GPIO function can be multiplexed on a multi-function I/O pin by selecting the GPIO alternate function in the GPIO Controller registers.

There are two types of GPIO designs in XR871: GPIO and AGPIO. Each GPIO can be configured with the following options:

- Input / Output / Floating(Hi-Z) mode
- Input mode: Pull-up or Pull-down
- Output mode: Active driving
- Pull-up/down control: the pull-up and pull-down resistance is 90KΩ with ±30% variation over PVT

condition

- External Interrupt IO with 5 trigger modes: high-level, low-level, rising edge, falling edge, double edge

The digital IO AGPIO function is equivalent to GPIO as shown above. A dedicated internal control signal is used to select between the digital and analog functions. These IOs are multiplexed with 8 channels ADC.

GPIO	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5
PA00	SPI1_MOSI	SD_CMD	UART0_TX	CSI_D0	EINTA0
PA01	SPI1_MISO	SD_DATA0	UART0_RX	CSI_D1	EINTA1
PA02	SPI1_CLK	SD_CLK	TWI1_SCL	CSI_D2	EINTA2
PA03	SPI1_CS0	SD_DATA1	TWI1_SDA	CSI_D3	EINTA3
PA04	UART1_CTS	SD_DATA2	TWI0_SCL	CSI_D4	EINTA4
PA05	UART1_RTS	SD_DATA3	TWI0_SDA	CSI_D5	EINTA5
PA06	UART1_TX	SPI1_CS1	TWI0_SCL	CSI_D6	EINTA6
PA07	UART1_RX	SPI1_CS2	TWI0_SDA	CSI_D7	EINTA7
PA08	ADC_CH0	PWM0/ECT0	TWI1_SCL	CSI_PCLK	EINTA8
PA09	ADC_CH1	PWM1/ECT1	TWI1_SDA	CSI_MCLK	EINTA9
PA10	ADC_CH2	PWM2/ECT2	DMIC_CLK	CSI_HSYNC	EINTA10
PA11	ADC_CH3	PWM3/ECT3	DMIC_DATA	CSI_VSYNC	EINTA11
PA12	ADC_CH4	PWM4/ECT4	I2S_MCLK	IR_TX	EINTA12
PA13	ADC_CH5	PWM5/ECT5	I2S_BCLK	32KOSCO	EINTA13
PA14	ADC_CH6	PWM6/ECT6	I2S_DI	IR_RX	EINTA14
PA15	ADC_CH7	PWM7/ECT7	I2S_DO	UART1_CTS	EINTA15
PA16	IR_TX	IR_RX	I2S_LRCLK	UART1_RTS	EINTA16
PA17	TWI0_SCL	IR_RX	TWI1_SCL	UART1_TX	EINTA17
PA18	TWI0_SDA	IR_TX	TWI1_SDA	UART1_RX	EINTA18
PA19	NUART_CTS		PWM0/ECT0	SPI1_MOSI	EINTA19
PA20	NUART_RTS		PWM1/ECT1	SPI1_MISO	EINTA20
PA21	NUART_TX	DMIC_CLK	PWM2/ECT2	SPI1_CLK	EINTA21
PA22	NUART_RX	DMIC_DATA	PWM3/ECT3	SPI1_CS0	EINTA22
PB00	UART0_TX		PWM4/ECT4		EINTB0
PB01	UART0_RX		PWM5/ECT5		EINTB1
PB02	SWD_TMS		PWM6/ECT6		EINTB2
PB03	SWD_TCK		PWM7/ECT7		EINTB3
PB04	SPI0_MOSI				EINTB4
PB05	SPI0_MISO				EINTB5
PB06	SPI0_CS0				EINTB6
PB07	SPI0_CLK				EINTB7

Table 2-1 GPIO Multiplexing

2.2.2 UART

The XR871 provides 3 UART controllers: one is used for debug and two with auto-flow control are used for

communication with external devices. The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

Features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- Support DMA controller interface
- Support Software/ Hardware Flow Control
- Support IrDA 1.0 SIR
- Support RS-485 mode
- Support configurable Baudrate from 9600, 19200, 38400, 115200 and 921600 etc.
- Support baudrate detection

2.2.3 SPI

The XR871 features two SPI controllers. Each controller can be configured to a SPI master or a SPI slave. They are used as an extension interface to control the peripheral devices. They support two options of clock polarity (CPOL) and two options of initial clock phase (CPHA).

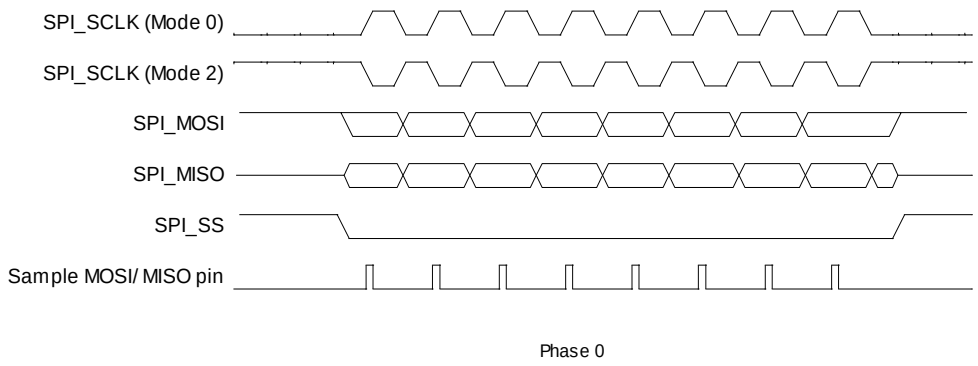


Figure 2-3 SPI Phase 0 Transfer Format

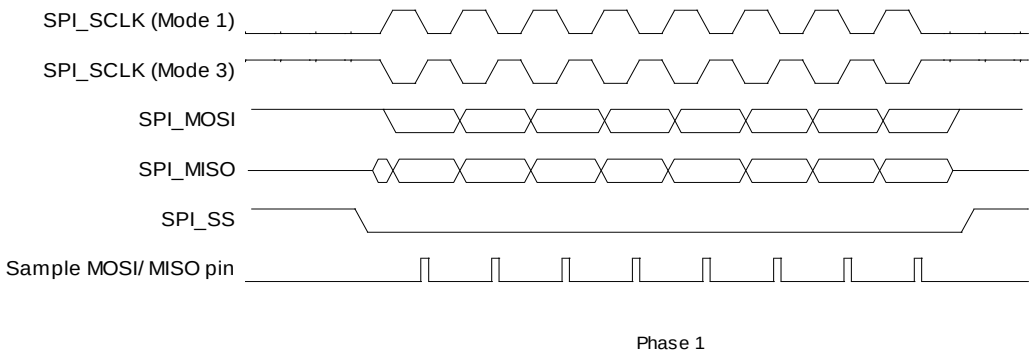


Figure 2-4 SPI Phase 1 Transfer Format

2.2.4 IIC

The XR871 features two I2C serial interfaces. They can be configured as master and salve mode. Each IIC controller supports three IO mapping. The IIC controllers can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

Features:

- Software-programmable for Slave or Master
- Supports Repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies
- Compatible with SCCB protocol

2.2.5 DAUDIO(IIS&PCM)

XR871 features one Digital Audio Interface, which is used to connect to an external audio codec. The controller supports standard I2S format, Left-justified Mode format, Right-justified Mode format, PCM Mode format and TDM Mode format.

Features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Support full-duplex synchronous work mode
- Support Master / Slave mode
- Support adjustable interface voltage
- Support adjustable audio sample resolution from 8-bit to 32-bit.
- Support up to 8 slots which has adjustable width from 8-bit to 32-bit.
- Support sample rate from 8KHz to 192KHz
- Support up to 4 data output pin
- Support 8-bits u-law and 8-bits A-law companding sample
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Support programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Support loopback mode for test

The Digital Audio Interface is the extended of I2S and PCM which provides a serial bus interface for stereo and multichannel audio data. This interface is most commonly used by consumer audio market, including compact disc,

digital audio tape, digital sound processors, and digital TV-sound.

2.2.6 DMIC

XR871 features one DMIC Controller which supports a 2-channels digital microphone interface, the DMIC controller can output 128fs or 64fs (fs= ADC sample rate).

Features:

- Support up to 2 channels
- Support sample rate from 8KHz to 48KHz

2.2.7 PWM

XR871 features 8 PWMs to generate pulse sequences with programmable frequency a duration for LCD, vibrators and other devices. The PWM controller provides 8 PWM channels, which are divided into four pairs of PWM pair, each is composed of three parts: a clock controller, two timer modules, a programmable dead-zone generator. The PWM channel logic can be configured as input capture function. The capturer detects the rising edge and the falling edge of the signal and calculates the high-level and the low-level duration with a 16-bit counter.

Features:

- 8 PWM channels, divided into 4 PWM pairs
- Supports pulse, period and complementary pair outputs
- Support input capture
- Programmable dead-zone generator
- Configurable output frequency, 0%-100% duty adjustable

2.2.8 SD/MMC/SDIO

XR871 features a SD/MMC controller can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

Features:

- Supports Secure Digital memory protocol commands (compatible with SD3.0)
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands
- Supports CE-ATA digital protocol commands
- Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.41) or CE-ATA device
- Supports hardware CRC generation and error detection
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports block size of 1 to 65535 bytes
- Supports internal DMA controller

2.2.9 IrDA

XR871 features an infrared remote transmitter and a receiver controller. Through the process control pulse waveform, the remote controller can support a variety of infrared protocol.

The IR receiver controller features:

- Full physical layer implementation
- Support IR for remote control
- 64x8 bits FIFO for data buffer

The IR transmitter controller features:

- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Interrupt and DMA support

2.2.10 ADC

XR871 features one auxiliary ADC function. The ADC function contains a 9-channel analog switch, a single end input asynchronous 12-bit SAR (Successive Approximation Register) ADC. The channels 0 to 7 are used to detect the voltage of the external input and the channel 8 is dedicated to detect the voltage of the VBAT.

Features:

- 12-bit Resolution and 10-bit effective SAR type A/D converter
- 9-channel multiplexer
- 64 FIFO depth of data register
- Power Supply Voltage: 2.5V, Analog Input Range: 0 to 2.5V
- Maximum Sampling frequency: 1 MHz
- Support self-calibration
- Support data compare and interrupt
- Support four operation mode: Single conversion mode, Single-cycle conversion mode, Continuous conversion mode, Outbreak conversion mode

2.2.11 CSI

The Camera Serial Interface (CSI) is a parallel image input interface. It includes the following features:

- 8 bits input data
- support CCIR656 protocol for NTSC and PAL
- 3 parallel data path s for image stream parsing
- received data double buffer support
- parsing bayer data into planar R,G,B output to memory
- parsing interlaced data into planar or MB Y, Cb, Cr output to memory

- pass raw data direct to memory
- all data transmit timing can be adjusted by software
- luminance statistical value

2.3 WIFI Subsystem

2.3.1 WIFI MAC

Supports MAC enhancements including:

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11h – Transmit power control dynamic and frequency selection
- 802.11i - Security including WPA2 compliance
- 802.11r – Roaming

2.3.2 WIFI Baseband

Features:

- Compatible with IEEE 802.11 b/g/n standard
- MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
- Short Guard Interval

2.3.3 WIFI Radio

Features:

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network

2.3.4 WIFI 2.4G RF Transmitter/Receiver Specification

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range	Center channel frequency	2412		2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS				dBm
	2Mbps DSSS				dBm
	5.5Mbps CCK				dBm
	11Mbps CCK				dBm
RX Sensitivity (802.11g)	6Mbps OFDM				dBm
	9Mbps OFDM				dBm

	12Mbps OFDM				dBm
	18Mbps OFDM				dBm
	24Mbps OFDM				dBm
	36Mbps OFDM				dBm
	48Mbps OFDM				dBm
	54Mbps OFDM				dBm
RX Sensitivity (802.11n, 20MHz)	MCS 0				dBm
	MCS 1				dBm
	MCS 2				dBm
	MCS 3				dBm
	MCS 4				dBm
	MCS 5				dBm
	MCS 6				dBm
	MCS 7				dBm
TX Power	1Mbps DSSS				dBm
	11Mbps CCK				dBm
	6Mbps OFDM				dBm
	54Mbps OFDM				dBm
	HT20, MCS 0				dBm
	HT20, MCS 7				dBm

3 Electrical Characteristics

3.1 Absolute Maximum Rating

Symbol	Parameter	Maximum rating	Unit
VCC	2.7-5.5V Power supply	-0.3 to 5.8	V
T_{opr}	Operating Temperature	-40 to 85	℃
T_{stg}	Storage Temperature	-40 to 125	℃
VESD	HBM	2000	V
VESD	CDM	500	V

Table 3-1 Absolute Maximum Rating

3.2 Digital IO Characteristics

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Input Low Voltage	VCC_IO=3.3V	-0.3	1.32	V
V_{IH}	Input High Voltage	VCC_IO=3.3V	2.06	3.6	V
V_{OL}	Output Low Voltage	|IOH| = 1.6~14 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	|IOH| = 1.6~14 mA	2.9	3.3	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	40	110	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	40	110	KΩ

Table 3-2 DC Characteristics

3.3 XTAL Oscillator

Parameter	Value
Frequency	24, 26, 40, 52MHz
Stability	+/-20ppm including temperature variation

Table 3-3 XTAL Oscillator Requirements

4 Package Specifications

4.1 Pin Layout

XR871 uses 6mm x 6mm QFN package of 52-pin with 0.4mm pitch.

4.1.1 XR871G Pin Layout

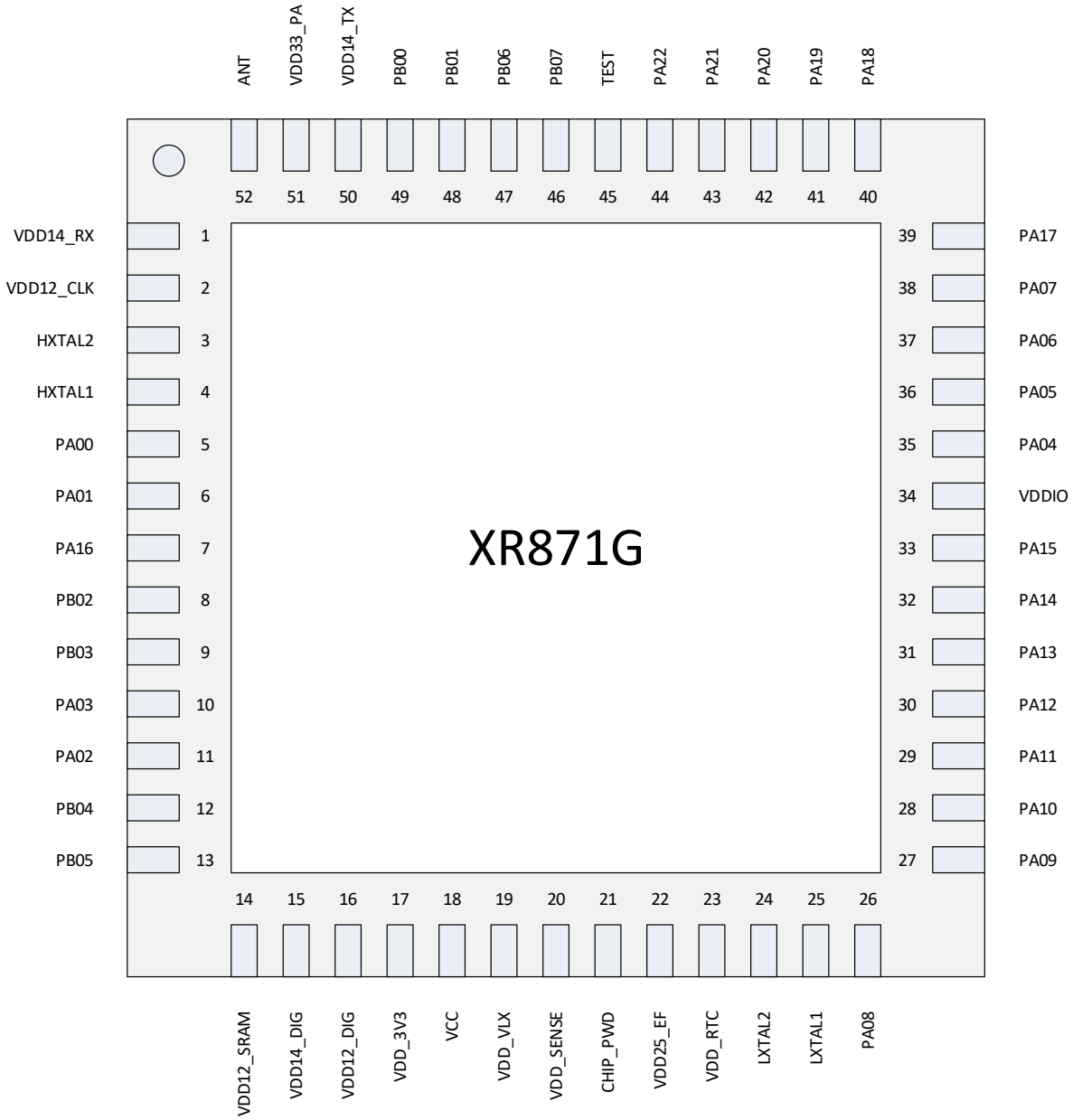


Figure 4-1 XR871G Pin Layout

4.1.2 XR871ET Pin Layout

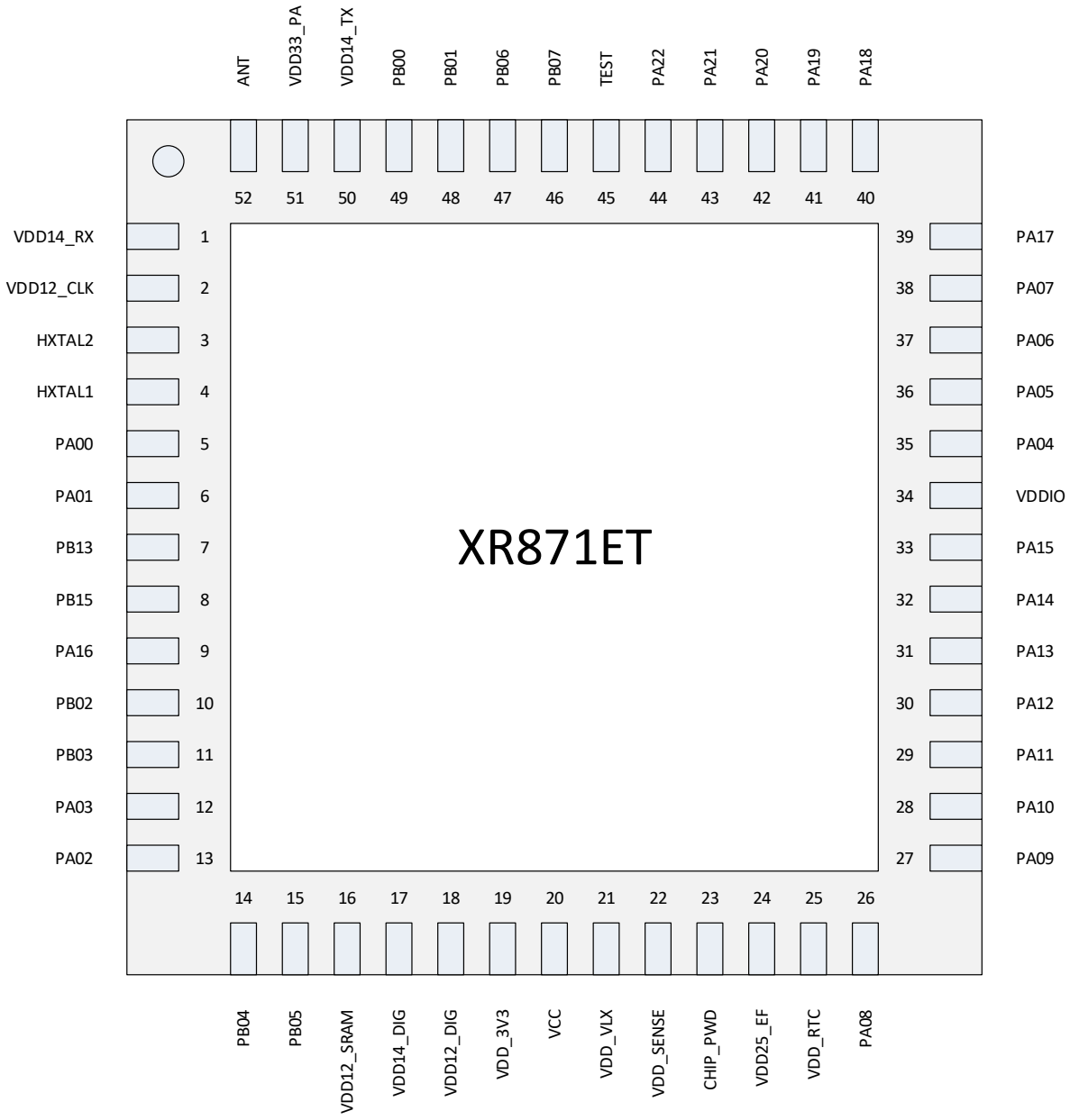


Figure 4-2 XR871ET Pin Layout

4.2 Pin Description

4.2.1 XR871G

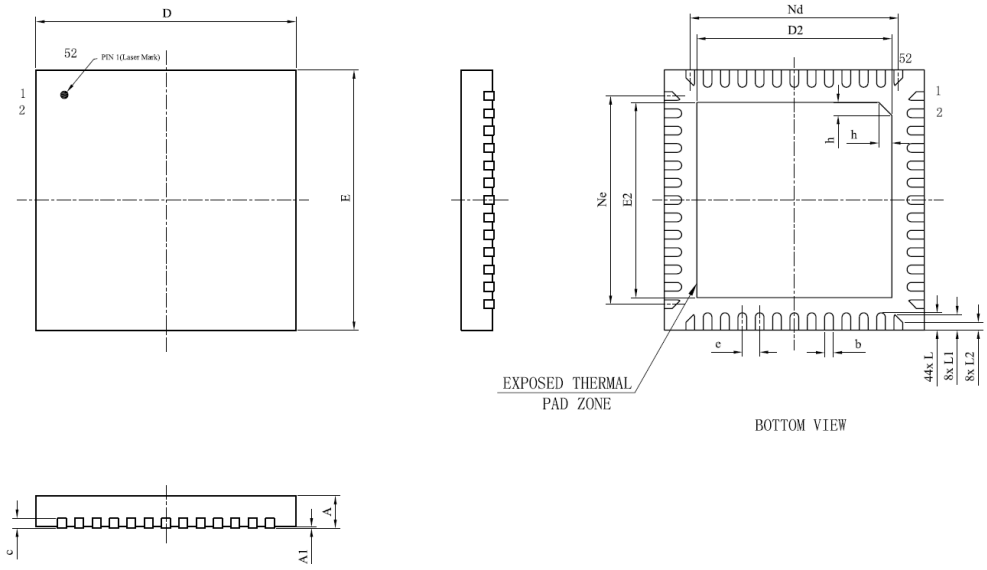
QFN NO.	Pin Name	Pin Description	I/O	Supply Domain
Power, Reset and Clocks				
25	LXTAL1	32KHz Crystal	Analog	VDD_3V3
24	LXTAL2	32KHz Crystal	Analog	VDD_3V3
4	HXTAL1	24/26/40/52MHz crystal	Analog	VDD_3V3
3	HXTAL2	24/26/40/52MHz crystal	Analog	VDD_3V3
23	CHIP_PWD/RESET	Chip Power Down/System Reset	Input	
2	VDD12_CLK	Clock 1.2V power supply	Power	
1	VDD14_RX	RF 1.4V power supply	Power	
50	VDD14_TX	RF 1.4V power supply	Power	
18	VCC	2.7-5.5V power supply	Power	
20	VDD_SENSE	BUCK power supply	Power	
19	VDD_VLX	BUCK output	Power	
15	VDD14_DIG	DLDO power supply	Power	
22	VDD25_EF	ADC and eFuse 2.5V power supply	Power	
34	VDD_IO	IO 3.3V power supply	Power	
17	VDD_3V3	3.3V power supply	Power	
14	VDD12_SRAM	SRAM 1.1V power supply	Power	
16	VDD12_DIG	Digital core 1.1V power supply	Power	
51	VDD33_PA	PA 3.3V power supply	Power	
23	VDD_RTC	RTC 1.1V power supply	Power	
Programmable I/O				
5	GPIOA0	Programmable input/output	In/Out	VDD_IO
6	GPIOA1	Programmable input/output	In/Out	VDD_IO
11	GPIOA2	Programmable input/output	In/Out	VDD_IO
10	GPIOA3	Programmable input/output	In/Out	VDD_IO
35	GPIOA4	Programmable input/output	In/Out	VDD_IO
36	GPIOA5	Programmable input/output	In/Out	VDD_IO
37	GPIOA6	Programmable input/output	In/Out	VDD_IO
38	GPIOA7	Programmable input/output	In/Out	VDD_IO
26	GPIOA8	Programmable input/output	In/Out	VDD_IO
27	GPIOA9	Programmable input/output	In/Out	VDD_IO
28	GPIOA10	Programmable input/output	In/Out	VDD_IO
29	GPIOA11	Programmable input/output	In/Out	VDD_IO
30	GPIOA12	Programmable input/output	In/Out	VDD_IO
31	GPIOA13	Programmable input/output	In/Out	VDD_IO

32	GPIOA14	Programmable input/output	In/Out	VDD_IO
33	GPIOA15	Programmable input/output	In/Out	VDD_IO
7	GPIOA16	Programmable input/output	In/Out	VDD_IO
39	GPIOA17	Programmable input/output	In/Out	VDD_IO
40	GPIOA18	Programmable input/output	In/Out	VDD_IO
41	GPIOA19	Programmable input/output	In/Out	VDD_IO
42	GPIOA20	Programmable input/output	In/Out	VDD_IO
43	GPIOA21	Programmable input/output	In/Out	VDD_IO
44	GPIOA22	Programmable input/output	In/Out	VDD_IO
49	GPIOB0	Programmable input/output	In/Out	VDD_IO
48	GPIOB1	Programmable input/output	In/Out	VDD_IO
8	GPIOB2	Programmable input/output	In/Out	VDD_IO
9	GPIOB3	Programmable input/output	In/Out	VDD_IO
12	GPIOB4	Programmable input/output	In/Out	VDD_IO
13	GPIOB5	Programmable input/output	In/Out	VDD_IO
47	GPIOB6	Programmable input/output	In/Out	VDD_IO
46	GPIOB7	Programmable input/output	In/Out	VDD_IO
WIFI Radio Interface				
52	ANT	RF Antenna	Analog	
Debug IO				
45	TEST	TEST pin	Input	

Table 4-1 XR871G Pin Description

4.3 Package Information

4.3.1 QFN52



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 4-3 QFN52 Package Outline Drawing

5 Application Circuit