Design & Simulate 14

ECE2204 CRN:82929

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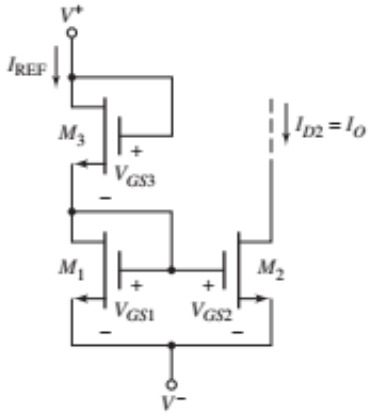
Problem 14.10-8.a.1:

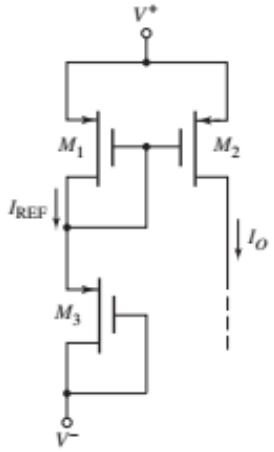
Switched from NMOS to PMOS.

Design

Design a MOSFET current source circuit to meet the following specifications. The circuit to be designed has the configuration shown below with all NMOS transistors swapped with PMOS transistors and V^+ swaps places with V^-. The bias voltages are $V^+ = 2.5V$ and $V^- = 0$. Transistors are available with parameters $k'_p = 100\mu A/V^2$, $V_{TP} = 0.4V$. and $\lambda = 0$. Design the circuit such that $I_{REF} = 100\mu A$, $I_O = 60\mu A$, and $V_{SD2}(sat) = 0.4V$.



(Original)



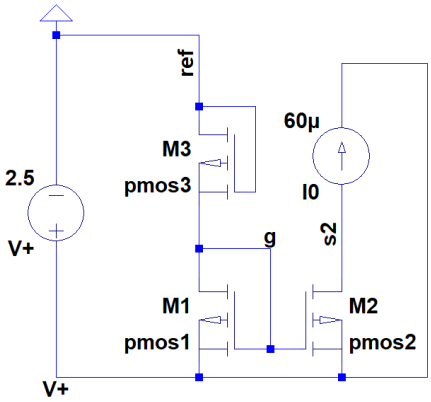
(w/ PMOS and Voltage Inversion)

$$
\begin{aligned}
V_{SD2}(sat) &= V_{SG2} + V_{TP} \\
V_{SG2} &= V_{SG1} = V_{SD2}(sat) - V_{TP} = 0.4V + 0.4V = 0.8V \\
\frac{W}{L}_2 &= \frac{2I_O}{k'_p(V_{SG2} + V_{TP})^2} = \frac{2(60\mu A)}{(100\mu A/V^2)(0.8V - 0.4V)^2} = 7.5 \\
\frac{W}{L}_1 &= \frac{2I_{REF}}{k'_p(V_{SG1} + V_{TP})^2} = \frac{2(100\mu A)}{(100\mu A/V^2)(0.8V - 0.4V)^2} = 12 \\
V_{SG3} &= V^+ - V^- - V_{GS1} = 2.5V - 0V - 0.8V = 1.7V \\
\frac{W}{L}_3 &= \frac{2I_{REF}}{k'_p(V_{SG3} + V_{TP})^2} = \frac{2(100\mu A)}{(100\mu A/V^2)(1.7V - 0.4V)^2} = 1.183
\end{aligned}
$$

The final design values are $\frac{W}{L}_1 = 12$, $\frac{W}{L}_2 = 7.5$, and $\frac{W}{L}_3 = 1.183$.

Validation

LTSpice Implementation (values within $< 1\%$)




```
.model pmos1 PMOS(Kp=100u W=12 L=1u Vto=-0.4)
.model pmos2 PMOS(Kp=100u W=7.5 L=1u Vto=-0.4)
.model pmos3 PMOS(Kp=100u W=1.183 L=1u Vto=-0.4)
.op
```

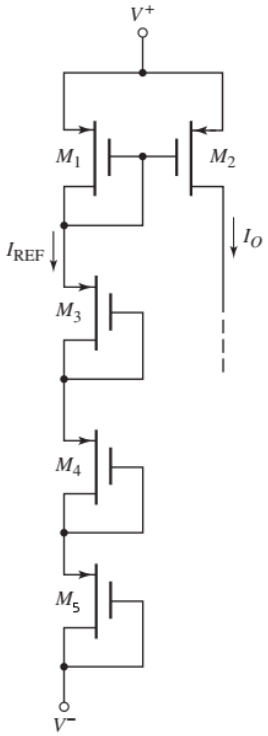
V(g):	1.69378	voltage
V(v+):	2.5	voltage
V(s2):	2.5	voltage
Id(M2):	-5.99248e-005	device_current
Ig(M2):	-0	device_current
Ib(M2):	2.72735e-019	device_current
Is(M2):	5.99248e-005	device_current
Id(M1):	-99.0091	device_current
Ig(M1):	-0	device_current
Ib(M1):	8.16221e-013	device_current
Is(M1):	99.0091	device_current
Id(M3):	-99.0091	device_current
Ig(M3):	-0	device_current
Ib(M3):	1.70378e-012	device_current
Is(M3):	99.0091	device_current
I(I0):	6e-005	device_current
I(V+):	-99.0091	device_current

$$Err_{V_{SG1}} = \frac{|1.7 - 1.69378|}{1.7} = 0.0037 = 0.37\%$$
$$Err_{I_{REF}} = \frac{|100 - 99.0091|}{100} = 0.0099 = 0.99\%$$
$$Err_{I_O} = \frac{|60 - 59.9248|}{60} = 0.00125 = 0.13\%$$

Problem 14.10-8.b.1:

Derived from Problem 10.54 from page 744 of the textbook by changing some values and adding a 5th transistor.

Design



The transistor circuit shown to the left is biased at $V^+ = 12V$ and $V^- = 0V$. The transistor parameters are $V_{TP} = -1.2V$, $k'_p = 80\mu A/V^2$, $\lambda = 0$, $\frac{W}{L}_1 = \frac{W}{L}_2 = 25$, and $\frac{W}{L}_3 = \frac{W}{L}_4 = \frac{W}{L}_5 = 4$. Determine I_{REF}, I_O, and $V_{SD2}(sat)$.

$V_{SG1} = V_{SG2}$, $V_{GD1} = V_{GD2} = V_{GD3} = V_{GD4} = V_{GD5} = 0V$

$$
\begin{aligned}
& V^+ = SG1 + V_{SG3} + V_{SG4} + V_{SG5} \\
\Longrightarrow\ & V_{SG3} + V_{SG4} + V_{SG5} = 3V_{SG3} \\
\Longrightarrow\ & V_{SG1} = V^+ - 3V_{SG3}
\end{aligned}
$$

Ran out of time and was unable to complete the second problem.

This assignment should demonstrate a basic understanding of designing basic MOSFET circuits by adapting the widths and lengths of the transistors.

I have neither given nor received unauthorized assistance on this assignment.