Homework 11

ECE2504 CRN:82729

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Question 1: (2 pts) How many flip flop values are complemented in an 6-bit binary ripple counter to reach the next count value after

a) 111111 : 6 Flip flops
b) 010101 : 2 Flip flops

Question 2: (3 pts) Use D type flip flops and gates to design a counter with the following repeated sequence: 00, 01, 10

Q_1 \ Q_0	0	1
0	1	0
1	0	-

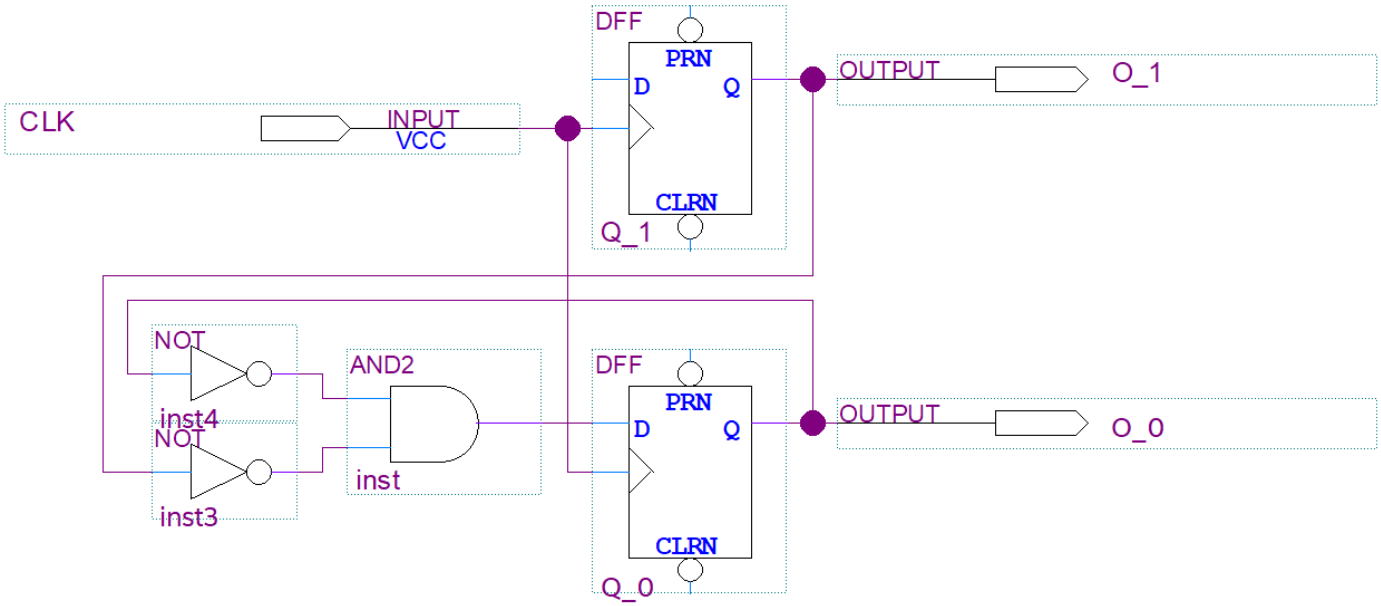
(a) D_0 Karnaugh Map

Q_1 \ Q_0	0	1
0	0	1
1	0	-

(b) D_1 Karnaugh Map

$$D_0 = Q_1' Q_0'$$
$$D_1 = Q_0$$

(c) Required Combination Logic



(d) Circuit Diagram

Figure 1: Question 2 Counter Design

Question 3: (6 pts) Use SR type flip flops and gates to design a counter with each of the following repeated sequences:

a) 000, 001, 010, 011, 100, 101, 110, 111

Current State	Next State	SR_2	SR_1	SR_0
000	001	00	00	10
001	010	00	10	01
010	011	00	00	10
011	100	10	01	01
100	101	00	00	10
101	110	00	10	01
110	111	00	00	10
111	000	01	01	01

(a) State Table

$$S_0 = Q_0'$$
$$R_0 = Q_0$$
$$S_1 = Q_1'Q_0$$
$$R_1 = Q_1Q_0$$
$$S_2 = Q_2'Q_1Q_0$$
$$R_2 = Q_2Q_1Q_0$$

(b) Required Combination Logic

Q_2Q_1 \ Q_0	0	1
00	1	0
01	1	0
11	1	0
10	1	0

(c) S_0 Karnaugh Map

Q_2Q_1 \ Q_0	0	1
00	0	1
01	0	0
11	0	0
10	0	1

(d) S_1 Karnaugh Map

Q_2Q_1 \ Q_0	0	1
00	0	0
01	0	1
11	0	0
10	0	0

(e) S_2 Karnaugh Map

Q_2Q_1 \ Q_0	0	1
00	0	1
01	0	1
11	0	1
10	0	1

(f) R_0 Karnaugh Map

Q_2Q_1 \ Q_0	0	1
00	0	0
01	0	1
11	0	1
10	0	0

(g) R_1 Karnaugh Map

Q_2Q_1 \ Q_0	0	1
00	0	0
01	0	0
11	0	1
10	0	0

(h) R_2 Karnaugh Map

Figure 2: Question 3a Counter Design

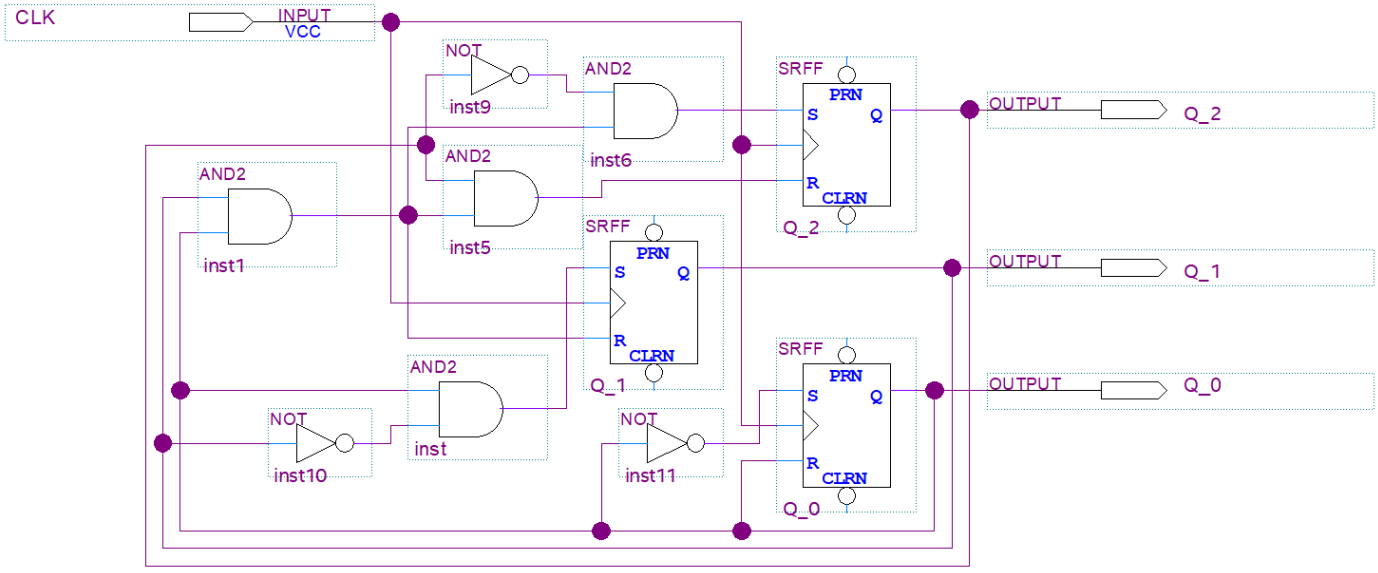


Figure 3: Question 3a Circuit Diagram

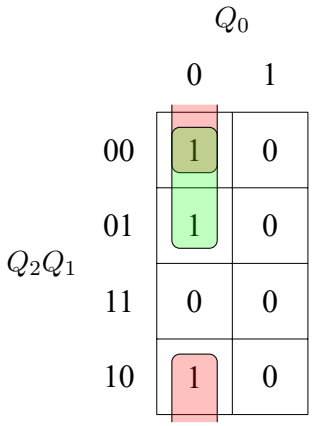
b) 000, 001, 010, 011, 100

Current State	Next State	SR_2	SR_1	SR_0
000	001	00	00	10
001	010	00	10	01
010	011	00	00	10
011	100	10	01	01
100	000	01	00	10

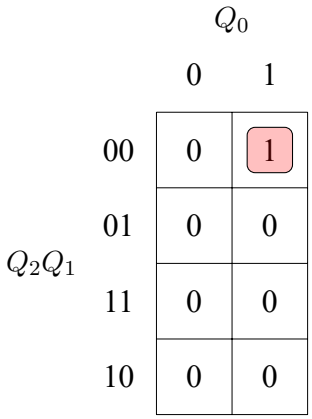
(a) State Table

$$S_0 = Q_2'Q_0' + Q_1'Q_0'$$
$$R_0 = Q_2'Q_0$$
$$S_1 = Q_2'Q_1'Q_0$$
$$R_1 = Q_2'Q_1Q_0$$
$$S_2 = Q_2'Q_1Q_0$$
$$R_2 = Q_2Q_1'Q_0'$$

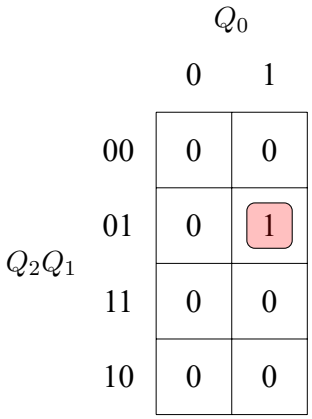
(b) Required Combination Logic



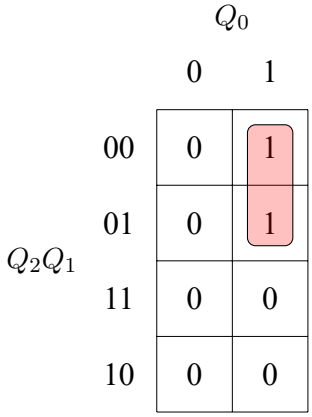
(c) S_0 Karnaugh Map



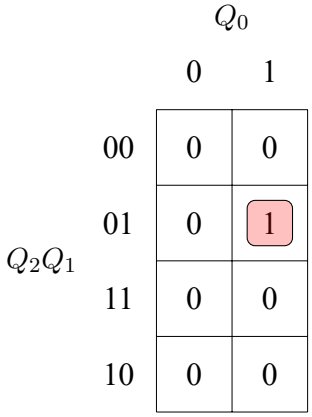
(d) S_1 Karnaugh Map



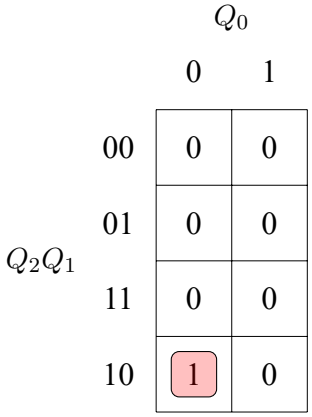
(e) S_2 Karnaugh Map



(f) R_0 Karnaugh Map



(g) R_1 Karnaugh Map



(h) R_2 Karnaugh Map

Figure 4: Question 3b Counter Design

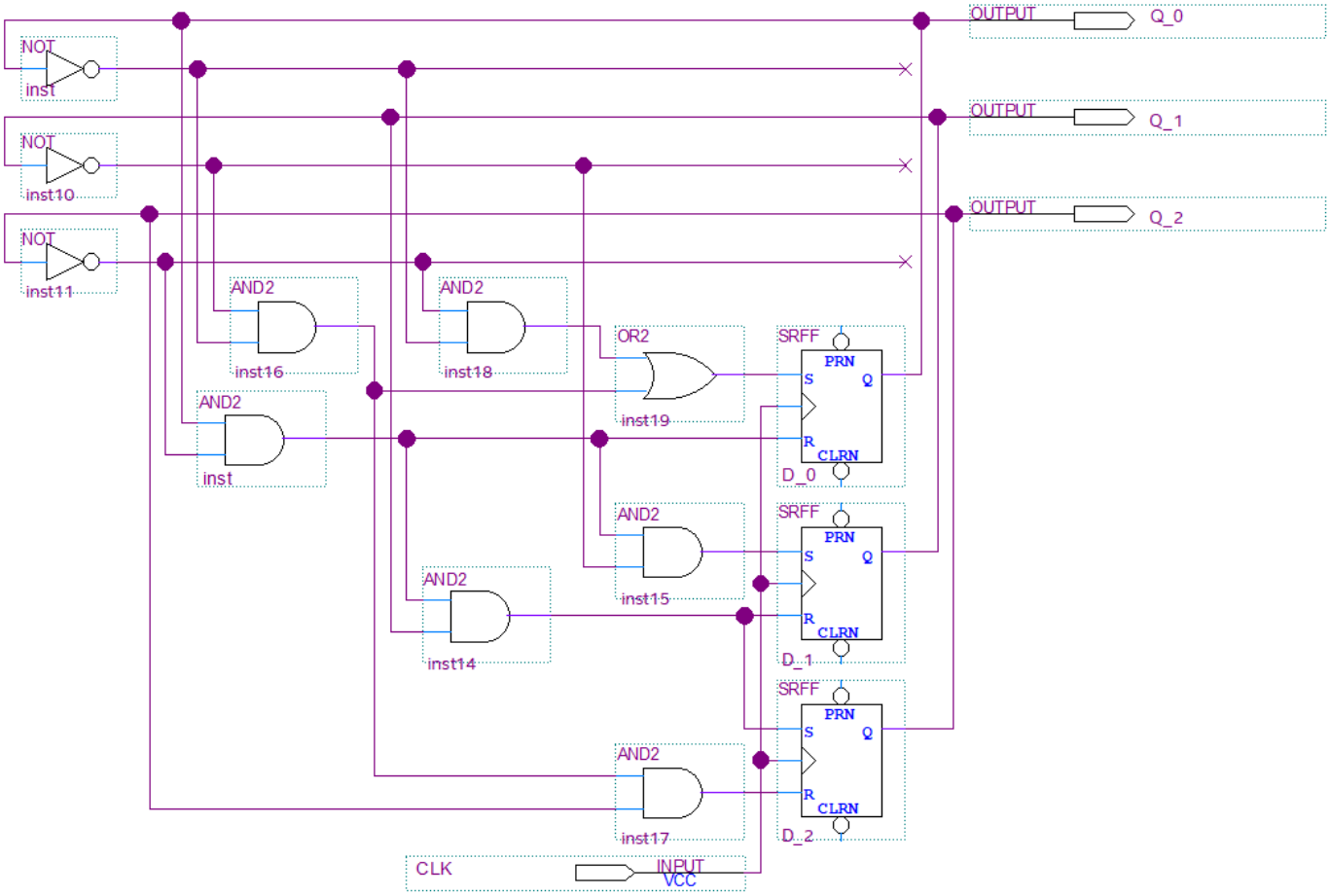


Figure 5: Question 3b Circuit Diagram

Question 4: (5 pts) Draw the state diagram for the following electronic vending machine specification. The vending machine sells Squirrel Nut Zippers for 25¢. The machine accepts N (nickels = 5¢), D (dimes = 10¢), and Q (quarters = 25¢). When the sum of the coins inserted in sequence is 25¢or more, the machine dispenses one Squirrel Nut Zipper by making V = 1 and returns to its initial state. If less than 25¢is inserted and the coin return button CR is pressed, then the coins deposited are returned by making C = 1. Change is not returned if more than 25¢is deposited.

Question 5: A communication link requires a circuit that produces the sequence 01111110. Design a synchronous sequential circuit that starts producing this sequence when the input E=1. Once the sequence starts, it completes. If E=1 during the last output in the sequence, the sequence repeats. Otherwise (if E=0) the output remains constant at 1.

a) (3 pts) Draw the state diagram.
b) (4 pts) Draw the state table and make a state assignment.
c) (3 pts) Design the circuit using SR flip flops and logic gates.

Question 6: (5 pts) A sequential circuit is described in HW10, Problem 4. Assume the timing parameters for the gates and flip flops are as follows:

Inverter: t_{pd} = 0.05 ns
AND gate: t_{pd} = 0.1 ns
OR gate: t_{pd} = 0.1 ns
Flip flop: t_{pd} = 0.2 ns, t_s = 0.02 ns, t_h = 0.01 ns
Note: t_{pd} = propagation delay, t_s = setup time, t_h = hold time

a) Find the longest path delay from an external circuit input passing through gates only to an external circuit output.
b) Find the longest path delay from an external circuit input to positive clock edge.
c) Find the longest path delay from a positive clock edge to output.
d) Find the longest path delay from positive clock edge to positive clock edge.
e) Determine the maximum frequency of operation of the circuit in GHz.

GRADING SCALE

Total: 31 pts

Pts	0	4	8	12	16	19	23	27
Letter Grade	D-	D	C-	C	B-	B	A-	A