Design & Simulate 26

ECE2204 CRN:82929

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November 8, 2018

Problem 21.16-11.a.1:

Design

Design a CMOS circuit that implements the following function.

$F(A, B, C, D, E) = \overline{AB + E(A + CD)}$

$F(A, B, C, D, E) = \overline{AB + AE + CDE} = \overline{A(B + E) + CDE}$

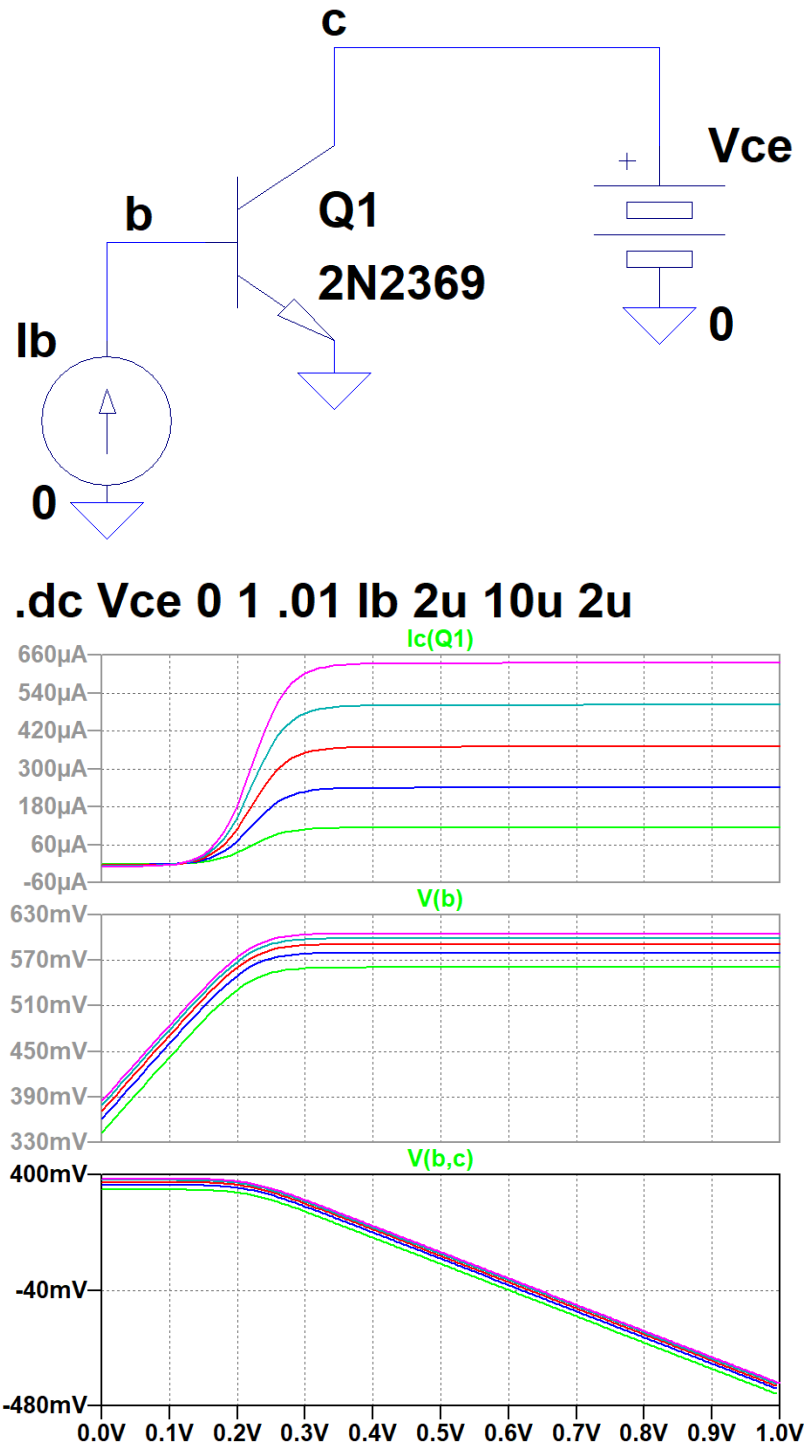
The NMOS element of F is F_n and the PMOS element is F_p.

$F_n(A, B, C, D, E) = (A + (B \parallel E)) \parallel (C + D + E)$

$F_p(A, B, C, D, E) = A \parallel (B + E) + (C \parallel D \parallel E)$

Validation

LTSpice Implementation (All values of truth table match waveform)



ABCDE	F(A,B,C,D,E)
00000	1
00001	1
00010	1
00011	1
00100	1
00101	1
00110	1
00111	0
01000	1
01001	1
01010	1
01011	1
01100	1
01101	1
01110	1
01111	0
10000	1
10001	0
10010	1
10011	0
10100	1
10101	0
10110	1
10111	0
11000	0
11001	0
11010	0
11011	0
11100	0
11101	0
11110	0
11111	0

This problem should demonstrate a basic ability to manipulate, design, and analyse MOSFET based logic circuits.

I have neither given nor received unauthorized assistance on this assignment.