Homework 6

ECE3544 CRN:82989

Jacob Abel

November 30, 2018

Problem 1: For each of the following memory sizes, given as number of words x size of word in bits, list the number of address lines and data lines are required.

1. 1K x 8: 10 addr lines, 7 data lines
2. 4K x 16: 12 addr lines, 16 data lines
3. 512 x 13: 9 addr lines, 13 data lines

Problem 2: How many memory chips would be required to build a memory that is 8192 x 8, if each memory chip is 256 x 1 bits? 32

Problem 3: Using the dual_port_rom module from slide 12 of the memory lecture as a starting point, create a model of a single port ROM (with ports similar to the one on slide 10) and then use the ROM to implement the sum and carry out for a 2-bit adder with carry in. The inputs will be A[1:0], B[1:0], and c_in, while outputs will be sum[1:0] and c_out. Your ROM should be the minimum size necessary to implement the adder. The ROM values should be stored in a text file that is read in using the $readmemh task. Create a testbench to show the correct operation of your ROM's functionality.

Files included

Problem 4: Using the single_clk_ram module from slide 29 of the memory lecture as a starting point, create a 16 x 8 memory where each memory location is initialized to (A5)16. Create a test bench for the memory that writes the value x+1 to each memory address x (i.e., address 0 has value 1, address 1 has value 2, address 2 has value 3, and so on), and then reads from each location to verify that it has been written correctly. Your test bench should write all 16 locations before reading them.