Design & Simulate 12

ECE2204 CRN:82929

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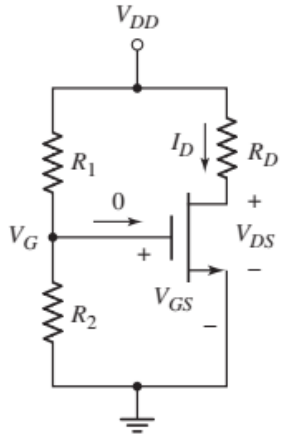
Problem 12.3-4.a.1:

Adapted ePMOS to eNMOS and changed values.

Design

Calculate the drain current and drain-to-source voltage of a common source circuit with a n-channel enhancement-mode MOSFET. Assume $R_1 = 50k\Omega$, $R_2 = 100k\Omega$, $R_D = 10k\Omega$, $V_{DD} = 5V$, $V_TN = 1V$, and $K_N = 0.03mA/V^2$.



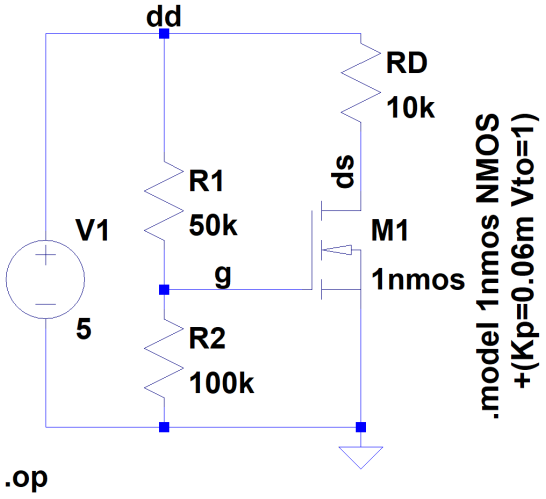
$$
\begin{aligned}
V_G = V_{GS} &= \frac{R_2}{R_1 + R_2}(V_{DD}) = \frac{100k\Omega}{150k\Omega}(5V) = 3.\overline{3}V \\
I_D &= K_N(V_{GS} - V_{TN})^2 = (0.03mA/V^2)(3.\overline{3}V - 1V)^2 = 0.163mA \\
V_{DS} &= V_{DD} - I_D R_D = 5V - 0.163mA \times 10k\Omega = 3.37V \\
V_{DS}(\text{sat}) &= V_{GS} - V_{TN} = 3.\overline{3}V - 1V = 2.\overline{3}V
\end{aligned}
$$

$V_{DS} > V_{DS}(\text{sat})$ and therefore the transistor is in the saturation region.

The drain to source voltage is $V_{DS} = 3.37V$ and the drain current is $I_D = 0.163mA$.

Validation

LTSpice Implementation (values within $< 1\%$)



V(dd):	5	voltage
V(g):	3.33333	voltage
V(ds):	3.36667	voltage
Id(M1):	0.000163333	device_current
Ig(M1):	0	device_current
Ib(M1):	-3.37667e-012	device_current
Is(M1):	-0.000163333	device_current
I(Rd):	0.000163333	device_current
I(R2):	3.33333e-005	device_current
I(R1):	3.33333e-005	device_current
I(V1):	-0.000196667	device_current

$$Err_{V_{DS}} = \frac{|3.37-3.36667|}{3.37} = 0.000988 = 0.09\%$$

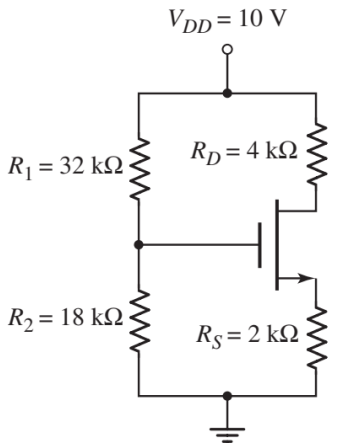
$$Err_{I_D} = \frac{|163-163.333|}{163} = 0.00204 = 0.20\%$$

Problem 12.3-4.b.1:

Adapted from Problem 3.26 on page 197 by changing some values, switching eNMOS to ePMOS.

Design

Considering the circuit below, assume that the transistor is instead an ePMOS, R_S and R_D are swapped, $V_{TP} = 0.75V$, $K_p = 0.25mA/V^2$, and $V_{DD} = 12V$. Calculate V_{SG}, I_D, and V_{SD}.



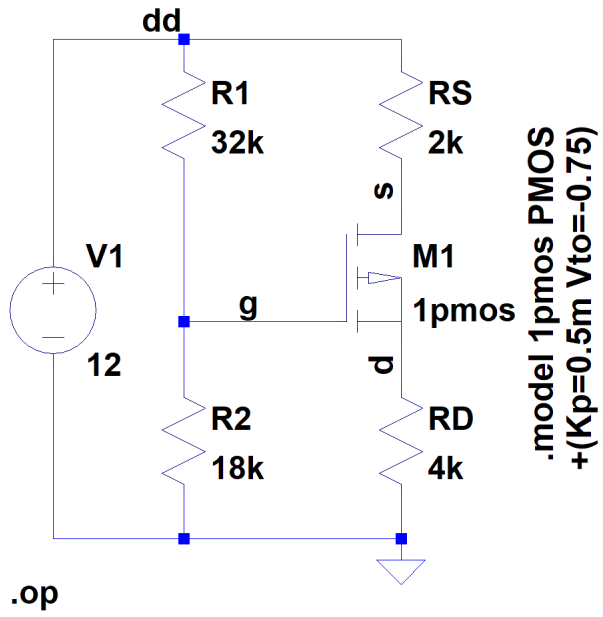
$$V_G = \frac{R_2}{R_1 + R_2}(V_D D) = \frac{18k\Omega}{32k\Omega + 18k\Omega}(12V) = 4.32V$$
$$V_{SG} = V_{DD} - V_G = 12V - 4.32V = 7.68V$$
$$I(R_1) =$$
$$I(R_2) = \frac{V_{DD} - V_G}{R_1} = \frac{12V - 7.68V}{32k\Omega} = 0.24mA$$

$$
\begin{aligned}
& V_{DD} - I_D(R_S + R_D) = V_{SG} + V_T \\
\implies & V_{DD} - K_P(V_{SG} + V_T)^2(R_S + R_D) = V_{SG} + V_T \\
\implies & 12V - (0.25mA/V^2)(V_{SG} - 0.75V)^2(2k\Omega + 4k\Omega) = V_{SG} - 0.75V \\
\implies & V_{SG} = 3.264V
\end{aligned}
$$

$$
\begin{aligned}
V_{SD} &= V_{SG} + V_T = 3.264V - 0.75V = 2.514V \\
I_D &= K_P(V_{SG} + V_T)^2 = (0.25mA/V^2)(3.264V - 0.75V)^2 = 1.58mA
\end{aligned}
$$

Validation

LTSpice Implementation (values within $< 1\%$)



V(dd):	12	voltage
V(g):	4.32	voltage
V(s):	8.2186	voltage
V(d):	7.56279	voltage
Id(M1):	0.00195211	device_current
Ig(M1):	-0	device_current
Ib(M1):	-0.00102718	device_current
Is(M1):	-0.000924925	device_current
I(Rd):	0.0018907	device_current
I(Rs):	0.0018907	device_current
I(R2):	0.00024	device_current
I(R1):	0.00024	device_current
I(V1):	-0.0021307	device_current

Note to grader: This problem gave me a lot of trouble. I know the results deviate from the simulation. If you could leave a note explaining where I messed up, that would be greatly appreciated.

This assignment should demonstrate a basic understanding of MOSFET transistor circuits.

I have neither given nor received unauthorized assistance on this assignment.