Homework 5

ECE3544 CRN:82989

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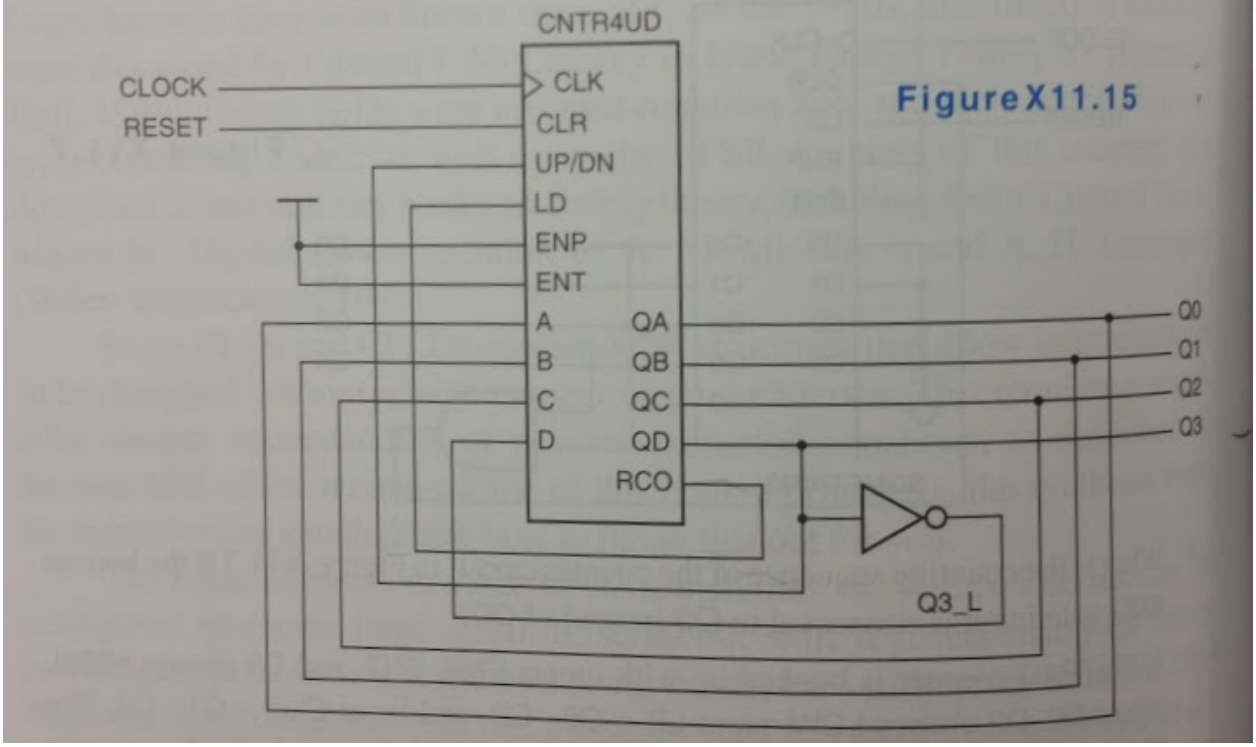
Note: Did not complete in time due to failure to scheduling failure.

Problem 1:

11.15 A CNTR4UD is a 4-bit up/down counter with the same inputs and outputs as the CNTR4U binary counter, plus an UP/DN input that controls whether it counts up (UP/DN=1) or down. The function of the RCO output also depends on UP/DN; it is asserted in state 1111 when counting up, and 0000 when counting down. What is the counting sequence of the circuit shown in Figure X11.15?



FigureX11.15

Problem 2: Design a modulo-16 counter, using one `CNTR4UD` (see problem 1) and at most one discrete logic gate, with the following counting sequence: 7, 6, 5, 4, 3, 2, 1, 0, 8, 9, 10, 11, 12, 13, 14, 15, 7, …

Program 11-1 Verilog module for CNTR4U 4-bit universal binary counter

```
module Vrcntr4u( CLK, CLR, LD, ENP, ENT, D, Q, RCO );
  input CLK, CLR, LD, ENP, ENT;
  input [3:0] D;
  output reg [3:0] Q;
  output reg RCO;

  always @ (posedge CLK)  // Create the counter f-f behavior
    if (CLR == 1)                              Q <= 4'd0;
    else if (LD == 1)                          Q <= D;
    else if ((ENT == 1) && (ENP == 1))  Q <= Q + 1;
    else                                       Q <= Q;

  always @ (Q or ENT)      // Create RCO combinational output
    if ((ENT == 1) && (Q == 4'd15))     RCO = 1;
    else                                       RCO = 0;
endmodule
```

Create a Verilog model based upon the code in the program above and show the correct operation of your design.

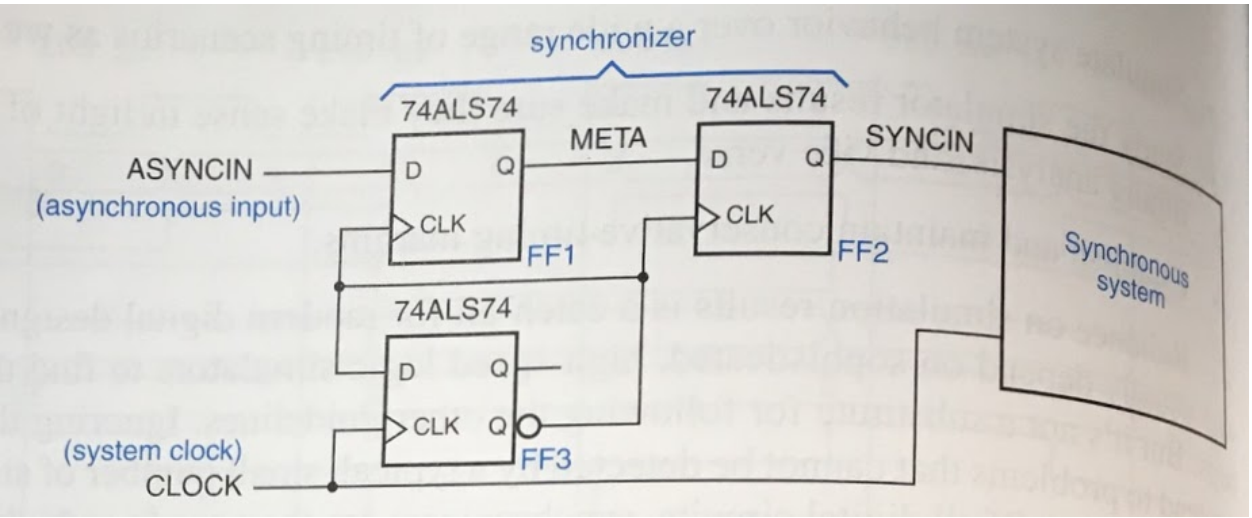
Problem 3:

Problem 4: Given what you know now about set-up and hold times, re-examine the circuit from project 2 and estimate the minimum clock period if the set-up time for the 74821 register is 4ns and the hold time is 2ns. You can assume the typical delays for the 7485 and the default delay for the eleven-bit counter. Below are the delays for the 7485 in nanoseconds.

```
specify
  (a_in, b_in => oa_lt_b) = (16);
  (a_in, b_in => oa_gt_b) = (16);
  (a_in, b_in => oa_eq_b) = (14);
  (ia_lt_b, ia_eq_b, ia_gt_b => oa_lt_b) = (11);
  (ia_lt_b, ia_eq_b, ia_gt_b => oa_gt_b) = (11);
  (ia_gt_b => oa_eq_b) = (9);
endspecify
```

$t_{setup} = 4ns + 16ns = 20ns$
$t_{margin} = 9ns - 2ns = 7ns$
$T = 20ns + 7ns = 27ns$
$f = \frac{1}{27ns} = 37.04MHz$

Problem 5: Calculate the MTBF of the synchroniser shown in the figure below, assuming a clock frequency of 30MHz and an asynchronous transition rate of 2 MHz. Assume that the set-up time t_{setup} and the propagation delay t_{pd} from clock to Q or QN in a 74ALS74 are both 10ns.



$t_r = \frac{1}{30MHz} - 10ns = 23.33ns$
$MTBF = e^{\frac{23.33ns}{}}$

Problem 6: Create a Verilog model of the circuit from problem 5 and verify that its operation is the same as described by your answer to problem 5. The reset signal is not shown on the schematic; you'll need to reset the flip-flops at the beginning of your simulation. You can use the D flip-flop modules from the previous homework.