# Homework 1

ECE3544 CRN:82989

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**Problem 1:** Using 2's complement arithmetic, add the following decimal numbers, showing all work. i.e. perform $17 + 19$. Use the smallest number of bits possible to represent each number and the sum without overflow.

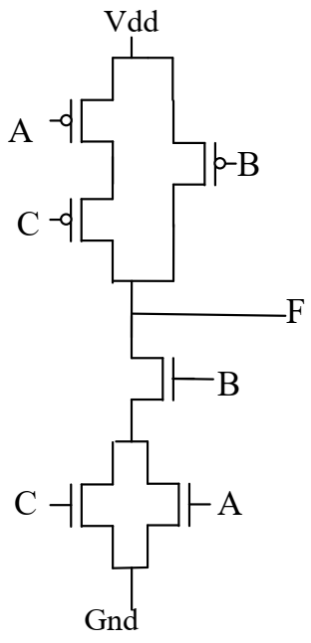
$$17 + 19 =$$

**Problem 2:** For the addition in problem 1, use one less bit to represent the numbers and show how the overflow can be detected.

**Problem 3:** Using the same guidelines as for problem 1, subtract decimal $87$ from $37$, i.e. perform $37 - 87$.

**Problem 4:** Give the hexadecimal representation of the answer to problem 3.

**Problem 5:** Write the truth table and Boolean function implemented by the CMOS gate below.




| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

**Problem 6:** Draw transistor schematics of a CMOS gate for each of the following Boolean functions:

a) $F = \overline{(W + Z) \cdot (Y + X)}$

b) $G = \overline{(B + C + D) \cdot A}$

**Problem 7:** Which would you expect to have a bigger effect on the power consumed by a CMOS circuit, a $5\%$ increase in the power supply voltage ($V_{dd}$)or a $10\%$ increase in total capacitance?Briefly explain your answer.