Homework 12

ECE2504 CRN:82729

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Question 1: (5 pts) Draw the logic diagram of a 4-bit register with function selection inputs S_1 and S_0. The register is to operate according to the following function table.

S_1S_0	Register Operation
00	Clear
01	Increment
10	Hold
11	Parallel Load

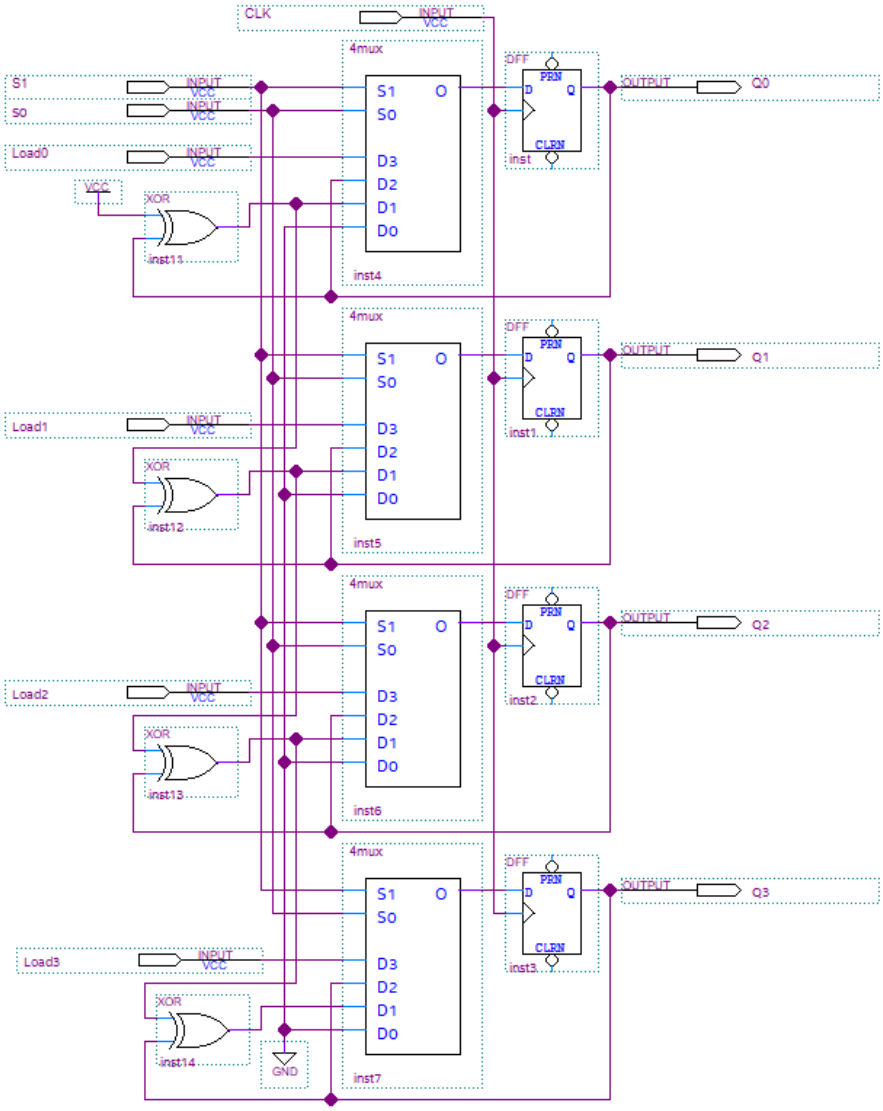

Figure 1: Question 1 Logic Diagram

Question 2: (6 pts) Implement the logic required to implement the following register transfers between three registers $R0$, $R1$, and $R2$.

$$C_A : R1 \leftarrow R0$$
$$C_B : R0 \leftarrow R1, R2 \leftarrow R0$$
$$C_C : R1 \leftarrow R2, R0 \leftarrow R2$$

The control variables C_i are mutually exclusive (only one can be high at a time). No transfer should occur when all control variables are equal to 0. Using registers and multiplexers, draw a detailed logic diagram of the hardware that implements a single bit of these register transfers. Include the logic required to map the control variables C_A, C_B, C_C as inputs to the mux select bits and the load signals for registers.

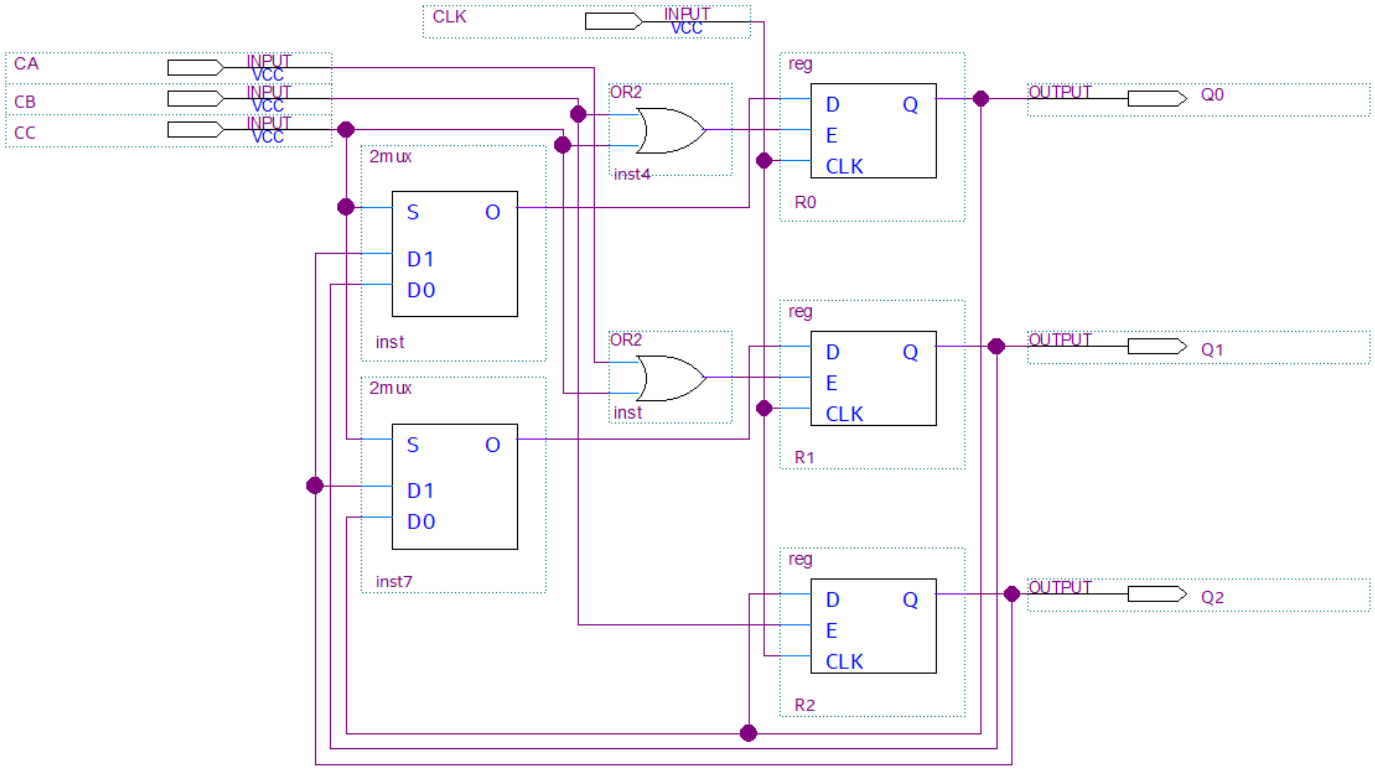

Figure 2: Question 2 Logic Diagram

Question 3: (4 pts) The content of a 4-bit register is initially 0111. The register is shifted four times to the right with the data sequence 1011 as the serial input. (The leftmost bit of the sequence is the first bit of the sequence.) What is the content of the register after each shift?

Initial Register Contents	0111
Shift Right #1	1011
Shift Right #2	0101
Shift Right #3	1010
Shift Right #4	1101

Question 4: (6 pts) Draw the block diagram for the hardware that implements the following statement.

$$T_3 + yT_0S_1 : A \leftarrow A \wedge B, B \leftarrow 0$$

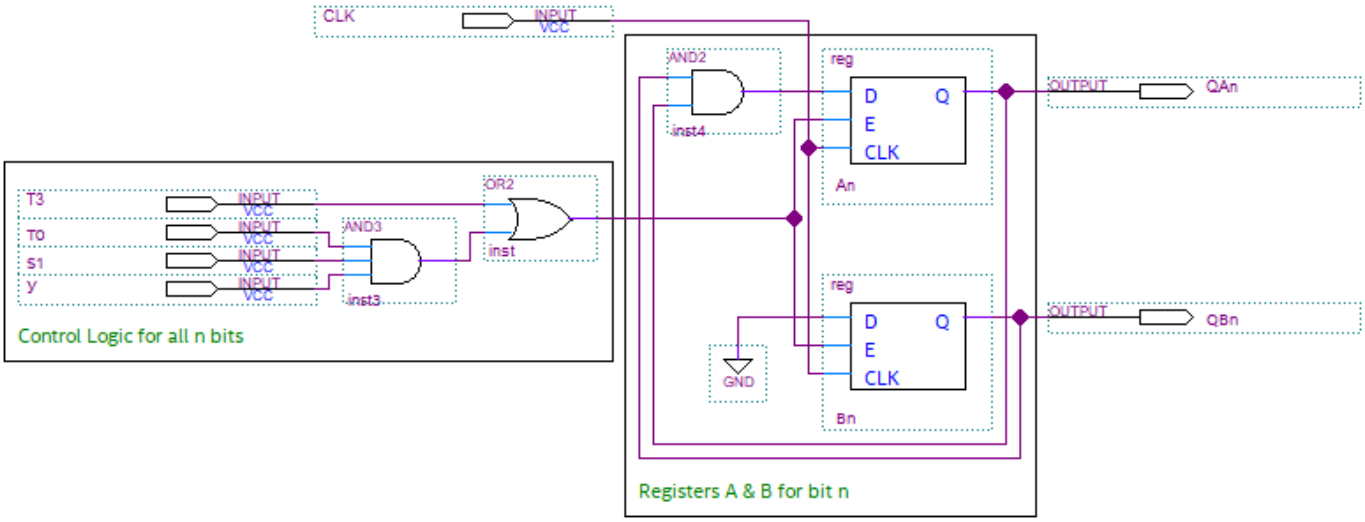

Figure 3: Question 4 Logic Diagram

where A and B are two n-bit registers and y, T_0, T_3, and S_1 are control variables. Include the logic gates for the control function.
Hint: Recall that the symbol + designates an OR function in the control or Boolean function and an arithmetic plus in a microoperation.

Question 5: Consider a 2M × 16 main memory that is built using 256K × 16 RAM chips.
(1 pt each)

a) How many chips are required? **8 256K x 16 chips**

b) How many address bits are required for each chip? **18 address bits**

c) How many address bits are required for the entire memory? **21 address bits**

d) What is the largest unsigned binary number that can be contained in a single word of this memory? Give your answer in decimal. **65535**

e) What is the largest positive 2's complement number that can be contained in a single word of this memory? Give your answer in decimal. **32767**

(3 pts each)

f) Configure the 256K × 16 RAM chips to form 2M 16-bit words using high order interleaving (block diagram).

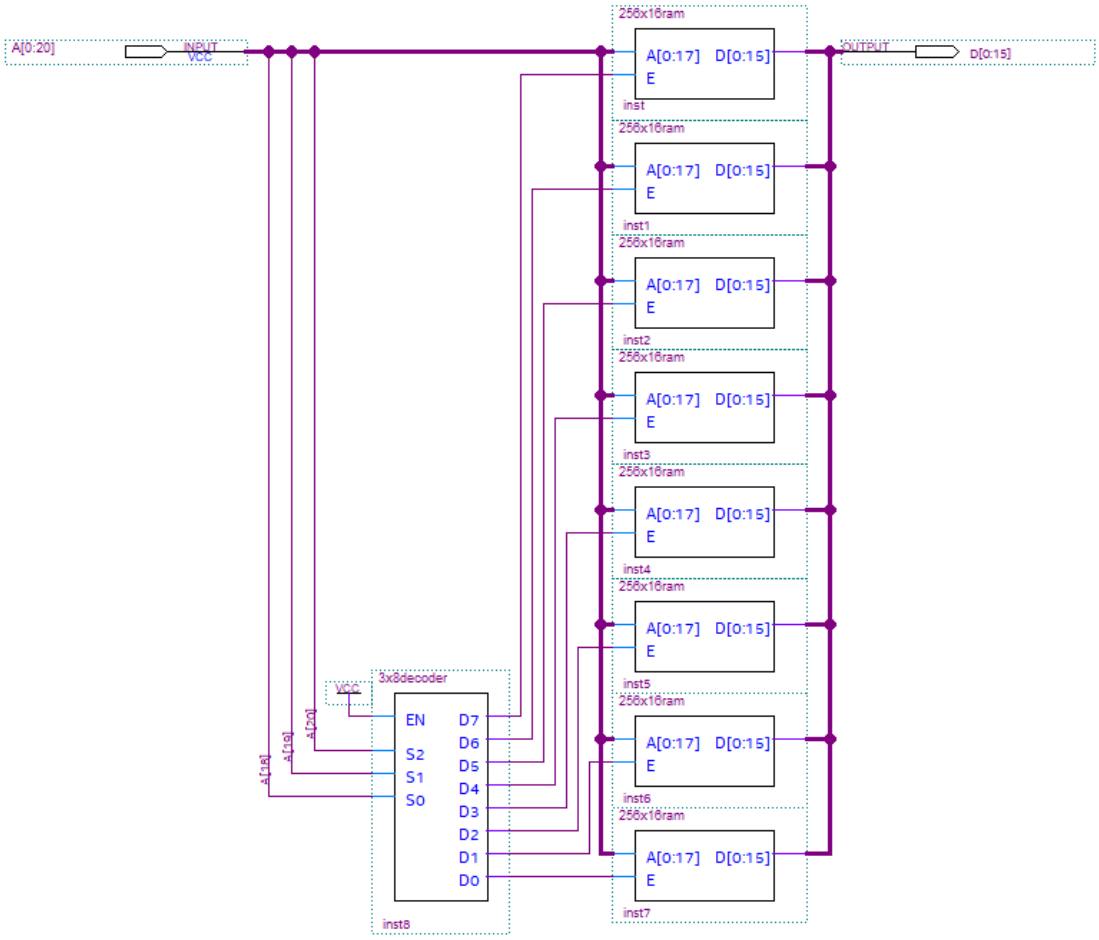

Figure 4: High Order Interleaving Logic Diagram

g) Now assume the memory is 2M x 32. Configure eight 512K × 16 RAM chips to form 2M 32-bit words using high order interleaving (block diagram).

GRADING SCALE

Total: 32 pts

Pts	0	4	8	12	16	20	24	28
Letter Grade	D-	D	C-	C	B-	B	A-	A