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Optional instruction implemented: [Yes] No

Validation Instructions

For the DIP switch settings, SW[3:1] values from 000 to 101 select registers R0-R5, with SW[0] selecting between the most significant byte (SW[0]=1) and the least significant byte (SW[0]=0) being displayed on the LEDs. The PC register is displayed for SW[3:1] = 110.

1. Program the FPGA on the DE0 Nano board using the Start button on the programmer window.
2. When the programming has successfully completed, reset the design by pressing and holding KEY0, and while keeping KEY0 pressed, pressing and releasing the KEY1 pushbutton.
3. Set the DIP switches to "1100" to show the program counter (PC). Press and release KEY1 two times. The LEDs should read 0x02.
4. Set the DIP switches SW[3:1] to "001", and then use SW[0] to record the 16-bit value for R1 in Table 1 (next page) as four digit hex.

6. Press and release KEY1 (PC = 0x03). Set the SW[3:1] for R4, and record the 16-bit value for R4 as four digit hex in Table 1.
7. Press and release KEY1 (PC = 0x04). Set the SW[3:1] for R2, and record the 16-bit value for R2 as four digit hex in Table 1.
8. Press and release KEY1 (PC = 0x05). Set the SW[3:1] for R3, and record the 16-bit value for R4 as four digit hex in Table 1.
9. Press and release KEY1 (PC = 0x06). Set the SW[3:1] for R4, and record the 16-bit value for R3 as four digit hex in Table 1.
10. Press and release KEY1. Set the SW[3:1] for R5, and record the 16-bit value for R4 as four digit hex in Table 1.
11. Press and release KEY1. Set the SW[3:1] for R5, and record the 16-bit value for R5 as four digit hex in Table 1.
12. If the student has implemented the optional instruction: Press and release KEY1. Set the SW[3:1] for R0 and then the PC, and record the 16-bit values for R0 and the PC register as four digit hex in Table 1.

Table 1: Checking the operation of the CPU.

All values of the registers should be recorded as four digit hexadecimal numbers, two digits for the most significant byte of the register and two digits for the least significant byte.

DIP switch settings SW[3:1]

- Values from 000 to 101 select Registers R0 – R5.
- The PC register is displayed for SW[3:1] = 110.
- SW[0] selects between the most significant byte (SW[0]=1) and the least significant byte (SW[0]=0) being displayed on the LEDs.

4	0x02	R1	001	___ ___	___ ___
6	0x03	R4	100	___ ___	___ ___
7	0x04	R2	010	___ ___	___ ___
8	0x05	R3	011	___ ___	___ ___
9	0x06	R4	100	___ ___	___ ___
10	0x07	R5	101	___ ___	___ ___
11	0x08	R5	101	___ ___	___ ___
12 (optional)	0x09	R0	000	___ ___	___ ___
12 (optional)	0x09	PC	110	___ ___	___ ___

Comments (only required if something is unusual or wrong):