Homework 8

ECE2504 CRN:82729

Jacob Abel

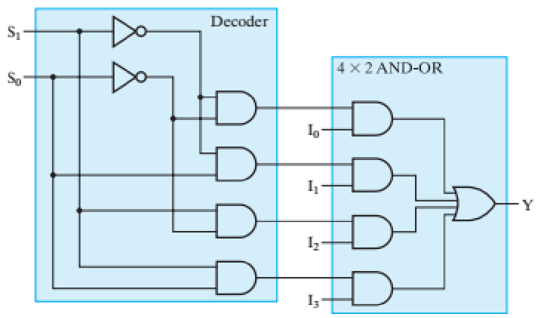
October 17, 2017

Question 1: Determine the propagation delay of the following circuits in terms of the gate propagation delays.

t_{pdNOT} : propagation delay of an inverter
t_{pdAND} : propagation delay of a 2-input AND gate
t_{pdOR} : propagation delay of a 2-input OR gate

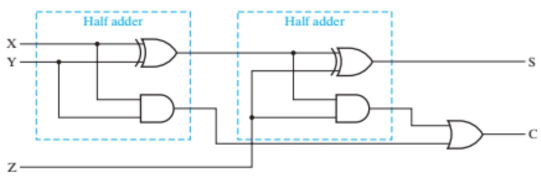
Give your answers in a form similar to $5t_{pdAND} + 2t_{pdOR} + 3t_{pdNOT}$

a) (2 pts) 4x1 multiplexer (see Figure 3-25)



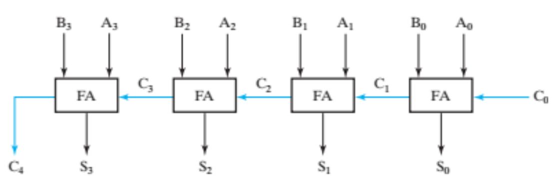
$$t_{pd4x1Mux} = t_{pdNOT} + 2t_{pdAND} + t_{pdOR}$$

b) (2 pts) Full adder (see Figure 3-42)



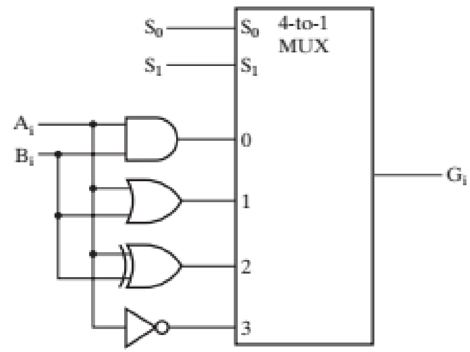
$$\begin{aligned} t_{pdFA} &= t_{pdAND} + t_{pdOR} + t_{pdXOR} \\ &= t_{pdAND} + t_{pdOR} \\ &+ t_{pdAND} + t_{pdOR} + t_{pdNOT} \\ &= 2t_{pdAND} + 2t_{pdOR} + t_{pdNOT} \end{aligned}$$

c) (2 pts) 4-bit ripple carry adder (see Figure 3-43)



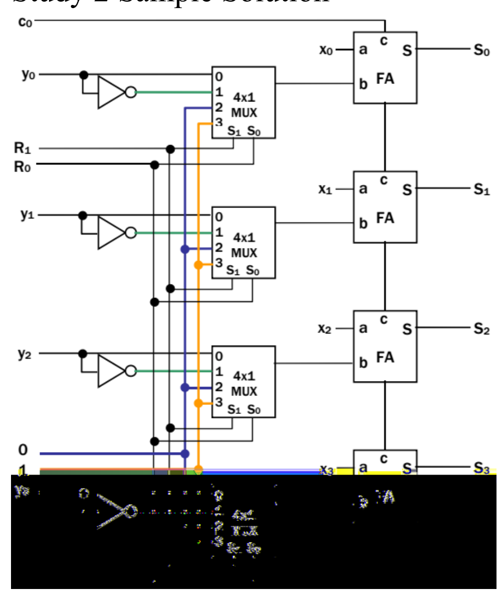
$$\begin{aligned} t_{pdRippleAdder} &= 4t_{pdFA} \\ &= 4(2t_{pdAND} + 2t_{pdOR} + t_{pdNOT}) \\ &= 8t_{pdAND} + 8t_{pdOR} + 4_{pdNOT} \end{aligned}$$

d) (2 pts) the logic circuit shown in Figure 8-6



$$\begin{aligned} t_{pd} &= t_{pdXOR} + t_{pd4x1Mux} \\ &= t_{pdAND} + t_{pdOR} + t_{pdNOT} \\ &+ t_{pdNOT} + 2t_{pdAND} + t_{pdOR} \\ &= 3t_{pdAND} + 2t_{pdOR} + 2_{pdNOT} \end{aligned}$$

e) (2 pts) the arithmetic circuit shown in the Case Study 2 Sample Solution



$$\begin{aligned} t_{pd} &= t_{pdXOR} + t_{pd4x1Mux} \\ &= t_{pdAND} + t_{pdOR} + t_{pdNOT} \\ &+ t_{pdNOT} + 2t_{pdAND} + t_{pdOR} \\ &+ 2t_{pdNOT} + 3t_{pdAND} + 2t_{pdOR} \end{aligned}$$

Question 2: (5 pts) Use contraction beginning with a 4-bit adder to design a 4-bit circuit that subtracts 4 from the 4-bit input. The function to be implemented is $Z = X - 4$. What does contraction mean? Do this:

- Recall the Boolean expressions for full adders. $S_i = A_i \oplus B_i \oplus C_i$ and $C_{i+1} = A_iB_i + A_iC_i + B_iC_i$
- Substitute for the known values in the equations for all four full adders to simplify the expression. For example, if $A = 0001$, $A_3 = 0$, $A_2 = 0$, $A_1 = 0$, $A_0 = 1$, which will result in terms such as A_3B_3 reducing to 0.
- Recall the necessary B and C_0 inputs to subtract using a 4-bit adder.

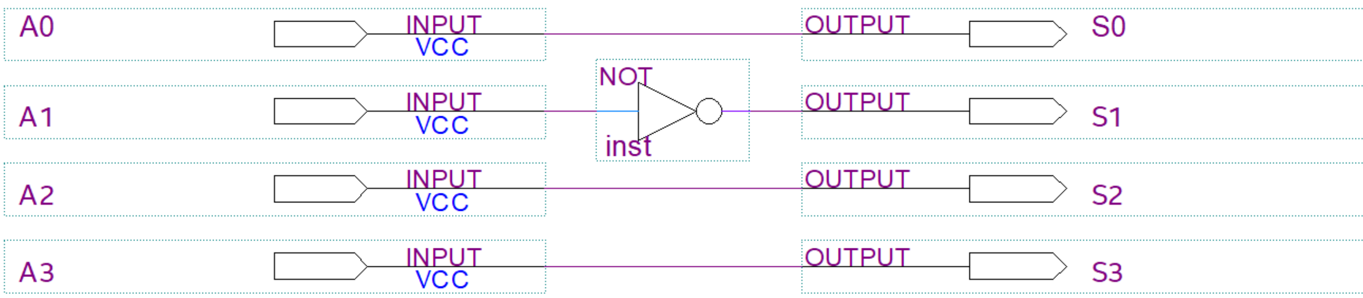
$$\begin{aligned} B &= \overline{0010} = 1101 \\ C_0 &= 1 \end{aligned}$$

$$\begin{aligned} S_0 &= (A_0 \oplus 1) \oplus 1 = A_0 \\ C_0 &= A_0 1 + A_0 1 + 1(1) = 1 \end{aligned}$$

$$\begin{aligned} S_2 &= (A_2 \oplus 1) \oplus 1 = A_2 \\ C_2 &= A_2 1 + A_2 1 + 1(1) = 1 \end{aligned}$$

$$\begin{aligned} S_1 &= (A_1 \oplus 0) \oplus 1 = \overline{A_1} \\ C_1 &= A_1 0 + A_1 1 + 0(1) = 1 \end{aligned}$$

$$\begin{aligned} S_3 &= (A_3 \oplus 1) \oplus 1 = A_3 \\ C_3 &= A_3 1 + A_3 1 + 1(1) = 1 \end{aligned}$$



Question 3: (10 pts) Design a combinational circuit that increments its 3-bit input when $S = 0$ and decrements its input when $S = 1$. (Note that incrementing means adding 001 and decrementing means subtracting 001 using 2cm arithmetic.)

a) Design a simplified 2-level circuit plus inverters as needed for the inputs. (Hint: This means use K maps.)

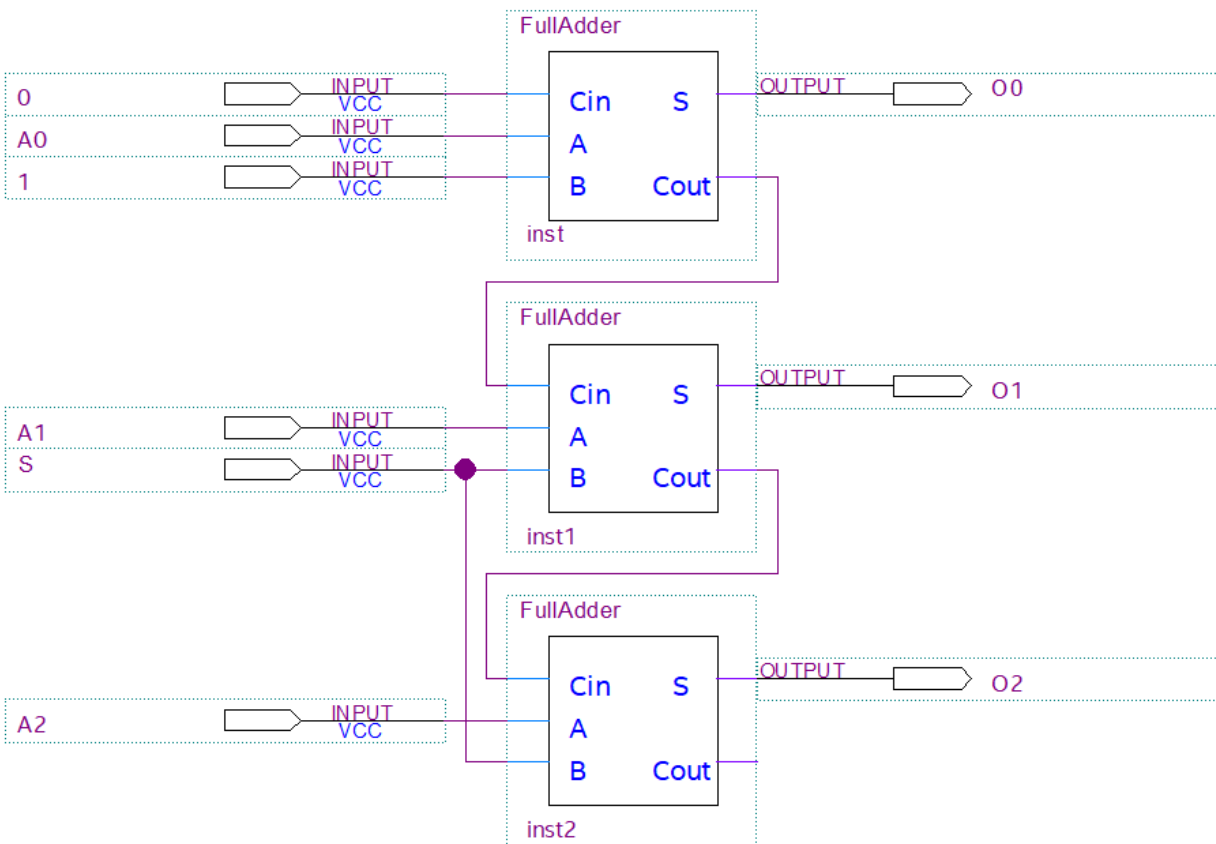
B_2 \ S	0	1
0	0	1
1	0	1

B_1 \ S	0	1
0	0	1
1	0	1

B_0 \ S	0	1
0	1	1
1	1	1

$B_2 = S$ $\quad$ $B_1 = S$ $\quad$ $B_0 = 1$

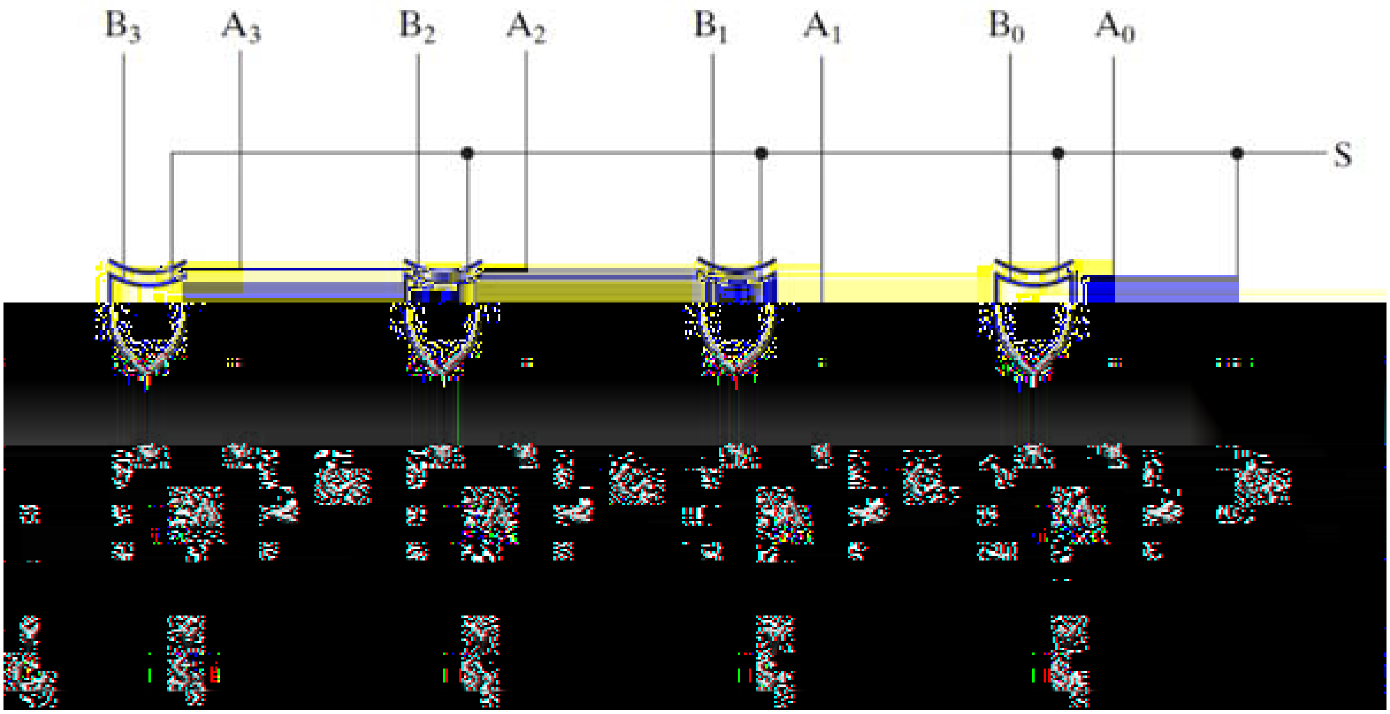
b) Start with a 3-bit ripple carry adder and use a process similar to Case Study 2 to design the circuit.



c) Determine the (2-input) gate count and propagation delay for parts a and b. Use a form similar to Problem 1

$$
\begin{aligned}
t_{pdb} =& 3t_{pdFA} \\
=& 6t_{pdAND} + 6t_{pdOR} + 3t_{pdNOT}
\end{aligned}
$$

Question 4: (5 pts) Consider the adder-subtractor circuit shown in the figure below. For the following inputs, determine the values of the outputs S_3, S_2, S_1, S_0, and C_4.



S	A	B	$A+(B\oplus S)$	$S_3S_2S_1S_0$	C_4
1	1010	0111	1010+1001	0011	1
0	0111	0110	0111+0110	1001	0
0	1010	1101	1010+1101	0111	1
1	1010	0011	1010+1101	0111	1
1	0111	1001	0111+0111	1110	0

GRADING SCALE

Total: 30 pts

Pts	0	3	7	11	15	18	22	26
Letter Grade	D-	D	C-	C	B-	B	A-	A