Homework 1

ECE2500 CRN:82943

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Problem 1: There are many different examples of Instruction Set Architectures (ISAs).Give three examples of ISAs other than MIPS. For each example, give the following details:

- What differentiates the ISA from MIPS?
- What similarities does the ISA share with MIPS?
- What devices or applications most often use the ISA?

1. x86
    - Unlike MIPS, x86 is a CISC architecture and therefore is more expensive to implement. x86 also has a variable instruction width unlike MIPS. Also x86 is little endian while MIPS can be either big or little endian.
    - Both MIPS and x86 are register based ISAs.
    - Most modern laptops and desktops are x86.
2. ARM
    - ARM often implements branch prediction and has an extremely varied/heterogeneous architecture unlike MIPS which despite allowing extensions, tends to be much more homogeneous.
    - Both ARM and MIPS are RISC ISAs, have fixed instruction widths, and are bi-endian.
    - Mobile devices and IoT devices often use ARM.
3. z/Architecture
    - z/Architecture is primarily big endian, is CISC instead of RISC, and has variable width instructions unlike MIPS.
    - MIPS and z/Architecture are largely dissimilar except that they are both register based architectures.
    - This ISA is primarily used on IBM mainframes.

Problem 2: Assume that the base address of the array, A, is stored in $\$s0$. The following table gives the memory addresses of $A[0], \ldots, A[3]$ along with the values stored in the corresponding memory location.

	Stored Value	Memory Address
$A[0]$	-3	4
$A[1]$	7	8
$A[2]$	-6	12
$A[3]$	11	16

What are the values stored in registers $\$s0$, $\$s1$, $\$s2$, and $\$s3$ after executing the following MIPS instructions?

Instructions	Changed Values
`sw $s0, 0($s0)`	A[0]=4, $s0=4
`lw $s1, 0($s0)`	A[0]=4, $s0=4, $s1=4
`lw $s2, 8($s0)`	A[0]=4, $s0=4, $s1=4, $s2=–6
`add $s3, $s1, $s2`	A[0]=4, $s0=4, $s1=4, $s2=–6, $s3=–2

Final Register Values: $\$s0 = 4$, $\$s1 = 4$, $\$s2 = -6$, $\$s3 = -2$

Problem 3: Convert each of the following C statements into MIPS instructions. Assume that the variables a, b, and c are stored in \$$s0$, \$$s1$, and \$$s2$, respectively. The base addresses of the arrays A and B are stored in \$$s3$ and \$$s4$, respectively. Assume the arrays A and B contain integers.

1. $b = c - B[2^{17}]$

```
lui   $s1, 0x0008
addu  $s1, $s1, $s4
lw    $s1, 0($s1)
sub   $s1, $s2, $s1
```

2. $A[3] = b + a + 2^{11}$

```
addi  $t0, $s0, 0x0800
add   $t0, $t0, $s1
sw    $t0, 12($s3)
```

3. $B[5] = A[6] - c + B[b]$

```
lw    $t0, 24($s3)
sll   $t1, $s1, 2
addu  $t1, $t1, $s4
lw    $t1, 0($t1)
sub   $t2, $t0, $s2
add   $t2, $t2, $t1
sw    $t2, 20($s4)
```

4. $A[1] = B[a - c] + b - c$

```
sub   $t0, $s0, $s2
sll   $t0, $t0, 2
addu  $t0, $t0, $s4
lw    $t0, 0($t0)
add   $t0, $t0, $s1
sub   $t0, $t0, $s2
sw    $t0, 4($s3)
```