Homework 2

ECE3544 CRN:82989

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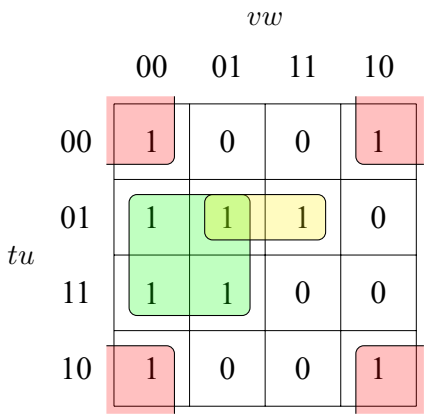
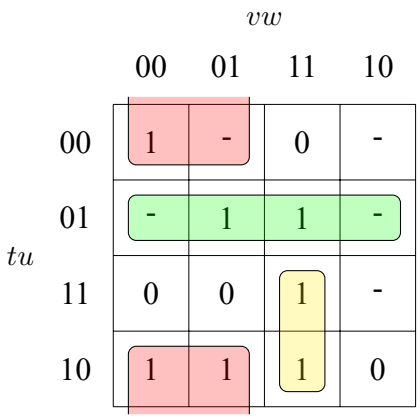
Problem 1: Use a Karnaugh map to find a minimal SOP expression for the function $F(t, u, v, w) = \Sigma(0, 2, 4, 5, 7, 8, 10, 12, 13)$.



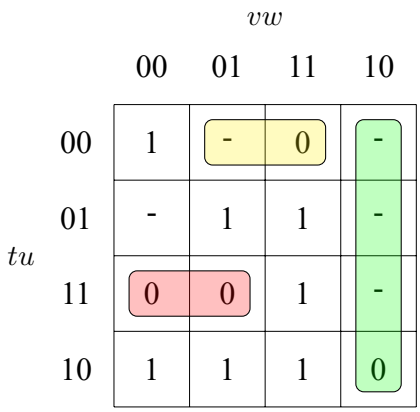
$F(t, u, v, w) = \overline{t}uw + u\overline{v} + \overline{u}\,\overline{w}$

Problem 2: Use a Karnaugh map to find a minimal SOP expression for the function $F(t, u, v, w) = \Sigma(0, 5, 7, 8, 9, 11, 15)$ with don't cares $d(w, x, y, z) = \Sigma(1, 2, 4, 6, 14)$.



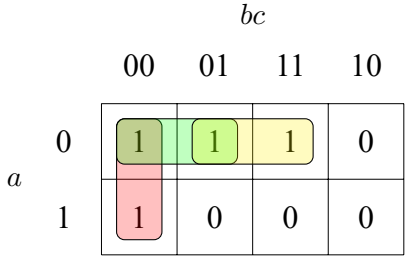
$F(t, u, v, w) = tuw + \overline{t}u + \overline{u}\,\overline{v}$

Problem 3: Using the function F and don't cares d from problem 2, use a Karnaugh map to find a minimal POS function for F.



$F(t, u, v, w) = (t + u + \overline{w})(\overline{t} + \overline{u} + v)(\overline{v} + w)$

Problem 4: Implement a hazard free circuit for F(a, b, c) = Σ(0, 1, 3, 4). In your circuit, show which term(s) are required for the minimal implementation and which term(s) are required to remove the hazard.



$$F_{hazard}(a, b, c) = a + c$$
$$F_{safe}(a, b, c) = a + \overline{a}b + c$$

The term $\overline{a}b$ removes the hazard.

Problem 5: Consider the following two functions:

$$F(a,b,c,d) = (a + \overline{b})(c + (bd)) \tag{1}$$
$$G(a,b,c,d) = (a(c + \overline{d})) + (c + (bd)) \tag{2}$$

For your circuits, you can assume the true and complement forms of the inputs (a, b, c, d) are available, so that you do not need to show inverters on the inputs or include them in the gate count.

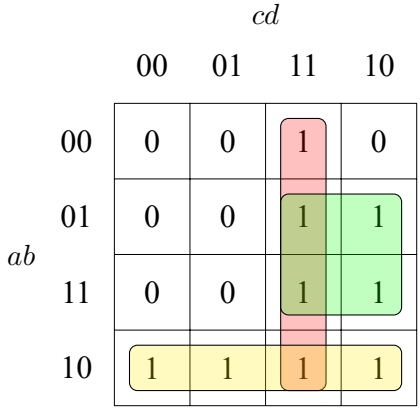
i. Show how to implement the functions using only two input NAND gates and inverters in a multilevel circuit. Share any sub-expressions that you can when implementing the circuit.

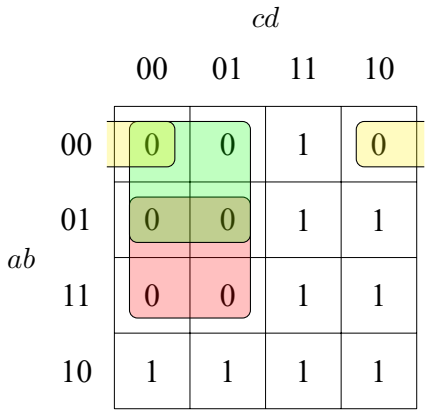
$$\begin{aligned} F(a,b,c,d) &= (a + b')(c + (bd)) \\ &= (a'b)'(c'(bd)''')' \\ &= ((a'b)'(c'(bd)')')'' \end{aligned}$$

$$\begin{aligned} G(a,b,c,d) &= (a(c + d')) + (c + (bd)'') \\ &= (a(c'd)')'' + (c'(bd)''')' \\ &= ((a(c'd)')'''(c'(bd)''')'')' \\ &= ((a(c'd)')'(c'(bd)')'')' \end{aligned}$$

ii. Find the minimized two-level SOP expressions for F and G.

$F(a,b,c,d) = (a+\overline{b})(c+b)(c+d)$ $\qquad$ $G(a,b,c,d) = ac + a\overline{d} + c + bd$





$F(a,b,c,d) = a'b'd' + a'c' + bc'$

iii. Implement the minimized SOP expressions using only two input NAND gates and inverters. Share any sub-expressions that you can when implementing the circuit.

iv. Compare your circuits i and iii in terms of gate counts for NANDs and inverters. Briefly explain which circuit you would rather build.