Homework 1 ECE3544 CRN:82989

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Problem 1: Using 2's complement arithmetic, add the following decimal numbers, showing all work. i.e. perform 17 + 19. Use the smallest number of bits possible to represent each number and the sum without overflow.

$$17 + 19 = 010001 + 010011$$

$$= 010010 + 010010$$

$$= 010100 + 010000$$

$$= 100100$$

$$= 36$$

Problem 2: For the addition in problem 1, use one less bit to represent the numbers and show how the overflow can be detected.

$$17 + 19 = 10001 + 10011$$

= $10010 + 10010$
= $10100 + 10000$
= 00100
= 4

Overflow can be detected during addition for unsigned integers when the most significant bit changes from 1 to 0.

Problem 3: Using the same guidelines as for problem 1, subtract decimal 87 from 37, i.e. perform 37 - 87.

$$37 - 87 = 00100101 - 01010111$$

$$= 00100101 + 10101001$$

$$= 00100110 + 10101000$$

$$= 01001110 + 10000000$$

$$= 11001110$$

$$= -00110010$$

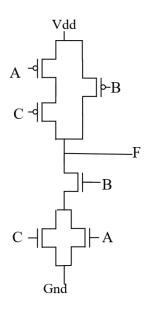
$$= -50$$

Problem 4: Give the hexadecimal representation of the answer to problem 3.

$$37 - 87 = -50$$

= 11001110
= CE_{16}

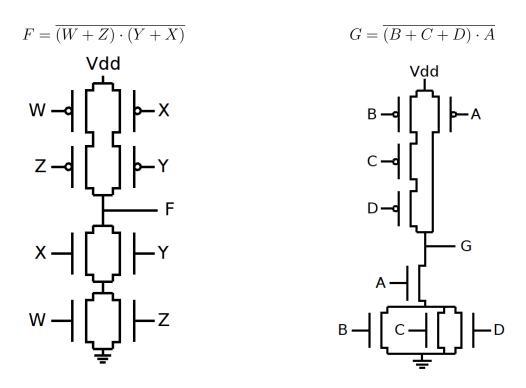
Problem 5: Write the truth table and Boolean function implemented by the CMOS gate below.



Α	В	С	F
0	0	0	1
0	0	1	1
$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$	0	0	1
0	0	1	1
0	1	1	1
0	1	1	1 0
0	1	1	1
0	1	1	0
1	0	1 0	1
1	$0 \\ 0$	1	1
1	0	0	1
1	0	1	1
1	1	1	
1	1	1	0
1	1	0	0
1	1	1	0

$$F = \overline{B \cdot (A + C)}$$

Problem 6: Draw transistor schematics of a CMOS gate for each of the following Boolean functions:



Problem 7: Which would you expect to have a bigger effect on the power consumed by a CMOS circuit, a 5% increase in the power supply voltage (V_{dd}) or a 10% increase in total capacitance? Briefly explain your answer.

$$\begin{split} P &= CV^2 f \implies \Delta P = \Delta C \times (\Delta V)^2 \times \Delta f \\ \Delta C &= 110\% \text{ and } (\Delta V)^2 = (105\%)^2 = 110.25\% \end{split}$$

The voltage increase will have a slightly larger effect.