Project 1

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Contents

List of Tables

List of Figures

Purpose

The purpose
of this circuit was to design, optimise, simulate, and construct a basic combinational circuit. This required basic wiring skills, application of combinational logic design skills, and usage of logic modelling, simulation, and hardware programmer software.

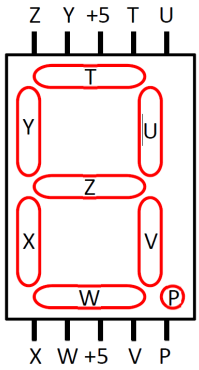


Figure 1: 7-Segment Display Pinout sourced from the ECE2504 Lab Manual

Problem Specification

This project requires that the final circuit convert a 641-2 (4-bit negatively weighted decimal) code into a 7-bit code for a 7-segment display with each lit part of the display corresponding to a 0-value bit. The circuit could be designed with only 2-input NAND gates and inverters. The required software for the modelling and simulation of the circuit was Quartus.

Final deliverables include
a circuit diagram of the completed circuit, a Quartus project archive of the latest revision of the circuit project, and this technical report detailing the project specifications as well as the development history and design process. Table 1 and Table 2 detail the mapping of decimal digits onto both the 641-2 codes as well as the 7-segment display codes. Figure 1 shows the pin mapping for the 7-Segment display.

Decimal	0	1	2	3	4
641-2	0000	0010	0101	0111	0100
Decimal	5	6	7	8	9
641-2	0110	1000	1010	1101	1111

Table 1: 1-digit decimals to 4-bit 641-2 codes sourced from the Project 1 Specifications

0	1	2	3	4
0000001	1001111	0010010	0000110	1001100
5	6	7	8	9
0100100	0100000	0001111	0000000	0001000

Table 2: 7-segment display configurations (TUVWXYZ) sourced from the Project 1 Specifications

Design Process

The first stage of the design process was to identify all necessary input and output variables. The 4-bit input 641-2 code was split into variables A, B, C, and D with A representing the most significant bit. The 7-Segment display bits were assigned to bits T, U, V, W, X, Y, and Z. When grouping the 7-Segment display bits together, T is always the first bit.

Dec	A	B	C	D	T	U	V	W	X	Y	Z
0	0	0	0	0	0	0	0	0	0	0	1
N/A	0	0	0	1	-	-	-	-	-	-	-
1	0	0	1	0	1	0	0	1	1	1	1
N/A	0	0	1	1	-	-	-	-	-	-	-
4	0	1	0	0	1	0	0	1	1	0	0
2	0	1	0	1	0	0	1	0	0	1	0
5	0	1	1	0	0	1	0	0	1	0	0
3	0	1	1	1	0	0	0	0	1	1	0
6	1	0	0	0	0	1	0	0	0	0	0
N/A	1	0	0	1	-	-	-	-	-	-	-
7	1	0	1	0	0	0	0	1	1	1	1
N/A	1	0	1	1	-	-	-	-	-	-	-
N/A	1	1	0	0	-	-	-	-	-	-	-
8	1	1	0	1	0	0	0	0	0	0	0
N/A	1	1	1	0	-	-	-	-	-	-	-
9	1	1	1	1	0	0	0	1	1	0	0

Table 3: 7 Segment Display Truth Table

Immediately following this step, the truth table was laid out. One assumption with this truth table was that non legal 641-2 codes were considered invalid. This resulted in Table 3. Following the completion of the truth table, a K-Map was prepared for each output variable. Figure 2 through figure 8 in Appendix A are the corresponding K-maps for output variables T-Z. With the K-map groupings, it was decided that Sum of Products groupings would be used as Product of Sums groupings tend to take more NAND gates to implement. However, if the project was to be done again with solely NOR gates, Product of Sums would be used.

After the K-maps were grouped the equations for the outputs were derived from the groupings and stored in Table 4. Additionally, common terms were identified and marked in this table.

Output	Sum of Products	$(A'D)$	$(C'D')$	$(BC'D')$	$(B'C)$	(BD')
T	$A'B'C + BC'D'$	0	1	1	1	0
U	$AC'D' + BCD'$	0	1	0	0	0
V	$A'C'D$	1	0	0	0	0
W	$AC + B'C + BC'D'$	0	1	1	1	1
X	$BD' + C$	0	0	0	0	1
Y	$A'D + B'C$	1	0	0	1	0
Z	$A'B' + B'C$	0	0	0	1	0

Table 4: Circuit Instances

Following identification of common terms, all common terms were pulled out of the equations and substituted with variables I through M. These variables as seen in Table 5 exist to simplify the equations and reduce the quantity of gates in use. 9 AND gates and 11 inverters were removed from the circuit. Compared to the optimised circuit with 11 AND gates, 7 OR gates, and 9 Inverters, this results in a 45% decrease in AND gates and a 55% decrease in Inverters. The optimised circuit is still 100% functionally equivalent to the original version.

Variable	Optimised Equation
I	$A'D$
J	$C'D'$
K	$B'C$
L	$(BJ)'$
M	BD'
T	$A'K + L'$
U	$AJ + CM$
V	$C'I$
W	$AC + K + L'$
X	$M + C$
Y	$I + K$
Z	$A'B' + K$

Table 5: Optimised Circuit

Implementation

At this point, the circuit was implemented in Quartus. The final circuit diagram is provided in Appendix B. The final design was then simulated with the results displayed in Table 6. The raw waveform of the simulation is provided in Appendix C. As shown in the table the results are identical to the legal values in Table 3.

Once simulation proved that the circuit was valid in theory, it was programmed onto the DE-0 FPGA development board and the board was wired into an LED with a pinout listed in Table 7 in Appendix D. The 4 dip switches on the board toggled the values of ABCD with DIP3 corresponding to A.

Dec	ABCD	TUVWXYZ
0	0000	0000001
1	0010	1001111
2	0101	0010010
3	0111	0000110
4	0100	1001100
5	0110	0100100
6	1000	0100000
7	1010	0001111
8	1101	0000000
9	1111	0001100

Table 6: Simulation Results

Validation

Final validation of the completed circuit was to cycle through all legal values manually on the FPGA board using the dip switches and the LED 7-Segment display. During this process there were no issues and the circuit worked properly.

Conclusion

This project was a worthwhile exercise that demonstrated knowledge in basic combinational circuit design and technical documentation. The requirements were sufficiently outlined and documented.

Given time to repeat the project, greater investment could be placed in optimising as alternative gate arrangements may have been able to result in a smaller total gate cost or shorter propagation delay. Otherwise, this implementation can be considered a complete success.

Appendix A: Karnaugh Maps

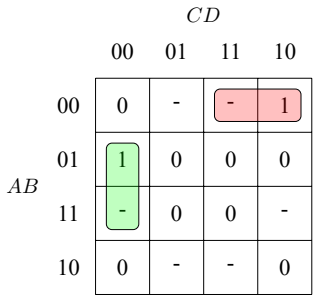


Figure 2: Output T K-Map

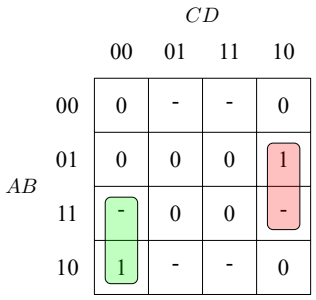


Figure 3: Output U K-Map

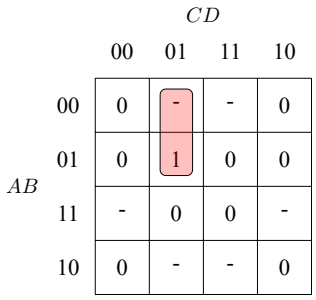


Figure 4: Output V K-Map

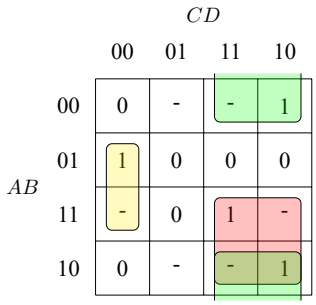


Figure 5: Output W K-Map

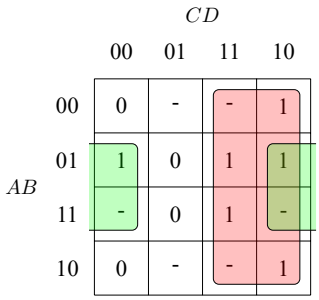


Figure 6: Output X K-Map

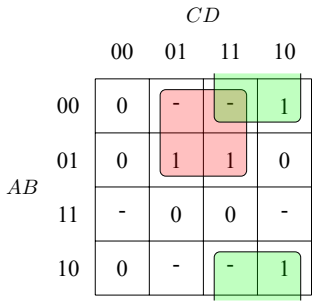


Figure 7: Output Y K-Map

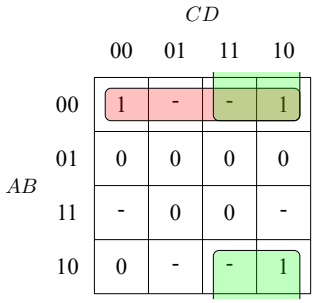
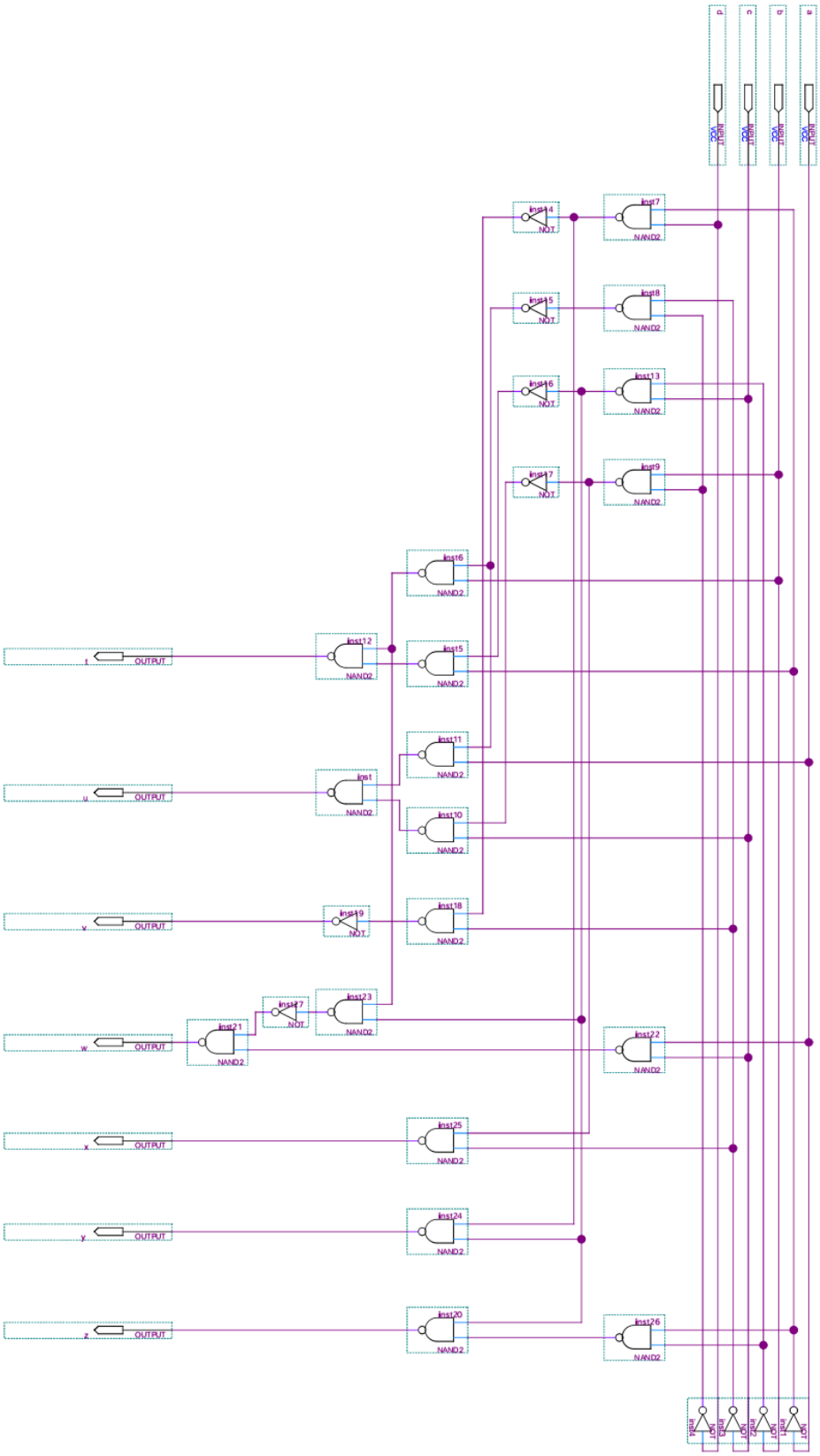
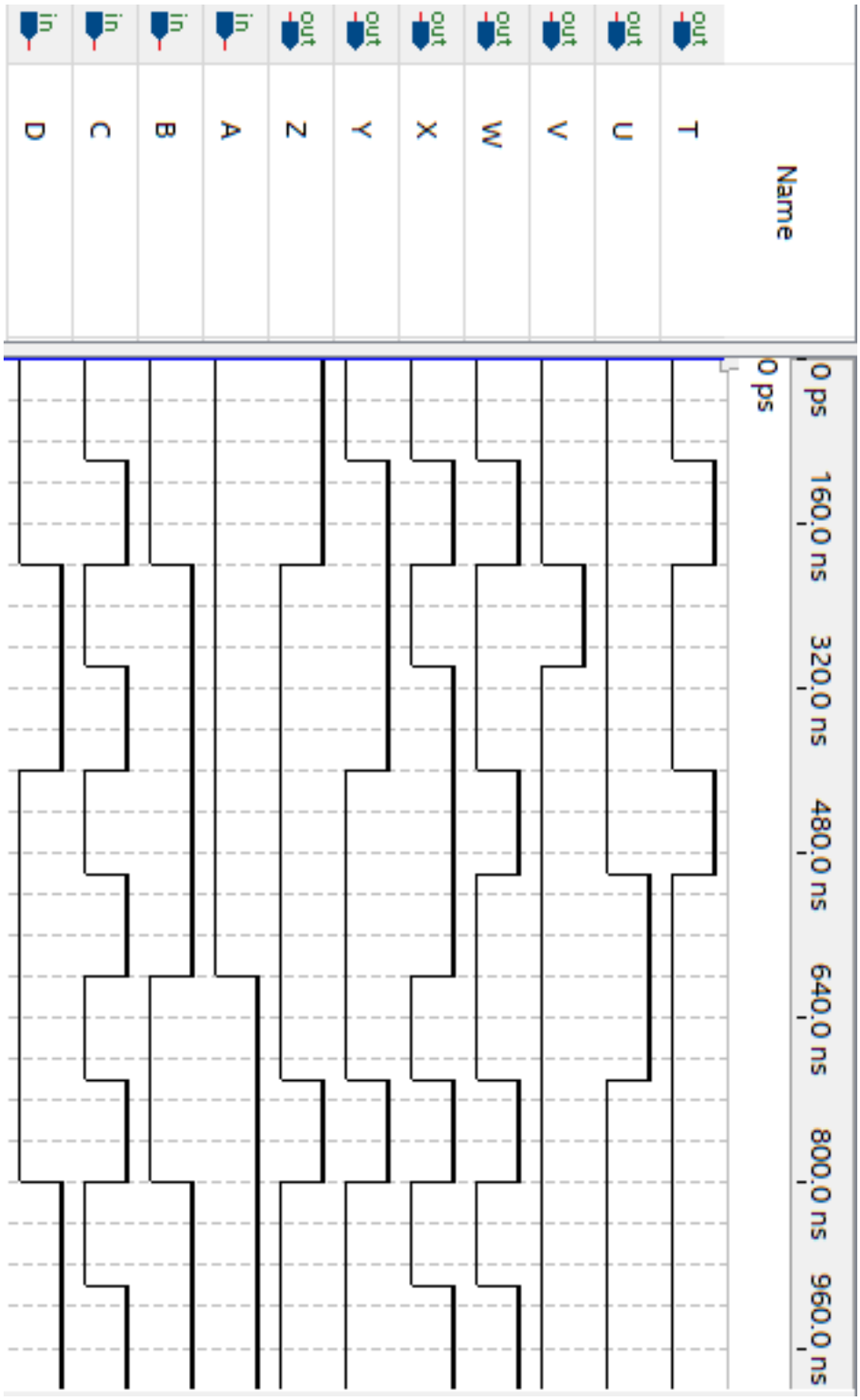


Figure 8: Output Z K-Map

Appendix B: 641-2 To 7-Segment Circuit Diagram



Appendix C: Simulation Waveform



Appendix D: Pinouts and Wiring Charts

LED Pin	DE-0 GPIO Pin
T	GPIO_16 (9)
U	GPIO_14 (7)
V	GPIO_128 (35)
W	GPIO_130 (37)
X	GPIO_132 (39)
Y	GPIO_18 (13)
Z	GPIO_110 (15)
P	Do not connect.
+5V Top	VCC_SYS (11)
+5V Bottom	Do not connect.

Table 7: LED Wiring Chart sourced from the Project 1 Specifications

Variable	Dip Switch
A	DIP3
B	DIP2
C	DIP1
D	DIP0

Table 8: DIP Switch Pinout