ECE 2500: Computer Organization and Architecture (Fall 2018)

Homework 6

Due: November 27th, 11:59PM

November 12, 2018

This homework constitutes 2% of the course grade. You must work on it individually. Your submission must be your original work. Please follow the submission instructions posted on Canvas exactly.

Assume all numbers are in decimal unless explicitly preceded by 0x for hexadecimal and 0b for binary.

Problem 1 (10 points)**.** Explain briefly, the principles of spatial and temporal locality in the context of cache design and memory hierarchy.

Problem 2 (50 points)**.** Suppose we have a cache that can hold a total of 8 blocks with 4 words per block.

1. How many bytes does the cache contain (cache size)?
2. How many bytes does one block contain (block size)?
3. Suppose that the cache is designed as a direct-mapped cache. Compute the block index, block offset, and the tag for the following addresses:
   (a) 0x00000004
   (b) 0x00000014
   (c) 0x01000004
   (d) 0x00000008
   (e) 0x00000018
   (f) 0x01000008

Problem 3 (40 points)**.** Suppose we have a cache that can hold 16 blocks with 2 words per block. Assume that initially the cache is empty. Draw tables to illustrate the state of the cache *after* each of the following data read operations from the processor:

1. Read word from 0x00000000
2. Read word from 0x00000004

3. Read word from 0x00000040

4. Read word from 0x00000020

The rows in the table should correspond to blocks, with columns for tag, block index, valid, and the memory *addresses* of data currently stored in the blocks (if no data is stored in a block, simply put dashes). Also, indicate if the processor will stall in order to complete each read operation.