Homework 10

ECE2504 CRN:82729

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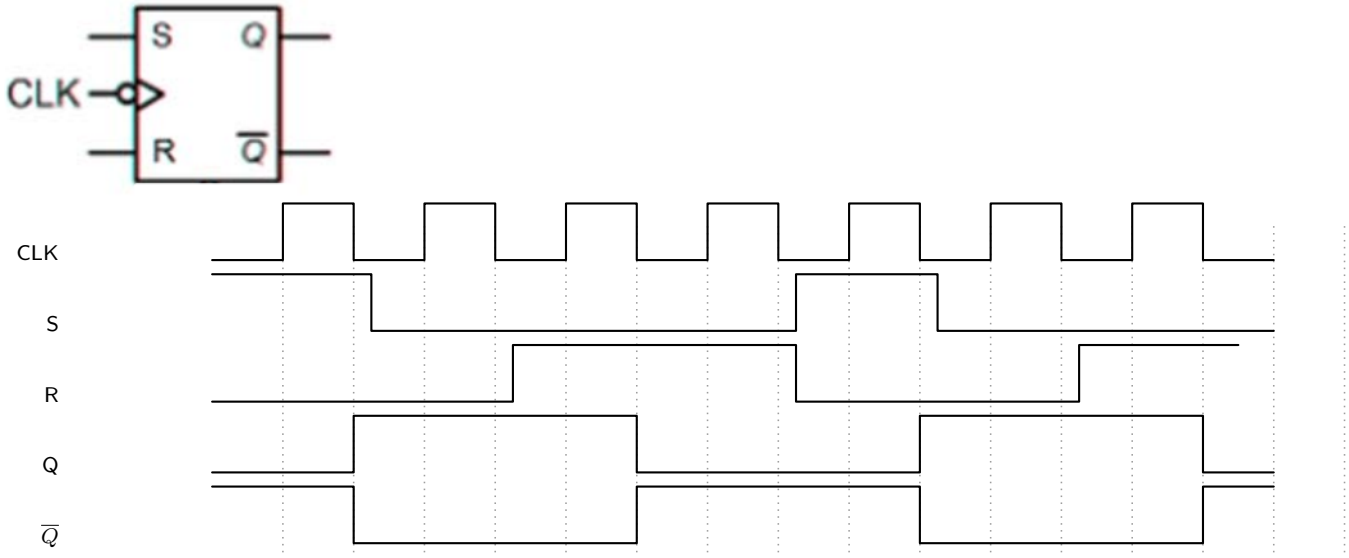
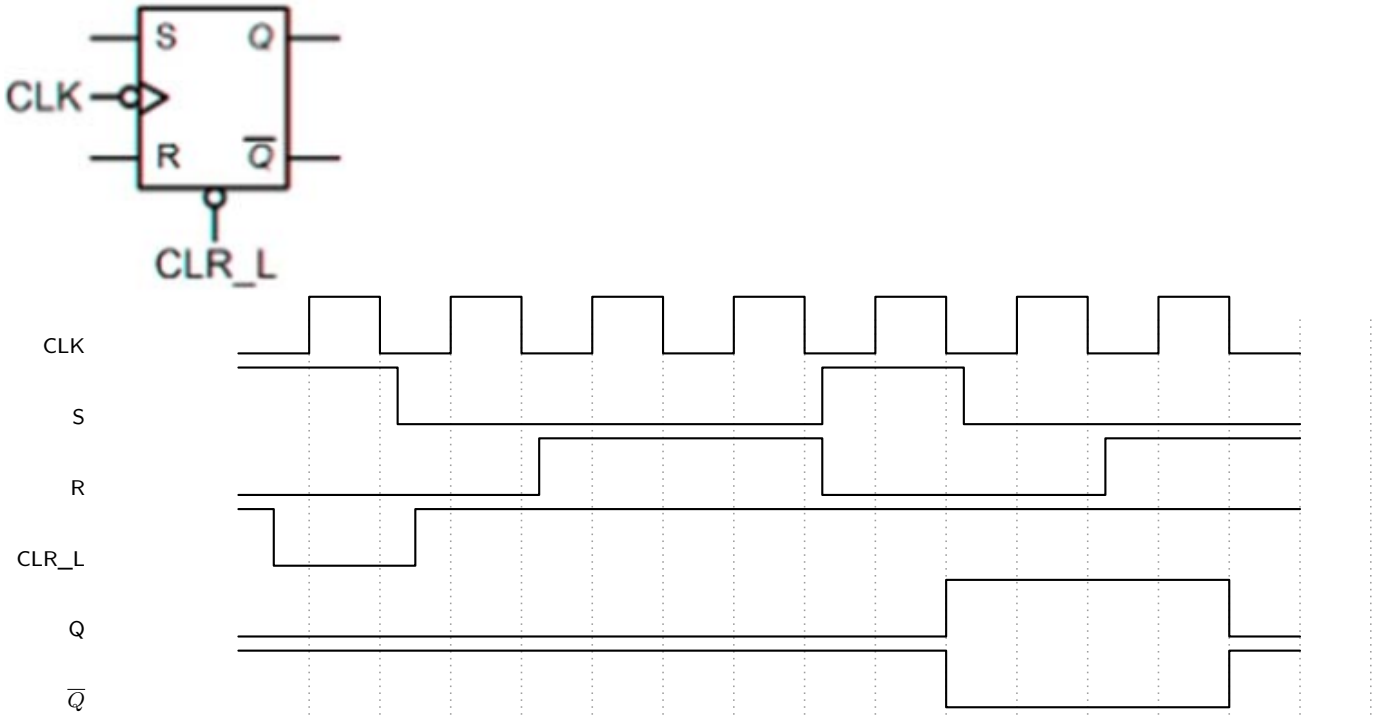
Note to the Grader Sorry I ran out of time, I wanted to actually do this HW but oh well.

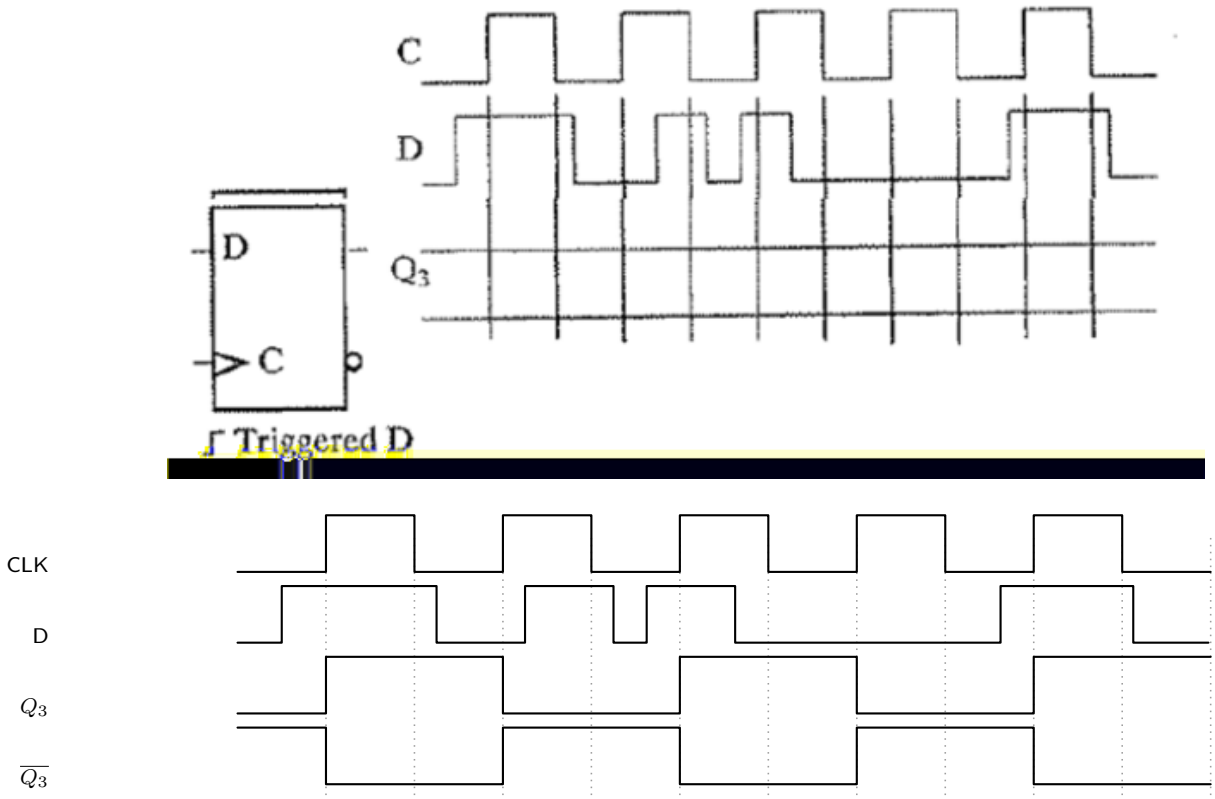
Question 1: (3 pts) Clock, and S, R waveforms are shown below for a negative edge triggered SR flip flop. Sketch the output Q, obtained in response to the input waveforms. Assume that the propagation delay is negligible. The initial state is 0.



Question 2: (3 pts) Clock, S, R and clear waveforms are shown below for a negative edge triggered SR flip flop. Sketch the output Q, obtained in response to the input waveforms. Assume that the propagation delay is negligible. The initial state is 0.



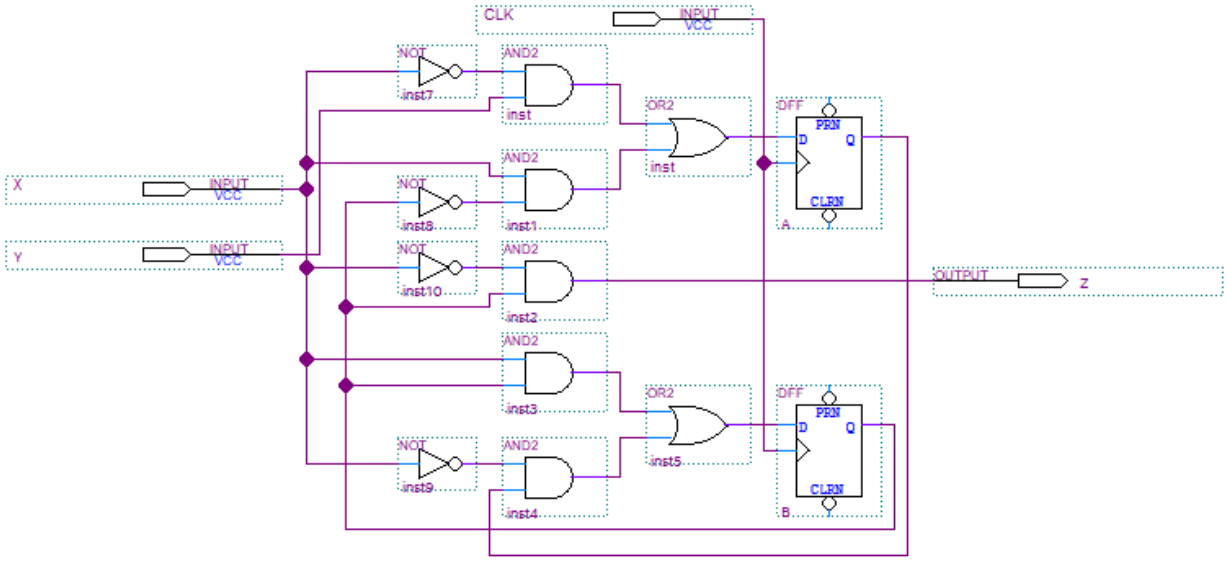
Question 3: (3 pts) Clock and D waveforms are shown below for a positive edge triggered D flip flop shown. Sketch the output Q3, obtained is response to the input waveforms. Assume that the propagation delay is negligible. The initial state is 0.



Question 4: (9 pts) A sequential circuit with two D flip flops A and B, two inputs X and Y, and one output Z is specified by the following input equations.

$$D_A = X'Y + XB'$$
$$D_B = XB + X'A$$
$$Z = X'B$$

a) Draw the logic diagram.

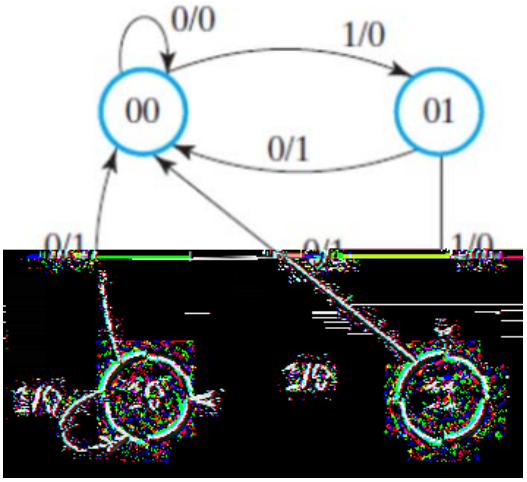


b) Derive the state table.

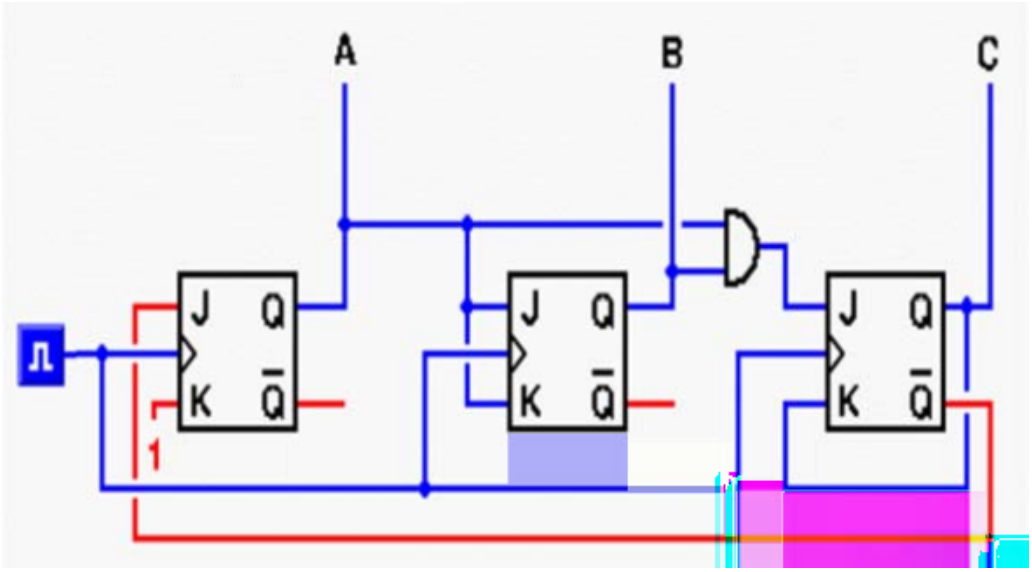
Current State		Input	Next State		Output
A	B	XY	A	B	Z
0	0	00	0	0	0
0	0	01	1	0	0
0	0	10	1	0	0
0	0	11	1	0	0
0	1	00	0	0	1
0	1	01	1	0	1
0	1	10	0	1	0
0	1	11	0	1	0
1	0	00	0	0	0
1	0	01	1	0	0
1	0	10	1	1	0
1	0	11	1	1	0
1	1	00	0	1	1
1	1	01	1	0	1
1	1	10	0	0	0
1	1	11	0	0	0

c) Derive the state diagram.

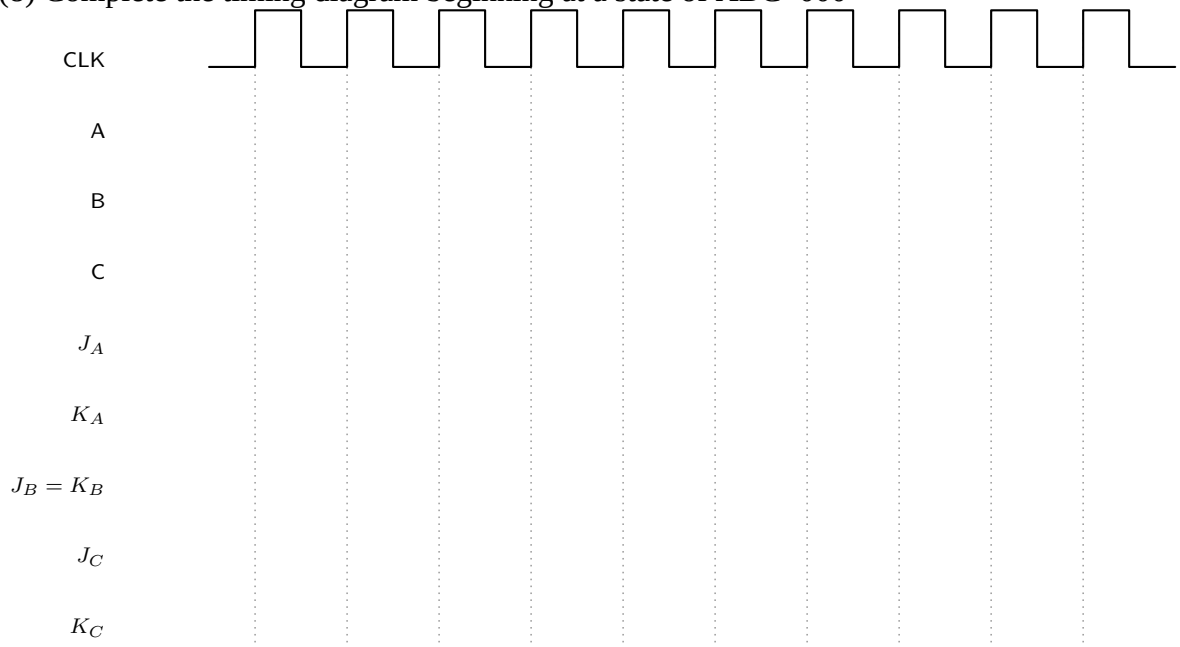
Question 5: (10 pts) Starting from state 10 in the state diagram below, determine the state transitions and output sequence that will be generated when an input sequence of 1011001111 is applied. (Note that the 1 in red text is the first input bit applied, the 1 in blue text in the last input bit applied.)



Question 6: Consider the following "divide-by-5" counter. (Don't worry about the label "divide-by-5"; just look at how the flip flops are connected.)



a) (8) Complete the timing diagram beginning at a state of ABC=000



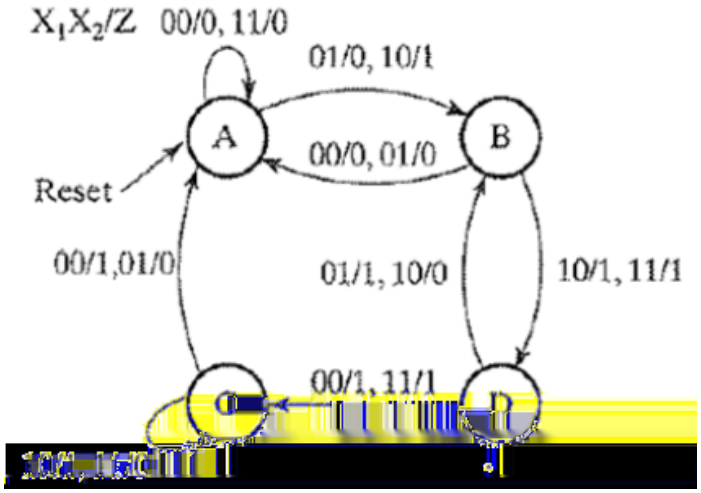
b) (3) Draw the state diagram

c) (1) If the input clock frequency is 10 kHz, what is the frequency of the C signal?

Question 7: (16 pts) Design a sequential circuit with two SR flip flops A and B and one input X. When X = 0, the state of the circuit remains the same. When X=1, the circuit goes through the state transitions from 00 to 10 to 11 to 01, back to 00 , then repeats.

a) Show your state diagram or state table, K-maps, FF input equations, and the logic diagram.
b) Repeat for JK flip flops

Question 8: The state diagram for a sequential circuit in shown below.



a) (4 pts) Find the state table
b) (1 pt) Make a state assignment
c) (3 pts) Find an optimized circuit implementation using D FFs, NAND gates, and inverters.

GRADING SCALE

Total: 64 pts

Pts	0	8	16	24	32	40	48	56
Letter Grade	D-	D	C-	C	B-	B	A-	A