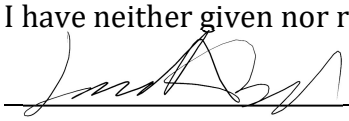
**ECE 3544: Digital Design I**
**Project 3 (Part A) – Design and Synthesis of a Magnitude Comparator System**

Student Name: Jacob Abel

Honor Code Pledge: I have neither given nor received unauthorized assistance on this assignment.



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**Grading: The design project will be graded on a 100 point basis, as shown below:**

*Manner of Presentation (30 points)*

_____ Completed cover sheet included with report (5 points)

_____ Organization: Clear, concise presentation of content; Use of appropriate, well-organized sections (15 points)

_____ Mechanics: Spelling and grammar (10 points)

*Technical Merit (70 points)*

_____ General discussion: *Did you describe the objectives in your own words? Did you discuss your conclusions and the lessons you learned from the assignment?* (5 points)

_____ Design discussion: *Did you discuss the approach you took to designing any original modules? Did you discuss the approach you took to assembling the top-level module?* (10 points)

_____ Testing discussion: *What was your approach to formulating your test benches? How did you verify the correctness of the modules you designed?* (5 points)

_____ Supporting figures: *Waveforms showing correct operation of the top-level module.* (10 points)

_____ Supporting files: *Do the modules pass any tests applied by the grading staff? Modules whose declarations do not conform to the requirements of the project specification cannot be tested, and will receive no credit.* (15 points)

_____ Validation of the final design on the DE1-SOC board (25 points): *Modules that exhibit the correct behavior but do not represent the correct implementation will receive no credit.*

_____ **Project Grade**

ECE 3544: Digital Design I
Project 3A Validation Sheet

Jacob Abel
Student's Name

GTA Validation Instructions:
Program the FPGA on the DE1-SoC Nano board with the student's implementation of the comparator system. When the programming has successfully completed, perform the set of tests described in the table below. For each case, indicate whether or not the student' design demonstrates the behavior described.

| Procedure and *Expected Result* | Correct Operation (**Yes** or **No**) |
|---|---|
| Set SW[7:4] = 0000, set SW[3:0] = 0000.<br>*HEX4 should display "0". HEX3 should display "0". HEX[2:0] should display "001".* | |
| Set SW[7:4] = 1011, set SW[3:0] = 0101.<br>*HEX4 should display "b". HEX3 should display "5". HEX[2:0] should display "100".* | |
| Set SW[7:4] = 0011, set SW[3:0] = 1000.<br>*HEX4 should display "3". HEX3 should display "8". HEX[2:0] should display "010".* | |
| Set SW[7:4] = 1111, set SW[3:0] = 1111.<br>*HEX4 should display "f". HEX3 should display "f". HEX[2:0] should display "001".* | |
| Set SW[7:4] = 1100, set SW[3:0] = 0110.<br>*HEX4 should display "c". HEX3 should display "6". HEX[2:0] should display "100".* | |
| Set SW[7:4] = 1110, set SW[3:0] = 1111.<br>*HEX4 should display "e". HEX3 should display "f". HEX[2:0] should display "010".* | |

GTA Printed Name and Signature: _____

Date and Time of Validation: _____

# Project 3A

ECE3544 CRN:82989

Jacob Abel

November 4, 2018

# Objective

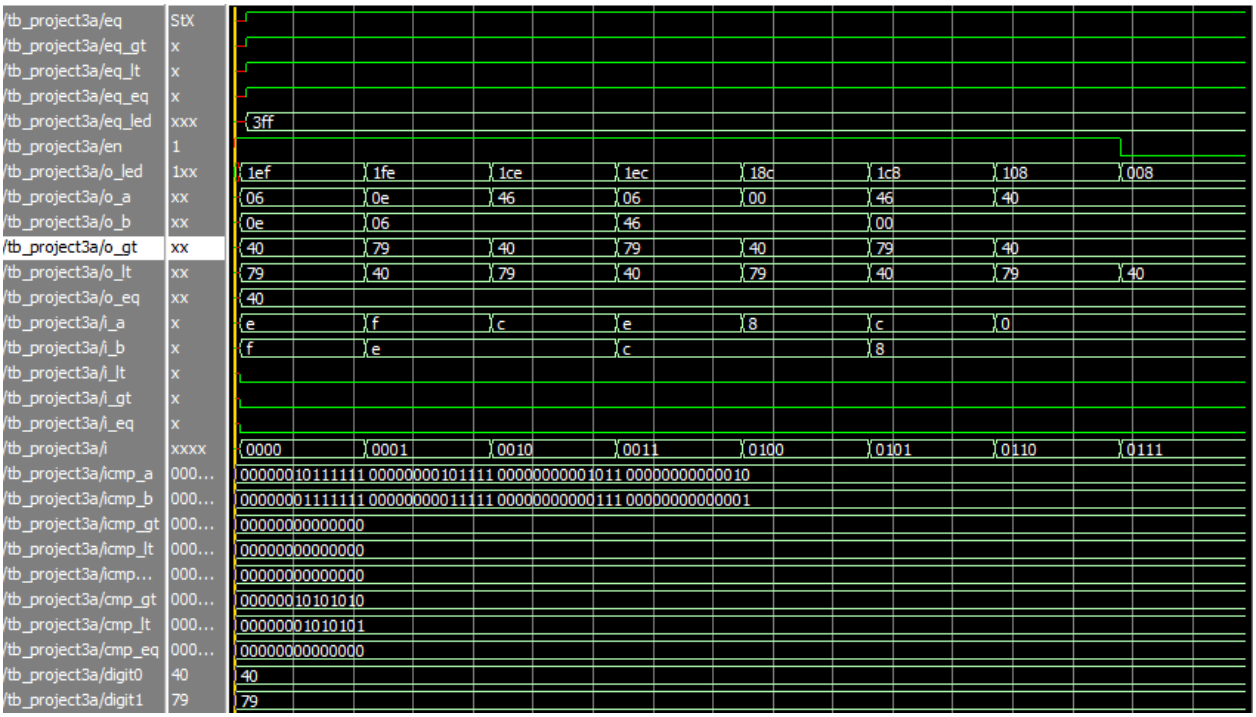
The objective of this project is to demonstrate a capability to synthesise designs onto a real world system such as an FPGA and produce the same output as the simulated designs. Additionally, this project demonstrates basic competence utilising the Quartus IDE.

# Module Design

The design process was rather straight forward. The pins were matched with the corresponding values using the manual. Once the board was functioning and designs were exportable, the module was implemented. As it was relatively straightforward, an enable bit was added to the hc85 module along with some self explanatory dataflow Verilog and the primary module was implemented using structural Verilog. The test bench was more or less a reimplementation of the hc85 test bench with some slight modifications. The 7-segment display driver module had previously been designed with a corresponding test bench. The entire module is essentially a large case block containing each possible display value and was a trivial design.

Once the primary module was implemented, the test bench was checked and the equivalence bit suggested that the design was functional. At this point the design was synthesised and the same tests as in the test bench were run on a DE1 board.

# ECE3544Project3a Module Simulation




This simulation demonstrates that all the basic inputs produce the correct outputs. The `en` and `i_` values are the inputs that compose the switch input values and the `o_` values are the outputs as 7 segment display values. The `eq_` wires demonstrate equivalence on each output pin and the `eq` wire demonstrates equivalence on all outputs. The equivalences are computed using an XNOR against expected results.

# Conclusion

This project demonstrated the equivalence of Verilog simulations and real world FPGA module synthesis. Despite starting this project late, the project went remarkably smoothly and very little of the time was spent debugging. As such the project can easily be considered a success with the exception of the scheduling failure that resulted in it being started late.