Date: 2020/6/23
Task Group: Fast Interrupts
Chair: Krste Asanovic
Co-Chair: Kevin Chen
Number of Attendees: ~10
Current issues on github:
https://github.com/riscv/riscv-fast-interrupt/blob/master/clic.adoc

Our new CTO Mark Himelstein attended our group meeting. He briefly introduced himself and offered his help on any issues we may have.

Issues discussed:

#84 asks about the upper limit of xtvt alignment

> There is no requirement for maximum alignment. It is implementation dependent and will not be specified. It is like xtvec. Any bits above minimum alignment can be WARL. SW can determine the actual alignment by writing all 1's then read them back.
>
> Programmers can define a parameter for '.align' in the header file. This parameter should be derivable from the configuration structure in the future.

> During the discussion, Mark suggested that we should consider recording the rationale and summary of discussions for github issues in the appendix of the spec. Some members liked the idea because it would be easier to search for topics, while other members thought discussions should stay in the github repository. Also, the appendix does not need to be reviewed as strict as the actual spec. This seems to be related to non-ISA (ecosystem) topic and spec later proposed by Mark.
>
> Mark also suggested that we should try to record software ABI and software related spec/definition (e.g., header). The TSC may discuss a universal place to record these. These seem to be related to the software overlay he proposed.

#88 xintstatus CSR numbers should be read-only

These CSRs are temporarily allocated in the read-write address range because we may have more read-write fields in the future. We may change this before we ratify the spec.

#51 Add xscratchcsw/xscratchcswl read and write pseudocode

We will discuss this further in our discussion group. This is because their behavior is somewhat not so intuitive.

#52 Clarify interrupt selection (enable signals for interrupts)

Yes, both clicintie[i] and mstatus.xie should be enabled. clicintie[i] is the individual control bit, while mstatus.xie is a global control bit for that particular mode (only valid in the corresponding mode).
This will be clarified in the spec later.