Date: 2020/7/21
Task Group: Fast Interrupts
Chair: Krste Asanovic
Co-Chair: Kevin Chen
Number of Attendees: ~10
Current issues on github:
https://github.com/riscv/riscv-fast-interrupt/blob/master/clic.adoc

Issues discussed:

We spent the entire meeting time extensively discussing the following issue:

#89 Proposal: reorder lower 16 interrupt IDs

Current proposal in the spec is to keep lower 16 interrupts compatible with the existing basic interrupt controller (as specified in CSR *mie* and *mip*):

```
15 12    11   10   9    8    7   6    5    4   3    2    1    0
  0      MEIP  0  SEIP  0   MTIP 0   STIP   0  MSIP  0  SSIP   0
```

- New proposal 1: anything goes (no default assignment)
- New proposal 2: define a minimum subset
  0 : timer
  1 : software
  2 : external (legacy)
  3-4095: external+

- Regarding software interrupt
  - For single-core, would like to have lowest priority being a software interrupt used for local context switching
  - But, for multi-core, also desire a higher-priority software interrupt (above context switch timer) used for inter-core signaling.

A fixed new ordering (proposal 2) is a subset of the "anything goes with a configuration description" model (proposal 1). For portable software, the fixed ordering is preferable. Proposal 1 supports backwards compatibility.

A packed ordering saves vector table memory size. Proposal 1 supports denser tables when not all interrupts are required, whereas proposal 2 mandates a few interrupts.

The legacy external can be folded into the other external (perhaps by convention always at the lowest number?)

Machine-mode should be able to see the lower-privilege mode interrupts with separate IDs, when not delegating the interrupts.
If there are no lower privilege modes, can pack as in proposal 2 above.

M-mode interrupt map (in M-only or M/U system without N extension)
0: M-mode software interrupt
1: M-mode timer interrupt
2+: external (including legacy)

External interrupts include inter-processor signaling interrupts. Dedicated software interrupt generally expected to be reserved for local software scheduler.

With more privilege modes, need to have lower-privilege mode interrupts visible at lower fixed priorities than M-mode interrupts when not delegated (as in original CLINT design, but not necessarily at same interrupt IDs), e.g.,

M-mode interrupt map (in M/S/U system without N extension)
0: S-mode software interrupt
1: S-mode timer interrupt
2: M-mode software interrupt
3: M-mode timer interrupt
4+: external (including legacy)

S-mode interrupt map (in M/S/U system)

0: Software interrupt
1: timer interrupt

This would be the recommended layout, but not clear if this should be mandated. Could be part of a profile for given set of RTOS to require this layout.