Date: 2020/6/9
Task Group: Fast Interrupts
Chair: Krste Asanovic
Co-Chair: Kevin Chen
Number of Attendees: ~10
Current issues on github:
https://github.com/riscv/riscv-fast-interrupt/blob/master/clic.adoc

Issues discussed:

#83 Clarify the behavior of writes to to xie/xip CSRs in CLIC mode

Writes to xie/xip will be ignored and will not trap (no access exceptions). xie/xip always appear to be zero in CLIC mode.

#(no number) Some member asked about the status of NMI proposal

Krste showed and briefly explained his multi-page draft proposal on NMI (Non-Maskable Interrupt) which also specify a new version of resumable NMI. This draft proposal has not been made public yet. This mini proposal will be ratified by itself and hopefully it can speed up the overall process.

#37 Allocate CSR address for minthresh

Assigned minthresh CSR to 0x*m*47, where *m* is the nibble encoding the privilege mode (M=0x3, S=0x1, U=0x0).

#42 Address of xintstatus CSR

Assigned xintstatus CSR to 0x*m*46, where *m* is the nibble encoding the privilege mode (M=0x3, S=0x1, U=0x0).

#(no number) Address of mclicbase

For now, mclicbase is temporarily kept as “0x3??.” This is because, in order to save one CSR, we would like to record this piece of information in the new global configuration structure in the future (assuming the Configuration Structure Task Group can finalize the structure before us).

#(no number) Reserved a range of memory address space for future use

F M-mode CLIC memory map:

Offset	
0x0008-0x07FF	reserved
0x0800-0x0FFF	custom

#36 Interrupt level of vector table read operation

Vector table read has the same level as interrupt handler.
For permissions-checking purposes, the memory access to retrieve the function pointer for
vectoring is treated as a load with the privilege mode and interrupt level of the interrupt handler.