Date: 2020/8/25
Task Group: Fast Interrupts
Chair: Krste Asanovic
Co-Chair: Kevin Chen
Number of Attendees: ~10
Current issues on github:
https://github.com/riscv/riscv-fast-interrupt/blob/master/clic.adoc

Regarding the recent discussion thread “PLIC and CLIC” from Bill:

> We discussed how CLIC can handle multiple inter-processor interrupts of different priorities with requirement for preemption and nesting. In this use case, PLIC is not appropriate because it only has one single wire per hart and does not have hardware support for preemption and nesting. Krste suggested that a better solution would be using Message Signalled Interrupts (MSI) to trigger multiple CLIC interrupt sources, and then let CLIC handle preemption and nesting. Nevertheless, we probably won’t have MSI feature available in the first ratification because we don’t have detailed proposal yet.

#92 Hypervisor compatibility

> There is discussion among hypervisor authors on using a subset of CLIC functionality as basis of virtualized interrupt capabilities, but I have not seen anything written down yet. The goal is not really to virtualize the CLIC per se, but to allow virtualization of device interrupts.

#94 CSR to indicate if in interrupt or not (originally a request from Ofer in the discussion group)

> The mintstatus CSR holds the current level, which if 0 indicates not in an interrupt. The mpil field of mcause holds the previous interrupt level.

#59 Legacy interrupts

> There is only hardware one timer interrupt in the original CLINT (from the memory-mapped mtimercmp circuit), the CLINT supervisor timer interrupt is generated by a machine-mode handler writing the stip bit. Similarly, in CLIC mode,

the machine-mode hardware timer handler can write a bit to indicate a supervisor timer interrupt, but now the effective "stip" bit is memory-mapped not in a CSR.

In CLIC mode, the software interrupts are all handled as memory-mapped IP bits (clicintip[]). Each can be routed to a supported privilege mode using clicintattr[].

Issue #89 proposes a standard mapping for the supervisor mode interrupts.

We'll close this issue and continue discussion on #89.

#89 Proposal: reorder lower 16 bits

This issue was raised in #59.
Might want to in addition specify a standard allocation for the PLIC external interrupts inputs, if they are present.

0: S-mode software interrupt
1: S-mode timer interrupt
2: S-mode external (PLIC) interrupt
3: M-mode software interrupt
4: M-mode timer interrupt
5: M-mode external (PLIC) interrupt
6: external

Not clear if this needs to be mandated, or just a recommendation.