CMPE 240 Midterm Exam (Version B)
S 2021
First Name:_____ Last Name:_____SID_____

Honor Code: All students agree, individually and collectively, that they will not give or receive unpermitted aid during examinations. Engaging in such unpermitted actions is considered cheating. By my signature, I affirm that I have adhered to the spirit of the Honor Code.

Signature:_____Date:_____

Please Read: *instructions for Zoon based online exam.*

1. this is an one hour exam, starting from 1:30 and last till 2:30;

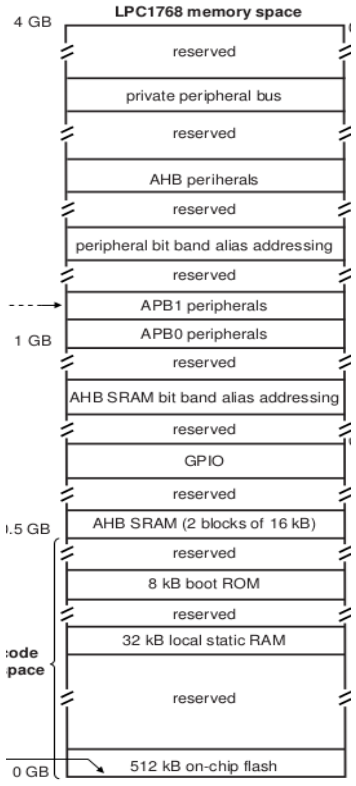
2. use cellphone to scan your papers, save them as pdf file, then you must convert it zip file;

3. Submit the zip file on line before 2:45, late submission will make the paper disqualified; After 2:45 no submission will be accepted (based on the time stamp of the submission). Thank you and stay safe.

This test has total 30 points. Please provide a step-by-step calculation.

1. (10 points) Based on the 32 RISC CPU architecture, answer the following design questions, the data sheet is given in the Appendix.

1.1 (4 pts) Given SSP1's CR0 register, find the memory bank which holds the SSP1 peripheral controller? Find the starting address of this memory bank?



1.2 (6 pts) In SPI Color LCD interface design, to display live video with 160x120 resolution, 30 FPS (frames per second), 24 bit color per pixel, (1) find the SPI clock rate based on the design in the class and in your lab? (2) find binary pattern to perform CR0 init and config to realize the design requirements (assume PCLK=50 Mhz, and CPSDVSR is minimum), (3) modify the following program code if needed to realize this requirements.

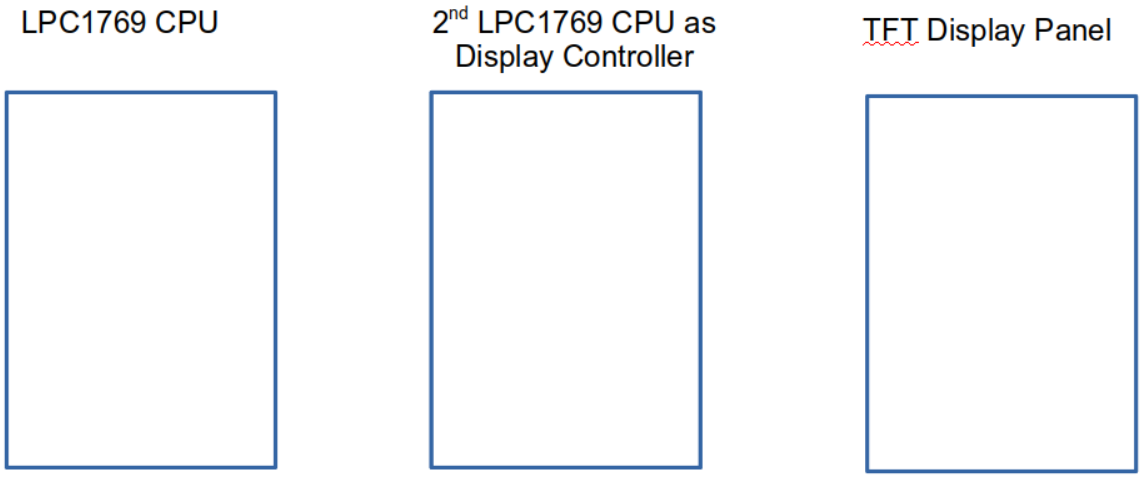
```
void initSSP1(void){
   //power up spi1
   LPC_SC->PCONP |= (1<<10);
   //01 PCLK_peripheral = CCLK.. 01, since it's CCLK/1
   LPC_SC->PCLKSEL0 &= ~(3<<20);
   LPC_SC->PCLKSEL0 |= (1<<20);

   //P0.6 is used as a GPIO output and acts as a Slave select
   LPC_GPIO0->FIODIR |= (1<<6);
   LPC_GPIO0->FIOSET = (1<<6);
   //P0.7:9 init
   LPC_PINCON->PINSEL0 &= ~((3<<18)|(3<<16)|(3<<14));
   LPC_PINCON->PINSEL0 |= ((2<<18)|(2<<16)|(2<<14));
   //data size set to 8 bits
   LPC_SSP1->CR0 = 0x07
.....
```

2. (10 points), In design of 2D GE (Graphics Engine), suppose a TFT color display panel is given, design display controller, e.g., display drive, by using one additional LPC1769 to realize SPI interface with CPU and to control LCD display (see Figure below).

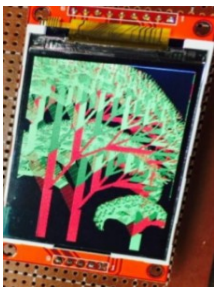
2.1 (2 pts) Design a display controller by drawing the schematics using the following blocks to realize CPU SPI interface to the display controller?

2.2 (3 pts) Continued from the above, draw schematics for the controller to control the TFT color display panel? (Reference design is based on the project in class, and it is given at the Appendix of this paper)

2.3 (5 pts) Assume the TFT display panel has 320-by-240 resolution, 24 bpp (bit per pixel), 30 FPS (frames per second), find the time needed to plot a green pixel at (201,137) location? Hint: use Sync_F, Sync_H, Sync_D in your calculation.



3. (10 pts) In graphics engine (GE) design, answer the following questions:
(1) (5 pts) Given P1=(0,-5), P2=(0,5), lamda = 0.8, based on 2D vector equation P(x,y) = P_1(x,y) + lamda * (P_2(x,y) – P_1(x,y)), and rotation matrix, generate tree patterns in the figure below by finding next level P'2 left, e.g., 30 degree counter clockwise rotation branch with respect to P2.
(2) (5 pts) Now, find the (x,y) value of the above result on the physical display whose origin (0,0) is set at the top left corner of the display device with its x-axis from left to right as positive, and y-aixs top down as positive. (assuming the display device resolution is 160x120).



Appendix A. Datasheet Reference

Table 371: SSPn Control Register 0 (SSP0CR0 - address 0x4008 8000, SSP1CR0 - 0x4003 0000) bit description

Bit	Symbol	Value	Description	Reset Value
3:0	DSS		Data Size Select. This field controls the number of bits transferred in each frame. Values 0000-0010 are not supported and should not be used.	0000
		0011	4-bit transfer	
		0100	5-bit transfer	
		0101	6-bit transfer	
		0110	7-bit transfer	
		0111	8-bit transfer	
		1000	9-bit transfer	
		1001	10-bit transfer	
		1010	11-bit transfer	
		1011	12-bit transfer	
		1100	13-bit transfer	
		1101	14-bit transfer	
		1110	15-bit transfer	
		1111	16-bit transfer	
5:4	FRF		Frame Format.	00
		00	SPI	
		01	TI	
		10	Microwire	
		11	This combination is not supported and should not be used.	
6	CPOL		Clock Out Polarity. This bit is only used in SPI mode.	0
		0	SSP controller maintains the bus clock low between frames.	
		1	SSP controller maintains the bus clock high between frames.	
7	CPHA		Clock Out Phase. This bit is only used in SPI mode.	0
		0	SSP controller captures serial data on the first clock transition of the frame, that is, the transition **away from** the inter-frame state of the clock line.	
		1	SSP controller captures serial data on the second clock transition of the frame, that is, the transition **back to** the inter-frame state of the clock line.	
15:8	SCR		Serial Clock Rate. The number of prescaler-output clocks per bit on the bus, minus one. Given that CPSDVSR is the prescale divider, and the APB clock PCLK clocks the prescaler, the bit frequency is PCLK / (CPSDVSR × [SCR+1]).	0x00
31:8	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Appendix B. Pin Reference for the display controller design.

Color LCD pins
LITE
SCK
MOSI
TFT_CS
D/C
RESET
Vcc
Gnd