

# Circuit Capture of Chisel

## Part 2. Naming

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# Problems involved

- Correctness
- Naming
- Debug info

# What is circuit capture?

```
1 import chisel3._
2
3 class DecCounter extends Module {
4   val io = IO(new Bundle{
5     val value = Output(UInt(4.W))
6   })
7
8   val counter = RegInit(0.U(4.W))
9
10  io.value := counter
11
12  when (counter === 9.U) {
13    counter := 0.U
14  } otherwise {
15    counter := counter + 1.U
16  }
17 }
```

```
circuit DecCounter :
  module DecCounter :
    input clock : Clock
    input reset : UInt<1>
    output io : { value : UInt<4>}

    reg counter : UInt<4>, clock with :
      reset => (reset, UInt<4>("h0")) @[main.scala 8:24]
    io.value <= counter @[main.scala 10:12]
    node _T = eq(counter, UInt<4>("h9")) @[main.scala 12:17]
    when _T : @[main.scala 12:26]
      counter <= UInt<1>("h0") @[main.scala 13:13]
    else :
      node _T_1 = add(counter, UInt<1>("h1")) @[main.scala 15:24]
      node _T_2 = tail(_T_1, 1) @[main.scala 15:24]
      counter <= _T_2 @[main.scala 15:13]
```

# Naming

```
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3 class DecCounter extends Module {
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17 }
```

```
4 (new ChiselStage).execute(
5   Array(
6     "-X", "verilog",
7   ),
8   Seq(ChiselGeneratorAnnotation(() => new DecCounter))
9 )
```

```
411 def build[T <: RawModule](f: => T): (Circuit, T) = {
...   ...
414   val mod = f
...   ...
421 }                                     src\main\scala\chisel3\internal\Builder.scala @ 4a0e828

30 def do_apply[T <: BaseModule](bc: => T)
31   (...)
32   : T = {
...   ...
67   val component = module.generateComponent()
...   ...
76 }                                     src\main\scala\chisel3\Module.scala @ 4a0e828

61 private[chisel3] override def generateComponent(): Component = {
...   ...
65   val names = namelds(classOf[RawModule])
...   ...
124 }                                     src\main\scala\chisel3\RawModule.scala @ 4a0e828

301 protected def namelds(rootClass: Class[_]): HashMap[HasId, String] = {
...   ...
318   for (m <- getPublicFields(rootClass)) {
319     Builder.nameRecursively(cleanName(m.getName), m.invoke(this), name)
320   }
...   ...
323 }                                     src\main\scala\chisel3\Module.scala @ 4a0e828
```

# Thanks!

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