





对照 RISCV32IM ,学习 C-SKY V2 指令集

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C-Sky V2 指令集体系结构概述



- 参考文档来源:
 - https://github.com/c-sky/csky-doc
- C-SKY V2 寄存器位宽 32bit , 地址位宽 32bit , 用户态可见寄存 c 下:
 - 32 个 32 位 GPR 寄存器
 - 1个32位PC
 - condition bit /carry bit (c bit):1 bit (条件执行)
 - 32bit encoding vs 16 bit encoding , 16bit 不是 32bit 的子集(与 RISCV 的 C 扩展不

RISCV32 IM 指令集简述



算术运算	addi slti sltiu andi ori xori 【 I-type, imm12 】
(RV32I)	slli srli srai 【 I-type , imm5 】
算术运算	add sub slt sltu and or xor sll srl sra
(RV32I R-type)	
乘除取余数	mul mulh mulhsu mulhu
(RV32M R-	div divu
type)	rem remu
跳转	Jal(J)
(RV32I)	Jalr (JR)
分支	beq bne blt bltu bge bgeu: 直接比较 rs1 和 rs2 的值,跳转
(RV32I)	
load/store 指令	LB LBU LH LHU LW
(RV32I)	SB SH SW
	(only one addressing mode , imm12)
addr gen (RV32I)	lui auipc 【 U-type , imm20 】
Fence	fence fence.i
(RV32I)	
Environment Call	ecall ebreak
and Breakpoints (RV32I)	
CSR	csrrw csrrs csrrc csrrwi csrrsi csrrci
(Zicsr extension)	

用户态 C-SKY V2 与 RISCV32 IM 之间的比较与学习





参考文档: 20200217-CSKYV2-RISCV32IM-qiuji.xlsx

	inst function	csky 32bit	encoding reference	csky 16bit	encoding reference	rv32 im counterpa	
data operation-1	add/sub	addu	4.3.3.1	addu	5.3.3.1/5.3.3.2-3	add	
		addc	4.3.3.1	addc	5.3.3.2-3		
		addi	4.3.2.4	addi	5.3.2.1/5.3.2.6	addi	
		subu	4.3.3.1	subu	5.3.3.1//5.3.3.2-3	sub	
		subc	4.3.3.1	subc	5.3.3.2-3		
		subi	4.3.2.4	subi	5.3.2.1/5.3.2.6		
		rsub	pseudo of subu rz,ry,rx	addi(sp)	5.3.2.5/5.3.2.6		
		ixh	4.3.3.1	subi(sp)	5.3.2.5/5.3.2.6		
		ixw	4.3.3.1				
		incf	4.3.3.2-2				
		inct	4.3.3.2-2				
		decf	4.3.3.2-2				
		dect	4.3.3.2-2				

用户态 CSky V2 与 RISCV32 IM 之间的比较与学习





5.3.3.2. Addressing Mode of Two Register

The instructions that adopt the addressing mode of two register can be further divided into three formats.

In the first format, the two register fields RX and RY are the first source register field and second source register field respectively; SOP field is the sub-operation code field. Instructions of this format include cmphs16,cmplt16,cmpne16,tst16.



In the second format, RZ field is the destination register field; RX is the source register; SOP field is the sub-operation code field. Instructions of this format include mov16, zextb16, zextb16, sextb16, sextb16, revb16 and revb16.



In the third format, RZ field is the destination register field and second source

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File Name: CSKY Architecture user guide

No:

register field; RX field is the first source register field; SOP field is the sub-operation code field. Instructions of this format include addu16, addc16, subu16, subc16, and16 andn16, or16, xor16, nor16, ls116, lsr16, asr16, rotl16 and mult16.

151413	10	9 6	5	2 1 0		
0 1	OP	RZ	RX	SOP	5.3.3.2-3	
2	1	Δ	1	2		

V32IM-qiuji.xlsx.xlsx

ce	csky 16bit	encoding reference	rv32 im counterpart
	addu	5.3.3.1/5.3.3.2-3	add
	addc	5.3.3.2-2	
	addi	5.3.2.1 5.3.2.6	addi
	subu	5.3.3.//5.3.3.2-3	sub
	subc	5.3.7.2-3	
	subi	5.3 2.1/5.3.2.6	
ry,rx	addi(sp)	5/3.2.5/5.3.2.6	
	subi(sp)	3 .3.2.5/5.3.2.6	







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