

1

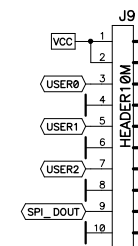
2

3

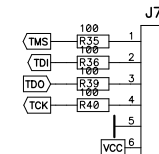
4

Changes from REV 1.0:
* SPI_DOUT is now connected to pin 19 of the FPGA
* PS/2 connectors shielding is now connected to frame ground
* R49 is now 100 Ohm
* no more wire patches needed!

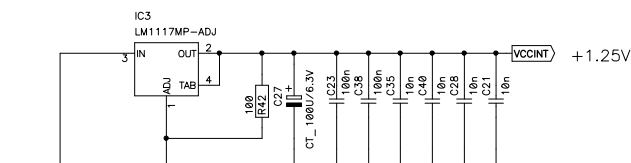
Spare I/O



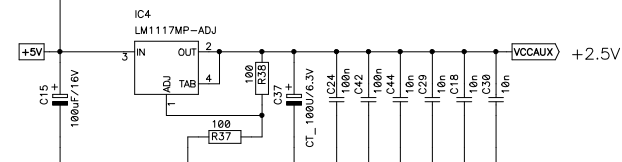
JTAG



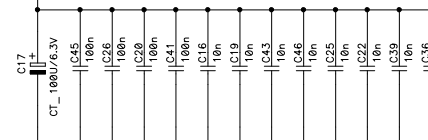
FPGA core voltage decoupling



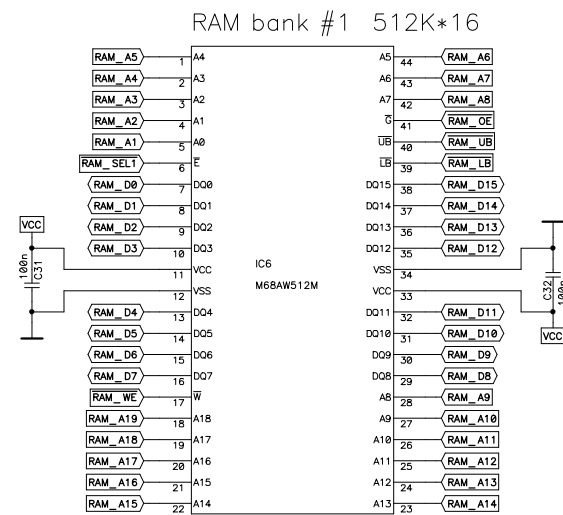
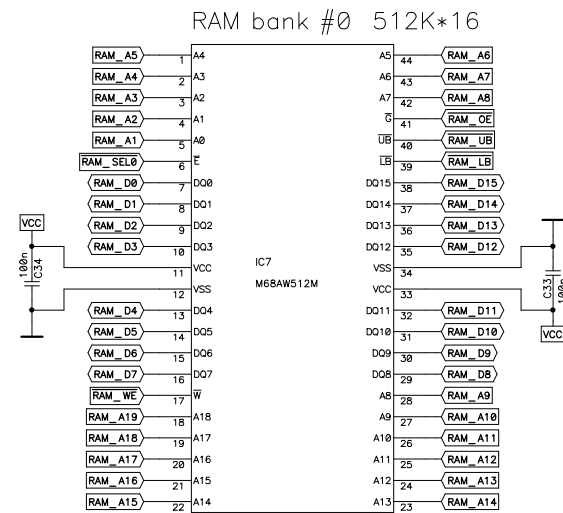
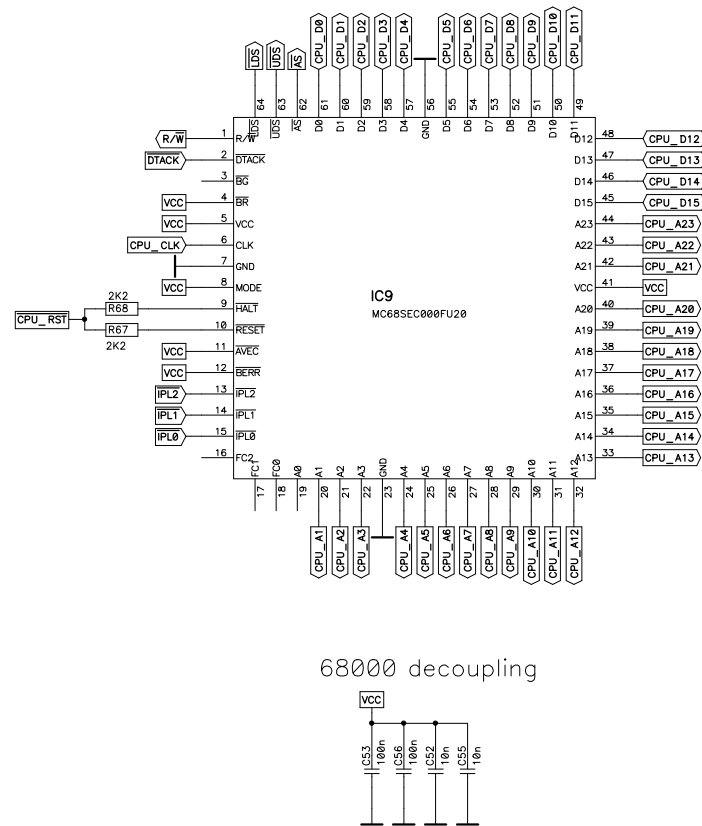
FPGA auxiliary voltage decoupling



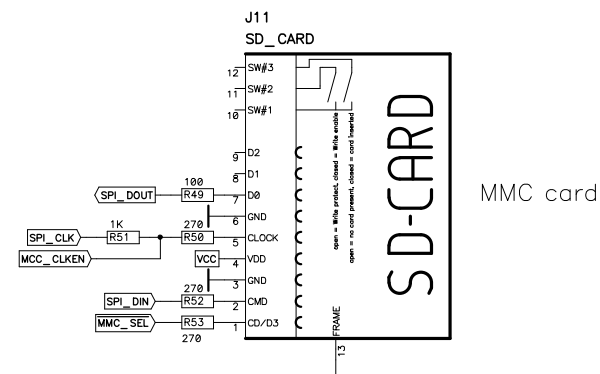
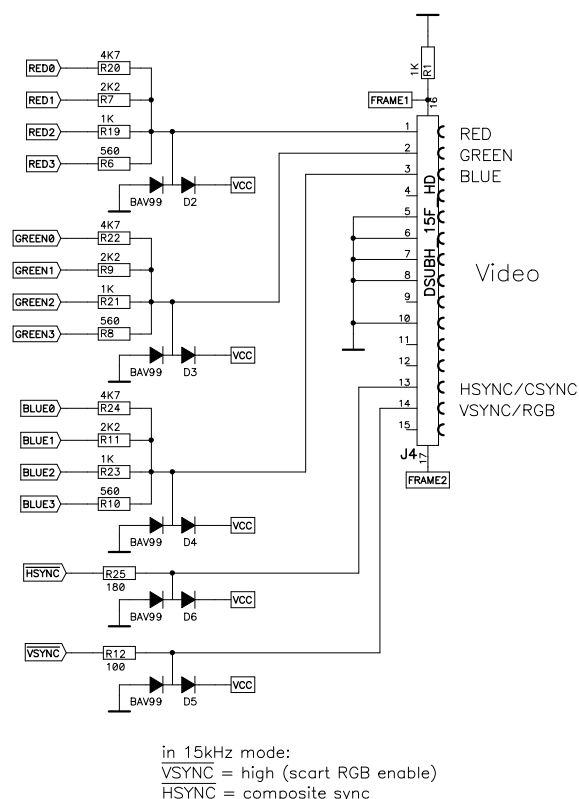
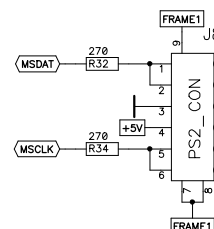
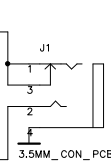
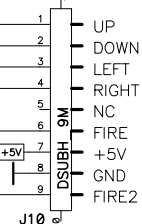
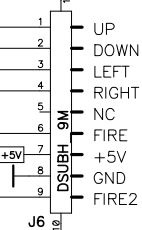
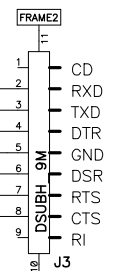
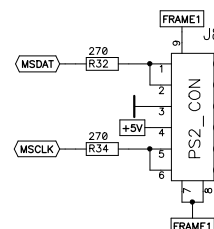
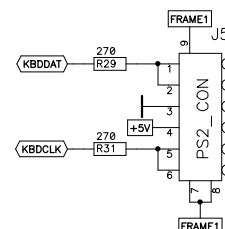
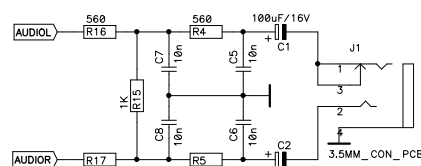
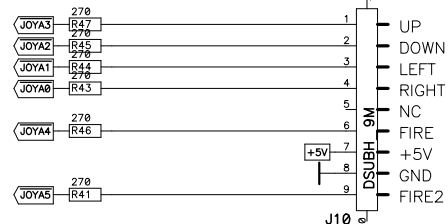
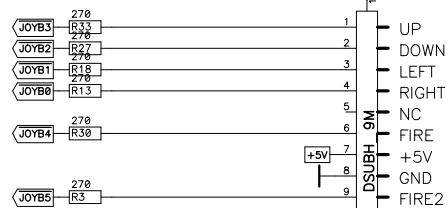
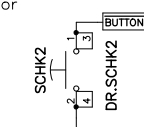
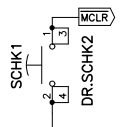
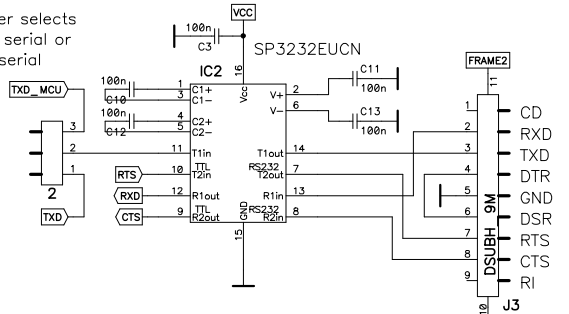
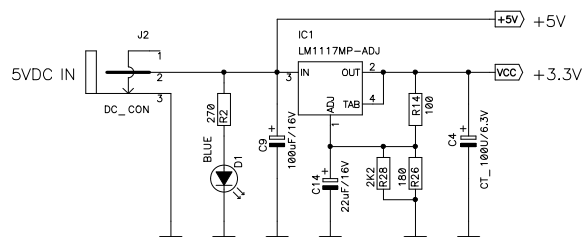
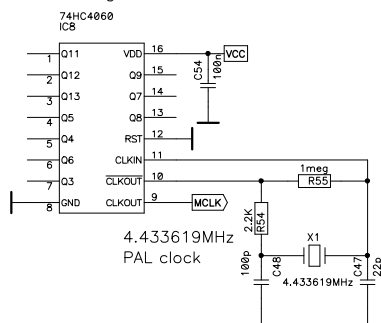
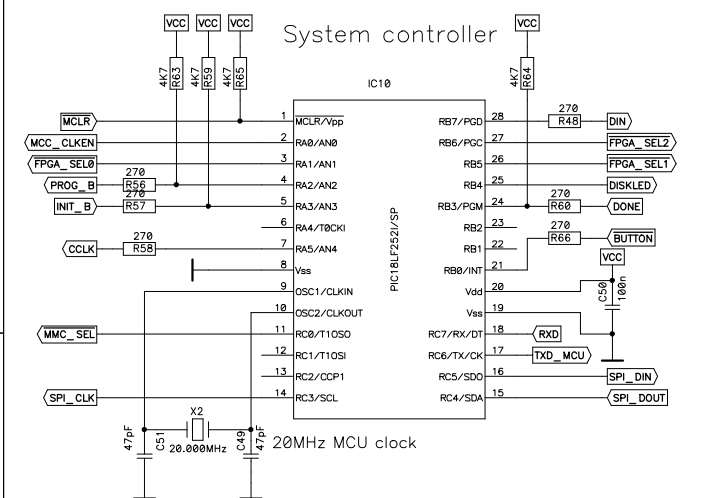
FPGA I/O voltage decoupling



Title MINIMIG REV 1.1		
Size A2	Number SPARTAN POWER	Rev 2
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Title		
MINIMIG REV 1.1		
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A2	68000 FOREVER & RAM	2
Date	03-10-2007	
Drawn by	Dennis van Weeren	
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Title			MINIMIG REV 1.1		
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A2		I/O GALORE			2
Date			03-10-2007		
Drawn by			Dennis van Weeren		
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