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Contract: FA8650-18-C-1141

CDRL: 0001AH Status Report No. 8

March 15, 2020

Dear Mr. Dooley,

In accordance with requirements off the referenced contract, Global Circuit Innovations, Inc. (GCI) is pleased to submit the enclosed Final Draft Report.

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Sincerely,



Diana Gault





INTEGRATED CIRCUIT (IC) DIE EXTRACTION AND REASSEMBLY

Final Report Draft

18 July 2019 – 18 October 2019

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Under Contract: FA8650-18-C-1141
CDRL No.: 0001
CLIN: Draft of Final

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LIST OF SYMBOLS, ABBREVIATIONS, ACRONYMS

ACRONYM	DESCRIPTION
AFB	Air Force Base
Ag	Silver
Au	Gold
BA	Barely Alive
C	Carbon
CLK	System Clock
CPGA	Ceramic Pin Grid Array
Cu	Copper
CQFP	Ceramic Quad Lead Flatpack
DEER TM	Die Extraction ENEPIG Reassembly
DER TM	Die Extraction and Re-assembly
DIP	Dual in-line package
DOE	Design of Experiments
ENEPIG	Electroless Nickel Electroless Palladium Immersion Gold
FET	Field Effect Transistor
FPGA	Field-Programmable Gate Array
FR4	Board Material Revision-4
G	Good
G-Force	Gravitational Force
GCI	Global Circuit Innovations, Inc.
GND	System Ground
HD	Heavily Degraded

IC	Integrated Circuit
IDD	Current Drain-Drain (Supply Current)
IEEE	Institute of Electrical and Electronics Engineers
IIH	Current Input High
IIL	Current Input Low
I/O	Input/Output
IR	Infrared
IVA	Internal Vapor Analysis
KGD	Known Good Die
KHZ	Kilo-Hertz
mA	milli-Ampere
MCM	Multi-chip module
MIL-STD	Military Standard
MOSFET	Metal Oxide Surface Field Effect Transistor
NCO	Kyocera Material Version
Ni	Nickel
NTK	Ceramic Package Supplier
O	Oxygen
OCM	Original Component Manufacturer
OPAMP	Operational Amplifier
Pd	Palladium
PEM	Plastic Encapsulated Microcircuit
PGA	Pin Grid Array
PPM	Parts Per Million
PQFP	Plastic Quad Lead Flat Pack
RIE	Reactive Ion Etch
RIF	Rapid Innovation Fund
SOIC	Small Outline Integrated Circuit
SPDT	Single Pole Double Throw
TI	Texas Instruments
TM	Test Method
TO	Transistor Outline
TGFP	Thin-Quad-Flat-Pack
uA	micro-Ampere
um	micrometer

V	Volt
VDD	Voltage Drain-Drain (Supply Voltage)
VIH	Voltage Input High
VIL	Voltage Input Low
VOH	Voltage Output High
VOL	Voltage Output Low
VSS	Voltage Supply-Supply
W	Watt
X	Failing

REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-0188	
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1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE		3. DATES COVERED (From - To)		
9/27/19	Status Report		4/16/19 - 7/15/19		
4. TITLE AND SUBTITLE			<p>Integrated Circuit (IC) Die Extraction and Reassembly Status Report</p> <p>5a. CONTRACT NUMBER FA8650-18-C-1141</p> <p>5b. GRANT NUMBER</p> <p>5c. PROGRAM ELEMENT NUMBER 0001</p> <p>5d. PROJECT NUMBER 001Ag</p> <p>5e. TASK NUMBER 001</p> <p>5f. WORK UNIT NUMBER</p>		
6. AUTHOR(S)			<p>Erick Spory</p>		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)			<p>Global Circuit Innovations, Inc. 4182 Center Park Drive Colorado Ssprings, CO 80916</p>		
8. PERFORMING ORGANIZATION REPORT NUMBER					
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)			<p>USAF/AFMC AFRL Wright Research Site 2130 Eighth Street, Building 45 Wright-Patterson AFB OH 45433-7541</p>		
10. SPONSOR/MONITOR'S ACRONYM(S)			<p>11. SPONSOR/MONITOR'S REPORT NUMBER(S)</p>		
12. DISTRIBUTION/AVAILABILITY STATEMENT					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT Program Status Report #7					
15. SUBJECT TERMS					
16. SECURITY CLASSIFICATION OF:		17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	<p>19a. NAME OF RESPONSIBLE PERSON Erick Spory</p> <p>19b. TELEPHONE NUMBER (Include area code) 719-573-6777</p>	
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1. SUMMARY

The main goal of this research was to compare and understand the reliability of integrated circuit product manufactured with GCI's *DEER™* (Die Extraction and Re-Assembly with Gold Ball Remnant removal and Aluminum Die Pad Electroless Nickel, Electroless Palladium, and Immersion Gold Plating) process as compared to the original component manufacturer, OCM, comparable integrated circuits (ICs). This final report will focus on equivalent MIL-STD 883K test data associated with the *DEER™* process for five independent integrated circuit devices (ICs) chosen. In essence, the testing performed was chosen to not only mirror the equivalent MIL-STD 883 testing, but also to subject the devices to dynamic, biased life-test conditions at 125°C at or above maximum operating load conditions, in addition to unbiased 250°C connectivity reliability exposure. All of the testing performed not only highlighted the known high-temperature reliability benefits of *DEER™* processing regarding the mitigation of inter-metallic diffusion (Kirkendall voiding), but also noting any potential adverse effects or benefits from the *DEER™* processing relative to MIL-STD 883K testing.

All Group A testing within Table I of Appendix I is included in the 125°C Dynamic biased Burn-In and Life testing implemented in this study was explicitly designed to examine functional shifts on the inputs (IIL and IIH testing), as well as any possible loading shifts on the outputs (VIL, VIH, VOL, and VOH testing) during actual functional signal toggling while the devices are under bias, nominal frequency switching, and maximum output loading. Schematic loading configurations for each of the five devices analyzed within Table I of this report are included within Appendices II – VI, respectively. The remainder of the MIL-STD-883K tests listed in Appendix I (Groups B, C, and D) were followed precisely with exception to package testing of the leads, corrosion resistance, etc., which was inherent to the robust and proven nature of the NTK and Kyocera ceramic/gold packages chosen. All tests performed within this study relative to MIL-STD-883K testing, as well as the accelerated electrical stress testing produced results showing superior performance in all categories for the *DEER™* ceramic equivalent devices when compared to their original plastic controls.

The five devices which were chosen are as follows:

- 1.) Low pin count (8 pins) originally gold wire bonded device: ADG859
- 2.) Large pin count (144 pins) originally gold wire bonded device: XC4005XL
- 3.) High-Temperature and Low-Temperature variant for head to head *DEER™* comparison (gold bond wire): OPA820
- 4.) Large pin count (64 pins) originally copper wire bonded device: ATSAMD21
- 5.) High-Power FET gold bond wire: STN1NK60Z

Each of the donor packaged devices was of a plastic variety as listed within Table 1 below. The new ceramic package is also listed accordingly. Typically, more than 99% of available die for extraction are within plastic packages, such that targeting donors within ceramic packages was not included within this study.

Table 1. Device Summary for 5 Devices Chosen to be Included in this Phase II

Part Type	Donor Package	Target Package
NC7SB3157P6 (ADG859)	SC70-6/SOT-66	8-Lead Ceramic Sidebrazed
XC4005XL	144-TQFP	144-Ceramic Pin Grid Array (PGA)
OPA820	8-SOIC	8-Lead Ceramic Sidebrazed
ATSAMD21	64-TQFP	64 or 144-Ceramic Pin Grid Array (PGA)
STN1NK60Z	SOT-223	8-Lead Ceramic Sidebrazed

Quarterly Technical Interchange meetings were performed with GCI, Steve Dooley, Jeff Sillart, and David Johnson to discuss everything from high-level goals to advise on device selection criteria, target device loading specifications, and technology process design of experiments (DOE) to ensure maximum value for the Phase II study. Target operating conditions and device loading, which produced stress conditions beyond the data sheet specifications, were taken into consideration to highlight any differences in reliability or performance between the donor plastic controls and their *DEER™* ceramic equivalents.

Steven Dooley requested specific surface analysis testing on *DEER™* extracted die to examine purity of GCI's extraction process and potential presence of ionic contaminants or residue. This study was performed by Honeywell, is included within Appendix VII, and most importantly does not indicate the presence of any surface ionic contaminant or heavy metal.

David Johnson requested if it was possible to find a historical USAF/DLA ceramic device to compare GCI's *DEER™* process for a commercial to ceramic conversion across the strenuous testing for MIL-STD 883 testing and beyond. Any 74 to 54 series Texas Instruments (TI) logic device conversion would have accomplished this task, but this exact study was already demonstrated and proven in GCI government Rapid Innovation RIF Study: FA8615-17-C-6053. Specifically, the TI devices chosen in the RIF study were ceramic part type conversions of PEM 74LS26, 74LS175, and 74LS32 devices which were extracted, processed with GCI's *DEER™* technology, and ultimately tested to meet all of the ceramic MIL-STD 883 equivalents for 54LS26, 54LS175, and 54LS32 devices, respectively.

In order to meet David Johnson's goal regarding high-stress environmental head to head exposure, GCI suggested a study using a commercially available, high-temperature (210°C) designated device which is available in die form only vs. its much more economical, and lower-temperature (125°C) version as an available plastic encapsulated microcircuit (PEM). This project is listed above as the TI OPA820 operational amplifier product line 8 pin device for which the high-temperature die sold at a \$300 premium to its \$5 packaged counterpart. The very interesting result is that the GCI *DEER™* processed plastic PEM equaled the high-temperature die performance with respect to MIL-STD 883 test exposure and beyond.

At the recommendation of the entire Quarterly Technical Interchange team, an additional study was performed to better understand plating variability for GCI's ENEPIG process. Results of the study concluded that although the plating process for each step within the ENEPIG process was well documented with respect to temperature and plating time, occasional surface oxide layers on the aluminum die pad surface were responsible for inconsistent plating, with the remedy being exposure of the extracted devices to argon reactive ion etching to remove any oxide prior to pad plating.

Lastly, low-temperature epoxy hermetic lid seal experiment updates were addressed to explore the possibility of integrating an organic FR4 substrate board into the cavity to accommodate additional components such as level shifters or voltage regulators for potential newer, lower core voltage generation FPGA devices. The goal of this experiment is to produce a hermetically sealed product that generates sufficiently low organic and moisture outgassing, while also meeting all shock and vibrational for all MIL-STD 883 requirements. All epoxies explored were unable to meet the maximum 5000 ppm moisture test.

2. INTRODUCTION (& BACKGROUND)

In the Phase I, Global Circuit Innovations, Inc. (GCI) researched the feasibility and value of a die extraction process which included remnant gold ball removal followed by Electroless Nickel, Electroless Palladium, and Immersion Gold (ENEPIG) plated die pad films to enhance the reliability of commercial integrated circuits (ICs) that were removed from their original plastic package and reassembled/repackaged into a ceramic package, while eliminating compound bonding. This work was the result of initial, random evaluation units extracted and exposed to the *DEER™* process with overall success. The objective of the Phase II was to further validate those initial findings by demonstrating manufacturability through process repeatability studies and with more comprehensive focus on the reliability by subjecting the parts to a MIL-STD 883 qualification sequence. GCI already established that Die Extraction/Reassembly (*DER™*) of commercial integrated circuits in ceramic packages increases the reliability of those devices within the high-temperature (200°C to 250°C) oil/gas drilling environments with respect to the integrated circuit interconnection process, namely gold bond wire bonding to the die surface.

GCI's *DER™* process enables the safe, reliable removal of a die from one package such that it can be used in another package or multi-chip module (MCM) – see Figure 1 below. The combination of *DER™* with resurfaced/reconditioned die pads results is a new process referred to as *DEER™* (Die Extraction, ENEPIG plating Reassembly) and eliminates undesired compound bonding for the reassembled products, thereby allowing the prospect for military qualified product solutions for otherwise obsolete IC components. GCI originally developed the *DEER™* process because although integrated circuits can frequently operate above their maximum rated temperature of 125°C, they are not packaged appropriately to reliably endure higher temperature exposure.

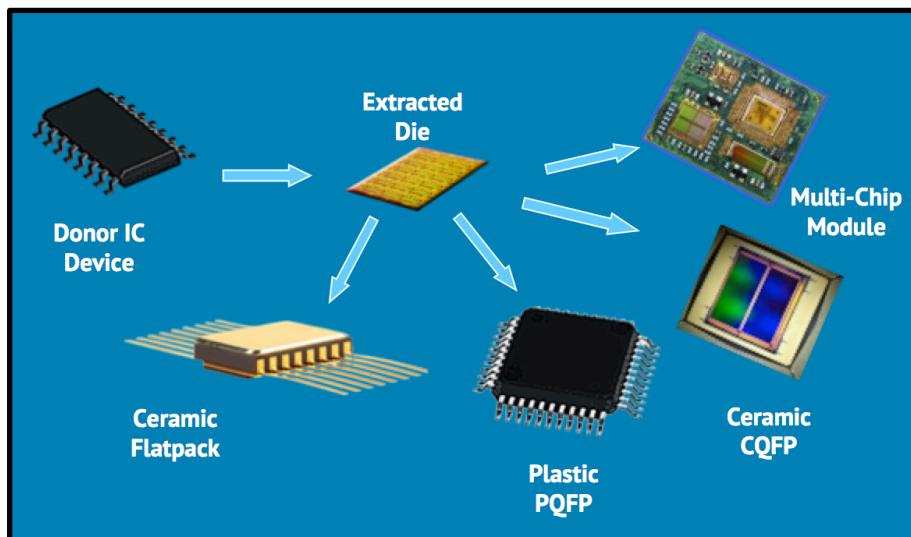


Figure 1. GCI's *DER™* Process Illustration

Specifically, the plastic packaging can rapidly degrade at temperatures greater than 125°C and generally does not perform reliably with exposure to high pressure and high humidity environments. However, subsequent ceramic packaging of these same die can produce robust and reliable performance relative to shock and vibration environments due to hermetic solutions and superior bonding procedures. The foremost reason that plastic packaging is not able to maintain its integrity at higher temperatures is that the original gold or copper bonds on the aluminum die pads are prone to Kirkendall or Horsting voiding, particularly at temperatures greater than 150°C and as high as 250°C. In some cases, commercial demand for higher temperature performance and packaging can justify

support of a ceramic line from the original component manufacturer (OCM). In most cases, the demand is insufficient.

Thus, ceramic packaging generally provides a higher reliability semiconductor solution relative to PEM (plastic encapsulated microcircuits) for the same die. Although the demand for ceramic-packaged semiconductor product has increased over the recent past due to higher temperature down-hole drilling applications and military program obsolescence requirements, it has not been sufficiently large for OCM's (original component manufacturers) to support the excessive cost in maintaining or developing the relatively low-volume ceramic product line demand as compared to the more lucrative high-volume commercial PEM flows. The *DER*TM and *DEER*TM processes also provide the added value of working with and producing singulated, known-good die (KGD) as well as added visual inspection capability for counterfeit mitigation.

Specifically, the Phase II study focused on understanding the impact of ENEPIG pad reconditioning process on the reliability of commercial integrated circuits extracted from their standard plastic packages and rebuilt into ceramic packages. Originally, only four different types of IC projects were proposed: 1) low pin count die with gold (Au) bond wire, 2) high pin count die with Au bond wire, 3) low to medium pin count die with copper (Cu) wire, and 4) *DEER*TM processing for a eutectic or solder die attached IC. Later, a fifth project was added: 5) a head-to-head comparison of a *DEER*TM processed commercially available plastic package die vs. its high-temperature version offered by the original component manufacturer. This last device selection will be used to compare the *DEER*TM processing of the commercial temperature plastic control units to the hermetic assembly of the original high-temperature die purchased directly from a franchised source.

An overall schedule of Phase II goals and milestone target completion dates is listed below in Table 2.

Table 2. Originally Suggested Kickoff Schedule for Reference through 24 Months

Task	Description	Month																							
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	Kickoff Meeting																								
2	Requisition Materials																								
3	Die Preparation																								
4	ENEPiG Plating																								
5	Die Reassembly																								
6	Build Test PCBs																								
7	Reliability Testing																								
8	Final Tests																								
9	Data Analysis																								
10	Technical Interchange Meetings																								
11	Interim Report																								
12	Final Report																								

The *DEER*TM process that will be used in this work begins by extracting the die from their commercial plastic package using processes that are controlled and well established by GCI. The resulting extracted die still have the gold balls from the original wire bond operation attached to the pads. GCI's proprietary *DEER*TM process is then used to remove the excess gold from the pad in a way that does

not damage the underlying aluminum pad structures. Some remnant material can remain on the aluminum pad surface after gold ball removal, but the Phase I work GCI conducted indicated that these remnants do not interfere with subsequent pad reconditioning. The composition of this remnant material shall be analyzed as part of this proposed work. In addition, the relative percent of the remnant material vs. the total pad areas will be calculated to see if there is any relation between the amount of remnant alloy material vs. subsequent failures.

The final result of the *DEER™* process produces single bonds on freshly re-plated pads, all similar to the bonding results seen within Figures 2 and 3 below.

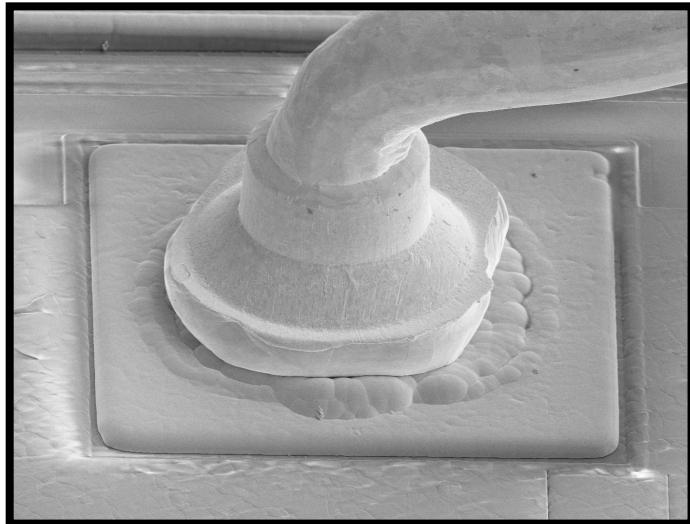


Figure 2. Gold Ball Bond on ENEPIG Die Pad Originally Bonded with Gold Wire

A very thorough presentation of GCI's *DER™* and *DEER™* technology can be found in Appendix VII with GCI's 2018 IEEE publication within the Surface Mount Technology Association's Electronics in Harsh Environments titled Increasing High-Temperature Reliability of Plastic ICs Using Die Extraction, Gold Ball Removal, and ENEPIG Die Pad Plating (*DEER™*)

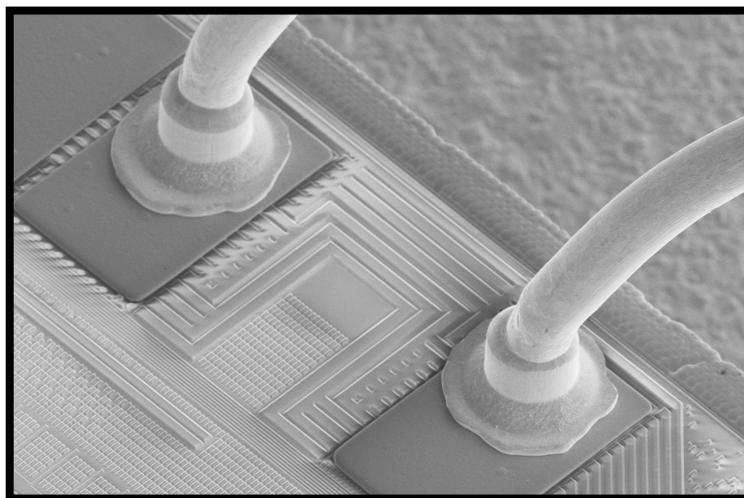


Figure 3. Gold Ball Bond on ENEPIG Die Pad Originally Bonded with Copper Wire

3. METHODS, ASSUMPTIONS, AND PROCEDURES

Overall goals associated with Methods, Assumptions, and Procedures:

- 1.) The design of experiments (DOE) for the epoxy lid seal have been listed and performed, with the data presented in the Results section. Although several lid seal epoxies can generate intra-cavity moisture levels near 5000 ppm, none were able to meet this stringent specification.
 - a. This project was organized due to the possibility of necessarily integrating an organic FR4 substrate board into the cavity to accommodate additional components such as level shifters or voltage regulators for potential newer, lower core voltage generation FPGA devices.
 - b. The goal of this experiment is to produce a hermetically sealed product that generates sufficiently low organic and moisture outgassing, while also meeting all shock and vibrational for all MIL-STD 883 requirements.
 - c. Some of the questions which will be addressed are as follows:
 - i. How does the cavity fill epoxy (target is for lowest C_{TE} (coefficient of thermal expansion) affect organic or moisture outgassing MIL-STD requirements? Does the reduction in cavity volume affect the requirement? Group D qualification testing which is defined in MIL-STD-883 TM 5010 (Test Requirements for Monolithic Circuits) requires Internal Water Vapor measurements made per TM 1018 (Internal Gas Analysis). The requirements are 5000 PPM water maximum with 0 fails allowed in a sample size of 3 units, or 1 fail is allowed in a sample size of 5 units.
 - ii. Can today's best epoxies meet the requirements of lid adhesion? If so, what is the minimum area of adhesion vs. area of lid (overall weight) requirement to do so?
 - iii. Mechanical testing of the best hermetic epoxy solutions (and fill solutions) needs to be performed relative to MIL-STD 883 testing
 - iv. Updates for hermetic requirements of the various epoxies chosen can be found in the Results and Discussion section.
 - d. The following (Table 3) describes the water vapor test method to be followed: C.7.5.4.9 Internal water vapor. An internal water vapor content sample of three devices (zero failures) or five devices (one failure) will be selected from the subgroup 1 sample. The use of electrical rejects, or representative mechanical samples, is permissible provided these samples have seen, as a minimum, the environmental exposures required in subgroup 1 (e.g., temperature cycle or thermal shock, mechanical shock or constant acceleration, and seal tests as applicable). The internal water vapor content shall not exceed 5,000 ppm. If the sample size (accept number) of 5 (1) is used and the sample contains one (1) failure, then the manufacturer shall perform an engineering evaluation of the failure. The evaluation, as an example, may include data to support materials used, element evaluation of materials, cure process time and temperature, bake-out process, seal chamber environment, seal process, adequacy of hermetic testing process, trend analysis, historical data review, or the consideration of other gases.

Table 3. Group D Testing Relative to Cavity Moisture Requirements

Subgroup	Class		Test	MIL-STD-883		Quantity/accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	Internal water vapor content 5000 PPM maximum water content at +100°C	1018		3 devices (0 failures) or 5 devices (1 failure)	
2	X	X	Moisture resistance	1004		5 (0)	
3	X	X	Salt atmosphere	1009		5 (0)	

METHOD 5010.4
18 June 2004

15

- 2.) The DOE for the ENEPIG plating focused mainly on palladium thickness variations to optimize subsequent gold and aluminum wire bonding on the plated pads. Plating optimization processing has now been targeted and documented with a controlled process, and although an official design of experiments (DOE) was not fully addressed, experimentations with chemistries and plating times have been addressed to optimize plating for all products within this study. The contamination study addressed was performed and highlighted remnant die pad oxide as the most significant variable contributing to poor subsequent plating.

A description of the current thickness targets based on optimized experimental results for consistent plating and bonding is as follows: 3 um – 4 um Nickel (Ni), 0.2 – 0.5 um Palladium (Pd), and 0.05 – 0.1 um Gold (Au). The study on original die pad aluminum purity and/or presence of contaminants as a variable for successful subsequent ENEPIG plating can be found in Appendix VIII, although the predominant factor influencing consistent ENEPIG plating on the original aluminum die pad surface is the presence of residual aluminum oxide. This oxide can, in the vast majority of cases, be removed with plasma reactive ion etching (RIE) using argon as a sputtering material to dislodge the surface oxide molecules. Sufficient reactive ion etching (RIE) to remove remnant oxide is a process now available when necessary, which has improved plating yields substantially.

- 3.) The Auger surface contamination study performed by Honeywell can be found in Appendix IX of this report and only revealed silver (Ag), oxygen (O), and carbon (C) as additional elements to what was expected on and around the aluminum pads following GCI's DER™ extraction processing. The silver (Ag) represents low-level remnant material from the silver die attach process and does not present a yield or reliability risk. The oxygen (O) and carbon (C) are typical of any inert organic particulate/residue from the original package or trace amounts of solvent used to rinse the die following extraction.
- 4.) The methods, assumptions, and procedures for each of the *DEER™* projects will be identical in that a proper extraction and ENEPIG die pad process flow will be initially engineered, followed by review of a reliable re-assembly process. The five device types chosen are as follows:

- a.) Low pin count (8 pins) originally gold wire bonded device: ADG859
- b.) Large pin count (144 pins) originally gold wire bonded device: XC4005XL
- c.) High-Temperature and Low-Temperature variant for head to head *DEER*TM comparison (gold bond wire): OPA820
- d.) Large pin count (64 pins) originally copper wire bonded device: ATSAMD21
- e.) High-Power FET, original eutectic die attach, gold bond wire: STN1NK60Z

Complete datasheets detailing the device specifications and performance can be found in the various quarterly reports as well as the following links:

ADG859:

<https://www.analog.com/media/en/technical-documentation/data-sheets/ADG852.pdf>

XC4005XL:

<https://www.digchip.com/datasheets/parts/datasheet/534/XC4005XL-pdf.php>

OPA820:

<http://www.ti.com/lit/ds/sbos303d/sbos303d.pdf>

ATSAMD21:

https://cdn.sparkfun.com/datasheets/Dev/Arduino/Boards/Atmel-42181-SAM-D21_Datasheet.pdf

STN1NK60Z:

<https://www.st.com/resource/en/datasheet/stn1nk60z.pdf>

Initial screening of all commercial plastic donor devices for each ceramic solution listed above was performed to ensure functional performance of the die across the -55°C to 125° military range. Additionally, all material used within this study (i.e., selected IC die and target ceramic packages) was purchased from franchised distributors representing the respective original component manufacturers (OCMs) to avoid any possibility of using counterfeit material.

Bond wire loop height optimization to avoid wire to lid shorting during MIL-STD centrifuge testing was performed for each product. After the respective processes were confirmed to produce acceptable yields with functional end product, the projects progressed into pre-production, or qualification processing. Approximately 180 - 200 devices of each type were manufactured for reliability testing and qualification processing, to meet the requirement for 116+ be available for full Groups A, B, C, and D MIL-STD 883 testing.

- 5.) Reliability testing was targeted to mirror Group A, B, C, and D MIL-STD 883 testing requirements, but given the unique increased stressing required in this study, the Burn-In/Life-Test and Life-Test stressing (Groups A & C) was exclusively be performed at GCI. The high-stress conditions continue to follow the recommendation for input and approval from David Johnson to assist in the verification that proper voltage, speed, and load testing of the devices is acceptable and meets his expectations and requirements. The high-stress dynamic, biased configurations that were agreed to within a technical interchange meeting and were used for the *DEER*TM Dynamic Biased Burn-In/Life-Test and Life-Test experiments.

Groups B and D testing involving package integrity, lead integrity, and lid seal as exposed to various moisture and corrosive environments, all of which are independent of the *DEER*TM process were less of a priority as compared to centrifuge, bond pull, bond shear, die shear, and vibration testing, due their reliance strictly on the integrity of the ceramic package, which has been

performed repeatedly within prior GCI device qualifications, as well as qualifications within the industry for these package types.

Burn-In/Life-Test board schematic configuration were designed to achieve the maximized recommended wattage for all 5 device types addressed in this research study (ADG859, OPA820, STN1NK60Z, XC4005XL, and ATSAMD21). All 125°C Dynamic Biased Burn-In/Life-Test Burn-In/Life-Test and Life-Test board configurations (ADG859, OPA820, STN1NK60Z, XC4005XL, and ATSAMD21) were targeted to operate and stress the devices over 4000+ hours. Appendices II – VI outline the schematic and board layout designs to meet the following device loading criteria.

- a. The ADG859 datasheet indicates a maximum load of 300 mA, which justifies the 18 ohms of output series resistance designed within the Burn-In Board (see Table 4 below). Switching speed for this mux for ‘low’ to ‘high’ transitions was chosen to be 100 kHz for a total dissipation per part of approximately 1.5W. Given that most of the ceramic packages indicate a thermal resistance in the range of 0.5 – 1 °C/W vs. the plastic equivalents, which is approximately 10x – 50x higher (i.e., 5° - 50°C/W), 1.5W could generate as much as a 75°C increase in junction temperature for the plastic equivalents vs. the ceramic counterparts under the specified loading conditions (see formula and illustration for thermal resistance below in Figure 4). The predominant reason for the increased junction temperature is the decrease in thermal conductivity, K, for the plastic vs. ceramic package (i.e., ~0.2 W/cm*K of Ceramic vs. ~0.02/0.005 W/cm*K for Molding Plastic). Targeted 125°C Burn-In/Life-Test exposure is 5000+ hours.

Table 4. ADG859 Maximum Load Rating

ABSOLUTE MAXIMUM RATINGS	
$T_A = 25^\circ\text{C}$, unless otherwise noted.	
Table 3.	
Parameter	Rating
V_{DD} to GND	-0.3 V to +7.0 V
Analog Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, S or D	
5 V Operation	500 mA
3 V Operation	460 mA
Continuous Current, S or D	
5 V Operation	300 mA
3 V Operation	275 mA
Operating Temperature Range	
Automotive	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
SOT-66 Package (4-Layer Board)	
θ_{JA} Thermal Impedance	191°C/W
Lead-Free Reflow	
Peak Temperature	260 (+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

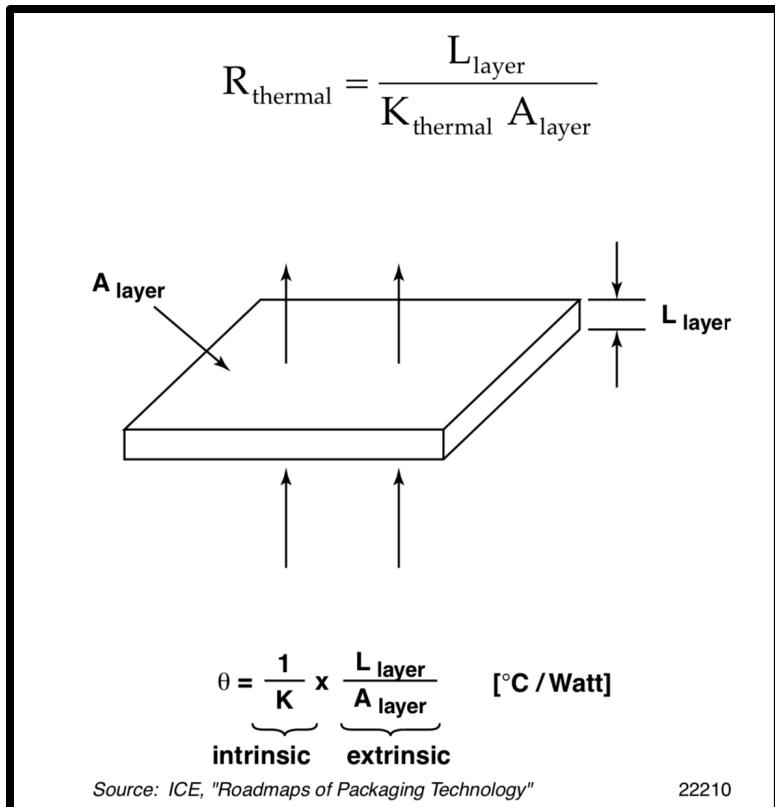


Figure 4. Calculation of Ambient to Junction Temperature rise for Thermal Conductivity Variation.

- b. As in the original Kick-Off meeting, an additional task relative to the potential true benefits of GCI's *DEERTM* process was suggested by Steve Dooley relating to the performance of a head-to-head reliability comparison study between an original already-qualified MIL-STD 883 device and its low-temperature commercial plastic equivalent exposed to *DEERTM* processing (i.e., ENEPIG die pad plating followed by re-packaging into a ceramic package). This device chosen for this study is the OPA820 Operational Amplifier, a product for which there is a high-temperature (210°C) option that can be purchased for a direct head-to-head comparison over time at temperature. Head-to-head testing of the OPA820 "high-temperature" Texas Instruments (TI) die version vs. the *DEERTM* harvested and processed plastic equivalent die re-packaged into a ceramic package targeted for testing at 125°C Dynamic Biased Burn-In/Life-Testing for 5000+ hours.

The high-temperature OPA820 datasheet version indicates a maximum load of +/-110 mA, which justifies the 50 ohms of output series resistance designed within the Burn-In Board (see Table 5 below). Total device wattage dissipated is approximately 0.5W, with a switching frequency of 1 kHz, ultimately leading to an increase in operating junction temperature of the original plastic device of between 1°C and 25°C relative to the ceramic equivalent.

Table 5. OPA820 Maximum Load Rating

FEATURES	
• High Bandwidth (240 MHz at 25°C and 100 MHz at 210°C, G = 2)	
• High Output Current (±110 mA at 25°C and 50 mA at 210°C)	
• Low Input Noise (2.5 nV/√Hz at 25°C and 4.5 nV/√Hz at 210°C)	
• Low Supply Current (5.6 mA at 25°C and 6.8 mA at 210°C)	
• Flexible Supply Voltage:	
– Dual ±2.5 V to ±5 V	
– Single +5 V	
APPLICATIONS	
• Downhole Drilling	
• Extreme Temperature Application	

- c. The STN1NK60Z datasheet indicates a maximum load of 300 mA (see Table 6 below), which justifies the 3 ohms of output series resistance in designed within the Burn-In Board to be in series with the 15 ohms of channel resistance, R_{DS} . Total device wattage dissipated is approximately 1.5W, with a switching frequency of 100 kHz, ultimately leading to an increase in operating junction temperature of the original plastic device of between 5°C and 75°C relative to the ceramic equivalent.

Table 6. STN1NK60Z Maximum Load Ratings

Features				
Order codes	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STN1NK60Z	600 V	15 Ω	0.3 A	3.3 W
STQ1NK60ZR-AP				3 W
• 100% avalanche tested				
• Extremely high dv/dt capability				
• Gate charge minimized				
• ESD improved capability				
• Zener-protected				

- d. The XC4005XL Burn-In/Life-Test board design was originally designed to produce an effective clock-tree within the FPGA, with at least 4 output nodes (one per side) to monitor functionality of the clock, while also providing an option of loading the outputs to maximum current. However, the serial scan chain option was chosen instead which enables two inputs and two outputs for toggling (see XC4005XL Burn-In/Life-Test board schematic within Appendix III). The corresponding 125°C maximum loading of these signals is a 100 ohm resistor in order to maintain logic levels for continued cycling. Total

wattage dissipation per part was calculated to be approximately 0.12W/output, or approximately 0.5W/device.

- e. The ATSAMD21 dynamic Burn-In/Life-Test board schematic and layout is represented within Appendix V. This device type also utilized 100 ohm resistors for maximum I/O loading. These loads present empirical maximum loading to maintain continuous logic toggling for the XC4005XL and testing loads for the ATSAMD21 for target I/O load output currents proposed at approximately 30 – 35 mA (100 ohm load resistors to both VDD and VSS). Total wattage dissipation per part was calculated to be approximately 0.12W/output, or approximately 0.5W/device.

Updated Burn-In/Life-Test and functionality data will be included in the Results/Discussion section. The GCI Burn-In/Life-Test oven which is capable of dynamic biased testing conditions at 125°C for reliability stressing of the 5 device types with functional biased Burn-In/Life-Test condition can be seen within Figures 5 and 6. Also present within these photos is required number and type of power supplies and signal generators to supply required voltage/power and dynamic stimulation to support the respective Burn-In/Life-Test requirements for each of the device types, keeping in mind target sockets, resistor loads, clock speeds, and VDD/power level requirements.



Figure 5. GCI Dynamic Biased Burn-In/Life-Test @ 125°C (all Boards Installed)



Figure 6. GCI Dynamic Biased Burn-In/Life-Test @ 125°C (Close-Up of all Boards)

Case temperatures under maximum loading conditions for each of the Burn-In/Life-Test boards were measured with a hand-held infrared temperature gun as seen below in Figure 7. Most device types measured between a 5°C and 25°C delta increase from ambient.

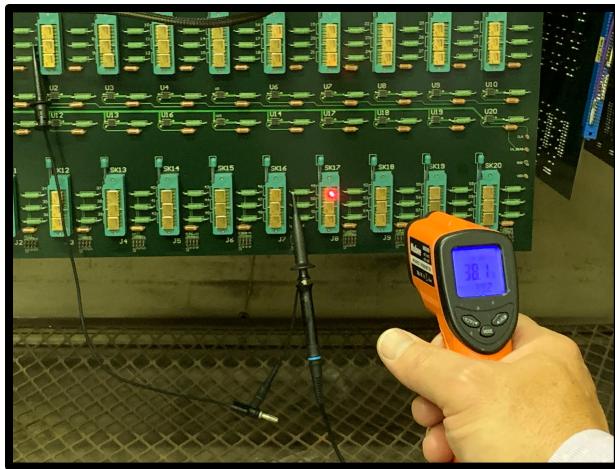


Figure 7. Method of Measuring Temperature Rise of Packages from Ambient

- 6.) GCI commercial *DEER*TM lot qualification testing for high-temperature oil and gas drilling customers requiring performance and reliability to 200°C and beyond has been a process requirement for many years. Therefore, this same standard 250°C unbiased bake testing for 72 hours was initiated to confirm the prospect for superior connectivity reliability of the *DEER*TM process within ceramic packaging relative to franchised (authorized supply chain) plastic donor control product. However, the 250°C unbiased connectivity bake for all five product types researched within this study was carried out to 1000's of hours to highlight any variance between GCI ceramic *DEER*TM processing and the donor commercial plastic controls.

This high-reliability connectivity test was designed to forward bias the P-type to N-type junction for every input/output (I/O) pin to substrate (ground) with 10 uA. The voltage required to force 10 uA typically varies between 0.5V and 1.2V, depending on the I/O schematic configuration.

Empirical data has demonstrated that even a 0.010V shift (10 mV) in this voltage over time is sufficient to generate a high resistance to produce analog failures at temperature. In most cases, the failure mechanism responsible for shifts greater than 10 mV is related to Kirkendall or Horsting voiding, involving intermetallic diffusion of the original aluminum die pad and the overlying gold wire bond to the pad. This intermetallic diffusion develops a highly resistive alloy at the gold/aluminum interface, which can also contribute to a brittle bond with poor adhesion. Degradation in bond pull strength is typically seen along with increases in connectivity resistance when intermetallic diffusion is present. GCI's *DEER*TM processing virtually eliminates the potential for this to occur with temperature exposure up to 250°C.

- 7.) Bond Pull data on each of the 5 device types will be included following Dynamic Burn-In/Life-Test testing at 125°C and consistent with test methods from MIL-STD 883.
- 8.) Hermetic and IVA data will be included for each of the device types following 125°C Dynamic Biased Burn-In/Life-Test. Test limits will be identical to the MIL-STD-883 with testing requirements of less than 5000 ppm of moisture in the cavity. Testing will be performed on a sample of devices which experienced 5000+ hours of 125°C Biased Dynamic testing.

4. RESULTS AND DISCUSSION

The results within this report will be updated according to the identical line items listed within the Methods, Assumptions, and Procedures section just above.

- 1.) Low-temperature epoxy hermetic lid seal experiment updates:
 - a. Tables 7 and 8 list the results and summary to date of the epoxy lid seal experiments.
 - b. Although the FP4651, Loctite 3128, Loctite 3220, Loctite 8387B, Matrix 1000, and Kyocera NCO 150SB all perform well with respect to providing a hermetic seal, the FP4651 is the only epoxy which does not require a clamp for sealing and the Loctite 8387B most likely requires additional clamping force. The Kyocera NCO 150 did not adhere well to the Au seal and did not provide a hermetic seal.
 - c. All epoxies, however, failed the water vapor testing requirement of 5,000 ppm or less.
 - d. Fill epoxy experiments are still ongoing and relate to securing multi-chip module die securely within the die cavity, particularly if an inter-cavity substrate is used. Again, the greatest concern is with respect to moisture outgassing within the cavity.

Table 7. Epoxy Encapsulation Results for Hermetic and Cavity Moisture

Epoxy evaluation for SBIR: Hermetic Seal						
Epoxy	Seal method	Inspection Results	Leak check	IVA	Temp Cycling	
FP4651	Gravity 1# Clamp	Marginal Good	5/5 Pass 5/5 Pass	12,216 ppmv moisture	NA	
Loctite 3128	Gravity 1# Clamp	Tilted Good	3/5 pass 5/5 pass	54,533 ppmv moisture	NA	
Loctite 3220	Gravity 1# Clamp	Fail (3 scrap) OK	1/5 pass 5/5 pass	NA	NA	
Loctite 8387B	Gravity 1# Clamp	Tilted Blowholes	4/5 pass 4/5 pass	NA	NA	
Matrix 1000	1# clamp	Good visual seal	5/5 pass	278,707 ppmv	NA	
Kyocera NCO 150SB	1# clamp	Good visual seal	5/5 pass	215,973 ppmv	NA	
Kyocera NCO 150	1# clamp	Did not adhere well to Au seal	NA	NA	NA	

Table 8. Epoxy Encapsulation Results for Temperature Cycling

Epoxy evaluation for SBIR: Fill				
Epoxy	Purpose	Temperature Cycling	Inspection Results	
FP4450	Fill	RIF1K fill and temp cycle test 5 units		
FP4651	Fill	RIF1K fill and temp cycle test 5 units		

2.) Plating Design of Experiments and Results Update:

A description of the current thickness targets based on optimized experimental results for consistent plating and bonding is as follows: 3 um – 4 um Nickel (Ni), 0.2 – 0.5 um Palladium (Pd), and 0.05 – 0.1 um Gold (Au). The study on original die pad aluminum purity and/or presence of contaminants as a variable for successful subsequent ENEPiG plating can be found in Appendix VIII, although the predominant factor influencing consistent ENEPiG plating on the original aluminum die pad surface is the presence of residual aluminum oxide. This oxide can, in the vast majority of cases, be removed with plasma reactive ion etching (RIE) using argon as a sputtering material to dislodge the surface oxide molecules. Sufficient reactive ion etching (RIE) to remove remnant oxide is a process now available when necessary, which has improved plating yields substantially.

Initial plating target thicknesses were determined to be near optimal based on industry research and consensus of industry experts supporting the GCI's vendor chemistry. Historic variations in plating thicknesses were determined to be related to original aluminum die pad preparation prior to plating. Thus, optimization of the ENEPiG process focused on the aluminum die pad reactive ion etch, chemical etch, and subsequent zirconation.

- 3.) The Auger surface contamination study performed by Honeywell can be found in Appendix IX of this report and only revealed silver (Ag), oxygen (O), and carbon (C) as additional elements to what was expected on and around the aluminum pads following GCI's DER™ extraction processing. The silver (Ag) represents low-level remnant material from the silver die attach process and does not present a yield or reliability risk. The oxygen (O) and carbon (C) are typical of any inert organic particulate/residue from the original package or trace amounts of solvent used to rinse the die following extraction. GCI's high-temperature bake data is consistent with these results as no evidence of mobile contamination induced leakage has been seen for the process to date.

- 4.) The five specific device types chosen within this study are as follows:
 - a.) Low pin count (8 pins) originally gold wire bonded device: ADG859
 - b.) Large pin count (144 pins) originally gold wire bonded device: XC4005XL
 - c.) High-Temperature and Low-Temperature variant for head to head DEER™ comparison (gold bond wire): OPA820
 - d.) Large pin count (64 pins) originally copper wire bonded device: ATSAMD21
 - e.) High-Power FET, original eutectic die attach, gold bond wire: STN1NK60Z

These devices were chosen based on meeting the following criteria in conjunction with a study focused on understanding the impact of ENEPIG pad reconditioning process on the reliability of commercial integrated circuits extracted from their standard plastic packages and rebuilt into ceramic packages: As mentioned previously, only four different types of IC projects were proposed initially: 1) low pin count die with gold (Au) bond wire, 2) high pin count die with Au bond wire, 3) low to medium pin count die with copper (Cu) wire, and 4) *DEER*TM processing for a eutectic or solder die attached IC. Later, a fifth project was added: 5) a head-to-head comparison of a *DEER*TM processed commercially available plastic package die vs. its high-temperature version offered by the original component manufacturer. This last device selection was used to compare the *DEER*TM processing of the commercial temperature plastic control units to the hermetic assembly of the original high-temperature die purchased directly from a franchised source.

Table 9 below demonstrates the original manufacturing schedule to produce the number of required devices of each for the ongoing and pending reliability studies. Included in this table is the yield report for each manufacturing step during *DEER*TM processing.

Table 9. Device Yield Summary for 5 Devices Chosen to be Included in this Phase II

Customer	Product	Job	Start	Start	Cut	Thin 1	Copper rem	Backside Clean	Thin 2	Extract	Wire Dress	Gold Ball Removal	Gold Ball Clean	Gold Ball Inspect	Pad Reconditioning	Die Clean	Die Inspect	Die Attach	Bond	Bake	Seal	Mark	Form/Trim	Continuity	IDD	Final Inspect	Ship	Delivered	Yield
SBIR Phase II	OPA820	ENG180615-2	8/17/18	200		199	199	199		198	194	194	194	194	182	182	176	176	175	175	170	167	166	165	165	165	165	82.50%	
SBIR Phase II	ADG859	ENG180712-3	8/24/24	207		203	203	203		203	201	201	201	200	200	197	195	195	195	195	187	181	180	180	180	180	180	86.96%	
SBIR Phase II	ATSAMD21	ENG180716-1	8/24/18	201		201	201	201		200	200			186	186	186	156	156	148	148	147	147	132	127	127	127	127	63.18%	
SBIR Phase II	STN1NK60Z	ENG181208-1	1/11/19	200		200	200	200		199	199			198	198	198	195	97	96	96	96	94	94	94	94	94	94.00%		
SBIR Phase II	XC4005XL	ENG180629-1	8/17/18	109	109	109	109	109	109	109	109	109	109	103	102	102	82	81	76	76	76	76	76	76	76	76	69.72%		
SBIR Phase II	XC4005XL	ENG180629-1-1	8/17/18	85						85	84	84	84	75	75	75	58	58	58	58	58	58	58	53	53	53	53	62.35%	

Updates to this table include successful completion of GCI's *DEER*TM process for the XC4005XL, OPA820, NC7SB3157P6 (ADG859), ATSAMD21, and STN1NK60Z with the final yield analysis as stated above. This assembly yield data includes 100% hermetic testing results (i.e., gross and fine leak check), as well as passing bond pull data and bond wire apex verification for 30,000 g-force acceleration testing. The final yields on the ATSAMD21 and XC4005XL devices were below the 80+% due to a more stringent visual inspection put in place following the gold ball removal and pad re-plating processing (to screen out smaller nodule formation during the electroless plating processing). The green areas within Table 9 indicate portions of the GCI processing, which deliver high-yields, including the high-pin count die (i.e., greater than 100 die pads) as with the ATSAMD21 and XC4005XL devices. The yellow regions within the chart indicate GCI processing for the same larger pad count devices that still remain challenging.

Optical photos for each device listed above can be seen in Figure 8 below:



Figure 8. Optical Photo of GCI Ceramic *DEER™* Versions for ADG859, XC4005XL, OPA820, ATSAMD21, and STN1NK60Z Integrated Circuits.

ADG859 Results Summary:

- a. This device selection supports requirement for low-pin count gold bond wire plastic donor (ADG859) to ceramic conversion.
- b. Device Functionality – Single Pole Double Throw (SPDT) Switch
- c. Initial device screening of the commercial plastic donors indicated functional performance across the -55°C to $+125^{\circ}$ military range for all 200 parts tested.
- d. The complete ADG859 datasheet can be found in the below link:
<https://www.analog.com/media/en/technical-documentation/data-sheets/ADG852.pdf>
- e. Extraction/plating (GCI *DEER™* processing) and hermetic ceramic assembly was performed on this selection with functional yields determined to be $\sim 87\%$. This assembly yield data includes 100% hermetic testing requirements (i.e., gross and fine leak check), as well as passing MIL-STD-883 bond pull data (minimum of 3g for 1.0 mil Au wire and $\sim 2.2\text{g}$ for 0.8 mil Au wire) and bond wire apex verification for 30,000 g-force acceleration testing requirements. The ADG859 ceramic builds were assembled with 1.0 mil Au wire. All devices passed bond pull testing and 30,000 g-force acceleration testing requirements.
- f. The commercial plastic donor device is offered in a 6-Pin Small Outline Transistor (SOT) package.
- g. The extracted and plated device was re-assembled into a hermetic 8-lead ceramic side-brazed dual in-line (DIP) package.
- h. Burn-In/Life-Test Board maximized input and output current load stressing of product during $+125^{\circ}\text{C}$ Dynamic Biased Burn-In/Life-Test. Target pull-down and pull-up currents are 250 - 300 mA each for this device type, or $\sim 1.5\text{W}/\text{device}$. This wattage/device elevates the package temperature to approximately 40°C above ambient as measured with an IR

thermometer. Dynamic toggling of the outputs was generated and maintained with an externally applied 100 kHz square wave.

- i. Appendix X indicates a trend for reduction in IDD draw for pull-up and pull-down loading of the ADG859 for all boards, with continued reduction for Board #'s 1 - 3 at the 7879 hour mark. Initial supply currents all match fairly consistently, although there was a marked degradation in supply current over the span of the Life-Test as seen in Appendix X. The Burn-In/Life-Test configuration for these boards is 48 devices/board for ceramic and 16 devices/board for plastic, for a total of 144 ceramic devices and 48 plastic devices. Figure 9 below depicts the ADG859 Burn-In board type used (1 of 3).

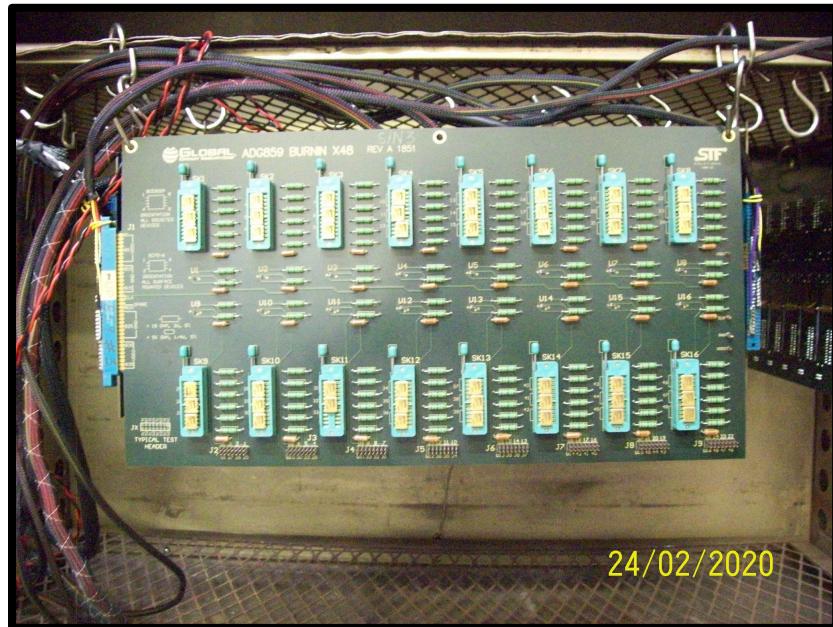


Figure 9. Optical Photo of GCI Ceramic *DEER*TM ADG859 Burn-In/Life-Test Board

Table 10 is a summary of the dynamic board currents for t=0 hours and t=7879 hours for all three ADG859 boards used in this study.

Table 10: ADG859: +125°C Testing, 3 Boards – (March 2, 2019 – 8:30 AM to January 24, 2020 – 3:30 PM)

<u>Board/Supply (@5.5V)</u>	<u>Current @ 0 Hour/7879 Hour</u>
Board1/Supply1	5.64 A/1.84 A
Board1/Supply2	6.40 A/3.86 A
Board2/Supply1	5.66 A/3.13 A
Board2/Supply2	6.37 A/4.36 A
Board3/Supply1	5.65 A/3.16 A
Board3/Supply2	6.40 A/5.30 A

Functional testing of the ADG859 devices at the intervals specified within Appendix X helped to better explain that the reason for the trend in reduced board IDD (supply currents), particularly with respect to Supply #1. Additionally, a lesser percentage of devices on the board indicate degraded outputs. Appendix XI represents an account of degraded, dead, and remaining functional ADG859 devices as it relates to the decrease in

supply current. In summary, functional testing proved that many devices for Supply #1 indicate degraded outputs (weak toggling), or “dead” output (no toggling). A lesser percentage of ceramic devices on the board indicate degraded outputs.

For functionality characterization of the ADG859 within the +125°C Dynamic Burn-In/Life-Test, the four categories are maintained: Passing (G), Slightly Degraded (SD), Heavily Degraded (HD), Barely Alive (BA), and Failing (X). Table 11 below shows the percentage of ceramic and plastic for the various categories following 7879 hours of exposure:

Table 11: Percentage of Ceramic vs. Plastic ADG859 Devices Within Functionality Categories Following 7879 Hours of +125°C Dynamic Biased Burn-In/Life-Test

	Ceramic	Plastic
Passing (G)	34.7%	27.1%
Slightly Degraded (SD)	18.1%	10.4%
Heavily Degraded (HD)	20.1%	4.2%
Barely Alive (BA)	10.4%	10.4%
Failing (F)	<u>14.6%</u>	<u>43.8%</u>
Mixture Between A/B Outputs	2.1%	4.1%

The failures always occurred in plastic first, but appear to be specifically related to degradation of the mux output drive currents for both plastic and ceramic versions, most likely due to charge injection or hot carriers shifting the respective output transistor threshold voltages. This degradation is not surprising given that the mux output transistors were operating at 100% of maximum load and temperature for almost 8000 hours. However, the most valuable conclusion which can be made is that the ceramic ADG859 DEER™ versions degraded more slowly than the ADG859 plastic OCM equivalents, with fewer failures, indicating the robustness and reliability of the DEER™ process and overall superior performance of the device in ceramic vs. plastic packaging.

- j. +250°C initial unbiased bake testing for reliability connectivity of the DEER™ process within ceramic packaging relative to franchised (authorized supply chain) plastic donor ADG859 product achieved the 5053 hour mark. Appendix XII shows that the original plastic donor devices began failing at 504 hours, with all pins failing connectivity resistance tests on all parts by 1000 hours. In stark contrast, Appendix XIII demonstrates that none of the pins for the Ceramic DEER™ equivalent devices have failed after 5053 hours with exposure to the same conditions.
- k. Not only did pre-bake bond pull data pass testing for production builds of the ADG859, but bond pull data consistent with test methods from MIL-STD 883 for two randomly selected devices following Dynamic Burn-In/Life-Test testing at 125°C was taken with Mean-3x(sigma) test results of 4.1g and 6.2g for the two devices tested (see Appendix XXII), with a pre-bake minimum specification limit of 3g. No failures were experienced on any pin during bond pull for the two post Burn-In/Life-Test devices tested and the Mean-3sigma data also passes the MIL-STD-883 testing requirements.
- l. Hermetic Package Testing on 4 devices each, followed by internal vapor analysis (IVA) testing on 1 each of the 5 device types were performed following 7879 hours of Dynamic Burn-In/Life-Test testing at 125°C, and with test methods and limits consistent

from MIL-STD 883. No failures were experienced (see Appendices XXIII and XXIV, respectively).

XC4005XL Results Summary:

- a. This device selection supports requirement for high-pin count gold bond wire plastic donor (XC4005XL) to ceramic conversion.
- b. Device Functionality – Field Programmable Gate Array (FPGA).
- c. Initial device screening of the commercial plastic donors indicated functional performance across the -55°C to +125° military range for all 195 parts tested.
- d. The complete XC4005XL datasheet can be found in the below link:
<https://www.digchip.com/datasheets/parts/datasheet/534/XC4005XL-pdf.php>
- e. Extraction/plating (GCI *DEER*™ processing) and hermetic ceramic assembly was performed on this selection with functional yields determined to be ~67%. The greatest yield hit in the *DEER*™ processing was the pad-reconditioning, or ENEPIG processing. This assembly yield data includes 100% hermetic testing requirements (i.e., gross and fine leak check), as well as passing MIL-STD-883 bond pull data (minimum of 3g for 1.0 mil Au wire and ~2.2g for 0.8 mil Au wire) and bond wire apex verification for 30,000 g-force acceleration testing requirements. The XC4005XL ceramic builds were assembled with 0.8 mil Au wire. All devices passed bond pull testing and 30,000 g-force acceleration testing requirements.
- f. The commercial donor device is offered in a 144-Pin Thin-Quad-Flat-Pack (TQFP) package.
- g. The extracted and plated device was re-assembled into a hermetic 144-Pin ceramic Pin Grid Array (PGA) package.
- h. Burn-In/Life-Test Board maximized input and output current load stressing of product during +125°C Dynamic Biased Burn-In/Life-Test. Target pull-down and pull-up currents are ~35 mA each on four outputs for this device type, or ~0.5W/device. This wattage/device elevated the package temperature to approximately 15°C above ambient as measured with an IR thermometer. The goal was to maximize input and output current load stressing of product during 125°C Dynamic Biased Burn-In/Life-Test. The original 60 mA load has been determined to excessively degrade the required logic level to maintain signal toggling (maximum logic “high” and “low” current levels of 60 mA and 100 mA, respectively). Burn-In/Life-Test boards for the 125°C dynamic testing were designed to program 20 XC4005XL ceramic devices and 8 plastic devices with the ability to propagate a 1 kHz square wave through each of the 14 devices per Burn-In/Life-Test board (daisy chain), with 4 I/O (one per side) loaded with 100 ohm resistors for maximum output current. No failure were experienced for the entirety of the test.
- i. Appendix X indicates a fairly stable IDD draw for pull-up and pull-down loading of the XC4005XL devices for all boards, with only a slight reduction in current from 0 hours at 125°C to 2543 hours at 125°C, with the entirety of the 6% reduction coming in the last 600 hours of testing. The Burn-In/Life-Test configuration for these boards is 10 devices/board

for ceramic and 4 devices/board for plastic, for a total of 20 ceramic devices and 8 plastic devices. Figure 10 below depicts the XC4005XL Burn-In board type used (1 of 2).

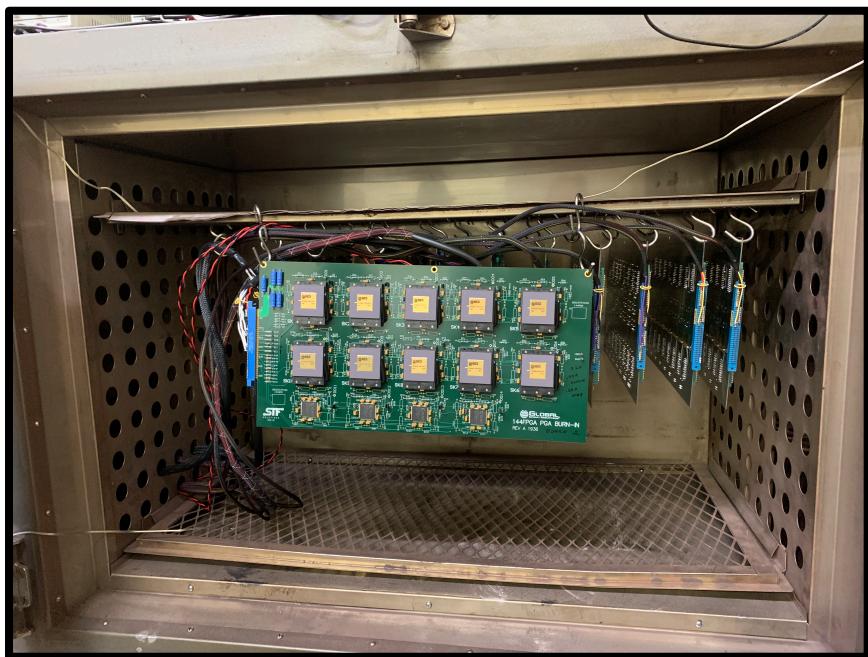


Figure 10. Optical Photo of GCI Ceramic *DEER*™ XC4005XL Burn-In/Life-Test Board

Table 12 is a summary of the dynamic board currents for t=0 hours and t=2543 hours for all three XC4005XL boards used in this study.

Table 12: XC4005XL: +125°C Testing, 2 Boards – (October 10, 2019 – 5:00 PM to January 24, 2020 – 3:30 PM)

Board/Supply (@5.5V)	Current @ 0 Hour/2543 Hour
Board1/Supply1 + Board2/Supply1	0.94 A/0.88 A

Functional testing of the XC4005XL devices at the intervals specified within Appendix X consistently determined that all devices (for the ceramic *DEER*™ conversions and plastic donor variety) continued functioning identically from the beginning of the Life-Test until the end, with only a slight degradation in output current after 2543 hours of cycling. VIH (voltage input high condition), VIL (voltage input low condition), VOL (voltage output Low condition), VOH (voltage output high condition), IOH (current output high condition), IOL (current output low condition) testing showed insignificant to no degradation in functional performance for the entirety of the test.

To be consistent with the results description, Table 13 below shows the percentage of ceramic and plastic for the various categories following 2543 hours of exposure:

Table 13: Percentage of Ceramic vs. Plastic XC4005XL Devices Within Functionality Categories Following 2543 Hours of +125°C Dynamic Biased Burn-In/Life-Test

	Ceramic	Plastic
Passing (G)	100%	100%

The conclusion which can be made is that neither the ceramic XC4005XL DEERTM versions nor the XC4005XL plastic equivalents produced failures, indicating the equivalent robustness and reliability of the DEERTM processing vs. the original OCM plastic variety.

- j. +250°C initial unbiased bake testing for reliability connectivity of the DEERTM process within ceramic packaging relative to franchised (authorized supply chain) plastic donor XC4005XL product achieved the 5053 hour mark. Appendix XIV shows that the original plastic donor devices began failing at 2000 hours. In stark contrast, Appendix XV demonstrates that none of the pins for the Ceramic DEERTM equivalent devices have failed after 5053 hours with exposure to the same conditions.
- k. Not only did pre-bake bond pull data pass testing for production builds of the XC4005XL, but bond pull data consistent with test methods from MIL-STD 883 for two randomly selected devices following Dynamic Burn-In/Life-Test testing at 125°C was taken with Mean-3x(sigma) test results of 3.1g and 2.9g for the two devices tested (see Appendix XXII), with a pre-bake minimum specification limit of 2.2g. No failures were experienced on any pin during bond pull for the two post Burn-In/Life-Test devices tested and the Mean-3sigma data also passes the MIL-STD-883 testing requirements.
- l. Hermetic Package Testing on 4 devices each, followed by internal vapor analysis (IVA) testing on 1 each of the 5 device types were performed following 2543 hours of Dynamic Burn-In/Life-Test testing at 125°C, and with test methods and limits consistent from MIL-STD 883. No failures were experienced (see Appendices XXIII and XXIV, respectively).
- m. Initial testing of the XC4005XL device performance indicates that the functional operation temperature range was increased by at least +15°C to +20°C by re-assembling the device from its plastic package into a higher heat conducting capable ceramic package (i.e., decreased °C/Watt heat transfer coefficient), thereby reducing the relative to junction to ambient temperature delta. Actual testing in plastic at the AAA test facility indicated nominal performance of 129 pieces to at least +125°C to +140°C.

OPA820 Results Summary:

- a. This device selection supports the High-Temperature and Low-Temperature vehicle for head-to-head DEERTM comparison for gold bond wire, with the experiment originally designed and engineered for high-temperature operation vs. its lower-temperature plastic equivalent in the same conditions. The low-temperature plastic was designed for a temperature range of -55°C to +85°C, while the high-temperature die was designed for -55°C to +210°C. Thus, the head-to-head comparison qualification and life test study request between an already MIL-STD 883 qualified device and its DEERTM ceramic packaged commercial equivalent (low-temperature plastic donor) was implemented by means of the OPA820 high-temperature die purchase (TO-can build for performance and reliability comparison) relative to the plastic lower temperature donor control units using the DEERTM ceramic conversions of the lower temperature plastic material.
- b. Device Functionality – Operational Amplifier (OPAMP)

- c. Initial device screening of the commercial plastic donors confirmed functional performance across the -55°C to +125° military range for all 200 parts tested.
- d. The complete OPA820 datasheet can be found in the below link:
<http://www.ti.com/lit/ds/sbos303d/sbos303d.pdf>
- e. Extraction/plating (GCI *DEER*™ processing) and hermetic ceramic assembly was performed on this selection with functional yields determined to be ~83%. This assembly yield data includes 100% hermetic testing requirements (i.e., gross and fine leak check), as well as passing MIL-STD-883 bond pull data (minimum of 3g for 1.0 mil Au wire and ~2.2g for 0.8 mil Au wire) and bond wire apex verification for 30,000 g-force acceleration testing requirements. The OPA820 ceramic builds were assembled with 1.0 mil Au wire. All devices passed in-line bond pull testing and 30,000 g-force acceleration testing requirements.
- f. The commercial plastic donor device is offered in an 8-Pin Small Outline Integrated Circuit (SOIC) package.
- g. The extracted and plated device was re-assembled into a hermetic 8-lead ceramic side-brazed dual in-line (DIP) package.
- h. Burn-In/Life-Test Board maximized input and output current load stressing of product during +125°C Dynamic Biased Burn-In/Life-Test. Load resistors were set at 50 ohms for a maximum output current load of 125 mA, or ~0.7W/device, for a net increase in package temperature of about 20°C above ambient (as confirmed with an IR thermometer). 60 ceramic devices/board and 20 plastic devices/board require 2 boards for a total of 120 ceramic and 40 plastic devices under test. Toggling of the OPA820 devices was performed at 1 KHz to provide alternating load/no-load conditions. Half of the devices were loaded through the 50 ohm resistor to VDD, while the other half were loaded to VSS.
- i. Appendix X indicates a trend for reduction in IDD draw for pull-up and pull-down loading of the OPA820 for Board #'s 1 & 2 at the 7829 hour mark. Initial supply currents all match fairly consistently, although there was an approximate 12% degradation in supply current over the span of the Life-Test. The Burn-In/Life-Test configuration for these boards is 60 devices/board for ceramic and 20 devices/board for plastic, for a total of 120 ceramic devices and 40 plastic devices. Figure 11 below depicts the OPA820 Burn-In board type used (1 of 2).

Table 14 is a summary of the dynamic board currents for t=0 hours and t=7829 hours for both boards used in this study.

Table 14: OPA820: +125°C Testing, 2 Boards – (March 4, 2019 – 10:00 AM to January 24, 2020 – 3:30 PM)

<u>Board/Supply (@5.5V)</u>	<u>Current @ 0 Hour/7829 Hour</u>
Board1/Supply1 + Board2/Supply1	6.97 A/6.11 A

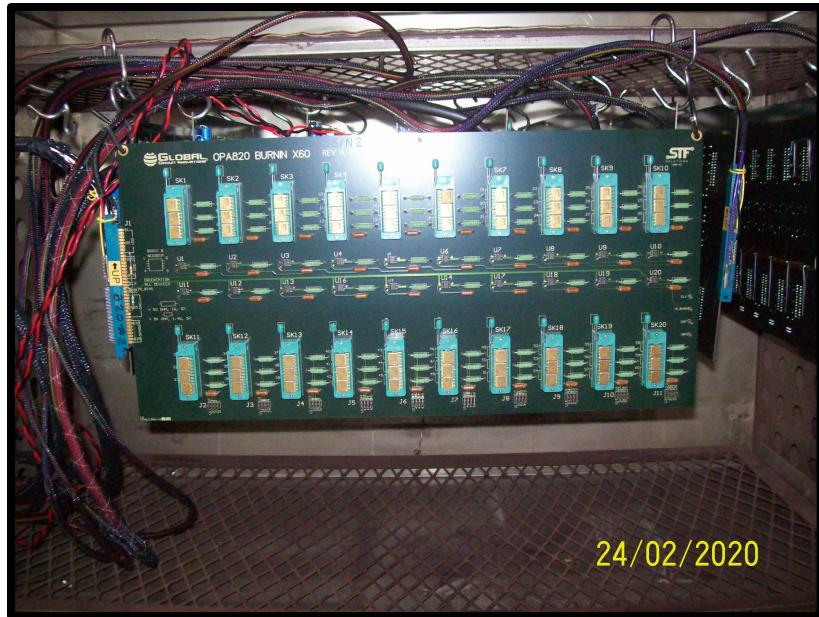


Figure 11. Optical Photo of GCI Ceramic *DEER*™ OPA820 Burn-In/Life-Test Board

The slight IDD current reduction seen in Appendix X is due to minimal degradation in the outputs for both the plastic controls and the ceramic *DEER*™ conversion devices, most likely due to hot carrier degradation in the output threshold transistors. All devices continued to pass VOL, VOH, VIL, VIH, IIL, and IIH criterial. No difference in performance between TI provided “high-temperature” OPA820 die and GCI OPA820 *DEER*™ die re-packaged into ceramic high-temperature package options was noted for +125°C Biased Dynamic Burn-In/Life-Testing. Oscilloscope probing of the each of the outputs provided confirmation that all parts continued to toggle at the designated frequency of 1KHz. No additional degradation in the plastic donor ‘control’ packages was seen for identical exposure (see Table 15 below).

Table 15: Percentage of Ceramic vs. Plastic OPA820 Devices Within Functionality Categories Following 7829 Hours of +125°C Dynamic Biased Burn-In

Passing (G)	<u>Ceramic</u>	<u>Plastic</u>
100%	100%	100%

- j. +250°C initial unbiased bake testing for reliability connectivity of the *DEER*™ process within ceramic packaging relative to franchised (authorized supply chain) plastic donor OPA820 product achieved the 5053 hour mark. Appendix XVI shows that the original plastic donor devices began failing at 2000 hours. By comparison, Appendix XVII demonstrates that none of the pins for the Ceramic *DEER*™ equivalent devices have failed after 5053 hours with exposure to the same conditions.
- k. Not only did pre-bake bond pull data pass testing for production builds of the OPA820, but bond pull data consistent with test methods from MIL-STD 883 for two randomly selected devices following Dynamic Burn-In/Life-Test testing at 125°C was taken with Mean-3x(sigma) test results of 7.7g and 7.0g for the two devices tested (see Appendix XXII), with a pre-bake minimum specification limit of 3g. No failures were experienced on any pin during bond pull for the two post Burn-In/Life-Test devices tested and the Mean-3sigma data also passes the MIL-STD-883 testing requirements.

1. Hermetic Package Testing on 4 devices each, followed by internal vapor analysis (IVA) testing on 1 each of the 5 device types were performed following 7829 hours of Dynamic Burn-In/Life-Test testing at 125°C, and with test methods and limits consistent from MIL-STD 883. No failures were experienced (see Appendices XXIII and XXIV, respectively).

ATSAMD21 Results Summary:

- a. This device selection supports requirement for high-pin count copper wire plastic donor (ATSAMD21) to ceramic conversion.
- b. Device Functionality – Microcontroller.
- c. Initial device screening of the commercial plastic donors indicated functional performance across the -55°C to +125° military range for all 200 parts tested.
- d. The complete ATSAMD21 datasheet can be found in the below link:
<http://ww1.microchip.com/downloads/en/DeviceDoc/40001882A.pdf>
- e. Extraction/plating ATSAMD21 (GCI *DEERT*TM processing) and hermetic ceramic assembly was performed on this selection with functional yields determined to be ~63.2%. The greatest yield hit in the *DEERT*TM processing was the pad-reconditioning, or ENEPIG processing. This assembly yield data includes 100% hermetic testing requirements (i.e., gross and fine leak check), as well as passing MIL-STD-883 bond pull data (minimum of 3g for 1.0 mil Au wire and ~2.2g for 0.8 mil Au wire) and bond wire apex verification for 30,000 g-force acceleration testing requirements. The ATSAMD21 ceramic builds were assembled with 0.8 mil Au wire. All devices passed bond pull testing and 30,000 g-force acceleration testing requirements.
- f. The commercial donor device is offered in a 48-pin plastic quad lead flat pack (PQFP).
- g. The extracted and plated device was re-assembled into a hermetic 64-Pin ceramic Pin Grid Array (PGA) package.
- h. Burn-In/Life-Test Board design maximized input and output current load stressing of product during +125°C Dynamic Biased Burn-In/Life-Test. Total output drive for both logic “high” and logic “low” levels were measured on the curve tracer ATSAMD21 I/O to determine optimum load resistance vs. performance. Target pull-down and pull-up currents are ~35 mA each on four outputs for this device type, or ~0.5W/device. This wattage/device elevated the package temperature to approximately 15°C above ambient as measured with an IR thermometer.

The goal was to maximize input and output current load stressing of product during +125°C Dynamic Biased Burn-In/Life-Test. The original 60 mA load was determined to excessively degrade the required logic level to maintain signal toggling (maximum logic “high” and “low” current levels of 60 mA and 100 mA, respectively). Even the final 35 mA loading I/O was excessive to maintain active VIL/VIH conditions, but the board was designed such that each daisy chain signals were not required and the outputs could be stressed accordingly.

Burn-In/Life-Test boards for the 125°C dynamic testing were designed to program 20 ATSAMD21 ceramic devices and 8 plastic devices with an effective internally generated and programmed clock toggling at 1 kHz, with 4 I/O (one per side) loaded for maximum output current. Plastic devices began to experience toggling issues in as little as 818 hours, with all but 1 (7/8) failing at 2259 hours. Ceramic devices began failing at 1825 hours, with 5 of 20 failing by the end of the test (2259 hours).

- i. Appendix X indicates a steadily increasing IDD draw for pull-up and pull-down loading of the ATSAMD21 devices for both boards during toggling (see Table 16 below). The Burn-In/Life-Test configuration for these boards is 48 devices/board for ceramic and 16 devices/board for plastic, for a total of 20 ceramic devices and 8 plastic devices. Figure 12 below depicts the ATSAMD21 Burn-In board type used (1 of 2).

Table 16: ATSAMD21: +125°C Testing, 2 Boards – (October 22, 2019 – 5:00 PM to January 24, 2020 – 3:30 PM)

Board/Supply (@3.3V) Current @ 0 Hour/2259 Hour

Board 1/Supply 1	2.50 A/3.74 A
Board 2/Supply 1	2.51 A/4.23 A

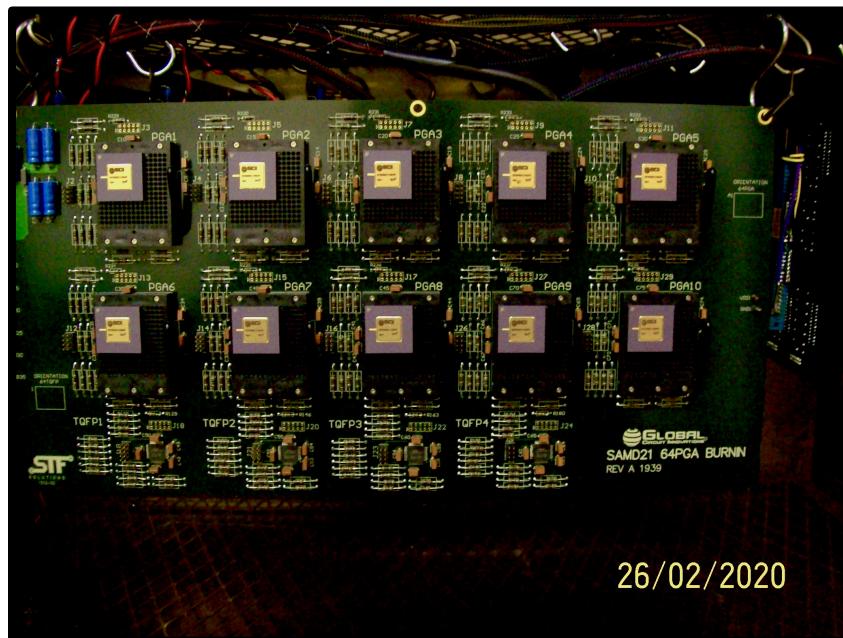


Figure 12. Optical Photo of GCI Ceramic *DEER*™ ATSAMD21 Burn-In/Life-Test Board

Functional testing of the ATSAMD21 devices at the intervals specified within Appendix X determined that both the plastic controls and *DEER*™ ceramic equivalents began failing during Life-Test, with the plastic controls failing sooner (818 hours) vs. the *DEER*™ processed devices not failing until 1825 hours. Further, the plastic devices failed at 3x the rate of ceramic (see Table 13).

Table 17 below shows the percentage of ceramic and plastic for the various categories following 2259 hours of exposure:

Table 17: Percentage of Ceramic vs. Plastic ATSAMD21 Devices Passing/Failing Following 2259 Hours of +125°C Dynamic Biased Burn-In/Life-Test

	<u>Ceramic</u>	<u>Plastic</u>
Passing (G)	75%	12.5%
Failing (F)	25%	87.5%

However, it was determined that VIH (voltage input high condition), VIL (voltage input low condition), VOL (voltage output Low condition), VOH (voltage output high condition), IOH (current output high condition), IOL (current output low condition) testing showed insignificant to no degradation in functional performance for the entirety of the test. Rather, the responsible failure mechanism was associated with charge retention of the EEPROM (Electrically Erasable Programmable Read Only Memory) cells. Reprogramming of the ceramic devices returned them to functionality in each case.

To explore this difference in reliability (i.e., memory retention in this case), one needs to reference the ATSAMD21 datasheet where memory retention vs. program cycling, temperature exposure, and time is referenced. For example, the devices researched in this study (both plastic and *DEER*™ ceramic processed) were exposed to cycling less than 100 program cycles. For an ambient temperature of 55°C, the devices could be expected to maintain memory for 25 to 100 years (or, 219K hours – 876K hours). However, this retention would necessarily be less at higher temperatures. If we assume that +125°C is the ambient, the junction temperature would be increased from the wattage dissipated from the part due to output loading, or 0.5W. For a ceramic package, the thermal resistance would be approximately 18°C/W for the ceramic package and approximately 45°C for the plastic encapsulated variety.

Therefore, the junction temperature of the die in the ceramic package would be on par with $125^{\circ}\text{C} + 0.5*18^{\circ}\text{C/W}$, or 134°C. The junction temperature of the die within the plastic package can be estimated at $125^{\circ}\text{C} + 0.5*45^{\circ}\text{C/W}$, or 148°C. If we assume that the activation energy for the electron leakage mechanism of the EEPROM doubles every 10°C (industry standard), then the retention would be reduced by $2^{(134^{\circ}\text{C} - 55^{\circ}\text{C})/10^{\circ}\text{C}}$, or 239x for the ceramic package, and $2^{(148^{\circ}\text{C} - 55^{\circ}\text{C})/10^{\circ}\text{C}}$, or 630x for the plastic package variety. Using the 25 to 100 year guideline at 55°C, this would equate to failures beginning around 219K hours/239, or 916 hours for the ceramic, and 219K hours/630, or 347 hours for the plastic equivalent package. These numbers are very close to what was experienced during Life-Test.

The conclusion which can be made the ceramic *DEER*™ versions are more reliable than the plastic ‘control’ equivalents, because the ATSAMD21 *DEER*™ die remains cooler in the ceramic package due to lower thermal resistance under output loading.

- j. +250°C initial unbiased bake testing for reliability connectivity of the *DEER*™ process within ceramic packaging relative to franchised (authorized supply chain) plastic donor ATSAMD21 product achieved the 5053 hour mark (see Appendix XVIII) . Appendix XIX shows that the original plastic donor devices began failing by 504 hours. In stark contrast, Appendix XVIII demonstrates that none of the pins for the Ceramic *DEER*™ equivalent devices have failed after 5053 hours with exposure to the same conditions.

- k. Not only did pre-bake bond pull data pass testing for production builds of the XC4005XL, but bond pull data consistent with test methods from MIL-STD 883 for two randomly selected devices following Dynamic Burn-In/Life-Test testing at 125°C was taken with Mean-3x(sigma) test results of 3.1g and 2.2g for the two devices tested (see Appendix XXII), with a pre-bake minimum specification limit of 2.2g. As a comparison, one pre-bake device was used to baseline the bond pull testing (also included in Appendix XXII) with a Mean-3x(sigma) value of 2.9g. No failures were experienced on any pin during bond pull for the two post Burn-In/Life-Test devices tested and the Mean-3sigma data also passes the MIL-STD-883 testing requirements.
- 1. Hermetic Package Testing on 4 devices each, followed by internal vapor analysis (IVA) testing on 1 each of the 5 device types were performed following 2259 hours of Dynamic Burn-In/Life-Test testing at 125°C, and with test methods and limits consistent from MIL-STD 883. No failures were experienced (see Appendices XXIII and XXIV, respectively).

STN1NK60Z Results Summary:

- a. This device selection supports requirement for a *DEER*TM processed eutectic die attach donor with high-current drain requiring subsequent backside low-resistance connection (project chosen to satisfy David Johnson's request regarding the merits of using die extracted from packages originally die attached with either solder or gold eutectic).
- b. New bonding of the backside high-current device has shown a die attach resistance (<1 ohm) is insignificant to the 13 ohm 'on' resistance (using H20E die attach).
- c. Device Functionality – N-Channel 600V, 13 ohm typical R_{ds(On)}, 0.3A Zener-Protected Power MOSFET
- d. Initial device screening of the commercial plastic donors indicated functional performance across the -55°C to +125° military range for all 200 parts tested.
- e. The complete ADG859 datasheet can be found in the below link:
<https://www.st.com/resource/en/datasheet/stn1nk60z.pdf>
- f. Extraction/plating (GCI *DEER*TM processing) and hermetic ceramic assembly was performed on this selection with functional yields determined to be ~94%. This assembly yield data includes 100% hermetic testing requirements (i.e., gross and fine leak check), as well as passing MIL-STD-883 bond pull data (minimum of 3g for 1.0 mil Au wire and ~2.2g for 0.8 mil Au wire) and bond wire apex verification for 30,000 g-force acceleration testing requirements. The STN1NK60Z ceramic builds were assembled with 1.0 mil Au wire. All devices passed bond pull testing and 30,000 g-force acceleration testing requirements.
- g. The commercial plastic donor device is offered in a 3-Pin Small Outline Transistor (SOT-223) package.
- h. The extracted and plated device was re-assembled into a hermetic 8-lead ceramic side-brazed dual in-line (DIP) package in a 2x configuration (i.e, Two STN1NK60Z die/package).

- i. Burn-In/Life-Test Board maximized input and output current load stressing of product during +125°C Dynamic Biased Burn-In/Life-Test. Target pull-down and pull-up currents are 300 - 350 mA each for this device type, or ~3.6W/device (operating at 5.5V with 2 die/package, 0.5V drop from 6.0V supply to Burn-In/Life-Test board). This wattage/device elevates the package temperature to approximately 50°C – 60°C above ambient as measured with an IR thermometer. Dynamic toggling of the outputs was generated and maintained with an externally applied 100 kHz square wave.
- j. Appendix X indicates a slight reduction in IDD draw for pull-down loading of the STN1NK60Z for Supply 1 on the board between Life-Test hours 6789 and 7390. All other supply currents all maintained fairly consistent current draw. The Burn-In/Life-Test configuration for these boards is 48 devices/board for ceramic and 16 devices/board for plastic, for a total of 60 ceramic packages (or, 120 units at 2/package) and 20 plastic devices. Figure 13 below depicts the STN1NK60Z Burn-In board type used.

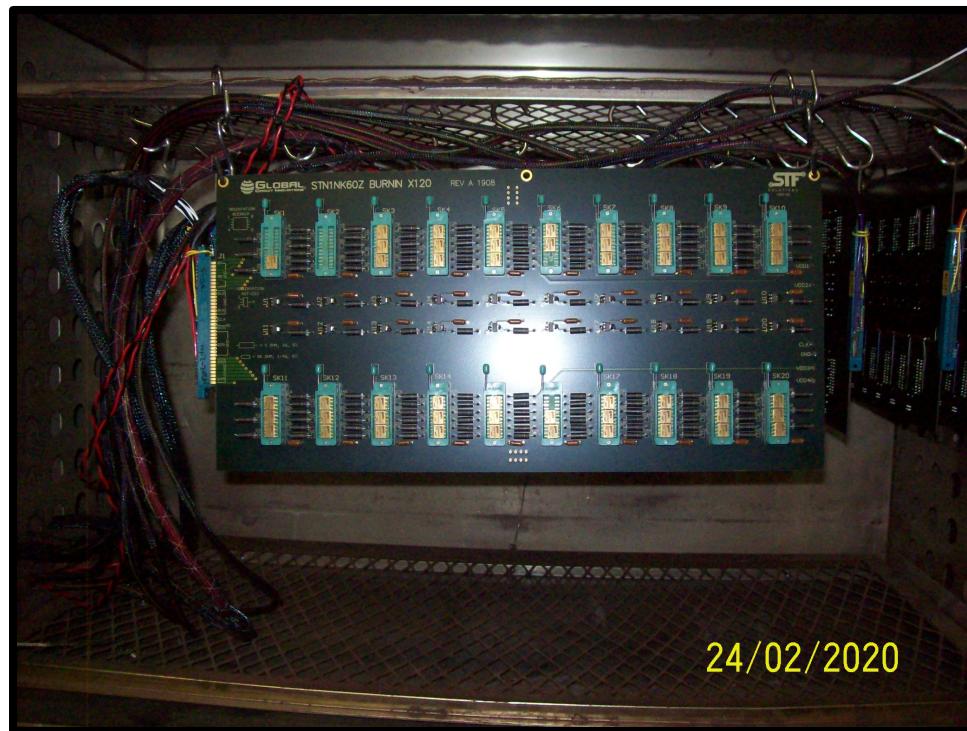


Figure 13. Optical Photo of GCI Ceramic DEER™ STN1NK60Z Burn-In/Life-Test Board

Table 18 is a summary of the dynamic board currents for t=0 hours and t=7390 hours for the singular STN1NK60Z board used in this study.

Table 18: STN1NK60Z: +125°C Testing, 1 Board – (March 22, 2019 – 5:00 PM to January 24, 2020 – 3:30 PM)

Board/Supply (@6.0V) Current @ 0 Hour/7390 Hour

Board 1 – Supply 1	2.49 A/1.77 A
Board 1 – Supply 2	2.47 A/2.33 A
Board 1 – Supply 3	2.51 A/2.47 A
Board 1 – Supply 4	2.52 A/2.36 A

Functional testing of the STN1NK60Z devices at the intervals specified within Appendix X helped to better explain that the reason for the trend in reduced board IDD (supply currents), particularly with respect to Supply #1. Additionally, a lesser percentage of devices on Supply #'s 2, 3, & 4 indicate degraded outputs. Appendix XI represents an account of degraded, dead, and remaining functional STN1NK60Z devices as it relates to the decrease in supply current. In summary, functional testing proved that many devices for Supply #1 indicate degraded outputs (weak toggling), or “dead” output (no toggling). A lesser percentage of ceramic devices on the board indicate degraded outputs.

For functionality characterization of the STN1NK60Z within the +125°C Dynamic Burn-In/Life-Test, the four categories are maintained: Passing (G), Slightly Degraded (SD), and Heavily Degraded (HD). Table 19 below shows the percentage of ceramic and plastic for the various categories following 7390 hours of exposure:

Table 19: Percentage of Ceramic vs. Plastic STN1NK60Z Devices Within Functionality Categories Following 7390 Hours of +125°C Dynamic Biased Burn-In/Life-Test

	<u>Ceramic</u>	<u>Plastic</u>
Passing (G)	99.2%	50.0%
Slightly Degraded (SD)	0.8%	45.0%
Heavily Degraded (HD)	<u>0.0%</u>	<u>5.0%</u>
	100.0%	100.0%

The failures always occurred in plastic first, and appear to be specifically related to degradation of the output drive currents, most likely due to charge injection or hot carriers shifting the respective output transistor threshold voltages. This degradation is not surprising given that the mux output transistors were operating at 100% of maximum load and temperature for 7390 hours. However, the most valuable conclusion which can be made is that the ceramic STN1NK60Z DEER™ versions degraded more slowly than the STN1NK60Z plastic OCM equivalents, and with far fewer failures, indicating the robustness and reliability of the DEER™ process and overall superior performance of the device in ceramic vs. plastic packaging. Much of this increase in reliability is most likely attributable to lower operating junction temperatures, for identical loading and heat generation, and which is due to the lower thermal resistance of the ceramic package.

- k. +250°C initial unbiased bake testing for reliability connectivity of the DEER™ process within ceramic packaging relative to franchised (authorized supply chain) plastic donor STN1NK60Z product achieved the 5053 hour mark. Appendix XX shows that the original plastic donor devices began failing at 1000 hours, with all pins failing connectivity resistance tests on all parts by 2000 hours. In stark contrast, Appendix XIII demonstrates that none of the pins for the Ceramic DEER™ equivalent devices have failed after 5053 hours with exposure to the same conditions.
- l. Not only did pre-bake bond pull data pass testing for production builds of the STN1NK60Z, but bond pull data consistent with test methods from MIL-STD-883 for two randomly selected devices following Dynamic Burn-In/Life-Test testing at 125°C was taken with Mean-3x(sigma) test results of 9.3g and 11.9g for the two devices tested (see Appendix XXII), with a pre-bake minimum specification limit of 3g. No failures were experienced on any pin during bond pull for the two post Burn-In/Life-Test devices tested.

m. Hermetic Package Testing on 4 devices each, followed by internal vapor analysis (IVA) testing on 1 each of the 5 device types were performed following 7390 hours of Dynamic Burn-In/Life-Test testing at 125°C, and with test methods and limits consistent from MIL-STD 883. No failures were experienced (see Appendices XXIII and XXIV, respectively).

5. CONCLUSIONS

Commercial integrated circuits have reliability limitations due in large part to the lack of hermetic packaging and the formation of undesired inter-metallics at the interface between the aluminum pad on the IC and gold wire bond that connects the pad to the IC package, particularly at higher temperatures. It is well known that die extraction/ reassembly (*DEER™*) of commercial integrated circuits into ceramic packages increases the reliability of those devices. By removing the existing gold ball remnant connections and reconditioning the aluminum pads on commercial die with a plated ENEPIG (Electroless Nickel, Electroless Palladium, Immersion Gold) layer, certain failure modes associated with the formation of Al-Au pad inter-metallics and compound bonding can be eliminated entirely.

The ultimate direction in all of the included process development and qualification results is to prove that the *DEER™* process is viable in producing reliable solutions to otherwise obsolete military IC devices. Lastly, GCI's *DEER™* processing was developed originally to eliminate compound bonding as well as any possibility of intermetallic formation between the original gold ball bond and the aluminum die pad.

Part selection for the low-pin count gold bond wire, high-pin count gold bond wire, high-pin count copper wire, high-temperature die vs. low-temperature plastic equivalent for conversion, and originally eutectic bonded high power FET devices were agreed to within Technical Interchange Meetings. The actual devices chosen to satisfy these requirements were the ADG859, XC4005XL, OPA820, ATSAMD21, and STN1NK60Z. Successful extraction and GCI *DEER™* processing was performed for each of the devices chosen. In each of the *DEER™* projects listed above, the proper ENEPIG plating process was optimized and characterized with respect to plating thickness and remnant gold alloy on the aluminum pads.

Yields on the lower pin count devices were above 80%, while yields on the higher pin count devices were lower than 80%. All devices were able to meet the MIL-STD-883 temperature range requirements of operation from -55°C to +125°C. Bond pull testing results prior to lid-seal met all requirements for the various devices: ADG859, OPA820, and STN1NK60Z devices were assembled with 1.0 mil gold wire, while the XC4005XL and ATSAMD21 devices were assembled with 0.8 mil gold wire (due to a reduced die pad size and pitch of 60 um and 80 um, respectively).

All bond wire heights were carefully optimized to meet 30,000 g-force centrifuge requirements. All die were attached with JM7000 silver glass, with exception to the STN1NK60Z requiring a higher resistance H20E die attach epoxy to meet backside contact resistance requirements.

All Group A testing within Table I of Appendix I is included in the 125°C Dynamic biased Burn-In and Life testing implemented in this study was explicitly designed to examine functional shifts on the inputs (IIL and IIH testing), as well as any possible loading shifts on the outputs (VIL, VIH, VOL, and VOH testing) during actual functional signal toggling while the devices are under bias, nominal frequency switching, and maximum output loading.

+125°C Dynamic Burn-In/Life-Test Board biasing requirements were increased to meet maximum loading and heat dissipation limits for each device as specified on the datasheets. The plastic donor control devices and the GCI *DEER*™ processed ceramic equivalents all passed 168 hours of Burn-In testing with these configurations. The total time exposure for each device under maximum loading conditions is as follows in Table 20 below:

Table 20: Maximum Hours of +125°C Dynamic Biased Life-Test Exposure for Each Device

<u>Device Type</u>	<u>Hours of Exposure for Dynamic Biased +125°C Life-Test</u>
ADG859	7879 Hours
XC4005XL	2543 Hours
OPA820	7829 Hours
ATSAMD21	2259 Hours
STN1NK60Z	7390 Hours

No failures were experienced for the XC4005XL or OPA820 devices during Life-Test. The ADG859, ATSAMD21, and STN1NK60Z devices all experienced failures during Life-Test, with the plastic donor controls always failing sooner and in higher frequency than the GCI *DEER*™ processed ceramic equivalents.

The most valuable conclusion which can be made is that the ceramic STN1NK60Z *DEER*™ versions degraded more slowly than the STN1NK60Z plastic OCM equivalents, and with far fewer failures, indicating the robustness and reliability of the *DEER*™ process and overall superior performance of the device in ceramic vs. plastic packaging. Much of this increase in reliability is most likely attributable to lower operating junction temperatures, for identical loading and heat generation, and which is due to the lower thermal resistance of the ceramic package.

250°C Unbiased Bake Connectivity testing has already demonstrated a marked improvement in reliability performance for the *DEER*™ processing relative to the plastic controls for all devices selected. No *DEER*™ ceramic devices failed this test following 5053 hours of exposure, while all of the plastic control types are failed at or before 2000 hours. The +250°C exposure acceleration factor is nearly 6000 compared to operation at +125°C and predicts no connectivity issues for devices operating continuously at +125°C for over 3500 years.

Following thousands of hours of +125°C Dynamic Biased Life-Testing exposure at maximum load conditions, Bond Pull data, Hermeticity, and IVA testing for each of the five devices studied produced passing MIL-STD-883 test results.

The Auger surface contamination study performed by Honeywell of this report only revealed silver (Ag), oxygen (O), and carbon (C) as additional elements to what was expected on and around the aluminum pads following GCI's DER™ extraction processing. The silver (Ag) represents low-level remnant material from the silver die attach process and does not present a yield or reliability risk. The oxygen (O) and carbon (C) are typical of any inert organic particulate/residue from the original package or trace amounts of solvent used to rinse the die following extraction.

Evaluations of epoxy outgassing within hermetic package configurations indicate that some epoxies are optimal to meet most MIL-STD 883 IVA cavity requirements and mechanical testing (shock, vibration, and centrifuge), but continue to be challenged by the 5000 ppm moisture criteria.

GCI has successfully demonstrated the manufacturability and benefit of plated ENEPIG films to enhance the reliability of commercial ICs that have been extracted from their original package and reassembled into a ceramic package (*DEER™*), while eliminating compound bonding with 10's of thousands of devices in the field for high-temperature, high-vibration, and high-reliability applications. A thorough reliability study involving MIL-STD 883 qualification for the *DEER™* process is now able to be reviewed in detail as well, with the GCI *DEER™* Ceramic solution

The significance of the conclusion that all GCI *DEER™* processed devices performed at the same or higher reliability level than all plastic donors, in addition to meeting or exceeding every MIL-STD 883 test parameter requirement is a testament to the quality that is inherent within GCI's *DEER™* process, as well as the overall benefit for plastic to ceramic device conversions.

6. RECOMMENDATIONS (use only if a course of action is being suggested)

A listing of all MIL-STD tests to be performed with data tabulation is currently being generated for the final report draft.

7. REFERENCES (use if references are provided)

1. Kuldip Johal, Sven Lamprecht, and Hugh Roberts, "Electroless Nickel/Electroless Palladium/Immersion Gold Plating Process for gold and Aluminum-Wire Bonding Designed for High-Temperature Applications," Atotech Deutschland BmbH, Berlin, Germany Atotech USA, Inc., Rock Hill, SC, USA
2. R. Wayne Johnson, M. Palmer, M.J. Bozack and T. Isaac-Smith, "Thermosonic Gold Wire Bonding to Laminate Substrates with Palladium Surface Finishes," IEEE Transactions on Electronics Packaging Manufacturing 22 (1999) 7.
3. S. Qu, S. Athavale, A. Prabhu, A. Xu, L. Nguyen, A. Poddar, C.S. Lee, Y.C. How, and K.C. Ooi, "Over Pad Metallization for High-Temperature Interconnections," IEEE Xplore, June 2011
4. Avery Cashion, Grzegorz Cieslewski, "High-Temperature Component Evaluation of Commercial Flash Memory and Capacitors for Enhancement of Geothermal Tool Development," HiTEN Conference, July 2015.

8. TRADEMARKS

Die Extraction and Reassembly – *DER™*, Global Circuit Innovations (2017)

Die Extraction and Reassembly with Gold Ball Removal and ENEPIG Die Pad Plating – *DEER™*, Global Circuit Innovations (2018)

9. APPENDICES (use if supplemental results and discussions are provided)

Appendix I – MILSTD883 Tables

Appendix II – ADG859 Burn-In

Appendix III – XC4005XL Burn-In

Appendix IV – OPA820 Burn-In

Appendix V – ATSAMD21 Burn-In

Appendix VI – STN1NK60Z Burn-In

Appendix VII – Harsh Environments Extended Abstract Submission

Appendix VIII – SLB Plating Report

Appendix IX – Honeywell Auger Technical Report

Appendix X – Phase II BurnIn LifeTest Board Currents

Appendix XI – ADG859 and STN1NK60Z Board 1 11_11_2019

Appendix XII – NC7SB3157 Plastic181219

Appendix XIII – GC859Ceramic060519

Appendix XIV – GC4005Plastic181219

Appendix XV – GC4005BCeramic82819

Appendix XVI – OPA820Plastic181219

Appendix XVII – OPA820Ceramic060519

Appendix XVIII – AT91SAMPlastic181219

Appendix XIX – AT91SAMCeramic060519

Appendix XX – STN1NK60ZPlastic190125

Appendix XXI – STN1NK06ZCeramic031519

Appendix XXII – Phase 2 Bond Pull Data001

Appendix XXIII – Hermeticity Reports 246771-001 246771-002 246771-003

Appendix XXIV – IVA Reports 246797-001 246797-002 246797-003 246797-004 246797-005