Monthly Report for ECE FYP/FYT

Project Code:	ZW01a-23	Supervisor(s):	Prof. Wei Zhang
Project Title:	Hardware Acceleration of Data Processing		
Group Member(s):	1) Luk Pak Him 2) Chio Yat Hei 3)Shum Kwan Ho		
Reporting Period:	Report #1 ☒ Oct (Fall) Report #2 ☐ Nov (Fall) Report #3 ☐ Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report: • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress.	Completed work: nine 8-bit unsigned integer median filter design with three pipeline stages -including a three 8-bit unsigned integer combinational median filter design -verified correctness with unit testing on both components. Major difficulties: Considering moving to a systolic array-based design to reduce memory access overhang, still in planning stage. Planning on systolic array based median filter is undergoing in great progress. Group members are not all proficient in Verilog programming and HDL. Overall Progress: Slightly behind schedule, with a lot of design work and changes to the system design from a pure Von Neumann architecture to a systolic array architecture.		
Future Plan: • Write down the working plan for the next reporting period.	Implement and Verify correctness of the systolic array based median filter. Design a systolic array based Sobel filter design. Implement a systolic array fetcher for image.		
Group Representative's Signature:			

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