Monthly Report for ECE FYP/FYT

Project Code:	ZW01a-23	Supervisor(s):	Prof. Wei Zhang
Project Title:	Hardware Acceleration of Data Processing		
Group Member(s):	1) Luk Pak Him 2) Chio Yat Hei 3) Shum Kwan Ho		
Reporting Period:	Report #1 ☐ Oct (Fall) Report #2 ☒ Nov (Fall) Report #3 ☐ Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report: • List the work completed in this reporting period. • Identify the major difficulties encountered. • Comment on the overall progress.	Completed work: Median Filter - Finalized design of systolic median filter - 3-sort module: sorting 3 8-bit numbers with 2 pipeline stages - 9-median systolic: input 3 new numbers and compute the new median every clock cycle Sobel Filter - Finalized design of systolic Sobel filter - Sobel module: single module, scalable for Sobel filter - Verify correctness by placing 3 Sobel filter CU side by side Major difficulties: - Figuring out the memory access of FPGA boards - Group members are not all proficient in Verilog programming and HDL. Overall Progress: Slightly behind schedule, still haven't implemented the memory access part		
Future Plan: • Write down the working plan for the next reporting period.	1. Implement scalable RTL schematic with for loops 2. Implement memory access of BOE 3. Implement Image division hardware		
Group Representative's Signature:			

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