



Hardware Acceleration of Data Processing (ZW01a-23)

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Overview

Nowadays, High Performance Computing (HPC) has become more and more popular in the industry of technology, with the growth of a variety of novel technologies and algorithms such as image recognition, large language model, generative artificial intelligence, data mining, etc. This creates a huge demand for hardware accelerators to run these algorithms quickly and efficiently.

Aim

This project aims to implement hardware acceleration on image processing algorithms on FPGA chips, which consists of color filtering, noise reduction and edge detection, with various optimization methods such as pipelining and spatial dataflow architecture.

Objective

1. To design an image processing accelerating circuit which accelerates the algorithms for different filters.
2. To implement the design of the hardware on an FPGA chip.
3. To measure the performance of the FPGA hardware accelerator, as well as compare its performance against existing solutions.

Methodology

Spatial dataflow architecture

Our project utilizes spatial dataflow architecture for our main system, where data is being passed from one module to another directly without the need for frequent access of data memory, as opposed to traditional Von Neumann architecture. This provides a high-performance and efficient way of processing images in our system, where each row of the image is fetched into the main processing modules in each clock cycle for concurrent processing.

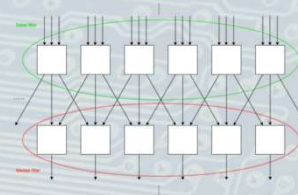


Fig. 1 Spatial dataflow architecture of our system

Noise Reduction (Median Filter)

We applied median filter for noise reduction in our system, where the output pixel is the median of the current and surrounding nine pixels. We applied an algorithm developed by Bevara and Sanki, which allows concurrent sorting of three numbers in groups to compute the median. The filter is scalable by scaling the number of computational units through the top module.

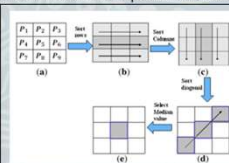


Fig. 2 Algorithm by Bevara and Sanki

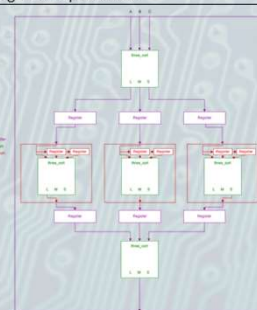


Fig. 3 Schematic of median filter computational unit

Edge Detection (Sobel Filter)

The Sobel filter module is designed to contain multiple computational units that can be scaled to allow concurrent processing images of various sizes, where the number of computational units are flexible. The modularization design of the system also allows reusing of calculations by sharing and exchanging the weighted sums between different sub-modules to achieve high-performance and efficient processing of edge detection.

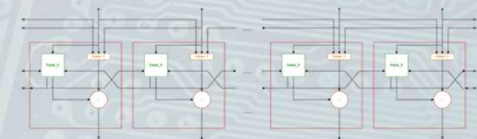


Fig. 4 Illustration on flexibility of filter

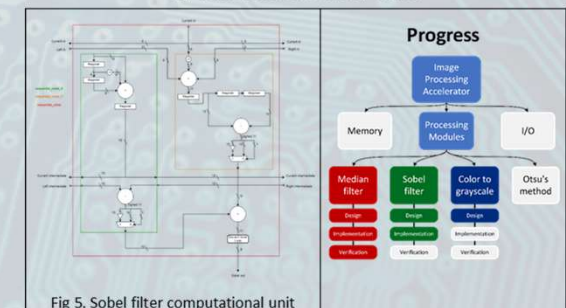


Fig. 5 Sobel filter computational unit

Conclusion

We hope that this project would provide a high-performance, efficient and scalable way to accelerate image processing through hardware acceleration, which would help the ever-changing industry of high-performance computing and machine learning fields.