
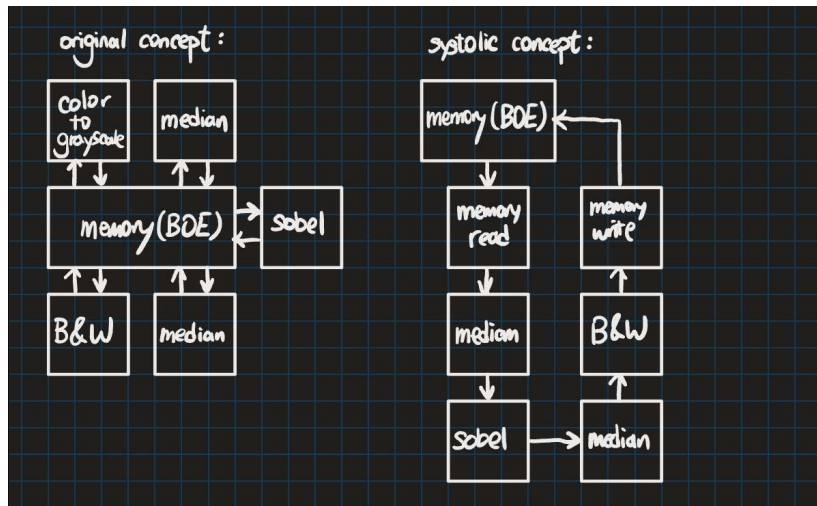


Monthly Report for ECE FYP/FYT

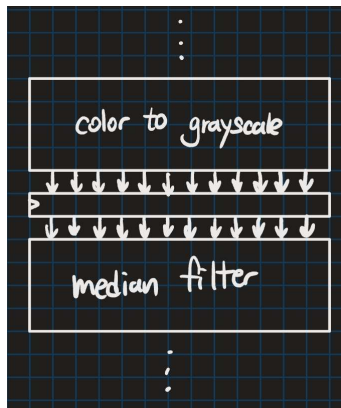
Project Code:	ZW01a-23	Supervisor(s):	Prof. Wei Zhang
Project Title:	Hardware Acceleration of Data Processing		
Group Member(s):	1) Luk Pak Him 2) Chio Yat Hei 3) Shum Kwan Ho		
Reporting Period:	Report #1 <input type="checkbox"/> Oct (Fall) Report #2 <input checked="" type="checkbox"/> Nov (Fall) Report #3 <input type="checkbox"/> Feb (Spring) (please attach Reports #1-2 to the Progress Report to be submitted in Jan) (please attach Reports #3 to the Final Report to be submitted in Apr)		
Progress Report:	<p>Completed work:</p> <p>Median Filter</p> <ul style="list-style-type: none"> - Finalized design of systolic median filter (Issac) - 3-sort module: sorting 3 8-bit numbers with 2 pipeline stages (Gordon) - 9-median systolic: input 3 new numbers and compute the new median every clock cycle (Gordon) <p>Sobel Filter</p> <ul style="list-style-type: none"> - Finalized design of systolic Sobel filter (Issac) - Sobel module: single module, scalable for Sobel filter (Issac and Haven) - Verify correctness by placing 3 Sobel filter CU side by side (Haven) <p>Major difficulties:</p> <ul style="list-style-type: none"> - Figuring out the memory access of FPGA boards - Group members are not all proficient in Verilog programming and HDL. <p>Overall Progress: Slightly behind schedule, still haven't implemented the memory access part</p>		
Future Plan:	<ul style="list-style-type: none"> 1. Implement scalable RTL schematic with for loops 2. Implement memory access of BOE 3. Implement Image division hardware 		
Group Representative's Signature:			

Appendix: Systolic Based Design

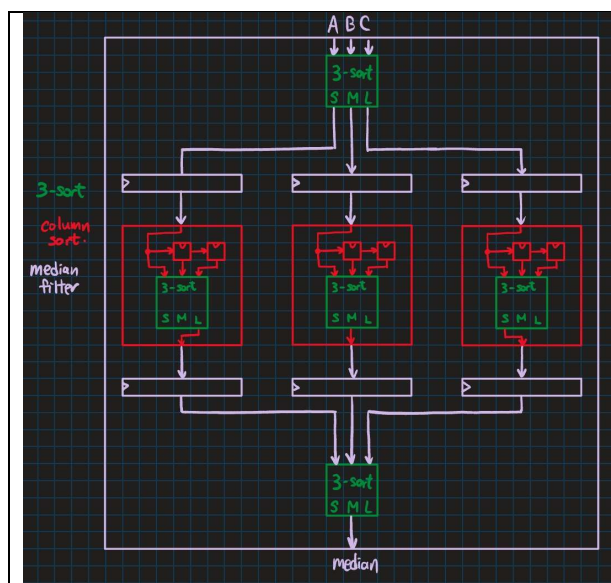


An image of width W and height H can be partitioned into multiple arrays of same height, but a smaller width to be fitted in the circuit.

Each clock cycle, a row of pixels is being loaded into the first step of the data processor, and the computational results would be stored intermediately in registers, waiting for the next task.



Design of module nine_median_systolic, a 9 8-bit median filter with sequential input and internal register

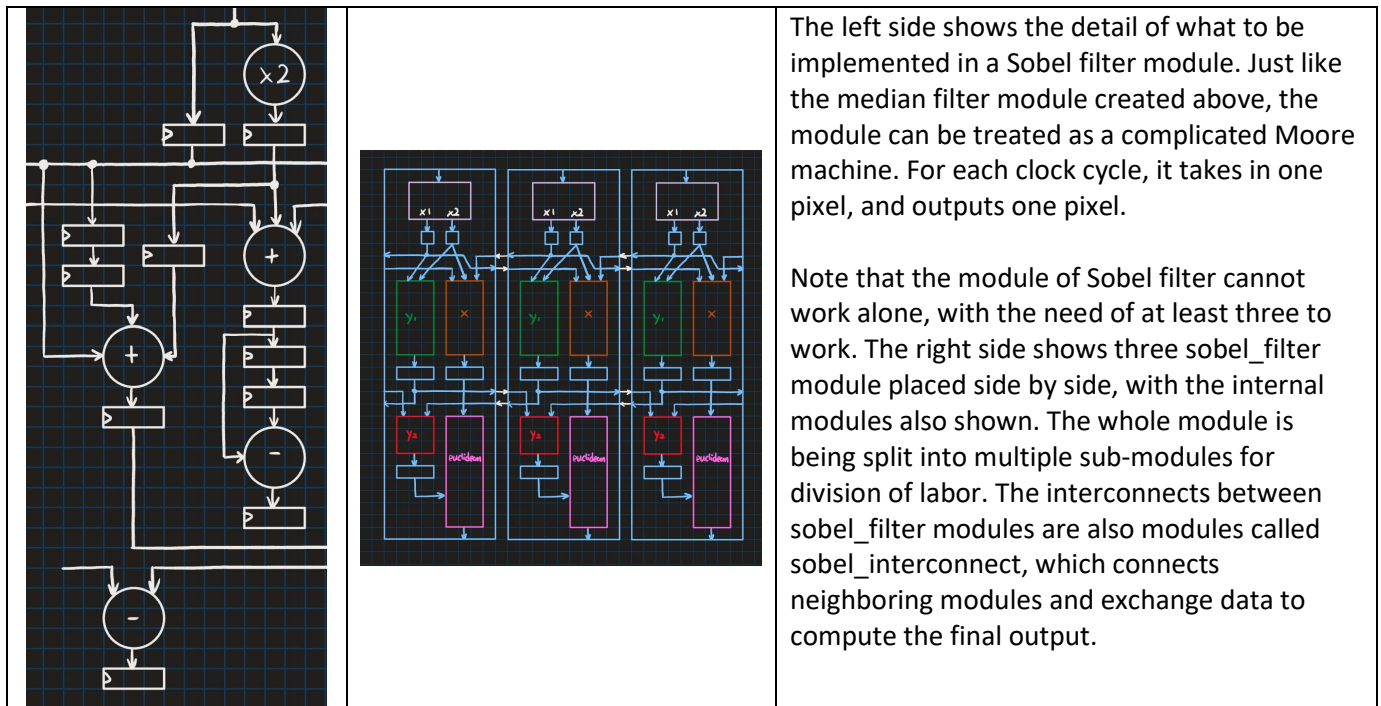


The design of a median filter module, as defined as a computational unit. Each CU handles one pixel output of median filter. The Filter takes in three new numbers in the same row for every clock cycle, and computes the output median using the values from the previous two clock cycles, as well as this cycle's value. It can be treated as a simple mealy machine.

three_sort is the module being implemented from the last progress report, with a major change in adding a additional pipeline stage in the middle between the comparators and MUXs.

The computational stage can simply be scaled up by adding more modules to run in parallel. Additional module would be made to route data into the median filter from previous stage.

Design of module sobel_filter



The color to grayscale filter is obviously easier to implement, as it is a point operation. We are still designing how the black-and-white filter is to be implemented, as it is a global operation, where data might need to store back to the memory for further processing.