cJTAG Adapter for RISC-V DTM

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1. Introduction

The draft RISC-V debug specification includes an IEEE 1149.1-compatible JTAG debug and control module called the Debug Transport Module (DTM). The JTAG spec includes a minimum of 4 external signals. In some applications, it is desirable to minimize the number of external signals allocated to debug. In the IEEE 1149.7 update to the JTAG spec, a new configuration consisting of only 2 external signals is defined. The adapter described here is a standalone converter from the 2-wire 1149.7 protocol (also called cJTAG) to 4-wire 1149.1.

The cJTAG Adapter will be an implementation option when building in federation.

Many debug probes can support both legacy JTAG and the new cJTAG. When connected to cJTAG, the TDI and TDO signals defined in the connector are not used and the TMS signal becomes bidirectional. The first probe to be tested will be the Olimex ARM-USB-TINY-H connected to Olimex ARM-JTAG-SWD adapter. Initial testing will be in the Arty FPGA board.

The 1149.7 specification is complex and much more flexible than is needed in this application. The IP implemented here is a subset of 1149.7.

2. Concept

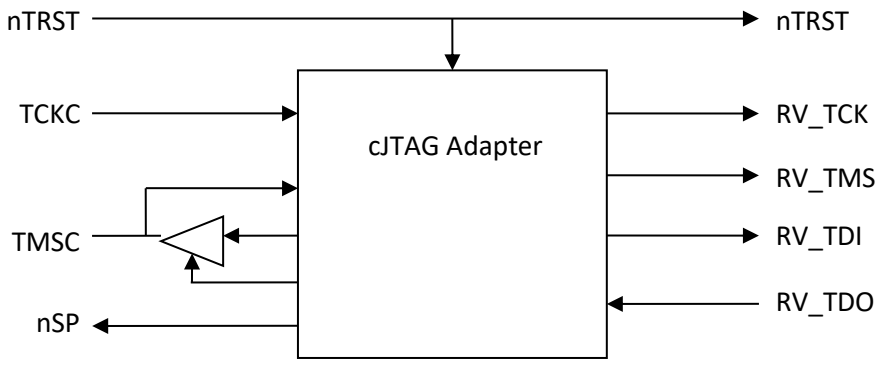

Figure 1. cJTAG System Block Diagram

The cJTAG Adapter provides a probe interface consisting of two signals, TCKC and TMSC, and a device interface consisting of four signals, RV_TCK, RV_TMS, RV_TDI, and RV_TDO. TMSC is a bidirectional signal, so the Adapter separates the signal into three ports – TMSC_IN, TMSC_OUT, and TMSC_EN – and requires the system designer

to provide the appropriate attachment to a bidirectional device pin. TCKC is sourced from the probe (called DTS in the IEEE spec). TMSC is bidirectional and carries control information to the Adapter and data in both directions.

3. Protocol – Online/Offline

The Adapter can be either online or offline. When the Adapter is offline, activity on the TCKC and TMSC signals does not affect the 1149.1 port. When online, TCKC and TMSC indirectly drive the 1149.1 port to perform JTAG scans. There is a protocol defined in 1149.7 to switch between the online and offline states.

When the Adapter is reset, it is in the offline state. A reset can be performed using the optional nTRST signal or through a sequential protocol on TCKC/TMSC. Switching online or offline and performing reset are accomplished using the Escape sequences described in the IEEE 1149.7 specification. While TCKC is held high, TMSC is toggled a certain number of times. The Adapter keeps a count of the number of edges observed on TMSC and executes the corresponding command at the next TCKC rising edge.

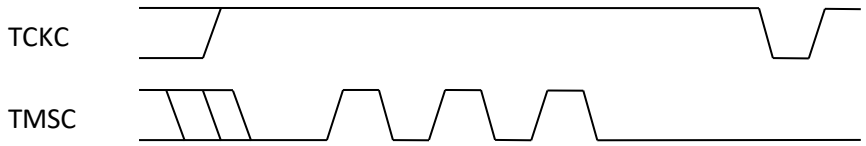

Figure 2. cJTAG Escape Sequence

As described in the IEEE spec, there may be a TMSC edge coincident with the last rising edge of TCKC before the Escape sequence begins and that edge may or may not be detected by the Escape logic, depending on signal skew. A single pulse that would normally be two edges could therefore be counted as three edges. Escape detection logic takes this possibility into account. The Adapter interprets TMSC edges in an Escape as follows.

2 or 3 edges	End of transfer
4 or 5 edges	Deselect (switch to offline state)
6 or 7 edges	Select (switch to online state)
8 or more edges	Reset

4. Protocol – Online Activation Code

Following the Online Escape sequence, the probe transmits an Online Activation Code (OAC), Extension Code (EC), and Check Packet (CP), 12 TCKC pulses in all. The Adapter observes the control data in these codes and activates only if the requested protocol variations are supported by the Adapter. In this implementation, only one form of activation code is supported; any sequence of control bits other than this form will return the Adapter to the offline state.

Referring to the IEEE standard, the OAC required is 1100, transmitted LSB first, which connotes TAP.7 star-2 scan topology. The EC must be 1000 indicating short form and use of the Run-Test/Idle TAP state when switching online or offline. The CP is 0000. At the rising edge of TCKC in the last bit of the CP, the Adapter is activated. From that point forward, activity on TCKC/TMSC is interpreted as Oscan1 format, described in the IEEE standard, until the Adapter is reset or taken offline.

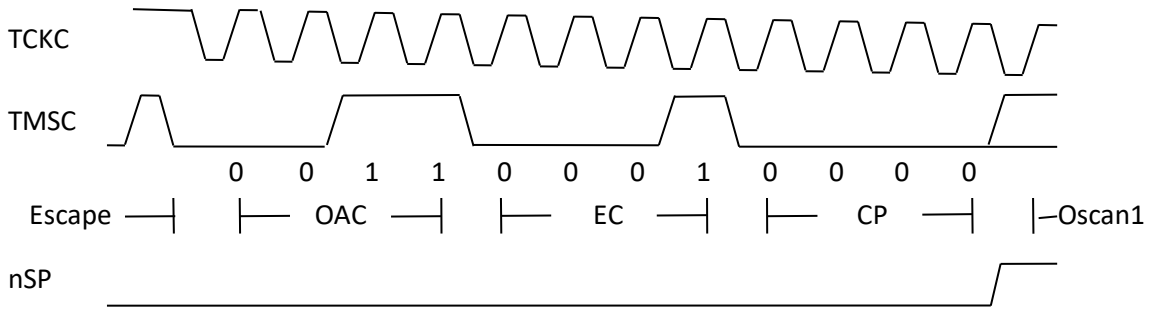

Figure 3. Advanced Protocol Activation Sequence

5. Protocol – Oscan1

Once activated, the Adapter supports only Oscan1 format. In Oscan1, the TMS, TDI, and TDO signals to the device are multiplexed onto the TMSC signal to and from the probe. Three TCKC pulses are required to perform one bit of JTAG scan. Per the IEEE standard, the first bit of each 3-bit group (called a Scan Packet or SP) is the *inverse* of the TDI signal, denoted nTDI. This is followed by TMS and finally TDO. The probe drives TMSC during the first two bit periods and the device drives TMSC during the third bit period. To avoid a drive conflict in Advanced Protocol (Oscan1), TMSC is driven by its source only while TCKC is low and relies on a system-level keeper circuit to maintain a valid logic level while TCKC is high.

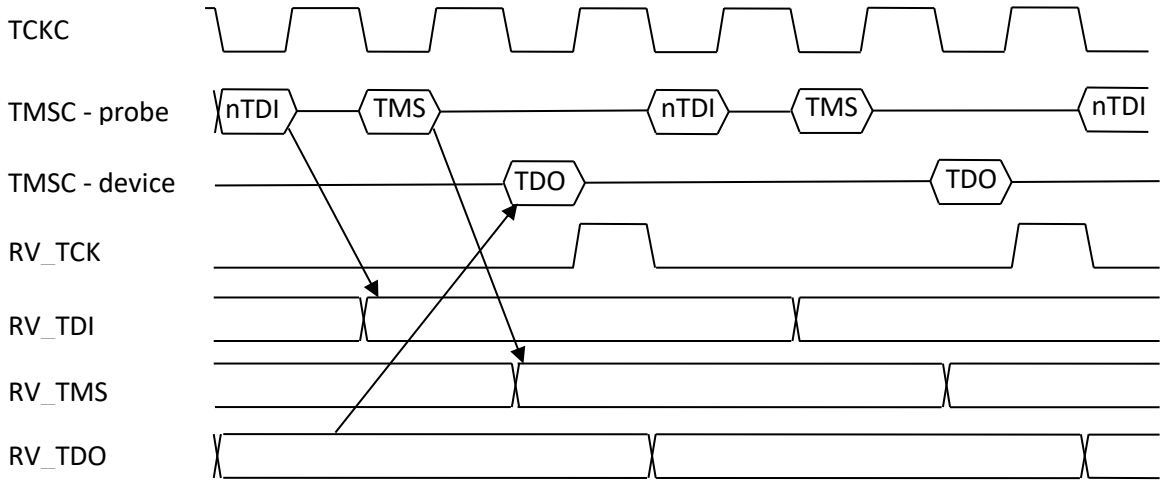

Figure 4. Advanced Protocol Scan Timing

6. Chip Pin Requirements

The IEEE specification requires the system to implement inputs with the following characteristics. To be strictly compliant with the specification, this is required of all system designs. To support this, the Adapter provides an output signal nSP which is low when the adapter is in Standard Protocol and high when in Advanced Protocol.

External signal	Power off	Power on, nSP=0	Power on, nSP=1
TCKC	Undefined	Pullup	Pullup
TMSC	Undefined	Pullup	Weak Keeper

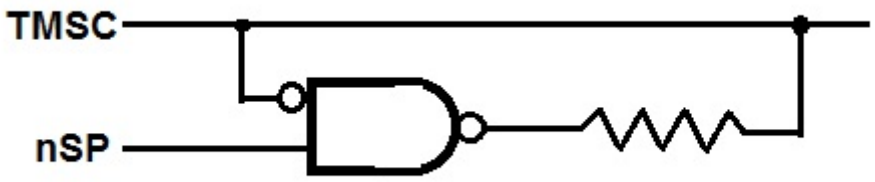

Figure 5. Weak Keeper and Pullup termination for TMSC

Most, if not all, probes will support a system designed with only the Weak Keeper termination on TMSC even though this is technically a violation of the 1149.7 spec. In Standard Protocol prior to activation, the probe will generally drive TMSC continuously and will not depend on a system-level pullup to maintain a valid logic state. When driven continuously, the TMSC pullup or keeper termination has no effect.

Figure 6. Weak Keeper termination for TMSC

Care should be taken to minimize the load on TCKC and TMSC since many components may be controlled from a single driver. Since these are both edge-triggered signals, care must be taken in system implementation to avoid reflections and other signal degradation which could cause mis-operation. In large designs with more than one load, pullup and keeper circuitry may need to be implemented at board-level rather than chip-level.

7. References

IEEE Std 1149.7™-2009, IEEE Computer Society, New York NY, 2010