Shariq Ahmad

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Examination	University	Institute	CPI/%
Post Graduation	IIT Bombay	IIT Bombay	9.7
Graduation	WBUT	MCKV Institute of Engineering	8.93
Intermediate/+2	ISC	St. Augustine Day School	89.75
Intermediate	ICSE	St. Augustine Day School	91.4

AREAS OF INTEREST

Machine Learning, Deep Learning, Computer Vision, Digital VLSI Design.

SCHOLASTIC ACHIEVEMENTS

- Ranked $\mathbf{2}^{nd}$ in **Microelectronics and VLSI** specialization of Electrical Engineering at **IIT Bombay**.
- Ranked $\mathbf{1}^{st}$ in second and third semester of B.Tech among 360 candidates in all department of MCKVIE.
- Secured **99.6** percentile in **GATE** (Electronics and Communication) among 2,16,367 candidates.
- Ranked $\mathbf{8}^{th}$ in the competition held by **PadhAI(IIT Madras)** at Kaggle to classify the text and non-text among 350 people.
- Ranked $\mathbf{1}^{st}$ in the the competition conducted by the **Weight and Bias** at **Qualcomm** among 400 employees to predict the 6^{th} video frame from the given 5 video frames.
- Got a scholarship for the course **Secure and Private AI** at Udacity from **Facebook**.
- Awarded with a **Qualstar** for the qlink4x I.P and S.O.C verification

WORK EXPERIENCE

- **RTL Verification engineer at Qualcomm Corporate R&D** [2018-2019]
  - Verification of V70 DSP processor core (R, I and J type instruction) for IOT applications.
  - As **R&D** engineer, verified the functionality of the **qlink4x I.P** for the next generation **5G** modem chip.
  - Performed verification in **System Verilog** using the concepts of **OOPS** like **Inheritance**, **Polymorphism** and **Encapsulation**.
  - Coverage analysis (Branch, FSM coverage etc.) of the **qlink4x I.P** was done in **Verdi**.
  - Established the functionality of all the registers by writing various test cases like POR, Alias, bit-bash.
  - Checked the functionality of various modes in the design like Fixed pattern, PRBS31 and PRBS11.
  - Established the driver, monitor, sequencer, adapter, sequences along with the test to verify the RTL.
  - Performed the connectivity checks at the interface of all the I/Os with the RW, RO registers.
  - Ran the regression containing all the test case for entire qlink4x I.P.

KEY ACADEMIC PROJECTS

- **Classify the Dog breed using Convolution Neural Network** [Udacity:Deep Learning]
  - Designed a CNN in order to classify the dog breed using **Pytorch**.
  - Trained on model on architecture like **Resnet** and **VGG19** in order to increase the model accuracy.
  - Predicted the dog breed on the model with an accuracy of 86% using transfer learning
- **Prediction of 6^{th} Video frame given 5 consecutive video frames** [Weight and Bias]
  - Analysed and normalized all the images and created a model consisting of Convolution layers and LSTM.
  - Used Dropout, Gaussian in order to prevent overfitting on the training data.
- **Generation of Human Faces using Generative Adversarial Networks** [Udacity:Deep Learning]
  - Created a discriminator/generator with strided convolution/fraction strided convolution respectively.
  - Used **Leaky ReLU**, **ReLU** as the acitvation function and **batch normalization**.
  - Generated the fake images that looked like real images.

- **Finding a donor for charity using ML algorithm** [Udacity:Machine Learning]
  - Analysed the datasets and pre-processed(scaling,clipping,encoding) it using **Pandas** and **Numpy**.
  - Trained the dataset on various alogorithm like **Logistic Regression**, **SVM** and **Random Forest**.
  - Evaluated the performance using cross-validation set and predicted it using Random Forest which has maximum accuracy of 86%.
- **Text -Non Text Classification using Logistic Regression, Perceptron** [PadhAI]
  Guide: *Prof. Mitesh Kharpa, Department of Computer Science, IIT Madras*
  - Preprocessed the image for text -non text classification using **OpenCV**.
  - Implemented the forward propagation, backpropagation and update of weights from scractch using **Numpy**.
  - Performoned a grid-search in order to tune the hyperparameters like **Learning rate** and **no of Epoch**.
- **Design of Sequential and Combinational ATPG in Python** [VLSI Testing]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*
  - Designed a Combinational ATPG using PODEM and Sequential ATPG using Time-Frame Expansion
  - The Sequential ATPG was benchmarked against s1196.v detecting 99.6 % of the faults.
  - The Combinational ATPG was benchmarked against c17.v detecting 100 % of the faults.
- **Design of 16-bit 6 Stage Pipelined Processor ISA** [Processor Design]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*
  - Designed a RISC Processor using 8 general purpose register for 3 instruction format (R, I and J) and total of 15 instructions in VHDL.
  - Implemented hazard mitigation technique, Data Forwarding in order to improve the CPI.
  - Verification of the design in FPGA Cyclone IVE using Altera Quartus.

MTECH PROJECT

- **Architectural Design and Implementation of Universal Serial Bus and Serial Peripheral Interface** [2017-2018]
  Guide: *Prof. D.K.Sharma, Department of Electrical Engineering, IIT Bombay*
  - Designed a SPI master and SPI GPIO slave device in VHDL and verified the design on the FPGA **Zedboard** using **Xilinx SDK**
  - Coverage analysis (Branch, FSM coverage etc.) of the entire SPI module was done in **Questa SIM**
  - Interfaced the SPI master with the ZYNQ-7000 processor and the DAC MCP4921 with the SPI master.
  - Designed a USB Transceiver Macrocell Interface for Full speed (FS), High speed (HS) mode.
  - Interfacing the USB Transceiver and SIE with the ZYNQ-7000 processor.

TECHNICAL SKILLS

- **Programming Languages:** Python, C, BASH, 8085/51(*Assembly*), MATLAB
- **Python Libraries:** Keras, Tensorflow, Pytorch, Numpy, Pandas, Scikit-learn, Matplotlib.

RELEVANT COURSES

o Deep Learning	o Processor Design	o VLSI Design	o VLSI Testing
o Machine Learning	o VLSI CAD	o VLSI Design Lab	o System Design

POSITIONS OF RESPONSIBILITY

- **Research Assistant, Wadhwani Electronics Laboratory, IIT Bombay** [2016-2018]
  - Teaching Assistant for Electronic Devices, Analog Circuit, Microprocessor and Digital Circuit lab.
  - **Mentored** and textbfevaluated over 40 undergraduate students in these lab courses in last two years.
- **Student Companion, ISCP, IIT Bombay** [July 2016]
  - Mentored a group of five 1st year P.G students as a member of Institute Student Companion Programme which addresses the need of over 1200 students.

EXTRA CURRICULAR ACTIVITIES

- Participated in the intra-college technical exhibition of **Technotica** 2012 held in MCKVIE.
- Represented MCKVIE in Pirate bay event during the tech fest, Kshitij at **IIT Kharagpur** in 2011.
- Participated in **Rover Ranger** event during the tech fest, **Pragati** held at MCKVIE in 2011.
- **Hobbies:** Trekking, watching movies.