Shariq Ahmad

ahmadshariq12@gmail.com
+919831619350

Examination	University	Institute	CPI/%
Post Graduation	IIT Bombay	IIT Bombay	9.7
Graduation	WBUT	MCKV Institute of Engineering	8.93
Intermediate/+2	ISC	St. Augustine Day School	89.75
Intermediate	ICSE	St. Augustine Day School	91.4

AREAS OF INTEREST

Digital VLSI Design, Processor Design, Analog VLSI Design

SCHOLASTIC ACHIEVEMENTS

- Ranked $\mathbf{2}^{nd}$ in **Microelectronics and VLSI** specialization of Electrical Engineering at **IIT Bombay**.
- Ranked $\mathbf{1}^{st}$ in second and third semester of B.Tech among 360 candidates in all department of MCKVIE.
- Secured **99.6** percentile in **GATE** (Electronics and Communication) among 2,16,367 candidates.

WORK EXPERIENCE

- **RTL Verification engineer at Qualcomm Corporate R&D** [2018-2019]
  - As **R&D** engineer, verified the functionality of the **qlink4x I.P** for the next generation **5G** modem chip.
  - Performed verification in **System Verilog** using the concepts of **OOPS** like **Inheritance**, **Polymorphism** and **Encapsulation**.
  - Coverage analysis (Branch, FSM coverage etc.) of the **qlink4x I.P** was done in **Verdi**.
  - Established the functionality of all the registers by writing various test cases like POR, Alias, bit-bash.
  - Checked the functionality of various modes in the design like Fixed pattern, PRBS31 and PRBS11.
  - Established the driver, monitor, sequencer, adapter, sequences along with the test to verify the RTL.
  - Performed the connectivity checks at the interface of all the I/Os with the RW, RO registers.
  - Ran the regression containing all the test case for entire qlink4x I.P.

MTECH PROJECT

- **Architectural Design and Implementation of Universal Serial Bus and Serial Peripheral Interface** [2017-2018]
  Guide: *Prof. D.K.Sharma, Department of Electrical Engineering, IIT Bombay*
  - Designed a SPI master and SPI GPIO slave device in VHDL and verified the design on the FPGA **Zedboard** using **Xilinx SDK**
  - Coverage analysis (Branch, FSM coverage etc.) of the entire SPI module was done in **Questa SIM**
  - Interfaced the SPI master with the ZYNQ-7000 processor and the DAC MCP4921 with the SPI master.
  - Designed a USB Transceiver Macrocell Interface for Full speed (FS), High speed (HS) mode.
  - Post-synthesis simulation and verification of the FS and HS mode in USB Transceiver using **Vivado**.
  - Interfacing the USB Transceiver and SIE with the ZYNQ-7000 processor.

KEY ACADEMIC PROJECTS

- **Group Lift Controller Design** [VLSI Design Lab]
  Guide: *Prof Virendra Singh, Department of Electrical Engineering, IIT Bombay*
  - Implemented a lift controller that serves a 6th storied building consisting of hall call and car call button.
  - Implemented a group lift controller consisting of 3 lifts with an object of minimizing avg. waiting time.
- **Design of Router for 4x4 NOC** [VLSI Design Lab]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*
  - Designed a Router for NOC, using Direction Ordered Routing (X-Y routing) to direct a flit from the source to the destination in Verilog.

– A priority logic was used to resolve the deadlock of the transmission of a packet.

- **Design of 2-way Fetch Superscalar Processor ISA** [Processor Design]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*

– Implemented a **Distributed Reservation Station** (RS), **Re-order Buffer** (ROB), **Rename Register File** (RRF), **Architecture Register File** (ARF), **Load-Store** queue in VHDL.

– Anti-dependencies and False data dependencies were handled using Rename Register File.

- **Design of 16-bit 6 Stage Pipelined Processor ISA** [Processor Design]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*

– Designed a RISC Processor using 8 general purpose register for 3 instruction format (R, I and J) and total of 15 instructions in VHDL.

– Implemented hazard mitigation technique, Data Forwarding in order to improve the CPI.

– Verification of the design in FPGA Cyclone IVE using Altera Quartus.

- **Design of Digital Circuits in VHDL** [VLSI Design Lab,]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*

– Designed a Booth Multiplier for 2-signed 8-bit numbers using structural modeling in VHDL.

– Designed a GCD calculator which computes the GCD of 2-signed numbers using behavioral modeling.

– Designed a Run length Encoder to compress the data and reduce redundancy.

- **Design of Sequential and Combinational ATPG in Python** [VLSI Testing]
  Guide: *Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*

– Designed a Combinational ATPG using PODEM and Sequential ATPG using Time-Frame Expansion

– The Sequential ATPG was benchmarked against s1196.v detecting 99.6 % of the faults.

– The Combinational ATPG was benchmarked against c17.v detecting 100 % of the faults.

- **Delay Optimization of Multi-Stage Digital Logic Circuits using Ngspice** [VLSI Design]
  Guide: *Prof D.K.Sharma, Department of Electrical Engineering, IIT Bombay*

– Designed a minimum sized inverter with equal rise and fall times.

– Evaluated logical effort of multiple NAND and NOR gate using delay versus fanout plot.

TECHNICAL SKILLS

- **Tools:** Xilinx Vivado and SDK, Altera Qaurtus, GHDL, Ngspice, ModelSim.
- **Programming Languages:** VHDL, Verilog, Pytohn, C, BASH, 8085/51(*Assembly*), MATLAB
- **Hardware Platforms:** Zedboard Xilinx ZYNQ 7000, Altera DE0-Nano Cyclone IVE, Krypton MAX V.

RELEVANT COURSES

o Processor Design	o VLSI Design	o CMOS Analog VLSI Design	o VLSI Testing
o VLSI CAD	o VLSI Design Lab	o Mixed Signal VLSI Design	o System Design

POSITIONS OF RESPONSIBILITY

- **Research Assistant, Wadhwani Electronics Laboratory, IIT Bombay** [2016-2018]

– Teaching Assistant for Electronic Devices, Analog Circuit, Microprocessor and Digital Circuit lab.

– **Mentored** and textbfevaluated over 40 undergraduate students in these lab courses in last two years.

- **Student Companion, ISCP, IIT Bombay** [July 2016]

– Mentored a group of five 1st year P.G students as a member of Institute Student Companion Programme which addresses the need of over 1200 students.

EXTRA CURRICULAR ACTIVITIES

- Participated in the intra-college technical exhibition of **Technotica** 2012 held in MCKVIE.
- Represented MCKVIE in Pirate bay event during the tech fest, Kshitij at **IIT Kharagpur** in 2011.
- Participated in **Rover Ranger** event during the tech fest, **Pragati** held at MCKVIE in 2011.
- **Hobbies:** Trekking, watching movies.