quiz_3_ans

2023年6月7日 星期三 下午6:39

quiz_3_ans

組合語言與計算機組織

Assembly Language and Computer Organization

Quiz 3

資訊工程學系

Computer Science and Engineering

Time: 15:10~17:00 Date: 05/18/2023

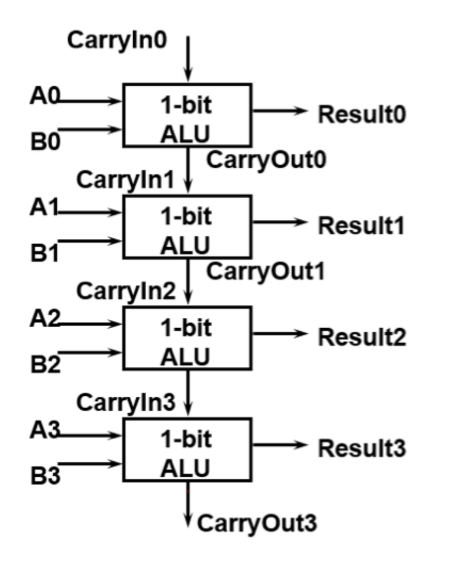
Note 1: This is a close-book quiz. No electronic devices can be used. Each rule violation will result in deduction of 10 points.
Note 2: You must present your answers in order, that is, the answer to problem 1 should be presented before that for problem 2. You must write neatly to make your answer readable. You had better print the answers.
Note 3: Students from International Bachelor Program in Informatics should give answers only in English. The other students can give answers in Chinese unless indicated otherwise.

1. What does the following code do? Please explain the operation of each instruction executed in detail. (10%)

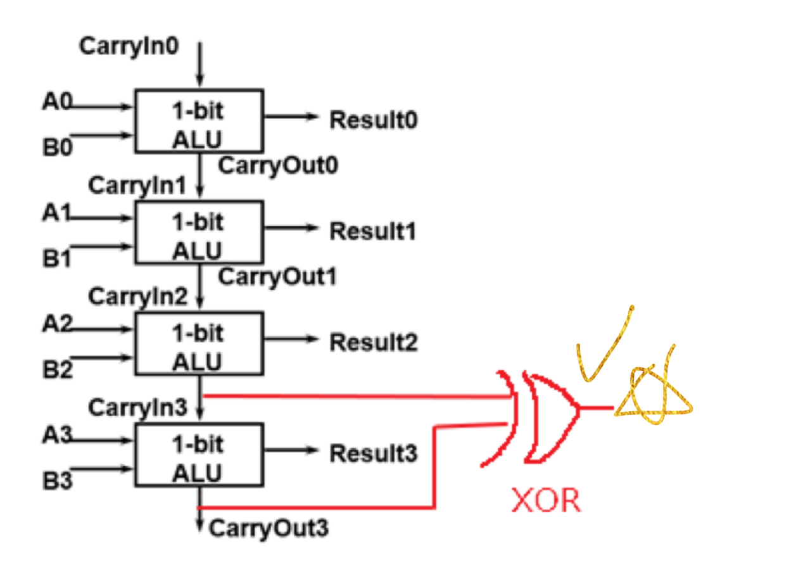
```
start:lr.w x10, (x20)
      sc.w x11, x23, (x20)
      bne  x11, x0, start
      addi x23, x0, 0
```

ANS: ***Atomically*** *move content of x23 and the content stored in the memory address specified in x20. Then, the content of x23 is set to zero*

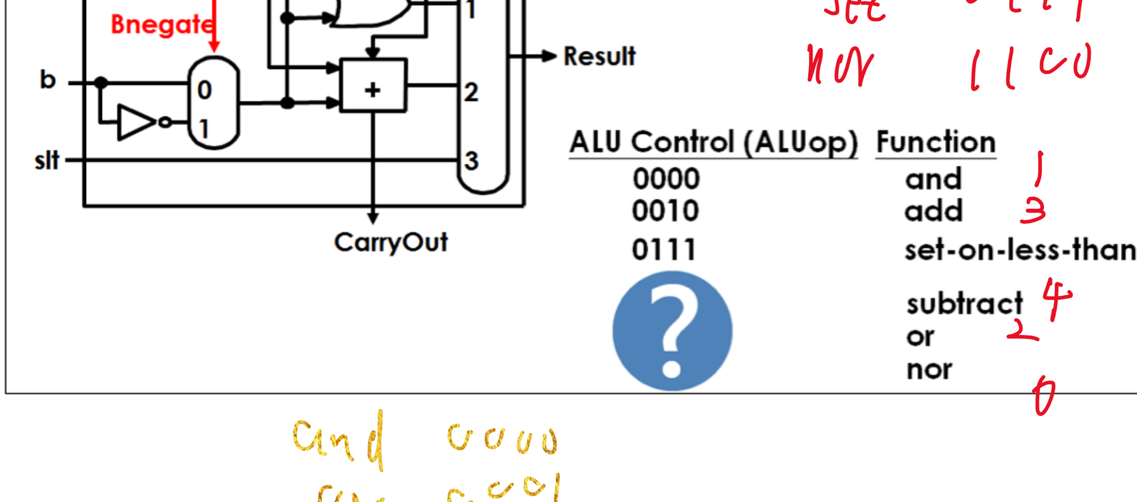
2. Please add the appropriate circuit in the figure below to detect **overflow**. (10%)



ANS



3.
(1) Please write the ALUop of Function **subtract, or, nor** in the figure below. (10%)
(2) Briefly explain how to save hardware to design 2's complement subtraction function. (10%)

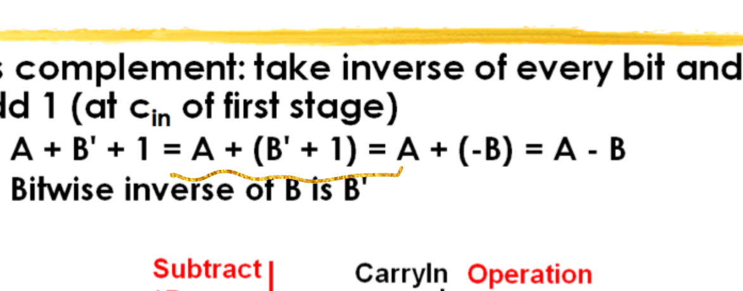


ANS:

substract	0110
or	0001
nor	1100

How about Subtraction?

- 2's complement: take inverse of every bit and add 1 (at c_{in} of first stage)
  - A + B' + 1 = A + (B' + 1) = A + (-B) = A - B
  - Bitwise inverse of B is B'



4. Why do the ripple carry adders perform additions in a sequential manner? Carry-lookahead adder is one of the fast-carry schemes to improve the adder performance over ripple carry adders. What is the principle of these fast-carry schemes? Briefly explain. (10%)

(1) ripple carry adder：是由多個 F.A.（全加器）組成，全加器是 3 bit（被加數、加數、前一級進位）相加而產生和與進位輸出，每一個全加器必須等前一個全加器的進位輸出，因此進位從最右邊的全加器往左邊的全加器一個一個傳遞，因此漣波進位加法器僅能循序執行。
(2) carry lookahead adder 是將 ripple carry adder 的進位傳遞延遲（$c_5 \leftarrow c_4 \leftarrow c_3 \leftarrow c_2 \leftarrow c_1$）改成所有進位（$c_5, c_4, c_3, c_2$）均與 c_1 與 a_i, b_i 所有輸入有關，即利用進位傳遞 $P_i = a_i + b_i$，進位產生 $g_i = a_i \cdot b_i$ 與 c_1 來組成 c_5, c_4, c_3, c_2，使得 ripple carry adder 的 8 Gate delay (AND 與 OR 二層 logic 組成)進位延遲減少成 carry lookahead adder 的 2 gate delay（他是 AND 與 OR 二層 logic 組成）進位延遲，因此 carry lookahead adder 執行速度較快。

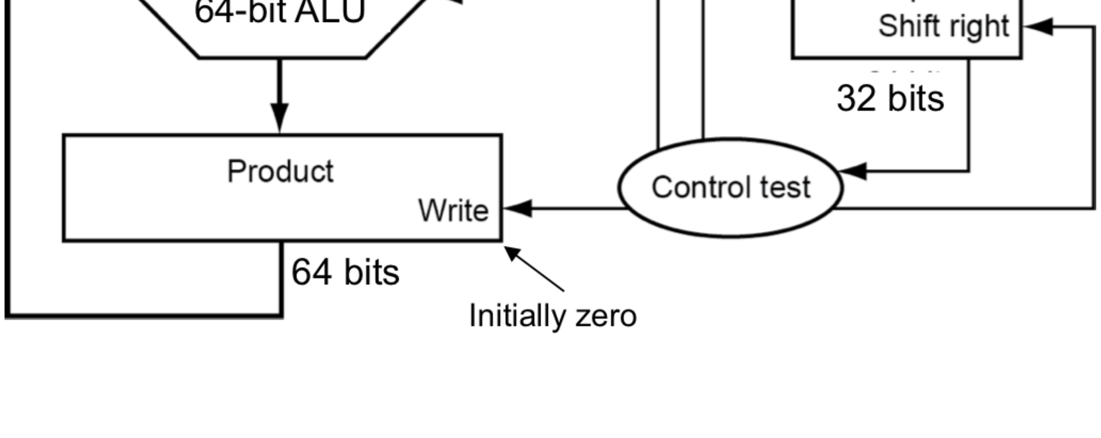
5. Modify the following code to avoid the syntax of 0x1 and use the "**rem**" instruction. (5%)

```
andi t0, s0, 0x1
li t1, 0x1
beq t0, t1, odd
bne t0, t1, even
```

```
#-----------------
#andi t0, s0, 0x1        # t0 -> N & 0x1
#li t1, 0x1              # t1 -> 0x1
#-----------------
li t2,2
rem t0,s0,t2
li t1, 1                 # t1 -> 0x1
#-----------------

beq t0, t1, odd                  # is odd
bne t0, t1, even         # is odd
```

6. Below is the hardware that implements a 32-bit multiplier. Describe the algorithm implemented by this piece of hardware. The algorithm should consist of only five steps. Present each step clearly. (10%)



Ans:
Step 1: Test whether the LSB of Multiplier is 1.
Step 2. If yes, add the multiplicand to the product and place the result in the Product register.
Step 3: Shift left the Multiplicand register by 1 bit.
Step 4: Shift right the Multiplier register by 1 bit.
Step 5: Check whether the above tasks have been done 32 times. If yes, stop. Otherwise, repeat Step 1~4.
You can also combine Step 1 and Step 2 into one step. Then, the answer has four steps. This is fine.

7. Are the following statements true or false? If it is true, why? If it is false, use examples to explain it. Just as a Shift Left Logical instruction can replace an integer multiply by a power of 2, a Shift Right Logical is the same as an integer division by a power of 2. (10%)

解 False，若整數是以無號數表示則左移 nbit 即乘 2^n，而右移 nbit 是除以 2^n，但整數是以 2 補數表示則必須是算術左移 nbit 才是乘 2^n 且算術右移 nbit 才是除 2^n。

Ans:

8. Given x=$(0011)_2$ and y=$(1100)_2$ in 2's complement notstion, compute step by step the product p=x*y with **Booth algorithm**. (20%)

				0	0	1	1
			x	1	1	0	0

Ans:

				0	0	1	1
			x	1	1	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	
1	1	1	1	0	1		
0	0	0	0	0			
1	1	1	1	0	1	0	0

9. (a) If the propagation delay time of S is **30ns** and that of C is **20ns** in an FA. What is the total propagation delay of a 4-bit Ripple Carry Adder (7483)? (5%)
(b) If the propagation delay time of S is **10ns** and that of C is **20ns** in an FA. What is the total propagation delay of a 32-bit Ripple Carry Adder? (5%)

Ans: (a) 20*(4-1)+max(20,30) = 60+30 = 90
(b) 20*(32-1)+max(20,10) = 620+20=640