

Bank Number VREF Pin Name/Function Optional Function(s) Configuration Function Dedicated Tx/Rx Channel Emulated LVDS Output Channel IO Performance E144 (2) VREFB1N0 IFFIO RX L1n DIFFOUT\_L1n Low\_Speed IFFIO RX L1p DIFFOLIT I 1n Low\_Speed DIFFOUT L3n VREFB1N0 DIFFIO RX L3n Low Speed REFB1N0 IFFIO RX L3p Low Speed Low\_Speed DIFFOUT L5p 1A VRFFB1N0 DIFFIO RX L5p Low Speed /REFB1N0 DIFFIO RX L7n Low Speed IFFIO\_RX\_L7p DIFFOUT\_L7p JTAGEN TMS 15 DIFFIO RX L11n DIFFOUT L11n /REFB1N0 Low Speed VREFB1N0 10 VREFB1N0 17 VREFB1N0 DIFFIO RX L11p DIFFOUT L11p Low Speed 18 DIFFIO RX I 12r DIFFOLIT I 12r VREFB1N0 VREFB1N0 DIFFIO RX L12p DIFFOUT\_L12p DIFFOUT\_L14n Low\_Speed Low Speed IO TDO 20 DIFFIO RX L14n IFFIO RX I 14r DIFFOLIT I 14r Low Speed VREFB1N0 VREFB1N0 IO DIFFIO RX L16n DIFFOUT\_L16n DIFFOUT\_L16p Low\_Speed 24 25 DIFFIO RX L16p Low Speed VREFB2N0 CLK0n DIFFIO RX L18r DIFFOUT L18r High\_Speed CLK0p DIFFIO RX L18p DIFFOUT\_L18p High Speed 27 VREFB2N0 DIFFOUT L20n DIFFIO RX L20n CLK1n High Speed CLK1p High Speed VRFFB2N0 VRFFB2N0 PLL L CLKOUTn DIFFIO RX L27n DIFFOUT L27n High Speed VREFB2N0 VRFFB3N0 DIFFIO\_RX\_L27p DIFFOUT\_L27p DIFFOUT\_B1n High\_Speed High\_Speed 10 PLL L CLKOUTP DIFFIO TX RX B1p DIFFOUT B1p REFB3N0 High Speed VREFB3N0 10 DIFFIO\_TX\_RX\_B3n DIFFOUT\_B3n High\_Speed 41 High Speed REFR3NO IFFIO TX RX B5n IFFOLIT B5r High Speed 44 DIFFIO TX RX B5p DIFFOUT\_B5p DIFFOUT\_B7n VREFB3N0 High\_Speed High\_Speed 10 45 /RFFR3N0 DIFFIO TX RX B7n DIFFOLIT B7n High Speed 47 VREFB3N0 IO DIFFIO TX RX B9n DIFFOUT\_B9n High\_Speed 50 48 /REFB3N0 VREFB3N0 VREFB3N0 DIFFIO TX RX B9r DIFFOUT B9r High Speed VRFFB3N0 54 55 DIFFIO\_TX\_RX\_B12n DIFFOUT\_B12n VREFB3N0 High\_Speed DIFFIO TX RX B12p DIFFIO TX RX B14n DIFFOUT B12p DIFFOUT B14n High Speed DIFFIO\_TX\_RX\_B14p DIFFOUT\_B14p 58 /REFB3N0 High Speed VREFB3N0 Ю DIFFIO TX RX B16n DIFFOUT B16n 59 High Speed DIFFIO TX RX B16r DIFFOLIT B16n 60 VREFB4N0 VREFB4N0 61 62 VREFB4N0 10 DIFFIO\_TX\_RX\_B23n DIFFOUT\_B23n High\_Speed VRFFB4N0 DIFFIO TX RX B23p DIFFOUT B23p High Speed 65 66 69 VREFB4N0 10 DIFFIO\_TX\_RX\_B27n /REFB4N0 DIFFOUT\_B27n High\_Speed DIFFOUT\_B27p DIFFOUT\_R1p DIFFOUT\_R2p DIFFIO\_TX\_RX\_B27p IFFIO RX R1p High Speed High\_Speed IFFIO\_RX\_R2p VREFB5N0 DIFFIO RX R1n DIFFOUT\_R1n High\_Speed VREFB5N0 VREFB5N0 DIFFIO\_RX\_R2n DIFFIO\_RX\_R7p DIFFOUT R2n DIFFOUT\_R7p High Speed High\_Speed DIFFIO RX R7n DIFFOUT R7n High Speed 81 VREFB5N0 VREFB5N0 80 DIFFIO\_RX\_R10p DIFFOUT\_R10p VREFB5N0 Ю High\_Speed 85 DIFFIO RX R11r DIFFOLIT R11n High Speed 84 VRFFB5N0 DIFFIO RX R10n DIFFOUT R10n High Speed 87 VREFB5N0 10 DIFFIO\_RX\_R11n DIFFOUT\_R11n DIFFOUT\_R14p 86 High\_Speed DIFFIO RX R14c DIFFOUT\_R14n DIFFOUT\_R16p DIFFOUT\_R16n High\_Speed High\_Speed High\_Speed VREFB6N0 VREFB6N0 CLK2n CLK3p DIFFIO RX R14r IFFIO\_RX\_R16p REFB6N0 IFFIO RX R16r High\_Speed DIFFIO\_RX\_R18p DIFFOUT\_R18p VREFB6N0 DIFFOUT R18n DIFFIO RX R18n High Speed 93 High Spee VREFB6N0 VREFB6N0 DIFFIO RX R26n DIFFOUT R26n VREFR6N0 DPCLK2 High Speed 98 0 /REFB6N0 DIFFIO RX R27p DIFFOUT R27p High Speed 99 DIFFIO\_RX\_R28p DIFFOUT\_R28p 100 High\_Speed DIFFIO RX R27r DIFFOLIT R27r High Speed High Speed High\_Speed VRFFB6N0 DIFFIO RX R28n DIFFOUT R28n 102 105 VREFB6N0 DIFFIO RX R33n DIFFOUT R33n High\_Speed 106 VRFFB7N0 DIFFIO RX T1p DIFFOUT T1p High Speed 110 VREFB7N0 DIFFIO\_RX\_T1n DIFFOUT\_T1n High Speed 111 VREFB7N0 VRFFB7N0 113 VREFB7N0 114 VREFB7N0 IFFIO\_RX\_T10p DIFFOUT\_T10p High\_Speed 118 VRFFB7N0 DIFFIO RX T10n DIFFOUT T10n High Speed 119 VREFB8N0 DIFFIO RX T16p DIFFOUT T16p Low Speed 120 VREFB8N0 IFFIO RX T16n 121 10 DEV\_CLRn DIFFOUT\_T16 Low Speed VREFB8N0 122 VREFB8N0 8 VRFFR8NO 10 8 VREFB8N0 IO CONFIG\_SEL 126



nk Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
	8 VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	
	8 VREFB8N0	Input only		nCONFIG				
	8 VREFB8N0	IO			DIFFIO RX T19n	DIFFOUT T19n	Low Speed	
	8 VREFB8N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	
	8 VREFB8N0	10			DIFFIO RX T20n	DIFFOUT_T20n	Low Speed	
	8 VREFB8N0	10			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	
	8 VREFB8N0	10		CRC ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low Speed	
	8 VREFB8N0	IO						
	8 VREFB8N0	10		nSTATUS	DIFFIO RX T24p	DIFFOUT T24p	Low Speed	
	8 VREFB8N0	10		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	
	8 VREFB8N0	10			DIFFIO_RX_T26p	DIFFOUT_T26p	Low Speed	
	8 VREFB8N0	io			DIFFIO RX T26n	DIFFOUT T26n	Low Speed	
		GND						
		GND						
		GND						
		GND	1			+		1
		GND						_
		GND	+	+		+	<del>-  </del>	-
		GND	+	+		+	<del>-  </del>	-
		GND	+	+		+	<del>-  </del>	-
		GND	+			+	<del>-  </del>	_
		GND					+	-
		GND						
		GND					+	
		GND						_
		GND						
		VCCIO1A						-
		VCCIO1A VCCIO1B						
	-	VCCIO1B VCCIO2						
		VCCIO2 VCCIO3						
	-							
		VCCIO3						
		VCCIO4						
		VCCIO5						
		VCCIO6						
		VCCIO6						
		VCCIO7						
		VCCIO8						
		VCCIO8						
		VCCA1						
		VCCA2						
		VCCA3						
		VCCA3						
		VCCA4						
		VCCA5						
		VCCA6						
		VCC_ONE						
		VCC_ONE						
		VCC ONE						
		VCC_ONE		-				
		VCC_ONE						
		VCC ONE						
		VCC_ONE						
		VCC_ONE						
		VCC ONE					i	
		VCC_ONE					i	

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.
(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground plane of the PCB.



								Note (1)
Bank Number V	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
	VREFB1N0	10			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D2
	VREFB1N0 VREFB1N0	IO IO			DIFFIO_RX_L1p DIFFIO_RX_L3n	DIFFOUT_L1p DIFFOUT_L3n	Low_Speed	C2 F5
	VREFB1N0	10			DIFFIO RX L3n	DIFFOUT_L3p	Low Speed Low Speed	G5
	VREFB1N0	10			DIFFIO RX LSp DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	C1
		10			DIFFIO RX L5p	DIFFOUT L5p		B1
	VREFB1N0	10			DIFFIO RX L7n	DIFFOUT L7n		E1
1A V	VREFB1N0	10			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	E2
	VREFB1N0	IO		JTAGEN				G7
	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	G1
		IO	VREFB1N0					G2
		10		TCK	DIFFIO RX L11p	DIFFOUT L11p		J1
	VREFB1N0	10		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n		H5
	VREFB1N0 VREFB1N0	IO IO		TDO	DIFFIO_RX_L12p DIFFIO_RX_L14n	DIFFOUT_L12p DIFFOUT_L14n		H4 H3
		10			DIFFIO RX L14II		Low_Speed	J2
	VREFB1N0	10			DIFFIO RX L16n	DIFFOUT_L16n		L1
		10				DIFFOUT L16p	Low Speed	K2
2 \	VREFB2N0	10	CLK0n		DIFFIO RX L18n	DIFFOUT_L18n	High_Speed	J4
2 \	VREFB2N0	Ю	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	J5
2 \	VREFB2N0	IO	CLK1n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	K5
2 \	VREFB2N0	IO	CLK1p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	K4
2 V	VREFB2N0	10	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n		L5
2 V	VREFB2N0	10	VREFB2N0		DISSIO DV LOS	DIFFOUT LOS		P1
2 \	VREFB2NO	10	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	L4
	VREFB2N0 VREFB2N0	10	DLL L CLEOUTS		DIFFIO RX L27n	DIFFOUT L27n	Lliah Casad	R2 N1
	VREFB2N0 VREFB2N0	10	PLL L CLKOUTD PLL L CLKOUTD		DIFFIO RX L2/h DIFFIO_RX_L27p	DIFFOUT L27n DIFFOUT_L27p		N1 P2
	VREFB3N0	10	I LL_L_OLNOUTP		DIFFIO_RX_L27p DIFFIO_TX_RX_B1n	DIFFOUT_L27B DIFFOUT_B1n	High_Speed High_Speed	M4
	VREFB3N0	10			DIFFIO RX B2n	DIFFOUT B2n		P3
		10			DIFFIO TX RX B1p		High Speed	M5
3 V	VREFB3N0	10			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	R3
3 V	VREFB3N0	IO			DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	L6
	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed	P4
	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	L7
		IO			DIFFIO RX B4p			R5
	VREFB3N0	10			DIFFIO_TX_RX_B5n	DIFFOUT_B5n		P6
	VREFB3N0	10			DIFFIO_RX_B6n	DIFFOUT_B6n		R7 P7
	VREFB3N0 VREFB3N0	IO IO			DIFFIO TX RX B5p DIFFIO RX B6p	DIFFOUT B5p DIFFOUT B6p	High Speed High Speed	P8
		10						18
	VREFB3N0	10			DIFFIO RX B8n	DIFFOUT B8n	High Speed	PQ
	VREFB3N0	10			DIFFIO TX RX B7p	DIFFOUT B7p	High_Speed	M7
3 \	VREFB3N0	10			DIFFIO RX B8p	DIFFOUT_B8p		R9
		10			DIFFIO TX RX B9n	DIFFOUT B9n	High Speed	M8
		IO	VREFB3N0					R11
3 \	VREFB3N0	IO			DIFFIO TX RX B9p	DIFFOUT B9p	High Speed	N8
	VREFB3N0	IO						P12
	VREFB3N0	10			DIFFIO_TX_RX_B10n	DIFFOUT_B10n		R14
	VREFB3N0 VREFB3N0	IO IO			DIFFIO_TX_RX_B10p DIFFIO_TX_RX_B12n	DIFFOUT_B10p DIFFOUT_B12n	High_Speed	P15 I 9
	VREFB3N0	10			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High Speed High_Speed	M9
	VREFB3N0	IO			DIFFIO TX RX B14n	DIFFOUT_B14n	High_Speed	L10
3 1	VREFB3N0	10			DIFFIO TX RX B14II		High Speed	M11
	VREFB3N0	10			DIFFIO TX RX B16n	DIFFOUT B16n	High_Speed	P14
		10						R13
5 \	VREFB5N0	Ю			DIFFIO RX R1p	DIFFOUT R1p	High Speed	M12
5 V	VREFB5N0	10		-	DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	N15
	VREFB5N0	10			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	L11
		10			DIFFIO RX R2n		High Speed	N14
	VREFB5N0	10			DIFFIO RX R7p	DIFFOUT_R7p	High_Speed	K11 M14
5 V	VREFB5N0 VREFB5N0	IO IO	-		DIFFIO RX R7n	DIFFOUT R7n	High Speed	M14 K12
		10	VREFB5N0		DITTO KA KIII	DITTOUT KAIL	riigir opeeu	L15
5 1	VREFB5N0	10	VINCI BUINU		DIFFIO RX R10p	DIFFOUT_R10p	High_Speed	J9
		IO					High Speed	K14
5 \	VREFB5N0	10			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	J11
5 V	VREFB5N0	10			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	J14
6 V	VREFB6N0	IO	CLK2p		DIFFIO RX R14p	DIFFOUT R14p	High Speed	J12
		10	CLK2n		DIFFIO_RX_R14n			H11
6 V	VREFB6N0	10	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p		H12
6 V	VREFB6N0	10	CLK3n		DIFFIO RX R16n	DIFFOUT R16n		H13
	VREFB6N0 VREFB6N0	IO IO			DIFFIO_RX_R18p DIFFIO_RX_R18n	DIFFOUT_R18p DIFFOUT_R18n	High_Speed High Speed	J15 G15
	VREFB6N0 VREFB6N0	10	DPCLK3		DIFFIO_RX_R18n DIFFIO_RX_R26p		High_Speed High Speed	G15 G11
	VREFB6N0	10	VREEB6N0		DILLIO KY KZOP	Dil 1 001 N20p	riigir opecu	F15
	VREFB6N0	10	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	G12
	VREFB6N0	10				. 712177	Jp	E14
6 V	VICEDOINU	10			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	F11
6 V		10			DIFFIO RX R28p	DIFFOUT R28p	High_Speed	C15
6 V 6 V 6 V	VREFB6N0 VREFB6N0	IO						
6 V 6 V 6 V 6 V	VREFB6N0 VREFB6N0 VREFB6N0	IO IO			DIFFIO RX R27n	DIFFOUT R27n	High Speed	F12
6 V 6 V 6 V 6 V	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10			DIFFIO RX R27n DIFFIO RX R28n	DIFFOUT R27n DIFFOUT R28n	High Speed High_Speed	C14
6 V 6 V 6 V 6 V 6 V	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10 10			DIFFIO RX R27n DIFFIO RX R28n DIFFIO_RX_R33p	DIFFOUT R27n DIFFOUT_R28n DIFFOUT_R33p	High_Speed High_Speed High_Speed	C14 E11
6 V 6 V 6 V 6 V 6 V 6 V 6 V	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10 10 10			DIFFIO RX R27n DIFFIO_RX_R28n DIFFIO_RX_R33p DIFFIO RX_R33n	DIFFOUT R27n DIFFOUT R28n DIFFOUT R33p DIFFOUT R33n	High Speed High_Speed High_Speed High Speed	C14 E11 D12
6 V 6 V 6 V 6 V 6 V 6 V 8 V	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB8N0	10 10 10 10 10 10			DIFFIO RX R27n DIFFIO RX R28n DIFFIO RX R33p DIFFIO RX R33n DIFFIO RX T14p	DIFFOUT R27n DIFFOUT_R28n DIFFOUT_R33p DIFFOUT_R33n DIFFOUT_T14p	High Speed High_Speed High_Speed High Speed Low_Speed	C14 E11 D12 D11
6 V 6 V 6 V 6 V 6 V 6 V 6 V 8 V 8 V	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB8N0 VREFB8N0 VREFB8N0	10 10 10 10 10 10			DIFFIO RX R27n DIFFIO RX R28n DIFFIO RX R33p DIFFIO RX R33n DIFFIO RX T14p DIFFIO RX T14p	DIFFOUT R27n DIFFOUT R28n DIFFOUT R33p DIFFOUT R33n DIFFOUT T14p DIFFOUT T15p	High Speed High Speed High Speed High Speed Low Speed Low Speed	C14 E11 D12 D11 B15
6 V 6 V 6 V 6 V 6 V 6 V 6 V 8 V 8 V	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB8N0 VREFB8N0 VREFB8N0	10 10 10 10 10 10			DIFFIO RX R27n DIFFIO RX R28n DIFFIO RX R33p DIFFIO RX R33n DIFFIO RX T14p	DIFFOUT R27n DIFFOUT_R28n DIFFOUT_R33p DIFFOUT_R33n DIFFOUT_T14p	High Speed High Speed High Speed High Speed Low Speed Low Speed Low Speed	C14 E11 D12 D11

Pin List M153



Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
	8 VREFB8N0	10			DIFFIO_RX_T17p	DIFFOUT_T17p	Low_Speed	B13
	8 VREFB8N0	10		DEV_CLRn	DIFFIO RX T16n	DIFFOUT T16n	Low_Speed	B8
	8 VREFB8N0	10		DEV_CERTI	DIFFIO RX T17n	DIFFOUT T17n	Low Speed	A14
	8 VREFB8N0	10		DEV OE	DIFFIO RX T18p	DIFFOUT_T18p	Low Speed	E10
	8 VREFB8N0	10		DEV CE	DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	E9
	8 VREFB8N0	10	VREFB8N0		Dirio_rot_rion	5111001_11011	Eun_opeca	A13
	8 VREFB8N0	10	VILLIBOITO	CONFIG_SEL				D8
	8 VREFB8N0	IO		0011110_0022	DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	B12
	8 VREFB8N0	Input only		nCONFIG				E8
	8 VREFB8N0	IO			DIFFIO RX T19n	DIFFOUT T19n	Low Speed	B11
	8 VREFB8N0	IO			DIFFIO RX_T20p	DIFFOUT_T20p	Low_Speed	B7
	8 VREFB8N0	IO	İ		DIFFIO RX T21p	DIFFOUT T21p	Low Speed	A9
	8 VREFB8N0	IO	İ		DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B6
	8 VREFB8N0	10			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	A11
	8 VREFB8N0	IO			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	D7
	8 VREFB8N0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	Low Speed	A7
	8 VREFB8N0	10		CRC_ERROR	DIFFIO RX_T22n	DIFFOUT_T22n	Low_Speed	E7
	8 VREFB8N0	10		Jo_Ennon	DIFFIO RX T23n	DIFFOUT T23n	Low Speed	A5
	8 VREFB8N0	10		nSTATUS	DIFFIO RX T24p	DIFFOUT_T24p	Low Speed	D6
	8 VREFB8N0	10			51110_10121219	21 001_12.19	2011_00000	B4
	8 VREFB8N0	10		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	E6
	8 VREFB8N0	10	<u> </u>	55111 55112	DIFFIO RX T26p	DIFFOUT_T26p	Low Speed	A2
	8 VREFB8N0	10			DIFFIO RX T26n	DIFFOUT T26n	Low_Speed	A3
	O VICEI BOING	GND			DII 110_10X_120II	Bir1 001_120i1	EOW_Opeca	D4
		GND						E4
		GND						R15
		GND						R1
		GND						M6
	1	GND						M2
		GND						M10
	1	GND						L12
	1	GND						J7
	+	GND						H8
	1	GND						H14
	+	GND						G9
	+	GND						G9 G4
	+	GND						E5
	+	GND						E12
	+	GND						D9
		IGND						D5
	+	GND						
								B2
		GND						A15
		GND						A1
	+	VCCIO1A						F2
	+	VCCIO1B						H2
	+	VCCIO2						L2
	+	VCCIO3						P5 P11
	+	VCCIO3						
		VCCIO3						P10
		VCCIO5						L14
	+	VCCIO6						G14
		VCCIO6						F14
	<del>                                     </del>	VCCIO8						B9
		VCCIO8						B5
		VCCIO8						B10
		VCCA1						N2
		VCCA2						D14
		VCCA3						F4
		VCCA3						B3
		VCCA4						P13
		VCC_ONE						J8
		VCC_ONE						H9
		VCC ONE						H7
		VCC_ONE						G8

(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
				· ·				
1A	VREFB1N0	10			DIFFIO RX L1n	DIFFOUT L1n	Low Speed	D1
1A	VREFB1N0	10			DIFFIO RX L1p	DIFFOUT L1p	Low Speed	C2
1A 1A	VREFB1N0 VREFB1N0	10			DIFFIO RX L3n DIFFIO RX L3p	DIFFOUT L3n DIFFOUT L3p	Low Speed Low Speed	E3
		10			DIFFIO RX L5p	DIFFOUT LSp	Low Speed	C1
1A		10			DIFFIO RX L5p	DIFFOUT L5p	Low Speed	B1
1A	VREFB1N0	IO			DIFFIO RX L7n	DIFFOUT L7n	Low Speed	F1
1A	VREFB1N0	Ю			DIFFIO RX L7p	DIFFOUT L7p	Low Speed	E1
1B	VREFB1N0	Ю		JTAGEN				E5
1B	VREFB1N0	Ю		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	G1
1B 1B	VREFB1N0	10	VREFB1N0	TCK	DIFFIG BY 144-	DIFFOUT L11p	I 0I	H1 G2
1B		10		TDI	DIFFIO RX L11p	DIFFOUT L11p	Low Speed Low Speed	F5
1B 1B		10		TDO	DIFFIO RX L12n	DIFFOUT L12n	Low Speed	F6
1B		10		100	DIFFIO RX L14n	DIFFOUT L14n	Low Speed	F4
1B		Ю			DIFFIO RX L14p	DIFFOUT L14p	Low Speed	G4
1B	VREFB1N0	Ю			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	H2
1B		Ю			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	H3
		Ю	CLK0n		DIFFIO RX L18n			G5
	VREFB2N0	10	OLIVO-		DIFFIO RX L19n		High Speed	J1
		IO IO	CLK0p		DIFFIO RX L18p DIFFIO RX L19p	DIFFOUT L18p DIFFOUT L19p		H6 J2
2		10	CLK1n		DIFFIO RX L19p		High Speed High Speed	H5
2	VREFB2N0	10	CERTII		DIFFIO RX L2011	DIFFOUT L21n	High Speed	M1
2		IO	CLK1p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	H4
2	VREFB2N0	10	<u> </u>		DIFFIO RX L21p	DIFFOUT L21p		M2
	VREFB2N0	Ю	DPCLK0		DIFFIO RX L22n		High Speed	N2
		Ю	VREFB2N0					L1
		Ю	DPCLK1		DIFFIO RX L22p	DIFFOUT L22p	High Speed	N3
2	VREFB2N0	10	DIL I OLIKOLIT		DIFFIG BY LOT:	DIFFOLIT LOT:	History Const.	L2
2		IO IO	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT L27n	High Speed	M3
2	VREFB2N0 VREFB2N0	10	PLL L CLKOUTp		DIFFIO RX L28n DIFFIO RX L27p	DIFFOUT L28n DIFFOUT L27p	High Speed High Speed	K1
	VREFB2N0 VREFB2N0	10	FLL L GLKOUIP		DIFFIO RX L27p		High Speed	K2
		10			DIFFIO TX RX B1n			15
		10			DIFFIO RX B2n			M4
3	VREFB3N0	Ю			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	L4
3	VREFB3N0	Ю			DIFFIO RX B2p	DIFFOUT B2p	High Speed	M5
3	VREFB3N0	Ю			DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	K5
3	VREFB3N0	Ю			DIFFIO RX B4n	DIFFOUT B4n	High Speed	N4
	VREFB3N0	10			DIFFIO TX RX B3p	DIFFOUT B3p	High Speed	J5
		10			DIFFIO RX B4p DIFFIO TX RX B5n		High Speed	N5 N6
		10			DIFFIO IX RX B5II		High Speed High Speed	N7
		10			DIFFIO TX RX B5p		High Speed	M7
3	VREFB3N0	IO IO			DIFFIO RX B6p		High Speed	N8
3	VREFB3N0	Ю			DIFFIO TX RX B7n	DIFFOUT B7n	High Speed	J6
3	VREFB3N0	Ю			DIFFIO RX B8n	DIFFOUT B8n	High Speed	M8
	VREFB3N0	Ю			DIFFIO TX RX B7p			K6
	VREFB3N0	IO.			DIFFIO RX B8p	DIFFOUT B8p	High Speed	M9
		10	VDEEDONO		DIFFIO TX RX B9n	DIFFOUT B9n	High Speed	J7
3	VREFB3N0 VREFB3N0	IO IO	VREFB3N0		DIFFIO TX RX B9p	DIFFOUT B9p	High Speed	N11
3		10			Billio IX IXX Bap	Dii 1 001 B3p	riigii opecu	N12
3	VREFB3N0	Ю			DIFFIO TX RX B10n	DIFFOUT B10n	High Speed	M13
3	VREFB3N0	Ю			DIFFIO RX B11n	DIFFOUT B11n	High Speed	N10
3	VREFB3N0	Ю			DIFFIO TX RX B10p	DIFFOUT B10p	High Speed	M12
		Ю			DIFFIO RX B11p			N9
		10			DIFFIO TX RX B12n		High Speed	M11
		IO IO			DIFFIO TX RX B12p DIFFIO TX RX B14n	DIFFOUT B12p DIFFOUT B14n	High Speed	L11 J8
3	VREFB3N0 VREFB3N0	10			DIFFIO TX RX B14n DIFFIO TX RX B14p	DIFFOUT B14n DIFFOUT B14p	High Speed High Speed	J8 K8
3		10			DIFFIO TX RX B14p	DIFFOUT B14p	High Speed	M10
	VREFB3N0	10			DIFFIO TX RX B16p		High Speed	L10
5	VREFB5N0	Ю			DIFFIO RX R1p	DIFFOUT R1p	High Speed	K10
		Ю			DIFFIO RX R2p	DIFFOUT R2p	High Speed	K11
5		Ю		·	DIFFIO RX R1n	DIFFOUT R1n	High Speed	J10
5	VREFB5N0	10			DIFFIO RX R2n	DIFFOUT R2n	High Speed	L12
5	VREFB5N0	10			DIFFIO RX R7p	DIFFOUT R7p	High Speed	K12
	VREFB5N0 VREFB5N0	IO IO			DIFFIO RX R7n	DIFFOUT R7n	High Speed	J12
		10	VREFB5N0		DITTO KA KAII	DILLOGI KAII	riigii opeeu	K13
		10	71121 20110		DIFFIO RX R8p	DIFFOUT R8p	High Speed	J9
5		10			DIFFIO RX R9p		High Speed	J13
	VREFB5N0	Ю			DIFFIO RX R8n	DIFFOUT R8n	High Speed	H10
5	VREFB5N0	Ю			DIFFIO RX R9n	DIFFOUT R9n	High Speed	H13
		IO.			DIFFIO RX R10p	DIFFOUT R10p	High Speed	H9
	VREFB5N0	10			DIFFIO RX R11p	DIFFOUT R11p	High Speed	G13
	VREFB5N0 VREFB5N0	10			DIFFIO RX R10n DIFFIO RX R11n		High Speed	H8 G12
		10	CLK2p		DIFFIO RX R11n		High Speed High Speed	G12 G9
		IO	CLK2p CLK2n		DIFFIO RX R14p		High Speed	G10
b	VREFB6N0	10	CLK2n CLK3p		DIFFIO RX R14h		High Speed	F13
6		10	CLK3n		DIFFIO RX R16n	DIFFOUT R16n	High Speed	E13
6		Ю			DIFFIO RX R18p	DIFFOUT R18p	High Speed	F12
		10			DIFFIO RX R18n	DIFFOUT R18n	High Speed	E12
	VREFB6N0							
6	VREFB6N0 VREFB6N0	Ю	DPCLK3		DIFFIO RX R26p	DIFFOUT R26p	High Speed	F9
6	VREFB6N0 VREFB6N0 VREFB6N0	IO IO	VREFB6N0					D13
6 6	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	IO IO IO			DIFFIO RX R26p DIFFIO RX R26n	DIFFOUT R26p DIFFOUT R26n	High Speed High Speed	D13 F10
6 6 6	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	IO IO	VREFB6N0			DIFFOUT R26n		D13



								Note
ank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
	VREFB6N0	Ю			DIFFIO RX R28p	DIFFOUT R28p	High Speed	B12
	VREFB6N0	10	1		DIFFIO RX R25p	DIFFOUT R27n	High Speed	E9
	VREFB6N0	10			DIFFIO RX R28n	DIFFOUT R28n	High Speed	B11
	VREFB6N0	10			DIFFIO RX R29p	DIFFOUT R29p	High Speed	C12
-	VREFB6N0	10					High Coord	B13
	VREFB6N0	10			DIFFIO RX R30p DIFFIO RX R29n	DIFFOUT R30p DIFFOUT R29n	High Speed	C11
							High Speed	
	VREFB6N0	10			DIFFIO RX R30n	DIFFOUT R30n	High Speed	A12
	VREFB6N0	10			DIFFIO RX R31p	DIFFOUT R31p	High Speed	E10
	VREFB6N0	Ю			DIFFIO RX R31n	DIFFOUT R31n	High Speed	D9
	VREFB6N0	Ю			DIFFIO RX R33p	DIFFOUT R33p	High Speed	D12
	VREFB6N0	Ю			DIFFIO RX R33n	DIFFOUT R33n	High Speed	D11
	VREFB8N0	Ю			DIFFIO RX T14p	DIFFOUT T14p	Low Speed	C10
	VREFB8N0	Ю			DIFFIO RX T15p	DIFFOUT T15p	Low Speed	A8
	VREFB8N0	Ю			DIFFIO RX T14n	DIFFOUT T14n	Low Speed	C9
	VREFB8N0	Ю			DIFFIO RX T15n	DIFFOUT T15n	Low Speed	A9
	VREFB8N0	Ю			DIFFIO RX T16p	DIFFOUT T16p	Low Speed	B10
	VREFB8N0	Ю			DIFFIO RX T17p	DIFFOUT T17p	Low Speed	A10
	3 VREFB8N0	Ю		DEV CLRn	DIFFIO RX T16n	DIFFOUT T16n	Low Speed	B9
	VREFB8N0	IO			DIFFIO RX T17n	DIFFOUT T17n	Low Speed	A11
	VREFB8N0	10		DEV OE	DIFFIO RX T18p	DIFFOUT T18p	Low Speed	D8
	VREFB8N0	10	İ		DIFFIO RX T18p	DIFFOUT T18n	Low Speed	E8
	VREFB8N0	10	VREFB8N0		5 10. 10	5 55. 11011	сон оросо	B7
	3 VREFB8N0	10	VINE DOING	CONFIG SEL	+	<u> </u>	<b>†</b>	D7
		10		CONFIG SEL	DIFFIO RX T19p	DIEEOLIT T10p	Low Coood	D7
	VREFB8N0		1	LOONEIO	DIFFIO KY 119b	DIFFOUT T19p	Low Speed	E7
	VREFB8N0	Input only		nCONFIG	DIFFIG. BY T40.	DIFFOUR TAGE	1 0	
	VREFB8N0	10	1		DIFFIO RX T19n	DIFFOUT T19n	Low Speed	A6
	VREFB8N0	Ю			DIFFIO RX T20p	DIFFOUT T20p	Low Speed	B6
	VREFB8N0	Ю			DIFFIO RX T21p	DIFFOUT T21p	Low Speed	A4
	VREFB8N0	Ю			DIFFIO RX T20n	DIFFOUT T20n	Low Speed	B5
	VREFB8N0	Ю			DIFFIO RX T21n	DIFFOUT T21n	Low Speed	A3
	VREFB8N0	Ю			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	E6
	VREFB8N0	Ю			DIFFIO RX T23p	DIFFOUT T23p	Low Speed	B3
	3 VREFB8N0	Ю		CRC ERROR	DIFFIO RX T22n	DIFFOUT T22n	Low Speed	D6
	VREFB8N0	10			DIFFIO RX T23n	DIFFOUT T23n	Low Speed	B4
	VREFB8N0	10		nSTATUS	DIFFIO RX T24p	DIFFOUT T24p	Low Speed	C4
	3 VREFB8N0	10		INSTATOS	DII 1 10 101 124p	Dii 1 001 124p	LOW Opeca	A5
	VREFB8N0	10		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	C5
	3 VREFB8N0	10		CONF DONE	DIFFIO RX 124II	DIFFOUT T26p		A2
-	3 VREFB8N0	10			DIFFIO RX 126p	DIFFOUT T26n	Low Speed	B2
	3 VREFB8NU	GND			DIFFIO RX 1260	DIFFOUT 1260	Low Speed	
								D2
		GND						E2
		GND						N13
		GND						N1
		GND						M6
		GND						L9
		GND						J4
		GND						H12
		GND						G7
		GND						F3
		GND						E11
		GND						D5
		GND						C3
	1	GND	1					B8
	1	GND					1	A13
	1	GND					1	A1
	1	VCCIO1A					1	F2
	+	VCCIO1A VCCIO1B	1		+	<u> </u>	<b>†</b>	G3
	+		1		+	<u> </u>	<b>†</b>	K3
	+	VCCIO2 VCCIO2			-		<del>                                     </del>	J3
	+				-		<del>                                     </del>	
	+	VCCIO3	1		<b>+</b>	-	1	L8
	+	VCCIO3	ļ		ļ			L7
	+	VCCIO3	1		1	<u> </u>	<u> </u>	L6
	4	VCCIO5						J11
	1	VCCIO5						H11
	<u> </u>	VCCIO6						G11
	1	VCCIO6				1		F11
		VCCIO8						C8
		VCCIO8						C7
	1	VCCIO8	1					C6
	1	VCCA1						K4
	1	VCCA2	İ		1	1	1	D10
	+	VCCA2	1	<del> </del>	+	<u> </u>	<b>†</b>	D3
	+				-		<del>                                     </del>	D3
	1	VCCA3						
	1	VCCA4	1	ļ	+	1		K9
		VCC ONE	i .				1	H7
		VCC ONE						G8
								G8 G6 F7

(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.



								Note (1)
Sank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
			* * * * * * * * * * * * * * * * * * * *			•		
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D4
1A 1A	VREFB1N0 VREFB1N0	10			DIFFIO_RX_L2n DIFFIO_RX_L1p	DIFFOUT_L2n DIFFOUT L1p	Low_Speed	C2
1A	VREFB1N0	10			DIFFIO RX L1p	DIFFOUT L2b	Low Speed Low Speed	E4
IA	VREFB1N0	10			DIFFIO RX L3n	DIFFOUT L3n	Low_Speed	G6
1A	VREFB1N0	IO			DIFFIO RX L4n	DIFFOUT L4n	Low Speed	B1
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	H6
1A	VREFB1N0	10			DIFFIO_RX_L4p	DIFFOUT_L4p	Low_Speed	C1
1A	VREFB1N0	10			DIFFIO RX L5n	DIFFOUT L5n	Low Speed	F5
1A	VREFB1N0 VREFB1N0	10			DIFFIO_RX_L6n DIFFIO_RX_L5p	DIFFOUT_L6n	Low_Speed	D1 E5
1A 1A	VREFB1N0	10			DIFFIO RX LSp DIFFIO RX L6p	DIFFOUT L5p DIFFOUT L6p	Low Speed Low Speed	E5
1A	VREFB1N0	IO			DIFFIO RX L7n	DIFFOUT_L7n	Low Speed	G3
1A	VREFB1N0	IO			DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed	F1
1A	VREFB1N0	10			DIFFIO RX L7p	DIFFOUT L7p	Low Speed	F2
1A	VREFB1N0	10			DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	G1
IB	VREFB1N0 VREFB1N0	10			DIFFIO_RX_L9n DIFFIO_RX_L10n	DIFFOUT_L9n DIFFOUT L10n	Low_Speed	G7 H2
1B 1B	VREFB1N0 VRFFB1N0	10		JTAGEN	DIFFIO RX L10n	DIFFOUT L10n	Low Speed Low Speed	H2 H7
IB	VREFB1N0	10		STAGEN	DIFFIO RX L10p	DIFFOUT L10p	Low_Speed	H1
1B	VREFB1N0	10		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	J7
1B	VREFB1N0	IO	VREFB1N0				Low_Speed	J3
1B	VREFB1N0	10		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	J8
1B	VREFB1N0	10			DIESIO DV I IO	DIFFOUR LAG	Low Speed	J4
1B 1B	VREFB1N0 VREFB1N0	10	-	TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	H3
1B	VREFB1N0 VREFB1N0	10		TDO	DIFFIO_RX_L13n DIFFIO_RX_L12p	DIFFOUT_L13n DIFFOUT_L12p	Low_Speed Low Speed	J2 H4
1B	VREFB1N0	10	<u> </u>		DIFFIO RX L12p	DIFFOUT L13p	Low Speed	J1
1B	VREFB1N0	10			DIFFIO RX L14n	DIFFOUT_L14n	Low_Speed	J6
1B	VREFB1N0	IO			DIFFIO RX L15n	DIFFOUT L15n	Low Speed	K2
1B	VREFB1N0	10		·	DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	K7
1B	VREFB1N0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	Low_Speed	K1
1B 1B	VREFB1N0 VREFB1N0	10			DIFFIO RX L16n DIFFIO RX L17n	DIFFOUT L16n	Low Speed	K4
1B	VREFB1N0	10			DIFFIO_RX_L17II	DIFFOUT_L16p	Low_Speed Low_Speed	K3
1B	VREFB1N0	IO			DIFFIO RX L17p	DIFFOUT L17p	Low Speed	L2
2	2 VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	L3
- 2	2 VREFB2N0	IO			DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed	M1
2	2 VREFB2N0	10	CLK0p		DIFFIO RX L18p	DIFFOUT L18p	High Speed	M3
	VREFB2N0	10	lours.		DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed	M2
	2 VREFB2N0 2 VREFB2N0	10	CLK1n		DIFFIO_RX_L20n DIFFIO_RX_L21n	DIFFOUT_L20n DIFFOUT L21n	High_Speed High Speed	K8 N1
	VRFFB2N0	10	CLK1p		DIFFIO RX L2111 DIFFIO_RX_L20p		High_Speed	18
	2 VREFB2N0	10	CERTIF		DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed	P1
2	2 VREFB2N0	IO	DPCLK0		DIFFIO RX L22n	DIFFOUT L22n	High Speed	M4
- 2	VREFB2N0	IO	VREFB2N0				High_Speed	R1
	VREFB2N0	IO	DPCLK1		DIFFIO RX L22p	DIFFOUT_L22p	High Speed	N3
	2 VREFB2N0 2 VREFB2N0	10			DIFFIO RX L23n	DIFFOLIT 1.23n	High Speed	R2
	2 VREFB2N0 2 VREFB2N0	10			DIFFIO_RX_L23n DIFFIO_RX_L24n	DIFFOUT_L24n	High_Speed High_Speed	R3
	2 VREFB2N0	10			DIFFIO RX L23p	DIFFOUT L23p	High Speed	T3
2	2 VREFB2N0	IO	İ		DIFFIO_RX_L24p	DIFFOUT_L24p	High_Speed	P3
- 2	VREFB2N0	IO			DIFFIO_RX_L25n		High_Speed	L7
	2 VREFB2N0	IO			DIFFIO RX L26n	DIFFOUT L26n	High Speed	T1
	VREFB2N0	10			DIFFIO_RX_L25p	DIFFOUT_L25p	High_Speed	M7
	2 VREFB2N0 2 VREFB2N0	10	PLL L CLKOUTn		DIFFIO_RX_L26p DIFFIO_RX_L27n	DIFFOUT_L26p DIFFOUT L27n	High_Speed High Speed	T2 N4
	2 VREFB2N0	10	LE E GENOGIII		DIFFIO RX L27II	DIFFOUT_L28n	High Speed	U1
	2 VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	P4
- 2	VREFB2N0	10			DIFFIO RX L28p	DIFFOUT L28p	High Speed	U2
	VREFB3N0	10			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	R4
	3 VREFB3N0 3 VREFB3N0	10			DIFFIO_RX_B2n DIFFIO_TX_RX_B1p	DIFFOUT_B2n	High_Speed	U3 T4
-	3 VREFB3N0 3 VREFB3N0	10			DIFFIO_RX_B2p	DIFFOUT_B2p	High Speed High_Speed	V2
-	3 VREFB3N0	10	<u> </u>		DIFFIO_RX_B2p DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	P6
-	3 VREFB3N0	10			DIFFIO RX B4n	DIFFOUT B4n	High Speed	V3
	3 VREFB3N0	10			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	P5
- 3	VREFB3N0	10		·	DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	V4
	VREFB3N0	10	-		DIFFIO TX RX B5n	DIFFOUT Bon	High Speed	R5
	3 VREFB3N0 3 VREFB3N0	10			DIFFIO_RX_B6n DIFFIO_TX_RX_B5p	DIFFOUT_B6n DIFFOUT_B5p	High_Speed High_Speed	U5 R6
-	3 VREFB3N0	10			DIFFIO_IX_RX_BSp DIFFIO_RX_B6p	DIFFOUT B6p	High_Speed High_Speed	V5
	3 VREFB3N0	10			DIFFIO TX RX B7n	DIFFOUT_B7n	High_Speed	T5
	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed	T7
- 3	VREFB3N0	10			DIFFIO TX RX B7p	DIFFOUT B7p	High Speed	T6
	3 VREFB3N0	10			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed	T8
	3 VREFB3N0 3 VREFB3N0	10	VREFB3N0		DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	N7 U6
	3 VREFB3N0 3 VREFB3N0	10	VKEFB3NU		DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High Speed High Speed	U6 N8
-	3 VREFB3N0 3 VREFB3N0	10	<del> </del>		DIFFIG TV KV DAD	DIFF OUT_DBD	High_Speed High_Speed	V6
	3 VREFB3N0	10			DIFFIO TX RX B10n	DIFFOUT B10n	High Speed	R8
	3 VREFB3N0	10			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed	U7
	3 VREFB3N0	10		·	DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	R9
	3 VREFB3N0	10			DIFFIO RX B11p	DIFFOUT B11p	High Speed	V7
	VREFB3N0	10			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	V9 U8
-	3 VREFB3N0 3 VREFB3N0	10	1		DIFFIO RX B13n DIFFIO TX RX B12p	DIFFOUT_B13n DIFFOUT_B12p	High Speed High Speed	U8 U9
	3 VREFB3N0	10			DIFFIO RX B13p		High_Speed	V8
	3 VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	M8



									Note (1)
OFFICE   C	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	
OFFICE   C						DISSIO BY DAS	DISCOULT DATE		1// 0
September		3 VREFB3NU					DIFFOUT_B15n	High_Speed	
Control   Cont								High_Speed	
1977   1978   1979									
Common   C								High_Speed	
OCCUPATION   OCC								High Speed	
A CAPPART   Color								High Speed	
CORNECT   CONTROL   CONT		4 VREFRANO						High Speed	
Company   Comp									
Company   Comp									
COMPAND   CONTINUE						DIFFIO RX B19p		High Speed	
OFFICE   O		4 VREFB4N0	IO					High Speed	
1   1   1   1   1   1   1   1   1   1				VREFB4N0				High Speed	T11
1   1   1   1   1   1   1   1   1   1		4 VREFB4N0	IO			DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	L10
		4 VREFB4N0	IO					High Speed	T12
1   1   1   1   1   1   1   1   1   1		4 VREFB4N0	10			DIFFIO_TX_RX_B21n	DIFFOUT_B21n	High_Speed	R10
								High_Speed	
1   COCCADO   COLUMN   COLUM			IO					High Speed	R11
4   605   180   190									
4.057540								High_Speed	
								High Speed	
4   000000000000000000000000000000000		4 VREFB4N0				DIFFIO_TX_RX_B23p	DIFFOUT_B23p		
4,979-90   0   1   1   1   1   1   1   1   1									
							DIFFOUT BASS	High_Speed	
4   0.044-0.00   0   0   0   0   0   0   0   0   0							DIFFOUT BOSS		
		4 VEETBAND					DIFFOUT BOZO		
								High Speed	
OFFICIAL   OFFICIAL								High Speed	
DECEMBER   DECEMBER	-							High Speed	
September   Sept									
1   1   1   1   1   1   1   1   1   1									
OPERISON   OPERISON									
1   1   1   1   1   1   1   1   1   1						DIFFIO RX R3n	DIFFOLIT R3n		M12
1   1   1   1   1   1   1   1   1   1							DIFFOUT R4p	High Speed	
STORY   State		5 VREFB5N0					DIFFOUT R3n		
1 (VREPSN)   10   10   10   10   10   10   10   1									
3 VRETSHOD   10   10   10   10   10   10   10   1		5 VREFB5N0	IO			DIFFIO RX R5p	DIFFOUT_R5p	High Speed	N15
S VISTERNAD   O		5 VREFB5N0	IO			DIFFIO RX R6p	DIFFOUT R6p	High Speed	N16
Symptoms								High Speed	
S. VREFERNO   O			IO			DIFFIO_RX_R6n		High_Speed	M16
Syrefield   Diffort Rich   Diffort Rich   High Seed   P15		5 VREFB5N0	10			DIFFIO_RX_R7p	DIFFOUT_R7p		R15
S   VREFERNO   IO								High Speed	
Syntemson			10			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	
Symposium   Symp		5 VREFB5N0		VREFB5N0				High_Speed	
SVREFBMD   O						DIFFIO RX R8p			
SVREPSHOW   O									
SyREFBAND   O   DEFOUR RIP   DEFOUT RIP   High, Seed   1.15			10					High_Speed	
S   WREFBOND   IO							DIFFOUT R9n	High Speed	
STREFERNO   C									
STREFERNO   O   DIFFO RX, R110   DIFFOUT R110   Hgp, Speed   K16									
STREEPSNO   O								High Speed	
S   YREF958/0   IO								High Speed	
SYREFBSNO   IO								High Speed	
S   WREFSBNO   IO		5 VREFB5N0					DIFFOUT R12n	High Speed	
6 VREFBRNO   O   CLXp									
6   VREFBRNO   IO				CLK2p				High Speed	
6   WREFBON   O			10			DIFFIO RX R15p	DIFFOUT R15p	High Speed	
6   VREFBBN0   IO				CLK2n		DIFFIO RX R14n	DIFFOUT R14n	High Speed	
6   VREEPBRN   O			10						L18
6   VREEPBRON   10   10   14   14   15   15   16   17   16   18   18   18   18   18   18   18				CLK3p			DIFFOUT_R16p	High_Speed	
6   VREFBBNO   0			10				DIFFOUT_R17p	High_Speed	
6   VREFB6N0   IO		6 VREFB6N0	10	CLK3n			DIFFOUT R16n	High Speed	K17
6   VREFBRNO   10   10   10   10   10   10   10   1								High_Speed	
6   VREFBRNO   10   10   10   10   10   10   10   1								High_Speed	
6   VREFBRNO   O							DIFFOUT R19p	High Speed	
FIVEEPBRND   IC   IDIFFIC RX R20D   DIFFOUT R20D   High Speed   J12		6 VREFB6N0						High_Speed	
6   VREFBBN0   O								High_Speed	
6   VREFBRNO   10   10   10   10   10   10   10   1									
6   VREFBBNO   10   10   10   10   10   10   10   1									
6   VREFBRNO   0   0   0   0   0   0   0   0   0						DIFFIO_RX_R22p	DIFFOUT ROS-	High_Speed	
6   VREFBBNO   10   DIFFIO   XX R23n   DIFFOUT   R23n   High   Speed   H16			10			DIFFIO BY B225	DIFFOUT R23p	High Speed	J16
6   VREFBRNO   O   O   O   O   O   O   O   O   O	-								
6   VREFBRNO   O   VREFBRNO   O   DPCL/2   DIFFIO RX R26n   DIFFOUT R26n   High Speed   H12				DBCI K3					
6   VREFBBNO   O   O   O   O   O   O   O   O   O						DIFFIU KA KZOP	DIFFOUT KZOP		
6   VREFBRNO   O						DIFFIO BY B26n	DIFFOLIT R26n		
6   VREFBBNO   D   DIFFIO RX R27p   DIFFOUT R27p   High Speed   F15				DI OLIVE		DII I IO_RA_RZOII	DITT OUT_RZUIT	High Speed	
6   VREFB6NO   10   0  10  10  10  10  10  10  10  1						DIFFIO BY B27n	DIFFOLIT P27n	High Speed	
6   VREFBBNO   10   DIFFIO RX R27n   DIFFOUT R27n   High Speed   G15							DIFFOUT R28n		
6   VREFBBND   O   DIFFIO RX R28n   DIFFOUT R28n   High Speed   F16   6   VREFBBND   O   DIFFIO RX R29p   DIFFOUT R29p   High Speed   E16   6   VREFBBND   O   DIFFIO RX R30p   DIFFOUT R30p   High Speed   E16   6   VREFBBND   O   DIFFIO RX R30p   DIFFOUT R30p   High Speed   D18   6   VREFBBND   O   DIFFIO RX R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFIO RX R39n   DIFFOUT R39n   High Speed   D16   6   VREFBBND   O   DIFFOUT R39n   DIFFOUT R39n   High Speed   D16   6   VREFBBND   O   DIFFOUT R39n   DIFFOUT R39n   High Speed   D16   6   VREFBBND   O   DIFFOUT R39n   DIFFOUT R39n   High Speed   D16   6   VREFBBND   O   DIFFOUT R39n   DIFFOUT R39n   High Speed   D16   6   VREFBBND   O   DIFFOUT R39n   DIFFOUT R39n   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   DIFFOUT R30p   DIFFOUT R30p   High Speed   D16   6   VREFBBND   O   D16									
6 VREFB6NO   D   DIFFIO RX R29p   DIFFOUT R29p   High Speed   E16									
6 VREFB6N0 IO DIFFO X R30p DIFFOUT R30p High Speed D18 6 VREFB6N0 IO DIFFO_RX_R29n DIFFOUT_R29n High_Speed D16			IO			DIFFIO RX R29p		High Speed	
6 VREFB6N0 IO DIFFO_RX_R29n DIFFOUT_R29n High_Speed D16							DIFFOUT R30p		
		6 VREFB6N0	IO			DIFFIO_RX_R30n			E17



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
	6 VREFB6N0	10			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed	G11
		10			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	C18
	6 VREFB6N0 6 VREFB6N0	10 10			DIFFIO RX R31n DIFFIO RX R32n	DIFFOUT_R31n DIFFOUT_R32n	High Speed High Speed	G12 B18
	6 VREFB6N0	10			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	E15
	6 VREFB6N0	10			DIFFIO RX R34p		High Speed	D17
		10			DIFFIO RX R33n	DIFFOUT R33n	High_Speed	D15
	6 VREFB6N0	10			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed	C17
	7 VREFB7N0	10			DIFFIO RX T1p	DIFFOUT T1p	High Speed	E14
		10			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed	B17
		IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High Speed	D14
		10			DIFFIO RX T2n	DIFFOUT T2n	High Speed	B16
		IO IO			DIFFIO_RX_T3p	DIFFOUT_T3p	High_Speed	D12
		10			DIFFIO RX T3n	DIFFOUT T3n	High_Speed High Speed	A17 D13
	7 VREFB7N0	10	VREFB7N0		DIFFIC RX 13II	DIFFOOT TSIT	High_Speed	A16
		10	VICEI DINO		DIFFIO_RX_T4p	DIFFOUT_T4p	High_Speed	C16
		10			DIFFIO RX T5p		High Speed	A15
	7 VREFB7N0	IO			DIFFIO RX T4n	DIFFOUT_T4n	High_Speed	C15
	7 VREFB7N0	10			DIFFIO_RX_T5n	DIFFOUT_T5n	High_Speed	A14
		10			DIFFIO RX T6p	DIFFOUT T6p	High Speed	C14
		10			DIFFIO_RX_T7p	DIFFOUT_T7p	High_Speed	B14
		10			DIFFIO_RX_T6n	DIFFOUT_T6n	High_Speed	C13
		10			DIFFIO RX T7n	DIFFOUT T7n	High Speed	B13
		10			DIFFIO_RX_T8p DIFFIO_RX_T9p	DIFFOUT_T8p DIFFOUT_T9p	High_Speed	F11 C12
		10			DIFFIO_RX_19p DIFFIO_RX_T8n		High_Speed High Speed	C12 F12
		10			DIFFIO RX 18h	DIFFOUT_T9n	High_Speed	B12
	7 VREFB7N0	10			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	C11
		10			DIFFIO RX T11p	DIFFOUT T11p	High Speed	A13
		IO			DIFFIO_RX_T10n		High_Speed	B11
		10			DIFFIO_RX_T11n	DIFFOUT_T11n	High_Speed	A12
		10			DIFFIO RX T12p	DIFFOUT T12p	Low Speed	D10
		10			DIFFIO_RX_T13p	DIFFOUT_T13p	Low_Speed	A11
		IO			DIFFIO_RX_T12n	DIFFOUT_T12n	Low_Speed	D9
		10			DIFFIO RX T13n DIFFIO RX T14n	DIFFOUT T13n DIFFOUT T14n	Low Speed	A10 F10
		10			DIFFIO_RX_T14p	DIFFOUT_T15p	Low_Speed	F10
		IO			DIFFIO_RX_113p	DIFFOUT T14n	Low_Speed Low Speed	G10
		10			DIFFIO RX T15n	DIFFOUT_T15n	Low_Speed	A8
	8 VREFB8N0	IO			DIFFIO RX T16p	DIFFOUT T16p	Low Speed	B9
	8 VREFB8N0	IO			DIFFIO RX T17p	DIFFOUT T17p	Low Speed	C10
		10		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B8
	8 VREFB8N0	10			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed	C9
		IO		DEV OE	DIFFIO RX T18p	DIFFOUT T18p	Low Speed	D8
		10			DIFFIG BY TA	DIFFOLIT TAR	Low_Speed	A7
	8 VREFB8N0 8 VREFB8N0	IO IO	VREFB8N0		DIFFIO RX T18n	DIFFOUT_T18n	Low Speed	D7 B7
		10	VREFBOINU	CONFIG SEL			Low Speed Low Speed	G9
		10		CONFIG_SEE	DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	A6
		Input only		nCONFIG	511110_10(_110p	5111 GG1_110p	Low Speed	H9
		10			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	A5
		10			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	C6
		10			DIFFIO RX T21p	DIFFOUT T21p	Low Speed	C8
		10			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B5
		10			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	C7
		10			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	C5 A4
	8 VREFB8N0 8 VREFB8N0	10		CRC ERROR	DIFFIO_RX_T23p DIFFIO_RX_T22n	DIFFOUT_T23p DIFFOUT_T22n	Low_Speed Low Speed	A4 C4
		10		UNU_ENNUN	DIFFIO_RX_122n DIFFIO_RX_T23n	DIFFOUT T23n	Low_Speed Low Speed	B4
		IO		nSTATUS	DIFFIO RX 12311 DIFFIO RX T24p	DIFFOUT_T24p	Low_Speed	G8
		10			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed	A3
	8 VREFB8N0	IO		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	H8
	8 VREFB8N0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	Low_Speed	B3
	8 VREFB8N0	10			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	D6
		Ю			DIFFIO RX T27p	DIFFOUT T27p	Low Speed	A2
		10			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	D5
		IO CND			DIFFIO_RX_T27n	DIFFOUT_T27n	Low_Speed	B2
		GND					<b> </b>	E2 E3
		GND GND					1	V18
	+	GND					l	V18
	†	GND					1	U4
		GND						U14
		GND						U10
_		GND						R7
		GND		-	-			N5
		GND			-			N2
		GND						N17
		GND					ļ	N12
	+	GND					ļ	N10
	<del>                                     </del>	GND GND					<b> </b>	M14
	+	GND					l	K9
		GND						K6
		GND					1	K13
	1	GND						J17
		GND						J10
		GND						H14
					· · · · · · · · · · · · · · · · · · ·			



ank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
			.,					
		GND						G4
		GND						G2
		GND						F8
		GND						F17
		GND						E6
		GND						E13
		GND						E10
		GND						D3
		GND						B6
		GND						B15
		GND	1					B10
		GND	1					A18
		GND						A10
		VCCIO1A						H5
		VCCIO1A VCCIO1A						G5
		VCCIO1A VCCIO1B						
								K5
		VCCIO1B	1	+				J5
		VCCIO2						M5
		VCCIO2						L6
		VCCIO2						L5
		VCCIO3						P9
		VCCIO3						P8
		VCCIO3						P7
		VCCIO3						N9
		VCCIO4						P12
		VCCIO4						P11
		VCCIO5						M13
		VCCIO5						L14
		VCCIO5						L13
		VCCIO5						K14
		VCCIO6						J14
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G14
		VCCIO6	1					G13
		VCCIO7						E12
		VCCIO7	+				1	E11
		VCCIO7						D11
		VCCIO7						
								F9 E9
		VCCIO8						
		VCCIO8						E8
	1	VCCIO8	1	1				E7
		NC NC	1	+				N13
		NC						F7
		VCCA1						M6
		VCCA2						F14
		VCCA3	1					F3
		VCCA3						F6
		VCCA3						F4
		VCCA4						P13
•		VCC ONE						L9
		VCC_ONE					_	K10
		VCC_ONE						J9
		VCC ONE						H10
		VCC_ONE						N6
	1	VCC_ONE						F13
	1	VCC ONE	1					C3

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.

