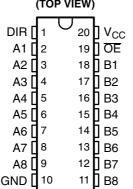
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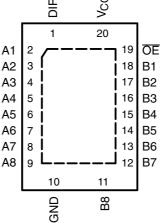
- Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Latch-Up Performance Exceeds 500 mA Per **JEDEC Standard JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54ABT245A...JORWPACKAGE SN74ABT245B...DB, DGV, DW, N, NS, **OR PW PACKAGE** (TOP VIEW)

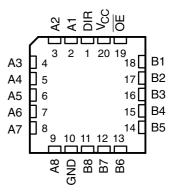


(TOP VIEW) Vcc α Ճ 20 ŌĒ 19 2 Α1 3 18 B1 A2 АЗ | 17 B2

SN74ABT245B...RGY PACKAGE



SN54ABT245B . . . FK PACKAGE (TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

T _A	PACKAGE [†]	†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74ABT245BN	SN74ABT245BN
	QFN – RGY	Tape and reel	SN74ABT245BRGYR	AB245B
	COIC DW	Tube	SN74ABT245BDW	ADTO4FD
	SOIC – DW	Tape and reel	SN74ABT245BDWR	ABT245B
	SOP - NS	Tape and reel	SN74ABT245BNSR	ABT245B
-40°C to 85°C	SSOP – DB	Tape and reel	SN74ABT245BDBR	AB245B
	TOCOD DW	Tube	SN74ABT245BPW	ADOAED
	TSSOP – PW	Tape and reel	SN74ABT245BPWR	AB245B
	TVSOP – DGV	Tape and reel	SN74ABT245BDGVR	AB245B
	VFBGA – GQN	Town and work	SN74ABT245BGQNR	ADOJED
	VFBGA – ZQN (Pb-free)	Tape and reel	SN74ABT245BZQNR	AB245B
	CDIP – J	Tube	SNJ54ABT245AJ	SNJ54ABT245AJ
–55°C to 125°C	CFP – W	Tube	SNJ54ABT245AW	SNJ54ABT245AW
	LCCC – FK	Tube	SNJ54ABT245AFK	SNJ54ABT245AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



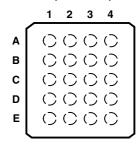
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description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74ABT245B...GQN OR ZQN PACKAGE (TOP VIEW)



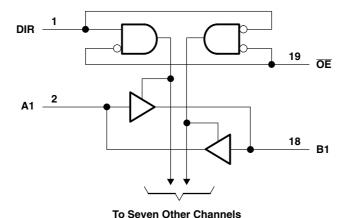
terminal assignments

	1	2	3	4
Α	A1	DIR	V_{CC}	ŌĒ
В	А3	B2	A2	B1
С	A5	A4	B4	В3
D	A7	B6	A6	B5
Е	GND	A8	B8	B7

FUNCTION TABLE

INP	UTS	ODEDATION					
OE	DIR	OPERATION					
L	L	B data to A bus					
L	Н	A data to B bus					
Н	Χ	Isolation					

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V t	to 7 V
Input voltage range, V _I (except I/O ports) (see Note 1)	
Voltage range applied to any output in the high or power-off state, V _O	
Current into any output in the low state, I _O : SN54ABT245A	
SN74ABT245B	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$)	
Package thermal impedance, θ _{JA} (see Note 2): DB package	
(see Note 2): DGV package	
(see Note 2): DW package	
(see Note 2): GQN/ZQN package	
(see Note 2): N package 69	
(see Note 2): NS package	
(see Note 2): PW package	
(see Note 3): RGY package	
Storage temperature range, T _{stq} –65°C to 1	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. The package thermal impedance is calculated in accordance with JESD 51-7.
- 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		SN54AB	T245A	SN74AB	T245B	
		MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	V_{CC}	0	V_{CC}	V
I _{OH}	High-level output current		-24		-32	mA
l _{OL}	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ABT245A, SN74ABT245B **OCTAL BUS TRANSCEIVERS** WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		7707.001	DITIONS	T	_A = 25°C	;	SN54AB	T245A	SN74AB	T245B	LINIT
PAI	RAMETER	TEST CON	DITIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
V _{IK}		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2		-1.2		-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
l ,,		$V_{CC} = 5 V$,	$I_{OH} = -3 \text{ mA}$	3			3		3		٧
V _{OH}		V - 45 V	$I_{OH} = -24 \text{ mA}$	2			2				V
		V _{CC} = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55			٧
		VCC = 4.5 V	$I_{OL} = 64 \text{ mA}$			0.55*				0.55	V
V_{hys}					100						mV
	Control inputs	$V_{CC} = 0 \text{ to } 5.5 \text{ V}, V_{I} =$	V _{CC} or GND			±1		±1		±1	
l _l	A or B ports	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$				±20		±100		±20	μΑ
I _{OZPU}		$V_{CC} = 0$ to 2.1 V, $V_{O} = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	μΑ
I _{OZPD}		$V_{CC} = 2.1 \text{ V to 0},$ $V_{O} = 0.5 \text{ V to 2.7 V}, \overline{\text{O}}$			±50		±50		±50	μΑ	
I _{OZH} ‡		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$ $V_{O} = 2.7 \text{ V}, \overline{OE} \ge 2 \text{ V}$				10		10		10	μА
I _{OZL} ‡		$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}, V_{O} = 0.5 \text{ V}, \overline{OE} \ge 2 \text{ V}$				-10		-10		-10	μΑ
I _{off}		$V_{CC} = 0$,	V_I or $V_O \le 5.5 \text{ V}$			±100				±100	μΑ
I _{CEX}		$V_{CC} = 5.5 \text{ V},$ $V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μА
I _O §		$V_{CC} = 5.5 \text{ V},$	V _O = 2.5 V	-50	-140	-180	-50	-180	-50	-180	mA
		V _{CC} = 5.5 V,	Outputs high		5	250		250		250	μΑ
Icc	A or B ports	$I_{O} = 0$,	Outputs low		22	30		30		30	mA
		$V_I = V_{CC}$ or GND	Outputs disabled		1	250		250		250	μΑ
	Data inputa	$V_{CC} = 5.5 \text{ V},$ One input at 3.4 V,	Outputs enabled			1.5		1.5		1.5	mA
ΔI _{CC} ¶	Data inputs Other inpu		Outputs disabled			50		50		50	μА
	Control inputs	V_{CC} = 5.5 V, One inp Other inputs at V_{CC} of				1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V			4						pF
C _{io}	A or B ports	$V_{O} = 2.5 \text{ V or } 0.5 \text{ V}$			8						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.



 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V.

[‡] The parameters I_{OZH} and I_{OZL} include the input leakage current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 $[\]P$ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

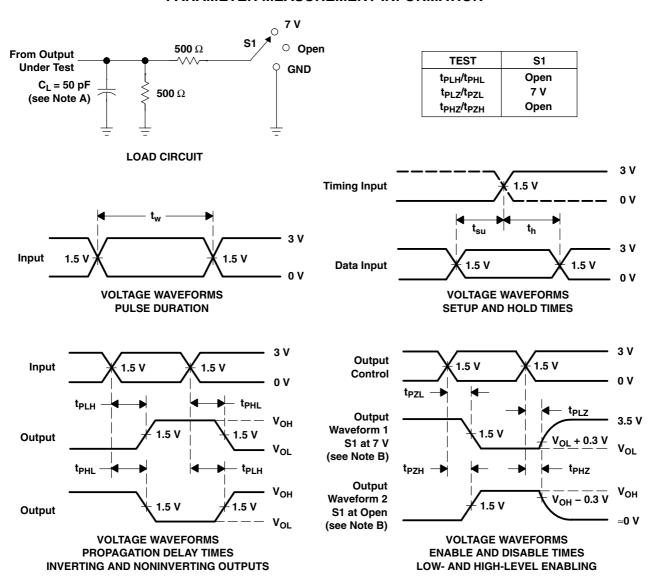
SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V _{CC} = 5 V, T _A = 25°C			SN54AB	T245A	SN74AB	UNIT	
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A D	D ou A	1	2	3.2	0.8	3.8	1	3.6	
t _{PHL}	A or B	B or A	1	2.6	3.5	1	4.2	1	3.9	ns
t _{PZH}	0 5	A ou D	2	3.5	4.5	1.2	6.2	2	5.6	
t _{PZL}	ŌĒ	A or B	1.9	4	5.3	1.3	6.8	1.9	6.2	ns
t _{PHZ}	ŌĒ	A or B	2.2	4.4	5.4	2.2	6.1	2.2	5.9	ns
t _{PLZ}	OE .	AOIB	1.5	3	4	1.0	4.9	1.5	4.5	115
t _{sk(o)}					0.5				0.5	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







24-Aug-2018

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9214802Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9214802Q2A SNJ54ABT 245AFK	Samples
5962-9214802QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9214802QR A SNJ54ABT245AJ	Samples
5962-9214802QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9214802QS A SNJ54ABT245AW	Samples
SN74ABT245BDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT245BN	Samples
SN74ABT245BNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT245BN	Samples
SN74ABT245BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT245B	Samples
SN74ABT245BPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples



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PACKAGE OPTION ADDENDUM

24-Aug-2018

Orderable Device	Status	Package Type	Package Drawing		Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT245BPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB245B	Samples
SN74ABT245BRGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB245B	Sample
SNJ54ABT245AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9214802Q2A SNJ54ABT 245AFK	Sample
SNJ54ABT245AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9214802QR A SNJ54ABT245AJ	Sample
SNJ54ABT245AW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9214802QS A SNJ54ABT245AW	Sample

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

24-Aug-2018

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ABT245B:

■ Enhanced Product: SN74ABT245B-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT245BDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT245BDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ABT245BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT245BNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ABT245BPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74ABT245BRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

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*All dimensions are nominal

All difficultions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT245BDBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74ABT245BDGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74ABT245BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT245BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ABT245BPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74ABT245BRGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20



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