

								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
_								
A A	VREFB1N0 VREFB1N0	10	ADC1IN1 ADC1IN2		DIFFIO_RX_L1n DIFFIO_RX_L1p	DIFFOUT_L1n DIFFOUT_L1p	Low_Speed	
A	VREFB1N0 VREFB1N0	10	ADC1IN2 ADC1IN3		DIFFIO_RX_LTP DIFFIO_RX_L3n	DIFFOUT L3n	Low_Speed Low Speed	+
A	VREFB1N0	10	ADC1IN4		DIFFIO RX L3p	DIFFOUT_L3p	Low_Speed	10
Ä	VREFB1N0	10	ADC1IN5		DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	12
A	VREFB1N0	10	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	12
A	VREFB1N0	10	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	13
A	VREFB1N0	10	ADC1IN8		DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	14
В		10		JTAGEN				15
В	VREFB1N0	IO .	VOESTANIA	TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	16
B B	VREFB1N0 VRFFB1N0	10	VREFB1N0	TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	1/
В	VREFB1N0	10		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	19
В	VREFB1N0	IO		TDO	DIFFIO RX L12p	DIFFOUT_L12p	Low_Speed	20
В	VREFB1N0	IO			DIFFIO RX L14n	DIFFOUT L14n	Low Speed	21
В	VREFB1N0	10			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	22
В	VREFB1N0	10			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	24
В	VREFB1N0	IO			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	25
2	VREFB2N0	10	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	26
2	VREFB2N0 VREFB2N0	10	CLK0p CLK1n		DIFFIO_RX_L18p DIFFIO_RX_L20n	DIFFOUT_L18p DIFFOUT_L20n	High_Speed	27
2	VREFB2N0	10	CLK11p		DIFFIO RX L20p	DIFFOUT_L20p	High Speed High Speed	29
2	VREFB2N0	10	VREFB2N0		DITTIO TO TO TO	DIT 001_E20p	riigii_opecu	30
2	VREFB2N0	IO	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT L27n	High Speed	32
2	VREFB2N0	10	PLL_L_CLKOUTp		DIFFIO RX L27p	DIFFOUT_L27p	High_Speed	33
	VREFB3N0	10			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	38
3	VREFB3N0	10			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	39
3	VREFB3N0	10			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	41
3	VREFB3N0 VREFB3N0	10			DIFFIO_TX_RX_B3p DIFFIO_TX_RX_B5n	DIFFOUT B3p DIFFOUT B5n	High Speed High Speed	43
3		10			DIFFIO TX RX B50		High_Speed	45
3	VREFB3N0	IO			DIFFIO TX RX B7n	DIFFOUT_B7n	High_Speed	46
3		IO			DIFFIO TX RX B7p	DIFFOUT B7p	High Speed	47
3	VREFB3N0	10			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	50
	VREFB3N0	10	VREFB3N0					48
	VREFB3N0	10			DIFFIO TX RX B9p	DIFFOUT B9p	High Speed	52 54
3	VREFB3N0 VREFB3N0	10			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	Llink Connd	54
3	VREFB3N0	10			DIFFIO TX RX B12II	DIFFOUT B12p	High_Speed High Speed	56
	VREFB3N0	10			DIFFIO TX RX B14n	DIFFOUT B14n	High_Speed	57
	VREFB3N0	10			DIFFIO TX RX B14p		High_Speed	58
3	VREFB3N0	10			DIFFIO TX RX B16n	DIFFOUT B16n	High Speed	59
3	VREFB3N0	10			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	60
	VREFB4N0	10	VREFB4N0					61
		10			DIFFIO TX RX B23n	DIFFOUT_B23n	Llink Connd	62 64
	VREFB4N0	10			DIFFIO_TX_RX_B23II DIFFIO_TX_RX_B23p	DIFFOUT_B23p	High_Speed High_Speed	65
4	VREFB4N0	10			BILLIO LY IX BESS	DITT GGT_B25p	riigii_opecu	66
4	VREFB4N0	10			DIFFIO TX RX B27n	DIFFOUT_B27n	High Speed	69
		10			DIFFIO_TX_RX_B27p	DIFFOUT_B27p	High_Speed	70
	VREFB5N0	10			DIFFIO RX R1p	DIFFOUT R1p	High Speed	75
5	VREFB5N0	IO .			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	74
5		10			DIFFIO_RX_R1n DIFFIO_RX_R2n	DIFFOUT_R1n DIFFOUT_R2n	High_Speed High Speed	77
		10			DIFFIO RX RZII	DIFFOUT_R7p	High_Speed	79
	VREFB5N0	10			511110_101_101	Bill Col_Kip	riigii_opood	78
	VREFB5N0	10			DIFFIO RX R7n	DIFFOUT R7n	High Speed	81
5	VREFB5N0	10	VREFB5N0					80
5	VREFB5N0	10			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	85
	VREFB5N0	10			DIFFIO RX R11p	DIFFOUT R11p	High Speed	84
	VREFB5N0 VREFB5N0	10			DIFFIO RX R10n DIFFIO RX R11n	DIFFOUT_R10n DIFFOUT_R11n	High_Speed High_Speed	87 86
	VREFB6N0	10	CLK2p		DIFFIO RX R14p	DIFFOUT R14p	High Speed	88
6	VREFB6N0	10	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	89
6	VREFB6N0	10	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	90
		10	CLK3n		DIFFIO RX R16n	DIFFOUT R16n	High Speed	91
		10			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	92
6	VREFB6N0 VREFB6N0	10	DPCLK3		DIFFIO_RX_R18n DIFFIO_RX_R26p	DIFFOUT_R18n DIFFOUT_R26p	High_Speed	93 96
		10	VREFB6N0		DIFFIU KA KZOP	DIFFOUT RZOP	High Speed	96
	VREFB6N0	10	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	98
	VREFB6N0	IO			DIFFIO RX R27p	DIFFOUT R27p	High Speed	99
6	VREFB6N0	10			DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	100
6	VREFB6N0	10		-	DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	101
		10			DIFFIO RX R28n	DIFFOUT R28n	High Speed	102
		10			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	105
	VREFB6N0 VREFB7N0	IO IO			DIFFIO_RX_R33n DIFFIO_RX_T1p	DIFFOUT_R33n DIFFOUT_T1p	High_Speed High_Speed	106 110
		10			DIFFIO RX 11p			110
		10	VREFB7N0		5 10. 10x 1111	5 561_1111	High_Speed	112
	VREFB7N0	10						113
7	VREFB7N0	IO						114
7	VREFB7N0	IO		·	DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	118
		10			DIFFIO RX T10n	DIFFOUT T10n	High Speed	119
		10		DEV OLD:	DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	120
8	VREFB8N0 VREFB8N0	IO IO		DEV CLRn DEV OE	DIFFIO RX T16n	DIFFOUT_T16n	Low Speed	121 122
			Į.	DEV OF	!			122
	VRFFB8N0	IIO	VRFFB8N0					123
8	VREFB8N0 VREFB8N0	10	VREFB8N0	CONFIG SEL				



Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
	8 VREFB8N0	IO			DIFFIO RX T19p	DIFFOUT_T19p	Low Speed	
	8 VREFB8N0	Input only		nCONFIG				_
	8 VREFB8N0	10			DIFFIO RX T19n	DIFFOUT T19n	Low Speed	_
	8 VREFB8N0	10			DIFFIO RX T20p	DIFFOUT T20p	Low Speed	
	8 VREFB8N0	10			DIFFIO RX T20n	DIFFOUT_T20n	Low Speed	_
	8 VREFB8N0	10			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	_
	8 VREFB8N0	10		CRC_ERROR	DIFFIO RX T22n	DIFFOUT_T22n	Low Speed	_
	8 VREFB8N0	IO						
	8 VREFB8N0	10		nSTATUS	DIFFIO RX T24p	DIFFOUT T24p	Low Speed	
	8 VREFB8N0	10		CONF_DONE	DIFFIO RX T24n	DIFFOUT_T24n	Low_Speed	_
	8 VREFB8N0	10		_	DIFFIO RX T26p	DIFFOUT_T26p	Low Speed	
	8 VREFB8N0	IO			DIFFIO RX T26n	DIFFOUT T26n	Low Speed	
		GND						
		GND					İ	_
		GND					İ	_
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		GND						
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		GND					İ	_
		GND						
		REFGND						
		VCCIO1A						
		VCCIO1B						
		VCCIO2						
		VCCIO3						
		VCCIO3						
		VCCIO4						
		VCCIO5						
		VCCIO6						
		VCCIO6						
		VCCIO7						
		VCCIO8						-
		VCCIO8						
		VCCA1						
	+	VCCA2	<u> </u>					_
	+	VCCA3	<u> </u>					_
	1	VCCA4						
	1	VCCA5						
	1	VCCA6						
		VCC_ONE						-
		VCC ONE					i i	_
	+	VCC_ONE	<u> </u>					_
	+	VCC ONE	<u> </u>					_
		VCC ONE					i i	_
	1	VCC ONE						
		VCC ONE						-
	+	VCC ONE	+					-
	+	VCC ONE	<u> </u>					_
		VCC ONE						-
	+	ADC VREF	+				-	-
	1	ANAIN1	+			+		-

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the

Intel MAX 10 FPGA Device Family Pin Connection Guidelines.

(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.



								Note (
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
A	VREFB1N0	10	ADC1IN1		DIFFIG BY LA	DIFFOUT 14-	ti ann Oanant	DO
1	VREFB1N0 VREFB1N0	10	ADC1IN1 ADC1IN2		DIFFIO_RX_L1n DIFFIO_RX_L1p	DIFFOUT_L1n DIFFOUT_L1p	Low_Speed	D2
	VREFB1N0 VREFB1N0	10	ADC1IN2 ADC1IN3		DIFFIO_RX_LIP	DIFFOUT L3n	Low_Speed Low Speed	F5
	VREFB1N0 VREFR1N0	10	ADC1IN4 ADC1IN5		DIFFIO RX L3p	DIFFOUT L3p	Low_Speed	G5 C1
	VREFB1N0	IO	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p		B1
	VREFB1N0	10	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	E1
	VREFB1N0	10	ADC1IN8		DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	E2
	VREFB1N0	IO		JTAGEN			1	G7
	VREFB1N0	10		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	G1
	VREFB1N0	IO	VREFB1N0				f	G2
	VREFB1N0	IO		TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	J1
	VREFB1N0	10		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low Speed	H5
	VREFB1N0	IO		TDO	DIFFIO RX L12p	DIFFOUT L12p		H4
	VREERINO	in		150	DIFFIO RX I 14n	DIFFOLIT I 14n	Low Speed	H3
	VREFB1N0	10			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	J2
	VREFB1N0	10			DIFFIO RX L16n	DIFFOUT L16n	Low_Speed	1.4
	VREFB1N0	10			DIFFIO RX L16p	DIFFOUT L16p	Low_Speed	K2
^	VREFBINO VRFFB2N0		Cl K0n		DIFFIO RX L18p	DIFFOUT L18n		.14
		10						.15
	VREFB2N0	2	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	riigii_opood	
2	VREFB2N0	10	CLK1n		DIFFIO RX L20n	DIFFOUT L20n		K5
2	VREFB2N0	10	CLK1p		DIFFIO RX L20p	DIFFOUT_L20p		K4
	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	L5
	VREFB2N0	10	VREFB2N0			l		P1
	VREFB2N0	10	DPCLK1		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	L4
2	VREFB2N0	10						R2
2	VREFB2N0	10	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT L27n		N1
2	VREFB2N0	IO	PLL L CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p	High Speed	P2
	VREFB3N0	10			DIFFIO TX RX B1n	DIFFOUT Bin		M4
	VREFB3N0	10			DIFFIO RX B2n	DIFFOUT B2n	High Speed	P3
	VREFB3N0	10			DIFFIO TX RX B1p	DIFFOUT_B1p		M5
	VREFB3N0	10	-		DIFFIO_TX_RX_B1p DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed High Speed	R3
	VREFB3N0 VREFB3N0	10			DIFFIO_RX_B2p DIFFIO_TX_RX_B3n	DIFFOUT B3n		L6
	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n		P4
	VREFB3N0	10			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	riigii_opood	L7
3	VREFB3N0	IO			DIFFIO RX B4p	DIFFOUT B4p		R5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	P6
3	VREFB3N0	10			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	R7
3	VREFB3N0	IO			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	P7
3	VRFFB3N0	IO			DIFFIO RX B6p	DIFFOUT B6p	High_Speed	P8
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	1.8
3	VREFB3N0	10			DIFFIO RX B8n	DIFFOUT B8n	High Speed	P9
2	VREFB3N0	10			DIFFIO TX RX B7n	DIFFOUT Bon		M7
<u> </u>	VREFB3N0	10			DIFFIO_IX_RX_B/p	DIFFOUT B8p		R9
<u> </u>		10						M8
	VREFB3N0	2) (DEEDAN)		DIFFIO TX RX B9n	DIFFOUT B9n		
3	VREFB3N0	IO	VREFB3N0					R11
3	VREFB3N0	10			DIFFIO TX RX B9p	DIFFOUT_B9p		N8
	VREFB3N0	10						P12
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n		R14
3	VREFB3N0	10			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	P15
3	VREFB3N0	10			DIFFIO TX RX B12n	DIFFOUT B12n	High Speed	L9
3	VREFB3N0	10			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High Speed	M9
3	VREFB3N0	IO			DIFFIO TX RX B14n	DIFFOUT B14n		L10
3	VREFB3N0	10			DIFFIO TX RX B14p	DIFFOUT B14p		M11
3	VREFB3N0	10			DIFFIO TX RX B16n	DIFFOUT B16n	High_Speed	P14
	VREFB3N0	10			DIFFIO_TX_RX_B16p	DIFFOUT_B16p		R13
	VREFB5N0	10	<u> </u>		DIFFIO RX R1p	DIFFOUT R1p		M12
5	VREFB5N0 VREFB5N0	10	-		DIETIO RA RIP	DIFFOUT_R2p	Ligh Speed	M12 N15
					DIFFIO_RX_R2p			
	VREFB5N0	10	<u> </u>		DIFFIO_RX_R1n	DIFFOUT_R1n		L11
5	VREFB5N0	10			DIFFIO RX R2n	DIFFOUT R2n		N14
5	VREFB5N0	10			DIFFIO RX R7p	DIFFOUT R7p	High_Speed	K11
5	VREFB5N0	10						M14
	VREFB5N0	10			DIFFIO RX R7n	DIFFOUT R7n	High Speed	K12
5	VREFB5N0	10	VREFB5N0					L15
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	J9
	VREFB5N0	10			DIFFIO RX R11p	DIFFOUT R11p	High Speed	K14
5	VREFB5N0	10			DIFFIO RX R10n	DIFFOUT_R10n	High Speed	J11
5	VREFB5N0	10	+		DIFFIO RX R11n	DIFFOUT R11n		J14
	VREFB6N0	10	CLK2p		DIFFIO_RX_RTIII	DIFFOUT R14n	High Speed	J12
	VREFB6N0	10	CLK2n		DIFFIO RX R14p	DIFFOUT R14n	High_Speed	J12 H11
6	VICEDONU						Lligh Coood	
	VREFB6N0	10	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p		H12
	VREFB6N0	IIO	CLK3n		DIFFIO RX R16n	DIFFOUT R16n		H13
	VREFB6N0	IO			DIFFIO_RX_R18p			J15
	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n		G15
6	VREFB6N0	10	DPCLK3		DIFFIO RX R26p	DIFFOUT R26p	High Speed	G11
6	VREFB6N0	10	VREFB6N0					E15
6	VREFB6N0	10	DPCLK2		DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed	G12
6	VREFB6N0	10						E14
	VREFB6N0	10			DIFFIO RX R27p	DIFFOUT_R27p		F11
	VREFB6N0	10	1		DIFFIO_RX_R28p	DIFFOUT_R28p	High_Speed	C15
6	VREFB6N0	10	<u> </u>		DIFFIO_RX_R28p DIFFIO_RX_R27n	DIFFOUT R27n	High Speed	F12
6			-		DIFFIO RX R2/h	DIFFOUT R28n		
6		10	+		DIFFIO_RX_R28n DIFFIO_RX_R33p		High_Speed	C14 E11
6	VREFB6N0				IDIEFIO RX R330	DIFFOUT_R33p	High Speed	IETT
6 6	VREFB6N0	10				DIFFOLIT DAG		
6 6 6	VREFB6N0 VREFB6N0	10			DIFFIO RX R33n	DIFFOUT R33n	High Speed	D12
6 6 6	VREFB6N0 VREFB6N0 VREFB8N0	2			DIFFIO RX R33n DIFFIO_RX_T14p	DIFFOUT_T14p	High Speed Low_Speed	D12 D11
6 6 6 6 8 8	VREFB6N0 VREFB6N0 VREFB8N0 VREFB8N0	10			DIFFIO RX R33n DIFFIO_RX_T14p DIFFIO_RX_T15p	DIFFOUT_T14p DIFFOUT_T15p	High Speed	D12 D11 B15
6 6 6 6 8 8 8	VREFB6N0 VREFB6N0 VREFB8N0 VREFB8N0 VREFB8N0	10 10 10 10			DIFFIO RX R33n DIFFIO RX_T14p DIFFIO RX_T15p DIFFIO RX_T14n	DIFFOUT_T14p DIFFOUT_T15p DIFFOUT_T14n	High Speed Low Speed Low Speed Low Speed Low Speed	D12 D11 B15 D10
6 6 6 6 8 8 8	VREFB6N0 VREFB6N0 VREFB8N0 VREFB8N0	10			DIFFIO RX R33n DIFFIO_RX_T14p DIFFIO_RX_T15p	DIFFOUT_T14p DIFFOUT_T15p	High Speed Low Speed Low Speed Low Speed Low Speed	D12 D11 B15

Pin List M153



Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	M153
Number	VKEF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated 1x/kx Channel	Emulated LVDS Output Channel	IO Performance	W153
	8 VREFB8N0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	Low Speed	B13
	8 VREFB8N0	10		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B8
	8 VREFB8N0	10			DIFFIO RX T17n	DIFFOUT T17n	Low Speed	A14
	8 VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	E10
	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	E9
	8 VREFB8N0	10	VREFB8N0					A13
	8 VREFB8N0	10		CONFIG_SEL				D8
	3 VREFB8N0	10			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	B12
	VREFB8N0	Input only		nCONFIG				E8
	VREFB8N0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	B11
	VREFB8N0	IO			DIFFIO RX T20p	DIFFOUT_T20p	Low Speed	B7
	8 VREFB8N0	10			DIFFIO RX T21p	DIFFOUT T21p	Low Speed	A9
	8 VREFB8N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B6
	8 VREFB8N0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	A11
	VREFB8N0	10			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	D7
	8 VREFB8N0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	Low_Speed	A7
	8 VREFB8N0	10		CRC_ERROR	DIFFIO_RX_T22n	DIFFOUT_T22n	Low_Speed	E7
	8 VREFB8N0	10			DIFFIO RX T23n	DIFFOUT T23n	Low Speed	A5
	VREFB8N0	10		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	D6
	8 VREFB8N0	10						B4
	8 VREFB8N0	10		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	E6
	8 VREFB8N0	IO			DIFFIO RX T26p	DIFFOUT_T26p	Low_Speed	A2
	8 VREFB8N0	10			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	A3
		GND						R15
		GND						R1
		GND						M6
		GND						M2
		GND						M10
		GND						L12
		GND						J7
		GND						H8
		GND						H14
		GND						G9
		GND						G4
		GND						E5
		GND						E12
		GND						D9
		GND						D5
		GND						B2
		GND						A15
		GND						A1
		REFGND						E4
	1	VCCIO1A						F2
	1	VCCIO1B						H2
	1	VCCIO2						L2
	1	VCCIO3						P5
	1	VCCIO3						P11
	1	VCCIO3						P10
	1	VCCIO5						L14
	1	VCCIO6						G14
	1	VCCIO6						F14
		VCCIO8						B9
		VCCIO8						B5
	1	VCCIO8						B10
	1	VCCA1						N2
		VCCA2						D14
	1	VCCA3						B3
		VCCA4						P13
	1	VCC_ONE						J8
		VCC ONE						H9
		VCC ONE						H7
		VCC_ONE						G8
		ADC VREF						F4
	1	ANAIN1						D4

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.



								Note
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
A	VREFB1N0	Ю	ADC1IN1		DIFFIO RX L1n	DIFFOUT L1n	Low Speed	D1
A	VREFB1N0	Ю	ADC1IN2		DIFFIO RX L1p	DIFFOUT L1p	Low Speed	C2
4	VREFB1N0	Ю	ADC1IN3		DIFFIO RX L3n	DIFFOUT L3n	Low Speed	E3
A	VREFB1N0	Ю	ADC1IN4		DIFFIO RX L3p	DIFFOUT L3p	Low Speed	E4
4	VREFB1N0	Ю	ADC1IN5		DIFFIO RX L5n	DIFFOUT L5n	Low Speed	C1
A	VREFB1N0	Ю	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	B1
A	VREFB1N0	Ю	ADC1IN7		DIFFIO RX L7n	DIFFOUT L7n	Low Speed	F1
A	VREFB1N0	Ю	ADC1IN8		DIFFIO RX L7p	DIFFOUT L7p	Low Speed	E1
В	VREFB1N0	IO		JTAGEN				F5
В	VREFB1N0	Ю		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	G1
B	VREFB1N0	in	VREFB1N0	Timo	Billio loc Elli	Dii 1 GOT ETIII	Low Opcou	H1
B	VREFB1N0	10	VICEI BINO	TCK	DIFFIO RX I 11p	DIFFOUT 11p	Low Speed	G2
B	VRFFB1N0	10		TDI	DIFFIO RX L11p	DIFFOUT L12n	Low Speed	F5
3	VRFFB1N0	IO		TDO	DIFFIO RX L12h	DIFFOUT L12n	Low Speed	F6
3		10		100	DIFFIO RX L12p			F4
	VREFB1N0	10				DIFFOUT L14n	Low Speed	
	VREFB1N0	Ю			DIFFIO RX L14p	DIFFOUT L14p	Low Speed	G4
	VREFB1N0	Ю			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	H2
	VREFB1N0	Ю			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	H3
2	VREFB2N0	Ю	CLK0n		DIFFIO RX L18n	DIFFOUT L18n	High Speed	G5
2	VREFB2N0	Ю			DIFFIO RX L19n	DIFFOUT L19n	High Speed	J1
2	VREFB2N0	Ю	CLK0p		DIFFIO RX L18p	DIFFOUT L18p	High Speed	H6
2	VREFB2N0	Ю			DIFFIO RX L19p	DIFFOUT I 19p	High Speed	J2
	VREEB2N0	IO	CI K1n		DIFFIO RX L20n	DIFFOLIT I 20n	High Speed	H5
	VREFB2N0	IO	T	+	DIFFIO RX L21n	DIFFOUT L21n	High Speed	M1
	VREFB2N0	lio	CLK1p	1	DIFFIO RX L20p	DIFFOUT L20p	High Speed	H4
2	VREFB2N0	10	OCIVIP	1	DIFFIO RX L20p	DIFFOUT L20p	High Speed	M2
		10	DDCI KO	+			High Speed	
2	VREFB2N0	10	DPCLK0		DIFFIO RX L22n	DIFFOUT L22n	High Speed	N2
	VREFB2N0	10	VREFB2N0	+	DIFFIO DV 1 **	DIFFOUR LOO-	Ulah On a i	L1
	VREFB2N0	Ю	DPCLK1	+	DIFFIO RX L22p	DIFFOUT L22p	High Speed	N3
	VREFB2N0	Ю	<u> </u>				- L	L2
	VREFB2N0	Ю	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT L27n	High Speed	M3
2	VREFB2N0	Ю			DIFFIO RX L28n	DIFFOUT L28n	High Speed	K1
2	VREFB2N0	Ю	PLL L CLKOUTp	1	DIFFIO RX L27p	DIFFOUT L27p	High Speed	L3
2	VREFB2N0	Ю	·		DIFFIO RX L28p	DIFFOUT L28p	High Speed	K2
3	VREFB3N0	Ю			DIFFIO TX RX B1n	DIFFOUT B1n	High Speed	15
3	VREFB3N0	in			DIFFIO RX B2n	DIFFOUT B2n	High Speed	M4
	VREFB3N0	10	1		DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	L4
	VRFFB3N0	10			DIFFIO TX RX BTD	DIFFOUT B2p	High Speed	M5
	VRFFB3N0	IO			DIFFIO TX RX B3n	DIFFOUT B2p	High Speed	K5
	VREFB3N0	Ю			DIFFIO RX B4n	DIFFOUT B4n	High Speed	N4
	VREFB3N0	Ю			DIFFIO TX RX B3p	DIFFOUT B3p	High Speed	J5
3	VREFB3N0	Ю			DIFFIO RX B4p	DIFFOUT B4p	High Speed	N5
3	VREFB3N0	Ю			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	N6
	VREFB3N0	Ю			DIFFIO RX B6n	DIFFOUT B6n	High Speed	N7
3	VREFB3N0	Ю			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	M7
	VREFB3N0	Ю			DIFFIO RX B6p	DIFFOUT B6p	High Speed	N8
	VREFB3N0	Ю			DIFFIO TX RX B7n	DIFFOUT B7n	High Speed	J6
	VREFB3N0	io			DIFFIO RX B8n	DIFFOUT B8n	High Speed	M8
	VREFB3N0	IO			DIFFIC TX RX B7n	DIFFOUT B811	High Speed	K6
		10						
3	VREFB3N0	IO IO			DIFFIO RX B8p	DIFFOUT B8p	High Speed	M9
3	VREFB3N0	IO			DIFFIO TX RX B9n	DIFFOUT B9n	High Speed	J7
3	VREFB3N0	10	VREFB3N0			<u> </u>		N11
3	VREFB3N0	Ю			DIFFIO TX RX B9p	DIFFOUT B9p	High Speed	K7
3	VREFB3N0	IO						N12
3	VREFB3N0	Ю			DIFFIO TX RX B10n	DIFFOUT B10n	High Speed	M13
3	VREFB3N0	Ю			DIFFIO RX B11n	DIFFOUT B11n	High Speed	N10
3	VREFB3N0	Ю			DIFFIO TX RX B10p	DIFFOUT B10p	High Speed	M12
	VREFB3N0	Ю			DIFFIO RX B11p	DIFFOUT B11p	High Speed	N9
3	VREFB3N0	Ю			DIFFIO TX RX B12n	DIFFOUT B12n	High Speed	M11
	VREFB3N0	10	1		DIFFIO TX RX B12p	DIFFOUT B12p	High Speed	L11
2	VREFB3N0	lio	i e	1	DIFFIO TX RX B12p	DIFFOUT B14n	High Speed	J8
	VREFB3N0	10	+	+	DIFFIO TX RX B14n	DIFFOUT B140	High Speed	K8
	VREFB3N0	10	1	+	DIFFIO TX RX B14p	DIFFOUT B14p	High Speed	M10
	VREFB3N0	10	+	+	DIFFIO TX RX B16n	DIFFOUT B16p	High Speed	I 10
		10	+					
	VREFB5N0		+	+	DIFFIO RX R1p	DIFFOUT R1p	High Speed	K10
	VREFB5N0	Ю			DIFFIO RX R2p	DIFFOUT R2p	High Speed	K11
5	VREFB5N0	Ю	1	1	DIFFIO RX R1n	DIFFOUT R1n	High Speed	J10
5	VREFB5N0	Ю		<u> </u>	DIFFIO RX R2n	DIFFOUT R2n	High Speed	L12
5	VREFB5N0	Ю			DIFFIO RX R7p	DIFFOUT R7p	High Speed	K12
5	VREFB5N0	Ю		<u> </u>				L13
5	VREFB5N0	Ю			DIFFIO RX R7n	DIFFOUT R7n	High Speed	J12
	VREFB5N0	Ю	VREFB5N0		i			K13
	VREFB5N0	10			DIFFIO RX R8p	DIFFOUT R8p	High Speed	J9
	VREFB5N0	IO	i e	1	DIFFIO RX R9p	DIFFOUT R9p	High Speed	J13
	VREFB5N0	10	i e	1	DIFFIO RX R8n	DIFFOUT R8n	High Speed	H10
5	VREFB5N0	10	†	1	DIFFIO RX R8II	DIFFOUT R9n	High Speed	H13
5		10	+	+			High Coast	1113
5	VREFB5N0	10	+		DIFFIO RX R10p	DIFFOUT R10p	High Speed	
5	VREFB5N0	IO	+	+		DIFFOUT R11p	High Speed	G13
	VREFB5N0	IO	+	1	DIFFIO RX R10n	DIFFOUT R10n	High Speed	H8
	VREFB5N0	Ю	1	1	DIFFIO RX R11n	DIFFOUT R11n	High Speed	G12
	VREFB6N0	Ю	CLK2p		DIFFIO RX R14p	DIFFOUT R14p	High Speed	G9
6	VREFB6N0	Ю	CLK2n		DIFFIO RX R14n	DIFFOUT R14n	High Speed	G10
6	VREFB6N0	Ю	CLK3p		DIFFIO RX R16p	DIFFOUT R16p	High Speed	F13
	VREFB6N0	IO	CLK3n	1	DIFFIO RX R16n	DIFFOUT R16n	High Speed	E13
	VREFB6N0	10		1	DIFFIO RX R18p	DIFFOUT R18p	High Speed	F12
		10	+	+	DIFFIO RX R18p	DIFFOUT RIOP	High Coast	
	VREFB6N0	10	DDOLKO	+		DIFFOUT R18n	High Speed	E12
	VREFB6N0	IO	DPCLK3	+	DIFFIO RX R26p	DIFFOUT R26p	High Speed	F9
	VREFB6N0	Ю	VREFB6N0				ļ	D13
6	VREFB6N0	Ю	DPCLK2		DIFFIO RX R26n	DIFFOUT R26n	High Speed	F10
		0		1				C13
	VREFB6N0 VRFFB6N0	IO			DIFFIO RX R27p	DIFFOUT R27p	High Speed	F8



umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
	6 VREFB6N0	Ю	1		DIFFIO RX R28p	DIFFOUT R28p	High Speed	B12
	6 VREFB6N0	IO			DIFFIO RX R27n	DIFFOUT R27n	High Speed	E9
	6 VREFB6N0	Ю			DIFFIO RX R28n	DIFFOUT R28n	High Speed	B11
	6 VREFB6N0	Ю			DIFFIO RX R29p	DIFFOUT R29p	High Speed	C12
	6 VREFB6N0	IO			DIFFIO RX R30p	DIFFOUT R30p	High Speed	B13
	6 VREFB6N0	10			DIFFIO RX R29n	DIFFOUT R29n	High Speed	C11
	6 VREFB6N0	10			DIFFIO RX R30n	DIFFOUT R30n	High Speed	A12
	6 VREFB6N0 6 VREFB6N0	10			DIFFIO RX R31p DIFFIO RX R31n	DIFFOUT R31p DIFFOUT R31n	High Speed	E10 D9
	6 VREFB6N0	IO IO			DIFFIO RX R31II	DIFFOUT R33p	High Speed High Speed	D12
	6 VREFB6N0	10	+		DIFFIO RX R33p	DIFFOUT R33p	High Speed	D12
	8 VREFB8N0	10	1		DIFFIO RX R33II	DIFFOUT T14p	Low Speed	C10
	8 VREFB8N0	10			DIFFIO RX T15p	DIFFOUT T15p	Low Speed	A8
	8 VREFB8N0	10			DIFFIO RX T14n	DIFFOUT T14n	Low Speed	C9
	8 VREFB8N0	10			DIFFIO RX T15n	DIFFOUT T15n	Low Speed	A9
	8 VREFB8N0	IO			DIFFIO RX T16p	DIFFOUT T16p	Low Speed	B10
	8 VREFB8N0	10			DIFFIO RX T17p	DIFFOUT T17p	Low Speed	A10
	8 VREFB8N0	Ю		DEV CLRn	DIFFIO RX T16n	DIFFOUT T16n	Low Speed	B9
	8 VREFB8N0	Ю			DIFFIO RX T17n	DIFFOUT T17n	Low Speed	A11
	8 VREFB8N0	Ю		DEV OE	DIFFIO RX T18p	DIFFOUT T18p	Low Speed	D8
	8 VREFB8N0	IO			DIFFIO RX T18n	DIFFOUT T18n	Low Speed	E8
	8 VREFB8N0	IO	VREFB8N0					B7
	8 VREFB8N0	IO		CONFIG SEL				D7
	8 VREFB8N0	Ю			DIFFIO RX T19p	DIFFOUT T19p	Low Speed	A7
	8 VREFB8N0	Input only		nCONFIG				E7
	8 VREFB8N0	Ю			DIFFIO RX T19n	DIFFOUT T19n	Low Speed	A6
	8 VREFB8N0	Ю			DIFFIO RX T20p	DIFFOUT T20p	Low Speed	B6
	8 VREFB8N0	Ю			DIFFIO RX T21p	DIFFOUT T21p	Low Speed	A4
	8 VREFB8N0	Ю			DIFFIO RX T20n	DIFFOUT T20n	Low Speed	B5
	8 VREFB8N0	IO			DIFFIO RX T21n	DIFFOUT T21n	Low Speed	A3
	8 VREFB8N0	Ю			DIFFIO RX T22p	DIFFOUT T22p	Low Speed	E6
	8 VREFB8N0	Ю			DIFFIO RX T23p	DIFFOUT T23p	Low Speed	B3
	8 VREFB8N0	IO		CRC ERROR	DIFFIO RX T22n	DIFFOUT T22n	Low Speed	D6
	8 VREFB8N0	IO	_		DIFFIO RX T23n	DIFFOUT T23n	Low Speed	B4
	8 VREFB8N0	IO		nSTATUS	DIFFIO RX T24p	DIFFOUT T24p	Low Speed	C4
	8 VREFB8N0	IO	_					A5
	8 VREFB8N0	IO .		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	C5
	8 VREFB8N0 8 VREFB8N0	IO IO			DIFFIO RX T26p	DIFFOUT T26p DIFFOUT T26n	Low Speed	A2
	B VREFB8N0				DIFFIO RX T26n	DIFFOUT 126n	Low Speed	B2
		GND						N13
		GND						N1 M6
		GND GND						1 9
		GND						J4
	1	GND	+					H12
	+	GND						G7
	+	GND	+					F3
		GND						F11
	+	GND	+					D5
		GND						C3
		GND			<u> </u>	T T		B8
		GND			<u> </u>	T T		A13
		GND	1	The state of the s	1			A1
		REFGND			<u> </u>	T T		E2
		VCCIO1A						F2
		VCCIO1B						G3
		VCCIO2						K3
		VCCIO2						J3
		VCCIO3						L8
		VCCIO3						L7
		VCCIO3			-			L6
		VCCIO5						J11
		VCCIO5						H11
		VCCIO6						G11
		VCCIO6						F11
		VCCIO8						C8
		VCCIO8						C7
		VCCIO8						C6
		VCCA1						K4
		VCCA2						D10
		VCCA3						D4
		VCCA4						K9
		VCC ONE						H7
		VCC ONE						G8
		VCC ONE						G6
		VCC ONE						F7
		ADC VREF	_					D3
	1	ANAIN1	i	1	1	i e	1	D2

(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
Α	VRFFB1N0	In	ADC1IN1		DIFFIO RX L1n	DIFFOUT L1n	Low_Speed	D4
A	VREFB1N0	10	ADC1IN9		DIFFIO_RX_L2n	DIFFOUT L2n	Low Speed	C2
A	VREFB1N0	IO	ADC1IN2		DIFFIO RX L1p	DIFFOUT L1p	Low Speed	E4
A	VREFB1N0	10	ADC1IN16		DIFFIO RX L2p	DIFFOUT L2p	Low_Speed	D2
	VREFB1N0	10	ADC1IN3		DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	G6
A	VREFB1N0	10	ADC1IN11		DIFFIO RX L4n	DIFFOUT L4n		B1
A A	VREFB1N0 VREFB1N0	IO IO	ADC1IN4 ADC1IN12		DIFFIO_RX_L3p DIFFIO_RX_L4p	DIFFOUT_L3p DIFFOUT_L4p	Low_Speed Low Speed	H6 C1
	VREFBINO VRFFB1N0	IO	ADC1IN12 ADC1IN5		DIFFIO_RX_L4p	DIFFOUT L5n	Low_Speed	F5
A	VREFB1N0	IO	ADC1IN3		DIFFIO_RX_L6n	DIFFOUT L6n		D1
A	VREFB1N0	10	ADC1IN6		DIFFIO RX L5p	DIFFOUT_L5p	Low_Speed	E5
A	VREFB1N0	10	ADC1IN14		DIFFIO RX L6p	DIFFOUT L6p	Low Speed	E1
A	VREFB1N0	IO	ADC1IN7		DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	G3
	VREFB1N0	10	ADC1IN15		DIFFIO_RX_L8n	DIFFOUT_L8n		F1
	VREFB1N0	10	ADC1IN8		DIFFIO RX L7p	DIFFOUT L7p	Low Speed	F2
A	VREFB1N0	10	ADC1IN10		DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	G1
B B	VREFB1N0 VREFB1N0	10			DIFFIO_RX_L9n DIFFIO_RX_L10n	DIFFOUT_L9n DIFFOUT_L10n	Low_Speed	G7 H2
B R	VREFB1N0 VREFR1N0	10		JTAGEN	DIFFIO RX L10h	DIFFOUT LION		HZ H7
В	VREFB1N0	10		JIAGEN	DIFFIO_RX_L10p	DIFFOUT_L10p	Low_Speed	H1
В	VREFB1N0	10		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	J7
	VREFB1N0	10	VREFB1N0	11110			Low Speed	J3
В	VREFB1N0	Ю		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	J8
В	VREFB1N0	10						J4
В	VREFB1N0	10		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	H3
	VREFB1N0	10			DIFFIO_RX_L13n	DIFFOUT_L13n		J2
	VREFB1N0	10		TDO	DIFFIO RX L12p	DIFFOUT L12p		H4
3	VREFB1N0	10			DIFFIO_RX_L13p	DIFFOUT_L13p		J1
3	VREFB1N0 VREFB1N0	IO IO			DIFFIO RX L14n DIFFIO RX L15n	DIFFOUT L14n		J6 K2
3	VREFB1N0 VREFB1N0	10			DIFFIO RX L15h	DIFFOUT_L15n DIFFOUT_L14p	Low Speed Low_Speed	K7
	VREFBINO VRFFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L15p		K1
	VREFB1N0	IO			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	K4
	VREFB1N0	IO			DIFFIO_RX_L17n	DIFFOUT L17n	Low_Speed	L1
3	VREFB1N0	10			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	K3
3	VREFB1N0	IO			DIFFIO RX L17p	DIFFOUT L17p	Low Speed	L2
	VREFB2N0	10	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	L3
	VREFB2N0	10			DIFFIO_RX_L19n	DIFFOUT_L19n		M1
2	VREFB2N0	10	CLK0p		DIFFIO RX L18p	DIFFOUT L18p		M3
	VREFB2N0	10	Cl K1n		DIFFIO_RX_L19p DIFFIO_RX_L20n	DIFFOUT_L19p		M2 K8
		10	CLK1n		DIFFIO_RX_L20n DIFFIO_RX_L21n	DIFFOUT L21n		N1
	VREFB2N0 VREFB2N0	10	CLK1p		DIFFIO RX L2111 DIFFIO_RX_L20p	DIFFOUT_L20p		L8
	VREFB2N0	10	CERTP		DIFFIO RX L21p	DIFFOUT_L21p	High_Speed	P1
	VREFB2N0	10	DPCLK0		DIFFIO RX L22n	DIFFOUT L22n		M4
2	VREFB2N0	IO	VREFB2N0					R1
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L22p	DIFFOUT L22p	High_Speed	N3
2	VREFB2N0	10					High Speed	R2
	VREFB2N0	10			DIFFIO_RX_L23n	DIFFOUT_L23n		R3
	VREFB2N0	10			DIFFIO_RX_L24n	DIFFOUT_L24n		P2
		10			DIFFIO RX L23p	DIFFOUT L23p	High Speed	T3
	VREFB2N0 VREFB2N0	10			DIFFIO_RX_L24p DIFFIO_RX_L25n	DIFFOUT_L24p DIFFOUT_L25n	High_Speed High Speed	P3 L7
	VREFB2N0	IO			DIFFIO_RX_L25II	DIFFOUT L26n		T1
	VREFB2N0	10			DIFFIO RX L25p	DIFFOUT_L25p		M7
	VREFB2N0	10			DIFFIO_RX_L26p	DIFFOUT_L26p	High_Speed	T2
2	VREFB2N0	10	PLL L CLKOUTn		DIFFIO RX L27n	DIFFOUT L27n	High Speed	N4
2	VREFB2N0	IO			DIFFIO_RX_L28n	DIFFOUT_L28n	High_Speed	U1
		IO	PLL_L_CLKOUTp		DIFFIO_RX_L27p	DIFFOUT_L27p		P4
	VREFB2N0	10			DIFFIO RX L28p	DIFFOUT L28p		U2
	VREFB3N0	10			DIFFIO TX RX B1n	DIFFOUT Bin		R4
	VREFB3N0 VREFB3N0	10			DIFFIO_RX_B2n DIFFIO_TX_RX_B1p	DIFFOUT_B2n DIFFOUT_B1p	High_Speed	U3 T4
	VREFB3N0 VREFB3N0	10			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed High Speed	T4 V2
	VREFB3N0	10			DIFFIO_RX_B2p	DIFFOUT B3n		V2 P6
	VREFB3N0	10			DIFFIO RX B4n	DIFFOUT B4n	High Speed	V3
	VREFB3N0	IO			DIFFIO TX RX B3p	DIFFOUT_B3p		P5
	VREFB3N0	10			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	V4
	VREFB3N0	IO			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	R5
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	U5
3	VREFB3N0	10			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	R6
3	VREFB3N0	10			DIFFIO RX B6p	DIFFOUT B6p		V5
		IO	l .		DIFFIO_TX_RX_B7n DIFFIO_RX_B8n	DIFFOUT_B7n	High_Speed	T5
	VREFB3N0					DIFFOUT B8n	High_Speed	T7 T6
3	VREFB3N0	IO					Lligh Coood	
3	VREFB3N0 VREFB3N0	IO IO			DIFFIO TX RX B7p	DIFFOUT B7p	High Speed	TR
3 3	VREFB3N0 VREFB3N0 VREFB3N0	IO IO IO			DIFFIO TX RX B7p DIFFIO_RX_B8p	DIFFOUT B7p DIFFOUT_B8p	High_Speed	T8
3 3 3	VREFB3N0 VREFB3N0	IO IO	VRFFB3N0		DIFFIO TX RX B7p	DIFFOUT B7p	High_Speed High_Speed	T8 N7 U6
3 3 3 3	VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0	10 10 10 10 10	VREFB3N0		DIFFIO TX RX B7p DIFFIO RX B8p DIFFIO TX RX B9n	DIFFOUT B7p DIFFOUT B8p DIFFOUT B9n	High_Speed High_Speed High Speed	T8 N7 U6
3 3 3 3 3	VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0	10 10 10 10	VREFB3N0		DIFFIO TX RX B7p DIFFIO_RX_B8p	DIFFOUT B7p DIFFOUT_B8p	High_Speed High_Speed High Speed High Speed	T8 N7
3 3 3 3 3 3 3	VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0	10 10 10 10 10 10	VREFB3N0		DIFFIO TX RX B7p DIFFIO RX B8p DIFFIO TX RX B9n	DIFFOUT B7p DIFFOUT B8p DIFFOUT B9n	High_Speed High_Speed High_Speed High_Speed High_Speed	T8 N7 U6 N8
3 3 3 3 3 3 3 3 3	VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3NO VREFB3NO VREFB3NO	10 10 10 10 10 10 10 10 10	VREFB3N0		DIFFIO TX RX B7p DIFFIO RX B8p DIFFIO TX RX B9n DIFFIO TX RX B9n DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO RX, B11n	DIFFOUT B7D DIFFOUT B8D DIFFOUT B9D DIFFOUT B9D DIFFOUT B1DD DIFFOUT B1DD DIFFOUT B1DD	High_Speed High_Speed High Speed High Speed High_Speed High_Speed High_Speed High_Speed High_Speed	T8 N7 U6 N8 V6 R8 U7
3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0	O	VREFB3N0		DIFFIO TX RX B7p DIFFIO TX RX B8p DIFFIO TX RX B9n DIFFIO TX RX B9n DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO TX RX B10n	DIFFOUT BYD DIFFOUT BBD DIFFOUT BBD DIFFOUT BBD DIFFOUT B10n DIFFOUT B11n DIFFOUT B11n DIFFOUT B11n DIFFOUT B11n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T8 N7 U6 N8 V6 R8 U7
3 3 3 3 3 3 3 3 3 3 3 3	VREFB3N0 VREEB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0 VREFB3N0	O	VREFB3N0		DIFFIO TX RX B7p DIFFIO TX RX B7p DIFFIO TX RX B9p DIFFIO TX RX B9n DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B11p	DIFFOUT B7D DIFFOUT B8D DIFFOUT B9D DIFFOUT B1D DIFFOUT B1D DIFFOUT B1D DIFFOUT B1D DIFFOUT B1D DIFFOUT B1D	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T8 N7 U6 N8 V6 R8 U7 R9
3 3 3 3 3 3 3 3 3 3 3 3 3	VREEB3NO VREFB3NO VREFB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO	O	VREFB3N0		DIFFIO TX RX B7p DIFFIO TX RX B8p DIFFIO TX RX B9p DIFFIO TX RX B9p DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO TX RX B11n DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B11p DIFFIO TX RX B11p	DIFFOUT BYD DIFFOUT BBD DIFFOUT BBD DIFFOUT BBD DIFFOUT B10n DIFFOUT B11n DIFFOUT B11n DIFFOUT B11p DIFFOUT B11p DIFFOUT B11p DIFFOUT B11p DIFFOUT B12n	High, Speed High, Speed High, Speed High Speed High Speed High, Speed High, Speed High, Speed High, Speed High, Speed High, Speed High, Speed High, Speed	T8 N7 U6 N8 V6 R8 U7 R9 V7 V9
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0 VREEB3N0	O	VREFB3N0		DIFFIO TX RX B7p DIFFIO TX RX B8p DIFFIO TX RX B9p DIFFIO TX RX B9p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B11p DIFFIO TX RX B11p DIFFIO TX RX B11p DIFFIO TX RX B12p DIFFIO TX RX B12p DIFFIO TX RX B13p	DIFFOUT BYD DIFFOUT BSD DIFFOUT BSD DIFFOUT BSD DIFFOUT BSD DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION DIFFOUT BION	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T8 N7 U6 N8 V6 R8 U7 R9 V7 V9 U8
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREEB3NO VREFB3NO VREFB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO VREEB3NO	O	VREFB3N0		DIFFIO TX RX B7p DIFFIO TX RX B8p DIFFIO TX RX B9p DIFFIO TX RX B9p DIFFIO TX RX B10n DIFFIO TX RX B10n DIFFIO TX RX B11n DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B10p DIFFIO TX RX B11p DIFFIO TX RX B11p	DIFFOUT BYD DIFFOUT BBD DIFFOUT BBD DIFFOUT BBD DIFFOUT B10n DIFFOUT B11n DIFFOUT B11n DIFFOUT B11p DIFFOUT B11p DIFFOUT B11p DIFFOUT B11p DIFFOUT B12n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T8 N7 U6 N8 V6 R8 U7 R9 V7 V9



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
3	VREFB3N0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	High Speed	V10
	VREFB3N0	10			DIFFIO TX RX B14p	DIFFOUT B14p	High_Speed	M9
3	VREFB3N0	Ю			DIFFIO RX B15p	DIFFOUT B15p	High Speed	V11
3	VREFB3N0	10			DIFFIO TX RX B16n	DIFFOUT_B16n	High_Speed	T9
	VREFB3N0 VREFB3N0	10			DIFFIO_RX_B17n DIFFIO_TX_RX_B16n	DIFFOUT_B17n DIFFOUT_B16p	High_Speed High_Speed	V12 T10
	VREFB3N0 VREFB3N0	10			DIFFIO IX RX B16p	DIFFOUT B15p	High_Speed High_Speed	110
	VREFB4N0	10			DIFFIO TX RX B18n	DIFFOUT B18n	High Speed	P10
4	VREFB4N0	IO			DIFFIO RX B19n	DIFFOUT B19n	High Speed	U12
	VREFB4N0	10			DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed	N11
	VREFB4N0	IO.			DIFFIO RX B19p	DIFFOUT B19p	High_Speed	U13
	VREFB4N0 VREFB4N0	10	VREFB4N0		DIFFIO TX RX B20n	DIFFOUT B20n	High Speed High_Speed	M10 T11
4	VREFB4N0	10	VKEI B4N0		DIFFIO TX RX B20p	DIFFOUT_B20p	High_Speed	L10
	VREFB4N0	10			51110_1X_1X_520p		High Speed	T12
4	VREFB4N0	IO			DIFFIO_TX_RX_B21n	DIFFOUT_B21n	High_Speed	R10
	VREFB4N0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	High_Speed	V13
4	VREFB4N0 VREFB4N0	IO IO			DIFFIO TX RX B21p DIFFIO RX B22p	DIFFOUT B21p DIFFOUT B22p	High Speed High_Speed	R11 V14
	VREFB4N0	10			DIFFIO_RX_B22p	DIFFOUT B23n	High Speed	R12
	VREFB4N0	10			DIFFIO RX B24n	DIFFOUT B24n		T13
4	VREFB4N0	IO			DIFFIO TX RX B23p	DIFFOUT B23p	High_Speed	R13
4	VREFB4N0	10			DIFFIO_RX_B24p	DIFFOUT_B24p	High_Speed	T14
	VREFB4N0	10			DIFFIO TX RX B25n	DIFFOUT B25n	High Speed	R14
4	VREFB4N0 VREFB4N0	10			DIFFIO_RX_B26n DIFFIO_TX_RX_B25p	DIFFOUT_B26n DIFFOUT_B25p	High_Speed High_Speed	V15 T15
	VREFB4N0	10	<u> </u>		DIFFIO_TX_RX_B25p	DIFFOUT B26p	High Speed	U15
	VREFB4N0	10			DIFFIO_TX_RX_B27n	DIFFOUT_B27n	High_Speed	U16
4	VREFB4N0	10			DIFFIO_RX_B28n	DIFFOUT_B28n	High_Speed	V16
	VREFB4N0	10			DIFFIO TX RX B27p	DIFFOUT B27p	High Speed	U17
	VREFB4N0 VREFB5N0	10			DIFFIO_RX_B28p DIFFIO_RX_R1p	DIFFOUT_B28p DIFFOUT_R1p	High_Speed	V17 N14
	VREFB5N0	10	 		DIFFIO_RX_R1p DIFFIO_RX_R2p	DIFFOUT R2p	High_Speed High Speed	T16
5	VREFB5N0	IO			DIFFIO RX R1n	DIFFOUT_R1n	High_Speed	P14
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	R16
	VREFB5N0	IO			DIFFIO RX R3p	DIFFOUT R3p		M12
	VREFB5N0 VREFB5N0	10			DIFFIO_RX_R4p DIFFIO_RX_R3n	DIFFOUT_R4p DIFFOUT_R3n	High_Speed	U18 M11
	VREFB5N0	10			DIFFIO_RX_R3II	DIFFOUT R4n	High_Speed High Speed	T18
	VREFB5N0	10			DIFFIO RX R5p	DIFFOUT_R5p	High_Speed	N15
		Ю			DIFFIO_RX_R6p	DIFFOUT_R6p	High_Speed	N16
5	VREFB5N0	10			DIFFIO RX R5n	DIFFOUT R5n	High Speed	M15
5	VREFB5N0 VREFB5N0	10			DIFFIO_RX_R6n DIFFIO_RX_R7p	DIFFOUT_R6n DIFFOUT_R7p	High_Speed High_Speed	M16 R15
	VREFB5N0	10			DIFFIO_RX_R/p	DIFFOUT_R/p	High_Speed High Speed	P16
	VREFB5N0	10			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	P15
5	VREFB5N0	IO	VREFB5N0				High_Speed	P17
5	VREFB5N0	10			DIFFIO RX R8p	DIFFOUT R8p	High Speed	L12
	VREFB5N0	10			DIFFIO_RX_R9p	DIFFOUT_R9p DIFFOUT_R8n	High_Speed	T17
5	VREFB5N0 VREFB5N0	10			DIFFIO_RX_R8n DIFFIO_RX_R9n	DIFFOUT_R8n	High_Speed High Speed	L11 R17
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	L15
5	VREFB5N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	L16
	VREFB5N0	10			DIFFIO RX R10n	DIFFOUT R10n	High Speed	K15
	VREFB5N0	10			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	K16 R18
		10			DIFFIO_RX_R12p	DIFFOUT_R12p	High_Speed	
5	VREFB5N0 VREFB5N0	10			DIFFIO_RX_R13p DIFFIO_RX_R12n	DIFFOUT_R13p DIFFOUT_R12n	High Speed High_Speed	N18 P18
5	VREFB5N0	10			DIFFIO_RX_R13n	DIFFOUT_R13n	High_Speed	M18
6	VREFB6N0	10	CLK2p		DIFFIO RX R14p	DIFFOUT R14p	High Speed	K12
	VREFB6N0	10	la ve	-	DIFFIO RX R15p	DIFFOUT_R15p	High Speed	M17
6	VREFB6N0 VREFB6N0	10	CLK2n		DIFFIO_RX_R14n DIFFIO_RX_R15n	DIFFOUT_R14n DIFFOUT_R15n	High_Speed	K11 L18
	VREFB6N0 VREFB6N0	10	CLK3p		DIFFIO RX R15n	DIFFOUT R15n	High Speed High Speed	L18 L17
	VREFB6N0	10	oc. top		DIFFIO_RX_R16p	DIFFOUT_R17p	High_Speed	K18
6	VREFB6N0	10	CLK3n		DIFFIO RX R16n	DIFFOUT R16n	High Speed	K17
	VREFB6N0	10		·	DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed	J18
6	VREFB6N0	10			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	H18
	VREFB6N0 VREFB6N0	10			DIFFIO RX R19p DIFFIO RX R18n	DIFFOUT R19p DIFFOUT R18n	High Speed High Speed	H17 G18
	VREFB6N0	10	İ		DIFFIO_RX_R18II	DIFFOUT R19n	High_Speed	G17
	VREFB6N0	IO			DIFFIO RX R20p	DIFFOUT R20p	High Speed	J11
6	VREFB6N0	10			DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed	J12
6		10			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	J15
	VREFB6N0	10			DIFFIO RX R23p	DIFFOUT R23p	High Speed High Speed	J16 H15
6	V/REEBSNO		1		DIFFIO_RX_R22n DIFFIO_RX_R23n	DIFFOUT_R22n	High_Speed	H16
6	VREFB6N0 VREFB6N0	IO						H11
6	VREFB6N0	IO IO	DPCLK3		DIFFIO RX R26p	DIFFOUT R26D	High Speed	
6 6 6 6	VREFB6N0 VREFB6N0 VREFB6N0	IO IO	DPCLK3 VREFB6N0		DIFFIO RX R26p	DIFFOUT R26p	High Speed	F18
6 6 6 6	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	IO IO IO			DIFFIO_RX_R26p DIFFIO_RX_R26n	DIFFOUT_R26n	High_Speed High_Speed	H12
6 6 6 6 6	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	10 10 10 10	VREFB6N0		DIFFIO_RX_R26n	DIFFOUT_R26n	High Speed High Speed High Speed	H12 E18
6 6 6 6 6 6 6	VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0 VREFB6N0	IO IO IO	VREFB6N0		DIFFIO_RX_R26n DIFFIO_RX_R27p	DIFFOUT_R26n DIFFOUT_R27p	High Speed High Speed High Speed High Speed High Speed	H12 E18 F15
6 6 6 6 6 6 6	VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO	10 10 10 10 10 10	VREFB6N0		DIFFIO_RX_R26n	DIFFOUT_R26n DIFFOUT_R27p DIFFOUT_R28p	High Speed High Speed High Speed	H12 E18 F15 G16
66 66 66 66 66 66 66	VREFB6N0	10 10 10 10	VREFB6N0		DIFFIO_RX_R26n DIFFIO_RX_R27p DIFFIO_RX_R28p DIFFIO_RX_R27n DIFFIO_RX_R28n	DIFFOUT_R26n DIFFOUT_R27p DIFFOUT_R28p DIFFOUT_R27n DIFFOUT_R28n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	H12 E18 F15 G16 G15 F16
66 66 66 66 66 66 66 66	VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO	10 10 10 10 10 10 10 10 10	VREFB6N0		DIFFIO RX R26n DIFFIO RX R27p DIFFIO RX R28p DIFFIO RX R27n DIFFIO RX R28n DIFFIO RX R29p	DIFFOUT_R25n DIFFOUT_R27p DIFFOUT_R28p DIFFOUT_R27n DIFFOUT_R28n DIFFOUT_R28n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	H12 E18 F15 G16 G15 F16 E16
66 66 66 66 66 66 66 66 66	VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO VREFB6NO	10 10 10 10 10 10 10 10	VREFB6N0		DIFFIO_RX_R26n DIFFIO_RX_R27p DIFFIO_RX_R28p DIFFIO_RX_R27n DIFFIO_RX_R28n	DIFFOUT_R25n DIFFOUT_R27p DIFFOUT_R28p DIFFOUT_R27n DIFFOUT_R27n DIFFOUT_R28n DIFFOUT_R28p	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	H12 E18 F15 G16 G15 F16



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
	6 VREFB6N0	10			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed	G11
	6 VREFB6N0	10			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	C18
	6 VREFB6N0 6 VREFB6N0	IO IO			DIFFIO_RX_R31n DIFFIO_RX_R32n	DIFFOUT_R31n DIFFOUT_R32n	High Speed High Speed	G12 B18
	6 VREFB6N0	10			DIFFIO RX R32II DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	E15
	6 VREFB6N0	IO			DIFFIO RX R34p		High Speed	D17
		10			DIFFIO RX R33n	DIFFOUT R33n	High_Speed	D15
	6 VREFB6N0	10			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed	C17
	7 VREFB7N0	10			DIFFIO RX T1p	DIFFOUT T1p	High Speed	E14
	7 VREFB7N0	10			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed	B17
	7 VREFB7N0	10			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	D14
		10			DIFFIO RX T2n	DIFFOUT T2n	High Speed	B16
		IO IO			DIFFIO_RX_T3p	DIFFOUT_T3p	High_Speed	D12
	7 VREFB7N0 7 VREFB7N0	10			DIFFIO RX T3n	DIFFOUT T3n	High_Speed High Speed	A17 D13
	7 VREFB7N0	10	VREFB7N0		DIFFIO RX 13II	DIFFOOT TSIT	High_Speed	A16
	7 VREFB7N0	10	VICE BING		DIFFIO_RX_T4p	DIFFOUT_T4p	High_Speed	C16
		10			DIFFIO RX T5p		High Speed	A15
	7 VREFB7N0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	High_Speed	C15
	7 VREFB7N0	10			DIFFIO_RX_T5n	DIFFOUT_T5n	High_Speed	A14
		10			DIFFIO RX T6p	DIFFOUT T6p	High Speed	C14
	7 VREFB7N0	10			DIFFIO RX T7p	DIFFOUT_T7p	High_Speed	B14
		IO			DIFFIO_RX_T6n	DIFFOUT_T6n	High_Speed	C13
		10	ļ		DIFFIO RX T7n	DIFFOUT T7n	High Speed	B13
	7 VREFB7N0 7 VREFB7N0	10			DIFFIO_RX_T8p DIFFIO_RX_T9p	DIFFOUT_T8p DIFFOUT_T9p	High_Speed	F11 C12
	7 VREFB7N0 7 VREFB7N0	10	 		DIFFIO_RX_19p DIFFIO_RX_T8n		High_Speed High Speed	C12 F12
		10			DIFFIO RX 1811 DIFFIO_RX_T9n	DIFFOUT_T9n	High_Speed	B12
	7 VREFB7N0	10	†		DIFFIO_RX_19II	DIFFOUT_T10p	High_Speed	C11
	7 VREFB7N0	10			DIFFIO RX T11p	DIFFOUT T11p	High Speed	A13
		IO			DIFFIO_RX_T10n		High_Speed	B11
	7 VREFB7N0	10			DIFFIO_RX_T11n	DIFFOUT_T11n	High_Speed	A12
		10			DIFFIO RX T12p	DIFFOUT T12p	Low Speed	D10
	8 VREFB8N0	10			DIFFIO_RX_T13p	DIFFOUT_T13p	Low_Speed	A11
	8 VREFB8N0	IO			DIFFIO_RX_T12n	DIFFOUT_T12n	Low_Speed	D9
	8 VREFB8N0 8 VREFB8N0	10			DIFFIO RX T13n DIFFIO RX T14n	DIFFOUT T13n DIFFOUT T14n	Low Speed	A10 F10
	8 VREFB8N0	10			DIFFIO_RX_T14p	DIFFOUT_T15p	Low_Speed	F10
	8 VREFB8N0	10			DIFFIO_RX_113p	DIFFOUT T14n	Low_Speed Low Speed	G10
	8 VREFB8N0	10			DIFFIO RX T15n	DIFFOUT_T15n	Low_Speed	A8
	8 VREFB8N0	10			DIFFIO RX T16p	DIFFOUT T16p	Low Speed	B9
	8 VREFB8N0	10			DIFFIO RX T17p	DIFFOUT T17p	Low Speed	C10
		10		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B8
	8 VREFB8N0	10			DIFFIO_RX_T17n	DIFFOUT_T17n	Low_Speed	C9
		10		DEV OE	DIFFIO RX T18p	DIFFOUT T18p	Low Speed	D8
		10			DIEELO DV TIA	DIFFOLIT TAR	Low_Speed	A7
	8 VREFB8N0 8 VREFB8N0	IO IO	VREFB8N0		DIFFIO RX T18n	DIFFOUT_T18n	Low Speed	D7 B7
	8 VREFB8N0	10	VKEFBONU	CONFIG SEL			Low Speed Low Speed	G9
		10		CONTIG_SEE	DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	A6
		Input only		nCONFIG	Bir rio_rix_riop	5111 GG1_110p	Low Speed	H9
	8 VREFB8N0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	A5
	8 VREFB8N0	10			DIFFIO_RX_T20p	DIFFOUT_T20p	Low_Speed	C6
		10			DIFFIO RX T21p	DIFFOUT T21p	Low Speed	C8
		10			DIFFIO_RX_T20n	DIFFOUT_T20n	Low_Speed	B5
		IO			DIFFIO_RX_T21n	DIFFOUT_T21n	Low_Speed	C7
	8 VREFB8N0	10	ļ		DIFFIO RX T22p	DIFFOUT T22p	Low Speed	C5 A4
	8 VREFB8N0 8 VREFB8N0	10	 	CRC ERROR	DIFFIO_RX_T23p DIFFIO_RX_T22n	DIFFOUT_T23p DIFFOUT_T22n	Low_Speed Low Speed	A4 C4
		10		UNU_ENNON	DIFFIO_RX_122n	DIFFOUT T23n	Low_Speed Low Speed	B4
	8 VREFB8N0	10		nSTATUS	DIFFIO RX 12311 DIFFIO RX T24p	DIFFOUT_T24p	Low Speed	G8
	8 VREFB8N0	10			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed	A3
	8 VREFB8N0	IO		CONF DONE	DIFFIO RX T24n	DIFFOUT T24n	Low Speed	H8
	8 VREFB8N0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	Low_Speed	B3
	8 VREFB8N0	10			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	D6
		10			DIFFIO RX T27p	DIFFOUT T27p	Low Speed	A2
		IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	D5
	8 VREFB8N0	IO CND			DIFFIO_RX_T27n	DIFFOUT_T27n	Low_Speed	B2
	+	GND	 					V18 V1
	+	GND GND	 				1	V1
	+	GND	 				1	U4 U14
	†	GND					1	U10
		GND						R7
		GND						N5
		GND						N2
		GND						N17
		GND						N12
		GND						N10
	1	GND					ļ	M14
	+	GND	 					L4 K9
	+	GND GND	 				1	K9 K6
	+	GND	†					K13
		GND						J17
		GND						J10
		GND						H14
		GND						G4
		GND						G2





								NOTE
nk Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
		GND						F8
	†	GND						F17
	+	GND						E6
	-	GND						E13
		GND						E10
		GND						D3
		GND						B6
		GND						B15
		GND						B10
		GND						A18
		GND						A1
		REFGND						E3
		VCCIO1A						H5
		VCCIO1A						G5
		VCCIO1B						K5
		VCCIO1B						J5
		VCCIO2						M5
	Ì	VCCIO2						L6
	İ	VCCIO2			İ			L5
		VCCIO3			İ			P9
		VCCIO3						P8
		VCCIO3						P7
		VCCIO3						N9
	t	VCCIO4						P12
	t	VCCIO4						P11
	+	VCCIO5						M13
	+	VCCIO5						L14
								L13
		VCCIO5						
		VCCIO5						K14
		VCCIO6						J14
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G14
		VCCIO6						G13
		VCCIO7						E12
		VCCIO7						E11
		VCCIO7						D11
		VCCIO8						F9
		VCCIO8						E9
		VCCIO8						E8
		VCCIO8						E7
		NC						N13
		NC						F7
		VCCA1						M6
		VCCA2						F14
		VCCA3						F6
	1	VCCA3			1			F4
	1	VCCA4			1			P13
	 	VCC_ONE			1			L9
	 	VCC_ONE			1			K10
	-	VCC_ONE VCC_ONE						J9
	-							
	ļ	VCC_ONE			1			H10
	ļ	VCC_ONE			1			N6
		VCC ONE						F13
		VCC_ONE						C3
		ADC_VREF						F3
		ANAIN1			1			E2

(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.

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