

								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
1A	VREFB1N0	IO			DIFFIO RX L1n	DIFFOUT_L1n	Low Speed	ļ
Α	VREFB1N0	10			DIFFIO_RX_LIII	DIFFOUT_L1p	Low_Speed	
A	VREFB1N0	IO			DIFFIO RX L3n	DIFFOUT L3n	Low Speed	1
À	VREFB1N0	10			DIFFIO RX L3p	DIFFOUT L3p	Low_Speed	1
A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	
A	VREFB1N0	IO			DIFFIO RX L5p	DIFFOUT L5p	Low Speed	
A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	
A	VREFB1N0	10			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	
В	VREFB1N0	IO		JTAGEN				
B B	VREFB1N0	IO	VREFB1N0	TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	
<u>в</u>	VREFB1N0 VREFB1N0	10	VREFB1N0	TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	
В	VREFB1N0	10		TDI	DIFFIO RX ETIP	DIFFOUT_L12n	Low Speed	<u> </u>
В	VREFB1N0	IO		TDO	DIFFIO RX L12p	DIFFOUT L12p	Low_Speed	1
В	VREFB1N0	IO		150	DIFFIO RX L14n	DIFFOUT L14n	Low Speed	
В	VREFB1N0	IO			DIFFIO RX L14p	DIFFOUT_L14p	Low_Speed	
В	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	
В	VREFB1N0	IO			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	
2	VREFB2N0	10	CLK0n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	
	VREFB2N0	IO	CLK0p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	
	VREFB2N0	IO	CLK1n		DIFFIO RX L22n	DIFFOUT L22n	High Speed	
2	VREFB2N0	10	CLK1p		DIFFIO RX L22p	DIFFOUT L22p	High_Speed	
	VREFB2N0 VREFB2N0	10	VREFB2N0 PLL L CLKOUTn		DIFFIO RX L31n	DIFFOUT L31n	High Speed	
2	VREFB2N0 VREFB2N0	10	PLL L CLKOUTD		DIFFIO RX L31h	DIFFOUT_L31h	High_Speed	
3	VREFB3N0	10	I LL_L_GENOUTH		DIFFIO_RX_LSTP	DIFFOUT_ESTP	High Speed	
	VREFB3N0	IO			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	
	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	
	VREFB3N0	IO			DIFFIO TX RX B3p	DIFFOUT_B3p	High_Speed	
3	VREFB3N0	10			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	
	VREFB3N0	10			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	
	VREFB3N0	IO			DIFFIO_TX_RX_B13n	DIFFOUT_B13n	High_Speed	
	VREFB3N0	10			DIFFIO TX RX B13p	DIFFOUT B13p	High Speed	
	VREFB3N0	10	LUDEED ON THE STATE OF THE STAT		DIFFIO_TX_RX_B15n	DIFFOUT_B15n	High_Speed	
	VREFB3N0 VREFB3N0	10	VREFB3N0		DIFFIO TX RX B15p	DIFFOUT B15p	Lliah Casad	
	VREFB3N0 VRFFB3N0	10			DIFFIO IX RX B15p	DIFFOUT B15p	High Speed	
	VREFB3N0	10	CLK6n		DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed	
	VREFB3N0	10	CLK6p		DIFFIO TX RX B18p	DIFFOUT B18p	High Speed	
	VREFB3N0	IO	CLK7n		DIFFIO_TX_RX_B20n	DIFFOUT B20n	High Speed	
3	VREFB3N0	IO	CLK7p		DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	
3	VREFB3N0	10			DIFFIO TX RX B22n	DIFFOUT B22n	High Speed	
3	VREFB3N0	IO			DIFFIO_TX_RX_B22p	DIFFOUT_B22p	High_Speed	
	VREFB4N0	10	VREFB4N0					
	VREFB4N0 VREFB4N0	10			DIFFIO TX RX B35n	DIFFOUT_B35n	High Count	
	VREFB4N0 VREFB4N0	10			DIFFIO_TX_RX_B35n DIFFIO_TX_RX_B35p	DIFFOUT_B35p	High_Speed	
4	VREFB4N0	10	İ		DIFFIO IX RX B33p	DIFFOUT_B33p	High Speed	
	VREFB4N0	IO			DIFFIO TX RX B41n	DIFFOUT B41n	High Speed	
	VREFB4N0	IO			DIFFIO_TX_RX_B41p	DIFFOUT_B41p	High_Speed	
5	VREFB5N0	IO	RUP		DIFFIO RX R1p	DIFFOUT R1p	High Speed	
	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	
	VREFB5N0	10	RDN		DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	
	VREFB5N0	10			DIFFIO RX R2n	DIFFOUT R2n	High Speed	
	VREFB5N0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	
	VREFB5N0	10			DIFFIG DV D44-	DIFFOLIT DATE	High Count	
5	VREFB5N0 VREFB5N0	10	VREFB5N0		DIFFIO RX R11n	DIFFOUT R11n	High Speed	
5	VREFB5N0 VREFB5N0	10	VINE BUING		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	
	VREFB5N0	IO			DIFFIO RX R15p	DIFFOUT R15p	High Speed	
	VREFB5N0	IO			DIFFIO RX R14n	DIFFOUT_R14n	High Speed	
5	VREFB5N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	High_Speed	
6	VREFB6N0	IO	CLK2p		DIFFIO RX R18p	DIFFOUT R18p	High Speed	
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	
	VREFB6N0	IO	CLK3p		DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	
	VREFB6N0	IO	CLK3n		DIFFIO RX R20n	DIFFOUT R20n	High Speed	
	VREFB6N0	10			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	
6	VREFB6N0 VREFB6N0	10	DPCLK3		DIFFIO_RX_R22n DIFFIO_RX_R30p	DIFFOUT_R22n DIFFOUT_R30p	High_Speed High Speed	
	VREFB6N0	10	VREEB6N0		DITTO KA KSUP	Dill Coll Roup	riigii opecu	
	VREFB6N0	IO	DPCLK2		DIFFIO RX R30n	DIFFOUT_R30n	High_Speed	
	VREFB6N0	IO			DIFFIO RX R31p	DIFFOUT R31p	High Speed	
6	VREFB6N0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	
6	VREFB6N0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	High_Speed	,
	VREFB6N0	IO			DIFFIO RX R32n	DIFFOUT R32n	High Speed	1
	VREFB6N0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	High_Speed	1
	VREFB6N0	10			DIFFIO_RX_R37n	DIFFOUT_R37n	High_Speed	
	VREFB7N0	10			DIFFIO RX T1p	DIFFOUT T1p	High Speed	
	VREFB7N0 VREFB7N0	10	VREFB7N0		DIFFIO_RX_T1n	DIFFOUT_T1n	High Speed	1
		10	VKEFB/INU		1			+
	VREFB7N0 VREFB7N0	10			†	+	1	
7	VREFB7N0 VREFB7N0	10	1		DIFFIO_RX_T22p	DIFFOUT_T22p	High_Speed	
7	VREFB7N0	10			DIFFIO RX T22n	DIFFOUT T22n	High Speed	1
	VREFB8N0	IO			DIFFIO RX T28p	DIFFOUT_T28p	Low Speed	·
	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T28n	DIFFOUT_T28n	Low_Speed	-
8	VREFB8N0	IO		DEV OE				1
	LYDEEDONIO	IO	VDEEDONIO	1				1
	VREFB8N0 VREFB8N0	10	VREFB8N0	CONFIG SEL		ļ		1

Pin List E144



ank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
	8 VREFB8N0	10			DIFFIO RX T31p	DIFFOUT_T31p	Low_Speed	
	8 VREFB8N0	Input only		nCONFIG				
	8 VREFB8N0	IO			DIFFIO RX T31n	DIFFOUT T31n	Low Speed	
	8 VREFB8N0	IO			DIFFIO RX T32p	DIFFOUT T32p	Low Speed	
	8 VREFB8N0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	Low_Speed	
	8 VREFB8N0	IO			DIFFIO RX T34p	DIFFOUT T34p	Low Speed	
	8 VREFB8N0	IO		CRC_ERROR	DIFFIO RX T34n	DIFFOUT_T34n	Low Speed	
	8 VREFB8N0	IO		ONO_ENNON	5	B.11 001_10 III	EGW_OPGGG	
	8 VREFB8N0	IO		nSTATUS	DIFFIO RX T36p	DIFFOUT T36p	Low Speed	
	8 VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T36n	DIFFOUT_T36n	Low Speed	
	8 VREFB8N0	IO			DIFFIO RX T38p	DIFFOUT_T38p	Low Speed	
	8 VREFB8N0	io			DIFFIO RX T38n	DIFFOUT T38n	Low Speed	
		GND						
		GND						
		GND						
	+	GND						1
		GND						
	+	GND			+	+	<u> </u>	
	+	GND			+	1		_
	+	GND			+	+	<u> </u>	
		GND						
		GND						
		GND						
		GND						
	+	GND						
	+	GND						
	+	VCCIO1A						_
	+							
	+	VCCIO1B						
	+	VCCIO2 VCCIO3						
	+							
		VCCIO3						
		VCCIO4						
		VCCIO5						
		VCCIO6						
		VCCIO6						
		VCCIO7						
		VCCIO8						
		VCCIO8						_
		VCCA1						_
		VCCA2						
		VCCA3						
		VCCA3						
		VCCA4						
		VCCA5						
		VCCA6						
		VCC_ONE						
		VCC ONE						
		VCC ONE						
		VCC_ONE						
		VCC_ONE						
		VCC ONE						
		VCC_ONE						
		VCC_ONE						
		VCC ONE						
		VCC_ONE						

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.
(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
1A	VREFB1N0	IO			DIFFIO RX L1n	DIFFOUT L1n	Low Speed	D1
1A	VREFB1N0	10			DIFFIO RX L1D	DIFFOUT LTD	Low Speed	D1
1A	VREFB1N0	10			DIFFIO RX L3n	DIFFOUT L'an	Low Speed	F3
1A	VREFB1N0	10			DIFFIO RX L3p	DIFFOUT L3p	Low Speed	F4
1A	VREFB1N0	10			DIFFIO RX L5n	DIFFOUT L5n	Low Speed	C1
1A	VREFB1N0	10			DIFFIO RX L5p	DIFFOUT L5p	Low Speed	B1
1A	VREFB1N0	IO			DIFFIO RX L7n	DIFFOUT L7n	Low Speed	F1
1A	VREFB1N0	10			DIFFIO RX L7p	DIFFOUT L7p	Low Speed	F1
1B	VREFB1N0	10		JTAGEN	DILLIO TOX CIP	511 CO1 E/P	сон оросс	F5
1B	VREFB1N0	Ю		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	G1
1B	VREFB1N0	10	VREFB1N0					H1
1B	VREFB1N0	10		TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	G2
1B	VREFB1N0	Ю		TDI	DIFFIO RX L12n	DIFFOUT L12n	Low Speed	F5
1B	VREFB1N0	Ю		TDO	DIFFIO RX L12p	DIFFOUT L12p	Low Speed	F6
1B	VREFB1N0	Ю			DIFFIO RX L14n	DIFFOUT L14n	Low Speed	F4
1B	VREFB1N0	Ю			DIFFIO RX L14p	DIFFOUT L14p	Low Speed	G4
1B	VREFB1N0	Ю			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	H2
1B		Ю			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	H3
2	VREFB2N0	Ю	CLK0n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	G5
2	VREFB2N0	10			DIFFIO RX L21n	DIFFOUT L21n	High Speed	J1
2	VREFB2N0	Ю	CLK0p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	H6
2	VREFB2N0	Ю			DIFFIO RX L21p	DIFFOUT L21p	High Speed	J2
2	VREFB2N0	Ю	CLK1n		DIFFIO RX L22n	DIFFOUT L22n	High Speed	H5
2	VREFB2N0	Ю			DIFFIO RX L23n		High Speed	M1
	VREFB2N0	Ю	CLK1p		DIFFIO RX L22p		High Speed	H4
2	VREFB2N0	Ю			DIFFIO RX L23p		High Speed	M2
2	VREFB2N0	Ю	DPCLK0		DIFFIO RX L24n	DIFFOUT L24n	High Speed	N2
2	VREFB2N0	Ю	VREFB2N0					L1
2	VREFB2N0	Ю	DPCLK1		DIFFIO RX L24p	DIFFOUT L24p	High Speed	N3
	VREFB2N0	Ю			·			L2
	VREFB2N0	Ю	PLL L CLKOUTn		DIFFIO RX L31n	DIFFOUT L31n	High Speed	M3
	VREFB2N0	Ю			DIFFIO RX L32n		High Speed	K1
2	VREFB2N0	Ю	PLL L CLKOUTp		DIFFIO RX L31p	DIFFOUT L31p	High Speed	L3
2	VREFB2N0	Ю			DIFFIO RX L32p	DIFFOUT L32p	High Speed	K2
3	VREFB3N0	Ю			DIFFIO TX RX B1n	DIFFOUT B1n	High Speed	L5
3	VREFB3N0	Ю			DIFFIO RX B2n	DIFFOUT B2n	High Speed	M4
3	VREFB3N0	Ю			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	L4
	VREFB3N0	Ю			DIFFIO RX B2p	DIFFOUT B2p	High Speed	M5
3	VREFB3N0	Ю			DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	K5
3	VREFB3N0	Ю			DIFFIO RX B4n	DIFFOUT B4n	High Speed	N4
3	VREFB3N0	Ю			DIFFIO TX RX B3p		High Speed	J5
3	VREFB3N0	Ю			DIFFIO RX B4p		High Speed	N5
3	VREFB3N0	Ю			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	N6
3	VREFB3N0	Ю			DIFFIO RX B6n	DIFFOUT B6n	High Speed	N7
3	VREFB3N0	Ю			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	M7
3	VREFB3N0	Ю			DIFFIO RX B6p	DIFFOUT B6p	High Speed	N8
3	VREFB3N0	Ю			DIFFIO TX RX B13n	DIFFOUT B13n	High Speed	J6
3	VREFB3N0	Ю			DIFFIO RX B14n	DIFFOUT B14n	High Speed	M8
3	VREFB3N0	Ю			DIFFIO TX RX B13p	DIFFOUT B13p	High Speed	K6
3	VREFB3N0	Ю			DIFFIO RX B14p		High Speed	M9
3	VREFB3N0	Ю			DIFFIO TX RX B15n	DIFFOUT B15n	High Speed	J7
3	VREFB3N0	Ю	VREFB3N0					N11
3	VREFB3N0	10			DIFFIO TX RX B15p	DIFFOUT B15p	High Speed	K7
3	VREFB3N0	Ю						N12
3	VREFB3N0	10			DIFFIO TX RX B16n	DIFFOUT B16n	High Speed	M13
3	VREFB3N0	Ю			DIFFIO RX B17n		High Speed	N10
3	VREFB3N0	IO			DIFFIO TX RX B16p	DIFFOUT B16p	High Speed	M12
3	VREFB3N0	Ю			DIFFIO RX B17p	DIFFOUT B17p	High Speed	N9
3	VREFB3N0	Ю	CLK6n		DIFFIO TX RX B18n	DIFFOUT B18n	High Speed	M11
3	VREFB3N0	Ю	CLK6p		DIFFIO TX RX B18p	DIFFOUT B18p	High Speed	L11
	VREFB3N0	Ю	CLK7n		DIFFIO TX RX B20n	DIFFOUT B20n	High Speed	J8
3	VREFB3N0	Ю	CLK7p		DIFFIO TX RX B20p	DIFFOUT B20p	High Speed	K8
3	VREFB3N0	Ю			DIFFIO TX RX B22n	DIFFOUT B22n	High Speed	M10
	VREFB3N0	Ю			DIFFIO TX RX B22p	DIFFOUT B22p	High Speed	L10
5	VREFB5N0	Ю	RUP		DIFFIO RX R1p	DIFFOUT R1p	High Speed	K10
5	VREFB5N0	Ю			DIFFIO RX R2p	DIFFOUT R2p	High Speed	K11
	VREFB5N0	Ю	RDN		DIFFIO RX R1n	DIFFOUT R1n	High Speed	J10
	VREFB5N0	Ю			DIFFIO RX R2n	DIFFOUT R2n	High Speed	L12
	VREFB5N0	Ю			DIFFIO RX R11p	DIFFOUT R11p	High Speed	K12
	VREFB5N0	Ю						L13
	VREFB5N0	Ю			DIFFIO RX R11n	DIFFOUT R11n	High Speed	J12
	VREFB5N0	Ю	VREFB5N0					K13
5	VREFB5N0	Ю			DIFFIO RX R12p	DIFFOUT R12p	High Speed	J9
5	VREFB5N0	Ю			DIFFIO RX R13p	DIFFOUT R13p	High Speed	J13
5	VREFB5N0	Ю			DIFFIO RX R12n	DIFFOUT R12n	High Speed	H10
5	VREFB5N0	Ю			DIFFIO RX R13n	DIFFOUT R13n	High Speed	H13
	VREFB5N0	Ю			DIFFIO RX R14p		High Speed	H9
		Ю			DIFFIO RX R15p	DIFFOUT R15p	High Speed	G13
		Ю			DIFFIO RX R14n	DIFFOUT R14n	High Speed	H8
	VREFB5N0	Ю			DIFFIO RX R15n	DIFFOUT R15n	High Speed	G12
- 6	VREFB6N0	Ю	CLK2p		DIFFIO RX R18p	DIFFOUT R18p	High Speed	G9
6	VREFB6N0	IO	CLK2n		DIFFIO RX R18n	DIFFOUT R18n	High Speed	G10
6	VREFB6N0	10	CLK3p		DIFFIO RX R20p		High Speed	F13
	VREFB6N0	IO	CLK3n		DIFFIO RX R20n		High Speed	E13
	VREFB6N0	IO			DIFFIO RX R22p		High Speed	F12
	VREFB6N0	10			DIFFIO RX R22n	DIFFOUT R22n	High Speed	E12
6	VREFB6N0	IO	DPCLK3		DIFFIO RX R30p	DIFFOUT R30p	High Speed	F9
6	VREFB6N0	10	VREFB6N0				1	D13
- 6	VREFB6N0	IO	DPCLK2		DIFFIO RX R30n	DIFFOUT R30n	High Speed	F10
6	VREFB6N0	IO						C13
	VREFB6N0	Ю			DIFFIO RX R31p	DIFFOUT R31p	High Speed	F8



	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
- 6	VREFB6N0	Ю	İ		DIFFIO RX R32p	DIFFOUT R32p	High Speed	B12
6	VREFB6N0	Ю			DIFFIO RX R31n	DIFFOUT R31n	High Speed	E9
6	VREFB6N0	Ю			DIFFIO RX R32n	DIFFOUT R32n	High Speed	B11
	VREFB6N0	Ю			DIFFIO RX R33p	DIFFOUT R33p	High Speed	C12
	VREFB6N0	Ю			DIFFIO RX R34p	DIFFOUT R34p	High Speed	B13
	VREFB6N0	Ю			DIFFIO RX R33n	DIFFOUT R33n	High Speed	C11
6	VREFB6N0	Ю			DIFFIO RX R34n	DIFFOUT R34n	High Speed	A12
6	VREFB6N0	IO			DIFFIO RX R35p	DIFFOUT R35p	High Speed	E10
	VREFB6N0	10	+		DIFFIO RX R35n	DIFFOUT R35n	High Speed	D9
6	VREFB6N0 VREFB6N0	10			DIFFIO RX R37p DIFFIO RX R37n	DIFFOUT R37p	High Speed	D12 D11
			OLIVE-				High Speed	
	VREFB8N0	10	CLK5p		DIFFIO RX T26p	DIFFOUT T26p	Low Speed	C10 A8
	VREFB8N0	10	CLK5n		DIFFIO RX T27p DIFFIO RX T26n	DIFFOUT T27p DIFFOUT T26n	Low Speed Low Speed	C9
			CLKSII					
	3 VREFB8N0 3 VREFB8N0	10	+		DIFFIO RX T27n DIFFIO RX T28p	DIFFOUT T27n DIFFOUT T28p	Low Speed	A9 B10
	VREFB8N0	10	+		DIFFIO RX T29p	DIFFOUT T29p	Low Speed Low Speed	A10
	VREFB8N0	10	+	DEV CLRn	DIFFIO RX T28n	DIFFOUT T28n	Low Speed	B9
	VREFB8N0	10	+	DEV CERTI	DIFFIO RX 12811	DIFFOUT T29n	Low Speed	A11
	VREFB8N0	10	+	DEV OE	DIFFIO RX T30p	DIFFOUT T30p	Low Speed	D8
	VREFB8N0	10	†	52 V OL	DIFFIO RX 130p	DIFFOUT T30n	Low Speed	E8
	VREFB8N0	10	VREFB8N0		5110 100 10011	5 55 155	Lon Opecu	B7
, a	VREFB8N0	10	THE BOILD	CONFIG SEL				D7
	VREFB8N0	IO	†		DIFFIO RX T31p	DIFFOUT T31p	Low Speed	A7
	VREFB8N0	Input only	i	nCONFIG	210 10. 1019			E7
	VREFB8N0	IO IO	1		DIFFIO RX T31n	DIFFOUT T31n	Low Speed	A6
я я	VREFB8N0	10	1		DIFFIO RX T32p	DIFFOUT T32p	Low Speed	B6
8	VREFB8N0	IO	1		DIFFIO RX T33p	DIFFOUT T33p	Low Speed	A4
	VREFB8N0	IO	1		DIFFIO RX T32n	DIFFOUT T32n	Low Speed	B5
	VREFB8N0	Ю	1		DIFFIO RX T33n	DIFFOUT T33n	Low Speed	A3
	VREFB8N0	Ю			DIFFIO RX T34p	DIFFOUT T34p	Low Speed	E6
	VREFB8N0	10			DIFFIO RX T35p	DIFFOUT T35p	Low Speed	B3
8	VREFB8N0	Ю		CRC ERROR	DIFFIO RX T34n	DIFFOUT T34n	Low Speed	D6
8	VREFB8N0	Ю			DIFFIO RX T35n	DIFFOUT T35n	Low Speed	B4
8	VREFB8N0	Ю		nSTATUS	DIFFIO RX T36p	DIFFOUT T36p	Low Speed	C4
	VREFB8N0	IO						A5
8	VREFB8N0	Ю		CONF DONE	DIFFIO RX T36n	DIFFOUT T36n	Low Speed	C5
8	VREFB8N0	IO			DIFFIO RX T38p	DIFFOUT T38p	Low Speed	A2
8	VREFB8N0	Ю			DIFFIO RX T38n	DIFFOUT T38n	Low Speed	B2
		GND						D2
		GND						E2
		GND						N13
		GND						N1
		GND						M6
		GND						L9
		GND						J4
		GND						H12
		GND						G7
		GND						F3
		GND						E11
		GND						D5
	.	GND	1					C3
		GND	1					B8
	 	GND	+					A13
	 	GND	+			+		
	 	VCCIO1A	+					F2
	1	VCCIO1B VCCIO2	+					G3 K3
	1		+					J3
	 	VCCIO2 VCCIO3	+					J3
	 	VCCIO3	+	<u> </u>		-	-	L8 L7
	†		+				-	
	1	VCCIO3 VCCIO5	1			<u> </u>	+	L6 J11
	1	VCCIO5	1			<u> </u>	+	H11
	I	VCCIO6	1			<u> </u>	+	G11
	1	VCCIO6	†					F11
	1	VCCIO8	†					C8
	1	VCCIO8	†					C7
	1	VCCIO8	†					C6
	1	VCCA1	†					K4
	1	VCCA1	†					D10
	I	VCCA2 VCCA3	1			<u> </u>	+	D3
	I	VCCA3	1			<u> </u>	+	D3
	I	VCCA3	1			<u> </u>	+	K9
	I	VCC ONE	1			<u> </u>	+	H7
	+	VCC ONE	†					G8
		VCC ONE						G6

(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.



Version 2017.12.15

								No
k Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
	VEEEDANO	10			DIFFIG BY 14-	DIFFOLIT LA	Leve Occasi	Di
	VREFB1N0	10			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D4
	VREFB1N0	10			DIFFIO_RX_L2n	DIFFOUT_L2n	Low_Speed	C2
	VREFB1N0	10			DIFFIO RX L1p	DIFFOUT L1p	Low Speed	E4
	VRFFB1N0	IO			DIFFIO RX L2p	DIFFOUT_L2p	Low_Speed	D2
	VREFB1N0	IO			DIFFIO RX L3n	DIFFOUT L3n	Low Speed	G6
		10	+					
	VREFB1N0	10			DIFFIO RX L4n	DIFFOUT L4n	Low Speed	B1
	VREFB1N0	10			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	H6
	VREFB1N0	10			DIFFIO RX L4p	DIFFOUT_L4p	Low Speed	C1
	VRFFB1N0	IO			DIFFIO RX L5n	DIFFOUT L5n	Low Speed	F5
	VREFB1N0	in			DIFFIO RX L6n	DIFFOUT_L6n		D1
		10	1				Low_Speed	
	VREFB1N0	10			DIFFIO RX L5p	DIFFOUT L5p	Low_Speed	E5
	VREFB1N0	IO			DIFFIO RX L6p	DIFFOUT L6p	Low Speed	E1
	VREFB1N0	IO			DIFFIO RX L7n	DIFFOUT_L7n	Low Speed	G3
	VREFB1N0	IO			DIFFIO RX L8n	DIFFOUT_L8n		F1
	VREFBINO	10	1			DIFFOUT_Lon	Low_Speed	F2
		10			DIFFIO RX L7p		Low Speed	
	VREFB1N0	IO			DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	G1
	VREFB1N0	IO			DIFFIO RX L9n	DIFFOUT_L9n	Low Speed	G7
	VRFFB1N0	IO			DIFFIO RX L10n	DIFFOUT I 10n	Low Speed	H2
	VREFB1N0	10		ITAGEN	DIFFIO RX 19p	DIFFOUT 190		
		10		JTAGEN			Low_Speed	H7
	VREFB1N0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	Low_Speed	H1
	VREFB1N0	10		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	J7
	VREFB1N0	in	VREFB1N0				Low Speed	J3
	VIDEEDANO	io	VICEDINO	TOV	DIFFIO BY 144-	DIFFOLIT L1110		
	VREFB1N0	10	4	TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	J8
	VREFB1N0	10	<u> </u>			<u> </u>	Low Speed	J4
	VREFB1N0	10		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low Speed	H3
	VREFB1N0	10	i	†	DIFFIO_RX_L13n	DIFFOUT_L13n	Low_Speed	J2
		12	+	TDO				
	VREFB1N0	IU	1	TDO	DIFFIO RX L12p	DIFFOUT L12p	Low Speed	H4
_	VREFB1N0	10	1		DIFFIO_RX_L13p	DIFFOUT_L13p	Low_Speed	J1
	VREFB1N0	IO			DIFFIO RX L14n	DIFFOUT L14n	Low Speed	J6
	VREFB1N0	in	1	†	DIFFIO RX L14II	DIFFOUT L15n	Low Speed	K2
		10	+	 			Low Speed	
	VREFB1N0	10	<u> </u>		DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	K7
	VREFB1N0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	Low_Speed	K1
	VREFB1N0	IO			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	K4
	VREFB1N0	10	1		DIFFIO RX L101	DIFFOUT L17n		1.1
		10	+	 			Low_Speed	
	VREFB1N0	IO	<u> </u>		DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	K3
	VREFB1N0	10			DIFFIO RX L17p	DIFFOUT L17p	Low Speed	L2
	2 VREFB2N0	10	CLK0n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	L3
			OLIVOIT					
	2 VREFB2N0	10			DIFFIO_RX_L21n	DIFFOUT_L21n	High_Speed	M1
	2 VREFB2N0	IO	CLK0p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	M3
	2 VREFB2N0	IO			DIFFIO_RX_L21p	DIFFOUT_L21p	High_Speed	M2
	2 VREFB2N0	10	CLK1n		DIFFIO_RX_L22n	DIFFOUT_L22n	High Speed	K8
		10	CLKIII					
	2 VREFB2N0	10			DIFFIO RX L23n	DIFFOUT L23n	High Speed	N1
	2 VREFB2N0	10	CLK1p		DIFFIO_RX_L22p	DIFFOUT L22p	High Speed	L8
	2 VRFFB2N0	IO			DIFFIO RX L23p	DIFFOUT_L23p	High Speed	P1
		in	DDOLIGO					M4
	2 VREFB2N0	10	DPCLK0		DIFFIO RX L24n	DIFFOUT L24n	High Speed	
	2 VREFB2N0	IO	VREFB2N0				High_Speed	R1
	2 VREFB2N0	IO	DPCLK1		DIFFIO RX L24p	DIFFOUT_L24p	High Speed	N3
	2 VREFB2N0	IO					High Speed	R2
		in			DIFFIO RX L25n	DISSOLUTION .		
	2 VREFB2N0	10				DIFFOUT_L25n	High_Speed	R3
	2 VREFB2N0	IO			DIFFIO_RX_L26n	DIFFOUT_L26n	High_Speed	P2
	2 VREFB2N0	10			DIFFIO RX L25p	DIFFOUT L25p	High Speed	T3
	2 VREFB2N0	10			DIFFIO_RX_L26p	DIFFOUT_L26p	High Speed	P3
	2 VREFB2N0	10			DIFFIO RX 127n			
		10				DIFFOUT_L27n	High_Speed	L7
	2 VREFB2N0	10			DIFFIO RX L28n	DIFFOUT L28n	High Speed	T1
	2 VREFB2N0	10			DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	M7
	2 VREFB2N0	IO	1	†	DIFFIO RX L28p	DIFFOUT L28p	High_Speed	T2
		liš	DIL I OLKOUT:	+				
	2 VREFB2N0	IO	PLL L CLKOUTn	-	DIFFIO RX L31n	DIFFOUT L31n	High Speed	N4
	2 VREFB2N0	10	<u> </u>		DIFFIO_RX_L32n	DIFFOUT_L32n	High_Speed	U1
	2 VREFB2N0	10	PLL_L_CLKOUTp		DIFFIO_RX_L31p	DIFFOUT_L31p	High_Speed	P4
	2 VREFB2N0	IO			DIFFIO RX L32p	DIFFOUT L32p	High Speed	U2
	2 VACE DEITO	10	+		DIFFIO TV DV D4-	DIFFOUT BAN	Lligh Con- 1	R4
	3 VREFB3N0	IIO	+	 	DIFFIO TX RX B1n	DIFFOUT_B1n	High Speed	
	3 VREFB3N0	10			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed	U3
	3 VREFB3N0	10			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	T4
	3 VRFFB3N0	10			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	V2
	3 VREFB3N0	lio	i	†	DIFFIO TX RX B3n	DIFFOUT B3n	High_Speed	P6
	O VIDEEDONIO	liš	+	+			gri_Opeeu	V3
	3 VREFB3N0	10	+	<u> </u>	DIFFIO RX B4n	DIFFOUT B4n	High Speed	
	3 VREFB3N0	10			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	P5
	3 VREFB3N0	10			DIFFIO RX B4p	DIFFOUT_B4p	High Speed	V4
	3 VRFFB3N0	IO	1		DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	R5
	3 VREFB3N0	lio	1		DIFFIO_RX_B6n	DIFFOUT_B6n		U5
	SIVINLIDONU	10			DIFFIO_RA_DII	DITTOUT_DOIL	High_Speed	05
	O MOEEDONIO			•	DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	R6
	3 VREFB3N0	10						
	3 VREFB3N0 3 VREFB3N0	10			DIFFIO RX B6p	DIFFOUT B6p	High Speed	V5
	3 VREFB3N0	10 10 10				DIFFOUT B6p DIFFOUT B13n	High Speed High Speed	V5 T5
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10 10			DIFFIO_RX_B6p DIFFIO_TX_RX_B13n	DIFFOUT_B13n	High_Speed	T5
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10			DIFFIO RX B6p DIFFIO_TX_RX_B13n DIFFIO_RX_B14n	DIFFOUT_B13n DIFFOUT_B14n	High_Speed High_Speed	T5 T7
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10 10 10 10			DIFFIO RX B6p DIFFIO_TX_RX_B13n DIFFIO_RX_B14n DIFFIO TX RX B13p	DIFFOUT_B13n DIFFOUT_B14n DIFFOUT_B13p	High_Speed High_Speed High_Speed	T5 T7 T6
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10 10			DIFFIO RX B6p DIFFIO_TX_RX_B13n DIFFIO_RX_B14n	DIFFOUT_B13n DIFFOUT_B14n	High_Speed High_Speed High_Speed	T5 T7
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10 10 10 10			DIFFIO RX B6p DIFFIO TX RX B13n DIFFIO RX_B14n DIFFIO TX RX B13p DIFFIO RX_B14p	DIFFOUT B13n DIFFOUT B14n DIFFOUT B13p DIFFOUT_B14p	High_Speed High_Speed High_Speed High_Speed	T5 T7 T6 T8
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10 10 10 10 10	I DEED NO.		DIFFIO RX B6p DIFFIO_TX_RX_B13n DIFFIO_RX_B14n DIFFIO TX RX B13p	DIFFOUT_B13n DIFFOUT_B14n DIFFOUT_B13p	High_Speed High_Speed High Speed High_Speed High_Speed	T5 T7 T6 T8 N7
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	O	VREFB3N0		DIFFIO RX B6p DIFFIO TX RX B13n DIFFIO TX B14n DIFFIO TX B14n DIFFIO TX RX B13p DIFFIO RX B14p DIFFIO TX RX B15n	DIFFOUT_B13n DIFFOUT_B14n DIFFOUT_B13p DIFFOUT_B14p DIFFOUT_B15n	High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed	T5 T7 T6 T8 N7 U6
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	10 10 10 10 10	VREFB3N0		DIFFIO RX B6p DIFFIO TX RX B13n DIFFIO TX B14n DIFFIO TX B14n DIFFIO TX RX B13p DIFFIO RX B14p DIFFIO TX RX B15n	DIFFOUT_B13n DIFFOUT_B14n DIFFOUT_B13p DIFFOUT_B14p DIFFOUT_B15n	High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed	T5 T7 T6 T8 N7
	3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0 3 VREFB3N0	O	VREFB3NO		DIFFIO RX B6p DIFFIO TX RX B13n DIFFIO RX_B14n DIFFIO TX RX B13p DIFFIO RX_B14p	DIFFOUT B13n DIFFOUT B14n DIFFOUT B13p DIFFOUT_B14p	High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed	T5 T7 T6 T8 N7 U6
	3 VREFB3NO 3 VREFB3NO	O	VREFB3N0		DIFFIO RX B60 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO RX B14p DIFFIO TX RX B15n DIFFIO TX RX B15n	DIFFOUT B13n DIFFOUT B14n DIFFOUT B13p DIFFOUT, B14p DIFFOUT_B15n DIFFOUT_B15n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6
	3 (VREFB3N0 3 (VREFB3N0	O	VREFB3N0		DIFFIO RX B60 DIFFIO TX RX B13n DIFFIO RX B14n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15p DIFFIO TX RX B15p DIFFIO TX RX B15p DIFFIO TX RX B16n	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT B13p DIFFOUT, B14p DIFFOUT, B15n DIFFOUT, B15n DIFFOUT, B15n	High_Speed High Speed High Speed High Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed High_Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8
	3 (VREFB3N0 3 (VREFB3N0	O	VREFB3N0		DIFFIO RX 860 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B14p DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO RX B17n	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT, B13p DIFFOUT, B14p DIFFOUT, B15n DIFFOUT B15n DIFFOUT B16n DIFFOUT B16n DIFFOUT B17n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8
	3 (VREFB3N0 3 (VREFB3N0	O	VREFB3N0		DIFFIO RX 860 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B14p DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO RX B17n	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT, B13p DIFFOUT, B14p DIFFOUT, B15n DIFFOUT B15n DIFFOUT B16n DIFFOUT B16n DIFFOUT B17n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8
	3 (VREFB3NO 3 (VREFB3NO	O	VREFB3N0		DIFFIO RX B6D DIFFIO TX RX B13n DIFFIO RX B14n DIFFIO RX B14n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15p DIFFIO TX RX B15n DIFFIO TX RX B15p DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO RX B17n DIFFIO RX, B17n DIFFIO TX, RX, B16p	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT B13p DIFFOUT B14p DIFFOUT B15n DIFFOUT B15n DIFFOUT B15n DIFFOUT B16n DIFFOUT, B17n DIFFOUT, B17n	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8 U7 R9
	3 (VREFB3N0 3 (VREFB3N0	O			DIFFIO RX 860 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO RX B14n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B16n DIFFIO TX RX B17n DIFFIO TX RX B17n DIFFIO TX RX B17n DIFFIO TX RX B17p DIFFIO TX RX B17p	DIFFOUT, B13n DIFFOUT B14n DIFFOUT B13p DIFFOUT B15p DIFFOUT B15n DIFFOUT B15n DIFFOUT B15p DIFFOUT B16n DIFFOUT B17n DIFFOUT B17n DIFFOUT B17p	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8 U7 R9 V7
	3 (WREFB3NO 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO)	O	VREFB3N0 CLK6n		DIFFIO RX B60 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO RX B17n DIFFIO TX RX B16p DIFFIO RX B17p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B18n	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT B13p DIFFOUT B14p DIFFOUT B15n DIFFOUT B15n DIFFOUT B16n DIFFOUT B16n DIFFOUT B17n DIFFOUT B17n DIFFOUT B17p DIFFOUT B17p DIFFOUT B17p	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8 U7 R9 V7 V9
	3 (WREFB3NO 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO)	O			DIFFIO RX B60 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO RX B17n DIFFIO TX RX B16p DIFFIO RX B17p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B18n	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT B13p DIFFOUT B14p DIFFOUT B15n DIFFOUT B15n DIFFOUT B16n DIFFOUT B16n DIFFOUT B17n DIFFOUT B17n DIFFOUT B17p DIFFOUT B17p DIFFOUT B17p	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8 U7 R9 V7 V9
	3 (VREFB3N0 3 (VREFB3N0) 3 (VREFB3N0) 3 (VREFB3N0) 3 (VREFB3N0) 3 (VREFB3N0)	O	CLK6n		DIFFIO RX B60 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO RX B14n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15p DIFFIO TX RX B15p DIFFIO TX RX B15p DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B17p DIFFIO TX RX B18n DIFFIO TX RX B18n	DIFFOUT B13n DIFFOUT B14n DIFFOUT B13p DIFFOUT B15p DIFFOUT B15p DIFFOUT B15p DIFFOUT B16n DIFFOUT B17n DIFFOUT B17n DIFFOUT B17p DIFFOUT B17p DIFFOUT B17p DIFFOUT B18n DIFFOUT B19n	High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8 U7 R9 V7 V9 U8
	3 (WREFB3NO 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO) 3 (WREFB3NO)	O			DIFFIO RX B60 DIFFIO TX RX B13n DIFFIO TX RX B13n DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B13p DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B15n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO TX RX B16n DIFFIO RX B17n DIFFIO TX RX B16p DIFFIO RX B17p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B16p DIFFIO TX RX B18n	DIFFOUT, B13n DIFFOUT, B14n DIFFOUT B13p DIFFOUT B14p DIFFOUT B15n DIFFOUT B15n DIFFOUT B16n DIFFOUT B16n DIFFOUT B17n DIFFOUT B17n DIFFOUT B17p DIFFOUT B17p DIFFOUT B17p	High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed High Speed	T5 T7 T6 T8 N7 U6 N8 V6 R8 U7 R9 V7 V9

Pin List U324

Page 5 of 9



								N
Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
3	VREFB3N0	IIO	+		DIFFIO_RX_B21n	DIFFOUT_B21n	High_Speed	V10
3	VREFB3N0	10	CLK7p		DIFFIO TX RX B20p	DIFFOUT_B20p	High_Speed	M9
	VREFB3N0	io			DIFFIO RX B21p		High Speed	V11
	VREFB3N0	10	1		DIFFIO TX RX B22n		High Speed	T9
	VREFB3N0	10			DIFFIO_RX_B23n	DIFFOUT_B23n	High_Speed	V12
	VREFB3N0	10			DIFFIO TX RX B22p		High Speed	T10
3	VREFB3N0	10			DIFFIO_RX_B23p	DIFFOUT_B23p	High_Speed	U11
	VREFB4N0	10			DIFFIO_TX_RX_B30n		High_Speed	P10
	VREFB4N0 VREFB4N0	10			DIFFIO RX B31n		High Speed	U12 N11
	VREFB4N0 VREFB4N0	10	+		DIFFIO_TX_RX_B30p DIFFIO_RX_B31p	DIFFOUT_B30p DIFFOUT_B31p	High_Speed	
4	VREFB4N0	10	+		DIFFIO TX RX B32n	DIFFOUT B32n	High Speed High Speed	U13 M10
	VREFB4N0	10	VREFB4N0		BILLIO IX IX BOEI	BITT GOT BOLIT	High Speed	T11
	VREFB4N0	io			DIFFIO_TX_RX_B32p	DIFFOUT_B32p	High Speed	L10
4	VREFB4N0	10	1				High Speed	T12
	VREFB4N0	10			DIFFIO_TX_RX_B33n	DIFFOUT_B33n	High_Speed	R10
	VREFB4N0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	High_Speed	V13
	VREFB4N0	10			DIFFIO TX RX B33p	DIFFOUT B33p	High Speed	R11
	VREFB4N0	10			DIFFIO_RX_B34p		High_Speed	V14
	VREFB4N0	10			DIFFIO_TX_RX_B35n	DIFFOUT_B35n	High_Speed	R12
	VREFB4N0	10			DIFFIO RX B36n		High Speed	T13
	VREFB4N0 VREFB4N0	10	+		DIFFIO TX RX B35p	DIFFOUT B35p	High Speed	R13
	VREFB4N0 VREFB4N0	10	+		DIFFIO_RX_B36p DIFFIO_TX_RX_B37n	DIFFOUT_B36p DIFFOUT_B37n	High_Speed High Speed	R14
	VREFB4N0 VRFFB4N0	10	+		DIFFIO TX RX B3/n DIFFIO RX B38n		High Speed High Speed	V15
	VREFB4N0 VRFFB4N0	10	+	 	DIFFIO_RX_B38n DIFFIO_TX_RX_B37n		High_Speed	V15
	VREFB4N0	10	† 		DIFFIO RX B38p	DIFFOUT B38p	High Speed	U15
	VREFB4N0	io	†		DIFFIO TX RX B41n		High_Speed	U16
	VREFB4N0	10	†		DIFFIO RX B42n		High Speed	V16
	VREFB4N0	10	1		DIFFIO TX RX B41p		High Speed	U17
4	VREFB4N0	10			DIFFIO_RX_B42p	DIFFOUT_B42p	High_Speed	V17
5	VREFB5N0	10	RUP		DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	N14
5	VREFB5N0	10			DIFFIO RX R2p	DIFFOUT R2p	High Speed	T16
	VREFB5N0	10	RDN		DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	P14
	VREFB5N0	10			DIFFIO_RX_R2n		High_Speed	R16
	VREFB5N0	10			DIFFIO RX R7p		High Speed	M12
	VREFB5N0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed	U18
5	VREFB5N0	10			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	M11
5	VREFB5N0	10			DIFFIO RX R8n	DIFFOUT R8n	High Speed	T18
	VREFB5N0 VREFB5N0	10			DIFFIO_RX_R9p DIFFIO_RX_R10p		High_Speed	N15 N16
	VREFB5N0	10	+		DIFFIO_RX_R10p DIFFIO_RX_R9n		High_Speed	M15
	VREFB5N0	10	+		DIFFIO RX R9II DIFFIO_RX_R10n	DIFFOUT_R10n	High Speed High_Speed	M16
5	VREFB5N0	io	+		DIFFIO RX R11p	DIFFOUT_R11p	High_Speed	R15
	VREFB5N0	io			Bii i io_lox_ki ip	Birr Gor_Krip	High Speed	P16
	VREFB5N0	10	†		DIFFIO_RX_R11n	DIFFOUT_R11n	High Speed	P15
	VREFB5N0	10	VREFB5N0		Sii i io_io_ioi_ki iii		High_Speed	P17
5	VREFB5N0	10	1		DIFFIO RX R12p	DIFFOUT R12p	High Speed	L12
5	VREFB5N0	10			DIFFIO_RX_R13p	DIFFOUT_R13p	High_Speed	T17
5	VREFB5N0	10			DIFFIO_RX_R12n	DIFFOUT_R12n	High_Speed	L11
	VREFB5N0	10			DIFFIO RX R13n		High Speed	R17
	VREFB5N0	10			DIFFIO_RX_R14p		High_Speed	L15
5	VREFB5N0	10			DIFFIO_RX_R15p	DIFFOUT_R15p	High_Speed	L16
	VREFB5N0 VREFB5N0	10			DIFFIO RX R14n DIFFIO RX R15n	DIFFOUT R14n DIFFOUT R15n	High Speed	K15
	VREFB5N0 VREFB5N0	10			DIFFIO_RX_R15n DIFFIO_RX_R16o		High_Speed High Speed	K16 R18
	VREFB5N0	10	+		DIFFIO_RX_R16p DIFFIO_RX_R17p			
	VREFB5N0 VRFFB5N0	10	+		DIFFIO RX R1/p		High Speed High_Speed	N18 P18
	VREFB5N0	10	†		DIFFIO_RX_R16II		High_Speed	M18
	VREFB6N0	lio	CLK2p		DIFFIO_RX_R17II	DIFFOUT R18p	High Speed	K12
	VREFB6N0	10	 		DIFFIO RX R19p		High Speed	M17
	VREFB6N0	10	CLK2n		DIFFIO_RX_R18n		High_Speed	K11
	VREFB6N0	10			DIFFIO RX R19n		High Speed	L18
6	VREFB6N0	10	CLK3p		DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	L17
6	VREFB6N0	10			DIFFIO_RX_R21p	DIFFOUT_R21p	High_Speed	K18
6	VREFB6N0	10	CLK3n		DIFFIO RX R20n	DIFFOUT R20n	High Speed	K17
	VREFB6N0	10	<u> </u>		DIFFIO_RX_R21n		High_Speed	J18
	VREFB6N0	10	<u> </u>		DIFFIO_RX_R22p		High_Speed	H18
	VREFB6N0	10	 		DIFFIO RX R23p	DIFFOUT R23p	High Speed	H17
	VREFB6N0	10	 		DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed	G18
	VREFB6N0 VREFB6N0	10	 		DIFFIO_RX_R23n	DIFFOUT_R23n DIFFOUT_R24p	High_Speed	G17 J11
	VREFB6N0 VRFFB6N0	10	+	 	DIFFIO RX R24p DIFFIO RX R24n		High Speed High Speed	J11 J12
	VREFB6N0	10	+		DIFFIO_RX_R24n DIFFIO_RX_R26p		High_Speed	J12 J15
	VREFB6N0	lio	†		DIFFIO_RX_R26p DIFFIO_RX_R27p		High Speed	J16
	VREFB6N0	10	† 		DIFFIO RX R26n	DIFFOUT_R26n	High_Speed	H15
	VREFB6N0	10	1		DIFFIO RX R27n	DIFFOUT_R27n	High Speed	H16
	VREFB6N0	10	DPCLK3		DIFFIO RX R30p		High Speed	H11
	VREFB6N0	10	VREFB6N0				High Speed	F18
	VREFB6N0	10	DPCLK2		DIFFIO_RX_R30n	DIFFOUT_R30n	High_Speed	H12
- 6	VREFB6N0	10	1				High Speed	E18
	VREFB6N0	10			DIFFIO_RX_R31p	DIFFOUT_R31p	High_Speed	F15
6	VREFB6N0	10	1		DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	G16
6 6		IO			DIFFIO RX R31n	DIFFOUT R31n	High Speed	G15
6 6 6	VREFB6N0	10				DIFFOUR DAG		F16
6 6 6	VREFB6N0 VREFB6N0	10			DIFFIO_RX_R32n	DIFFOUT_R32n	High_Speed	
6 6 6 6	VREFB6N0 VREFB6N0 VREFB6N0				DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	E16
6 6 6 6	VREFB6N0 VREFB6N0				DIFFIO_RX_R32n DIFFIO_RX_R33p DIFFIO_RX_R34p DIFFIO_RX_R33n	DIFFOUT_R33p DIFFOUT_R34p		

Pin List U324



Version 2017.12.15

k Number								No
it italiiboi	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
	6 VREFB6N0	IO	+		DIFFIO_RX_R35p	DIFFOUT_R35p	High_Speed	G11
	6 VREFB6N0	10	†		DIFFIO RX R36p	DIFFOUT_R36p	High_Speed	C18
	6 VREFB6N0	io	1		DIFFIO RX R35n	DIFFOUT R35n	High Speed	G12
	6 VREFB6N0	IO	1		DIFFIO RX R36n	DIFFOUT R36n	High Speed	B18
	6 VREFB6N0	10			DIFFIO_RX_R37p	DIFFOUT_R37p	High_Speed	E15
	6 VREFB6N0	10			DIFFIO RX R38p	DIFFOUT R38p	High Speed	D17
	6 VREFB6N0	IO	1		DIFFIO_RX_R37n	DIFFOUT_R37n	High_Speed	D15
	6 VREFB6N0	IO	1		DIFFIO_RX_R38n	DIFFOUT_R38n	High Speed	C17
	7 VREFB7N0	10			DIFFIO RX T1p	DIFFOUT T1p	High Speed	E14
	7 VREFB7N0	10			DIFFIO_RX_T2p	DIFFOUT_T2p	High_Speed	B17
	7 VREFB7N0	10			DIFFIO_RX_T1n	DIFFOUT_T1n	High Speed	D14
	7 VREFB7N0	10	1		DIFFIO RX T2n	DIFFOUT T2n	High Speed	B16
	7 VREFB7N0	10	1		DIFFIO_RX_T9p	DIFFOUT_T9p	High Speed	D12
	7 VREFB7N0	10	1				High Speed	A17
	7 VREFB7N0	10	1		DIFFIO RX T9n	DIFFOUT T9n	High Speed	D13
	7 VREFB7N0	10	VREFB7N0				High_Speed	A16
	7 VREFB7N0	10			DIFFIO_RX_T10p	DIFFOUT_T10p	High_Speed	C16
	7 VREFB7N0	10	1		DIFFIO RX T11p	DIFFOUT T11p	High Speed	A15
	7 VREFB7N0	10			DIFFIO_RX_T10n	DIFFOUT_T10n	High Speed	C15
	7 VREFB7N0	10			DIFFIO RX T11n	DIFFOUT T11n	High_Speed	A14
	7 VREFB7N0	10			DIFFIO RX T12p	DIFFOUT T12p	High Speed	C14
	7 VREFB7N0	10	†		DIFFIO_RX_T13p	DIFFOUT_T13p	High Speed	B14
	7 VREFB7N0	io	†		DIFFIO_RX_T12n	DIFFOUT_T12n	High_Speed	C13
	7 VREFB7N0	10	 	 	DIFFIO RX T13n	DIFFOUT T13n	High Speed	B13
	7 VREFB7N0	IO	+	1	DIFFIO RX 11311	DIFFOUT T20p		F11
	7 VREFB7N0 7 VRFFB7N0	IIO	+		DIFFIO_RX_120p DIFFIO_RX_T21p	DIFFOUT T21p	High_Speed High_Speed	C12
		10	+					
	7 VREFB7N0		 		DIFFIO RX T20n	DIFFOUT T20n	High Speed	F12
	7 VREFB7N0	10	 		DIFFIO_RX_T21n	DIFFOUT_T21n	High_Speed	B12
	7 VREFB7N0	10	 		DIFFIO_RX_T22p	DIFFOUT_T22p	High Speed	C11
	7 VREFB7N0	10	 		DIFFIO RX T23p	DIFFOUT T23p	High Speed	A13
	7 VREFB7N0	10	 		DIFFIO_RX_T22n	DIFFOUT_T22n	High_Speed	B11
	7 VREFB7N0	10			DIFFIO_RX_T23n	DIFFOUT_T23n	High_Speed	A12
	8 VREFB8N0	10	CLK4p		DIFFIO RX T24p	DIFFOUT T24p	Low Speed	D10
	8 VREFB8N0	10			DIFFIO_RX_T25p	DIFFOUT_T25p	Low_Speed	A11
	8 VREFB8N0	10	CLK4n		DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	D9
	8 VREFB8N0	10			DIFFIO RX T25n	DIFFOUT T25n	Low Speed	A10
	8 VREFB8N0	10	CLK5p		DIFFIO RX T26p	DIFFOUT_T26p	Low_Speed	F10
	8 VREFB8N0	10	1		DIFFIO_RX_T27p	DIFFOUT_T27p	Low_Speed	A9
	8 VREFB8N0	10	CLK5n		DIFFIO RX T26n	DIFFOUT T26n	Low Speed	G10
	8 VREFB8N0	10	CENTON		DIFFIO_RX_T27n	DIFFOUT_T27n	Low_Speed	A8
	8 VREFB8N0	10	† 		DIFFIO_RX_T28p	DIFFOUT T28p	Low Speed	B9
	8 VREFB8N0	in	† 		DIFFIO RX T29p	DIFFOUT T29p	Low Speed	C10
	8 VREFB8N0	10	 	DEV_CLRn	DIFFIO_RX_T28n	DIFFOUT_T28n	Low_Speed	DO
	8 VREFB8N0	10	+	DEV_GENT	DIFFIO RX T29n	DIFFOUT_T29n	Low_Speed	C9
	8 VREFB8N0	10	+	DEV OE	DIFFIO_RX_12911 DIFFIO_RX_T30p	DIFFOUT T30p	Low_Speed	D8
	8 VRFFB8N0	IO	+	DEV OE	DIFFIO RX 130p	DIFFOUT 130p		A7
	8 VREFB8N0	10			DIFFIG BY TOO.	DIFFOLIT TOO.	Low_Speed	D7
	8 VREFB8N0	10	VREFB8N0		DIFFIO RX T30n	DIFFOUT_T30n	Low Speed	B7
	8 VREFB8N0	10	VKEFDOINU	CONFIG OF			Low Speed	G9
	8 VREFB8N0	10		CONFIG_SEL	DIFFIO DV TO4-	DIFFOLIT TO1-	Low_Speed	
				nCONFIG	DIFFIO_RX_T31p	DIFFOUT_T31p	Low_Speed	A6
	0 VREFDONO	land sale						H9
	8 VREFB8N0	Input only		IICONITIG	DIESIO DV TO	DIFFOUR TAL	Low Speed	
	8 VREFB8N0 8 VREFB8N0	10		TICONI IG	DIFFIO_RX_T31n	DIFFOUT_T31n	Low_Speed	A5
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0	10 10		III.CON IG	DIFFIO_RX_T32p	DIFFOUT_T32p	Low_Speed Low_Speed	C6
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0	10 10 10		III.CONITS	DIFFIO_RX_T32p DIFFIO_RX_T33p	DIFFOUT_T32p DIFFOUT_T33p	Low_Speed Low_Speed Low Speed	C6 C8
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0	10 10 10 10		INCOME TO	DIFFIO_RX_T32p DIFFIO_RX_T33p DIFFIO_RX_T32n	DIFFOUT_T32p DIFFOUT_T33p DIFFOUT_T32n	Low_Speed Low_Speed Low_Speed Low_Speed	C6 C8 B5
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0	IO		INCOME!	DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T32n	DIFFOUT_T32p DIFFOUT_T33p DIFFOUT_T32n DIFFOUT_T33n	Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed	C6 C8 B5 C7
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0	O		INCOME TO	DIFFIO_RX_T32p DIFFIO_RX_T33p DIFFIO_RX_T32n DIFFIO_RX_T33n DIFFIO_RX_T34p	DIFFOUT_T32p DIFFOUT_T33p DIFFOUT_T32n DIFFOUT_T33n DIFFOUT_T34p	Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed	C6 C8 B5 C7 C5
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0				DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p	DIFFOUT_T32p DIFFOUT_T33p DIFFOUT_T33p DIFFOUT_T32n DIFFOUT_T32n DIFFOUT_T34p DIFFOUT_T35p	Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed	C6 C8 B5 C7 C5 A4
	8 VREFBBN0 8 VREFBBN0 8 VREFBBN0 8 VREFBBN0 8 VREFBBN0 9 VREFBBN0 8 VREFBBN0 8 VREFBBN0 9 VREFBBN0 9 VREFBBN0 8 VREFBBN0 8 VREFBBN0	O		CRC_ERROR	DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32p DIFFIO RX T32n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35p DIFFIO RX T35p DIFFIO RX T34n	DIFFOUT T32p	Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed	C6 C8 B5 C7 C5 A4 C4
	8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 9 VREFBBNO 8 VREFBBNO 9 VREFBBNO 8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 9 VREFBBNO 9 VREFBBNO 9 VREFBBNO				DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T32n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T34n DIFFIO RX T35p	DIFFOUT T32p DIFFOUT T33p DIFFOUT T33n DIFFOUT, T32n DIFFOUT, T33n DIFFOUT, T34p DIFFOUT, T34p DIFFOUT, T34p DIFFOUT, T34n DIFFOUT, T34n	Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4
	8 VREFBBN0 8 VREFBBN0 8 VREFBBN0 8 VREFBBN0 8 VREFBBN0 9 VREFBBN0 8 VREFBBN0 8 VREFBBN0 9 VREFBBN0 9 VREFBBN0 8 VREFBBN0 8 VREFBBN0	O			DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32p DIFFIO RX T32n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35p DIFFIO RX T35p DIFFIO RX T34n	DIFFOUT T32p	Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed Low_Speed	C6 C8 B5 C7 C5 A4 C4
	NREFB8NO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35p	DIFFOUT T32p DIFFOUT T33p DIFFOUT T33n DIFFOUT, T32n DIFFOUT, T33n DIFFOUT, T34p DIFFOUT, T34p DIFFOUT, T34p DIFFOUT, T34n DIFFOUT, T34n	Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3
	8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 9 VREFBBNO 8 VREFBBNO 8 VREFBBNO 8 VREFBBNO 9 VREFBBNO 9 VREFBBNO 9 VREFBBNO 9 VREFBBNO 9 VREFBBNO 9 VREFBBNO 8 VREFBBNO 8 VREFBBNO 8 VREFBBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T320 DIFFIO RX T320 DIFFIO RX T320 DIFFIO RX T320 DIFFIO RX T320 DIFFIO RX T320 DIFFIO RX T340 DIFFIO RX T355 DIFFIO RX T355 DIFFIO RX T356 DIFFIO RX T356 DIFFIO RX T356	DIFFOUT T32b DIFFOUT T32b DIFFOUT T32b DIFFOUT T32h DIFFOUT T32h DIFFOUT T34d DIFFOUT, T34d DIFFOUT, T34d DIFFOUT, T34n DIFFOUT, T35n DIFFOUT, T35n DIFFOUT T35n DIFFOUT T35n	Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8
	8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0 8 VREFB8N0	O		CRC_ERROR	DIFFIO RX T320 DIFFIO RX T330 DIFFIO RX T330 DIFFIO RX T331 DIFFIO RX T331 DIFFIO RX T340 DIFFIO RX T355 DIFFIO RX T355 DIFFIO RX T356 DIFFIO RX T370 DIFFIO RX T370 DIFFIO RX T370 DIFFIO RX T366	DIFFOUT T32b DIFFOUT T32b DIFFOUT T32b DIFFOUT T32h DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35p DIFFOUT T37p DIFFOUT T37p	Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed Low, Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3 H8
	8 VREFB8N0 8 VREFB8N0	O		CRC_ERROR INSTATUS	DIFFIO RX T320	DIFFOUT T32p DIFFOUT T33p DIFFOUT T33p DIFFOUT, T32n DIFFOUT, T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T35p DIFFOUT T35p DIFFOUT T35p DIFFOUT T36p DIFFOUT T36p DIFFOUT T36p DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p	Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3 H8 B3
	8 VREFB8N0 8 VREFB8N0	O		CRC_ERROR INSTATUS	DIFFIO RX T320	DIFFOUT T32p	Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3 H8
	8 VREFB8N0 8 VREFB8N0	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35p DIFFIO RX T37p DIFFIO RX T37p DIFFIO RX T37p		Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3 H8 B3 D6 A2
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T320	DIFFOUT T32p	Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3 H8 B3 D6
	8 VREFB8N0 8 VREFB8N0	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38p DIFFOUT T38p DIFFOUT T38p DIFFOUT T38p DIFFOUT T38p	Low Speed Low Speed	C6 C8 B5 C7 C7 C5 A4 C4 B4 G8 A3 H8 B3 D6 A2 D5 B2
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C8 B5 C7 C5 A4 C4 B4 G8 A3 H8 B3 D6 A2 D5 B2
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C2 S5 C7 C7 C5 C5 C6 C7 C7 C7 C7 C7 C7 C7
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C8 B5 C7 C5 C5 A4 C4 B4 C4 C4 B4 C5 C5 C5 C5 C4 C4 C4 C
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S5 C7 C7 C5 C5 C4 B4 G8 B3 B3 B3 B3 D5 D5 A2 D5 E2 E2 E3 V/18 V/1
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C2 C2 B5 C7 C7 C5 A4 C4 C4 B4 G8 A3 H8 B3 D6 A2 D5 B2 E2 E3 E3 V18 V1 U4
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S5 C7 C7 C5 C5 C4 B4 G8 B4 G8 B3 D6 D6 D5 S2 E3 V/18 V/1 U/4 U/4
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C2 C2 B5 C7 C7 C5 A4 C4 C4 B4 G8 A3 H8 B3 B3 D6 A2 D5 B2 E2 E3 V18 V1 U14 U14 U14 U10 U10 U10 U10
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S5 C7 C7 C5 C8 A4 C4 C4 B4 B4 B9 B3 C0 C5 C5 C7 C7 C7 C4 C4 C4 C4 C4 C4 C4 C4 C4 C4 C4 C4 C4
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C2 C3 C5 C5 C5 C5 C5 C4 C4 C4 C4 C4 C5 C5 C5 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C8 S5 C7 C7 C7 C7 C6 A4 A4 C4 C4 B4 B4 B9 B3 D6 D5 B2 E2 E3 V1 U14 U10 R7 R7 N5
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C2 C3 C5 C5 C5 C5 C5 C4 C4 C4 C4 C4 C5 C5 C5 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6 C6
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C8 B5 C7 C7 C5 A4 A4 C4 C4 B4 B4 B9 B3 B3 D6 A2 D5 B2 E2 E3 V/I U14 U10 R7 N5 N2 N17 N12
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S5 C7 C7 C5 A4 A4 C4 C4 B4 B4 B9 B3 D6 A2 D5 B2 E2 E3 V11 U14 U10 R7 N5 N2 N17 N12
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 C3 C5 C5 C5 C7 C7 C5 C5 C6 C4 C4 C4 C4 C4 C5 C5 C6 C7 C7 C5 C6 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C8 B5 C7 C7 C5 A4 A4 C4 C4 B4 B4 B8 B3 C6 D6 D6 B2 E2 E3 E3 V18 V1 U10 U10 U10 U114 U110 U110 U110 U110 U
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 C3 C5 C5 C5 C7 C7 C5 C5 C6 C7 C7 C5 C6 C7 C7 C6 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C8 R5 C3 R5 C7 C7 C5 A4 A4 C4 C4 B4 B4 B8 B3 C6 C7 C9 C9 C9 C9 C9 C9 C9 C9 C9 C9 C9 C9 C9
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S5 C7 C7 C5 C5 C4 B4 G8 B3 B3 B3 B3 B3 B3 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7 C7
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S3 S5 C3 S5 C4 C4 C4 C4 B4 B4 B4 G8 B3 B3 D6 D5 B2 E2 E3 B7 V1 U14 U110 R7 R7 N5 N2 N12 N112 N112 N110 N112 N110 K9 K9 K6 K13
	NEFEBNO	O		CRC_ERROR INSTATUS	DIFFIO RX T32p DIFFIO RX T32p DIFFIO RX T33p DIFFIO RX T32n DIFFIO RX T33n DIFFIO RX T33n DIFFIO RX T34p DIFFIO RX T34p DIFFIO RX T35n DIFFIO RX T35n DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T36p DIFFIO RX T37p DIFFIO RX T38p	DIFFOUT T32p DIFFOUT T33b DIFFOUT T33b DIFFOUT T33c DIFFOUT T33n DIFFOUT T34p DIFFOUT T34p DIFFOUT T34p DIFFOUT T35c DIFFOUT T35c DIFFOUT T36c DIFFOUT T36c DIFFOUT T36c DIFFOUT T37p DIFFOUT T37p DIFFOUT T37p DIFFOUT T38c	Low Speed Low Speed	C6 C3 S5 C7 C7 C5 C5 C4 A4 C4 B4 B4 B8 B3 B3 D6 A2 D5 B2 E2 E2 E2 E3 V18 V1 U4 U10 R7 N15 N17 N15 N17 N15 N17 N16 N17 N110 M114 L4 L69 K66

Page 8 of 9



lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
		GND						G4
		GND						G2
		GND						F8
		GND						F17
		GND						E6
		GND						E13
		GND						E10
		GND						D3
		GND						B6
		GND						B15
		GND						B10
		GND						A18
		GND						A1
		VCCIO1A						
		VCCIO1A VCCIO1A						H5 G5
		VCCIO1A VCCIO1B						K5
		VCCIO1B						J5
		VCCIO2						M5
		VCCIO2						L6
		VCCIO2						L5
		VCCIO3						P9
		VCCIO3						P8
		VCCIO3						P7
		VCCIO3						N9
		VCCIO4						P12
		VCCIO4						P11
		VCCIO5						M13
		VCCIO5						L14
		VCCIO5						L13
		VCCIO5						K14
		VCCIO6						J14
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G14
		VCCIO6						G13
		VCCIO7						E12
		VCCIO7						E11
		VCCIO7						D11
		VCCIO8						F9
		VCCIO8						E9
		VCCIO8						E8
		VCCIO8						E7
		VCCA1						M6
		VCCA2						F14
		VCCA3						F3
	+	VCCA3	<u> </u>				+	F6
	+	VCCA3	<u> </u>				+	F4
		VCCA3					+	P13
	+	VCC_ONE	<u> </u>				+	L9
	+	VCC_ONE	+					K10
	-							
	-	VCC ONE VCC ONE						J9 H10
	-	VCC_ONE						
		VCC_ONE						N6
		VCC ONE						F13
		VCC_ONE						C3
		VCC_ONE						F7
	1	VCC ONE	1	i e		ı	I	N13

(1) For more information about pin definition and pin connection guidelines, refer to the Intel MAX 10 FPGA Device Family Pin Connection Guidelines.

