











V SUPPLY **FEATURES** 10u,50V TC2117 V\_SUPPLY) Operating Supply Voltage 8V-60V 10u,50V · 2.3A Sink and 1.7A Source Gate Drive Current C24 C51 15u, 100v Capability Integrated Dual Shunt Current Amplifiers With 2 Adjustable Gain and Offset Integrated Buck Converter to Support up to 1.5A External Load Independent Control of 3 or 6 PWM Inputs R21 Bootstrap Gate Driver With 100% Duty Cycle V\_SUPPLY Programmable Dead Time to Protect External RT\_CLK SS\_TR 55 X FETs from Shoot Through COMP EN\_BUCK 54 VSENSE PVDD2 Programmable Overcurrent Protection of 53 PWRGD PVDD2 C39 100n **External MOSFETs** 52 OCTW BST\_BK 1 <sub>C27</sub> FAULT (1 6 Thermally Enhanced 56-Pin TSSOP Pad Down FAULT PH R20 10k 50 + C33 DTC PH DCA Package 49 M\_PWM BIAS 48 M\_OC BST\_A 100u SENS14 → H3\_VS 10 <del>47</del> ▶ M\_H1 GAIN GH\_A 11 46 OC\_ADJ SH\_A 45 DM\_L1 DC\_CALD-12 DC\_CAL GL\_A H1\_LOW GVDD SL\_A 43 **⊸**H2\_VS CP1 BST\_B <u>42</u> **⊳**M\_H2 CP2 GH\_B SH\_B 41 EN\_GATED 16 EN\_GATE H2\_VS H1D 17 <u>40</u> **D** M\_L2 INH\_A GL\_B 39 dH2\_LOW L1D 18 INL\_A SL\_B H2D 19 SENS34 H1\_VS 38 INH\_B BST\_C L2D 20 INLB <del>37</del> ▶ M\_H3 GH\_C C52 21 INH\_C 36 SH\_C H3\_VS MCU must sense the voltage at each phase. 2.2u L3D 22 <del>35</del> ▶ M\_L3 INL\_C GL\_C 23 34 -**⊲**H3\_L0W C20 DVDD SL\_C 33 2.2u REF SN1 32 501 SP1 -**d**SH1\_B VĢ¢ 31 502 SN2 SH2\_A 27 AVDD SP2 28 29 AGND PVDD1 DRV8302 V\_SUPPLY 6,20 RECOMMENDED OPERATING CONDITIONS DC supply voltage PVDD1 for normal operation Relative to PGND 10u,50V - Pin 1 Index Area DC supply voltage PVDD2 for buck converter External capacitance on AVDD pin (ceramic cap) 20% tolerano External canacitance on DVDD pin (ceramic cap) 20% tolerance External capacitance on GVDD pin (ceramic cap) 20% tolerance Flying cap on charge pump pins (between CP1 and CP2) (ceramic cap) 20% tolerance Bootstrap cap (ceramic cap) I<sub>DIN\_EN</sub> Input current of digital pins when EN\_GATE is high J<sub>DIN\_DIS</sub> Input current of digital pins when EN\_GATE is low Benjamin Vedder Maximum capacitance on digital input pin Maximum output capacitance on outputs of shunt amplifie Sheet: /Mosfet driver/ Dead time control resistor range. Time range is 50ns (-GND) to 500ns (150k $\Omega$ ) with a linear approximation. kΩ File: Power.sch FAULT pin sink current. Open-drain OCTW pin sink current. Open-drain Title: BLDC Driver 4.9 OCTW pin sink current. Open-drain

External voltage reference voltage for current shurrt amptifiers

Operating switching frequency of gate driver

Og(TOT) = 25 nC or total 30 mA gate driver works average current Size: A4 Date: 21 aug 2015 Rev: 4.9 200 kHz KiCad E.D.A. kicad 0.201510030351+624130ubuntu15.10.1-product Id: 7/7