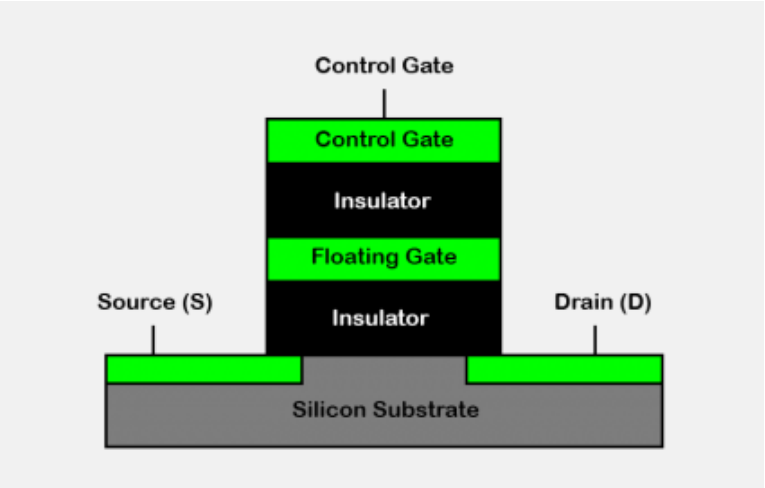
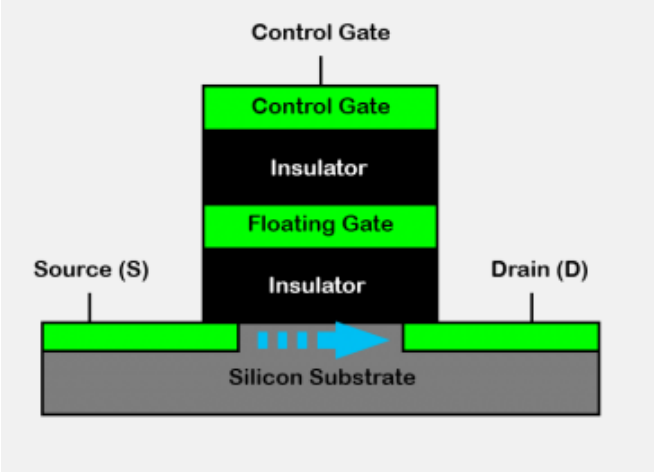
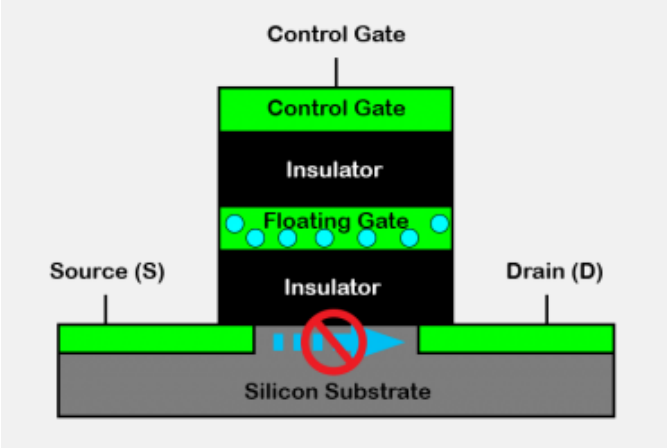
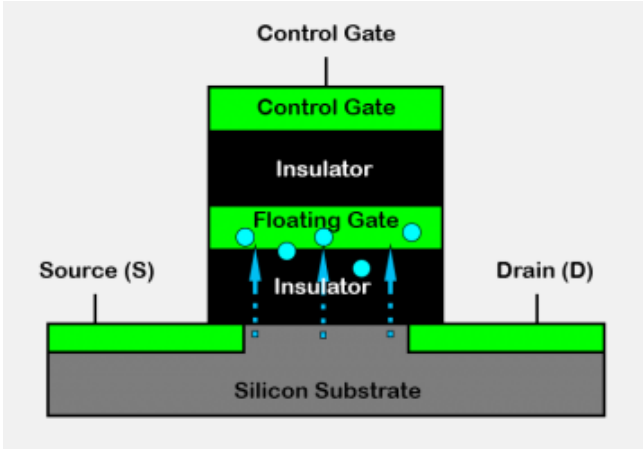
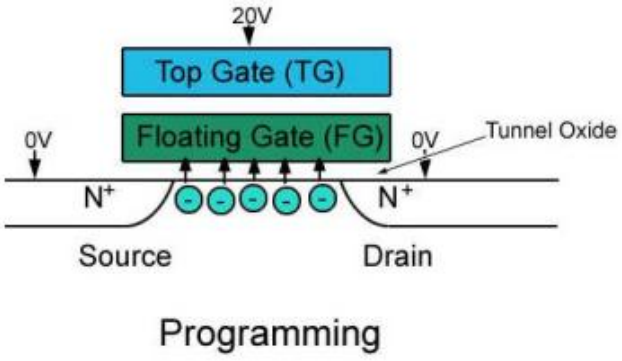




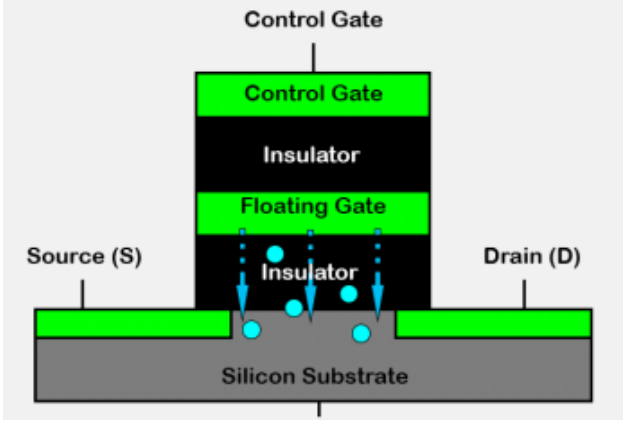


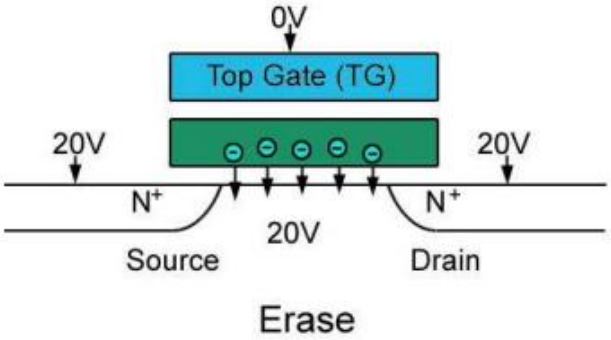
FLOATING GATE STATE	REFERRED TO AS	BINARY VALUE ASSIGNED
CHARGED	PROGRAMMED	ZERO - 0
NO CHARGE	ERASED	ONE - 1



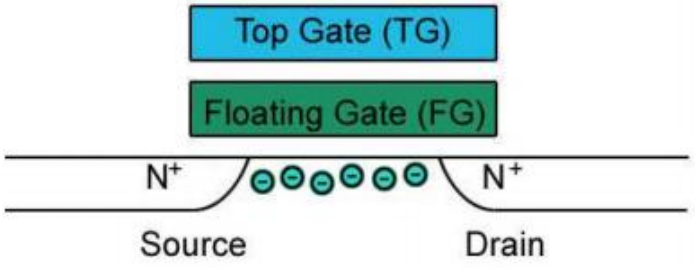


Programming

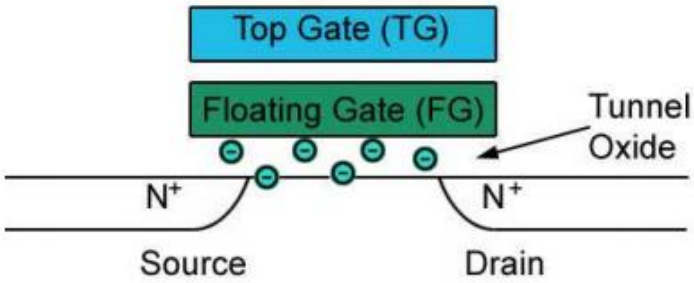




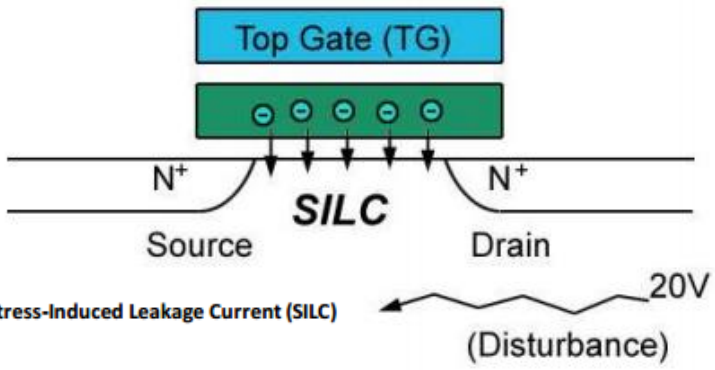
Erase



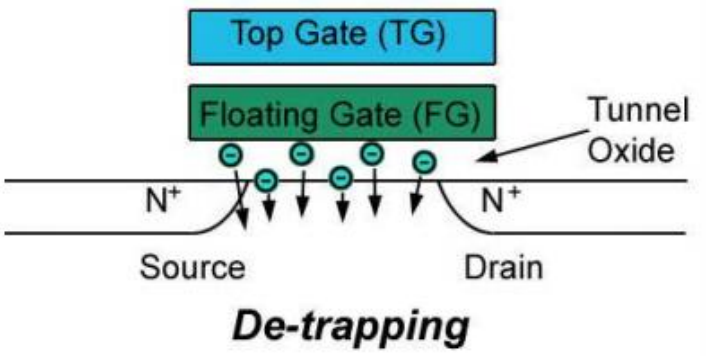
New NAND Flash Memory Cell



End Of Life NAND Flash Memory Cell

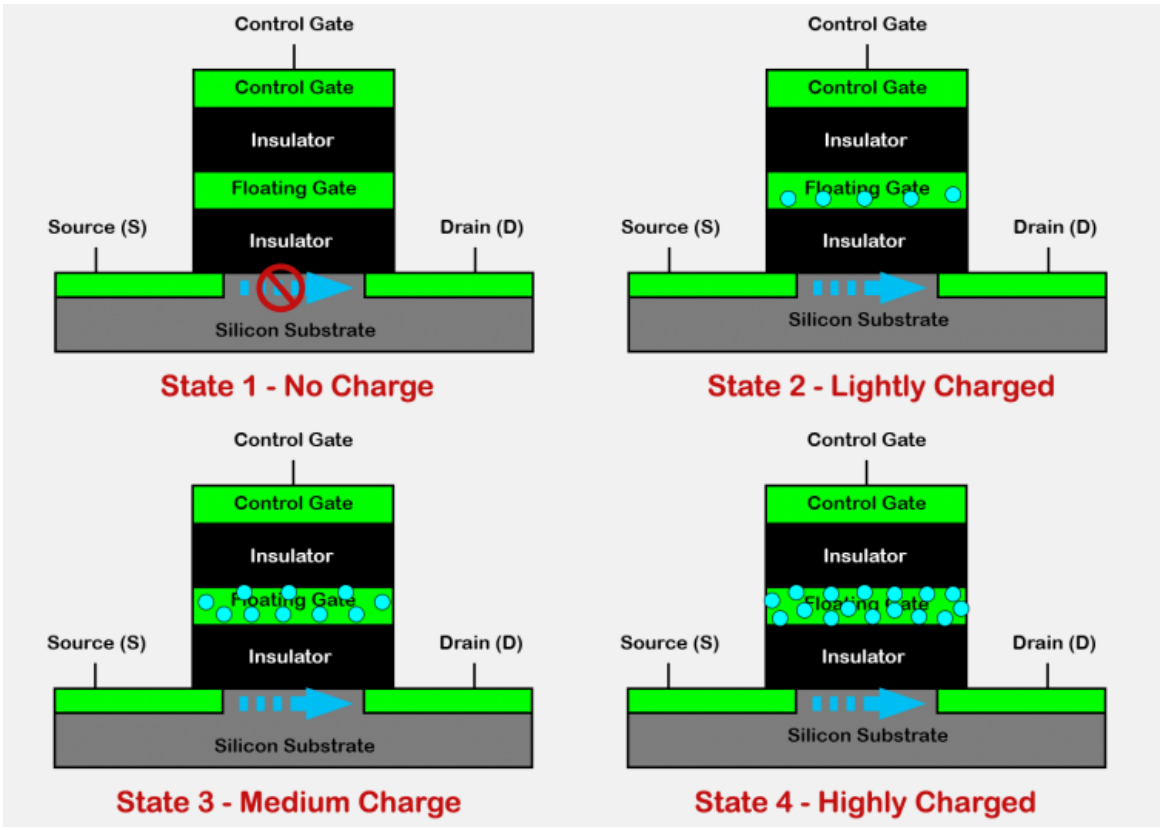


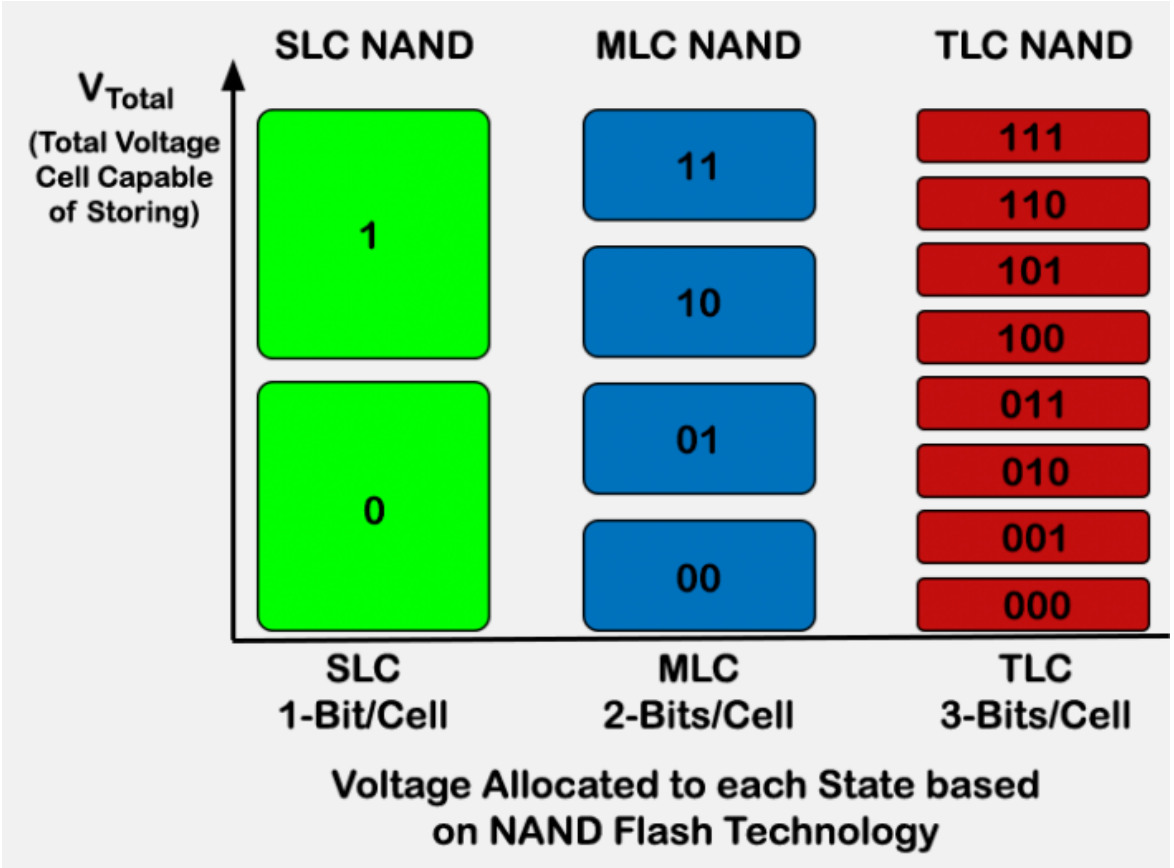
Stress-Induced Leakage Current (SILC)

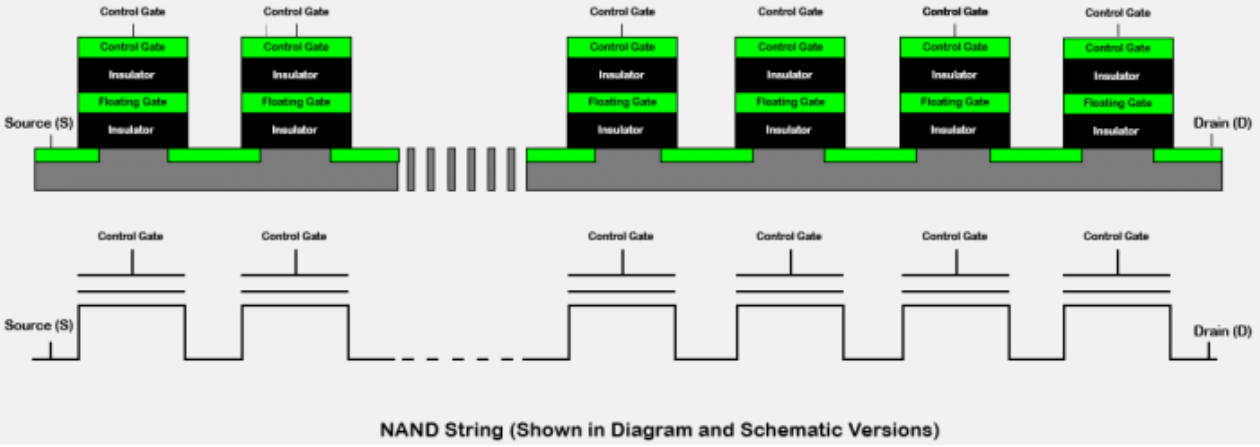


De-trapping

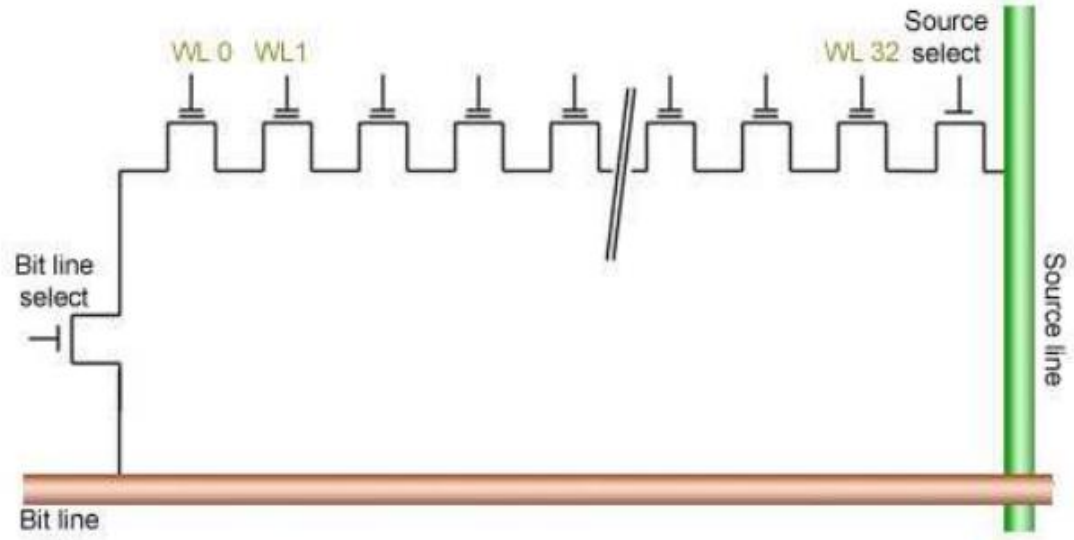
SLC, MLC and TLC NAND Flash

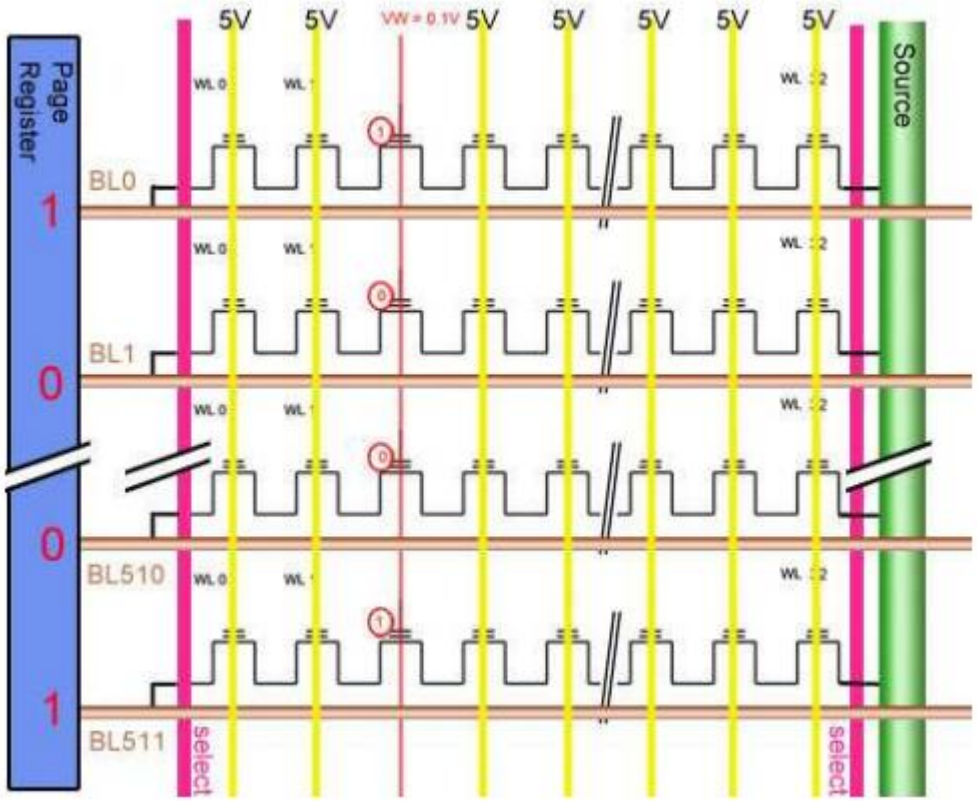


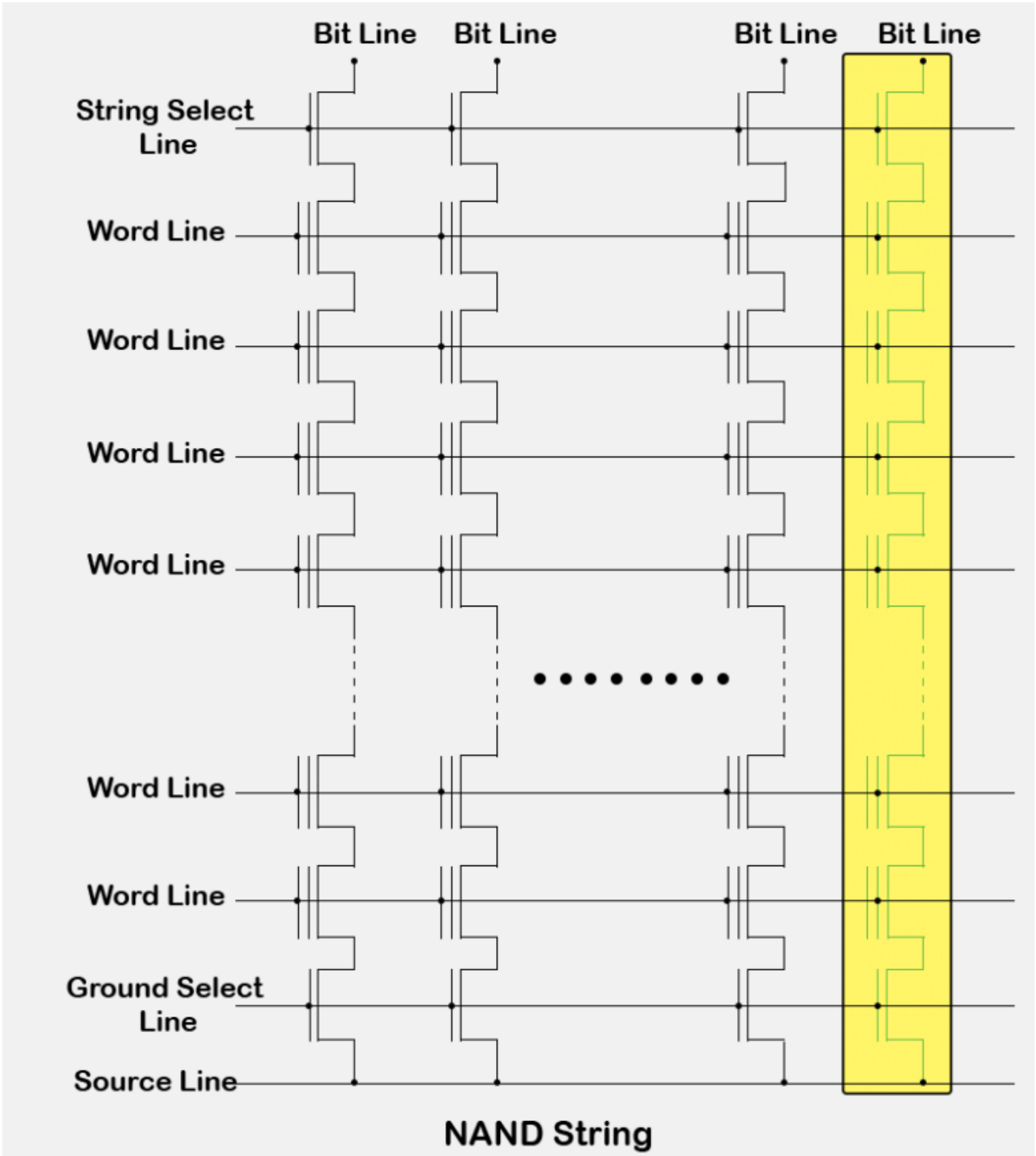




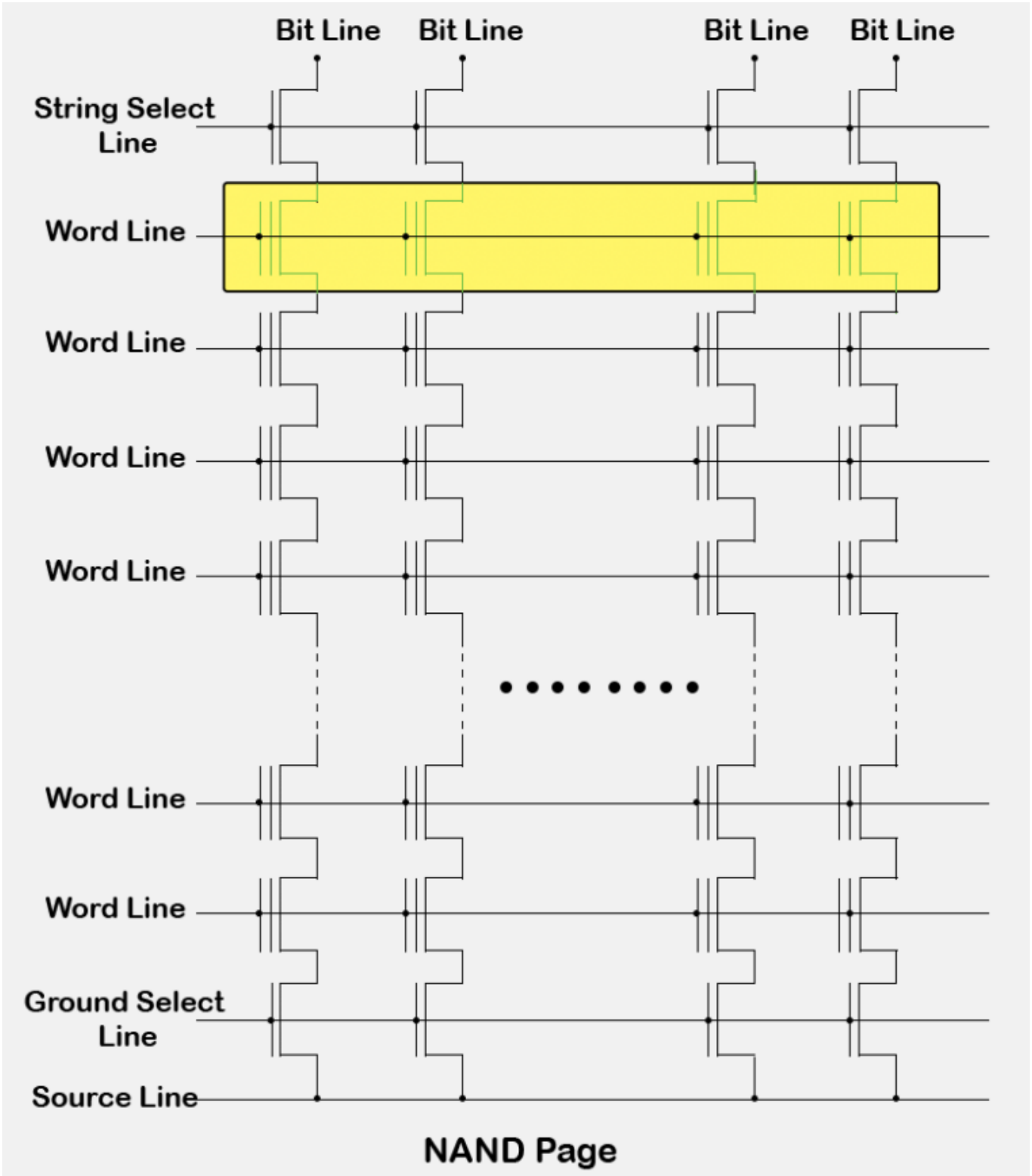
NAND String (Shown in Diagram and Schematic Versions)






Bit Line
Bit Line
Bit Line
Bit Line
String Select Line
Word Line
Word Line
Word Line
Word Line
Word Line
Word Line
Ground Select Line
Source Line

NAND String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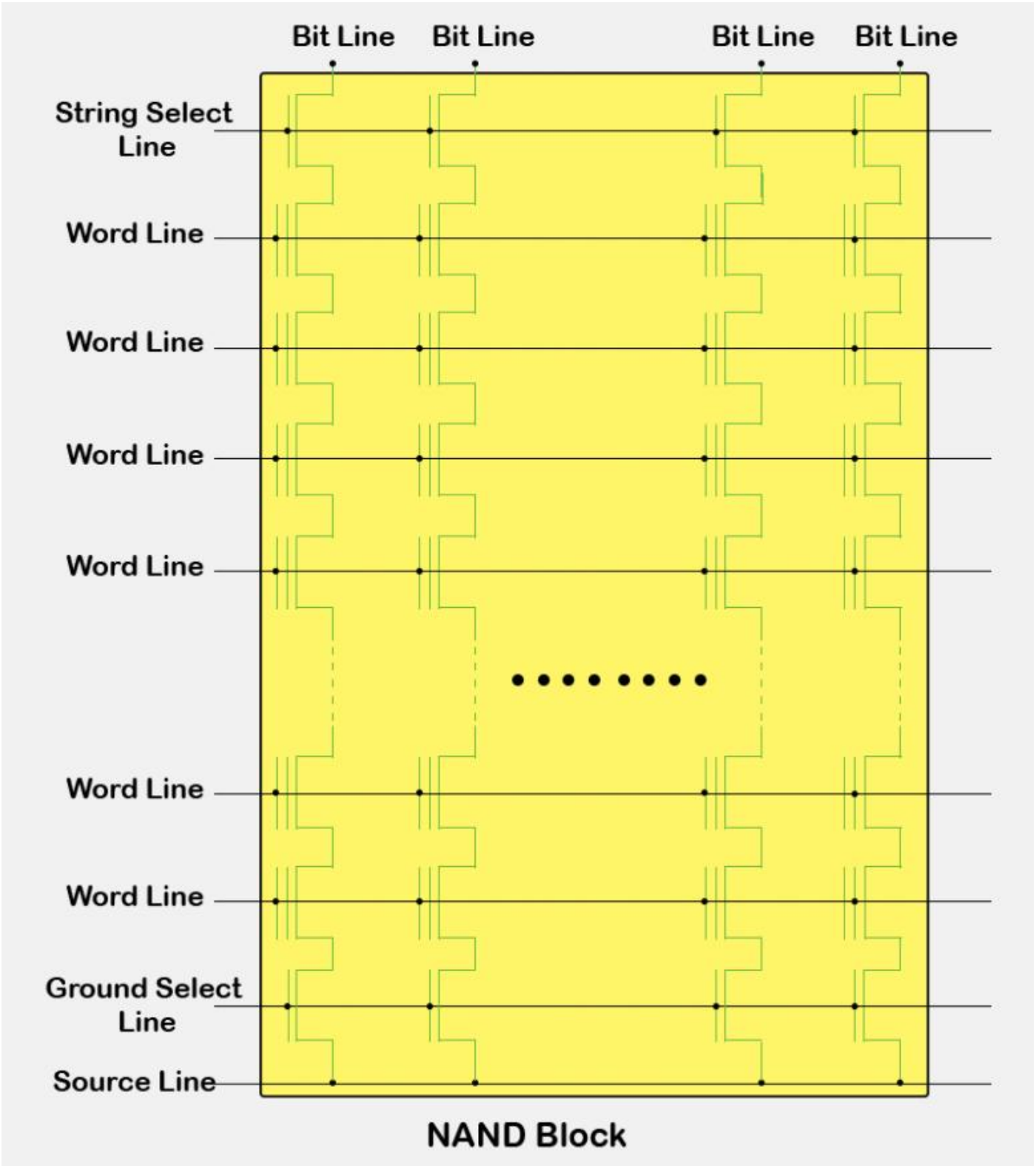
Bit Line
Bit Line
Bit Line
String Select Line
Word Line
Word Line
Word Line
Word Line
Word Line
Word Line
Ground Select Line
Source Line

NAND Page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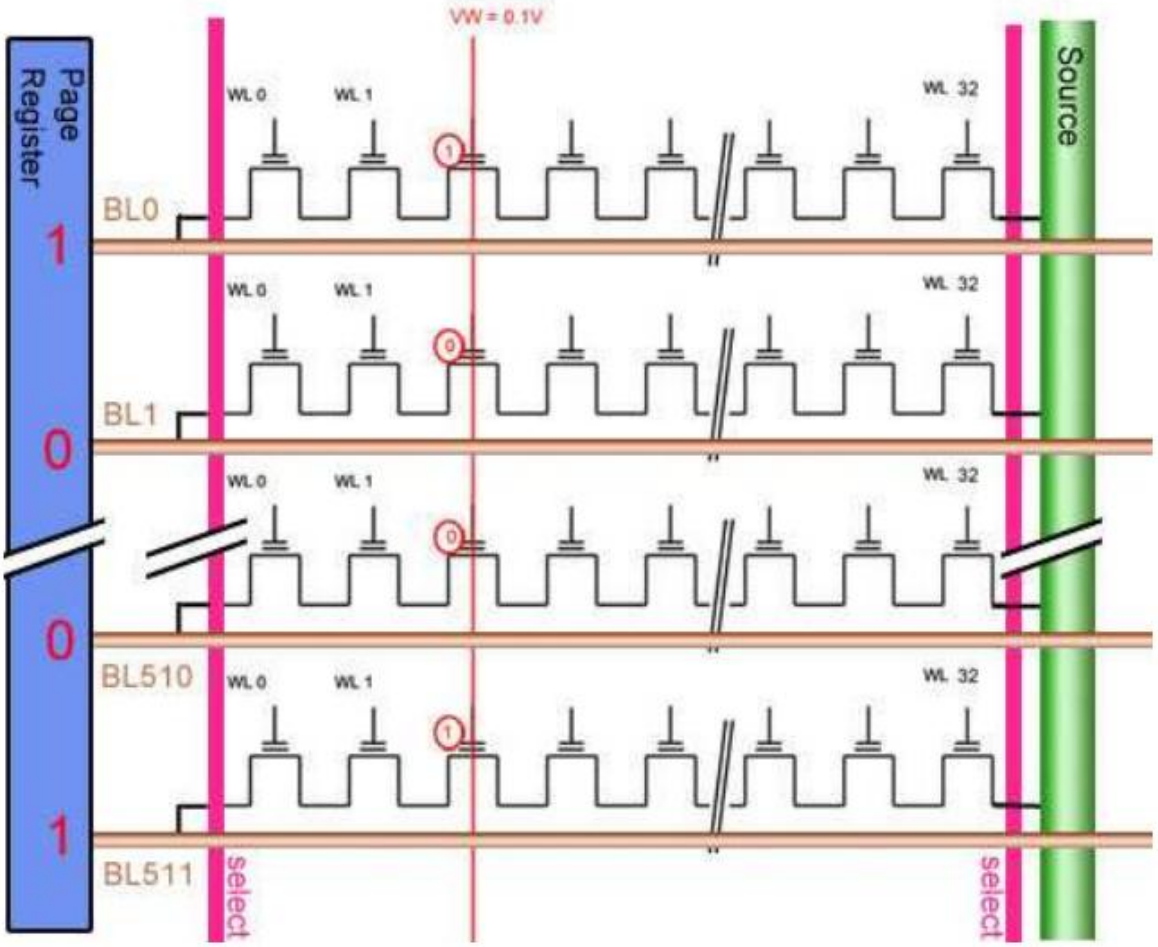
Bit Line
Bit Line
Bit Line
String Select Line
Word Line
Word Line
Word Line
Word Line
Word Line
Word Line
Ground Select Line
Source Line
NAND Block


VW = 0.1V
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0
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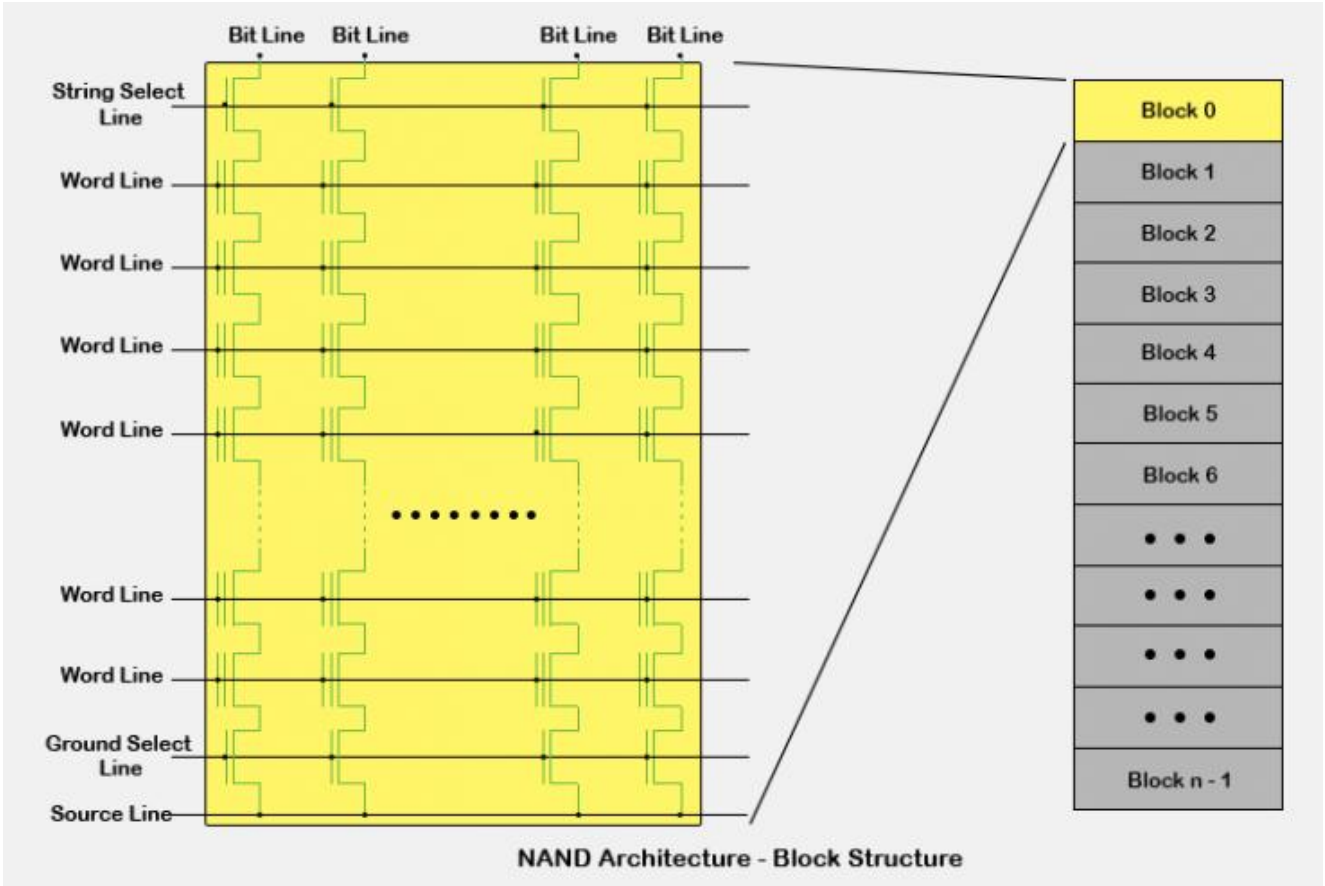
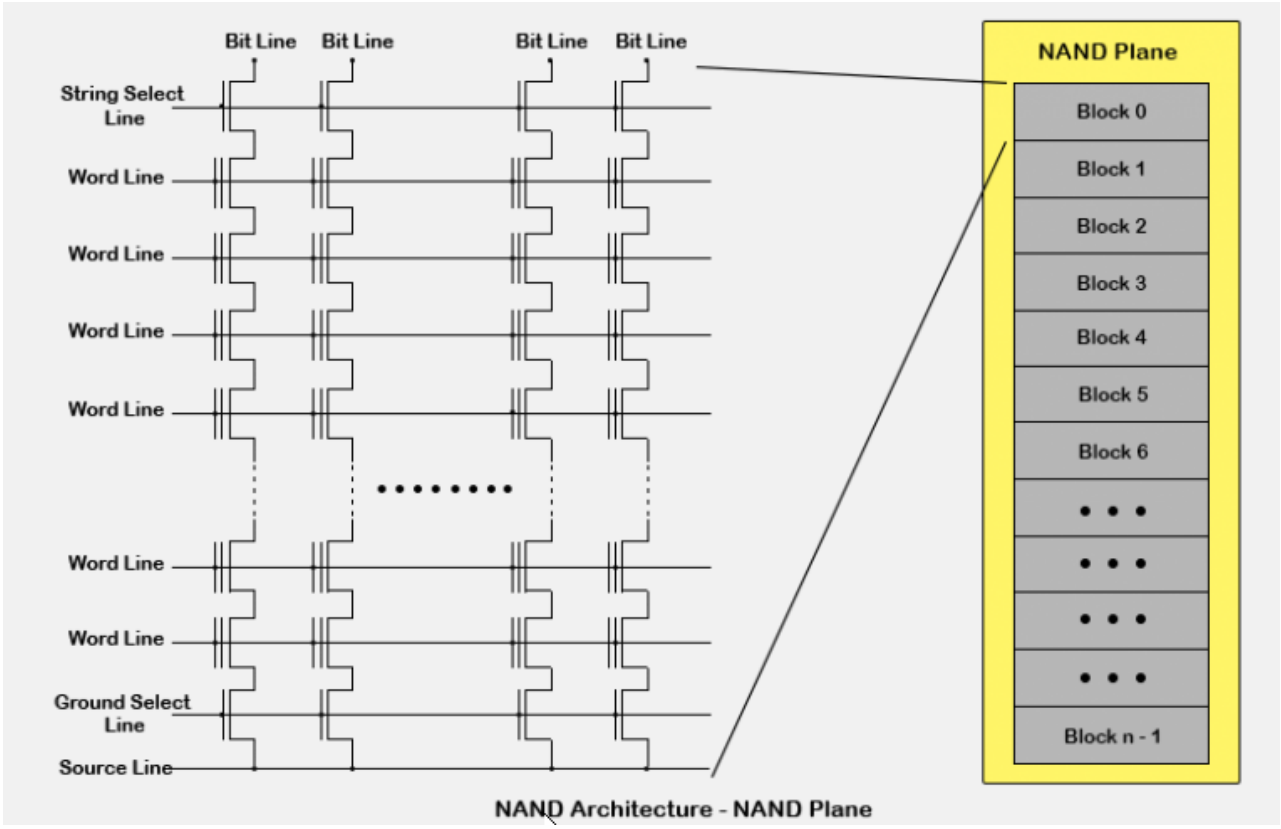
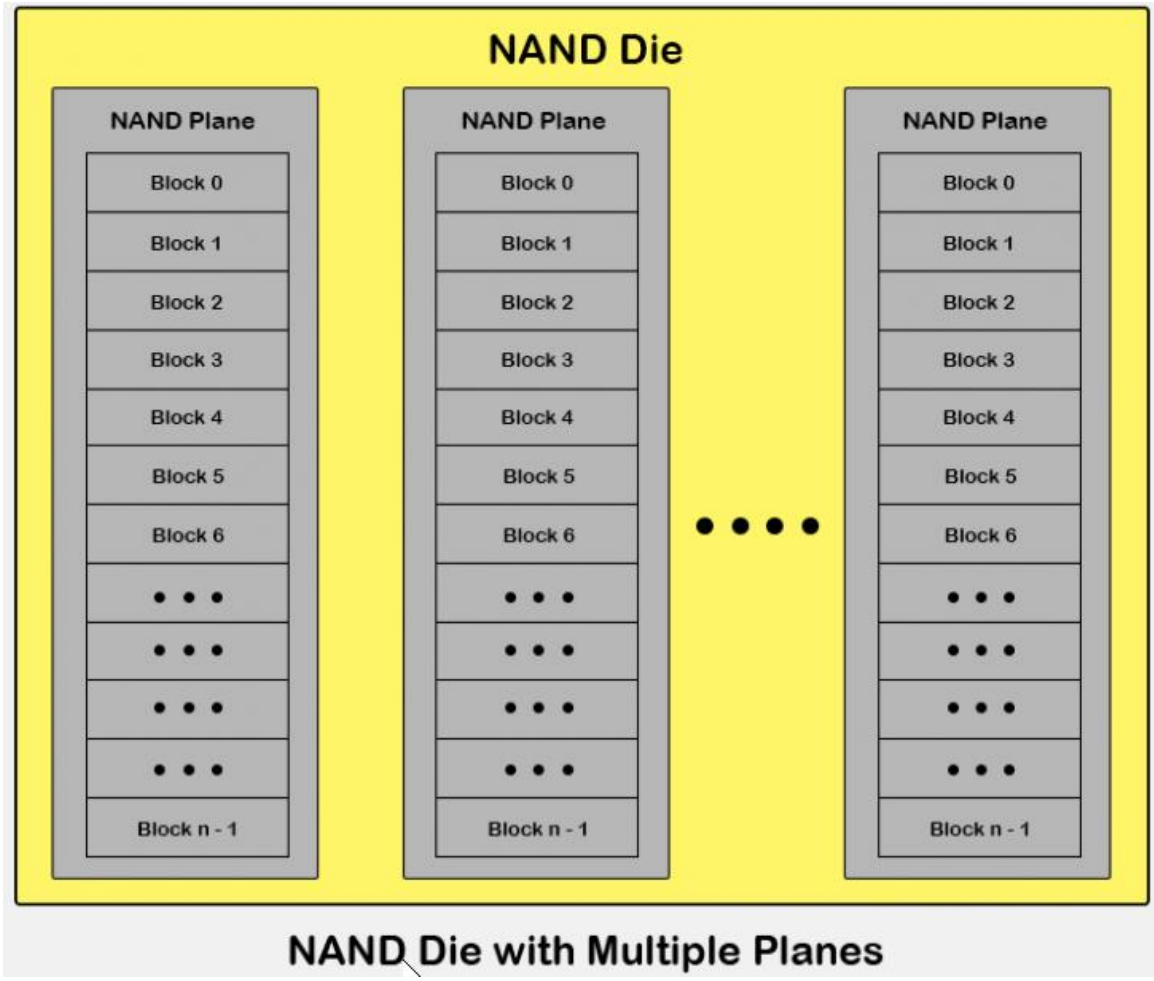
1
BL0
BL1
BL510
BL511
WL 0
WL 1
WL 32
Source
select
select



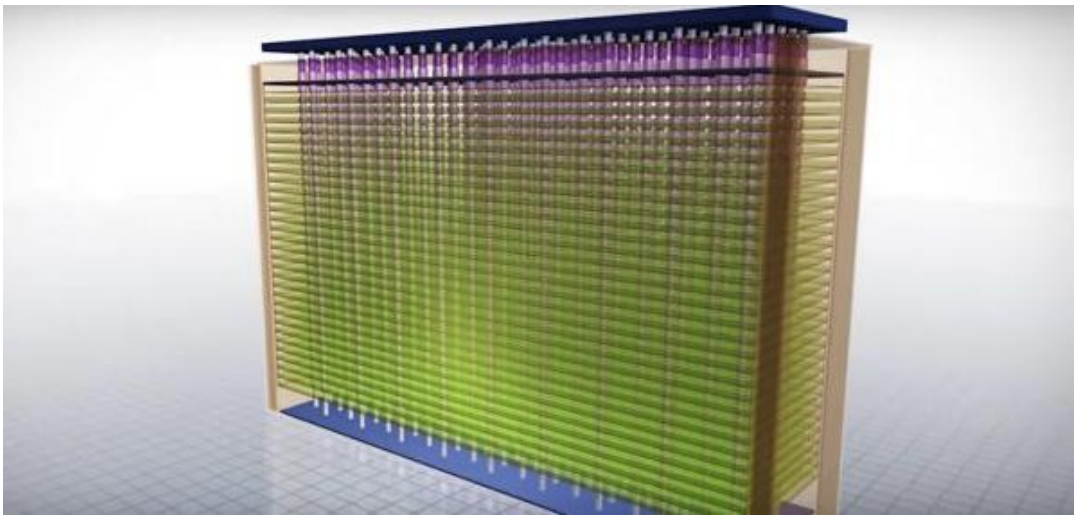
NAND Architecture - Block Structure

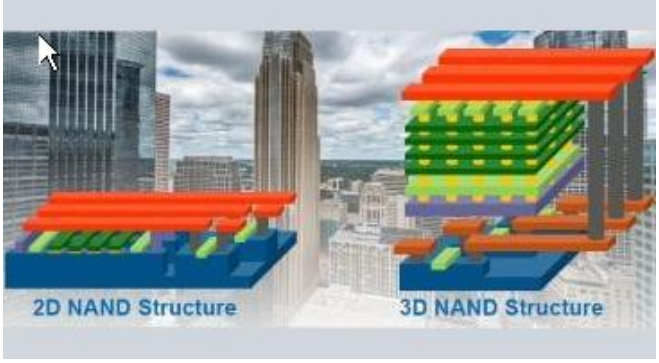


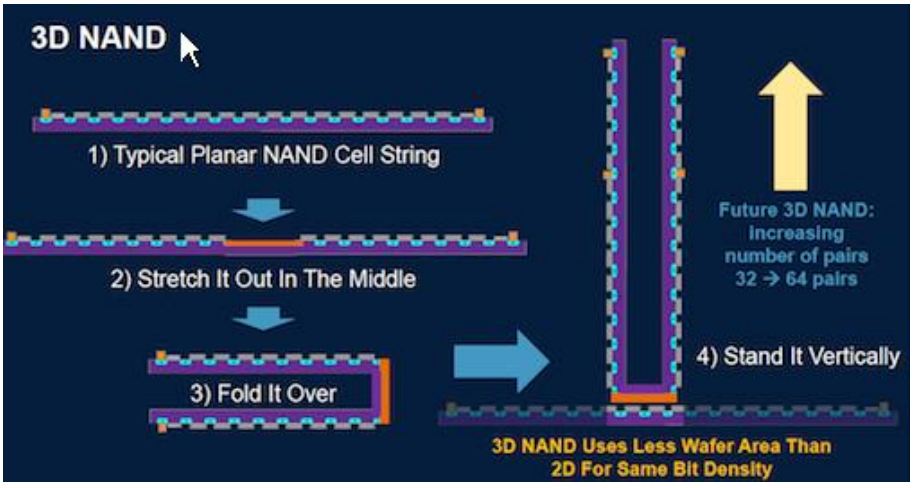
NAND Architecture - NAND Plane

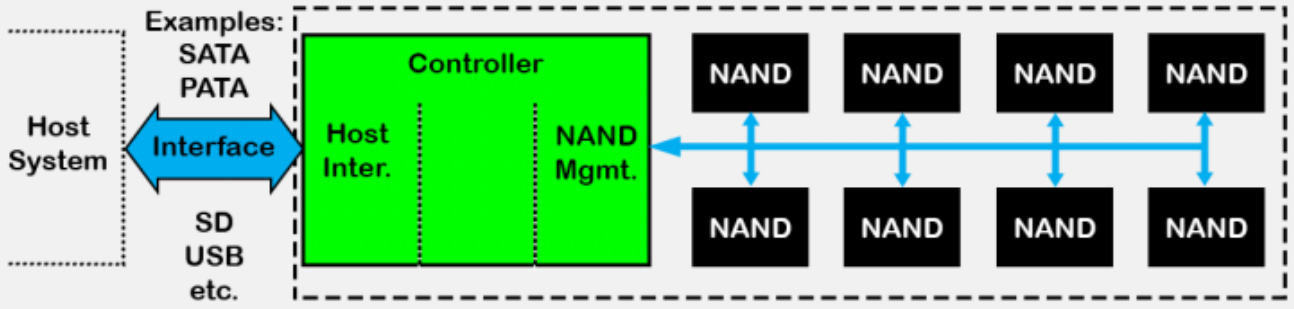


NAND Die with Multiple Planes

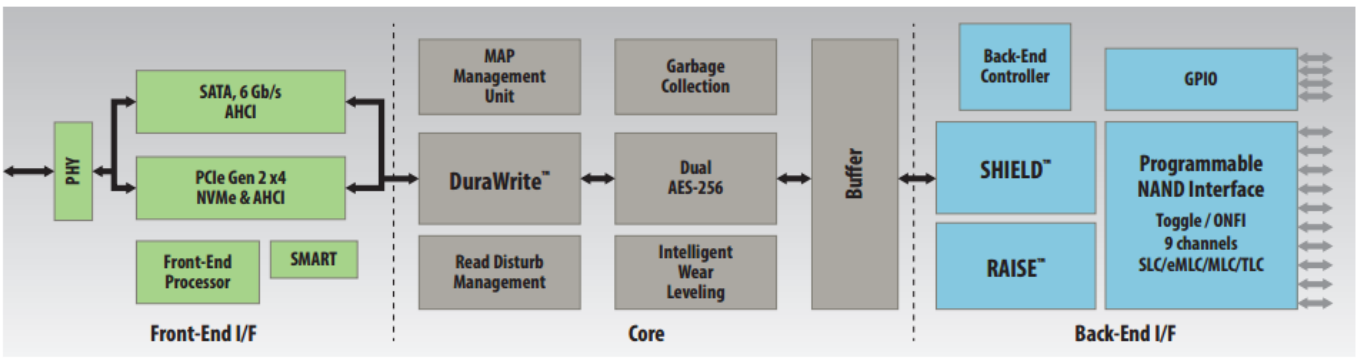



2D NAND Structure
3D NAND Structure


3D NAND
1) Typical Planar NAND Cell String
2) Stretch It Out In The Middle
3) Fold It Over
4) Stand It Vertically
Future 3D NAND:
increasing
number of pairs
32 → 64 pairs
3D NAND Uses Less Wafer Area Than
2D For Same Bit Density



Basic Solid State Drive (SSD) Architecture



SF3700 Block Diagram

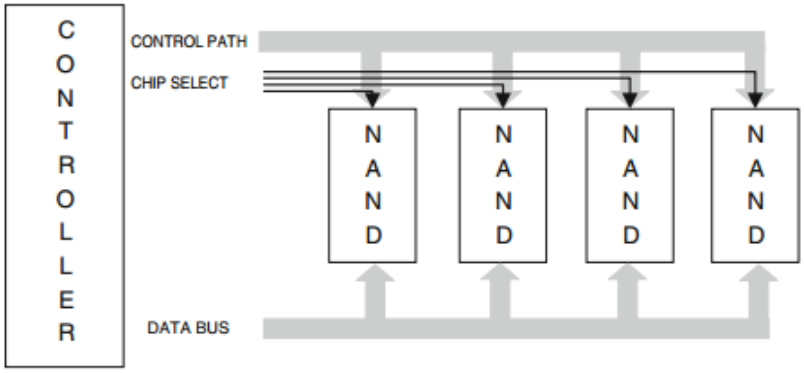


Fig. 5.12 Single-channel architecture

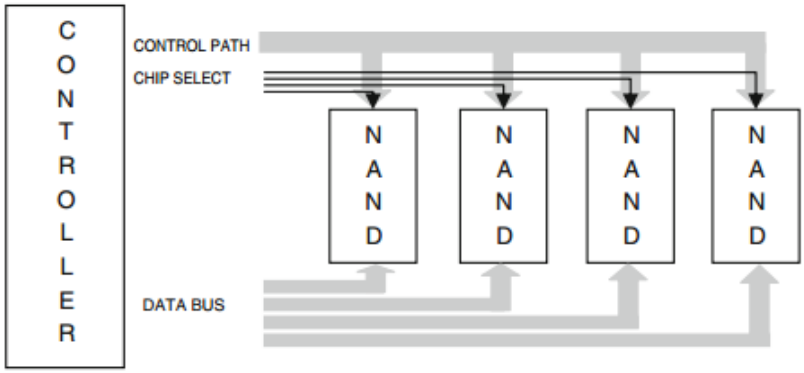


Fig. 5.13 Multichannel architecture

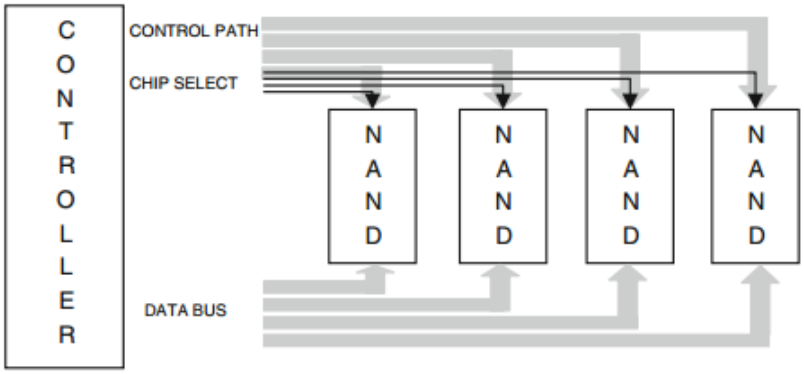
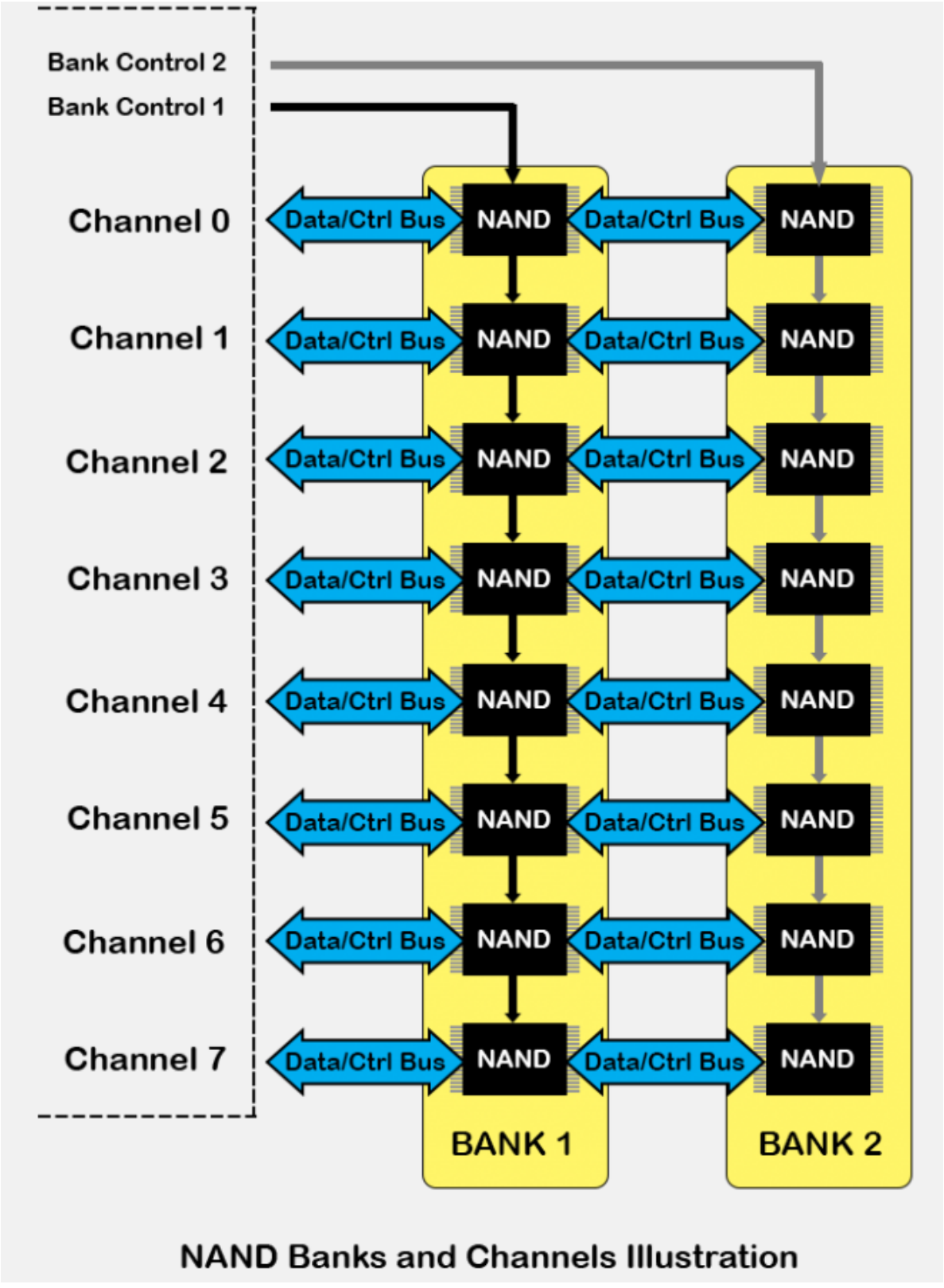
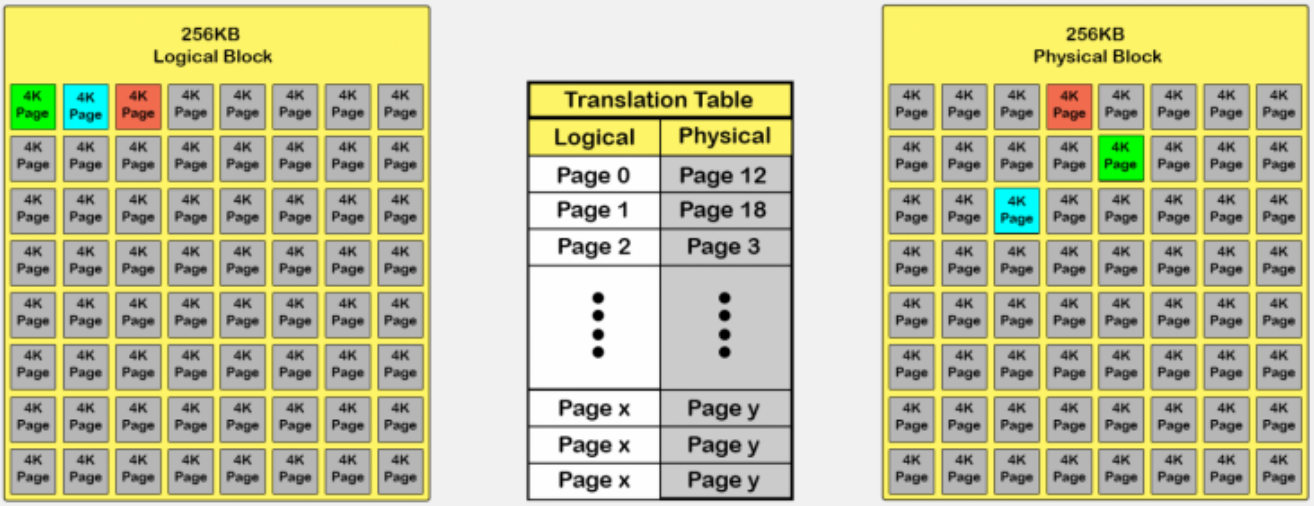


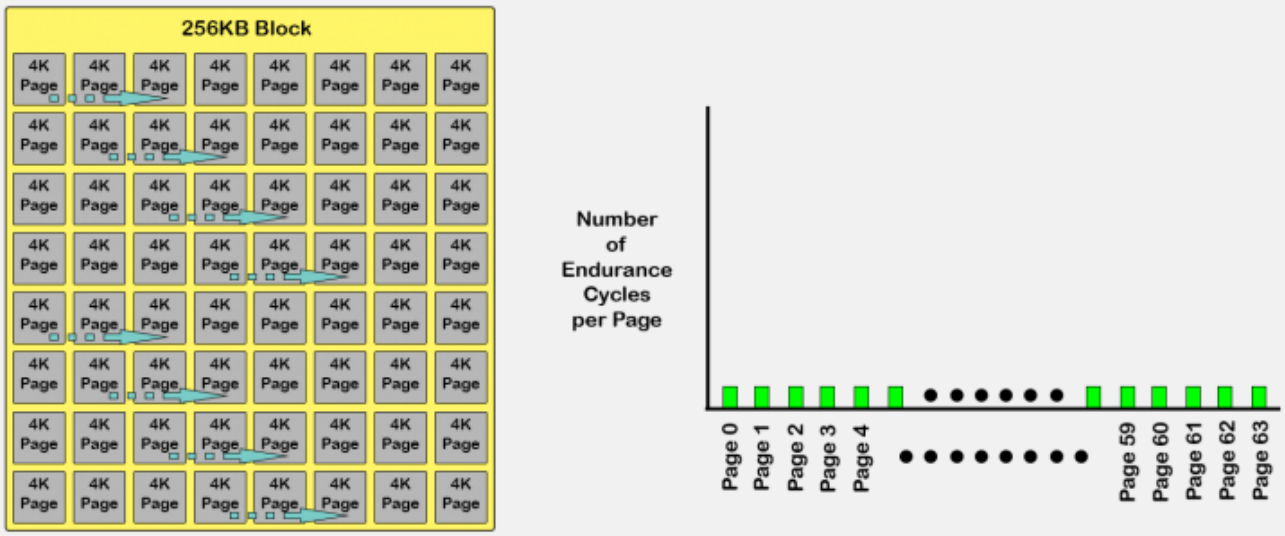
Fig. 5.14 Fully connected architecture



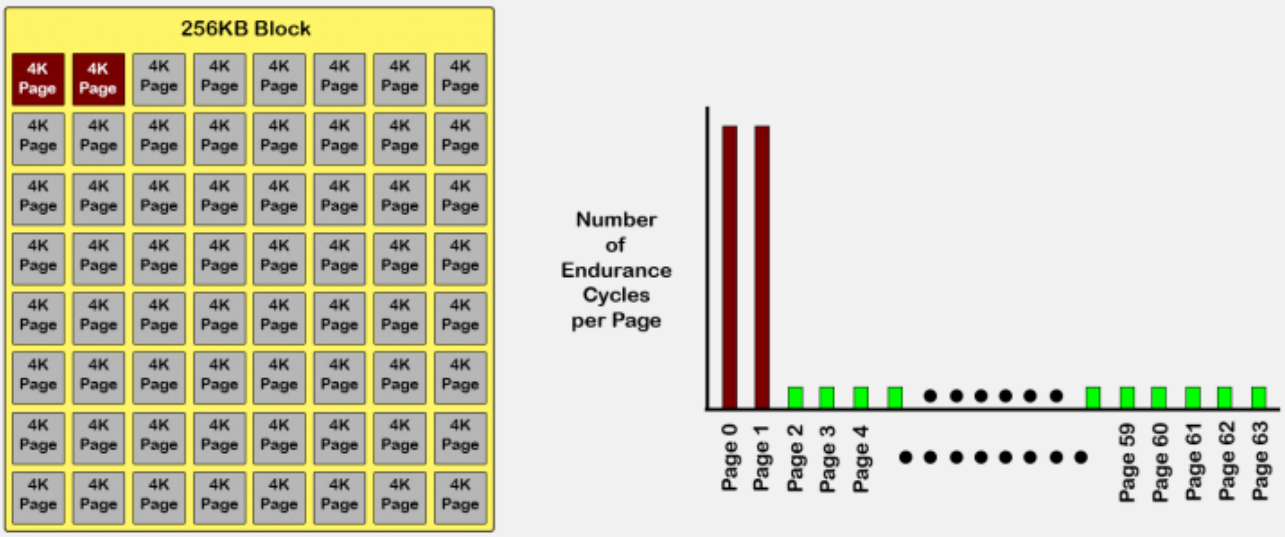
NAND Banks and Channels Illustration



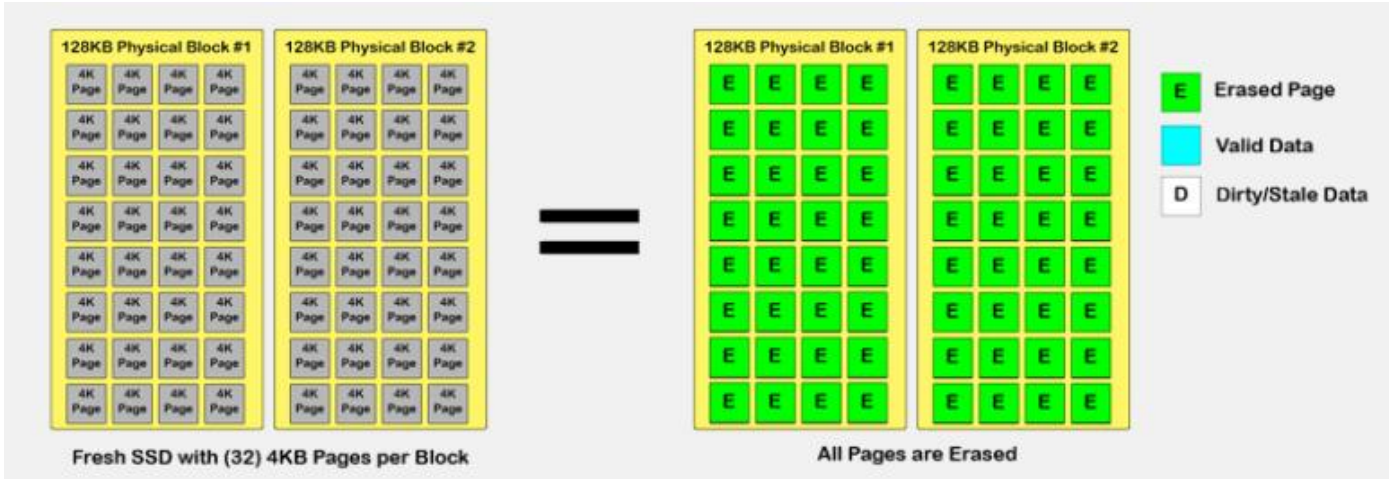
Logical to Physical Translation

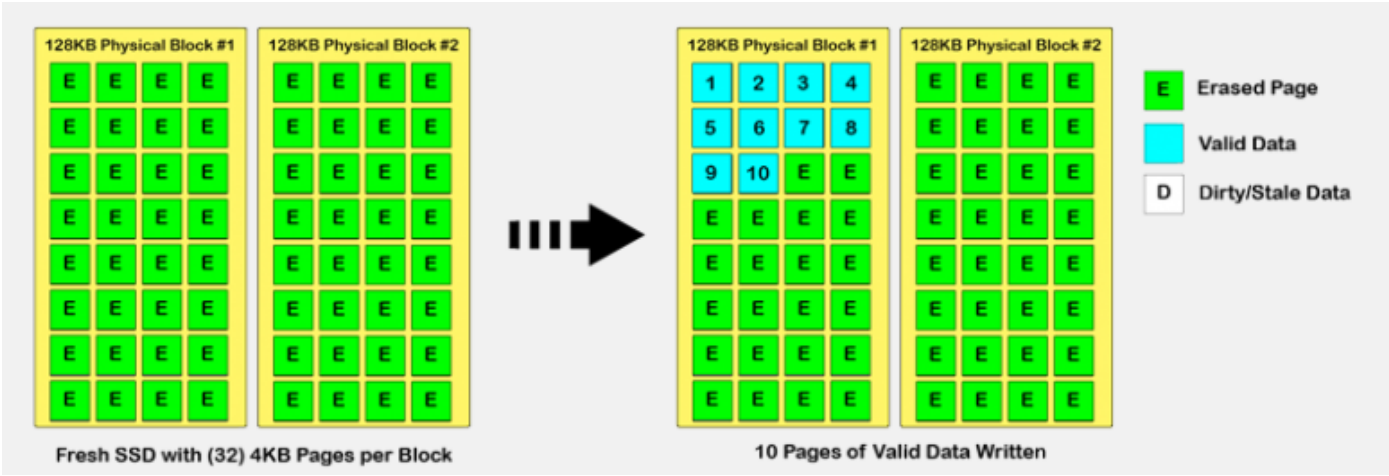


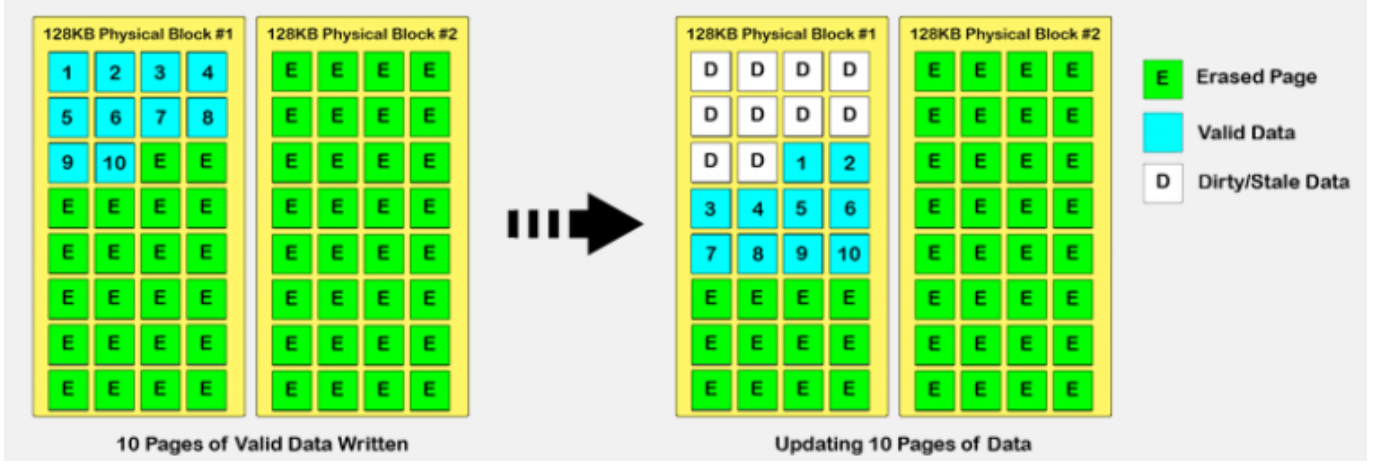
Sequentially Written Flash Block

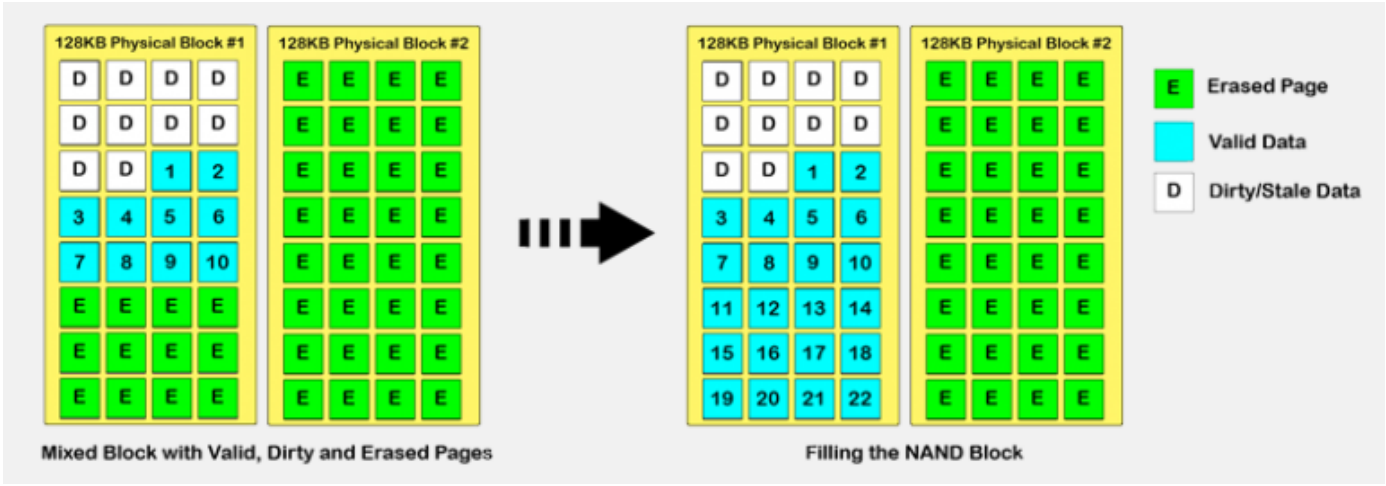


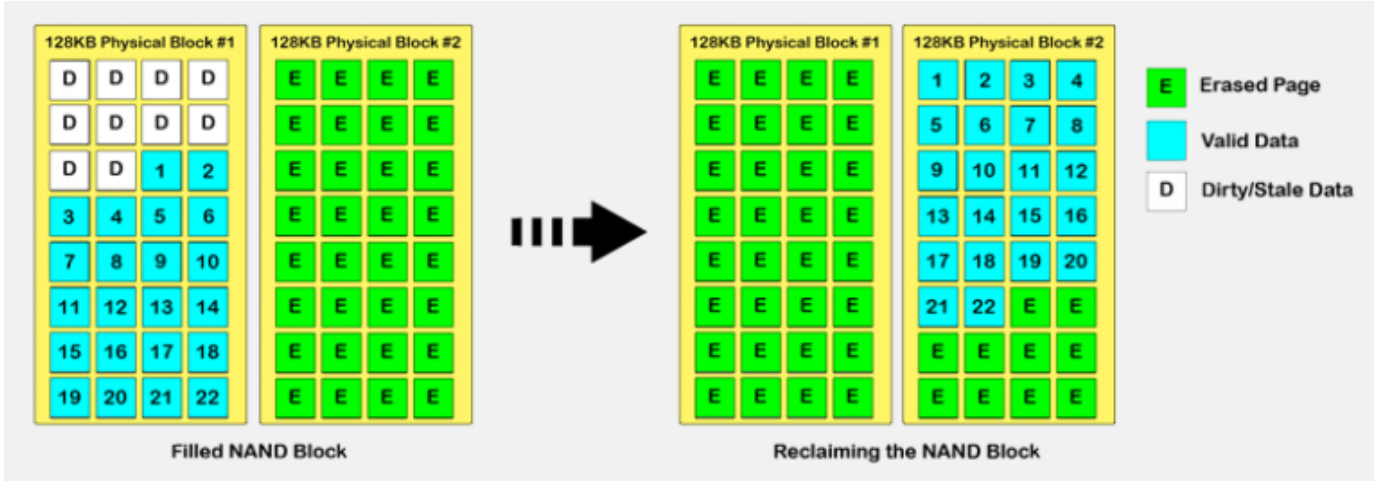
Non-Sequentially Written Flash Block


128KB Physical Block #1
128KB Physical Block #2
4K Page
Fresh SSD with (32) 4KB Pages per Block
All Pages are Erased
E Erased Page
Valid Data
D Dirty/Stale Data


128KB Physical Block #1
128KB Physical Block #2
Fresh SSD with (32) 4KB Pages per Block
10 Pages of Valid Data Written
E Erased Page
Valid Data
D Dirty/Stale Data

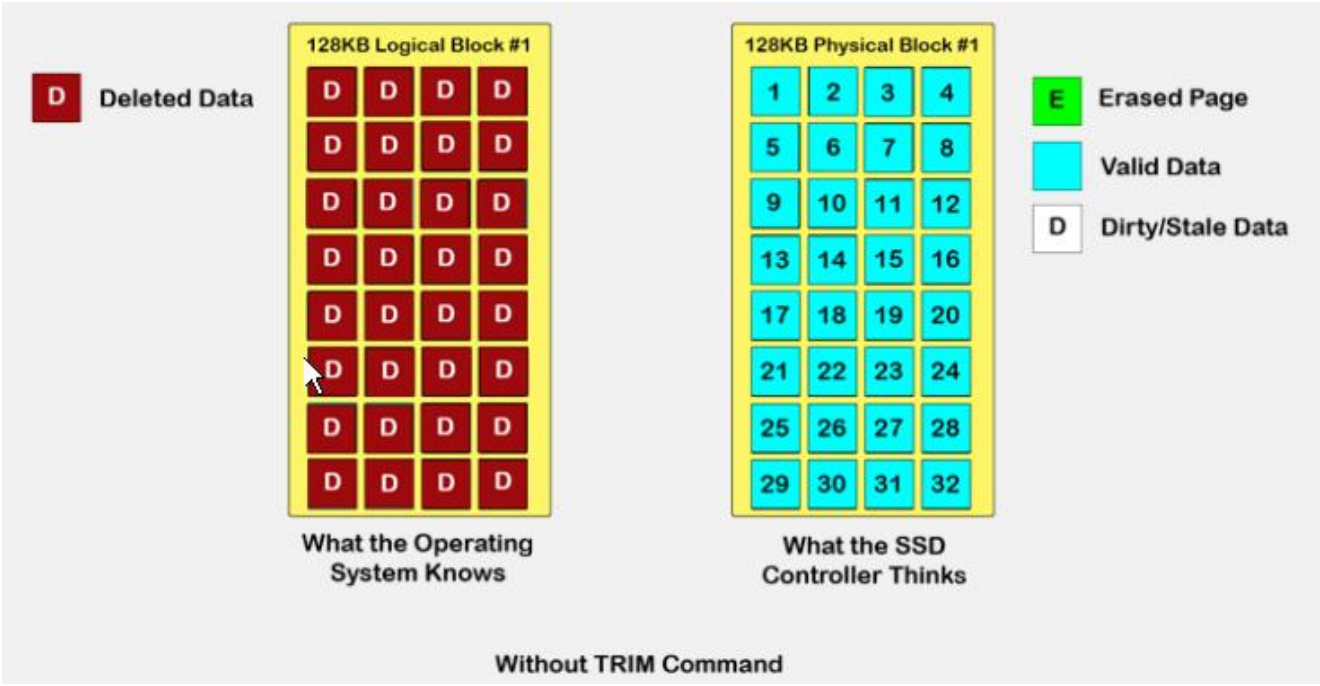

128KB Physical Block #1
128KB Physical Block #2
10 Pages of Valid Data Written
Updating 10 Pages of Data
E Erased Page
Valid Data
D Dirty/Stale Data

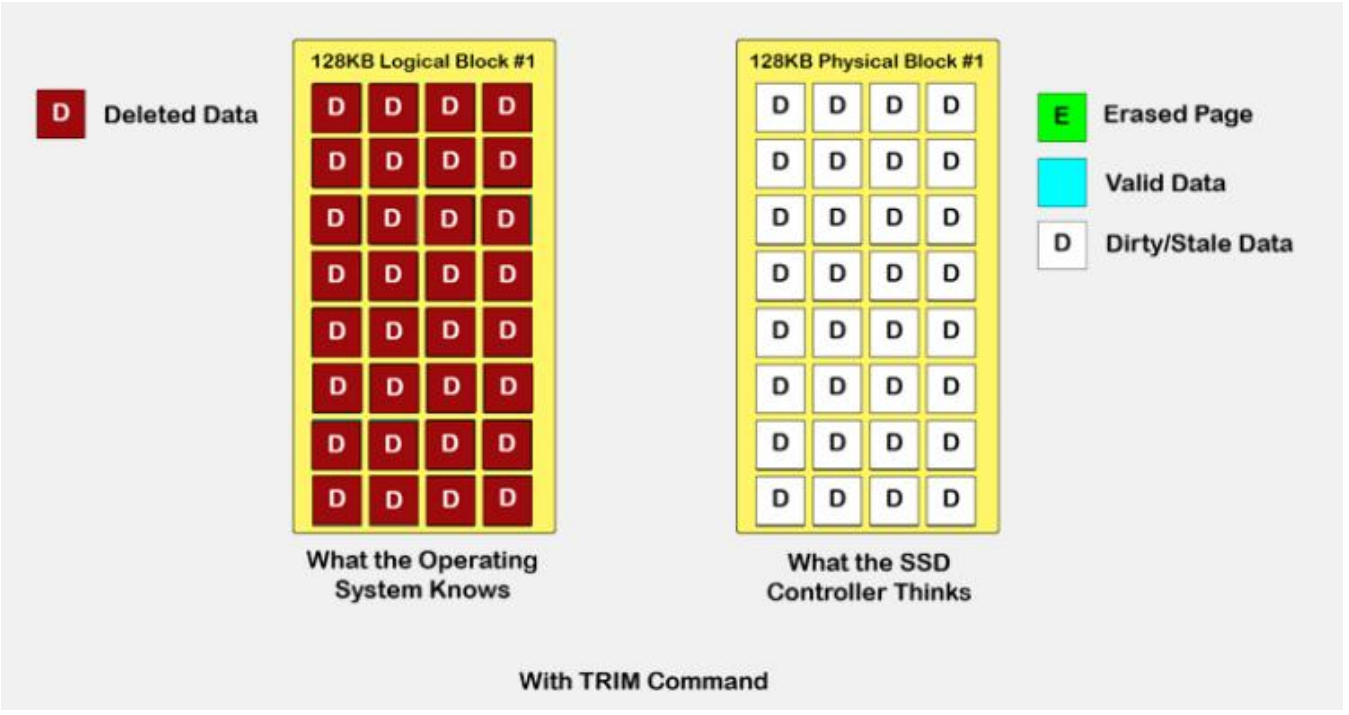




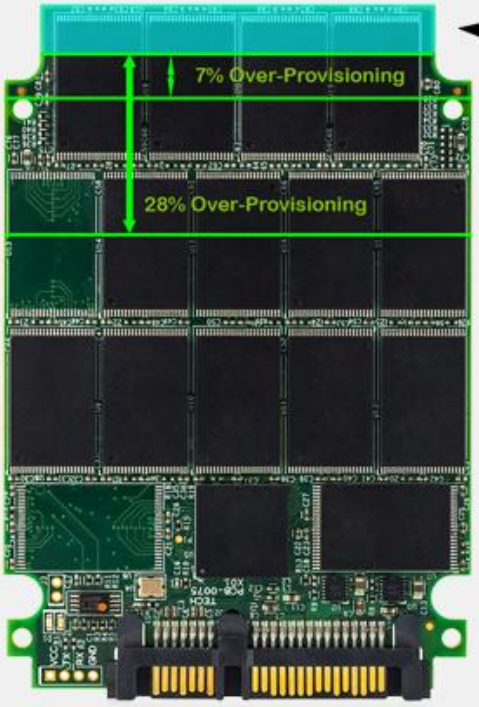
Write amplification

Write amplification (WA) is an SSD phenomenon that occurs when the actual amount of written physical data is more than the amount of logical data that is written by the host computer. There are two main factors that cause this difference: First, every storage device that uses NAND Flash memory is made of elements that must be erased before they can be rewritten. Second, while NAND Flash devices can be written a single page at a time (a page is typically 4KiB–16KiB), NAND Flash devices can only be erased one block at a time; and a block (also known as a "NAND block" or an "erase block") can contain hundreds of pages. This requires the internal movement of saved user data in background operations to free up adjacent pages of data that are eligible to be erased, and therefore available for new data written by the host computer. Consequently, the total number of actual writes to an SSD is typically more than the number of writes intended to be written by the host computer.


D Deleted Data
128KB Logical Block #1
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
What the Operating System Knows
128KB Physical Block #1
1 2 3 4
5 6 7 8
9 10 11 12
13 14 15 16
17 18 19 20
21 22 23 24
25 26 27 28
29 30 31 32
What the SSD Controller Thinks
E Erased Page
Valid Data
D Dirty/Stale Data
Without TRIM Command


D Deleted Data
128KB Logical Block #1
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
What the Operating System Knows
128KB Physical Block #1
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
D D D D
What the SSD Controller Thinks
E Erased Page
Valid Data
D Dirty/Stale Data
With TRIM Command

Over-Provisioning at 0%, 7% and 28%



7% Difference in Binary to Decimal SSD Capacity used internally by SSD Controller

0% Over-Provisioning	7% Over-Provisioning	28% Over-Provisioning
128GB	120GB	100GB
512GB	480GB	400GB

Marketed Capacity	IDEMA Decimal Capacity (Bytes)	Binary Capacity (Bytes)	Difference
128GB	128,035,676,160	137,438,953,472	7.34%
512GB	512,110,190,592	549.755,813,888	7.35%