A Boost-Full-Bridge-Type Single-Active-Bridge Isolated AC-DC Converter

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***Abstract*—A boost-full-bridge (BFB) concept is proposed in this paper. It improves the control dynamics of boost-half-bridge (BHB) converters, and makes the converters feasible for dc-dc applications as well as ac-dc. A BFB-type single-active-bridge (SAB) ac-dc converter is proposed and investigated in this paper, as an example case from the BFB family of topologies for the validation of the BFB concept. The proposed converter topology has high power density and galvanic isolation, thanks to its high-frequency (HF) transformer link. It also features dc-side short-circuit fault-blocking capability. This paper analyzes the operation principles of the converter and presents suitable modulation and controller schemes. Experiment results are also provided to demonstrate the start-up dynamics, steady-state waveforms, and the dc-fault-blocking capability of the converter.**

Keywords—AC-DC Converter, Boost Full Bridge, Boost Half Bridge, Dual Active Bridge, Fault Blocking, Single Active Bridge.

I. INTRODUCTION

Isolated ac-dc converters play an important role in a wide range of applications, such as: dc distribution, chargers for electric vehicles, adapters for consumer electronics, etc [1]-[8]. A conventional isolated ac-dc converter normally consists of two stages: (a) an ac-dc stage; and (b) an isolated dc-dc stage. The dc-dc stage usually includes a medium-frequency (MF) or high-frequency (HF) transformer, for voltage step-up/down and the galvanic isolation. Forward and flyback converters are ubiquitous for isolated dc-dc applications with power ratings below hundreds of watts, but are usually unfit for multi-hundred-watt-scale or kilo-watt-scale applications [9], [10]. Alternatively, dual-active-bridge (DAB) converters (see Fig. 1 [3], [11], [12]) and single-active-bridge (SAB) converters (see Fig. 2 [11], [13]) are two promising candidates for relatively high power applications [3]. Their advantages include: (a) high power delivery ability; (b) galvanic isolation and high power density [3], [11]; (c) soft-switching performance [3], [11]; (d) fault blocking capability [12]; (e) multi-port expansion capability [14]-[16]. Compared with the DAB converter enabling bidirectional power flow, the SAB converter uses less active switches and requires a simpler auxiliary control system, and therefore is more suitable for applications that only need unidirectional power flow.

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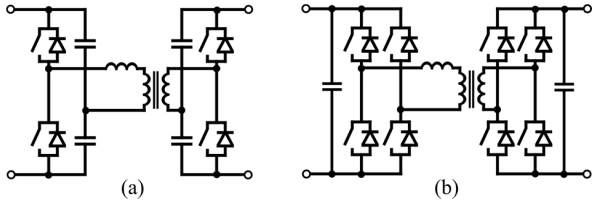

Fig. 1. Dual-active-bridge (DAB) isolated dc-dc converters [3], [11], [12]. (a) Half-bridge topology. (b) Full-bridge topology.

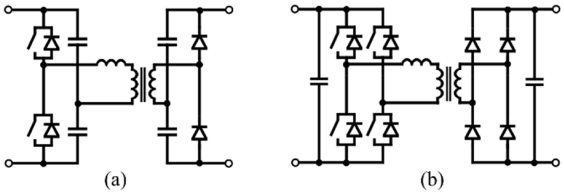

Fig. 2. Single-active-bridge (SAB) isolated dc-dc converters [11], [13]. (a) Half-bridge topology. (b) Full-bridge topology.

The two-stage ac-dc conversion structure reduces the system efficiency, increases system costs and meanwhile leads to a complex gate-driving circuit. To avoid those problems, one-stage isolated ac-dc topologies have been proposed (see Fig. 3 [7], [8]). For the topology in Fig. 3(a) [7], four-quadrant switch cells are used, which results in difficult switching commutation and increased conduction losses. As for Fig. 3(b) [8], a line-frequency-switched synchronous rectifier is required, which also increases system costs, losses, and control burden.

In this paper, a boost-full-bridge (BFB) concept is proposed which improves the control dynamics of the boost-half-bridge (BHB) converter [15]-[19]. Furthermore, based on the widely-used single-active-bridge (SAB) converter [11], [13], a new type of isolated ac-dc converter (called BFB-SAB converter) is proposed and investigated in this paper, as an example case from the BFB converter family. The proposed converter can be easily controlled, and meanwhile inherits the benefits of conventional SAB dc-dc converters. Additionally, unlike the conventional ac-dc VSC (i.e., H4 active rectifier), the proposed ac-dc converter is able to block the dc-side short-circuit fault. However, because of the secondary-side diode bridge, the proposed converter is only suitable for unidirectional power flow applications, such as dc distribution, electric vehicle (EV) chargers, etc.

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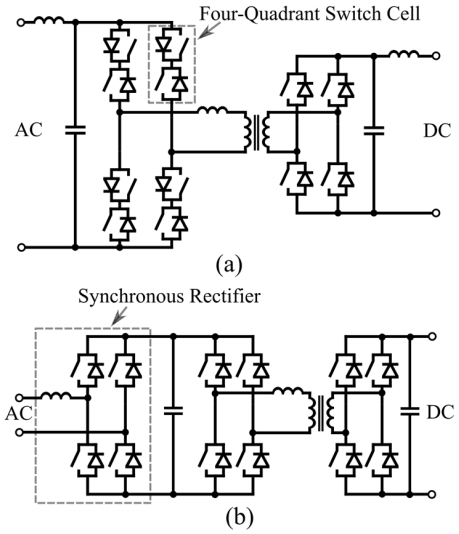

Fig. 3. Typical one-stage HF-transformer-based ac-dc converter topologies. (a) Topology proposed in [7]. (b) Topology proposed in [8].

This paper is organized as follows: Section II introduces the BFB concept and proposes the BFB-SAB converter topology. The proposed dc-dc topology is analysed first in Section III. In Section IV, operation principles of the proposed ac-dc topology are analysed. Experiment results are illustrated and discussed in Section V. Section VI presents the conclusions of the paper.

II. Topology Derivation

In [17], [18], a BHB dc-dc converter is proposed, as shown in Fig. 4(a). A BHB combines a boost converter and a half bridge. It gives a current-fed input port with a terminal inductor L_p, and makes the input current continuous and controllable. Furthermore, by adjusting the duty cycle d_p, the BHB converter is able to provide a variable input voltage v_{tp} [15]. However, this topology is actually unfit for applications requiring a dynamically variable input voltage v_{tp} (e.g., ac-dc conversion), because:

a) Both the high-frequency (HF) transformer and the terminal inductor L_p are connected to the same leg of the BHB. However, only one control degree of freedom (i.e., the duty cycle d_p) is available. When d_p is adjusted, not only the input current is controlled, but also the HF transformer current i_p is impacted, driven by the asymmetry and the volt-second imbalance of v_p in each switching period. This leads to a challenging design of a closed-loop controller [19].

b) For ac-dc conversion, both the input current and the duty cycle d_p should be line-frequency sinusoidal at the steady state. As a result, v_p and i_p also contain line-frequency components, which leads to the core saturation or oversize of the HF transformer.

c) Even though the input voltage v_{tp} is adjustable, its polarity has to be positive, or else the control of the BHB will be lost due to its anti-parallel diode.

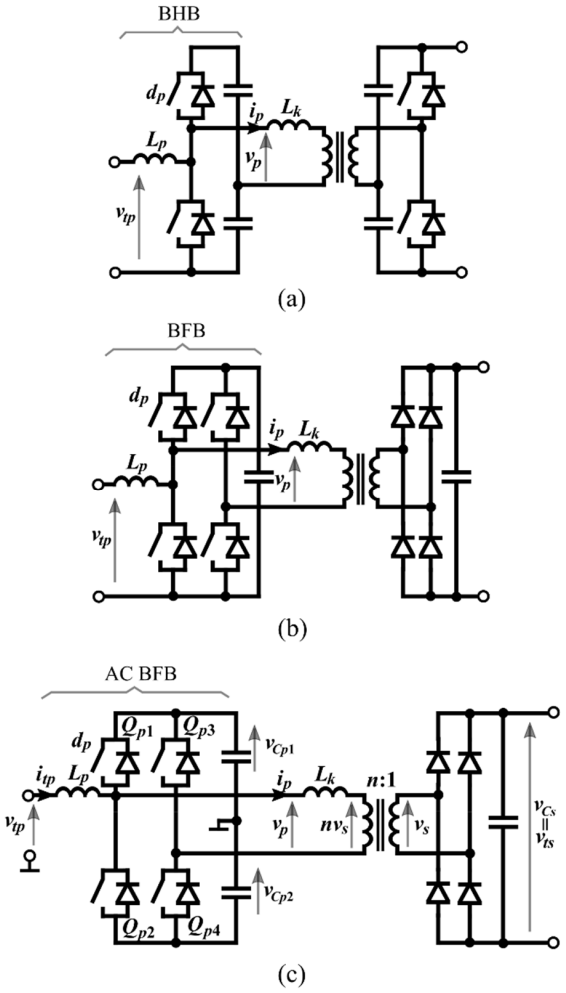

Fig. 4. Topology derivation. (a) BHB-DAB dc-dc converter proposed in [17], [18]. (b) Proposed BFB-SAB dc-dc converter. (c) Proposed BFB-SAB ac-dc converter. (Notes: d_p is the duty cycle for the high-side switch.)

For solving these problems, the BHB is extended to boost-full-bridge (BFB) in this paper, as shown in Fig. 4(b). Additionally, a diode bridge can be used at the secondary side to reduce the system costs and control complexity. Moreover, by moving the negative input terminal to the neutral of the dc bus (see Fig. 4(c)), the proposed converter is able to handle ac input voltage v_{tp}. Similarly to a BHB, a BFB combines a boost converter and a full H bridge, and gives one more control freedom than the BHB due to its extra leg (i.e. Q_{p3} and Q_{p4}). By controlling Q_{p3} and Q_{p4}, v_p can be always symmetrical and volt-second-balanced in each switching period, with arbitrary value of the duty cycle d_p, as discussed in Section III.A later. Therefore, the saturation of the HF transformer can be avoided and good converter dynamics can be ensured. Additionally, the BFB-SAB converter is able to deliver more power, thanks to the full bridge structure and the higher terminal voltage of the HF transformer [3]. Higher voltage means lower current, and potentially less power losses, which also make the full-bridge structure attractive. The detailed operation principles of the proposed converters are analysed next.

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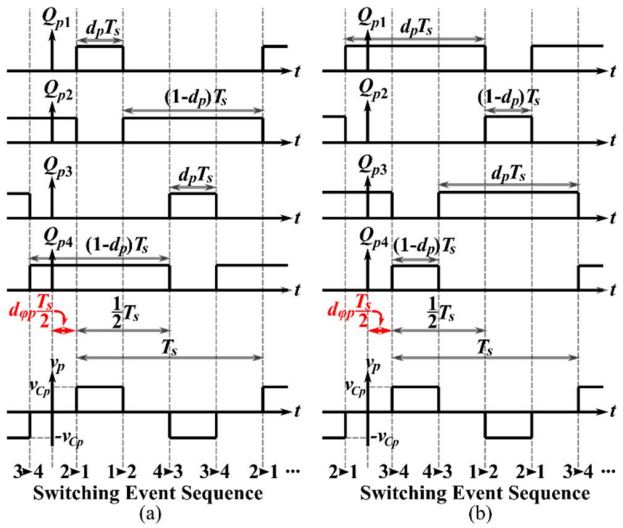

Fig. 5. Gate signals, switching event sequence, and square waveform of v_p. (a) For $d_p < 0.5$. (b) For $d_p > 0.5$.

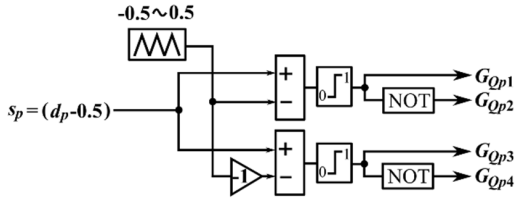

Fig. 6. Proposed implementation of the required gate signals.

It is worth noting that the BFB concept introduced in this paper has certain similarities with the interleaved-boost-full-bridge (IBFB) concept proposed in [20], [21]. But IBFB was investigated for dc-dc applications only, and not so intuitional to be used for ac-dc.

III. BFB-SAB DC-DC Converter

For the proposed ac-dc topology in Fig. 4(c), when the switching frequency is much higher than the line frequency (i.e. $f_s \gg f_{ac} = 50\text{Hz or } 60\text{Hz}$), the duty cycle d_p can be approximately regarded as a constant in one switching period. In other words, the ac-dc topology in one switching period is corresponding to the dc-dc topology with certain value of d_p. This will be discussed in detail in Section IV and will be validated by experiment results in Section V later. Hence, before analysing the ac-dc topology in Fig. 4(c), the dc-dc topology in Fig. 4(b) is analysed first in this section.

A. PWM of the Primary-Side BFB Cell

A pulse-width-modulation (PWM) strategy for the BFB is proposed, as shown in Fig. 5, where $T_s = 1/f_s$ is the switching period. Notably, Q_{p1} and Q_{p3} have a same duty cycle (d_p); Q_{p2} and Q_{p4} also have a same duty cycle $(1 - d_p)$. The gate signals of Q_{p3} and Q_{p4} have a half-switching-period delay (i.e. $T_s/2$) compared with those of Q_{p1} and Q_{p2}, respectively. In this case, the square-wave v_p is always symmetrical and volt-second-balanced in each switching period. A simple way to implement these required gate signals is shown in Fig. 6, where zero-biased duty cycle $s_p = d_p - 0.5$ is used to facilitate the controller design later.

Moreover, it is notable that two different switching patterns can give a same waveform of v_p, as shown in Figs. 5(a) and (b), which are corresponding to the cases of $d_p > 0.5$ and $d_p < 0.5$, respectively. The half of the zero-voltage time slot of v_p is defined as $d_{\phi p}T_s/2$. The relationship between $d_{\varphi p}$ and d_p is

$$d_{\varphi p} = \frac{1}{2} \cdot \begin{cases} 1 - 2d_p, & \text{if } 0 \le d_p \le 0.5 \\ 2d_p - 1, & \text{if } 0.5 < d_p \le 1 \end{cases} = \frac{1}{2}\left|1 - 2d_p\right| \tag{1}$$

where $0 \le d_{\varphi p} \le 0.5$ if $0 \le d_p \le 1$.

B. Steady-State Analysis

The steady-state waveforms of the HF transformer are shown in Fig. 7. The converter operation can be classified into two modes [13]:

Mode 1: border mode (BM), if $d_\phi > d_{\phi p}$.

Mode 2: discontinuous current mode (DCM), if $d_\phi < d_{\phi p}$.

The critical condition between two modes is $d_\phi = d_{\phi p}$.

According to the waveforms,

$$nv_{Cs} = v_{Cp} \times \begin{cases} (1 - 2d_\varphi) & \text{if BM} \\ \dfrac{1 - 2d_{\varphi p}}{1 + 2d_\varphi - 2d_{\varphi p}} & \text{if DCM} \end{cases} \tag{2}$$

which gives the relationship between the primary- and secondary-side voltages. Obviously, $nv_{Cs} \le v_{Cp}$ if $d_\varphi \ge 0$. Additionally, (2) can be rewritten as

$$d_\varphi = \begin{cases} \dfrac{1}{2}\left(1 - \dfrac{1}{k}\right) & \text{if BM} \\ \dfrac{1}{2}\left(k\left(1 - 2d_{\varphi p}\right) + 2d_{\varphi p} - 1\right) & \text{if DCM} \end{cases} \tag{3}$$

with

$$k = \frac{v_{Cp}}{nv_{Cs}} \tag{4}$$

This equation gives the relationship between d_φ and $d_{\varphi p}$ with given values of v_{Cp} and v_{Cs}. Based on this equation, the critical condition between BM and DCM can be calculated as

$$d_{\varphi p} = d_\varphi = \frac{1}{2}\left(1 - \frac{1}{k}\right) \tag{5}$$

In addition, according to the waveforms, the active power can be calculated as

$$P = \frac{nv_{Cp}v_{Cs}}{4f_sL_k} \times \begin{cases} \left(2d_{\varphi p}^2 - \dfrac{1}{2} + \dfrac{1}{2k^2}\right) & \text{if BM} \\ \left(2d_{\varphi p} - 1\right)^2(k - 1) & \text{if DCM} \end{cases} \tag{6}$$

and the peak value of the current i_p can be calculated as

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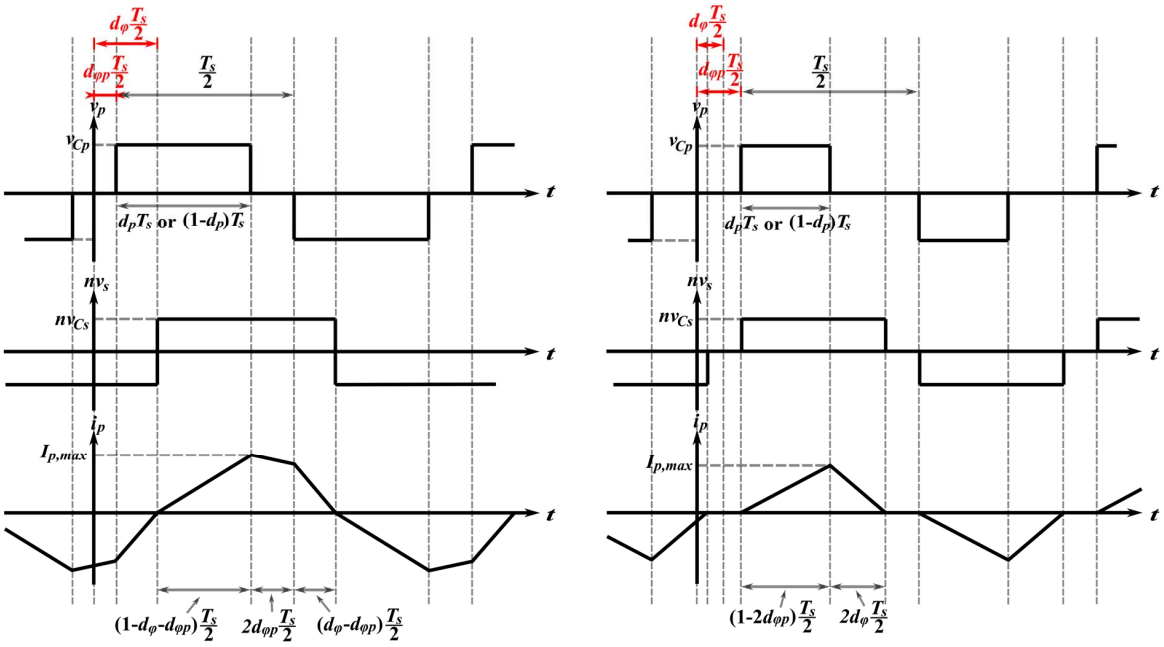

Fig. 7. Voltage and current waveforms of the BFB-SAB dc-dc converter. (a) Mode 1: border mode (BM) if $d_\phi > d_{\phi p}$. (b) Mode 2: discontinuous current mode (DCM) if $d_\phi < d_{\phi p}$.

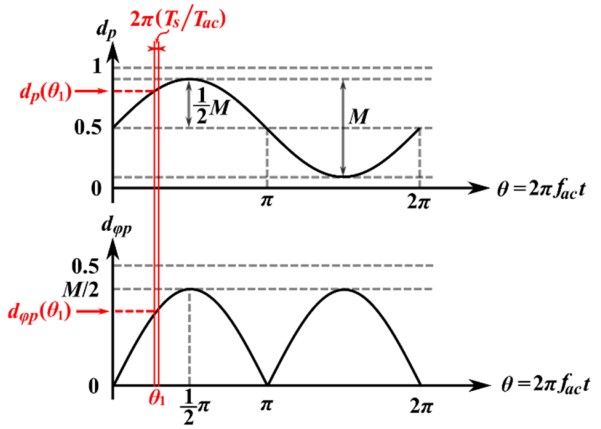

Fig. 8. Steady-state waveforms of d_p and $d_{\phi p}$ in one line-frequency period. (Notes: $T_{ac} = 1/f_{ac}$ is one grid-frequency period; $T_s = 1/f_s$ is one switching period; and M is the modulation index.)

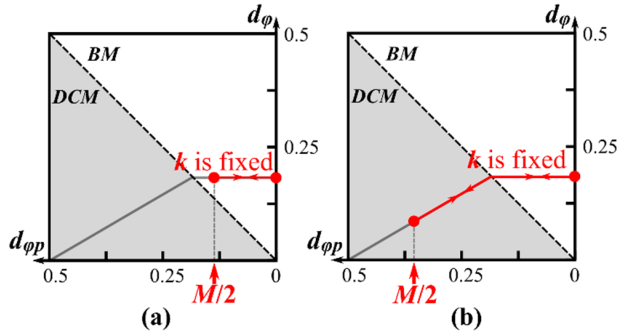

Fig. 9. d_φ versus $d_{\varphi p}$ with a given value of k and M. (a) $M < 1 - 1/k$. (b) $M > 1 - 1/k$. (Notes: $k = \frac{v_{Cp}}{nv_{Cs}}$; M is the modulation index.)

$$I_{p,max} = \frac{nv_{Cs}}{2f_sL_k} \times \begin{cases} (k-1)\left(\frac{1}{2k} - 2d_{\varphi p} + \frac{1}{2}\right) & \text{if BM} \\ (k-1)\left(1 - 2d_{\varphi p}\right) & \text{if DCM} \end{cases} \quad (7)$$

In conclusion, (1)-(7) give the steady-state equations of the proposed BFB-SAB dc-dc converter in Fig. 4(b). The BFB-SAB ac-dc converter in Fig. 4(c) will be analysed next.

IV. BFB-SAB AC-DC Converter

A. Steady-State Analysis

For the dc-dc topology in Fig. 4(b), both d_p and $d_{\varphi p}$ are constant at steady state. By contrast, for the ac-dc topology in Fig. 4(c), d_p is sinusoidal at steady state due to the ac voltage input. Ideally,

$$d_p = \frac{1}{2}(Msin(\theta) + 1) \quad (8)$$

where M is the modulation index; and $\theta = 2\pi f_{ac}t$ is the phase angle. According to (1), (8) can be re-written as

$$d_{\varphi p} = \frac{1}{2}|1 - 2d_p| = \frac{1}{2}M|sin(\theta)| \quad (9)$$

Based on these equations, the waveforms of d_p and $d_{\varphi p}$ are plotted in Fig. 8. When the switching frequency is much larger than the line-frequency, i.e. $f_s \gg f_{ac} = 50\text{Hz}$ or 60Hz, d_p and $d_{\varphi p}$ can be regarded as constant in each switching period. In other words, the operation of the ac-dc topology in one

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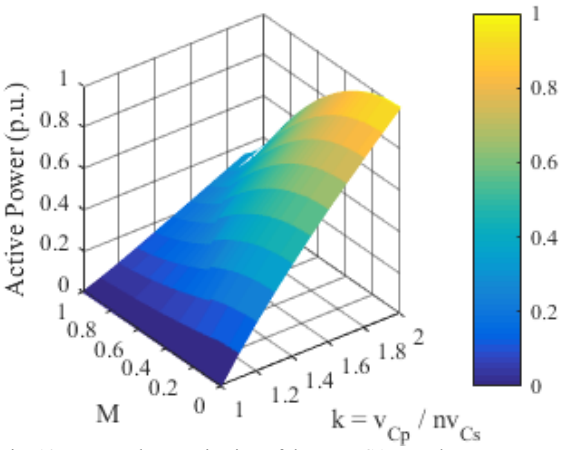

Fig. 10. Power characterization of the BFB-SAB ac-dc converter.

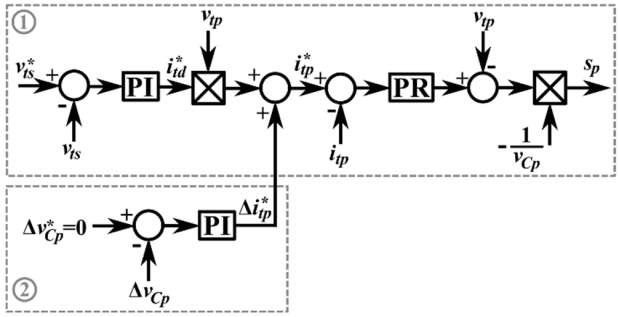

Fig. 11. Control structure for the BFB-SAB ac-dc converter.

switching period is corresponding to the operation of the dc-dc topology with certain values of d_p and $d_{\varphi p}$. Therefore, the modulation methods in Fig. 5, the waveforms in Fig. 7, and the equations (1)-(7) are still fit for the ac-dc topology, which will also be validated by the experiment results later in Section V.A.

For the ac-dc topology at the steady state, the primary- and secondary-side voltages remain unchanged, i.e., $k = \frac{v_{Cp}}{nv_{Cs}}$ is constant. According to (2)-(4), with a fixed k, the operation of the converter periodically tracks the red trace in Fig. 9 with a variable $d_{\phi p}$, i.e., a variable duty cycle d_p. According to (5) and (9), when modulation index $M < 1 - 1/k$, the converter operates in BM only, i.e., Fig. 9(a); when $M > 1 - 1/k$, the converter operates in BM and DCM alternatively, i.e., Fig. 9(b).

B. Power Characterization

The active power of the ac-dc topology can be obtained by integrating the active power of the dc-dc topology with variable $d_{\varphi p}$ by using (6). Two different cases are considered:

Case 1: $M < 1 - 1/k$

$$P = \frac{\int_0^{\frac{\pi}{2}} P_{BM}\, d\,\theta}{\pi/2} \tag{10}$$

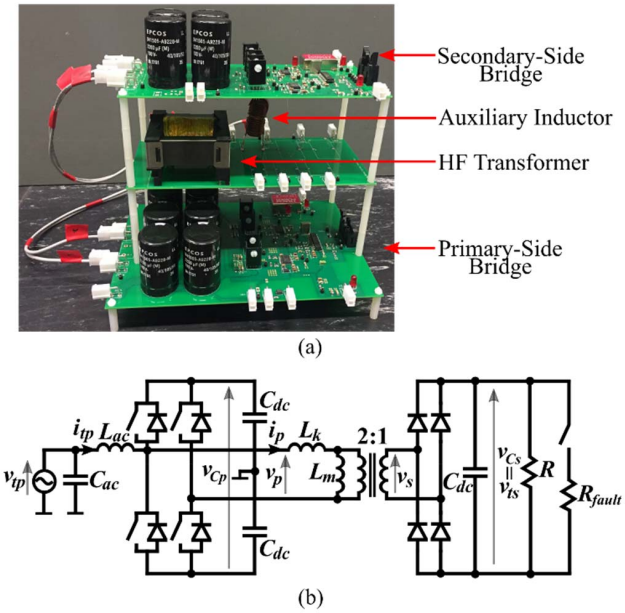

Fig. 12. Prototype of the proposed converter. (a) Photo of the converter. (b) Schematic of the experiment platform.

Case 2: $M > 1 - 1/k$

$$P = \frac{\int_0^{\theta 1} P_{BM}\, d\,\theta + \int_{\theta 1}^{\frac{\pi}{2}} P_{DCM}\, d\,\theta}{\pi/2} \tag{11}$$

$$\theta 1 = \arcsin\left(\frac{1 - 1/k}{M}\right)$$

where P_{BM} and P_{DCM} are corresponding to the BM power and DCM power in (6), respectively.

According to (10) and (11), the power characterization for the ac-dc topology can be plotted in Fig. 10. (For practical applications, k should be limited below a certain value so that the primary-side voltage v_p meets the insulation requirement. In this paper, $k_{max} = 2$ is selected.)

C. Closed-Loop Control

A control structure is proposed for generating the required duty cycle $s_p = d_p - 0.5$ of the BFB, as shown in Fig. 11. The control structure is divided into two parts:

a) The first part consists of a double-loop control path: the outer-loop PI controller is for regulating the output voltage v_{ts}; the inner-loop PR controller is for controlling the ac-side current i_{tp}, improving the system dynamics, and setting the ac-side power factor. This part is almost same as the control of a normal VSC [22]. Notably, to achieve the unity power factor, the product of d-axis current i_{td}^* and measured ac voltage v_{tp} is used as the ac current reference. If non-zero reactive power is required, a single-phase phase lock loop (PLL) can be added to set the phase difference between the ac voltage and the ac current [23].

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TABLE I
PARAMETERS OF THE EXPERIMENT PLATFORM

AC Voltage	$v_{tp,RMS} = 12\text{V}$, $f_{ac} = 50\text{Hz}$
HF Transformer	Tap Ratio: 2: 1 Magnetic Inductance: $L_m = 20\text{mH}$, $R_m = 4.85\Omega$ Auxiliary Inductance: $L_k = 275\mu\text{H}$, $R_k = 0.67\Omega$
AC Filter	$L_{ac} = 6\text{mH}$, $C_{ac} = 2.2\mu\text{F}$
DC Voltage	$v_{ts} = 15\text{V}$
DC Filter	$C_{dc} = 8800\mu\text{F}$
DC Load	$R = 11\Omega$
Fault Resistance	$R_{fault} = 0.1\Omega$
Switching Frequency	$f_s = 5\text{kHz}$

b) The second part is for balancing the voltages of upper and lower capacitors of the primary side, which is almost same as that of a conventional half-bridge VSC [24].

With a given s_p, by applying the PWM method in Figs. 5 and 6, the gate driving signals for all four switches can be obtained.

V. EXPERIMENTAL TESTS

A down-scaled prototype for the proposed BFB-SAB ac-dc converter is built, as shown in Fig. 12(a). The schematic and parameters of the experiment platform are displayed in Fig. 12(b) and Table I, respectively. The experiment results are discussed next.

A. Steady-State Operation

The steady-state waveforms of the proposed ac-dc converter are shown in Figs. 13 and 14(b). The ac-side voltage and current are illustrated in the top sub-figure in Fig. 14(b). Notably, a unity power factor is ensured. Primary- and secondary-side dc capacitor voltages are shown in the second sub-figure. The second-order line-frequency harmonics (100Hz) are observed because of the single-phase structure [25]. The bottom sub-figure shows the waveforms of the HF transformer. Notably, the converter operates in DCM and BM alternatively, caused by the variable duty cycle d_p. Close-up plots of two operation modes of the proposed ac-dc converter are displayed in Fig. 13, which coincide with the theoretical waveforms of the dc-dc converter in Fig. 7. This also validates that the operation of the ac-dc topology in each switching period is actually equivalent to the dc-dc topology with a certain value of duty cycle d_p. Notably, waveforms of v_p and v_s are always volt-second-balanced in each switching period, and the current i_p has switching-frequency harmonics only. Small oscillations can be observed during the discontinuous current period in DCM, because of the resonance between the parasitic capacitors of power switches and the HF transformer, as highlighted in Fig. 13(b).

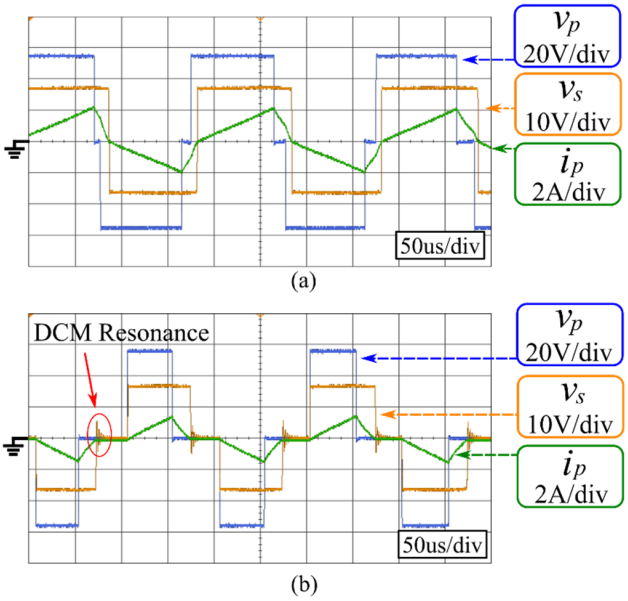

Fig. 13. Close-up plots of the steady-state waveforms of the HF transformer in two modes. (a) Border mode (BM). (b) Discontinuous current mode (DCM).

B. Converter Start Up

The converter start-up performance is shown in Fig. 14(a). In the top sub-figure, the converter actively increases its ac-side current gradually. Then, as displayed in the second sub-figure, the primary-side dc voltage is boosted from its pre-charge value to its rated value smoothly, and the secondary-side dc voltage is boosted from zero to its rated value as well. As illustrated in the bottom sub-figure, the HF transformer current also increases to delivery more power and boost the output voltage. The terminal voltages of the HF transformer increase as well, following the increase of primary- and secondary-side dc voltages.

C. DC-Side Short-Circuit Fault Blocking

The converter is able to block the ac-side contribution to dc-side short-circuit faults by switching off all primary-side switches. Test results are shown in Fig. 14(c). As shown in the second sub-figure, when a dc fault happens, v_{Cs} drops quickly due to the short circuit. When it drops to 66% of its rated value, the fault is detected by the converter and all power switches are turned off. After that, as shown in the top sub-figure, the ac inductor discharges smoothly through the primary-side anti-parallel diodes to the dc capacitors, and its current drops to zero gradually. In the bottom sub-figure, the voltages and current of the HF transformer also drop to zero quickly. Some small oscillations appear after shutting down the converter, which is caused by the resonance between parasitic capacitors of power switches and the HF transformer.

According to the results, under a dc-side short-circuit fault event, the converter is protected without using any external protection devices (such as circuit breakers), and no fault current is fed from the primary side to the secondary side.

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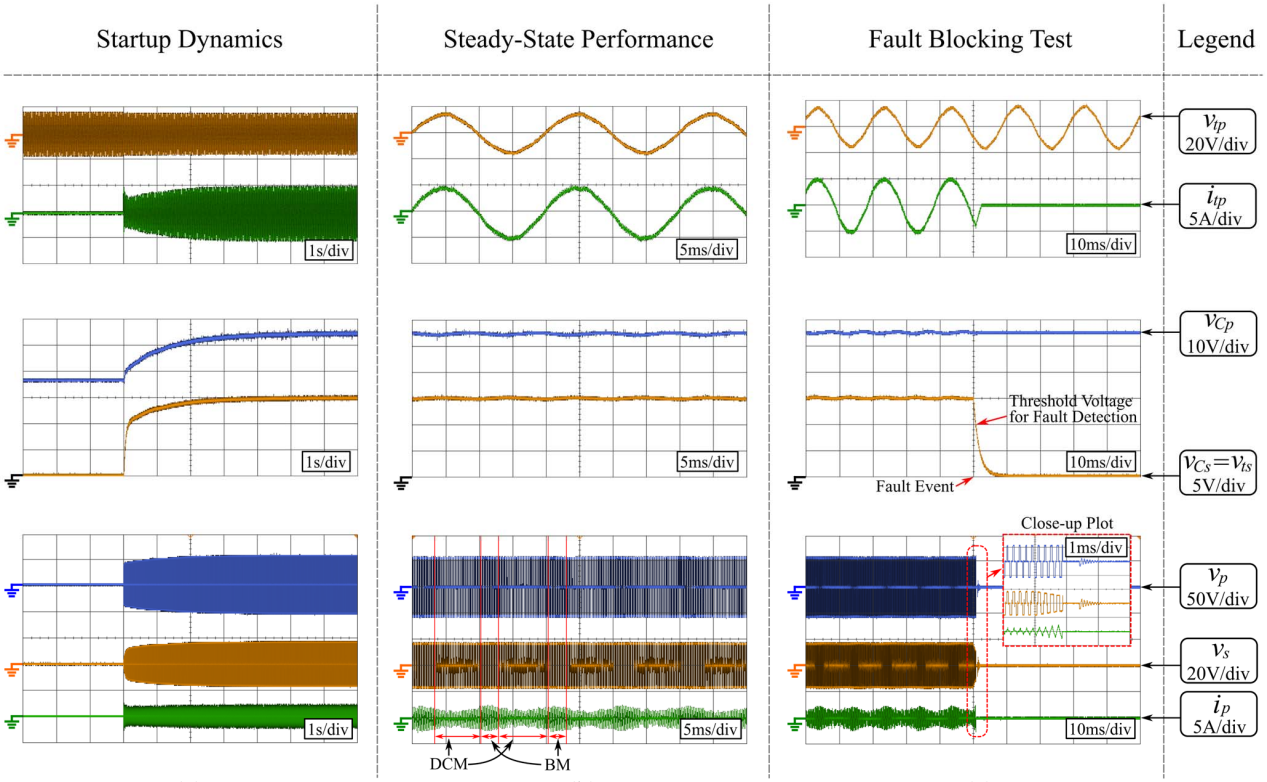

Fig. 14. Experiment results. (a) Start-up dynamics. (b) Steady-state waveforms. (c) Dc-side short-circuit fault blocking test.

VI. Conclusions

A BFB concept is proposed in this paper, which improves the control dynamics of BHB converters by ensuring the volt-second-balance in each switching period, and gives an enhanced power delivery ability thanks to the full bridge structure. Additionally, the BFB is also modified to fit the ac-dc application. For validating the BFB concept, a BFB-SAB isolated ac-dc converter is proposed, as an example case from the BFB converter family. The proposed converter has advantages including high power density, galvanic isolation, flexible voltage step ratio, simple structure, simple control, and dc-side short-circuit fault-blocking capability. Operation principles are analysed. Experiment results are also given to validate the corresponding theoretical analysis.

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