Comparative Study of Soft-Switched Isolated DC-DC Converters for Auxiliary Railway Supply

Olivier Deblecker, Adriano Moretti, and François Vallée

***Abstract*—In modern railways coaches, the electrical separation between the high voltage side and the auxiliary equipments on the consumer side is realized by means of heavy and bulky 50-Hz transformers. In order to reduce the weight and size of the devices, today new power supply systems are proposed that consist in soft-switched isolated dc-dc converters with a lightweight medium frequency transformer and diverse output modules supplied by a common 600-V dc intermediate circuit. This paper aims to investigate in detail two such solutions of isolated dc-dc converters for auxiliary railway supply where zero-current transitions are achieved for the primary inverter switches. A comparison based on several criteria (overall power rating, losses in power semiconductor devices, operation in the whole range of load, etc.) is presented.**

***Index Terms*—Auxiliary power supply, dc-dc converters, railway traction, soft-switching.**

I. Introduction

DUE TO increased comfort and higher traveling speed demands, modern railways coaches require a continuous energy supply to auxiliary equipments such as air conditioning, lighting, pressure protection, etc. Due to the different voltage levels of the European trains, the electric energy from the locomotive is transferred to the coaches via a supply line with the nominal voltage varying from 1-kV ac to 3-kV dc [1]. For instance, the Belgian railways (Société Nationale des Chemins de fer Belges-SNCB) are supplied by 3-kV dc voltage. The supply voltage of the consumers connected to such an electricity supply unit reaches from 24 V for battery charger to three-phase 400-V ac for three-phase consumers. The frequency of the output voltage can be fixed 50 Hz or variable frequency.

Currently, the electrical separation between the high voltage side (3-kV dc) and the consumers side at each output port of the power supply system of the auxiliary equipments is realized by heavy and bulky 50-Hz transformers (see Fig. 1). In order to reduce the size and weight of the devices (filters, low frequency transformers, etc.), new power supply systems [2]–[4] are considered that consist of soft-switched dc-dc converters and diverse output modules supplied by a common 600-V dc intermediate circuit. The input and output sides are electrically separated by a lightweight medium frequency (MF) transformer

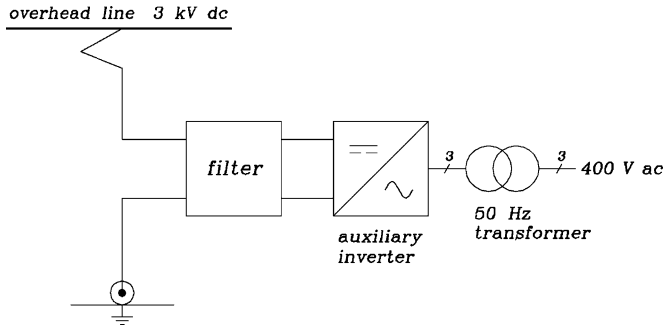

Fig. 1. Power supply system of three-phase 400-V ac consumers realized by a 50-Hz transformer.

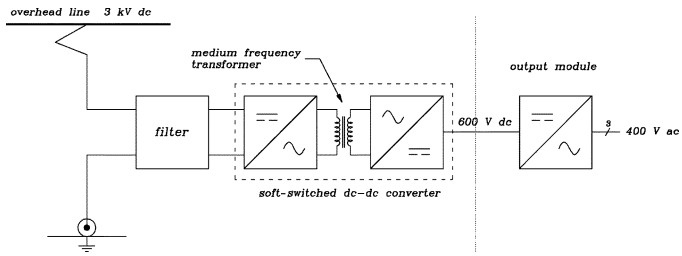

Fig. 2. Power supply system of three-phase 400-V ac consumers realized by a soft-switched dc-dc converter and output module.

(typically several kilohertz) as shown in Fig. 2. Such an approach is in keeping with other research activities that have been going on in railway traction to substitute the low frequency transformer, commonly used to reduce the line voltage to a level more convenient for motors, by alternative solutions, either with an intermediate conversion stage using MF transformers ("MF-topologies") [5]–[8] or by means of transformerless configurations [9], [10].

To enable operating at high frequency with reduced EMI and switching losses, several soft-switching techniques for high-power isolated dc-dc converters have been proposed in the literature (see, e.g., [11]–[17]). These can be classified into two groups, namely zero-voltage switching (ZVS) and zero-current-switching (ZCS), where the soft transitions are (most often) achieved by the use of an auxiliary circuit that creates some form of inductance–capacitance (*LC*) resonance [18], [19].

The present contribution aims to investigate two different solutions of half bridge zero-current switching pulse-width modulation (HB-ZCS-PWM) dc-dc converters for auxiliary railway supply. It follows previous works devoted to ZVS isolated dc-dc converters for railway applications [20]–[22]. The first converter topology, suggested by Alstom Transport, makes use of an auxiliary circuit somewhat similar to that

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TABLE I
OPERATING CONDITIONS

Maximum output power	P_o	100 kW
DC input voltage	V_d	2 ~ 4 kV
DC output voltage (regulated)	V_o	600 V
Load current	I_o	0 ~ 333 A
Switching frequency	f_s	4 kHz

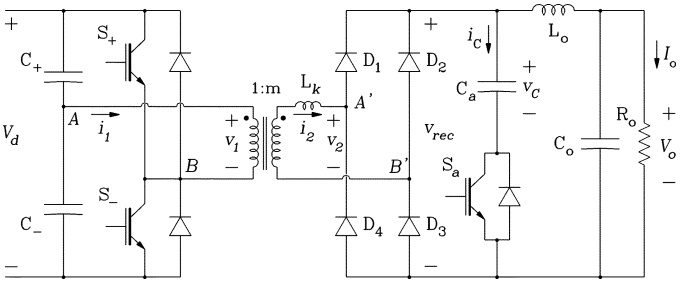

Fig. 3. First topology of HB-ZCS-PWM dc-dc converter.

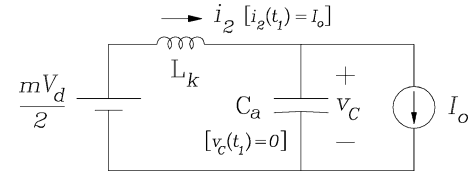

Fig. 4. Equivalent series-resonant circuit during mode 2 (topology #1).

considered in [23], which is attached to the secondary side of the MF transformer in order to achieve ZCS. The second converter is inspired by a patented circuit topology [2], [24] consisting of a primary hard-switched step-up module to supply an HB-ZCS inverter, with an intermediate leg of resonant capacitors. The proposed solutions, using 6.5-kV IGBT transistors as high-voltage switches [25], [26], should meet the requirements of operating conditions listed in Table I, where the main working parameters are the input voltage, subject to wide variations, and the output current that can vary from no load up to twice the value of the rated current (at 3-kV nominal input).

This paper is organized as follows. In Section II, we present the two dc-dc converter topologies and their principles of operation. In Section III, we discuss the design of the resonant parameters in order to achieve soft-switching. We also state the design equations from which the maximum voltage and current stresses of the power devices can be determined. Then, simulation results are shown in Section IV to complete the theoretical analysis. The steady-state output voltage characteristics are examined in order to verify the ability of each converter to supply the specified output voltage in the whole range of load. Finally, in Section V, we carry out the comparative analysis of the two candidates dc-dc converter topologies for auxiliary railway supply based on several criteria such as power losses in semiconductor devices, overall power rating, etc.

II. TOPOLOGIES AND PRINCIPLES OF OPERATION

A. First Topology

The first HB-ZCS-PWM dc-dc converter topology is shown in Fig. 3. A simple auxiliary circuit consisting of a resonant capacitor C_a and an auxiliary switch S_a is attached to the secondary side in order to achieve ZCS for the primary switches S_+ and S_-. L_k refers to the leakage inductance of the transformer. $D_1 \sim D_4$ are the output rectifier diodes. V_d, V_o and I_o are the dc input voltage, output voltage and output current, respectively. The transformer turns ratio is denoted by m (primary to secondary).

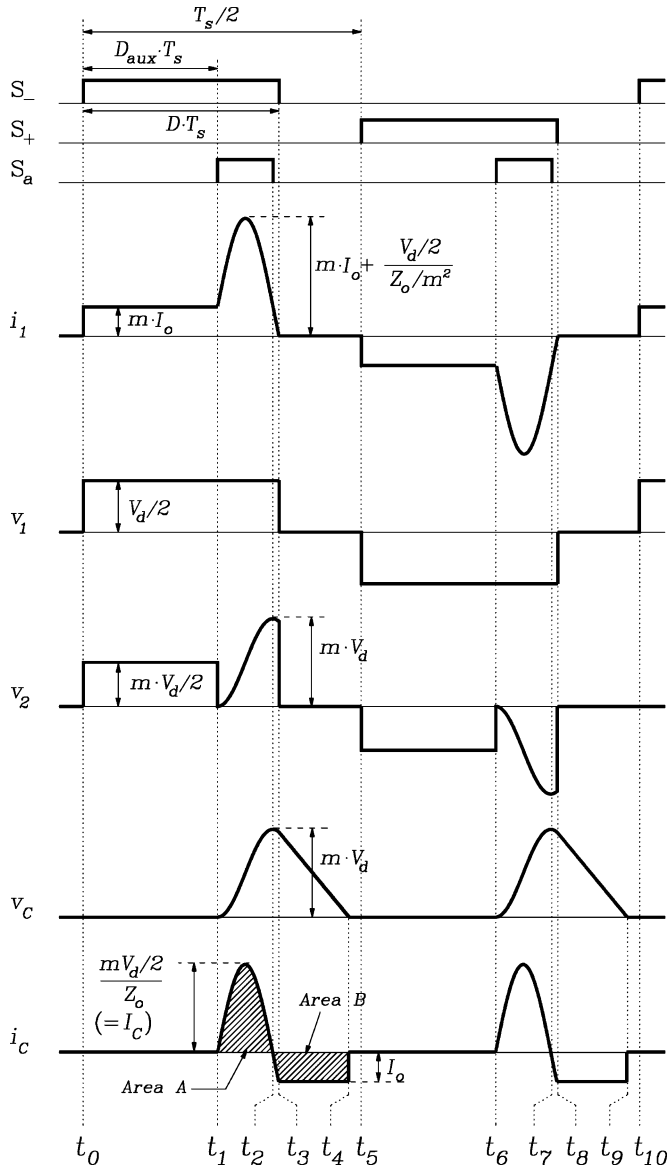

Fig. 5. Operational key waveforms of topology #1.

Fig. 5 shows the operational key waveforms of the converter. One cycle period T_s $(= 2\pi/\omega_s)$ is divided into two half cycles, $t_0 \sim t_5$ and $t_5 \sim t_{10}$. Because the operating principles of two half cycles are symmetric, only the first half cycle is explained.

This half-cycle is divided into five modes. For convenience of the mode analysis in the steady state, several assumptions are made as follows.

- All components used in this converter have ideal characteristics; the transformer leakage inductance will, however, not be neglected.
- C_+, C_- and L_o are large enough to be considered as constant voltage sources $V_d/2$, $V_d/2$, and constant current source I_o, respectively.

Each operating mode is simply described as follows.

Mode 1 $[t_0 \sim t_1]$: In this mode, S_- turns on and the power is delivered from the input to the output. This operating mode is just the same as for a conventional hard switching PWM HB converter.

Mode 2 $[t_1 \sim t_2]$: At time t_1, the auxiliary switch S_a turns on, the resonance between L_k and C_a starts. At t_2, the voltage across the resonant capacitor reaches $m \cdot V_d$ and the transformer secondary side current decreases to the value of the output current I_o. Referring to Fig. 4, the resonant voltage across C_a and the resonant current in L_k are given as

$$v_C = \frac{mV_d}{2}\left[1 - \cos\left(\omega_0(t - t_1)\right)\right] \tag{1}$$

$$i_2 = I_o + \frac{mV_d}{2Z_0}\sin\left(\omega_0(t - t_1)\right) \tag{2}$$

where $\omega_0 = 1/\sqrt{(L_k \cdot C_a)}$ and $Z_0 = \sqrt{(L_k/C_a)}$.

Mode 3 $[t_2 \sim t_3]$: At time t_2, the capacitor current reverses and now must flow through the anti-parallel diode of S_a. In the same time, S_a can be turned off with ZCS. The resonant capacitor is discharged according to (1) and the secondary current decreases to zero according to (2).

Mode 4 $[t_3 \sim t_4]$: At time t_3, the secondary current reduces to zero and cannot change direction. The reflected current in the primary side is cancelled in S_-. The switch can therefore be turned off with ZCS at t_3. During this mode, the output rectifier diodes are all turned off, while the resonant capacitor C_a is discharged linearly by the output current I_o.

Mode 5 $[t_4 \sim t_5]$: At t_4, the voltage across C_a reduces to zero and the capacitor current is forced to zero (it corresponds to area $A = B$ in Fig. 5). The output current I_o freewheels through $D_1 \sim D_4$ and the secondary voltage reduces to zero. Since S_+ and S_- are both turned off, the primary current cannot flow and the primary voltage is imposed to zero by the secondary.

From the previous analysis, the first topology of dc-dc converter achieves ZCS for both the primary and auxiliary switches. The operating modes during the subsequent half cycle are symmetric to those described previously. It should be noticed that the anti-parallel diodes of the primary switches (commercial IGBT modules) are not used during operation.

Hereafter, the equations will be normalized by using the base voltage and current

$$V_{\text{base}} = m \cdot V_d/2 \tag{3}$$

$$I_{\text{base}} = \frac{V_{\text{base}}}{Z_0}. \tag{4}$$

Assuming that the resonant capacitor is completely discharged at $t_0 + T_s/2$, the steady-state output voltage characteristics for different values of D_{aux} and a given applied input voltage V_d can be expressed as follows:

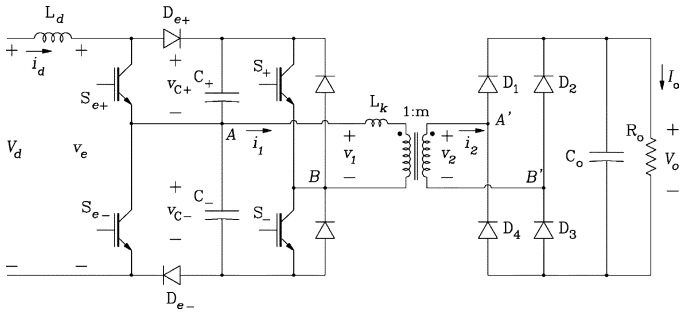

Fig. 6. Second topology of HB-ZCS-PWM dc-dc converter.

$$V_{oN} = 2D_{\text{aux}} + \frac{k}{\pi}\left[(\alpha + \pi) + I_{oN} + \frac{1}{2I_{oN}}(\cos\alpha + 1)^2\right] \tag{5}$$

where the ratio ω_s/ω_0 is simply denoted by k, the operational duty cycle D_{aux} is defined from the time delay between t_0 and the turn-on of S_a, and

$$\alpha = \arcsin(I_{oN}). \tag{6}$$

Note that the normalized quantities are denoted by an additional subscript "N."

For given values of the applied input voltage and the operational duty cycle D_{aux}, the minimum load current can be determined in solving the following implicit expression:

$$I_{o,\min N} = \frac{1 + \cos\alpha_{\min}}{\frac{\pi}{k} \cdot (1 - 2D_{\text{aux}}) - (\alpha_{\min} + \pi)} \tag{7}$$

which expresses the voltage across C_a exactly reduces to zero at the end of a half-cycle, i.e., at $t_4 = t_5\ (= t_0 + T_s/2)$.

B. Second Topology

The second dc-dc converter topology is shown in Fig. 6. Basically, the primary converter module is a conventional hard switching PWM step-up converter consisting of two switches S_{e+} and S_{e-} connected in series which are coupled to a soft switching HB-PWM inverter. The leakage inductance L_k (here defined in the primary side of the transformer) together with the capacitors C_+ and C_- of the step-up converter form the resonant elements of the HB-ZCS inverter. Hereafter, the same notations and basic assumptions as for the first studied topology will be used. Furthermore, we get the following.

- The leg of resonant capacitors (C_+, C_-) is assumed a constant voltage source to determine the input current waveform $i_d(t)$ and the steady-state output voltage characteristics.
- L_d is assumed a constant current source to determine the voltages $v_{C+}(t)$ and $v_{C-}(t)$ across the series resonant capacitors.

At this stage, we state D_e to be the duty cycle of the step-up converter. It will be varied to adjust the average voltage across the series resonant capacitors and, hence, the dc output voltage (C_o is assumed large enough to be considered as a constant voltage source). Due to the previously mentioned connection

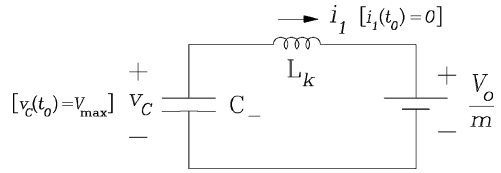

Fig. 7. Equivalent series-resonant circuit during mode 1 (topology #2).

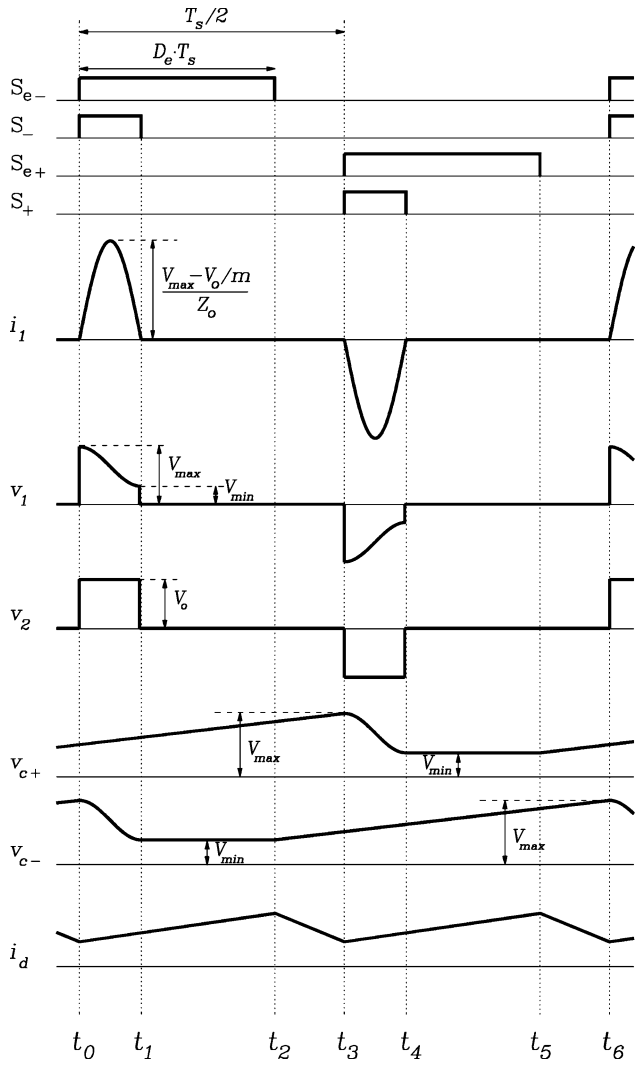

Fig. 8. Operational key waveforms of topology #2.

between the input step-up converter and the HB inverter, the common capacitance value C of the series resonant capacitors can be kept low, as will be shown.

Fig. 8 shows the operational key waveforms of the converter operating in the continuous-conduction mode, i.e., when the inductor current i_d flows continuously in the steady state. D_e is assumed a value less than 0.5 in order to avoid the conduction intervals of the switches S_{e+} and S_{e-} overlapping one another.

The first half-cycle is divided into three operating modes. Each one is simply described as follows.

Mode 1 $[t_0 \sim t_1]$: At t_0, S_{e-} and S_- are both turned on, the resonance between L_k and C_- starts. D_{e+} is conducting, while D_{e-} becomes reverse biased. Since the rectifier diodes D_1 and D_3 are conducting, referring to Fig. 7, the resonant voltage across C_- and the resonant current in L_k are given by

$$v_{C-} = V_{\max} - \left(V_{\max} - \frac{V_o}{m}\right) \cdot [1 - \cos(\omega_0 (t - t_1))] \quad (8)$$

$$i_1 = \frac{V_{\max} - V_o/m}{Z_0} \sin(\omega_0 (t - t_1)) \quad (9)$$

where $\omega_0 = 1/\sqrt{(L_k \cdot C)}$ and $Z_0 = \sqrt{(L_k/C)}$.

According to the previously mentioned assumptions, the current through L_d increases linearly and C_+ is charged linearly as well.

Mode 2 $[t_1 \sim t_2]$: At t_1, the primary current decreases to zero. Therefore, S_- can be turned off with ZCS. During this interval, the output rectifier diodes are all turned off. Both the primary and secondary voltages are cancelled. C_+ is still being charged linearly as the path (S_{e-}, D_{e+}) remains on until t_2. The voltage across C_- is clamped to $V_{\min}$.

Mode 3 $[t_2 \sim t_3]$: At t_2, S_{e-} is turned off and the current is transferred to the diode D_{e-}. This mode is characterized by the sole conduction of the diodes D_{e+} and D_{e-}, and the input current i_d decreases linearly. The corresponding amount of inductive energy is released to the capacitors C_+ and C_- which are charged linearly.

From the previous analysis, it appears that the second topology of dc-dc converter only achieves ZCS for the HB inverter switches, the input stage being a hard switched step-up converter. The operating modes during the subsequent half cycle are symmetric to those described previously.

The steady-state output voltage characteristics for different values of the duty ratio D_e can be obtained by expressing that the average rectified secondary current is equal to I_o over one cycle period. Using the normalized quantities (3) and (4), it follows:

$$V_{oN} = \frac{1}{1 - D_e} + m^2 \pi \frac{D_e - D_{e,\min}}{2k} \cdot I_{oN} \quad (10)$$

where $D_{e,\min}$ $(= k/2)$ corresponds to the lowest value of the duty cycle (for which the conduction intervals of S_{e-} and S_- are identical). In practice, as will be shown in Section III, those characteristics are straight lines with very small positive sloops, which means that the converter almost operates as a dc voltage source $V_{oN} \cong 1/(1 - D_e)$, just in the same fashion as a conventional step-up converter.

It should be pointed out that (10) is not valid in the whole range of values of the output current. Indeed, at light loads, the converter operates in the discontinuous-conduction mode (as regards the input current). This mode has also been studied analytically. Yet, the corresponding (tedious) developments will not be exposed in this paper for the sake of conciseness. As will be shown further, in this discontinuous mode, the output voltage characteristics are like (but not exactly) pieces of hyperbola.

III. Design Considerations

A. First Topology

1) Resonant Components: In order to achieve ZCS for the primary switches in every load conditions, the peak resonant

TABLE II
ANALYTICAL EXPRESSIONS OF THE MAXIMUM VOLTAGE AND CURRENT STRESSES OF THE POWER DEVICES USED IN TOPOLOGY #1

Power devices	Peak voltage	Peak, average and rms currents
S_+, S_-	$V_{S,\text{peak}} = V_{d,\max}$	$I_{S,\text{peak}} = m\cdot\left(I_{\text{o,max}} + I_{C,\max}\right),\ \ I_{S,\text{ave}} = \frac{V_\text{o}\cdot I_{\text{o,max}}}{V_{d,\min}},$ $I_{S,\text{rms}} = m\cdot\sqrt{\frac{V_\text{o}\cdot I_{\text{o,max}}^2}{m\cdot V_{d,\min}} + \frac{k}{2\pi}\left(-\frac{I_{\text{o,max}}^3}{I_{C,\min}} + \left(-\xi_1^2+\xi_1+3\right)\cdot\frac{I_{\text{o,max}}\cdot I_{C,\min}}{2} + \frac{\alpha_1+\pi}{2}\cdot I_{C,\min}^2\right)}$
S_a	$V_{S_a,\text{peak}} = \frac{mV_{d,\max}}{2}$	$I_{S_a,\text{peak}} = I_{C,\max},\ \ I_{S_a,\text{ave}} = \frac{2k}{\pi}\cdot I_{C,\max},\ \ I_{S_a,\text{rms}} = \frac{\sqrt{k}}{2}\cdot I_{C,\max}$
D_a	$V_{D_a,\text{peak}} = \frac{mV_{d,\max}}{2}$	$I_{D_a,\text{peak}} = I_{\text{o,max}},\ \ I_{D_a,\text{ave}} = I_{S_a,\text{ave}},\ \ I_{D_a,\text{rms}} = \sqrt{\frac{k}{2\pi}\cdot\left(\left(\xi_2+2\right)\cdot I_{\text{o,max}}\cdot I_{C,\max} + \alpha_2\cdot I_{C,\max}^2\right)}$
$D_1 \sim D_4$	$V_{D,\text{peak}} = mV_{d,\max}$	$I_{D,\text{peak}} = \frac{I_{S,\text{peak}}}{m},\ \ I_{D,\text{ave}} = \frac{I_{\text{o,max}}}{2},$ $I_{D,\text{rms}} = \sqrt{\left(\frac{V_\text{o}}{m\cdot V_{d,\max}}+\frac{1}{2}\right)\frac{I_{\text{o,max}}^2}{2} + \frac{k}{4\pi}\left(-\frac{I_{\text{o,max}}^3}{I_{C,\max}} + \left(\alpha_2+\pi\right)\cdot\left(2I_{\text{o,max}}^2 + I_{C,\max}^2\right) - 3\cdot\xi_2\cdot\left(\xi_2+1\right)\cdot\frac{I_{\text{o,max}}\cdot I_{C,\max}}{2}\right)}$

current in the auxiliary circuit should be larger than the maximum output current. Therefore, according to (2), L_k and C_a should satisfy

$$\sqrt{\frac{L_k}{C_a}} \le \frac{1}{2}\frac{mV_d}{I_{o,\max}} \tag{11}$$

where $I_{o,\max}$ is the maximum output current. Otherwise stated, for given transformer characteristics m and L_k, the following condition should be adopted:

$$C_a \ge C_{a,\min} \tag{12}$$

where

$$C_{a,\min} = 4L_k\cdot\left(\frac{I_{o,\max}}{mV_d}\right)^2. \tag{13}$$

The resonant period of L_k and C_a should be limited to a reasonable part of the whole switching period. In practice, the minimum turn on time of the primary switches S_+ and S_- should be larger than the required turn on time of the auxiliary switch, which is determined by the resonant period. If the resonant period is too long, the required minimum duty cycle D will be increased. Otherwise, the ZCS condition will be lost at some particular conditions. Usually, the resonant period should therefore be a small part of the switching period, which can be expressed as

$$T_0 = 2\pi\cdot\sqrt{L_kC_a} = k\cdot T_s \tag{14}$$

where $T_0\ (=2\pi/\omega_0)$ is the resonant period, T_s the switching period, and k represents the maximum acceptable value of T_0/T_s, which should be limited to a reasonable value (say 20%).

Based on (12)–(14), the resonant parameters can be calculated and the smaller one should be adopted in the design.

2) Power Devices: The design equations reported in Table II provide suitable ratings of the power semiconductor devices under worst case operating conditions to ensure proper operation of the converter. For reasons of conciseness, the complete developments of the proposed design equations cannot be exposed here. Still these have been derived by applying the conventional definitions of the peak, average, and rms values to the devices voltage and current idealized waveforms (deduced from the previous theoretical analysis in Section II). Using (5) (non-normalized), the auxiliary duty cycle was also substituted with an expression in terms the output voltage and the output current. The ratings of the devices calculated from the given design equations provide a good approximation for the final values used in an actual implementation which, however, may be somewhat different due to other practical considerations [25].

The maximum and minimum peak resonant current through the resonant capacitor C_a are defined by

$$I_{C,\max} = \frac{m\cdot V_{d,\max}}{2Z_0} \qquad I_{C,\min} = \frac{m\cdot V_{d,\min}}{2Z_0}. \tag{15}$$

Referring to Table II, the maximum voltage stress across both the primary and secondary power devices occurs at the maximum input voltage $V_{d,\max}$. Under the condition that the output voltage is properly regulated, the maximum current stress through the secondary side devices arises for the maximum output current and the maximum input voltage (i.e., for the highest value of the peak resonant current). In the primary side, it is noticed that the maximum stress in terms of average and rms currents through the primary switches, S_+ and S_-, occurs at the minimum input voltage.

Note that, in order to calculate the rms currents reported in Table II, we also defined

$$\alpha_1 = \arcsin\left(\frac{I_{o,\max}}{I_{C,\min}}\right),\quad \alpha_2 = \arcsin\left(\frac{I_{o,\max}}{I_{C,\max}}\right) \tag{16}$$

and, hence, $\xi_1 = \cos(\alpha_1)$ and $\xi_2 = \cos(\alpha_2)$.

B. Second Topology

1) Resonant Components: As for topology #1, the resonant period of L_k and C should be a reasonable part of the whole switching period. Indeed, if the resonant period T_0 is too long, the required minimum duty cycle $(D_{e,\min})$ will be increased to ensure that S_- turns off with ZCS at t_1 before the end of the

TABLE III
ANALYTICAL EXPRESSIONS OF THE MAXIMUM VOLTAGE AND CURRENT STRESSES OF THE POWER DEVICES USED IN TOPOLOGY #2

Power devices	Peak voltage	Peak, average and rms currents
S_{e+}, S_{e-}	$V_{S_e,\text{peak}} = \frac{V_o}{m}$	$I_{S_e,\text{peak}} = \frac{V_o \cdot I_{o,\max}}{V_{d,\min}}$, $I_{S_e,\text{ave}} = \left(\frac{V_o}{V_{d,\min}} - \frac{m}{2}\right) \cdot I_{o,\max}$, $I_{S_e,\text{rms}} = \sqrt{\frac{V_o}{V_{d,\min}} \cdot \left(\frac{V_o}{V_{d,\min}} - \frac{m}{2}\right)} \cdot I_{o,\max}$
D_{e+}, D_{e-}	$V_{D_e,\text{peak}} = \frac{V_o}{m}$	$I_{D_e,\text{peak}} = I_{S_e,\text{peak}}$, $I_{D_e,\text{ave}N} = I_{S,\text{ave}}$, $I_{D_e,\text{rms}N} = \sqrt{\frac{m}{2} \cdot \frac{V_o}{V_{d,\min}}} \cdot I_{o,\max}$
S_+, S_-	$V_{S,\text{peak}} = \frac{2V_o}{m}$	$I_{S,\text{peak}} = \frac{\pi}{2k} m \cdot I_{o,\max}$, $I_{S,\text{ave}} = \frac{1}{2} m \cdot I_{o,\max}$, $I_{S,\text{rms}} = \frac{\pi}{4\sqrt{k}} m \cdot I_{o,\max}$
$D_1 \sim D_4$	$V_{D,\text{peak}} = V_o$	$I_{D,\text{peak}} = \frac{I_{S,\text{peak}}}{m}$, $I_{D,\text{ave}} = \frac{I_{S,\text{ave}}}{m}$, $I_{D,\text{rms}} = \frac{I_{S,\text{rms}}}{m}$

conduction interval of S_{e-}. On another hand, if it is too short, the peak resonant primary current will become prohibitive.

Therefore, in practice, the resonant parameters should be calculated so that the ratio T_0/T_s is equal to about 20%. Hence, for typical values of L_k (say a few microhenrys), the common capacitance C of the resonant capacitors is kept low (about ten microfarads) in the case of medium switching frequency (4–5 kHz).

2) Power Devices: The ratings of the devices used in topology #2 can be estimated based on the design equations reported in Table III. These have been derived for the most demanding operating conditions, in a similar fashion to the first topology, but with the following assumptions.

- The voltage ripple across the leg of resonant capacitors can be neglected to determine the maximum voltages applied to the devices.
- The ripple in the input current is ignored to establish the peak, average, and rms currents of the power devices.

In order that the (regulated) output voltage appears explicitly in the design equations, the duty cycle D_e was also substituted from (10) (non-normalized) neglecting the output current-proportional term (i.e., the converter operates as a dc voltage source).

From the results reported in Table III, it is noticed that the maximum voltage stress across both the primary and secondary devices is proportional to the output voltage level, whatever voltage applied at the input (provided that a control loop properly adjusts the duty cycle of the input step-up converter). The maximum current stress occurs, as for it, under the maximum output current and the minimum input voltage.

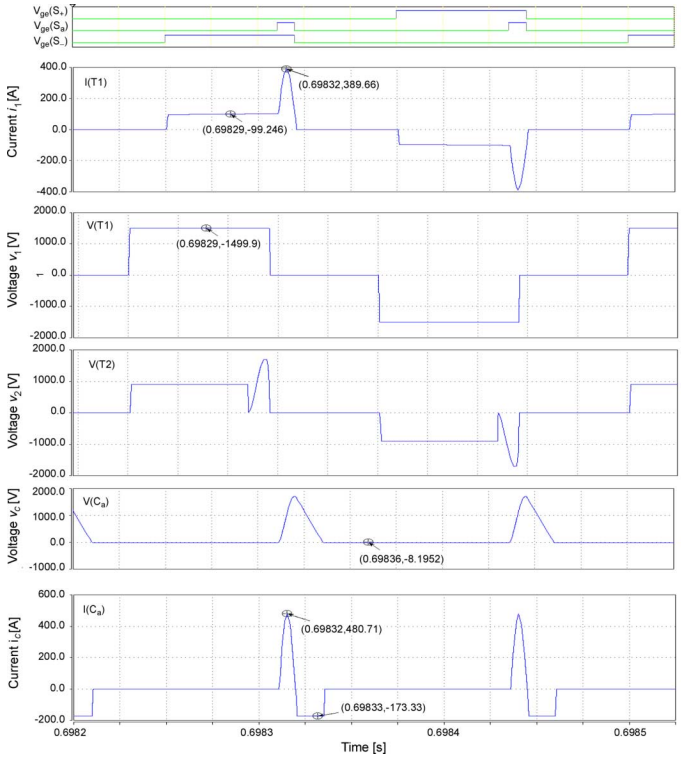

Fig. 9. Simulation waveforms (Traces from top to bottom: gate drive voltage v_{ge} of S_+, S_a and S_-, primary current i_1, primary and secondary voltages v_1 and v_2, resonant capacitor voltage v_C, and current i_C). Full load condition (V_d = 3 kV, P_o = 100 kW, I_o =166 A, $D_{\text{aux}} = 0.237$).

IV. SIMULATIONS AND ANALYSIS

To verify the theoretical analysis, simulation results obtained with Saber [27] are presented.

A. First Topology

The simulation waveforms at full load condition are represented in Fig. 9. The output filter parameters are $L_o = 2\ \mu$H and $C_o = 11.4\ \mu$F. The transformer turns ratio is selected to be 0.6 at 600 V output arguing that, when the input voltage V_d decreases to its minimum value (2 kV), the primary switches should be conducting each one about a half cycle (i.e., the longest allowed duration) in order to obtain the lowest peak resonant primary current. The resonant circuit parameters are chosen to be $L_k = 4\ \mu$H and $C_a = 1.5\ \mu$F, which corresponds to a resonant frequency of 65 kHz (that is about 16 times the switching frequency f_s). It can be verified, using (11)–(13), that for the given circuit parameters, the worst ZCS condition can be achieved (i.e., for the maximum output current 2×166 A $= 333$ A at 2-kV input) as

$$C_{a,\min} = 4 \times 4 \cdot 10^{-6} \times \left(\frac{333}{0.6 \cdot 2000}\right)^2 = 1.23\ \mu\text{F}$$

is less than the previously selected value of C_a ($= 1.5\ \mu$F).

TABLE IV
MAXIMUM VOLTAGE AND CURRENT STRESSES OF THE DEVICES USED IN TOPOLOGY #1. COMPARISON BETWEEN ANALYTICAL AND SIMULATION RESULTS

	Analytical				Simulation			
	Volt. [V]	Current [A]			Volt. [V]	Current [A]		
Device	peak	peak	ave.	rms	peak	peak	ave.	rms
S_+, S_-	4000	640	99.6	146	3998	573	95.2	142
S_a	1200	735	28.8	91.2	1165	624	22.4	126
D_a	1200	332	28.8	96.9	1165	343	22.0	86.3
D_1~D_4	2400	1066	166	227	2331	941	166	227

In the previous theoretical analysis, it has been mentioned that the auxiliary switch S_a and the primary switches (say S_-) could be turned off with ZCS at t_2 and t_3, respectively. However, considering the gate drive signals shown in Fig. 9, one may notice that the two switches are turned off at the same time corresponding to $t_3\ (= t_0 + D_{\rm aux}T_s + T_0)$, when the primary current decreases to zero, plus some short time delay $T_{\rm delay}$ to prevent a possible small increase of the resonant period T_0 with regard to its theoretical value [see (14)]. This control technique was found more convenient in practice since zero-crossing detection of the resonant current in S_a is avoided. Normally, $T_{\rm delay}$ should be a value large enough to ensure that ZCS is achieved at $t_3 + T_{\rm delay}$ in all operating conditions, though not too large to be certain both primary and auxiliary switches are turned off before the end of the first half cycle.

The maximum voltage and current stresses across and through the power devices are reported in Table IV. The results have been calculated both from the design equations stated in Section III and in simulation, assuming the most demanding operating conditions and 600-V output. For instance, the maximum stresses were selected among the whole set of results obtained from the simulations performed under different input voltages (taken successively 2–4 kV) and for the maximum load current ($I_{o,\max} = 2 \times 166$ A). As shown in Table IV, there is a good agreement between the analytical and simulation results.

Fig. 10 shows the steady-state output voltage characteristics at 3-kV input for different values of $D_{\rm aux}$, obtained both theoretically, using (5), and from simulations. The minimum load current condition, shown by a dashed line, is established by (5)–(7) for every $D_{\rm aux}$. Considering, e.g., the characteristic obtained with $D_{\rm aux} = 0.333$, the minimum load current $I_{o,\min N}$ and the corresponding output voltage V_{oN} are found to be equal to 0.147 and 1.001 p.u, respectively. As a matter of fact, the values of V_{oN} as a function of $I_{o,\min N}$ remain (quasi) unity whatever operational duty cycle $D_{\rm aux}$ is chosen and, hence, the minimum load boundary curve looks like an horizontal line segment. Furthermore, it should be pointed out that the theoretical characteristics are not physically realistic, and so they are not represented, above that boundary line (i.e., for $I_{oN} < I_{o,\min N}$). Indeed, in that case, the output current is not sufficient to discharge completely the resonant capacitor every half cycle; therefore, (5) is no longer a valid expression. In order to get an insight into this incomplete-discharge mode, extra simulations have been conducted. So, the steady-state output voltage characteristics obtained with $D_{\rm aux} = 0$, 0.055 and 0.111 have been represented as well in Fig. 10.

From Fig. 10, it can now be concluded that the converter topology under consideration will not be able to supply 600-V output at light loads. Consider indeed the action of a control loop adjusting $D_{\rm aux}$ to maintain the output voltage V_o to its reference value (600 V). If the converter would initially be operating in point 1 at $V_o > 600$ V, the regulator will reduce $D_{\rm aux}$ to 0.111 so as to restore 600 V output in point 2. From there, if the load would suddenly decrease, the operating point will move to point 3 located in the incomplete-discharge mode region (with $D_{\rm aux}$ still equal to 0.111). From this moment, the sole action of the regulator will not be enough to restore 600 V output. Indeed, as the output voltage controller would reduce $D_{\rm aux}$ to zero, the converter will get stuck in point 4 at $V_o > 600$ V.

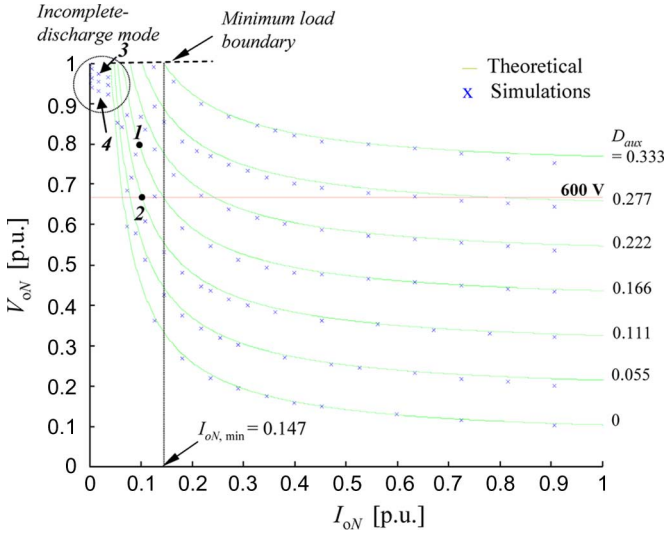

Fig. 10. Steady-state output voltage characteristics ($V_d = 3$ kV). Dashed curve: minimum load current boundary.

In order to circumvent this drawback, a solution consists in making the auxiliary circuit inoperative. Every half-cycle, the power is delivered from input to output such as in mode 1 and the primary switch (say S_-) is turned off at t_1 achieving a hard switching transition. In this case, the switching power loss is reduced since the switch current is small.

B. Second Topology

The simulation waveforms at full load condition are illustrated in Fig. 11. The input inductance and output capacitance are $L_d = 5$ mH and $C_o = 10$ mF, respectively. The transformer turns ratio is selected to be 0.28 at 600 V output, assuming a 4 kV input voltage and $D_e = D_{e,\min}\ (= 0.1)$. The resonant circuit parameters are chosen to be $L_k = 4\ \mu$H and $C = 15.8\ \mu$F, which corresponds to the resonant frequency of 20 kHz. Hence, the required minimum duty cycle is 0.1.

Unlike the first topology, it can be noticed from the theoretical analysis that S_- (or S_+) is always conducting the same time duration corresponding to one half of the resonant period, whatever the load current. This makes the control much easier than for topology #1 since one knows in advance that, e.g., S_- can be turned off with ZCS at $t_1 = t_0 + T_0/2$. Note that, in practice, it is advisable to introduce some time delay and, hence, rather turn off S_- at $t_0 + T_0/2 + T_{\rm delay}$. Indeed, this allows one to account for a possible small increase of the resonant period T_0 with regard to its theoretical value (calculated from the rated resonant circuit parameters).

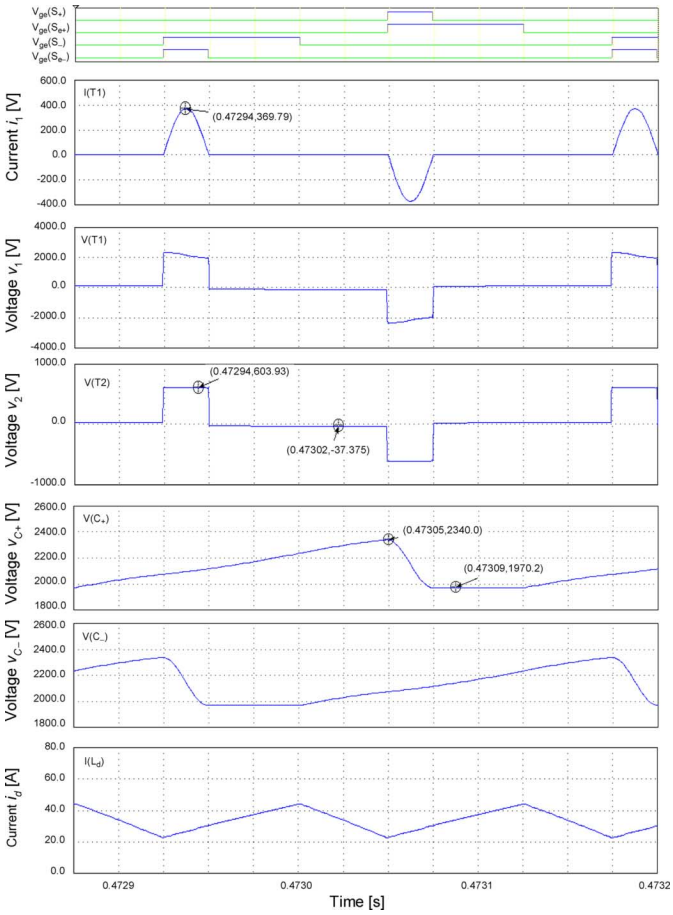

Fig. 11. Simulation waveforms (Traces from top to bottom: gate drive voltage $v_{\rm ge}$ of S_+, S_{e+}, S_- and S_{e-}, primary current i_1, primary and secondary voltages v_1 and v_2, resonant capacitor voltages v_{C+} and v_{C-}, and input current i_d). Full load condition ($V_d = 3$ kV, $P_o = 100$ kW, $I_o = 166$ A, $D_e = 0.318$).

TABLE V
MAXIMUM VOLTAGE AND CURRENT STRESSES OF THE DEVICES USED IN TOPOLOGY #2. COMPARISON BETWEEN ANALYTICAL RESULTS AND SIMULATION

	Analytical				Simulation			
	Volt. [V]	Current [A]			Volt. [V]	Current [A]		
Device	peak	peak	ave.	rms	peak	peak	ave.	rms
S_{e+}, S_{e-}	2143	99.6	53.1	72.7	2340	95.7	54.2	73.8
D_{e+}, D_{e-}	2143	99.6	46.5	68	2339	102	46	68
S_+, S_-	4286	730	46.5	163	4416	762	49	169
D_1~D_4	600	2607	166	582	602	2705	173	424

In Table V, a comparison is made for the maximum values of the devices voltage and current stresses calculated both from the design equations (see Table III) and using simulation. It is assumed a 600-V output voltage. Once again, a good agreement is found between the analytical and simulation results. As for topology #1, the worst case stresses were selected among the simulation results obtained with different dc input voltages (2–4 kV) and for the highest value of the output current.

Fig. 12 shows the steady-state output voltage characteristics at 3 kV input for different values of D_e. Both the theoretical [obtained by (10)] and simulated characteristics are represented

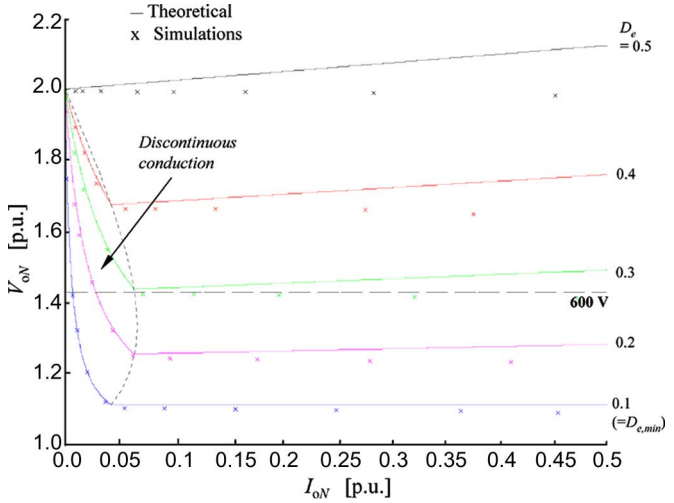

Fig. 12. Steady-state output voltage characteristics. Dashed curve: boundary between continuous and discontinuous conduction in L_d.

using normalized quantities. The dashed line corresponds to the boundary between continuous and discontinuous conduction in L_d. As can be seen, the theoretical and simulated results are in good agreement at light loads. These however diverge as the output current increases to full load, which can be explained as follows. At high load, the voltage ripple across the resonant capacitors leg (C_+, C_-) becomes significant and, therefore, cannot be neglected. Since this was not taken into account in the previous theoretical analysis, (10) obviously yields worse results as the load current becomes large.

It is also observed in Fig. 12 that the second topology of dc-dc converter will not be able to supply 600-V output at light load, which does not fully satisfy to the requested operating conditions (see Table I). In this case, a solution however consists of operating the input step-up converter with a duty cycle D_e less than $D_{e,\min}$ $(= 0.1)$. The simulation waveforms at no load condition are shown in Fig. 13 for $D_e = 0.03$. As can be seen, the output voltage V_o is approximately equal to 564 V. Considering the action of a control loop adjusting D_e, the dc-dc converter should therefore be able to supply 600-V output at no load. Of course, the operational key waveforms are slightly different from those predicted from the theoretical analysis (assuming $D_e \geq D_{e,\min}$). Considering, e.g., the voltage across C_-, when S_{e-} is turned on, the capacitor is first discharged exactly the same way as described previously (step 1). Then, as S_{e-} is turned off (step 2), the input current partly flows through C_- which, at the same time, is still discharged through the path (S_-, D_{e-}). When i_d decreases to zero, the capacitor continues to be discharged normally (step 3). The resonant period of the primary current is now $\sim$ 30 μs which is greater than $T_0/2$ $(= 25\ \mu\text{s})$. Consequently, the HB inverter switches are turned off achieving a hard-switched transition. However, the corresponding power loss is negligible since the switch currents are very small at no load.

V. COMPARISON

A benchmark for the comparison of the two soft-switched isolated dc-dc converters is the number of components they utilize (see Table VI). The first converter topology has three switches,

TABLE VI
POWER COMPONENTS FOR EACH TOPOLOGY

Topology #1	Topology #2
S_+, S_-	S_+, S_-
$D_1 \sim D_4$	S_{e+}, S_{e-}
C_+, C_-	$D_1 \sim D_4$
Transformer	D_{e+}, D_{e-}
L_o, C_o	C_+, C_-
S_a, C_a	Transformer
L_d	L_d, C_o

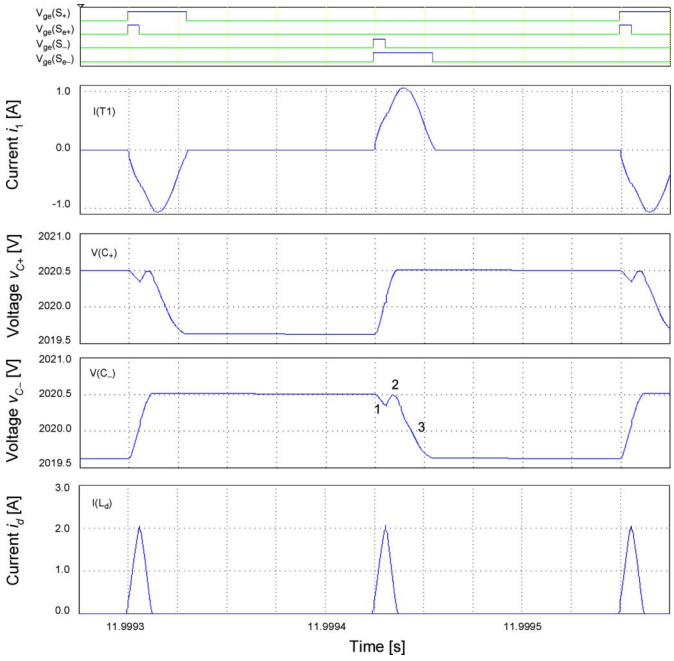

Fig. 13. Simulation waveforms (Traces from top to bottom: gate drive voltage $v_{\rm ge}$ of S_+, S_{e+}, S_- and S_{e-}, primary current i_1, resonant capacitor voltages v_{C+} and v_{C-}, and input current i_d). No load[1] condition ($V_d = 3$ kV, $P_o = 540$ W, $I_o = 0.95$ A, $D_e = 0.030$). [1]The output power of the converter is taken a very small value in order to account for the supply of its own auxiliary equipments, such as fans, etc.

switches, four output rectifier diodes, and seven passive components[1] (including one MF transformer), whereas the second topology makes use of more switches and diodes but includes only five passive components.

Another benchmark is the ratings of the components. Power semiconductor devices must be designed with higher power ratings as they have to withstand large peak voltage and/or current. Table VII lists the power semiconductor devices that can be used in the two converter topologies, and their respective voltage and current required specifications (deduced from the conducted simulations and thermal considerations). Table VII reveals that the primary switches S_+ and S_- have the same ratings for the two topologies. On the contrary, the total current rating of the rectifier diodes of the second converter topology is higher than the companions in the first one. Moreover, the second topology is made of a primary converter module consisting of switches

[1]Although the input inductor L_d was not considered in the previous analysis of the first dc-dc converter topology, it is of course always present to filter the input current drawn from the overhead line. This is the reason why it has been taken into account in Table VI, whereas it was not represented in Fig. 3.

TABLE VII
POWER SEMICONDUCTOR DEVICES AND RATED SPECIFICATIONS

	Power devices	Part number	Rated voltage [kV]	Rated current [A]
Topology #1	S_+, S_-	FZ 200 R65 KF1	6.5	200
	S_a	FF 200 R33 KF2C	3.3	200
	$D_1 \sim D_4$	DD 400 S33 K2C	3.3	400
Topology #2	S_{e+}, S_{e-}	FZ 1200 R33 FF2C	3.3	1200
	D_{e+}, D_{e-}	DD 200 S33 K2C	3.3	200
	S_+, S_-	FZ 200 R65 KF1	6.5	200
	$D_1 \sim D_4$	BYM 300A 120 DNZ (2 in parallel)	1.2	2×300

TABLE VIII
CURRENT AND VOLTAGE RATINGS IN THE TRANSFORMER

	Current [A]				Voltage [V]			
	i_1		i_2		v_1		v_2	
Topol.	rms	peak	rms	peak	rms	peak	rms	peak
#1	167	585	278	976	1301	2000	830	2268
#2	241	761	862	2717	1020	2587	282	618

and diodes with a common voltage rating 3.3 kV and current ratings 1200 and 200 A, respectively, which increases the global power rating of the circuit.

The reduced size and weight of the transformer is a merit of the first topology. This can be explained from the primary/secondary current and voltage ratings listed in Table VIII. These are obtained from the conducted simulations at full load, assuming either 2- or 4-kV input, according to whether the current or voltage ratings are concerned. Although the voltage ratings are higher (especially as concerns the secondary voltage v_2), it can be seen that the requirements in terms of currents are significantly less for topology #1. So, it is expected to bring a reduction in cost of the transformer due to the less material compared to topology #2.

Yet, regarding other parts of the dc-dc converters (mainly passive components), one can expect the overall size and weight reduction gain be rather in favour of topology #2. The qualitative reasons for that are as follows: 1) the first topology includes two additional passive components, C_r and L_o, which do not have their companions in the other topology; 2) the input inductor L_d is expected to be smaller in topology #2 due to the interleaved input current ripple drawn by the primary step-up converter at twice the fundamental frequency compared to topology #1; and 3) due to the connection between the input step-up converter and the HB converter in topology #2, the common capacitance value C of the capacitors leg is kept very low (15.8 μF) compared to the size of the input capacitors required in topology #1 (typically of the order of 10 mF).

The size of the output capacitor C_o is almost the same in both topologies (11.4 and 10 mF, respectively). In the case of 600-V regulated output, the capacitor energy storage ability must be chosen $0.5 \cdot C_o V_o^2$ (= 2052 and 1800 J, respectively).

Based on simulation results, the total power loss (conduction and switching) in power semiconductor devices are compared for the two topologies assuming full load condition and 3-kV input (see Table IX). The conduction losses of the devices

TABLE IX
LOSSES IN POWER SEMICONDUCTOR DEVICES AT RATED INPUT VOLTAGE AND FULL LOAD CONDITION

	Power devices	Losses [W]	Total loss [W]
Topology #1	S_+, S_-	2× 166.3	1159.7
	S_a	134.3	
	$D_1 \sim D_4$	4× 173.2	
Topology #2	S_{e+}, S_{e-}	2× 887.8	3337.6
	D_{e+}, D_{e-}	2× 51.8	
	S_+, S_-	2× 142.8	
	$D_1 \sim D_4$	8× 146.6	

(diodes and IGBTs) are calculated from their average and rms currents given the well-known formula

$$P_{\rm on} = V_{\rm th} \cdot I_{\rm ave} + r \cdot I_{\rm rms}^2 \tag{17}$$

where $V_{\rm th}$ represents the threshold voltage and r the on-state resistance taken from the manufacturers data sheets (corresponding to the power devices listed in Table VII). In a first approach, it is assumed that the switching losses under soft commutation and the diodes turn-off recovery losses may be ignored compared to the switching losses due to the hard-switched step-up module in topology #2. Following this idea, the switching losses are calculated for the sole switches, S_{e+} and S_{e-}, by using the following expression:

$$P_{\rm sw} = f_s \cdot (E_{\text{turn-on}} + E_{\text{turn-off}})_{T_j, I_C, V_{CE}} \tag{18}$$

where $E_{\text{turn-on}}$ and $E_{\text{turn-off}}$ are the energies dissipated during the transitions at given junction temperature T_j, on-state collector current I_C, and blocking voltage V_{CE}.

Simulations on both topologies have been carried on also changing the values of the resonant capacitor C_a (or $C = C_+ = C_-$ in topology #2) and leakage inductance L_k. We considered a $\pm 5\%$ tolerance on the resonant capacitor and $\pm 20\%$ tolerance on L_k, in accordance with the typical variations related to the manufacturing process. In every case, the simulation waveforms remained similar to those obtained with the reference values and the primary switches, S_+ and S_-, achieved ZCS (introducing some short time delay $T_{\rm delay}$ for the switches being turned off as explained in the previous sections).

The proper operation of the converters in the whole range of the dc input voltage (i.e., between 2∼4 kV) is another important requirement. In the second topology, the transformer turns ratio was selected to be 0.28 at 600-V output, assuming 4-kV input and $D_e = D_{e,\min}\ (= 0.1)$. For other values of the input voltage (in the range 2∼4 kV), the duty cycle D_e is normally adjusted by the action of a control loop to maintain $V_o\ (= 600\ \text{V})$. Hence, the simulations have shown that the voltage across the leg of the resonant capacitors (C_+, C_-) is about 4.4 kV. This result can be verified theoretically from the voltage transfer function of the input step-up converter. Indeed, assuming, e.g., $V_d = 3$ kV, the duty cycle is brought to 0.318 by the control loop (just as in Fig. 11), which results in the average voltage

$$\frac{1}{1 - 0.318} \times 3000 = 4.4\ \text{kV}$$

across the capacitors leg. For reliability reasons (thermal cycling capability), such a value cannot be accepted using 6.5-kV IGBT modules for the design of the switches S_+ and S_-. Therefore, in practice, the transformer turns ratio m should be selected a higher value (>0.28) in order that the average voltage across the capacitors leg does not exceed 3.6 kV (which is the rated dc voltage for reliable operation using 6.5-kV IGBT modules). Unfortunately, the dc-dc converter will not be able then to supply 600-V output when $V_d > 3.6$ kV due to the step-up operation of its input stage. Thus, from the above reasoning, it can be concluded that topology #2 cannot operate correctly in the whole range of the dc input voltage. On the other hand, this drawback does not relate to the first studied topology which, therefore, should be preferred with respect to the previously discussed criterion.

An asset of topology #2 is that it is inherently able to operate correctly from no load to the maximum load of the power supply, provided the duty cycle of the input step-up converter is reduced below $D_{e,\min}$. On the contrary, in topology #1, it is necessary to adapt the control scheme at light loads in order to supply 600-V output. A solution has been presented that consists in making the auxiliary circuit inoperative. Hence, the primary switches achieve hard-switched transitions; however, the corresponding switching power loss is reduced since the involved currents are small.

VI. CONCLUSION

This paper has investigated two topologies of soft-switched isolated dc-dc converters for auxiliary railway supply. First, the operating principles and the design considerations have been presented in detail. Then, computer simulations have been conducted in accordance with the requirements of the specific railway application in order to verify the theoretical analysis. The steady-state output voltage characteristics at 3-kV input have been discussed for the two topologies, highlighting specific operating conditions such as incomplete-discharge mode or discontinuous conduction. As an important requirement, the ability to supply 600-V output at light loads has also been studied from these characteristics and it was shown that both converters could meet this objective, on the condition to accept hard-switching. Finally, a comparative analysis of the two candidate topologies has been carried out, the main outcomes are as follows: 1) the global power rating of the semiconductor devices is higher for the second topology; 2) on another hand, the overall weight and size reduction of the passive components is rather in favour of the topology #2, even though less material is expected for the other topology as regards the transformer; 3) at rated conditions, the total power loss of the power semiconductor devices is significantly less for topology #1 (no hard-switching); 4) if the values of the resonant elements are changed within a prescribed tolerance, the two converters are still able to achieve ZCS; 5) the second topology cannot operate above 3.6 kV dc input voltage using 6.5 kV IGBT modules; and 6) however, contrary to the topology #1, it is able to operate correctly in the whole range of the output power, even at no load, without the need to adapt the control technique, which is an advantage.

APPENDIX A

The steady-state output voltage equation of the first dc-dc converter topology [see (5)] can be derived as follows.

The secondary rectifier voltage $v_{\rm rec}$, which is defined in Fig. 3, is a repetitive waveform at the fundamental period $T_s/2$. From the theoretical analysis conducted in Section II, we have

$$v_{\rm rec}(t)=\begin{cases} v_2(t), & \text{for } t_0\le t<t_1\\ v_C(t), & \text{for } t_1\le t<t_4\\ 0, & \text{for } t_4\le t<T_s/2. \end{cases} \tag{A1}$$

Since the average value of the voltage across the filter inductor L_o is zero, the average value of $v_{\rm rec}$ is equal to the dc output voltage

$$\begin{aligned} V_o&=\frac{2}{T_s}\int_{t_0}^{t_0+T_s/2} v_{\rm rec}(t)dt\\ &=\frac{2}{T_s}\cdot\left[\frac{mV_d}{2}D_{\rm aux}T_s+\frac{mV_d}{2}\left(\Delta t_{1\sim3}-\frac{\sin(\omega_0\Delta t_{1\sim3})}{\omega_0}\right)\right.\\ &\qquad\left.+v_C(t_3)\cdot\Delta t_{3\sim4}-\frac{1}{2}\frac{I_o}{C_a}(\Delta t_{3\sim4})^2\right]. \end{aligned} \tag{A2}$$

Then, the time durations $\Delta t_{1\sim3}\ (=t_3-t_1)$ and $\Delta t_{3\sim4}$, and the capacitor voltage $v_C(t_3)$ should be determined.

Referring to Fig. 5, $\Delta t_{1\sim3}$ can be obtained by noting that the primary current (reflected in the secondary side) decreases to zero at time t_3. So, we have

$$\frac{mV_d}{2Z_0}\sin(\omega_0\Delta t_{1\sim3})=-I_o \tag{A3}$$

and rearrangement of this expression yields

$$\Delta t_{1\sim3}=\frac{1}{\omega_0}\left[\arcsin\left(\frac{2Z_0I_o}{mV_d}\right)+\pi\right]=\frac{\alpha+\pi}{\omega_0}. \tag{A4}$$

Hence, using (1), the voltage $v(t_3)$ across the resonant capacitor is expressed as

$$\begin{aligned} v_C(t_3)&=\frac{mV_d}{2}\cdot[1-\cos(\omega_0\Delta t_{1\sim3})]\\ &=\frac{mV_d}{2}\cdot(1+\cos\alpha). \end{aligned} \tag{A5}$$

Since the resonant capacitor C_a is discharged linearly during the time interval $[t_3\sim t_4]$ (i.e., during mode 4) and the voltage reduces to zero at time t_4, it can also be written

$$v_C(t_3)=\frac{I_o}{C_a}\Delta t_{3\sim4}. \tag{A6}$$

Thus, combining (A5) and (A6), the time duration $\Delta t_{3\sim4}$ is given by

$$\Delta t_{3\sim4}=\frac{C_a}{I_o}\cdot\frac{mV_d}{2}\cdot(1+\cos\alpha). \tag{A7}$$

Finally, substituting (A4), (A5), and (A7) into (A2) leads to

$$\begin{aligned} V_o=\frac{2}{T_s}\frac{mV_d}{2}\cdot\left[D_{\rm aux}T_s+\frac{1}{\omega_0}(\alpha+\pi+\sin\alpha)\right.\\ \left.+\frac{1}{2}\frac{mV_d}{2}\frac{C_a}{I_o}\cdot(1+\cos\alpha)^2\right] \end{aligned} \tag{A8}$$

and the corresponding normalized equation can be derived dividing both sides by the base voltage [defined by (3)].

Equation (6) is derived, as for it, by expressing that the voltage across the resonant capacitor C_a exactly decreases to zero at the end of a half-cycle (i.e., at $t_4=t_0+T_s/2$)

$$v_C(t_3)-\frac{I_{o,\min}}{C_a}\left[\left(t_0+\frac{T_s}{2}\right)-t_3\right]=0. \tag{A9}$$

Hence, using (A4) and (A5), the minimum output current can be stated as

$$\begin{aligned} I_{o,\min}&=\frac{C_a\cdot v_C(t_3)}{\frac{T_s}{2}-\Delta t_{0\sim1}-\Delta t_{1\sim3}}\\ &=\frac{mV_d}{2Z_0}\cdot\frac{1}{\omega_0}\cdot\frac{1+\cos\alpha_{\min}}{\frac{T_s}{2}-D_{\rm aux}T_s-\frac{\alpha_{\min}+\pi}{\omega_0}} \end{aligned} \tag{A10}$$

and the corresponding normalized expression is obtained dividing each side by the base current [given by (4)].

APPENDIX B

The steady-state output voltage relationship for the second dc-dc converter topology [see (10)] can be derived by noting that the average value of the current flowing through the filter capacitor C_o is zero. Therefore, the average value of the rectified secondary current is equal to the dc output current I_o, which is expressed as

$$\begin{aligned} I_o&=\frac{1}{T_s}\int_{t_0}^{t_0+T_s}|i_2(t)|\,dt\\ &=\frac{2}{T_s}\int_{t_0}^{t_1}\frac{V_{\max}-V_o/m}{mZ_0}\sin\left(\omega_0(t-t_0)\right)\cdot dt\\ &=\frac{2k}{\pi}\cdot\frac{V_{\max}-V_o/m}{mZ_0} \end{aligned} \tag{B1}$$

where the maximum voltage $V_{\max}\ (=v_{C-}(t_0))$ across one of the resonant capacitors (say, e.g., C_-) is to be determined.

For that purpose, the following set of simultaneous equations should be solved:

$$\begin{cases} V_{\min}+V_{\max}=\frac{2V_o}{m}\\ (D_e+1-k)V_{\min}+(1-D_e)V_{\max}=\frac{V_d}{1-D_e}-k\frac{V_o}{m} \end{cases} \tag{B2}$$

where the first relationship between $V_{\max}$ and $V_{\min}$ is simply given by (8), which is expressed at time t_1 [note that $V_{\min}=v_{C-}(t_1)$], and the second one is derived from the dc-to-dc voltage transfer function of the input step-up converter

$$\frac{\frac{1}{T_s}\int_{t_0}^{t_0+T_s}\left(v_{C+}(t)+v_{C-}(t)\right)dt}{V_d}=\frac{1}{1-D_e} \tag{B3}$$

noting that, in steady-state operation, the average values of the voltages across each resonant capacitor are the same.

The solution of (B2) gives

$$V_{\max}=\frac{V_o\cdot(1+D_e-k/2)-\frac{mV_d}{2}\frac{1}{(1-D_e)}}{m\cdot(D_e-k/2)} \tag{B4}$$

$$V_{\min}=\frac{-V_o\cdot(1-D_e+k/2)+\frac{mV_d}{2}\frac{1}{(1-D_e)}}{m\cdot(D_e-k/2)}. \tag{B5}$$

Hence, substituting (B4) into (B1) yields the following equation:

$$V_o = \frac{mV_d}{2} \cdot \frac{1}{1 - D_e} + m^2\pi \cdot \frac{D_e - k/2}{2k} \cdot Z_0 I_o \qquad \text{(B6)}$$

which can be normalized dividing each side by the base voltage.

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