Zero Voltage Soft-Switching Phase-Shift PWM Controlled Three-Level DC-DC Converter for Railway Auxiliary Electric Power Unit

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***Abstract*—This paper presents a new type of soft switching dc-dc converter with high frequency(HF)-link for auxiliary power unit (APU) of railway applications. The proposed topology features a single-stage power conversion process with dc voltage regulation by a diode-clamped three-level dc-dc converter. A time-domain analysis on the high-frequency transformer current is presented in terms of zero voltage soft switching (ZVS) in all the active switches. Performances of the proposed APU is demonstrated by a $2-\mathrm{kW}$ miniature prototype under the control principle of zero voltage soft-switching (ZVS) phase shift pulse-width-modulation (PS-PWM), after which the feasibility is discussed from a practical point of view.**

I. Introduction

Low emission of carbon dioxide is a critical issue in the filed of transportation amid the wide-spreading activities toward realization of green power society and community all over the world.

The APU is essential for converting the high voltage from a third rail or a catenary of bus line to the low voltage[1]-[3]. Its capacity reaches $100\,\mathrm{kVA}$ class, accordingly galvanic isolation is demanded for ensuring the safety. The low frequency transformer-link circuit topology of APU is a typical architecture in the Japanese domestic railways as depicted in Fig. 1[4].

To reduce the size and weight of APU, a high-frequency transformer-link dc-dc power converter is the best solution with minimizing a switching power loss by introducing a soft switching technology. The existing two-stage topology-based APU is drawn in Fig. 2. The buck converter and series-resonant half-bridge converter brings about efficiency degradation due to a large amount of switching power devices and components under the light load condition. As a new solution for efficiency improvement, the diode-clamped ZVS-PWM three-level dc-dc converter (TL-DDC) is newly developed for APU in this research subject. The fundamental theory and operating principle was introduced in the literature [5], and several topologies of TL-DDCs have been developing for a wide variety of electric power systems such as a microgrid system of an offshore wind power generation[6] and an arc welding machine[7].

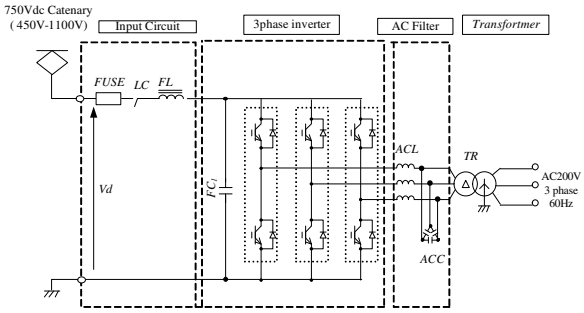

Fig. 1. Conventional low frequency transformer-link APU.

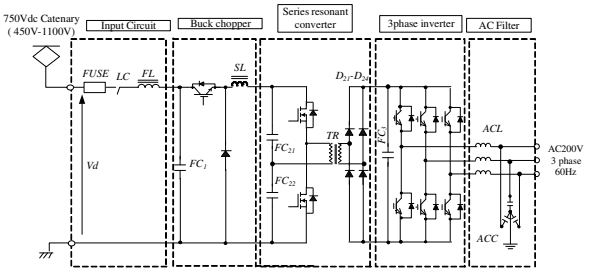

Fig. 2. High frequency transformer-link two-stage APU.

Adoption of TL-DDCs can be justified with the technical trend of increasing the dc-bus voltage, say $800\,\mathrm{Vdc}$ in the railway electric power system in terms of high power density and a low voltage stress of power device.

The rest of this paper is organized as follows: the circuit topology and operating principle are described in Section II. The essential performances of the ZVS-PWM TL-DDC are investigated by experiment, thereby the practical effectiveness as an APU is verified from the practical point of view.

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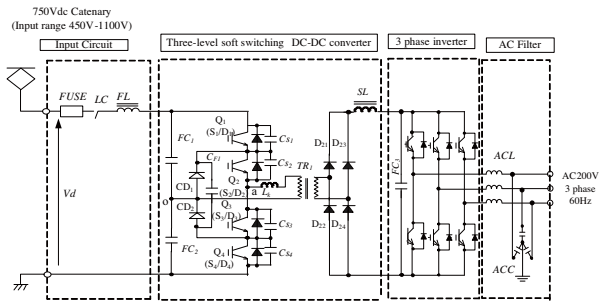

Fig. 3. Proposed high frequency-link APU based on a ZVS-PWM controlled TL-DDC.

II. ZVS-PWM THREE-LEVEL DC-DC CONVERTER WITH HF-LINK

A. Circuit Topology and Control

The circuit diagram of the proposed APU is presented in Fig. 3. The three-phase inverter, ac line filter and load are replaced by a resistor R_o for simplifying the circuit diagram. The dc-dc conversion part consists of a neutral-clamped three-level inverter while a lying capacitor C_{F1} is added for ensuring ZVS commutation in the outer switches Q_1 and Q_4. The lossless snubber capacitors C_{s1}-C_{s4} are additionally connected in parallel with Q_1–Q_4 respectively in order to achieve ZVS operations.

The output power is controlled by PS-PWM under the condition of constant switching frequency. The zero-voltage and zero-current soft switching (ZVZCS) TL-DDCs have been proposed with assist of auxiliary passive components[8][9] featuring reduction of circulating current due to PS-PWM. For the sake of simplicity, reliability, and cost effectiveness, the conventional ZVS-PWM TL-DDC is adopted in the proposed APU.

B. Switching Mode Transitions and ZVS Conditions

The switching one cycle of the TL-DDC is comprised of the twelve modes. Only the positive half period is indicated for simplicity in Fig. 4, and the corresponding waveforms are presented in Fig. 5.

- [Mode 1 ($0 \le t < t_1$): power delivering flow in positive direction] The active switches Q_1, Q_2 are on-state, and the current from the divided dc voltage $V_d\,/\,2$ flows through the network S_1-S_2-TR_1. During this interval, the magnetizing energy is stored in the leakage inductance L_k of TR_1. In this interval, the HF transformer current i_k is expressed by

$$i_k(t) = \Big[\big(\frac{V_d}{2} - aV_o\big)/L_k\Big]t + i_k(0), \tag{1}$$

  where $a\,(= w1/w2)$ represents the transformer windings turns ratio.

- [Mode 2 ($t_1 \le t < t_2$): ZVS commutation in outer switches] The active switch Q_1 is turned off, then the lossless snubber capacitors C_{s1}, C_{s4} and leakage inductance L_k make the resonance. Thereby, the voltage v_{Q1} rises with a slope from zero, and the ZVS turn-off commutation starts in Q_1. At the same time, C_{s4} discharges through C_{F1}-Q_2 and the voltage v_{Q4} declines from $V_d\,/\,2$. After that, the anti-parallel diode D_4 of Q_4 is forward biased. During this interval, gate-on signal is supplied to Q_2, whereby the ZVZCS turn-on attains in Q_2. In this interval, the HF transformer current i_k is expressed by

$$i_k(t) = \Big[\big(\frac{V_d}{2} - aV_o - v_{s1}\big)/L_k\Big](t - t_1) + i_k(t_1) \tag{2}$$

$$v_{s2}(t) = \frac{1}{C_{s1}}\int_{t_1}^{t} i_{14,off}\,d\lambda \tag{3}$$

  where $i_{14,off}$ represents the turn-off currents of outer switches.

- [Mode 3 ($t_2 \le t < t_3$): circulating current] The voltage v_{Q1} reaches $V_d\,/\,2$ at $t = t_2$, whereby ZVS turn-off commutation completes. The high frequency current circulates through S_2-TR_1-CD_1 while the power is fed to the load R_o through D_{21}, D_{24} and SL in the secondary side. In this interval, the HF transformer current i_k is expressed by

$$i_k(t) = \frac{-aV_o}{L_k}(t - t_2) + i_k(t_2)mbox. \tag{4}$$

- Mode 4 ($t_3 \le t < t_4$): ZVS commutation in the inner switches] The gate-on signal is removed from Q_2 at $t = t_3$, then the lossless snubber capacitors C_{S2}, C_{S3} and the leakage inductance L_k create the edge resonance. In this interval, the HF transformer current i_k is expressed by

$$i_k(t) = \frac{-v_{s2}}{L_k}\big(t - t_3\big) + i_k(t_3) \tag{5}$$

$$v_{s2}(t) = \frac{1}{C_{s2}}\int_{t_3}^{t} i_{23,off}\,d\lambda, \tag{6}$$

  where $i_{23,off}$ represents the turn-off currents of inner switches.

- [Mode 5 ($t_4 \le t < t_5$): power-back flow] The voltage v_{Q2} reaches $V_d/2$, thereby ZVS turn-off is completed in Q_2. At the same time, the voltage v_{Q3} declines to zero level, then the anti-parallel diode D_3 of Q_3 is forward biased. During this interval, the gate-on signal is supplied to Q_3, whereby ZVZCS operation is attained in Q_3. In this interval, the HF transformer current i_k is expressed by

$$i_k(t) = -\frac{V_d}{2K_k}(t - t_4) + ik(t_4). \tag{7}$$

- [Mode 6 ($t_5 \le t < t_6$): power delivering in negative direction] The conduction current in Q_3 commutates naturally from D_3 to S_3 due to the inductive load condition of TL-DDC. The primary-side current i_k changes its

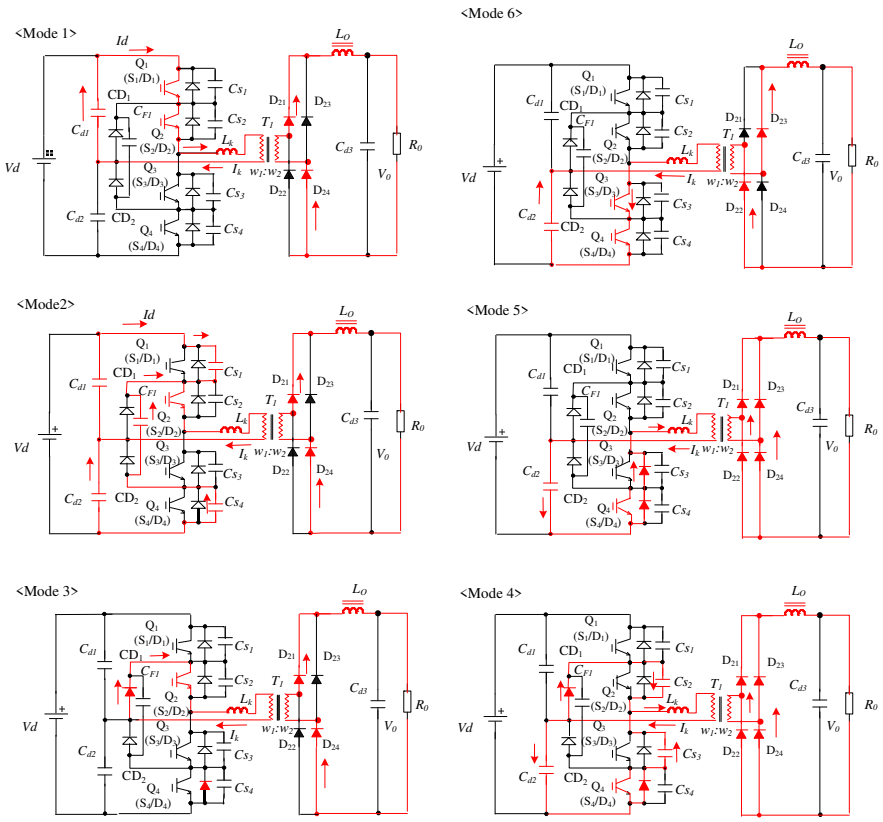

Fig. 4. Mode transitions and equivalent circuits during the half interval of a switching period.

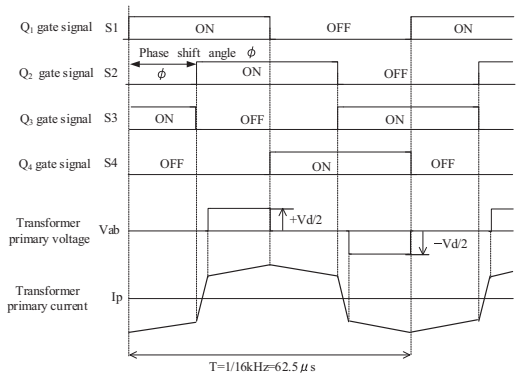

Fig. 5. Key waveforms of TL-DDC during the half interval of a switching period.

polarity at $t = t_5$, and the leakage inductance L_k stores the energy. The next cycle of circuit operation starts and the circuit operation gets into the negative half cycle. In this interval, the HF transformer current i_k is expressed by

$$i_k(t) = \left[\left(\frac{-V_d}{2} + aV_o\right)/L_k\right](t - t_5) + i_k(t_5). \quad (8)$$

The voltage conversion ratio $M = V_o / V_d$ can be defined approximately by assuming the time integral of L_k is zero as

$$M = \frac{V_d}{a}\left(\frac{T_s}{2} - \frac{\alpha}{360}\right), \quad (9)$$

where α denotes the phase shift angle in degree. Thus, ability of the step-down voltage regulation is mathematically indicated in the proposed APU.

The soft switching conditions are expressed by the inductive and capacitive energy balance among the leakage inductance L_k and the lossless snubber capacitors of outer and inner switches as expressed by:

i) outer switches Q_1 / Q_4

$$\frac{1}{2}L_k i_{14,off}^2 > C_{s1}\left(\frac{V_d}{2}\right)^2, \quad C_{s1} = C_{s4} \quad (10)$$

ii) inner switches Q_2 / Q_3

$$\frac{1}{2}L_k i_{23,off}^2 > C_{s2}\left(\frac{V_d}{2}\right)^2, \quad C_{s2} = C_{s3}. \quad (11)$$

III. Simulation Analysis

The simulation waveforms of HF transformer are indicated in Fig. 6. The power delivering and current circulating intervals appear in the resultant waveforms, as described in the Section II. The switching waveforms of the fixed switch Q_1 and controlled switch Q_2 are shown in Figs. 7 and 8, respectively. It can be confirmed from each waveforms that ZVS operations achieve in both the fixed and controlled phase switches. The

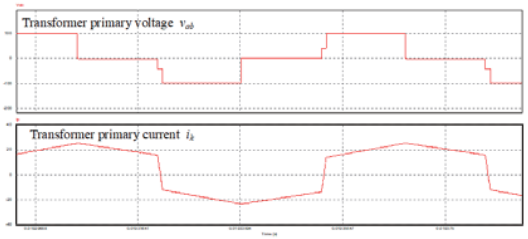

Fig. 6. Simulation waveforms of HF transformer.

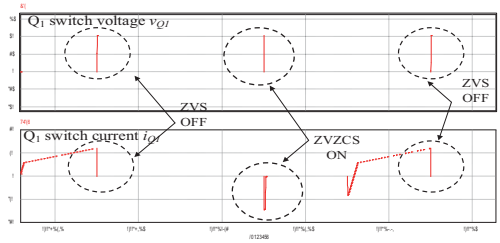

Fig. 7. Simulation waveforms of active switch Q_1.

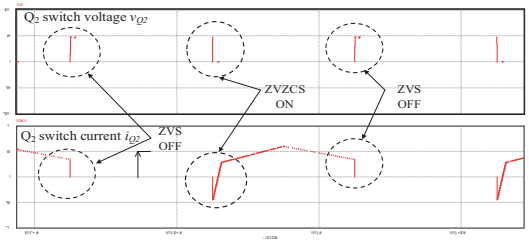

Fig. 8. Simulation waveforms of active switch Q_2.

discontinuous current emerges in Q_1, which is concerned with the phase shift angle and load resistor.

IV. Experimental Results

The performances of the TL-DDC is verified by experiment of a 2 kW prototype. The schematic diagram of the experimental setup is illustrated in Fig. 9. The exterior appearance of the prototype is shown in Fig. 10. The specification and circuit parameters of the prototype are summarized in TABLE. I. The switching frequency is selected as 16 kHz in consideration for the actual APU of the domestic railway facility. The gate signals are generated by the PS-PWM control IC (UCC3895) under the condition of a constant frequency and open loop control.

The key operating waveforms of the prototype are displayed in Fig. 11. The ZVS commutations with PS-PWM can be observed from the waveforms, accordingly the essential switching operations are verified herein. The circulation current may cause the power loss in the primary side of HF transformer. In order to reduce the circulation current, an auxiliary circuit can be adopted in the rear end of rectifiers as mentioned above.

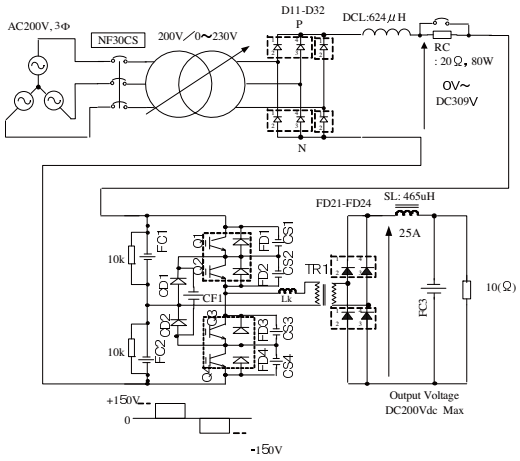

Fig. 9. Circuit digram of experimental systems.

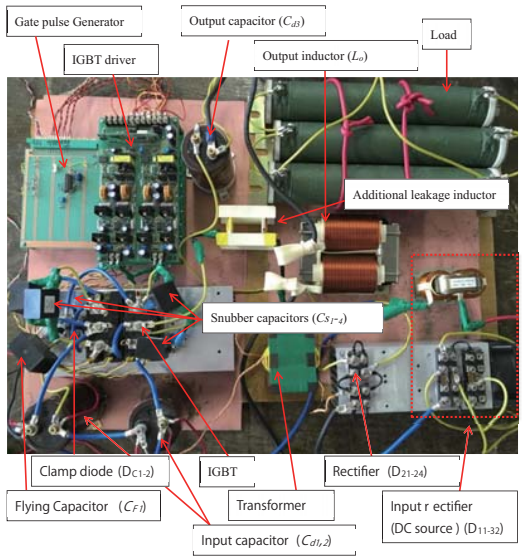

Fig. 10. Exterior appearance of prototype.

The Lissajous figures of voltage and current for the switching transitions of the inner Q_1 and outer Q_2 are illustrated in Fig. 12, which indicates trajectories along with the axes. Thereby, achievement of sot switching is clearly confirmed from the traces.

The characteristics of output voltage regulation are indicated in Fig. 13 with a parameter variation of load resistor R_o. It can be observed that the load voltage can be controlled by changing the phase angle ϕ. Accordingly, the single-stage step-down voltage conversion of TL-DDC is verified for the proposed APU.

The measured characteristics of output power versus phase shift angle are presented in Fi. 14, where a wide range of power regulation is proven. In this curve, ZVS of all the switches can be observed in the power range of 390 W–2 kW. The

TABLE I
CIRCUIT PARAMETERS AND CONDITIONS

Item	Symbol	Value [unit]
Input dc voltage	V_d	200 V
DC output voltage	V_o	100 V
Output power rating	P_o	500 W
Switching frequency	f_s	200 kHz
Smoothing capacitors	C_{d1},C_{d2}	1000 μF
Series resonant capacitors	C_{r1},C_{r2}	440 nF
Series resonant inductors	L_{r1},L_{r2}	40 μF
HF-T magnetizing inductance	L_m	500 μF
Snubbing capacitors in IGBTs	C_{s1}-C_{s8}	[1 nF
Resonant frequency	f_r	40 kHz
Transformer turns ratio	$a = w_1/w_2$	6 / 12
$Q_1 - Q_4$: IGBT(CM100DU-24NFH, 1200 V, 100 A)		
C_{D1}, C_{D2} (DSEI 2x31-10B, 1000 V, 30 A, IXYS)		
D_{21}, D_{24} (DSEI 2x31-10B, 1000 V, 30 A, IXYS)		
Phase-shift PWM controller: UCC3895		

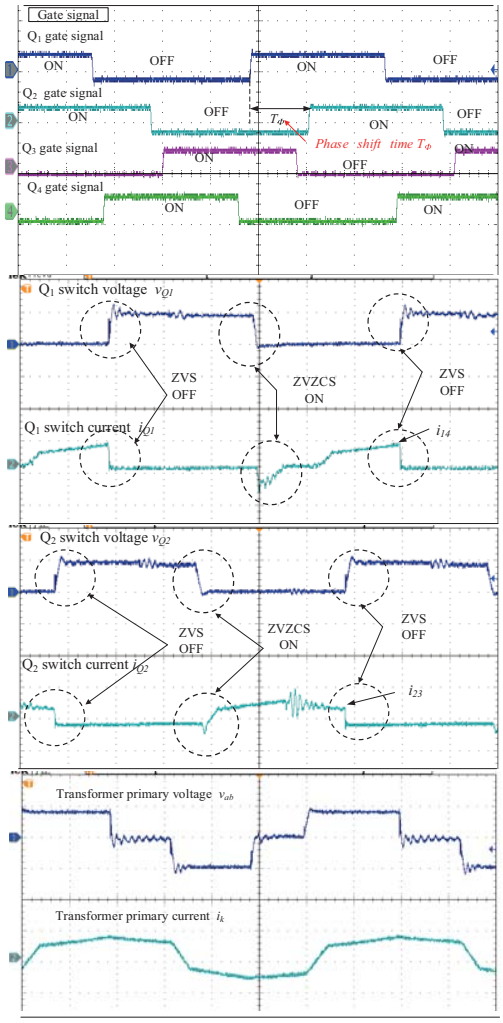

Fig. 11. Observed waveforms of prototype.

actual efficiency curve of the prototype is displayed in Fig. 15.

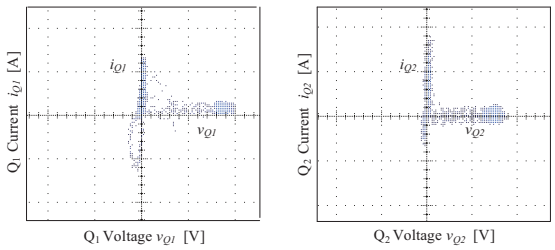

Fig. 12. Lissajous figures of switching operations at $V_d = 100$ V, $P_o = 250$ W (25 V/div,10 A/div)

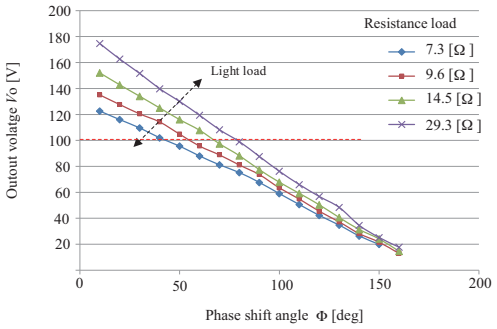

Fig. 13. Measured output voltage characteristics by PS-PWM the open loop control.

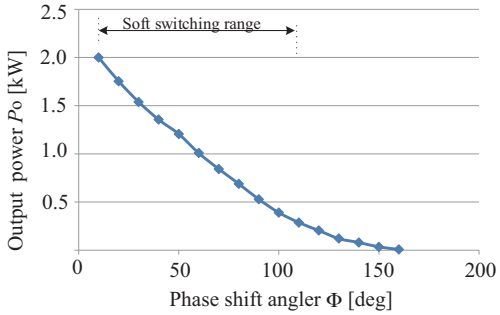

Fig. 14. Measured steady-state curve of output power versus phase shift angle.

The maximum efficiency is recorded as 90.1 % at 2 kW. The dc input voltage is relatively low as compared to the voltage rating of IGBTs Q_1–Q_4, consequently the conduction losses of the power devices have greatly impact on the efficiency. In addition, the tail current of IGBT affects the switching loss reduction. The wide band gap power devices such as SiC-MOSFET is suitable for the TL-DDC in the proposed APU as a solution for improving the conversion efficiency.

V. CONCLUSION

The three-level dc-dc converter for an auxiliary power unit of railway application has been proposed in this paper. The zero voltage soft switching operations and phase shift-PWM power control have been described in a time domain analysis.

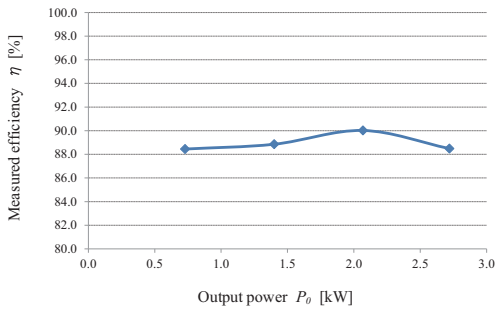

Fig. 15. Actual efficiency curve of prototype.

The practical performance of the dc-dc converter has been verified by experiment of the 2 kW-16 kHz prototype. The wide range of soft switching has been attained successfully for 20 % load to full load in the experiment, and the 10 %–90 % load voltage regulation has been demonstrated with PS-PWM scheme.

The future challenges of this research include; power loss analysis, efficiency improvement and comparison of performances with the existing two-stage APUs.

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