Design of FPGA based Frame Transceiver of MVBC *

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***Abstract*—A design of frame transceiver of Multifunction Vehicle Bus Controller (MVBC) utilized by FPGA is proposed in this paper.Firstly at all, on the basis of analyzing the MVB communication mechanisms and characteristics, the algorithm of the MVBC frame transceiver core functions has been described by the VHDL language, such as Manchester encoder and decoder (CODEC), Cyclic Redundancy Check (CRC) and so on. Then, the transmitter module and receiver module have been designed. At last, the transmitting and receiving of MVB master frame and slave frame have been realized on FPGA.**

Keywords—MVBC; FPGA; Manchester encoding and decoding; CRC

I. INTRODUCTION

The distributed control based MVB is a recommended program for IEC61375-1(1999) (Train Communication Network International Standard, TCN). The train communication bus including MVB and Wired Train Bus (WTB) has the characteristics of strong real-time and high reliability [1]. MVBC is a key component of realizing the MVB bus network functions, which is responsible for accessing the MVB bus, offering the communication interface with the microprocessor and realizing data transmission [2].

The MVBC frame transceiver is responsible for the data communication between the bus and the MVBC, which includes the codec module, CRC check module and the control module of the transmission reception. The dedicated chip MVBC is currently for achieving MVB transceiver. But with the development of the system-on-chip technology, modern electronic design tends to be high level of integration. Therefore most of similar interface chips have been alternated by the soft core of the ASIC (Application Specific Integrated Circuit) [3]. This design of MVB frame transceiver module based on VHDL will be as a soft-core of the the MVBC.

* Grant from the National Natural Science Foundation (No.61132003, 61171086, 51267005) of China, Shanghai Leading Academic Discipline Project (No.S30108), Youth Science Foundation of Jiang'xi Educational Committee (No.GJJ13322) and Foundation of East China Jiaotong University (No.10DQ07, NO.11DQ01).

II. MVBC

The processing of frame receiving and sending is completed by utilizing MVBC on the data link layer and relying to send and receive electrical signals with electrical characteristics on the physical layer.While the MVBC offers a variable interface of the process data and the message data on the network layer, whose interface utilizes the communication memory(TM). Fig. 1 is the block diagram of MVBC internal structure in this project, including the Manchester encoding and decoding module, the transmission/reception buffer configuration register, the TM and the main control unit (MCU).

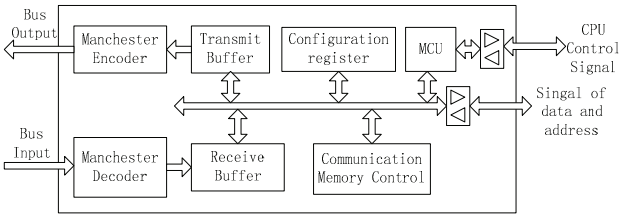

Figure 1. the Structure Diagram of MVBC

MVBC is connected with MVB via a dual redundant provided by the physical layer, and receives CPU access control in order to get and send device in MVB. At the same time, the management of MVB is completed by accessing the monitored data.

When the data is transmitted, MCU reads frame data from the TM and writes to the transmission buffer. Then, the data is readed out by the encoder to encode and check and then sent to the MVB bus. When the data is received, the decoder is responsible for completion of the decoding of the input frame;

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and verifying its validity, and then the data is stored in the corresponding communication memory, thereby which has been completed the process of receiving data. In addition, according to the configuration, the MVBC can achieve the master bus and the slave bus to bring about the data processing of the data link layer and the transport layer and interacte with the upper-layer software by communication memory.

III. FRAME TRANSCEIVER DESIGN

The frame transceiver of MVBC is mainly responsible for the transmitting and receiving of the frame, including Manchester encoding/decoding, CRC generation and checking, construction and identification of different types of frames, and the code wrong identification and conflict detection. Among those modules, Manchester encoding and decoding and the CRC check are the most important algorithms.

A. Manchester encoding / decoding

The Manchester encoding unit is responsbile for encoding the main frame data and the slave frame data, whose structure is shown in Figure 2 [9].

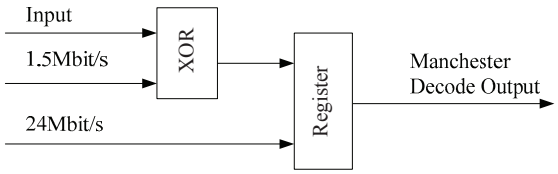

Figure 2. the Diagram of Manchester's Code

The data first combines the serial data and clk_l6div by utilzing XOR operator. The serial data is generated by the data serial-to-parallel conversion unit, CRC generating unit and the frame delimiter unit and the multiplexer. The clk_l6div is divided-by-16 clock of 1.5MHZ by utilzing XOR operator. Then the data passes a first-order register on the rising edge of the system clock of 24MHZ and then outputs the encoded data. Although it will be a clock cycle late than the serial input data after the above process, the output encoded data is ensured a stable output signal.

In Manchester coding [4-5], a hop changes in the middle of every bit, which is as both the clock signal and the data signal. From high to low jump indicates "1", from low to high transition represents "0". The code type has the advantages of rich timing information and no DC component, which is especially suitable for fast switching of multi-channel data. Figure 3 shows the Manchester encoding waveform using QuartusII.

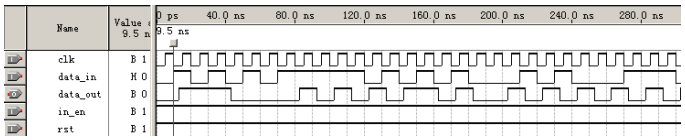

Figure 3. the Simulation Waveform of Manchester's Code

Due to the header, the end of the frame is not Manchester encoding, the traditional Manchester codec can not complete the work. The design method by combining with the specific state codec of the transceiver state machine will solve this problem [3].

For decoding module, the synchronous detection is the key. The decoding cycle will not start before the synchronization information has been detected. Manchester decoding is implemented with FPGA by the use of edge judgment: rising edge is 0, falling edge is 1.

As has been described, MVB link layer data is based on the frame as the basic unit. A data includes the frame header, data, and end of the frame. The frame is divided into the main frame and the slave frame. The frame header uses a different encoding, and the end of frame is the 0.75BT+125 ns low level. The data encoding is done using Manchester encoding. The decoder detectes line start bit to determine the correct header data and then converts the followed Manchester encoded data into its normal logic data, which will be sent to the control logic.

Manchester encoded input will eliminate the metastable state after three registers synchronization. If the falling edge arised on the bus after the idle state, it will be considered the start bit of the frame.The 16-bit counter will be enabled to counte when the high level arises on the bus. Manchester encoding in each bit cycle is divided into 16 parts. The sampling value obtained at sampling data 1 is the original data before Manchester encoding, and the sampling value obtained at sampling data 2 is used to test frame header and frame tail. The principle of the bus conflict detection is that with half a bit-cycle of Manchester encoding on the bus the level should be the same and the level of first half bit-cycle should be different from the level of the another half bit-cycle, otherwise it is considered wrong code.

B. Data check

In TCN agreement, the data needs to be checked by CRC check and even-odd check. In the international standard, according to the type of the generating polynomial g (x), CRC can be divided into several standards [3]. In this paper, the calculation formula of 7-bit CRC followes the provisions of the IEC 60870-5 format class FT2, which will be calculated according to the following generator polynomial: $g(x) = x^7 + x^6 + x^5 + x^2 + 1$. The data expression divided by generator polynomial makes CRC check code. CRC check is divided into two kinds of serial and parallel. Serial CRC check is simple but takes a long time. The algorithm complexity of parallel CRC check is high, which is only suitable for long bit check. As the frame length of the MVB data is constantly changing and the length of the frame data is short, the serial CRC check will be used in this paper.

The generation circuit of CRC check code uses a linear feedback shift register, which is the circuit of the universal serial CRC algorithm. As shown in Figure 4. Each of the D flip-flop saves a symbol data [5-6].

In Figure 4, the register is connected via an exclusive OR gate. The gate is used to control the input of the information code. When the door is opened, the information symbols input. When all of the information symbols have been finished entered, the door is closed and prohibits any symbols input, the

parity bit of the 7-bit symbols stored in the register 7 is obtained.

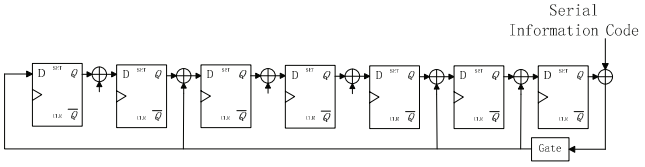

Figure 4. the Diagram of CRC

Secondly, 7 bit CRC will be checked by even parity. According to the principle of even parity, the parity bit a_0 is calculated as: $a_0 = a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7$, $a_1 - a_7$ is 7-bit CRC code. The a_0 follows the CRC code is to constitute 8-bit check sequence. Finally, the final check sequence is obtained by reversing all 8-bit check sequence.

C. The design and implementation of the bus interface module

The bus interface includes the transmission module and the reception module.

The sending module under the control of the main control unit is responsible for Manchester encoding of the main frame and the slave frame, packaging, generating the corresponding parity sequence and transmitting. Sending module includes the transmission control unit, the unit of frame delimiter, the parallel-serial conversion unit, CRC generation unit, the First-In First-out (FIFO) unit, the the multiplexer selector unit and the Manchester encoding unit. The realization of entire module is done through the state machine and its internal structure as shown in Figure 5 [9].

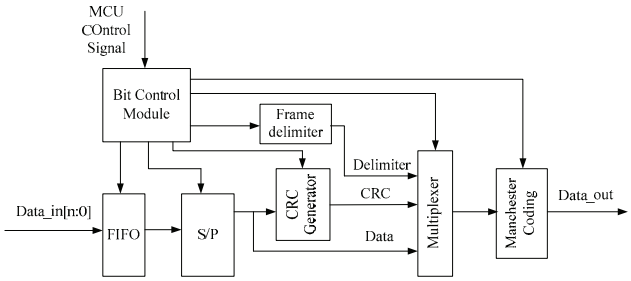

Figure 5. the Structure Chart of Send Module

In addition to the CRC generation unit and Manchester encoding unit, bit control module is the core of the entire send module. It will be the IDLE state when the system is reset or the previous one has been finished sending, and be waiting for transmitting enable signal. Then after the starting delimiter has been sent, the counter starts to counte and send module starts to send data. The word count the variable of word_counter add 1 every sending 16-bit data. The check sequence calculated by ckeck sequence generation unit is sent to the Manchester encoding unit. judgment should transmits a frame of words variable word_counter is the value for equality. It will access to the termination delimiter generate status if the number of the frame data to be sent equals the varialbe of word_counter, or continue to transmit data, until the data has been sent. This design uses a finite state machine to achieve a transmission control unit and the convertation between states is shown in Figure 6 [10].

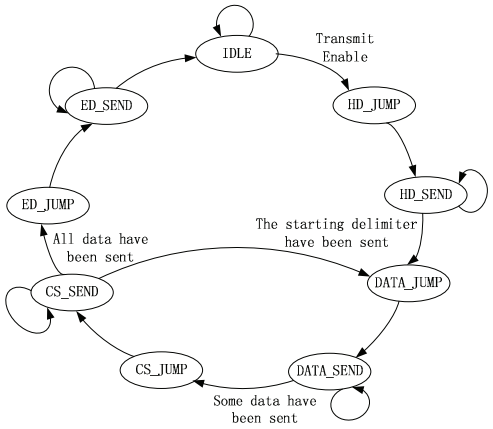

Figure 6. the State Transition Diagram of Encode Control Unit

The four states of HD_JUMP, DATA_JUMP, CS_JUMP and ED_JUMP indicate transitional states. IDLE state is idle waiting. HD_SEND, DATA_SEND, CS_SEND, ED_SEND identify send state of the start delimiter, data, CRC checksum and the end delimiter.

MVB bus uses redundant media, so the redundant MVBC receiver module is needed to complete reception of the frame. The functions of receiver module include the following: the determination completion of the frame data start bit, data sampling, data decoding and data shift function, determinant the type of frame data and extracting from the frame data stored in the receive buffer. The design circuit of the receiver module is shown in Figure 7.

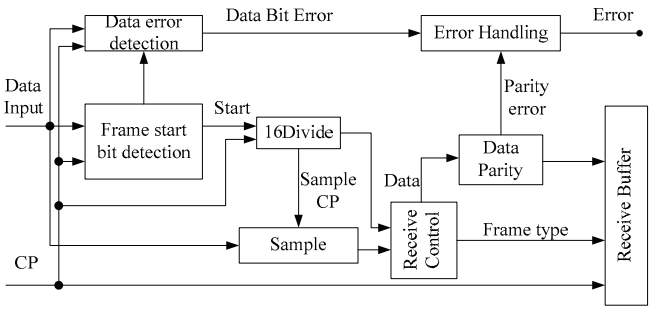

Figure 7. the Structure Chart of Receiver Module

The decoder receives the frame at the same time the decoder tells some information to the line control module, such as whether the frame has been received, what is frame type, whether reception has been completed, or the result is right or wrong. The module will report the above mentioned information and the reception buffer to the upper layer module for packets analysis. The control module verifys the properties of the frame from the reception state: the validity of the frame, the frame type, the frame length, and the correctness of the data by verified from the read-out data [9]. The reception control unit is the core of the receiving module, whose implementation

uses the finite state machine to complete the flow chart shown in Figure 8 [10].

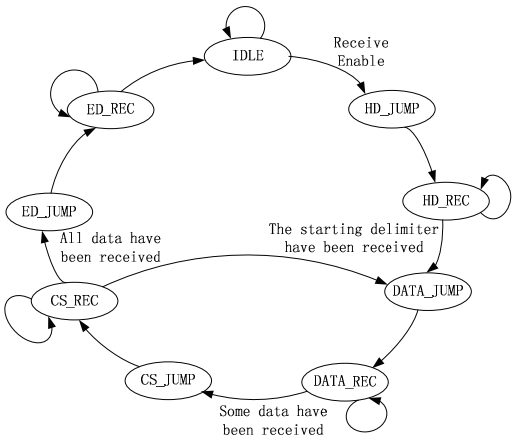

Figure 8. the State Transition Diagram of Decode Control Unit

HD_REC, DATA_REC, CS_REC, ED_REC identify the receiving state of start delimiter, data, parity bit, and end delimiter.

IV. BOARD-LEVEL TESTING

In the project two net-interfaces to be verified connecting to bus will be test, as shown in Figure 9. The results of the validation are mainly to see whether it has the ability to transmit packets, analyzes a variety of errors of the received data frame and then makes the appropriate treatment according to the error.

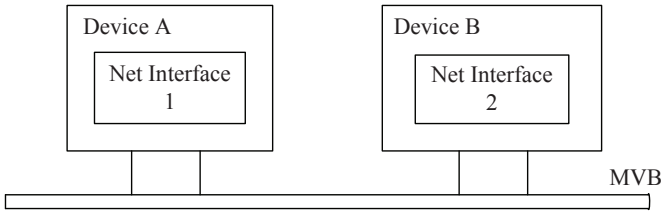

Figure 9. the Test Platform

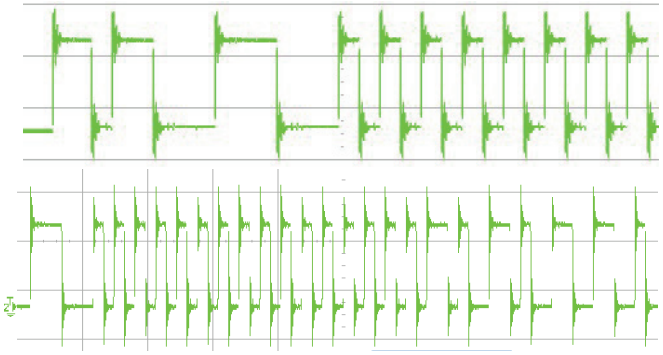

Figure 10. the Main Frame Waveform of MVB

Figure 10 is a waveform diagram of the main frame, which shows that the design correctly send data frames. Figure 11 shows the messages transmission results. The value of device A destination port 2 is 0x123, while the value of device B destination port 1 is 0x1234567. Thus, the network interface can correctly receive the data frame and store the data into the corresponding port.

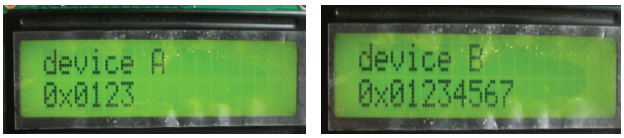

Figure 11. The result of packet transition

V. CONCLUSION

With the rapid development of Chinese high-speed railway, TCN has beening began to be applied in CRH. The train network control system network architecture of CRH5 is the use of TCN standard. The TCN network of widely use also gives a huge MVBC market prospects. This paper describes MVBC and the algorithm analysis, design and implementation of the frame transceiver of MVB interface. FPGA verification of each module has fully demonstrated the feasibility of the design.

ACKNOWLEDGMENT

This work is supported by Key Laboratory of Specialty Fiber Optics and Optical Access Networks, Shanghai University of Chin.

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