

# A 12-Level Series-Capacitor 48-1 V DC-DC Converter With On-Chip Switch and GaN Hybrid Power Conversion

Haixiao Cao<sup>ID</sup>, Xu Yang<sup>ID</sup>, Chenkang Xue, Lenian He, *Member, IEEE*, Zhichao Tan<sup>ID</sup>, *Senior Member, IEEE*, Menglian Zhao, Yong Ding<sup>ID</sup>, *Member, IEEE*, Wuhua Li<sup>ID</sup>, *Member, IEEE*, and Wanyuan Qu<sup>ID</sup>, *Member, IEEE*

**Abstract**—This work presents a 48-1 V dc-dc converter with an on-chip switch and gallium nitride (GaN) hybrid power conversion. By series connecting a 12-level Dickson switched-capacitor with a two-phase switched-inductor circuit, the capacitors take over most of the 48-V voltage stresses. The circuit, thus, reduces to an equivalent 4-1 V converter, making the on-chip 5-V transistor applicable for a 48-V high-voltage design. Due to the easy integration of on-chip switches and superior switch figures of merit over other 48-1 V counterparts, this proposed design is able to achieve the highest switching frequency, the lowest external switch count, and the improved power density compared with other prior-state-of-the-arts. The prototype was fabricated using a 0.18- $\mu\text{m}$  BCD process with an evaluation board volume of 17 mm × 15 mm × 2.6 mm. The converter achieves a maximum 8-A loading capacity with the input range from 36 to 60 V and the output from 0.5 to 1 V. The measured peak power efficiency is 90.2%, and the power density is 998 A/in<sup>3</sup> considering the power stage volume.

**Index Terms**—12-level, 48-1 V, dc-dc converter, gallium nitride (GaN), hybrid power conversion, on-chip switch, series capacitor.

## I. INTRODUCTION

WITH the rapid growth of artificial intelligence, devices are becoming more intelligent and power-hungry. High-efficiency and high-power-density dc-dc converters play a more important role in high-performance data centers. To reduce the distribution loss due to the power delivery network of data centers, the 48-V power bus has been proposed in place of the conventional 12-V bus. However, achieving good efficiency and power density has always been a nontrivial

Manuscript received April 20, 2021; revised July 14, 2021; accepted August 4, 2021. Date of publication August 24, 2021; date of current version November 24, 2021. This article was approved by Associate Editor Jason Stauth. This work is supported in part by the National Natural Science Foundation of China under Grant 61804133 and in part by Zhejiang Provincial Natural Science Foundation under Grant LZ20F040002. (*Corresponding author: Wanyuan Qu*.)

Haixiao Cao, Xu Yang, Chenkang Xue, Lenian He, Zhichao Tan, Menglian Zhao, Yong Ding, and Wanyuan Qu are with the School of Microelectronics, Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China (e-mail: caohx@zju.edu.cn; yangxucs@gmail.com; xueck@zju.edu.cn; helenian@zju.edu.cn; zhichaotan@zju.edu.cn; zhaoml@zju.edu.cn; dingy@vlsi.zju.edu.cn; wyqu@zju.edu.cn).

Wuhua Li is with the School of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (email: wuhualee@zju.edu.cn).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/JSSC.2021.3104328>.

Digital Object Identifier 10.1109/JSSC.2021.3104328

task, especially for the 48-1 V design, due to its high step-down ratio and large output current.

Several prior-state-of-the-arts have been proposed to address these challenges. For example, the Sigma converter combines an un-regulated *LLC* and a regulated Buck converter in parallel for good efficiency and power density since the high-efficiency *LLC* takes over most of the load current in typical conditions [1]. However, when the output voltage varies below 1 V, the power from the *LLC* path drops sharply and leads to severe efficiency degradations. Besides, the active-clamp forward converter [2] and the half-bridge with current doubler [3], [4] also make good tradeoffs between the efficiency and power density. Nevertheless, either a large turns ratio transformer or a multi-level primary stage is required to reduce the switching loss, which impedes further improvements. The switch tank converter employs full resonant operation to obtain a fixed-ratio power conversion [5], while a complete design requires a pre-/post-regulation stage, which limits the overall efficiency. In addition, the dual inductor hybrid converter also shows favorable efficiency [6], [7]. However, large numbers of switches and capacitors are needed, which hurts power density and increases costs.

A close inspection shows that, instead of directly converting a 48 V input to a 1-V output, most prior work reduces the equivalent input voltages either by large turns ratio transformers, by multi-level designs, or by hybrid architectures. Hence, the switching loss is reduced and performance enhanced. To disclose the detailed relationship between the efficiency and the input voltage of a typical step-down converter, a careful investigation is implemented (the Appendix).

Fig. 1(a) shows a typical step-down converter with its various power losses [8], which includes the conduction loss  $P_{\text{CON}}$ , the hard-switching overlap loss  $P_{\text{overlap}}$ , the output capacitance loss  $P_{\text{COSS}}$ , the driver loss  $P_G$ , the reverse recovery loss  $P_{\text{RR}}$ , the dead time reverse conduction loss  $P_d$ , and the passive component loss  $P_{\text{passive}}$ . To distinguish the losses related to the power switch from that to the input voltage  $V_{\text{IN}}$ , a switch quality determined loss  $P_{\text{FOM}}$  is defined as

$$P_{\text{FOM}} = P_{\text{CON}} + P_G + P_{\text{COSS}} + P_{\text{RR}} \quad (1)$$

which reflects the tradeoff between the switch conduction and switching losses. Higher switch quality reduces the

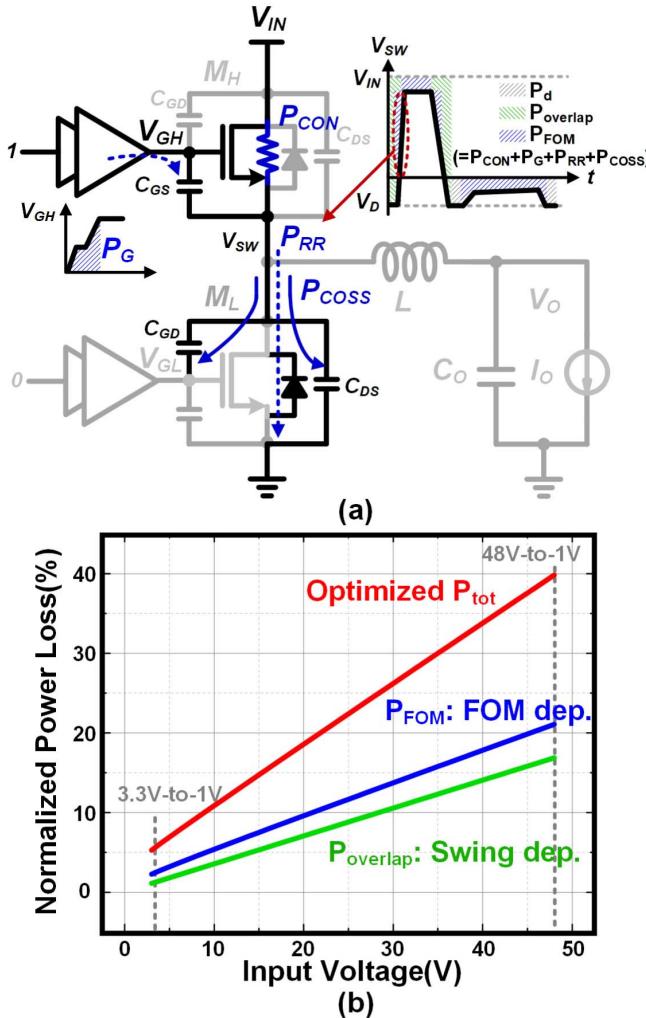


Fig. 1. (a) Typical step-down converter and (b) its normalized minimum power losses versus input voltages with  $I_{OUT} = 1$  A and  $f_{sw} = 1$  MHz.

overall losses. The hard-switching overlap loss  $P_{overlap}$  is defined as

$$P_{overlap} \approx V_{IN} \times (t_r + t_f) \times f_{sw} \times I_{OUT}/2 \quad (2)$$

where  $t_r$  and  $t_f$  are the transition times during the switch turn on and off periods, respectively.  $f_{sw}$ ,  $I_{OUT}$ , and  $V_{IN}$  are the switching frequency, the output current, and the input voltage, respectively.  $P_{overlap}$  shows a direct dependence on the input voltage level.

Fig. 1(b) depicts the optimized power losses of a step-down converter versus input voltages according to the optimization scheme in the Appendix. As is shown, although a 3.3-1 V converter easily achieves 95% peak efficiency, a 48-1 V design shows merely 60% optimum efficiency. A careful examination indicates that both  $P_{overlap}$  and  $P_{FOM}$  increase greatly as the input voltage rises. Equation (2) shows a clear dependence of  $P_{overlap}$  on  $V_{IN}$ , while that of  $P_{FOM}$  is indirect. To better appreciate the dependence of  $P_{FOM}$  on  $V_{IN}$ , Fig. 2 summarizes the figures of merit (FOM) of typical silicon and gallium nitride (GaN) power switches with different breakdown voltages. Here,  $FOM = Q_{OSS}R_{ON}$  is adopted, which is

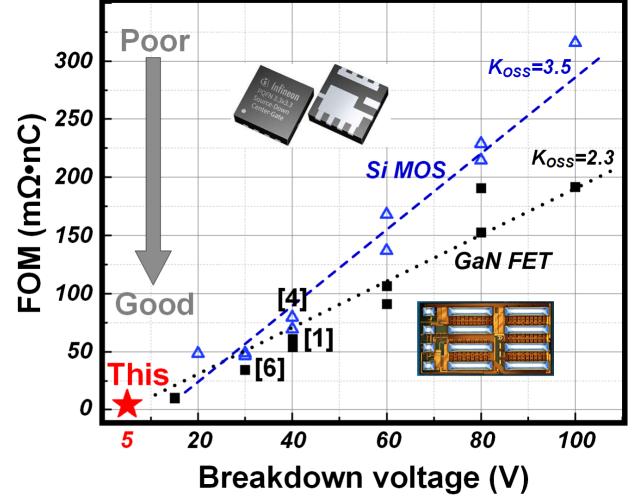


Fig. 2. FOM comparison for Si and GaN power devices under different breakdown voltages.

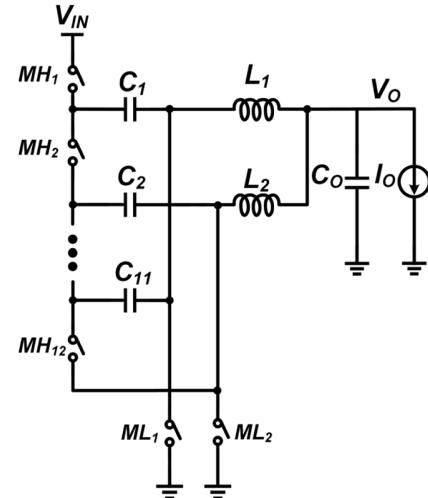


Fig. 3. Proposed 12-level series-capacitor buck converter.

suit for hard switching design. Fig. 2 clearly indicates that switch quality deteriorates as  $V_{IN}$  rises, leading to severe  $P_{FOM}$  degradations.

According to the above observations, the input voltage reduction is beneficial to both the hard-switching overlap loss  $P_{overlap}$  and the switch quality determined loss  $P_{FOM}$ . Therefore, an effort is exerted in this design to greatly reduce the equivalent input voltages for superior performances.

This work devises a 12-level series-capacitor dc-dc converter, which turns the 48-V input into 4-V equivalent inputs [9]. From Fig. 2, the switch FOM of a typical 5-V 0.18- $\mu$ m BCD process significantly outperforms that of the prior-state-of-the-arts. Besides, the 5-V transistors can be easily integrated. Therefore, this work achieves superior efficiency and power density with significantly reduced external switch count. This article is organized as follows. Section II describes the operation principle and analysis of the proposed converter. Section III presents the detailed

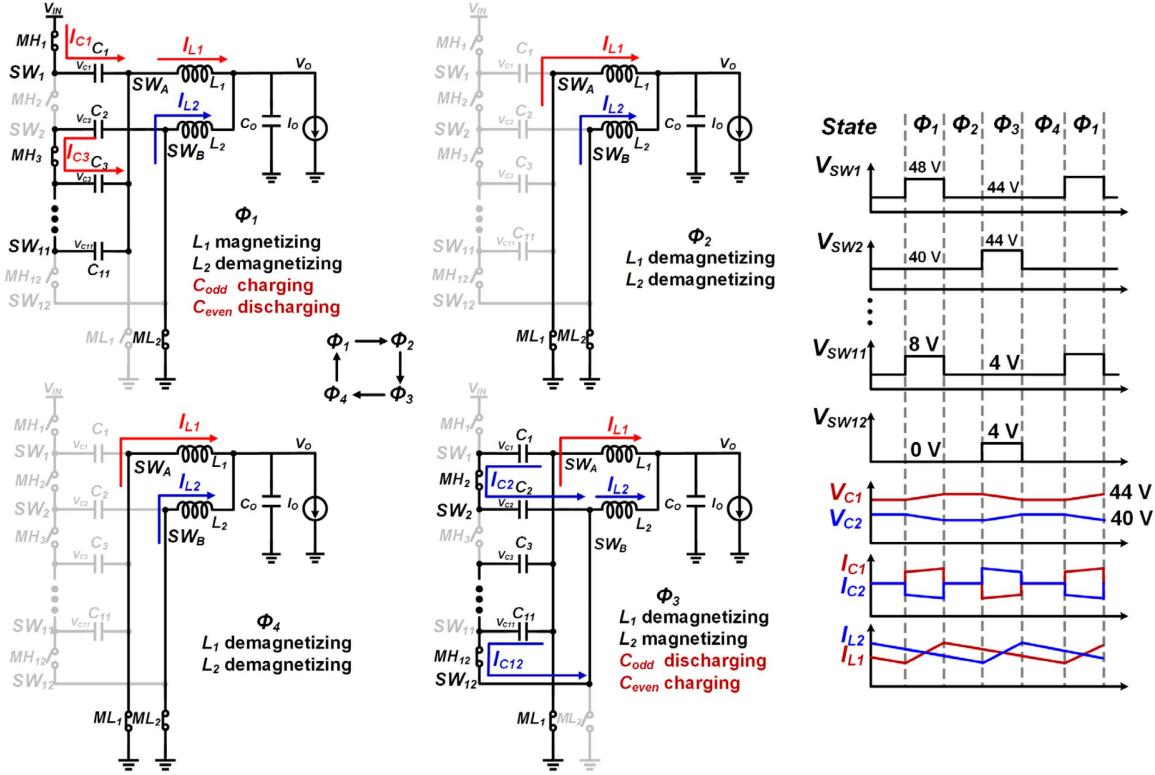


Fig. 4. Operation states and waveforms of the proposed converter.

circuit implementations. Section IV describes the measurement results. Finally, a conclusion is drawn in Section V.

## II. PROPOSED DC-DC CONVERTER

The series-capacitor buck converters [10]–[13], with capacitors in series with the inductors, demonstrate both multi-level and multi-phase switching properties. Besides, the duty cycle is extended, leading to simplified low-duty gate driver and controller designs. Inspired by this, this work proposes a 12-level series-capacitor dc–dc converter, as shown in Fig. 3. The converter consists of 12 series high-side switches  $MH_1$ – $MH_{12}$ , two low-side switches  $ML_1$ – $ML_2$ , eleven series capacitors  $C_1$ – $C_{11}$ , and two inductors  $L_1$  and  $L_2$ . The switches and the capacitors form a 12:1 Dickson step-down converter [14]. Therefore, the hybrid converter sees an equivalent input of 4 V, instead of 48 V, at the inductor switching nodes. The on-chip 5-V transistor is, thus, applicable for the 48-1 V design, resulting in excellent switch quality, power efficiency, and switch integration. The detailed operation principles and analysis are described as follows.

### A. Operation Principles

Fig. 4 illustrates the four consecutive operation states of the proposed converter.

**State  $\phi_1$  ( $L_1$  Magnetizing and  $L_2$  Demagnetizing State):** The odd-number high-side switches ( $MH_1$ ,  $MH_3$ , ...,  $MH_{11}$ ) and even-number low-side switch  $ML_2$  turn on. The switching node  $SW_A$  is pulled up to  $V_{IN}/12 = 4$  V, and  $SW_B$  is grounded. During  $\phi_1$ , the odd-number series capacitors are

in the charging state, and the even-number capacitors are in the discharging state. As is shown,  $I_{L1}$  is supplied by six parallel capacitive current paths, i.e.,  $I_{C1}$ ,  $I_{C3}$ , ...,  $I_{C11}$ . Hence, charge redistribution could occur when the capacitive paths are shunted.

**State  $\phi_2$  ( $L_1$  and  $L_2$  Demagnetizing State):** Both low-side switches turn on with all the high-side switches OFF. Both switching nodes  $SW_A$  and  $SW_B$  are grounded, and both inductors are in demagnetization.

**State  $\phi_3$  ( $L_1$  Demagnetizing and  $L_2$  Magnetizing State):** The even-number high-side switches ( $MH_2$ ,  $MH_4$ , ...,  $MH_{12}$ ) and odd-number low-side switch  $ML_1$  turn on. The switching node  $SW_B$  is pulled up to  $V_{IN}/12 = 4$  V, and  $SW_A$  is grounded. During  $\phi_3$ , the even-number series capacitors are in the charging state, and the odd-number capacitors are in the discharging state. Similarly,  $I_{L2}$  is now supplied by six parallel capacitive current paths, i.e.,  $I_{C2}$ ,  $I_{C4}$ , ...,  $I_{C12}$ . Charge redistribution occurs when the capacitive paths are shunted.

**State  $\phi_4$  ( $L_1$  and  $L_2$  Demagnetizing State):** The same as state  $\phi_2$ .

According to the above states, the upper voltages of the switching nodes  $SW_A$  and  $SW_B$  are  $V_{IN} - V_{C1}$ , instead of  $V_{IN}$  as in the conventional buck converters. Since the switches and capacitors form a 12-stage Dickson step-down operation, in which the capacitors sustain a large portion of  $V_{IN}$ , the residue voltages on the switching nodes are, thus, significantly reduced, making it possible to implement the power switches with on-chip devices. A quantitative analysis is given as follows.

### B. Inductor Current Self-Balance and Power Stage Transfer Function

During the steady-state continuous conduction mode (CCM) into two-phase operation, the voltage conversion ratio can be calculated according to the voltage-second balance of the inductors. It follows that

$$\begin{aligned} D_1(V_{\text{IN}} - V_{C1}) - V_O &= \dots = D_1(V_{C10} - V_{C11}) - V_O = 0 \\ D_2(V_{C1} - V_{C2}) - V_O &= \dots = D_2V_{C11} - V_O = 0 \end{aligned} \quad (3)$$

where  $D_1$  and  $D_2$  are the duty cycles of the odd and even-number high-sides switches, respectively, while the  $V_C$ ,  $V_{\text{IN}}$ , and  $V_O$  are the average values of the series-capacitor voltages and the input and output voltages, respectively. Assuming that  $D_1 = D_2$ , the conversion ratio and capacitor voltages are given as

$$D_1 = D_2 = \frac{V_O}{V_{\text{IN}}/12} \quad (4)$$

$$V_{Ci} = \frac{12-i}{12}V_{\text{IN}}. \quad (5)$$

From (4), the duty cycle is boosted by 12 times compared to the conventional buck converter, leading to greatly simplified low-duty driver and controller designs. Besides, (5) indicates that the series capacitors, instead of the power switches, take over most of the input voltage stresses. For example, according to (5), the voltage across the first series capacitor  $C_1$  is  $V_{C1} = 44$  V, and the switching node voltage  $\text{SW}_A$  is, thus,  $48-44$  V = 4 V during the  $L_1$  magnetization period, rather than the total 48-V input as in the conventional buck converters. Therefore, as indicated in Fig. 1, the total power loss  $P_{\text{tot}}$  can be greatly reduced. In addition, according to the charge balance of the series capacitors during the steady state, the average capacitor currents  $I_{ci}$  and the inductor currents  $I_{Li}$  obey the following rules:

$$\begin{aligned} I_{Ci} &= I_{C(i+1)} \\ I_{L1} &= I_{L2} \end{aligned} \quad (6)$$

which implies that the current balance between the inductors is automatically achieved [15]. The high precision current sensors and complex current balance control circuits are, hence, waived.

During the CCM operation, the inductor current and series capacitor voltage ripples are approximated as

$$\Delta i_L \approx \frac{V_O(1 - 12V_O/V_{\text{IN}})T_{\text{SW}}}{L} \quad (7)$$

$$\Delta V_{Ci} \approx \frac{DT_{\text{SW}}I_C}{C} = \frac{V_OI_O}{f_{\text{sw}}V_{\text{IN}}C}. \quad (8)$$

From (7) and (8), the  $L$  and  $C$  values can be properly selected according to the inductor current and series capacitor voltage ripple specifications. As suggested in (7), the series-capacitor buck shows smaller current ripples compared to conventional buck converters, indicating more relaxed inductor choices. With a large  $V_{\text{IN}}$  and fast  $f_{\text{sw}}$ , (8) indicates the applicability of small value capacitors that help power density.

Using the state-space averaging and linearization techniques with small-ripple approximation, the power stage's control-to-output transfer function and the corresponding pole-zero

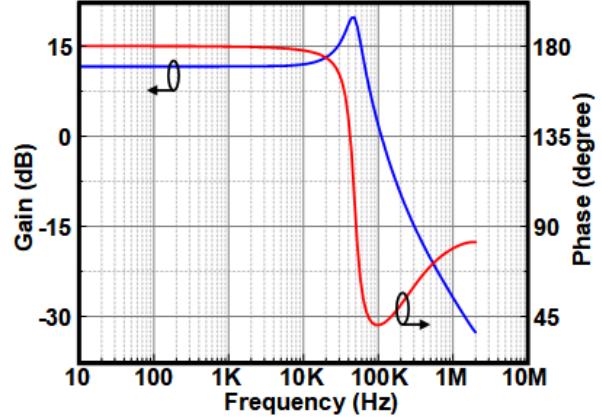


Fig. 5. Derived power stage transfer function of the proposed converter.

locations are given as

$$\begin{aligned} \hat{\frac{V_o}{d}} &= \frac{V_{\text{IN}}/12(1 + sR_{\text{ESR}}C_O)}{s^2 \frac{L}{2}C_O + s \frac{L}{2}/R + 1} \\ \Rightarrow \omega_p &= \frac{1}{\sqrt{LC_O/2}}\omega_{\text{ESR}} = \frac{1}{R_{\text{ESR}}C_O} \end{aligned} \quad (9)$$

where  $C_O$  is the output capacitance,  $R_{\text{ESR}}$  is the equivalent series resistance (ESR) of the output capacitor, and  $R = V_O/I_O$ . From (9), the series-capacitor buck converter shows the same form of the transfer function as that of a conventional buck. Therefore, all the typical compensation schemes for conventional buck converters can be applied here. Fig. 5 depicts the derived transfer function of this proposed work.

### C. Power Loss Analysis

Here, the switch quality determined loss  $P_{\text{FOM}}$ , the hard-switching overlap loss  $P_{\text{overlap}}$ , the passive loss, and the charge redistribution losses are described, respectively. For simplicity, the loss analysis is derived assuming all the high-side and low-side switches with the same FOM.

1) *Switch Quality Determined Loss  $P_{\text{FOM}}$ :* According to (1),  $P_{\text{FOM}}$  consists of switch conduction loss, driver loss, output capacitance loss, and reverse-recovery loss. Different applications usually show different dominant losses. For example, high-voltage designs usually focus on the conduction and output capacitance losses, while the low-voltage counterparts mostly target the conduction and driver losses. In order to make a general description, switching energy is adopted here to describe the power loss related to switching losses [16], [17]. Thus,  $P_{\text{FOM}}$  for a specific design is

$$P_{\text{FOM}} = I_{\text{rms}}^2 R_{\text{ON}} + f_{\text{sw}} E_{\text{SW}} \quad (10)$$

where  $I_{\text{rms}}$  is the root mean square current of the switch,  $R_{\text{ON}}$  is the ON-resistance,  $f_{\text{sw}}$  is the switching frequency, and  $E_{\text{SW}}$  is the energy required for one switching period, which includes the driver energy, the output capacitance energy, and the reverse-recovery energy.

To disclose a fair relationship between  $P_{\text{FOM}}$  and switch quality under different applications, an energy-based switch

FOM is defined here as  $\text{FOM}_E = R_{\text{ON}} E_{\text{SW}}$ . Substituting  $\text{FOM}_E$  into (10) gives

$$\begin{aligned} P_{\text{FOM}} &= I_{\text{rms}}^2 R_{\text{ON}} + f_{\text{sw}} \frac{\text{FOM}_E}{R_{\text{ON}}} \\ \Rightarrow P_{\text{FOM},\min} &= 2\sqrt{\text{FOM}_E f_{\text{sw}}} I_{\text{rms}}. \end{aligned} \quad (11)$$

It is clear that, for a specific application for specified  $f_{\text{sw}}$  and  $I_{\text{rms}}$ , the lower the  $\text{FOM}_E$ , which indicates better switch quality, the lower the minimum switch quality determined loss  $P_{\text{FOM}}$ .

For the proposed 12-level series-capacitor converter, using small-ripple assumption for simplicity,  $P_{\text{FOM}}$  of the total 12 high-side and two low-side switches are approximated as

$$\begin{aligned} P_{\text{FOM,LS,min}} &\approx 2\sqrt{\text{FOM}_E f_{\text{sw}}} I_{O,\text{rms}} \sqrt{1+2D} \\ P_{\text{FOM,HS,min}} &\approx 2\sqrt{\text{FOM}_E f_{\text{sw}}} I_{O,\text{rms}} \sqrt{D} \end{aligned} \quad (12)$$

respectively.

2) *Hard-Switching Overlap Loss  $P_{\text{overlap}}$* : In hard switching buck converters, the high-side switches show brief saturation operation during the turn on and off transients, in which the large switch  $V_{\text{DS}}$  and large  $I_{\text{DS}}$  overlap with each other and incurring huge instantaneous overlap losses. When the overlap time is  $t_r$  and  $t_f$ , respectively, for the turn on and off transients, the overall  $P_{\text{overlap}}$  is

$$P_{\text{overlap}} = 6f_{\text{sw}} V_{\text{DS}} I_{\text{DS}} (t_r + t_f) = 12f_{\text{sw}} I_{\text{DS}} V_{\text{DS}}^2 \left/ \left( \frac{dv}{dt} \right) \right. \quad (13)$$

in which  $t_r = t_f$  is assumed and  $dv/dt$  represents the slew rate of the switching node. Since this proposed work reduces the equivalent  $V_{\text{DS}}$  from 48 to 4 V,  $P_{\text{overlap}}$  is sharply reduced.

3) *Inductor DCR and Series-Capacitor ESR Loss*: According to the current profile of the inductor and series capacitors with the assumption of current balance between the inductors and capacitors, the total inductor DCR and the series-capacitor ESR losses are given as

$$\begin{aligned} P_{\text{DCR}} &= 2I_{L,\text{rms}}^2 R_{\text{DCR}} \approx 2 \left( \left( \frac{I_O}{2} \right)^2 + \frac{(\Delta i_L)^2}{12} \right) R_{\text{DCR}} \\ P_{\text{ESR}} &= 11I_{C,\text{rms}}^2 R_{\text{ESR}} \approx 11 \times 2D(I_{L,\text{rms}}/6)^2 R_{\text{ESR}}. \end{aligned} \quad (14)$$

Since the proposed work adopts two inductors to share the full load and the ripple current is attenuated by the 12-level design, as implied by (7), the inductor selection is relatively relaxed. In this design, two 110-nH inductors with 3-mΩ DCR are employed to make a tradeoff between the efficiency and power density. In addition, the series capacitors also share the inductor current with each capacitor flowing only one-sixth of the inductor current; thus, the ESR losses are greatly attenuated. Multilayer ceramic capacitors (1 μF) with low ESR (typical 5 mΩ) are adopted here. Substituting the typical values into (14) gives the estimated  $P_{\text{DCR}}$  and  $P_{\text{ESR}}$  of 99.83 (7.4% of total loss) and 12.69 mW (0.9% of total loss), respectively, at an 8-A load.

4) *Charge Redistribution Loss*: As described in Section II-A, during the inductor magnetization period, each inductor current is supplied by a parallel combination of six capacitive paths. The shunting of the series capacitors,

however, induces charge redistribution losses, especially under capacitance and switch resistance variations. To attenuate this issue, either each series capacitor should be exactly calculated [18] or the turn-on timing of each high-side switch be carefully controlled [19]. In this design, considering that a large number of series capacitors are employed here and the switching frequency is high, the residual redistribution charge and the corresponding loss should be small. Simulation results in Section IV give an estimated charge redistribution loss of 24.68 mW (1.8% of total loss) under an 8-A load condition.

According to the above analysis, the total loss of a converter can be written as

$$P_{\text{tot}} \approx P_{\text{FOM}} + P_{\text{overlap}} + P_{\text{passive}}. \quad (15)$$

Assuming all the switches achieve minimum  $P_{\text{FOM}}$ , the minimum  $P_{\text{tot}}$  of a conventional buck and the proposed converter can be described as

$$\begin{aligned} P_{\text{tot,min,buck}} &= 2\sqrt{f_{\text{sw}} \text{FOM}_{E,\text{HV}}} I_{O,\text{rms}} (\sqrt{D} + \sqrt{1-D}) \\ &\quad + V_{\text{IN}}^2 f_{\text{sw}} I_{\text{OUT}} \left/ \left( \frac{dv}{dt} \right) \right. + P_{\text{passive}} \end{aligned} \quad (16)$$

$$\begin{aligned} P_{\text{tot,min,proposed}} &= 2\sqrt{f_{\text{sw}} \text{FOM}_{E,\text{LV}}} I_{O,\text{rms}} (\sqrt{D} + \sqrt{1+2D}) \\ &\quad + \left( \frac{V_{\text{IN}}}{12} \right)^2 I_{\text{OUT}} f_{\text{sw}} \left/ \left( \frac{dv}{dt} \right) \right. + P_{\text{passive}}. \end{aligned} \quad (17)$$

According to (16) and (17), the proposed 12-level series-capacitor design significantly reduces the hard-switching overlap loss  $P_{\text{overlap}}$ . Besides, the switch quality determined loss  $P_{\text{FOM}}$  is also greatly attenuated using the superior 5-V devices. The extra capacitor ESR and charge redistribution losses, as indicated by the above simulations, are still negligible compared to the above losses. Therefore, a higher switching frequency is applicable in this design for better passive device volumes.

### III. CIRCUIT IMPLEMENTATIONS

Fig. 6 depicts the circuit diagram of the proposed 12-level series-capacitor dc-dc converter. Here,  $\text{MH}_1\text{-}\text{MH}_{12}$  form the high-side power switches, and  $\text{ML}_1$  and  $\text{ML}_2$  are the two groups of low-side switches. All the power switches, except  $\text{MH}_1$ , are integrated on-chip using 5-V transistors. Besides, a time-domain voltage mode controller is implemented with an operational transconductance amplifier (OTA), a voltage-controlled delay line (VCDL)-based pulselwidth modulator (PWM), and logic circuits. The proposed controller retains both the robustness of the conventional OTAs and the high-frequency PWM modulation ability of the time-domain circuits. Since the high-frequency VCDL is shared among the channels, the duty cycles are easily balanced.

#### A. Power Switch Design Considerations

1) *Startup Using GaN FET  $\text{MH}_1$* : Although the maximum  $V_{\text{DS}}$  of the high- and low-side switches are only  $V_{\text{IN}}/6$  and  $V_{\text{IN}}/12$ , respectively, during the steady state, the voltage stress of the power transistors could be larger during the startup when the series capacitors have yet built up enough voltages, or when the converter is not switching. To solve this problem,

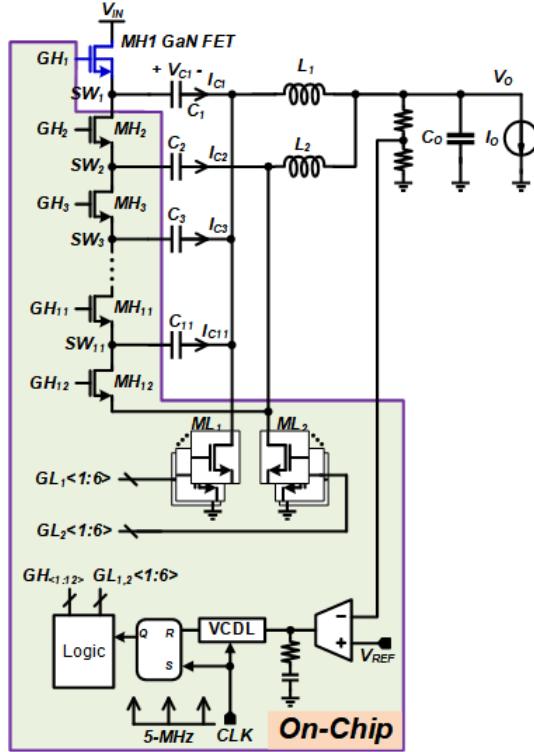


Fig. 6. Circuit diagram of the proposed converter.

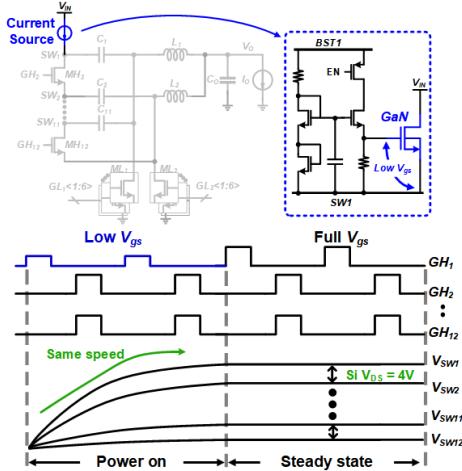


Fig. 7. Converter startup operations waveforms.

a 60-V EPC2035 GaN FET is chosen as the uppermost high-side switch  $MH_1$  to take over all the extreme voltage stress. In Fig. 7, during the startup,  $MH_1$  works in the current source mode and delivers a limited amount charge to  $C_1$  every cycle. Therefore, the voltage on  $C_1$  increases slowly with most of the input voltage stress taken by  $MH_1$ . Due to the series-capacitor voltage-balance feature of this topology, all the capacitor voltages build up with evenly distributed voltage differences. After the series capacitors build enough voltages,  $MH_1$  turns back to the switching mode operations.

2) *High-Side Switch Implementation:* The maximum  $V_{DS}$  of the high-side switches  $MH_2$ - $MH_{12}$  is  $V_{IN}/6 = 8$  V, which

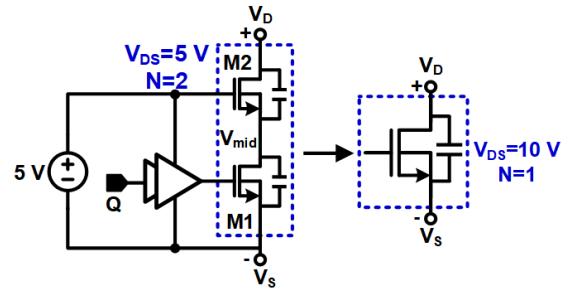


Fig. 8. High-side power switch implementation.

is larger than the voltage rating of 5-V on-chip devices. Fig. 8 demonstrates the high-side switch implementations of this work.

Here, a cascaded switch is implemented with the upper switch  $M_2$  driven by a constant 5-V voltage, and the lower switch  $M_1$  performs the ON-OFF function. When the control signal  $Q$  is low,  $M_1$  turns off with its drain  $V_{mid}$  be protected below 5 V. Since both  $M_1$  and  $M_2$  are implemented using 5-V devices, the maximum  $V_{DS}$  rating becomes 10 V.

To roughly appreciate the advantages of the cascade devices to high-voltage devices, the output capacitance related FOM =  $R_{ON} Q_{OSS}$  is derived here for simple comparisons

$$FOM_{stack-10V} \approx N \times R_{ds(on)} \frac{C_{oss}}{N} = FOM_{5V} < FOM_{10V} \quad (18)$$

where  $FOM_{stack-10V}$  is the equivalent FOM of the stacking transistors, while  $FOM_{5V}$  and  $FOM_{10V}$  are that of the 5- and 10-V transistors. Equation (18) shows that stacking increases the switch conduction resistance and proportionally reduces the output capacitance. Thus, the stacking 10-V transistors show superior FOM compared to the original 10-V devices. Therefore, the stacking low-voltage switches are usually more area- and energy-efficient compared to the high-voltage counterparts, as reported in [20] and [21].

### B. Gate Driver Design

Since the 12 high-side switches all operate at different voltage levels, 12 individual floating voltage sources are needed to drive the high-side switches. Directly powering the driver circuits from the uppermost 48-V input could be excessively lossy, especially for the lower level switches. Fig. 9 depicts the proposed energy-efficient driver circuits. Here, since  $MH_1$  and  $MH_2$  operate at the voltage levels close to the 48-V input,  $MH_1$  and  $MH_2$  adopt the driver scheme shown in Fig. 9 (top), which is powered directly by  $V_{IN}$ . The driver consists of a self-biased boot-strap voltage monitor, an active diode, and a bootstrap capacitor. The voltage monitor detects whether the boot-strap voltage exceeds 5 V and determines the conduction of the active diode.

For  $MH_3$ - $MH_{12}$  which operate at lower voltage levels, the driver scheme shown in Fig. 9 (bottom) is applied. Instead of being powered by  $V_{IN}$ , the  $i$ th high-side driver is supplied by the switching node  $SW_{(i-2)}$  considering that the voltage difference between  $SW_{(i-2)}$  and  $SW_i$  is a constant 8 V, which results from the common bottom connection of odd (even)

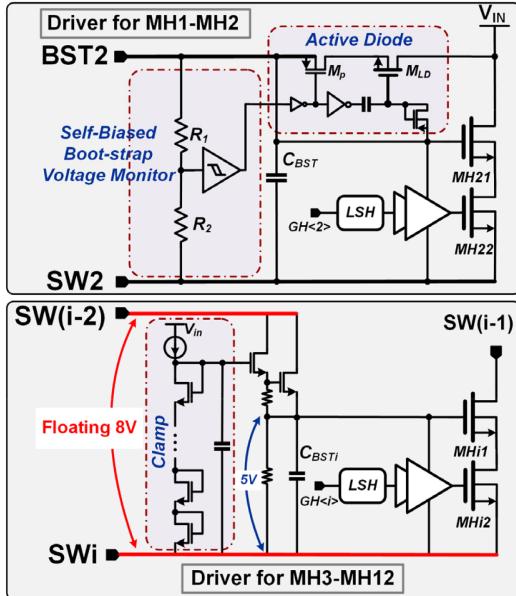


Fig. 9. Proposed energy-efficient high-side drivers.

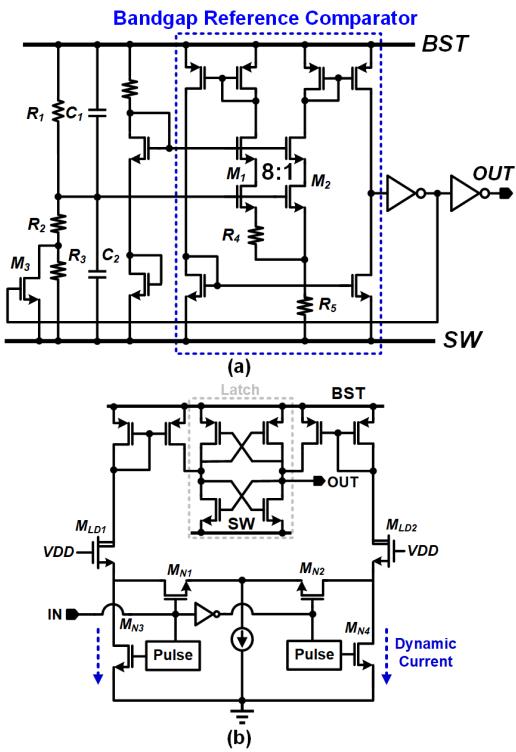


Fig. 10. (a) Self-biased boot-strap voltage monitor and (b) level shifter circuits.

number series capacitors. A 5-V clamp circuit generates the 5-V floating supply for each switch from the 8-V floating sources. In this way, an energy-efficient high-side switch driving scheme is achieved.

Fig. 10(a) depicts the circuit design of the self-biased boot-strap voltage monitor that adopts a bandgap reference core for voltage detection [22]. Here, the subthreshold

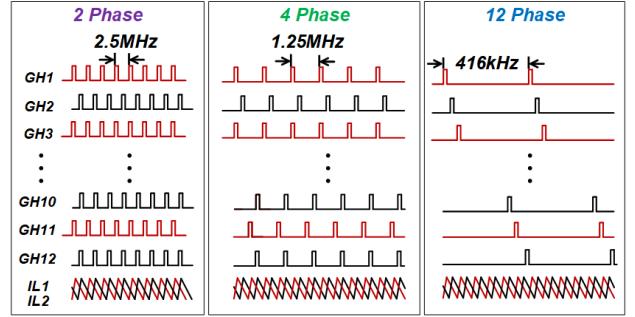


Fig. 11. Split-phase control scheme under different load conditions.

operations  $M_1$ ,  $M_2$ ,  $R_4$ , and  $R_5$  form a Brokaw bandgap core circuit, while  $R_1-R_3$  sense the boot-strap voltage. The devices are sized to toggle the output when the boot-strap voltage exceeds 5 V. Since the boot-strap voltage is relatively slow, little power is required for accurate voltage detection. Fig. 10(b) gives the circuit implementation of the level shifter. By applying a pulsing current during the signal transition time, high-speed level shifting and decent common-mode transient immunity are achieved with moderate current consumptions.

### C. Controller Design

Due to the superior switch FOM of this proposed work, a relatively higher switching frequency can be adopted in this design. To accommodate the converter with high switching speed, this work proposes a VCDL-based PWM modulator with a typical Type-III compensator. By applying the compensator output to the VCDL, a compensator-controlled delay is obtained. In this way, the controller retains both the robustness of the conventional OTAs and the high-frequency PWM modulation ability of the time-domain circuits. In this work, the duty cycle  $D$  is designed as  $D \approx K_{VCDL}/V_C - 0.36$ , where  $K_{VCDL}$  approximates 1.6 V and the maximum duty ratio is limited below 0.5.

In addition, a manually controlled split-phase control scheme is implemented to verify the driver loss reduction under light load conditions, as shown in Fig. 11. During the heavy load, the odd and even number switches form two switching groups, respectively, with 2.5-MHz per group and 180° phase shifted. For medium load, the odd and even number groups are further divided into four, each with 1.25-MHz frequency and 90° phase shift. Finally, for light load conditions, the high- and low-sides switches are split into 12 phases, each with 416-kHz frequency and 30° phase shift. As will be shown, the split-phase control helps improve the light load efficiency.

## IV. MEASUREMENT RESULTS

The proposed 48-1 V converter was implemented and verified using a 0.18- $\mu$ m 80 V BCD process. Fig. 12 shows the die photograph and evaluation board. The die area is 4.034 mm × 4.534 mm. The high- and low-side power switches are placed around the peripheral to minimize the layout routing and bonding-wire resistances. The evaluation

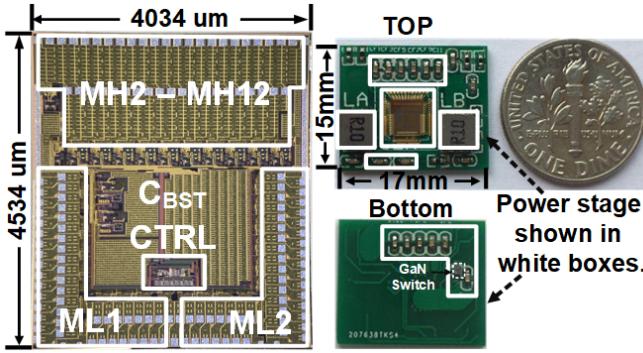


Fig. 12. Chip microphotograph and evaluation board of the proposed converter.

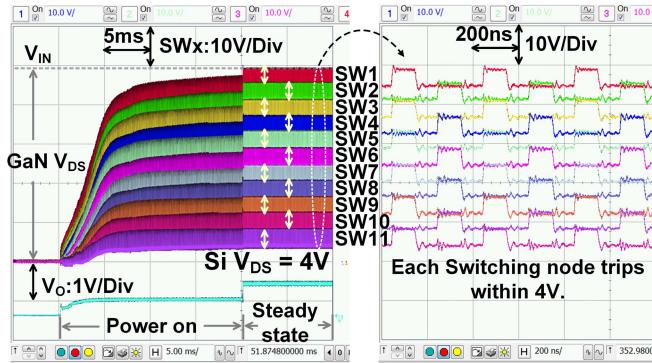


Fig. 13. Measured waveforms of each switching node  $SW_i$  and  $V_O$  during the power ON and steady-state operations.

board volume is  $17 \text{ mm} \times 15 \text{ mm} \times 2.6 \text{ mm}$  and that of the power stage is around  $50 \text{ mm}^2 \times 2.6 \text{ mm}$ . Due to the switch integration, the external switch count is significantly reduced. The prototype operates with an input voltage from 36 to 60 V and generates a regulated output from 0.5 to 1 V.

Fig. 13 shows the measured waveforms of each switching node during the power ON and normal operation. When the converter is idled,  $MH_1$  sustains the full 48-V voltage stress. As the circuit powers ON, all the switching nodes move up at the same speed and settle with maximum voltage stress of one-twelfth of  $V_{IN}$ , i.e., 4 V. The steady-state waveform clearly indicates the odd and even number operating phases. Besides, the voltage levels of each switching node are well controlled.  $SW_1$  switches between 48 and 44 V,  $SW_2$  between 44 and 40 V, and so on, with each switching node trips within 4 V.

Fig. 14 shows the measured self-balance of switching nodes during the line transient. As  $V_{IN}$  steps from 48 to 60 V, all the switching nodes move up at the same speed with the maximum voltage stress changing from 4 to 5 V. The self-balance of each switching node demonstrates the strong robustness of the proposed hybrid conversion over a wide input range.

Fig. 15 gives the measured inductor currents  $I_{L1}$  and  $I_{L2}$  and series capacitor currents  $I_{C3}$  and  $I_{C9}$  during split-phase control. For two-phase operations with a 6-A load, all the odd (or even) number switches operate at the same phase at 2.5 MHz, and each inductor delivers 3 A. For four phases with a 2.5-A load, the odd number switches are divided into

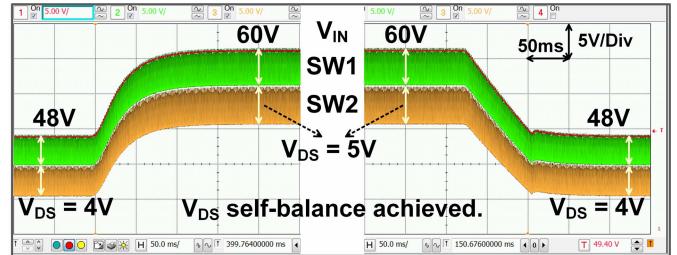


Fig. 14. Measured self-balance of switching nodes during the line transient between 48 and 60 V.



Fig. 15. Current waveforms during the split-phase control.

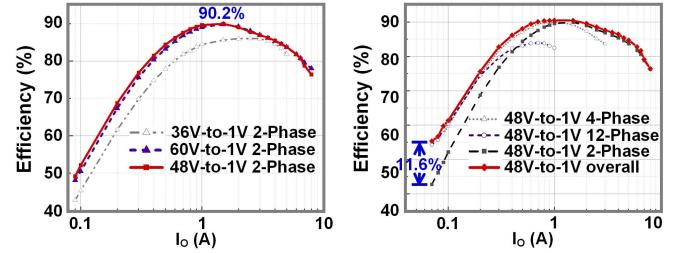


Fig. 16. Measurement efficiency curves.

two groups with a 1.25-MHz switching frequency with each inductor current of 1.25 A. For 12 phases with a 100-mA load, each switch  $MH_i$  operates sequentially with a switching frequency of 416 kHz.

Fig. 16 shows the measured power efficiency. The 48-1 V converter delivers a maximum load current of 8 A with a peak efficiency of 90.2%. Besides, the split-phase control scheme helps improve the efficiency by 11.6% at a 70-mA load.

Fig. 17(a) illustrates an estimated power loss breakdown extracted from simulations based on device parameters, post-layout extractions, and estimated passive component resistances. The switch quality determined loss  $P_{FOM}$ , the hard-switching overlap loss  $P_{overlap}$ , and the layout and bonding wire losses are around 42%, 22.1%, and 23.6%, respectively. Fig. 17(b) shows the measured load transient responses. The output  $V_O$  shows under/overshoot voltages of  $-114.5$  and  $92.3$  mV, respectively, when the load changes between 0 and 5 A.

Table I demonstrates the performance summary of the proposed work and the prior-state-of-the-arts. Due to the integration and superior FOM of 5-V on-chip transistors, the external switch count reduces to one, and the switching frequency is boosted to 2.5 MHz per phase without severely

TABLE I  
COMPARISON WITH THE STATE-OF-THE-ARTS

	APEC 2017 [1]	TPE 2020 [2]	ISSCC 2020 [4]	ECCE 2018 [6]	APEC 2019 [7]	This Work
Structure	Sigma converter	Active clamp forward converter	3-level + current doubler	Dual-phase dual-inductor hybrid	Dual-phase multi-inductor hybrid	12-level series capacitor + on-chip switch & GaN hybrid
V <sub>IN</sub> [V]	48	48	48 – 60	40 – 54	48	36 – 60
V <sub>O</sub> [V]	0.8 – 1	0.7 – 1.1	0.5 – 1	1 – 2	1 – 5	0.5 – 1
I <sub>O_MAX</sub> [A]	80	60	60	10	100	8
Power Transistor	MOSFET & GaN	MOSFET	MOSFET	GaN	GaN	On-chip MOSFET & GaN
Peak Efficiency [%] at V <sub>IN</sub> =48V	93.4	89.5	92.8	93	90.9	90.2
Peak Efficiency [%] at V <sub>IN</sub> =60V	–	–	92	–	–	89.8
Switch FOM [ $\text{m}\Omega \cdot \text{nC}$ ]	9.8 & 54	40.5	28.3	34.5	34.5	4.2
# of magnetics	5	2	3	2	4	2
# of ext. switches	14	4	6	8	8	1
FSW [kHz]	1000/600	325	333	300	333	2500 x 2
Current Density [A/inch <sup>2</sup> ]	420*	230.8*	–	225**	440**	196* / 998**

\* Consider the overall board volume. \*\* Consider the power stage volume.

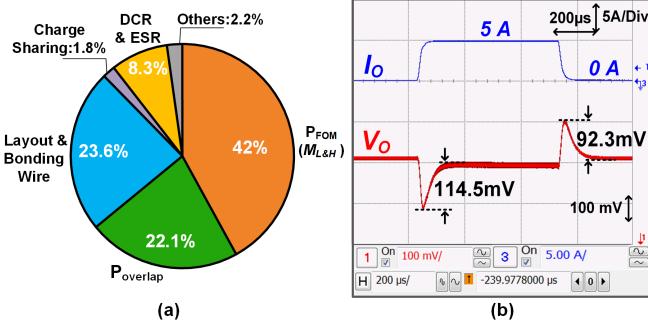


Fig. 17. (a) Estimated power loss breakdown when  $I_O = 8$  A. (b) Measured load transient response between 0 and 5 A with  $C_o = 47 \mu\text{F} \times 4$ .

degrading power efficiency. Therefore, low-value inductors can be adopted, and a 998-A/in<sup>3</sup> power density is achieved, which considers only the power stage and chip volumes of the white boxes in Fig. 12 (right).

## V. CONCLUSION

In summary, this proposed work carefully investigated the power loss bottleneck of a typical buck converter, i.e., the switch quality determined loss and the hard switching overlap loss, both of which are proportional to the input voltage. Guided by the above observation, this work proposes a 12-level series-capacitor 48-1 V dc-dc converter, which spreads most of the 48-V voltage stress on the series capacitors and turns the 48-1 V into a 4-1 V converter, thus making 5-V on-chip switch applicable for 48-V high-voltage design. Due to the easy integration of on-chip switches and superior switch FOM over other 48-1 V counterparts, this proposed design is able to achieve the lowest switch FOM, the highest switching frequency, the lowest external switch count, and the improved power density compared with other prior-state-of-the-arts.

TABLE II  
POWER LOSS EQUATIONS

Loss	Formula
P <sub>overlap</sub>	$P_{SW} = \left(\frac{V_{IN}}{2} \times (t_{r-H} + t_{f-H}) + \frac{V_D}{2} \times (t_{r-L} + t_{f-L})\right) \times f_{SW} I_{OUT}$
P <sub>CON</sub>	$P_{CON} = (I_{OUT}^2 + (\Delta I)^2 / 12) \times (R_{ON-H} D + (1 - D) R_{ON-L})$
P <sub>G</sub>	$P_G = (Q_{g-H} + Q_{g-L}) \times V_{gs} \times f_{SW}$
P <sub>RR</sub>	$P_{RR} = V_{IN} \times Q_{RR} \times f_{SW}$
P <sub>COSS</sub>	$P_{COSS} = \frac{1}{2} \times (Q_{oss-L} + Q_{oss-H}) \times V_{IN} \times f_{SW}$
P <sub>d</sub>	$P_d = V_D \times I_{OUT} \times (t_{dr} + t_{df}) \times f_{SW}$
P <sub>DCR</sub>	$P_{DCR} = (I_{OUT}^2 + (\Delta I)^2 / 12) \times R_{DCR}$
P <sub>ESR</sub>	$P_{ESR} = (\Delta I)^2 / 12 \times R_{ESR}$

To the best of our knowledge, this work is the first 48-1 V design that adopted on-chip devices as main power switches.

## APPENDIX

For a typical buck converter shown in Fig. 1, the power losses can be categorized in Table II, where  $P_{CON}$ ,  $P_{overlap}$ ,  $P_{COSS}$ ,  $P_G$ ,  $P_{RR}$ ,  $P_d$ ,  $P_{DCR}$ , and  $P_{ESR}$  are the conduction loss, the hard-switching overlap loss, the output capacitance loss, the driver loss, the reverse recovery loss, the dead time reverse conduction loss, the inductor DCR loss, and the output

capacitor ESR loss, respectively [8]. To fairly disclose the relationship between  $P_{\text{FOM}}$  and switch quality under different applications, an energy-based switch FOM is defined here as  $\text{FOM}_E = R_{\text{ON}} E_{\text{SW}}$ , where  $R_{\text{ON}}$  is the resistance of the switch and  $E_{\text{SW}}$  is defined as the switching energy for each switching period.  $E_{\text{SW}}$  can be expressed as

$$E_{\text{SW}} = Q_G V_{\text{DD}} + Q_{\text{OSS}} V_{\text{IN}}/2 + Q_{\text{RR}} V_{\text{IN}}. \quad (19)$$

For a typical buck converter, the total power loss  $P_{\text{tot}}$  is derived as

$$P_{\text{tot}} = I_{\text{rms},H}^2 R_{\text{ON},H} + f_{\text{SW}} E_{\text{SW},H} + I_{\text{rms},L}^2 R_{\text{ON},L} + f_{\text{SW}} E_{\text{SW},L} + P_{\text{other}} \quad (20)$$

where  $I_{\text{rms},H}$ ,  $I_{\text{rms},L}$ , and  $P_{\text{other}}$  are

$$\begin{cases} I_{\text{rms},H} = \sqrt{(I_{\text{OUT}}^2 + (\Delta I)^2/12)D} \\ I_{\text{rms},L} = \sqrt{(I_{\text{OUT}}^2 + (\Delta I)^2/12)(1-D)} \\ P_{\text{other}} = P_{\text{overlap}} + P_d + \left( I_{\text{OUT}}^2 + \frac{(\Delta I)^2}{12} \right) R_{\text{DCR}} + R_{\text{ESR}} \frac{(\Delta I)^2}{12} \end{cases} \quad (21)$$

respectively.

Substituting (21) into (20) gives the minimum loss  $P_{\text{tot,min}}$ , under a specific input voltage  $V_{\text{IN}}$ , as

$$P_{\text{tot,min}} = 2\sqrt{f_{\text{SW}} \text{FOM}_E} I_{\text{rms},H} + 2\sqrt{f_{\text{SW}} \text{FOM}_E} I_{\text{rms},L} + P_{\text{other}} \quad (22)$$

and the corresponding optimum switch parameters are

$$\begin{cases} R_{\text{ON},L,\text{optimized}} = \frac{\sqrt{f_{\text{SW}} \text{FOM}_E}}{I_{\text{rms},L}} E_{\text{SW},L} = \frac{\text{FOM}_E}{R_{\text{ON},L,\text{optimized}}} \\ R_{\text{ON},H,\text{optimized}} = \frac{\sqrt{f_{\text{SW}} \text{FOM}_E}}{I_{\text{rms},H}} E_{\text{SW},H} = \frac{\text{FOM}_E}{R_{\text{ON},H,\text{optimized}}} \end{cases} \quad (23)$$

## REFERENCES

- [1] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 48/1 V sigma converter voltage regulator module," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Tampa, FL, USA, Mar. 2017, pp. 2207–2212.
- [2] X. Zhang *et al.*, "A 12- or 48-V input, 0.9-V output active-clamp forward converter power block for servers and datacenters," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1721–1731, Feb. 2020.
- [3] *Using the LMG5200POLEVIM-10A GaN 48V-1V Point-of-Load EVM*, LMG5200POLEVIM-10A User's Guide, Texas Instruments, Dallas, TX, USA, Oct. 2017. [Online]. Available: <http://www.ti.com/lit/ug/snvu520b/snvu520b.pdf>
- [4] M. Choi *et al.*, "A 92.8%-peak-efficiency 60A 48V-to-1V 3-level half-bridge DC-DC converter with balanced voltage on a flying capacitor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2020, pp. 296–298.
- [5] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5048–5062, Jun. 2019.
- [6] G.-S. Seo, R. Das, and H.-P. Le, "A 95%-efficient 48 V-to-1 V/10A VRM hybrid converter using interleaved dual inductors," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 3825–3830.
- [7] R. Das and H.-P. Le, "A regulated 48 V-to-1 V/100A 90.9%-efficient hybrid converter for POL applications in data centers and telecommunication systems," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Anaheim, CA, USA, Mar. 2019, pp. 1997–2001.
- [8] D. Jauregui *et al.*, "Power loss calculation with common source inductance consideration for synchronous buck converters," Texas Instrum., Dallas, TX, USA, Appl. Note SLPA009A, Jun. 2011.
- [9] X. Yang *et al.*, "An 8A 998A/inch<sup>3</sup> 90.2% peak efficiency 48V-to-1V DC-DC converter adopting on-chip switch and GaN hybrid power conversion," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2021, pp. 466–468.
- [10] D. Yan *et al.*, "Direct 48-1-V GaN-based DC-DC power converter with double step-down architecture and master-slave AO<sup>2</sup>T control," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 988–998, Apr. 2020.
- [11] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "A double step-down two-phase buck converter for VRM," in *Proc. Eur. Conf. Power Electron. Appl.*, Dresden, Germany, 2005, p. 8.
- [12] Texas Instruments. (2019). *TPS54A20EVM-770 User Guide*. Accessed: Dec. 1, 2020. [Online]. Available: <https://www.ti.com/tool/TPS54A20EVM-770>
- [13] P. S. Shenoy, M. Amaro, J. Morroni, and D. Freeman, "Comparison of a buck converter and a series capacitor buck converter for high-frequency, high-conversion-ratio voltage regulators," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7006–7015, Oct. 2016.
- [14] R. Das, G.-S. Seo, and H.-P. Le, "A 120V-to-1.8V 91.5%-efficient 36-W dual-inductor hybrid converter with natural soft-charging operations for direct extreme conversion ratios," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2018, pp. 1266–1271.
- [15] P. S. Shenoy *et al.*, "Automatic current sharing mechanism in the series capacitor buck converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 2003–2009.
- [16] Y. Lei, W. C. Liu, R. Carl, and N. Pilawa-Podgurski, "An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018.
- [17] P. H. McLaughlin *et al.*, "Analysis and comparison of hybrid-resonant switched-capacitor DC-DC converters with passive component size constraints," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3111–3125, Mar. 2021.
- [18] R. Das, G.-S. Seo, and H.-P. Le, "Analysis of dual-inductor hybrid converters for extreme conversion ratios," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Apr. 2, 2020, doi: [10.1109/JESTPE.2020.2985116](https://doi.org/10.1109/JESTPE.2020.2985116).
- [19] P. Assem, W.-C. Liu, Y. Lei, P. K. Hanumolu, and R. C. N. Pilawa-Podgurski, "Hybrid Dickson switched-capacitor converter with wide conversion ratio in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2513–2528, Sep. 2020.
- [20] P. Renz *et al.*, "A fully integrated 85%-peak-efficiency hybrid multi ratio resonant DC-DC converter with 3.0-to-4.5V input and 500μA -to-120mA load range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 156–158.
- [21] F. Neveu, B. Allard, C. Martin, P. Bevilacqua, and F. Viron, "A 100 MHz 91.5% peak efficiency integrated buck converter with a three-MOSFET cascode bridge," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 3985–3988, Jun. 2016.
- [22] R. Yan, J. Xi, and L. He, "A 2–10 MHz GaN HEMTs half-bridge driver with bandgap reference comparator clamping and dual level shifters for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1446–1454, Feb. 2020.



**Haixiao Cao** received the B.S. degree in electronic information science and technology from Hefei University of Technology, Anhui, China, in 2018, and the M.S. degree in electronic science and technology from the School of Micro-Nano Electronics, Zhejiang University, Hangzhou, China, in 2021.

He is currently working at Silergy Corporation, Hangzhou. His current research interests include gallium nitride (GaN) drivers and power management integrated circuits.



**Xu Yang** received the B.S. degree in electronic information science and technology from Central South University, Changsha, China, in 2018. He is currently pursuing the Ph.D. degree in electronic science and technology with the School of Micro-Nano Electronics, Zhejiang University, Hangzhou, China.

His current research interests include gallium nitride (GaN) drivers, power converter topologies, and power management integrated circuits.



**Chenkang Xue** received the B.S. degree in IC design and integrated systems from Xidian University, Xi'an, China, in 2019. He is currently pursuing the Ph.D. degree in electronic science and technology with the School of Micro-Nano Electronics, Zhejiang University, Hangzhou, China.

His current research interests include energy harvesting systems and power converter topologies.



**Menglian Zhao** received the M.S. degree in microelectronics and solid-state circuits and the Ph.D. degree in engineering circuits and systems from Zhejiang University, Hangzhou, China, in 2001 and 2004, respectively.

She joined the College of Electrical Engineering, Zhejiang University, in 2004. From 2005 to 2006, she was a Research Assistant with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong. She is currently an Associate Professor with the College of Information Science and Electronic Engineering, Zhejiang University. Her current interests include CMOS analog and mixed-signal integrated circuit design, low-power techniques for integrated circuits and system on chip (SoC), and power management integrated circuits.



**Yong Ding** (Member, IEEE) received the Ph.D. degree from Southeast University, Nanjing, China, in 2008.

He joined the faculty of Zhejiang University, Hangzhou, China, in 2009, as a Full Professor. Up until now, he has published over 100 publications in journals and holds more than 30 Chinese patents. His research interests concentrate on digital image processing and system on chip (SoC) design.



**Lenian He** (Member, IEEE) received the B.Sc. degree from the Department of Electronic Engineering, Southeast University, Nanjing, China, in 1983, and the Ph.D. degree from Kanazawa University, Ishikawa, Japan, in 1996.

From 1983 to 1990, he was a principal Engineer/CTO with Suzhou Semiconductor Cooperation, Suzhou, China, where he was responsible for developing CMOS sensors and ICs. In 1999, he joined Zhejiang University, Hangzhou, China, as an Associate Professor. Since 2002, he has been a Full Professor with the College of Electrical Engineering, Zhejiang University. He is currently the Professor with the Institute of VLSI Design and the Vice-Dean of the School of Micro and Nano Electronics, Zhejiang University. He is the author or a coauthor of more than 120 articles and three books on analog/power IC design. He holds 34 patents. His research interests are power management ICs, ac/dc controllers, and data converters.



**Wuhua Li** (Member, IEEE) received the B.Sc. and Ph.D. degrees in power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From 2004 to 2005, he was a Research Intern and, from 2007 to 2008, a Research Assistant with the GE Global Research Center, Shanghai, China. From 2008 to 2010, he held a postdoctoral position at the College of Electrical Engineering, Zhejiang University, where he was promoted to an Associate Professor in 2010. From 2010 to 2011, he was a Ryerson University Post-Doctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. Since 2013, he has been a Full Professor with Zhejiang University. He is currently the Executive Deputy Director of the National Specialty Laboratory for Power Electronics and the Vice-Director of the Power Electronics Research Institute, Zhejiang University. He has published more than 300 peer-reviewed technical articles. He holds over 50 issued/pending patents. His research interests include power devices, converter topologies, and advanced controls for high-power energy conversion systems.



**Zhichao Tan** (Senior Member, IEEE) received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 2004, the M.Eng. degree from Peking University, Beijing, China, in 2008, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2013.

He was a Staff IC Design Engineer with Analog Devices Inc., Wilmington, MA, USA, from 2013 to 2019. In 2019, he joined Zhejiang University, Hangzhou, China, as a Faculty Member. His current research interests are in the areas of energy-efficient sensor interfaces, precision analog circuits, and ultralow-power analog to digital converters (ADCs); this has resulted in more than 30 technical articles and five U.S. patents.

Dr. Tan is also a member of the Technical Program Committee (TPC) of the IEEE Asian Solid-State Circuits Conference. He has served as an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS. He is also an Associate Editor of IEEE SENSORS JOURNAL.



**Wanyuan Qu** (Member, IEEE) received the B.S. degree from Beijing University of Posts and Telecommunications, Beijing, China, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2008 and 2016, respectively.

He was a Principle Circuit Design Engineer with Silicon Works Ltd., Daejeon, from 2008 to 2017. In 2017, he joined Zhejiang University, Hangzhou, China, where he is currently an Associate Professor. He has been granted eight U.S. patents and five Korean patents. His current research interests include high-power density dc–dc converters, gallium nitride (GaN) drivers and converters, energy harvesters, and high-performance amplifiers.

Dr. Qu also serves as a member of the Technical Program Committee (TPC) of the IEEE Asian Solid-State Circuits Conference and the IEEE International Conference on Integrated Circuits, Technologies and Applications. He also serves as an Associate Editor for *The Journal of Engineering* (IET).