

Design and Implement of MVB BUS Controller Based on FPGA

Lixia Zuo, Qingfeng Ding, Yunbao Tang

School of Electronical and Electrical Engineering Departments , East China Jiaotong University
Nanchang, Jiangxi Province, China
brandy724@sina.com

Abstract—This paper introduces the TCN MVB (Multifunction Vehicle Bus) communication mechanism and characteristics. On this basis, a method of VHDL language is designed for the core part of MVBC (MVB bus controller), such as the Manchester encoding and decoding, CRC check functions, etc. Among them, the bus's CRC checksum data is formed with a double check of the 8-bit check sequence, including the 7 CRC checksum and an even parity bit. As different frame formats of MVB bus, serial CRC algorithm is choosed. Eventually, the right simulation waveforms of the cores of MVBC is obtained and realized on FPGA hardware.

Keywords—MVBC; FPGA; CRC; Manchester; encoding; decoding.

I. INTRODUCTION

At present, there are large amounts of information used for controlling equipment and passenger services. Since the number and type of information is growing, there is an urgent need for a large-capacity and high-speed information transmission system. With the further advanced development stage of onboard computer, the TCN (Train Communication Network) has also emerged, which includes the whole set of internal monitoring and control of information processing tasks.

TCN^[1] consists of MVB and WTB. MVB is the bus connecting a variety of devices inside the compartment. WTB is the train bus connecting train components. TCN supports for remote control of the car driving, passenger comfort, as well as maintenance.

II. THE TECHNICAL CHARACTERISTICS OF TCN

A. Topology

Because WTB connects to the train carriages from different sources, there are very strict definition. Two types of train-bus are defined. The use of twisted-pair line, especially as a medium UIC Wired Train Bus (WTB) and the optical fiber-based train network (FTN) bus train. Three types of train-bus type is considered in communication architecture including multi-compartment Bus (MVB), derived from inside the bus (DVB), flat-panel inside the bus (BVB).

Train Communication Network (TCN) is followed by

the structure of the OSI model, which is drawing on ISO standards. TCN includes MVB and WTB. MVB connects with a device inside the Multifunction Vehicle Bus.

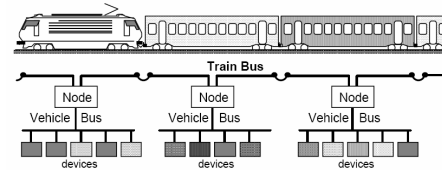


Fig.1 Train Bus and Vehicle Bus

B. Information Characteristics

TCN includes three kinds of data.

- The process of data

Process variables express the state of the train, such as speed, motor current, the operator of the order. The value of the process is called the process variable data. The transmission time is determined and bounded. Urgent process variables must be less than 100ms to be transmitted through the train-bus. To ensure that the delay time, the data is transmitted periodically. The course of less urgent data can be transmitted by the command.

- Source of data

Information is divided into small packets. these packets are confirmed number by the destination station, which are including information packets and control data associated with the formation of news data. Message data is transferred by the way of the command. Function of information is used by application layer; service information is used for train communication system of its own management.

- The management of data

The frame is short, which is used by the main equipment for the same bus with its state of calibration equipment, on-line testing equipment, transfer of sovereignty, the train early running and other management functions. Management information and

service data should not be confused, the latter restrictions are not the same bus.

C. Medium Access form

According to the different levels of bus, medium access method is divided into two broad categories.

- MVB Medium Access

MVB Bus Manager is managed by the bus ,which is the only main equipment and all other equipment are from the equipment. Main facilities are in accordance with the order of a scheduled periodic polling of the port. In the interval between two cycles, the main equipment deals with occasional request to turn. Because at the same time a number of equipment may be ready to send, occasional poll is need for a arbitration mechanism. The realization of the method is the main equipment of all equipment issued to the general poll, asked whether there were occasional data. The response of the poll are three kinds of situation: silence (no request), there is only one response (right frame), a number of response (frame error).

- WTB Medium Access

The master node of train bus is responsible for media access, and other equipment are from the equipment.Only when the main equipment are in response to polling, the arbitration need not poll. In conventional operation, the main equipment operates by the cycle, and it compartmentalizes the bus number of the basic cycle, basic cycle from several months and an occasional cycle phase. The definition of the main equipment obtains the process data by polling each node in advance of the cycle. Between the two fixed cycle time, the main equipment obtains the process data by polling the equipment.

III. MVB BUS CONTROLLER

MVBC is a new generation of MVB bus-core processors. It is independent of the physical layer and functional equipment,which provide communication interface and communications services to all equipment on the bus. MVBC internal structure is shown in figure 2 [3]. MVBC connects MVB by two redundant ,which is provided through the physical layer, and receives access control from CPU to the TM,and controls the MVBC's configuration register.Thus, the send device's data from the MVB is achieved, and MVB is managed through visiting monitor data.

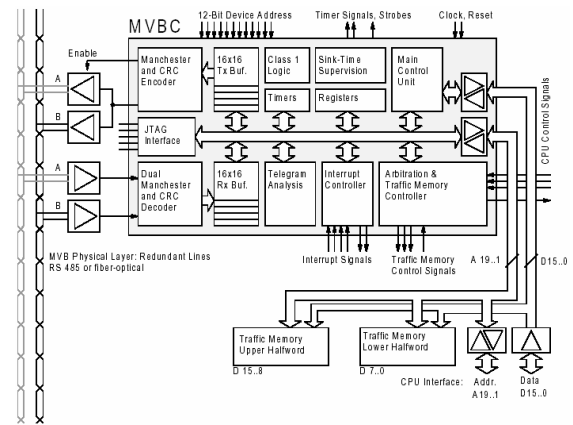


Fig.2 Internal Structure of MVBC

MVBC consists of the following modules,such as Module code (Encoder), decoding module (Decoder), input and output buffer, the array configuration register, packet analysis unit (TAU), main control unit (MCU), memory control module communication (TMC), Arbiter (ARBTRATION), address logic module (Address Logic), Class1 module,etc.

There are introduced codec module, packet analysis unit and the interrupt logic unit for analysis.

A. Main Control Unit

Main Control Unit(MCU) is the core of MVBC responsible for the scheduling of the controller. The main task is to determine the correlation between the main and slave frame,in order to determine whether the communication is error; come into being various memory access control signals and address signals, coordinate the data exchange of input and output buffer between the TM. MCU are mainly including of the main frame, producing and receiving unit, port preprocessing unit, data transmission unit, port command post-processing unit and processing unit [2].

B. Codec Module

Codec module is interface circuit between MVBC and the MVB bus. TCN standard prescript MVB bus data by transfer rate of 1.5Mbit / s, therefore the encoding module translates 16b Manchester encoding of data into a 1.5Mb / s serial data stream and sent by the main frame or slave frame form. And the decoding module receives Manchester encoded signal, and observes by detecting the signal to obtain the correct online code. When the frame is received, the module distinguishes the difference between the main frame and slave the frame,stores in the receive buffer in the RXB, and ensures that the Hamming distance is 8 by the internal error detection mechanisms.

On the figure 3 shows the main frame and the slave frame have the beginning of the definition of boundaries in TCN. The main frame in place after the start of the function has four types of code as the main frame of the type of logo.

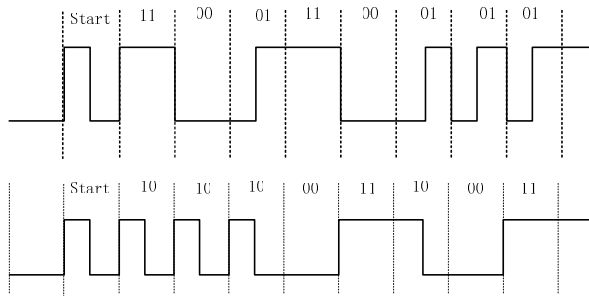


Fig.3 Start Delimiter of Mater Frame and Slave Frame

• Coding

Coding module accomplishes the following main functions, for instance, to complete the assembly of frame data, mainly unprocessed header and frame; to check by CRC; to encode follow Manchester encoding rules; final to send data.

Based on the above functions, the module include coding module, header transmitter, data transmitter, the control unit, transmitter parity-check codes, such as Manchester encoding.

CRC^{[4][5]} Check is a widely used method of error control, which is also one of the most commonly used method of channel coding. As a result of slowing by serial algorithm, it is difficult to meet the communication requirements of TCN. The parallel algorithm is used in this article. In TCN agreement, the frame of the main slave use the CRC checksum for the standard generating polynomial CRC-7 code: $G(x) = x^7 + x^6 + x^5 + x^2 + 1$.

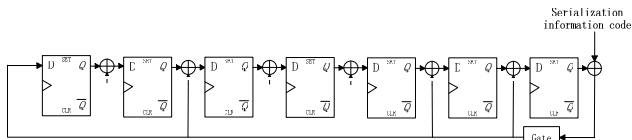


Fig.4 Schematic diagram of CRC

Manchester coding^{[6][7]} is an encoding kind of hopping along to show the binary information. The code type has a wealth of information from time to time, without the advantages of DC component, especially suitable for rapid multi-channel data switch. The following is a Manchester encoding algorithm and the realization of waveform in the use of QuartusII.

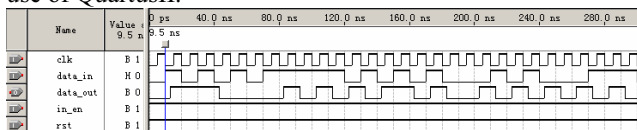


Fig.5 Using VHDL Designed Manchester encoding/decoding

• Decoding

Decoding module accomplishes the following main functions, for instance, to complete the frame of data to determine the start bit, data sampling, data decoding and data transfer functions; to determine the type of frame data, extract data from the frame and deposited in the receiving buffer; the

final to realize CRC checkout and to receive status reports. The state transition diagram of decoding controlling unit is shown in Fig.6^[8].

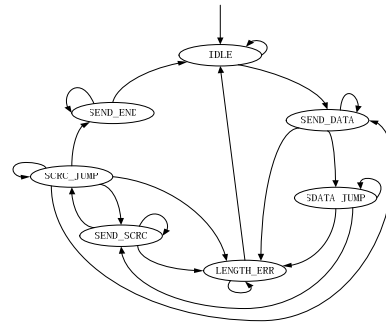


Fig.6 State transition diagram of decoding controlling unit

For the decoding module, the synchronous detection is the key. Only detected synchronization information, decoding cycle began. MVBC data have frame synchronization and bit synchronization word: the main frame and the slave frame have the header and the end of frame synchronization information; and data encode by using Manchester encoding, which contains synchronization information by itself. By determining the type of frame header can be judged.

The state transition diagram of Main frame's and slave frame's start delimiter detecting is shown in figure 7, 8^[9].

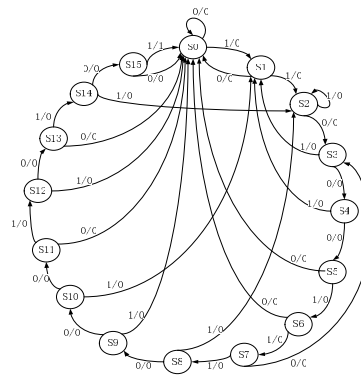


Fig.7 State transition diagram of master frame start delimiter detecting

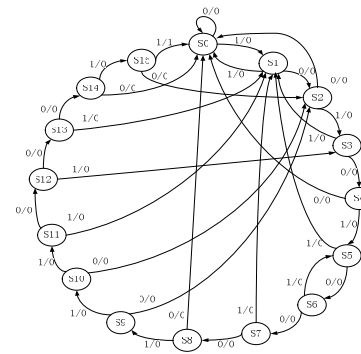


Fig.8 State transition diagram of slave frame start delimiter detecting

C. Communication and memory access control module

Controller stores communication data in Traffic Memory (TM), and communicates with the CPU through the TM. The data are including the definition of the three types of data, such as, process data, manage data and information data. TM must provide data, address, control, interrupt and other signals for the CPU access.

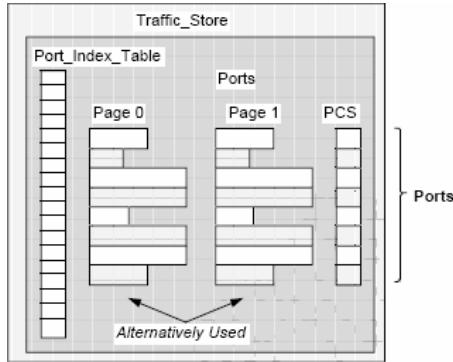


Fig.9 Chart of TM

Access Control and TM modules (TMC) receive visit request from various ports of the main MCU and CPU to realize the communication between link layer and network layer. Address logic is controlled by the TMC, and achieves the address resolution and decoding of the MCU to visit TM, as well as realizes encoding and decoding the address of CPU to visit TM and the configuration register. The array of internal registers realize not only MVBC reading and writing each bit configuration register, and the CPU reading and writing each register, but also the need, such as disruption of the logic of automatic status updating and other functions.

IV. SUMMARY

In this paper, MVB Bus FPGA-based controller design are realized ;Through using of VHDL programming language, codec Manchester, CRC check functions are achieved. As a result of the software design of hardware system, the designs are not only very flexible when need to be modified, but also

are conducive when updates in the future, which provides a convenience to popularize the TCN.

ACKNOWLEDGEMENT

The work described in this paper has been supported by National Natural Science Foundation of China (60964004) and Foundation of East China Jiaotong University (09DQ03).

REFERENCES

- [1] IEC61357-1-1999, Part 1: Train Communication Network [S].
- [2] Y Cai. Multifunctional compartment bus controller (MVBC) Research and Design [D]: master's thesis. Chengdu: Southwest Jiaotong University, 2005.
- [3] Q.F. Li. Research and design of the new generation of MVBC[D]: master's thesis Chengdu: university of electronic science and technology of China, 2005
- [4] S.M. Jin, J.L. Wang. FPGA-based realization of CRC encoder [J]. Modern electronic technology, 2005, (24) :18-22.
- [5] S.G. Zhang, S.N. Zhang, S.T. Huang. CRC Check the FPGA to achieve parallel computation [J]. Computer Technology and Development, 2007, (2) :26-62.
- [6] W.D. Jiang, etc. Based on the VHDL language, multi-purpose vehicle bus encoder design and analysis [J]. Railway communications signal engineering, 2008, (10), 9-12.
- [7] L. Fu, Z.P. Ren, C.J. Liu. Manchester coding technology based on FPGA design [J]. Modern electronic technology, 2007, (17) :55-59.
- [8] H. Li. The Design of Class 1 MVB Device Controller Based on FPGA[D]. DaLian: Dalian University of Technology, 2006.
- [9] Q.R. Xing. The Design of Class 2 MVB Device Controller Based FPGA[D]. Nanchang: East China Jiaotong University, 2009.