Improved Modulation Strategy Using Dual Phase Shift Modulation for Active Commutated Current-Fed Dual Active Bridge

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***Abstract*—This paper proposes dual phase shift modulation (DPSM) for active commutated current-fed dual active bridge for low-voltage (LV) high-power application to improve the performance of the converter at light loads. The proposed DPSM uses an additional control variable to actively control the peak current in the converter that helps to improve the performance as compared to simpler single variable but unregulated peak current control, phase shift modulation (PSM). The control variables are chosen such that the excess current is just enough to achieve zero current switching (ZCS) turn-off of the LV devices. In the reverse direction, the converter is a full-bridge converter with *LC* filter. The implementation of the conventional PSM to the full bridge, popularly known as phase-shift full bridge is simple but restricted by the zero voltage switching (ZVS) range. The proposed DPSM is implemented in the reverse direction to maintain the ZVS turn-on of the high-voltage (HV) devices even at very light loads by utilizing the LV devices instead of using them only for synchronous rectification. At higher loads where achieving ZVS is relatively easy, the modulation shifts to conventional PSM to reduce the circulating current and the associated duty cycle loss. The improvement in the performance is validated experimentally with a 1-kW prototype developed for a 30% variation in the LV voltage (42–56 V) for both directions of operation. The control of the peak current improved the efficiency by 12% from the conventional PSM at 10% load at the highest current (42 V) in the forward operation. In the reverse direction, the ZVS turn-on for the HV devices is achieved even at 6% load by the proposed modulation at the highest voltage (56 V). Thus, the proposed DPSM is a software-only solution that does not require any additional active or passive components, offering an improved performance while maintaining a low component count and simplicity of the power electronics circuit.**

***Index Terms*—Active clamp, bidirectional converter, clamping diodes, current-fed dual active bridge (CFDAB), dual phase shift modulation (DPSM), phase shift full bridge (PSFB), phase shift modulation (PSM), secondary-side modulation.**

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I. Introduction

THE Dual Active Bridge (DAB) has been an appealing topology for bidirectional power conversion applications with galvanic isolation [1]. It can also be used for multiport operation that enables interfacing multiple dc sources and loads using a single converter [2]. The DAB converter utilizes the leakage inductance of the high-frequency transformer as the power transfer element, therefore, increasing the power density with simple control requirements. However, dc sources such as the energy storage, fuel cells, or renewable sources have wide voltage variations, which results in limited zero voltage switching (ZVS) range and high circulating current especially at light loads. To ensure soft switching over the entire load range, complex modulation with three or more control variables have been suggested [3]–[6]. This, however, makes the controller implementation complex and requires offline optimization and look-up table to select the best possible combination of the variables.

Owing to the lower input current ripple, high step-up ratio, efficient operation over a wide input range as required by the energy storage, and the dc input current controllability, the current-fed DAB (CFDAB) is a good alternative compared to voltage-fed DAB (VFDAB) [7]. Also, the input boost inductor reduces the input current *di/dt*, which reduces the electromagnetic interference (EMI) and allows the use of a small dc-link capacitor. Fig. 1 shows the circuit diagram of a CFDAB. The main drawback of this topology has been the voltage spike across the turning off devices. This is due to the nonzero parasitic inductance at the switching node because of the unavoidable nonidealities, such as the PCB trace inductance and the leakage inductance of the transformer. When the devices are switched, the boost inductor is in series with this leakage inductance and the boost inductor forces the latter current to match with it. This abrupt change in the current through the leakage inductance creates a huge voltage spikes across the turning off switches, which can be catastrophic to the MOSFETs. A common solution is to use an active clamp circuit to suppress the voltage spike [8]–[10]. Xiao and Xie [8] utilizes an active clamp circuit in the current-fed half-bridge topology with phase-shift plus PWM to achieve ZVS in the low-voltage (LV) switches and voltage balancing across the transformer. However, additional two active switches along with a clamping capacitor are used, which increases the

components count and losses associated with it. Sha *et al.* [9] utilizes the phase-shift plus symmetrical dual PWM to control the power flow and balance the transformer voltages. However, the converter is unidirectional and for very large voltage difference between ports, this modulation is not suitable as either the duty required for voltage balancing is very high or the turns ratio is high. Shi *et al.* [10] implemented two H-bridges (HBs) with current source side clamped by a capacitor. A detailed analysis on the optimal selection of the variables is given to ensure minimal RMS current instead of minimum peak current by voltage balancing modulation. However, the optimized operating points varies from application to application that makes it more complicated than minimum-peak-current-mode.

Reimann *et al.* [11] first proposed the idea of utilizing the high-voltage (HV) devices for LV active current commutation. This is an effective solution because the voltage spike was avoided without using any additional switching or passive components. The commutation time is predetermined such that the current through the LV devices just reaches zero at the switching instant making the boost current equal to the series inductor current for every load condition. This avoids the reverse recovery issue of the LV devices but the HV devices are hard switched. Also, the LV devices lose soft switching at light loads since the commutation time calculated might not enough for zero current turning off. Similar concept known as secondary-side modulation technique where the HV switches are modulated to avoid the voltage spike in the LV side is implemented in [12] and [13]. The HV switches are utilized to force the current through the commutating LV devices to a negative value instead to ensure natural turn off of the device when the current reaches zero through the body diode. This helps avoid the voltage spike by achieving zero current switching (ZCS) turn-off of the LV switches and the body-diode conduction in the HV side helps achieve ZVS turn-on in the HV switches. Hence, the voltage spike is avoided with soft-switching on both the bridges without any additional component. In [12] and [13], the LV duty is varied to regulate the output power and the HV duty is dependent on the LV duty to achieve secondary-side modulation. It is a single variable control with one independent control variable. It is similar to the single variable phase shift modulation (PSM) discussed in this paper. The phase shift is chosen as the independent variable in this paper instead of the LV duty to make the analysis of the CFDAB simpler and more intuitive.

The implementation of the single control variable to regulate the power transfer makes the body diode current unregulated. It is fixed irrespective of any load change. This results in a higher RMS and peak current in the converter at lights loads and poor performance because the peak current is many times higher than the average load current.

This paper proposes dual PSM (DPSM) with an aim to actively control the diode current at different loads by utilizing an additional independent variable. In this modulation, along with the phase shift φ, the phase difference between the legs in the HV side (α_s) is varied too. α_s regulates the peak diode current at different loads such that the current is just sufficient to forward bias the body diodes of the LV switches and φ is decided based on the output power transfer required. The modulation proposed

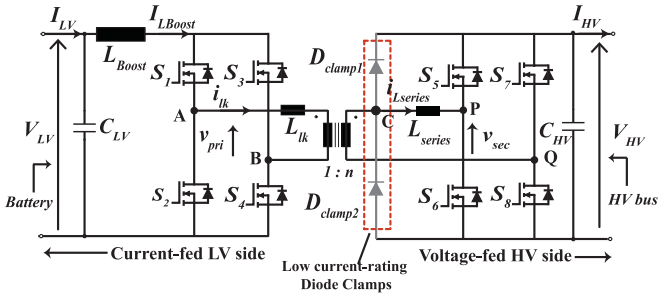

Fig. 1. Circuit diagram of CFDAB dc/dc converter with the diode clamp circuit.

is simple and easy to implement and yet significant improvement in the performance is achieved. The idea of using more than one control variable to improve the performance of the converters with capacitive filter is reported in previous literature [6], [14], [15]. The topology discussed here has an inductive filter at the LV bridge and this makes the converter significantly different. Also, the active commutation implemented here makes the analysis different from those earlier reported current-fed topologies with clamp circuits. Hence, even though similar modulation techniques such as DPSM or Triple PSM are reported in the existing literature [5] and [6], they are not directly applicable for the present topology studied in this paper.

The CFDAB is a full-bridge converter with an *LC* filter in the reverse direction (see Fig. 1). The phase shift full-bridge (PSFB) converter with PSM in the HV side and synchronous rectification in the LV side has been one of the most widely implemented converters in various high-power applications. It is because of the simplicity in its control; inherent ZVS ability by utilizing the circuit parasitics, which reduces the EMI issues; and the simple circuitry without any additional components, which helps increase the power density [16], [17]. However, the ZVS range is limited and is load dependent for the lagging leg. If the series inductor is increased to extend the range, the excess energy stored leads to higher circulating current at higher loads and reduced effective duty limiting the maximum power transfer possible.

An alternate approach proposed in this paper to extend the ZVS range till very light load condition is to actively control the LV MOSFETs instead of using them only for synchronous rectification. The idea is to turn ON the diagonal LV MOSFETs' channels before their antiparallel body diodes are turned ON by controlling the phase shift between the bridges φ. This is achieved by implementing the DPSM. The backflow of the current due to the channel conduction increases the energy stored in the series inductor and thus, extends the soft-switching range of the converter with a reduced series inductance.

At higher loads where achieving ZVS is relatively easy, conventional phase shift with synchronous rectification has higher efficiency as compared to the proposed controlled rectification. Thus, a hybrid modulation technique with active rectification at lower loads and synchronous rectification at higher loads is proposed to utilize the advantages of both the modulations and achieve an overall improved performance.

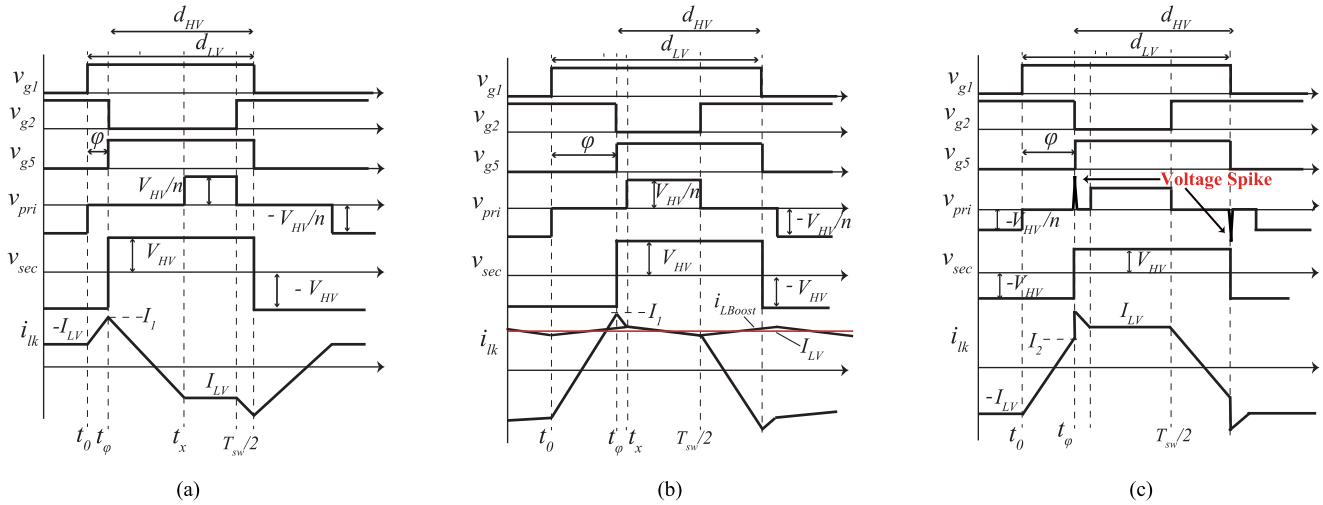

Fig. 2. Basic operating waveforms for PSM with fixed HV duty ($d_{\rm HV} = 0.5$) and LV duty $d_{\rm LV} = (0.5+\varphi)$: (a) Mode I: $0 < \varphi \leq x/2$ and $P \leq 0$, (b) Mode II: $x/2 < \varphi < \varphi_{\max}$ and $0 < P \leq P_{\max}$, (c) Mode III: $\varphi_{\max} < \varphi < 0.5$ and $P > P_{\max}$.

The paper is organized as follows: Section II details the basic architecture of the CFDAB. Section III describes the basic operation of the conventional PSM. Section IV proposes DPSM and is compared with the conventional PSM in Section V. Section VI proposes DPSM for the reverse direction of the operation to extend the ZVS range for light-load conditions and experimental results are included in Section VII.

II. Topology Description

The basic CFDAB converter schematic is shown in Fig. 1. The converter consists of two HBs with a current source on the LV side and a voltage source on the HV side, connected through an ac link. The ac link comprises of a HF transformer with leakage inductance $L_{\rm lk}$. External series inductance $L_{\rm series}$ is connected in series to achieve the required total inductance for the power transfer. The power transfer is considered positive ($P > 0$) for power flow from the LV to the HV side (forward direction of operation) and negative ($P < 0$) for power flow from the HV to the LV side (reverse direction of operation). The $L_{\rm Boost}$ helps boost the voltage during forward direction operation and works as a filter to smoothen the current when power flows in the opposite direction. For convention, the directions of the currents shown in Fig. 1 are for ($P > 0$) and a negative sign is assumed when discussed about the operation in the reverse direction.

The switches in the LV side are operated at duty ratio $d_{\rm LV}$ greater than $> 50\%$ for additional voltage gain through the boost inductor $L_{\rm Boost}$ when $P > 0$. The voltages $v_{\rm pri}(t)$ and $v_{\rm sec}(t)/n$ on the LV and the HV side of the transformer, respectively, appear across the total series inductance $L_T = (L_{\rm lk}+L_{\rm series}/n^2)$, which determines the magnitude and the direction of the power flow. The phase shift (φ) between the LV and the HV bridges and the phase difference (α_s) between the legs in the HV side alter the voltage appearing across the total series inductance and thus, influence the power transfer. The switching frequency $f_{\rm sw}$ ($1/T_{\rm sw}$) is kept fixed for the entire operating range.

It is well known that the devices on the inductive filtered bridge experience higher voltage stress. This is due to the resonance between the switches' parasitic capacitances and the series inductance. The ringing leads to higher conduction losses, a peak voltage of more than twice the blocking voltage across the devices and additional EMI issues. This parasitic ringing is observed in the active-commutated current-fed topologies because of the absence of any capacitor that can clamp the switch voltage. A clamp circuit with two low current rated ultrafast diodes are connected in the HV side as shown in Fig. 1 to clamp the switch node to the output voltage through the transformer [18]. However, a small oscillation is still observed due to the energy stored in the leakage inductance. By first-order approximation, the clamping will reduce the voltage overshoot in the ratio of the leakage and external series inductances [17]. Hence, by proper design the value of leakage inductance can be made low, which would reduce the voltage overshoot.

III. Conventional PSM

In the conventional PSM, the power transfer to the output is solely controlled by φ. It is defined as the phase shift between the gating pulses of the LV and the corresponding HV switches (e.g., between S_1 and S_5) and is expressed in p.u. To transfer power greater than zero ($P > 0$), φ should be lesser than 1/2. The duty ratio of the HV MOSFETs ($d_{\rm HV}$) is kept fixed at 0.5 and the duty ratio of the LV MOSFETs ($d_{\rm LV}$) is derived from φ and is expressed as

$$d_{\rm LV} = \varphi + 0.5. \tag{1}$$

A. Basic Operation and Power Transfer

Fig. 2 shows the basic operating waveforms of the three modes of operation in PSM for different ranges of φ. The gating signals to the diagonal switches in the LV and the HV side are the same. The gating signal to the top and bottom switches S_1 and S_2 of a leg in the LV and S_5 in the HV side are shown in Fig. 2. The gating signal to S_6 is complementary to that of S_5. $i_{\rm lk}$ is the current through the transformer in the LV side. For easier analysis and understanding of the converter operation,

the parasitic capacitances of the LV and the HV switches, the MOSFETs' body-diode reverse recovery charge and the dead time between the switches of a leg in the HV side are ignored.

Fig. 2 shows the waveform for the three modes of operation with 2(a) for $P < 0$ and Fig. 2(b) and (c) for $P > 0$. A huge voltage spike of magnitude (7–10) times the blocking voltage is observed across the LV devices and transformer as shown in Fig. 2(c) due to the mismatch between the currents at the switching instant.

The voltage across the transformer in the HV side ($v_{\rm sec}(t)$) is given by

$$v_{\rm sec}(t) = s.V_{\rm HV} \tag{2}$$

where s can be +1 or −1 depending on which pair of complementary devices are ON. s is equal to 1 if S_5 and S_8 are ON and −1 if S_6 and S_7 are ON. The LV side being current sourced, the voltage across the transformer in the LV side ($v_{\rm pri}(t)$) is current dependent and is given by

$$v_{\rm pri}(t) = \begin{cases} \frac{+V_{\rm HV}}{n}, & i_{\rm lk}(t) = i_{\rm LBoost}(t) \\ 0, & i_{\rm lk}(t) \neq i_{\rm LBoost}(t) \\ \frac{-V_{\rm HV}}{n}, & i_{\rm lk}(t) = -i_{\rm LBoost}(t). \end{cases} \tag{3}$$

Hence, to obtain $v_{\rm pri}(t) = V_{\rm HV}/n$, not just the complementary devices S_1 and S_4 should be ON, but also the series inductor current $i_{\rm lk}(t)$ should be equal to $i_{\rm LBoost}(t)$. Thus, $v_{\rm pri}(t)$ can be modeled as a current dependent voltage source.

From Fig. 2(b), it can be observed that the input boost inductor charges for a time period of t_x and discharges for $(T_{\rm sw}/2 - t_x)$. Here, x is defined as the fraction of the switching time for which the boost inductor charges. Hence, applying volt–sec balance across $L_{\rm Boost}$

$$V_{\rm LV}\, x = \left(\frac{V_{\rm HV}}{n} - V_{\rm LV}\right)(0.5 - x) \;\rightarrow\; x = \frac{1}{2}\left(1 - \frac{V_{\rm LV}}{V_{\rm HV}/n}\right). \tag{4}$$

Thus, from (4), x is dependent on the operating conditions and is independent of any control variable. With the decrease in the LV voltage $V_{\rm LV}$, the value of x increases and thus, a higher voltage gain can be obtained. Thus, CFDAB can operate for a wide range of input voltage variation, which is desired for energy storage application.

As can be observed from Fig. 2, the transformer current is periodic and symmetrical over a switching cycle. The instantaneous current $i_{\rm lk}(t)$ over a half switching cycle in Mode II is represented as

$$i_{\rm lk}(t) = \begin{cases} -I_{\rm LV} + \frac{(I_1 + I_{\rm LV})}{t_\varphi} t, & t_0 < t < t_\varphi \\ I_1 - \frac{(I_1 - I_{\rm LV})}{(t_x - t_\varphi)}(t - t_\varphi), & t_\varphi < t < t_x \\ I_{\rm LV}, & t_x < t < T_{\rm sw}/2 \end{cases} \tag{5}$$

where $t_0 = 0$. The currents I_1, I_2 and $I_{\rm LV}$ for Mode II are given in Table I. For Mode III, the current I_2 is expressed in terms of $I_{\rm LV}$. The transformer currents I_1 and $I_{\rm LV}$ in Mode I [see Fig. 2(a)] are the same as in Mode II [see Fig. 2(b)] with $I_{\rm LV} < 0$.

The power flow equation is derived by integrating the instantaneous power over half the switching cycle for Mode I and Mode II and is given as

TABLE I
LEAKAGE INDUCTOR CURRENT EQUATIONS FOR PSM AND DPSM

	PSM $0 \le P \le P_{\max}$	DPSM $0 \le P \le P_{\max}$
I_1	πx	$\pi(x - \alpha_s)$
$I_{\rm LV}$	$\pi(2\varphi - x)$	$\pi(2\varphi - x + \alpha_s)$
$I_{\rm cir}$	$2\pi(x - \varphi)$	$2\pi\{x - (\varphi + \alpha_s)\}$

Note: All currents are normalized to $I_{\rm base} = V_{\rm HV}/(nX_L)$.

$$P_{\rm p.u.} = \begin{cases} 2\pi(0.5 - x)(2\varphi - x), & \varphi < x/2; P \le 0 \\ 2\pi(0.5 - x)(2\varphi - x), & x/2 < \varphi < \varphi_{\max}; 0 < P \le P_{\max} \end{cases} \tag{6}$$

where, $P_{\rm base} = \dfrac{V_{\rm HV}^2}{n^2}\dfrac{1}{X_L}$.

The control variable φ is expressed in p.u.. $X_L = 2\pi L_T f_{\rm sw}$ represents the impedance of the power transfer element with $L_T = (L_{\rm series} / n^2) + L_{\rm lk}$. For $\varphi \le x/2$ [see Fig. 2(a)], P is negative even though $\varphi > 0$. Hence, for $P > 0$, φ should be greater than $x/2$. Equation of power transfer for Mode III is not taken into consideration since it falls beyond the operating region of the converter. $P_{\max}$ is the maximum power that the converter can transfer without entering into Mode III.

As can be observed from (6), the output power is dependent on the phase shift φ and x, given all other parameters fixed. From (4), it is clear that for the given operating conditions ($V_{\rm LV}$ and $V_{\rm HV}$), x is fixed too. Hence, the power varies linearly with the phase shift variation. Fig. 3(a) shows the plot of output power versus φ for $V_{\rm LV} = 42$ and 56 V, respectively. The plot confirms with (6) where an increase in φ linearly increases the output power for a given LV side voltage $V_{\rm LV}$. The cross sign (X) represents the boundary condition of the converter operation. Beyond that, the converter gets into Mode III region and experiences a voltage spike across the LV devices. It can be observed from the figure that as the LV voltage decreases, the maximum power that can be transferred reduces. Hence, the design parameters should be selected such that the same maximum power is transferred even for the lowest LV voltage. An important observation is that as opposed to the VFDAB where the output power follows a quadratic relation, here the relationship between the output power and the control variable is linear. This makes the controller design simpler compared to VFDAB.

B. Soft-Switching Condition Analysis

One of the major advantages of the DAB is that the parasitics in the converter (such as the leakage inductance) are used to achieve the soft switching which not only helps increase the efficiency and the power density of the converter but also solves the problems associated with the parasitics [19]. Achieving soft

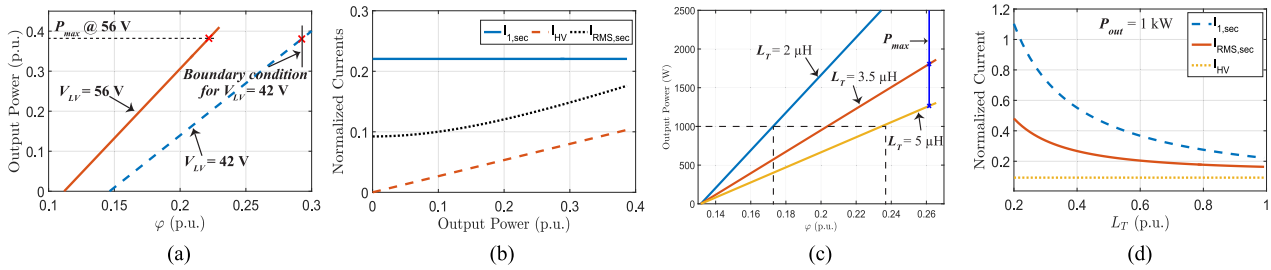

Fig. 3. Plots for PSM: (a) Output power versus phase shift (φ) for LV voltages $V_{\mathrm{LV}} = 42$ and 56 V for PSM. The cross sign (X) denote the $P_{\max}$ for different V_{LV}; (b) normalized currents for different load conditions; (c) output power versus φ for different L_T; (d) plot of normalized currents in the HV side with respect to L_T (p.u.) for $P_{\mathrm{out}} = 1$ kW. $L_{T,\mathrm{base}}$ is calculated using (15). The above plots are obtained for $V_{\mathrm{HV}} = 380$ V. The output power, φ and currents are represented in p.u.

switching is not only important for improving the efficiency of the converter but also to reduce the EMI filter requirements and improve the reliability of the converter.

LV Side: In CFDAB, if the converter loses ZCS at turn-off, a huge voltage spike will appear across the LV devices and the primary side of the transformer. The peak of the voltages can be as high as (7–10) times the blocking voltage of the devices for a very short duration of time. This high *dv/dt* across the device can damage the MOSFETs and thus, reduce the reliability of the converter. Hence, ZCS turn-off in the LV side is a necessary condition to be met for CFDAB.

From Fig. 2(c), we observed that if $i_{\mathrm{lk}}(t) < i_{\mathrm{LBoost}}(t)$ at the instant the LV diagonal switches S_2 and S_3 are turned OFF, i.e., at $t = t_\varphi$, it results in a voltage spike of amplitude corresponding to the energy due to the difference in the magnitude of i_{LBoost}(t) and $i_{\mathrm{lk}}(t)$. This thus puts a necessary constraint on the converter operation. At any point of time it should be ensured that the converter operates below the boundary region. Thus

$$I_2 \geq I_{\mathrm{LV}}. \tag{7}$$

Note that here the ripple in i_{LBoost} (t) is ignored. The currents are normalized to I_{base}. Substituting the values of I_2 and I_{LV} of PSM from Table I, the maximum value of the control variable is

$$\varphi \leq x \longrightarrow \varphi \leq \frac{1}{2}\left(1 - \frac{V_{\mathrm{LV}}}{V_{\mathrm{HV}}/n}\right). \tag{8}$$

The above equation is obtained by substituting (4) into the above equation. Hence, the maximum value of the control variable is dependent on the operating conditions of the converter and the turns ratio. $\varphi_{\max}$ in Fig. 2 corresponds to the maximum value of (8) for a given operating condition. Using (6)–(8), the maximum output power possible is given by

$$P_{\mathrm{p.u.}} \leq \pi x(1 - 2x) \tag{9}$$

with output power expressed in p.u. The output power corresponding to the cross sign in Fig. 3(a) is the maximum value of the above equation. Note that the above equation is derived considering a lossless system with $P_{\mathrm{in}} = P_{\mathrm{out}}$. Thus, the maximum power ($P_{\max}$) that the converter can deliver without risking the voltage spike and the failure of the MOSFET is decided by the operating conditions of the converter and the design parameter. The range of the control variable φ such that $0 < P \leq P_{\max}$ is given from (6), (9) as

$$x/2 < \varphi \leq x. \tag{10}$$

HV Side: Achieving ZVS for the HV MOSFETs during $P > 0$ is easy because the HV bridge is used mostly for the rectification and the current flows from drain to source for a short period of time. There are different methods, such as, current-based method and energy based (EB) [20] method, to determine the ZVS condition of the converter. The necessary condition to ensure that the current flows through the parasitic body diodes of the transistor before the current flows through its channel is given by EB method as

$$\frac{1}{2}L_T\, i_{\mathrm{sw}}^2 > y\frac{1}{2}C_{\mathrm{oss},r}(v_{\mathrm{ds}})\frac{V_{\mathrm{HV}}}{n}^2 \tag{11}$$

where $C_{\mathrm{oss},r}$ is the secondary transistor capacitance reflected to the primary side and $L_T = L_{\mathrm{series}}/n^2 + L_{\mathrm{lk}}$. The term y in the equation indicates the number of capacitors involved in the energy transaction. Since, S_5 and S_8 are discharging to zero and S_6 and S_7 are charging to the V_{HV} rail at the same time, $y = 4$. The current at the switching instant $i_{\mathrm{sw}} = I_1$. Due to the reverse flow of the current from the HV capacitor into the converter before the switching, the inductor current (I_1) is at its peak and greater than I_{LV} at the switching instant and thus, are turned ON with ZVS for all load conditions. Since the current in the inductor is large, the time taken for the capacitors to change to the opposite rail is small. The dead time can be approximated to

$$t_{\mathrm{dead}} = y\frac{Q_{\mathrm{coss}}}{I_1/n} \tag{12}$$

where Q_{coss} is the charge required for the voltage transition of an HV device. The above equation assumes that the series inductor current $i_{\mathrm{lk}}(t)$ is constant during the entire voltage transition. Even though in practice these values change during the transition because of the *LC* oscillation between the switch capacitances and the series inductance, it is but a good approximation and avoids the cumbersome calculations if the sinusoidal change is included.

C. Transformer RMS and Circulating Current

Table I enlists the currents through the converter in PSM. The equations for currents I_1 and I_{LV} are the same for Modes I and II with the sign of I_{LV} reversed for Mode I. The current that

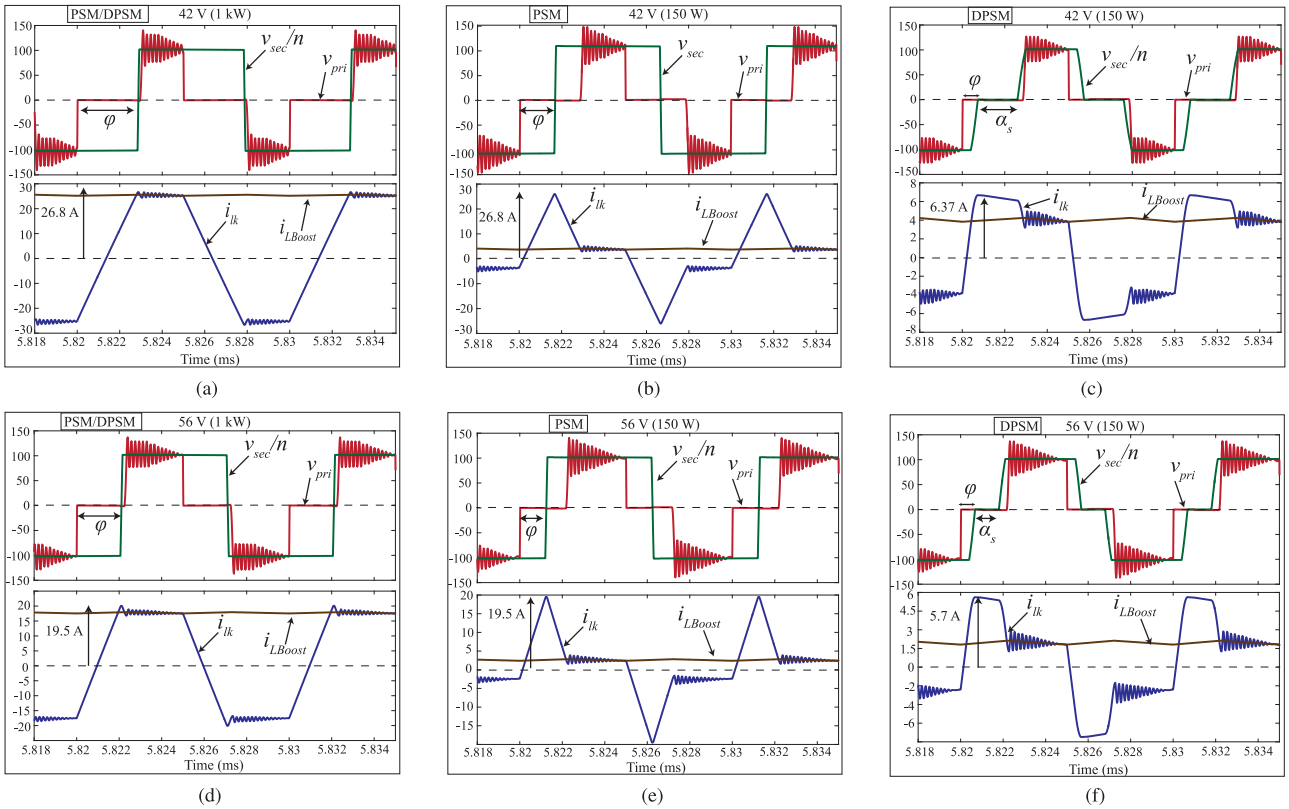

Fig. 4. Simulation results for: 42 V $V_{\rm LV}$ (a) PSM/DPSM at 1 kW; (b) PSM at 150 W; (c) DPSM at 150 W and 56 V $V_{\rm LV}$ (d) PSM/DPSM at 1 kW; (e) PSM at 150 W; (f) DPSM at 150 W. The above plots are for $V_{\rm HV} = 380$ V, $L_T = 5.57$ μ H, and $n = 3.75$.

contributes to the circulating current in the converter is given by

$$I_{\rm cir} = I_1 - I_{\rm LV}. \tag{13}$$

$I_{\rm cir}$ is due to the current transferred from the HV capacitor ($C_{\rm HV}$) into the converter that aids in the HV and LV soft switching. For a given output power, the circulating current in the converter is decided by the peak current I_1. Higher the value of I_1, higher is the circulating current available for soft switching in the converter. From Table I and Fig. 3(b), it is clear that I_1 is constant for given operating conditions irrespective of any power level. The theoretical calculation can be validated through simulation results given in Fig. 4 for full load (1 kW) and 150 W at 42 and 56 V $V_{\rm LV}$ with PSM. As can be observed, the peak of the current $i_{\rm lk}(t)$ is constant for a given LV voltage irrespective of the output load. This results in higher current available for soft switching than that required specially at lighter loads. The increased circulating current in the converter means higher LV switches' body diode conduction which not only results in increased conduction losses but also incurs higher reverse recovery losses thus, affecting the performance of the converter. Also, the reverse recovery of the antiparallel diodes result in a voltage across the switch higher than the blocking voltage $V_{\rm HV}/n$. This requires for LV switches of higher voltage rating, which usually have higher $R_{\rm ds,on}$.

The RMS current in Mode II is obtained by integrating (5). At lighter loads, to compensate for the higher backflow of the current, higher real power is drawn from the source that leads to higher RMS current through the transformer and the switches. Fig. 3(b) shows the plot of the average output current $I_{\rm HV}$ and the transformer RMS current $I_{\rm RMS,sec}$ for different output powers for a given LV voltage, i.e., $V_{\rm LV} = 48$ V and $V_{\rm HV} = 380$ V. As can be observed from the figure, the form factor ($I_{\rm HV}$ / $I_{\rm RMS,sec}$) is poor at lower loads leading to poor efficiency of the converter at light-load conditions.

From the above discussions, it is clear that it is necessary to regulate the peak current I_1 so that the current is just enough to ensure soft switching of the LV devices. This will not only increase the form factor of the converter for all load conditions, but also reduce the loss due to the LV diode conduction. Hence, the inductor current $i_{\rm lk}(t)$ should be manipulated by changing the voltage appearing across it. Since, $v_{\rm pri}(t)$ is current dependent (3), $v_{\rm sec}(t)$ needs to be changed. The conventional PSM implementing a single variable cannot simultaneously control the peak current and transfer the required power. Thus, it is necessary to introduce another independent variable to regulate the current as the output power required changes.

D. Design Considerations

As discussed in Section III-B, the operating conditions determine the maximum value of the control variables to maintain the converter in safe operation region (8). This limits the maximum power transfer possible and thus, requires the parameters L_T and n to be designed to accommodate the required maximum output power for a varying LV voltages.

In the steady state, the voltage gain through the boost inductor in the LV side is given in (4). The maximum value of x is obtained for minimum $V_{\rm LV}$ at fixed $V_{\rm HV}$. Higher the value of x, lower is the turns ratio (n) required. As can be observed from Fig. 2, the power transfer from the LV to the HV is during the time period $\Delta t = (T_{\rm sw}/2\text{-}t_x)$. Hence, for higher effective power transfer area with lower associated conduction losses, Δt should be high, which is obtained by increasing the turns ratio. This is in contrast with the advantage obtained with the input inductor-type converter and will lead to increased transformer winding losses. Also, with the increase in n $\varphi_{\max}$ decreases, which reduces the maximum achievable duty (1). This might lead to the under-utilization of the MOSFETs. Thus, there is a tradeoff between the two and the selection of the best value of the turns ratio requires a number of iterations. For the initial solution, a desirable $d_{\max}$ is selected at $V_{\rm LV,min}$ and using (1), (4), and (8), n is calculated as

$$n = \frac{2V_{\rm HV}}{V_{\rm LV,min}}(1 - d_{\rm LV,max}). \tag{14}$$

Once, the turns ratio is determined, the leakage inductance is decided based on the maximum power that needs to be transferred. Using (9)

$$L_T \leq \frac{V_{\rm HV}^2}{2n^2 f_{\rm sw} P_{\rm max,ZCS}}\{x_{\max}(1 - 2x_{\max})\}. \tag{15}$$

The total series inductance should be enough to transfer the maximum required power for the minimum LV side voltage ($V_{\rm LV,min}$). As can be observed from Fig. 3(c), the maximum output power transfer possible increases with the decrease in the value of L_T. However, as L_T reduces, the converter becomes more sensitive to the change in φ as shown in the figure. This requires a very precise control of φ, which might be difficult to implement in the digital platform. However, large L_T takes longer time to change the current direction and thus reduces the effective area of the power transfer, also known as the duty cycle loss.

In terms of the RMS currents, a closer observation of the Mode II operation of PSM (see Table I) shows that $I_{1,p.u.} \propto x$, which is dependent on the operating conditions only. Hence, a decrease in L_T results in an increase in the peak current I_1, which increases the effective RMS current in the converter. Fig. 3(d) shows the plot of the variation of the peak and the RMS current of the transformer reflected to the HV side with respect to L_T at 1 kW. Note that the series inductance is normalized to $L_{T,\max}$ given in (15) and the currents are normalized to $I_{\rm base}$. For lower value of L_T, the peak current can be around ten times the HV current $I_{\rm HV}$. Hence, the minimum value of the inductor is limited by the maximum peak current allowed and is given by

$$I_1 < mI_{\rm LV}$$
$$L_T > \frac{V_{\rm LV,min}V_{\rm HV}}{2nf_{\rm sw}(mP_{\rm max,ZCS})}x \tag{16}$$

where m represents the percentage of the input current. Assuming a lossless system, $P_{\rm in} = P_{\rm out}$, $I_{\rm LV} = P_{\rm max,ZCS} / V_{\rm LV}$. Also, the lower limit of L_T is determined by the ZVS condition. Even though the ZVS condition is maintained for the HV devices till no-load for $P > 0$, L_T should ensure ZVS in the reverse direction as well. Hence, the selection of L_T should be a compromise between the conduction losses, soft-switching range, and the size of the external series inductance.

IV. DUAL PSM (DPSM)

From the discussions in the earlier sections, in order to reduce the backflow power, $v_{\rm sec}(t)$ should not be confined to square wave with 50% duty ratio. As discussed in [3], the three step voltage in HV side reduces the circulating current. Hence, similar concept is being implemented for current-fed case. In the proposed modulation technique for CFDAB, the power transfer is controlled by φ and α_s. φ is defined as the phase shift between the gating pulses of the LV and the corresponding HV switches and α_s is defined the phase difference between the diagonal switches in the HV side, i.e., between S_5 and S_8. All the variables are expressed in p.u. The HV legs corresponding to S_5–S_6 and S_7–S_8 are the leading and lagging legs, respectively. For positive power transfer, (α_s+φ) should be less than 0.5. The duty of the HV switches ($d_{\rm HV}$) is kept fixed at 0.5 and the duty of the LV switches ($d_{\rm LV}$) is given by (1) ($d_{\rm LV} = 0.5 + \varphi$).

A. Basic Operation and Power Transfer

Fig. 5 shows the basic operating waveforms of the CFDAB for the proposed modulation for different mode of operation for different ranges of φ and α_s. The switches in the same leg are driven in complementary in the HV side. The assumptions made for the analysis are the same as mentioned for PSM.

Fig. 5(a) shows the waveform for $P < 0$. Fig. 5(b) and (c) shows the waveforms for $P > 0$ but without and with voltage spike. As can be observed from the figures, the phase shift α_s between the diagonal switches in the HV, i.e., between S_5 and S_8 shorts the secondary winding of the transformer and thus, introduces a zero state in $v_{\rm sec}(t)$ making it three level similar to $v_{\rm pri}(t)$. The HV side transformer voltage is given as

$$v_{\rm sec}(t) = s.V_{\rm HV}$$
$$\text{where } s = \begin{cases} \pm 1, & \text{diagonal switches ON} \\ 0, & \text{switches on the same side ON} \end{cases} \tag{17}$$

s is +1 if S_5 and S_8 are ON and -1 if S_6 and S_7 are ON. The LV side transformer voltage is dependent on the current in the converter and is given in (3). The instantaneous current $i_{\rm lk}(t)$ over half a switching cycle in Mode II is given as

$$i_{\rm lk}(t) = \begin{cases} -I_{\rm LV} + \frac{(I_1 + I_{\rm LV})}{t_\varphi}t, & t_0 < t < t_\varphi \\ I_1, & t_\varphi < t < t_c \\ I_1 - \frac{(I_1 - I_{\rm LV})}{(t_x - t_c)}(t - t_c), & t_c < t < t_x \\ I_{\rm LV}, & t_x < t < T_{\rm sw}/2 \end{cases} \tag{18}$$

where $t_0 = 0$, t_c is given as $(\varphi + \alpha_s)/f_{\rm sw}$. The current equations for Mode I and Mode II are the same with $I_{\rm LV} < 0$ in Mode I. Note that the expressions for I_1, $I_{\rm LV}$, and I_2 are different for DPSM as compared to PSM. Table I enlists the expressions for

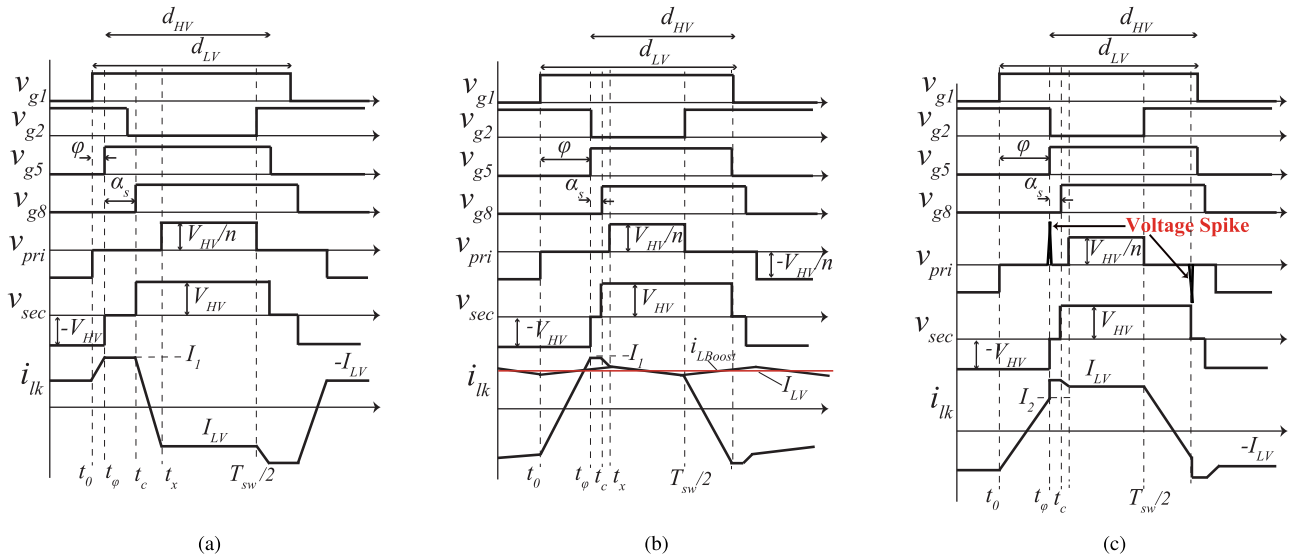

Fig. 5. Basic operating waveform of DPSM with fixed HV duty ($d_{\rm HV} = 0.5$), LV duty $d_{\rm LV} = (0.5+\varphi)$: (a) Mode I: $0 < \alpha_s < (x- 2\varphi)$ and $P \leq 0$, (b) Mode II: $(x- 2\varphi) < \alpha_s \leq (x-\varphi)$ and $0 < P \leq P_{\rm max}$, (c) Mode III: $(x-\varphi) < \alpha_s$ and $P > P_{\rm max}$.

currents for DPSM. For Mode III, I_2 can be expressed in terms of $I_{\rm LV}$. The operation of the converter in Mode II and the voltage spike observed in Mode III are discussed in this section.

Fig. 6 illustrates the theoretical waveforms and the equivalent circuit diagrams of the converter in Mode II implementing DPSM for half the switching cycle.

Interval I (t_0–t_φ): All the LV switches S_1–S_4 are ON providing separate paths for the boost inductor current $i_{\rm LBoost}(t)$ and the leakage inductor current $i_{\rm lk}(t)$ similar to the conventional PSM. On the HV side, the current through S_6 and S_7 changes its direction during this mode. The voltage across the transformer is zero in the LV side since the currents are not equal (3). By the end of this interval, $i_{\rm lk}(t) > I_{\rm LV}$.

Interval II (t_φ–t_c): The switches S_1 and S_4 carry $i_{\rm LBoost}(t)$ and the excess current in $i_{\rm lk}(t)$ forward biases the antiparallel diodes of S_2 and S_3. Unlike conventional PSM, this interval introduces a zero state in $v_{\rm sec}(t)$, which helps reduce the peak value of the transformer current $i_{\rm lk}(t)$. Hence, instead of turning ON the switch S_8, S_7 is kept turned ON for α_s / $f_{\rm sw}$ time period.

Interval III (t_c–t_x): This interval begins with the turning ON of S_8. The secondary transformer voltage is increased to $V_{\rm HV}$ (17) and hence, the current through $i_{\rm lk}(t)$ gradually reduces to $I_{\rm LV}$. The reverse bias of the antiparallel diodes of S_2 and S_3 mark the end of this interval.

Interval IV (t_x–$T_{\rm sw}/2$): This is the power transfer interval in this half switching cycle. Fig. 6(h) shows the equivalent circuit diagram of the converter in this interval. The transformer current $i_{\rm lk}(t) = I_{\rm LV}$ thus, increasing $v_{\rm pri}(t)$ to $V_{\rm HV}$ / n. The rest of the cycle is a repetition of this half-cycle.

Voltage-spike in Mode III: Fig. 7 shows the difference between Mode II and Mode III operation for the proposed DPSM. The theoretical waveforms along with the equivalent circuit diagrams are shown for before and after the switching time instant $t = t_\varphi$. For $0 < t < t_\varphi$, all the LV switches S_1–S_4 and HV switches S_6 and S_7 are ON as shown in Fig. 7(a), which is the same as interval I in Mode II operation. At time instant $t = t_\varphi$, the LV switches S_2 and S_3 and the HV switch S_6 are turned OFF [see Fig. 7(c)]. At the switching instant, the current $i_{\rm lk}(t)$ is still lesser than $i_{\rm LBoost}(t)$. Since, S_1 and S_4 are the only conducting switches in the LV, the larger boost inductor forces the smaller total series inductor to match its current to $i_{\rm LBoost}(t)$. Thus, $i_{lk}(t)$ increases from I_2 to $I_{\rm LV}$ almost instantaneously and the energy corresponding to the difference in the currents appear across the parasitic capacitors of the blocking LV switches S_2 and S_3. Since, such high magnitude of the voltage can damage the switches and reduce the reliability of the converter, the Mode III of proposed DPSM also falls beyond the operating range of the converter.

Thus, similar to PSM, Mode II of DPSM is also the only operating region of the converter. The average output power for this Mode is given as

$$P_{\rm p.u.} = 2\pi(0.5 - x)(\alpha_s + 2\varphi - x)$$
$$\text{with, } \alpha_s > (x - 2\varphi) \text{ for } P > 0. \tag{19}$$

From Fig. 8(a), it can be observed that the output power increases linearly with the increase in α_s within the range $0 < P \leq P_{\rm max}$ for different values of φ. The gray line is the boundary condition for Mode II operation ($P_{\rm max}$) beyond which the converter enters Mode III region. As can be observed from the plot, different combinations of φ and α_s are possible for the same output power. As the output power required increases, the value of φ needs to be increased and α_s needs to be decreased to meet the required power. Once α_s decreases to zero, (19) reduces to (6) and the modulation converges to the conventional PSM. Thus, there is a smooth transition from DPSM to PSM. The smooth transition and the linear dependence of the output power on the control variables make the PI controller design easy.

B. Soft-Switching Condition

LV Side: Similar to conventional PSM, a huge voltage spike appear across the switches and the transformer in the LV side if

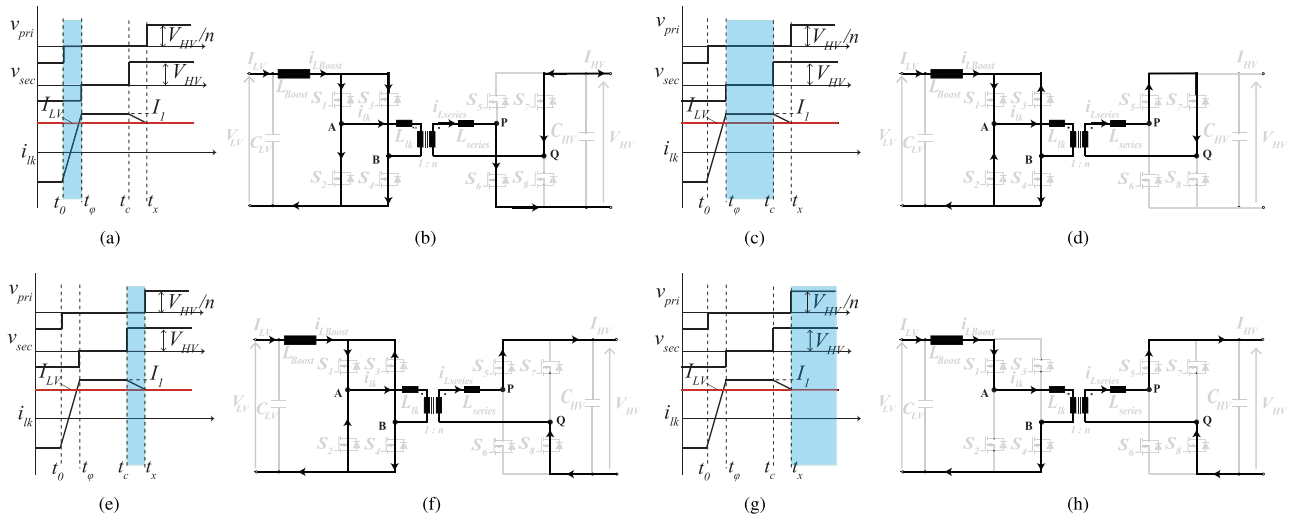

Fig. 6. Equivalent circuit diagrams for Mode II operation in DPSM: (a) and (b) Interval I (t_0–t_φ); (c) and (d) Interval II (t_φ–t_c) with $t_c = (t_\varphi + t_{\alpha s})$; (e) and (f) Interval III (t_c–t_x); (g) and (h) Interval IV (t_x–$T_{\rm sw}/2$).

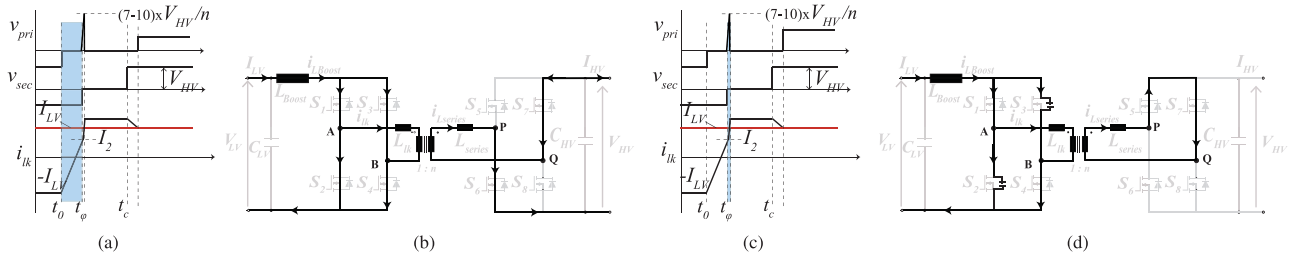

Fig. 7. Equivalent circuit diagrams for Mode III operation in DPSM: (a) and (b) Interval I (t_0–t_φ) same as Mode II; (c) and (d) voltage spike due to the turn OFF of S_2 and S_3.

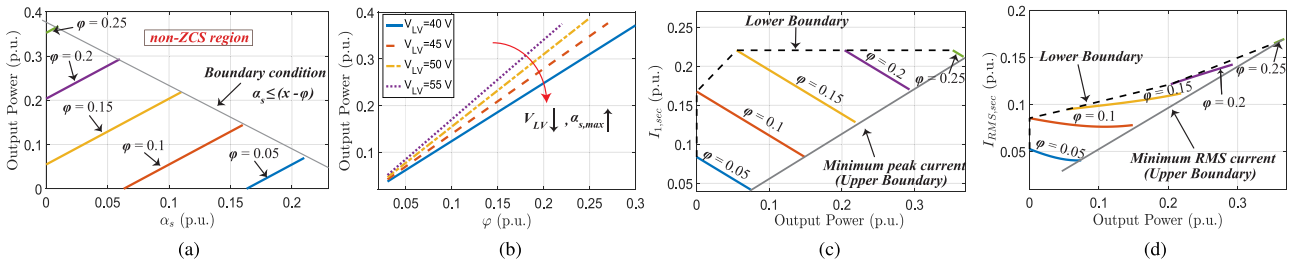

Fig. 8. Plots for DPSM in forward direction: (a) Output Power versus phase difference between the HV legs (α_s) for different phase shifts φ in the ZCS region. The solid line in gray bounds is the maximum power transfer possible for a given φ. (b) Plot of output power versus φ with $\alpha_{s,\max}$ given by (21); (c) plot of the peak current through series inductor ($I_{1,sec}$) versus output power, and (d) RMS current $I_{\rm RMS,sec}$ versus output power for different values of φ. The dashed line shows the lower boundary (19) and the solid line shows the upper boundary (21). The above plots are obtained for $V_{\rm LV} = 48$ V and $V_{\rm HV} = 380$ V.

the LV devices lose ZCS. From Figs. 5(c) and 7, we can observe that if $i_{\rm lk}(t) < i_{\rm LBoost}(t)$ when the diagonal switches S_2 and S_3 are turned OFF at $t = t_\varphi$, $i_{\rm lk}$(t) is forced to match the boost inductor current that results in a huge voltage spike across the LV devices. Hence, the necessary constraint for soft switching is given by

$$I_2 \geq I_{\rm LV}. \tag{20}$$

The currents are normalized to $I_{\rm base}$. Note that the above-mentioned constraint is the same as the conventional PSM current constraint given in (7). Substituting the values of I_2 and $I_{\rm LV}$ from Table I, the maximum value of the control value is obtained as

$$\alpha_s \leq (x - \varphi) \tag{21}$$

with x derived from (4). Using (19)–(21) for a given φ the output power should be

$$P_{\rm p.u.} \leq \pi(1 - 2x)\varphi. \tag{22}$$

The gray line in Fig. 8(a) corresponds to the maximum value of (22) for different values of φ. Below the gray line in the plot is the operating region of the converter (Mode II), which ensures ZCS of the LV switches. From (21), it can be observed that the maximum α_s possible increases with the increase in x. As can be seen from Fig. 8(a), a decrease in $V_{\rm LV}$ increases the value of $\alpha_{s,\max}$ due to an increase in x. As α_s reduces to zero at full load, the operation of the converter converges to conventional PSM. Thus, the maximum output power possible and the maximum value of control variable (φ) in DPSM is the same as PSM and is given by (9) and (8), respectively. Hence, for $P > 0$ and within the ZCS region for all operating conditions, the range of phase shift α_s is given by

$$(x - 2\varphi) < \alpha_s \leq (x - \varphi). \tag{23}$$

HV Side: The necessary condition for the ZVS in the HV side is given by (11) where $y = 2$ for DPSM. It is so because at any switching instant only one leg undergoes the voltage change. Assuming that $i_{\rm lk}(t_\varphi) = i_{\rm lk}(t_c)$ by ignoring the MOSFETs' and winding resistive losses and PCB losses, $i_{\rm sw}(t) = I_1$. $v_{\rm pri}(t) = 0$ during both the leading and lagging leg switching and hence, the energy in the total series inductor should be enough to charge/discharge the parasitic capacitors. From Fig. 5, it can be observed that all the HV switches are turned ON when the transformer current is at its peak (I_1) and is greater than $I_{\rm LV}$. Thus, the ZVS of HV devices is maintained for the entire operating range.

C. RMS and Circulating Current

Table I details the equation of currents for different modes of operation for DPSM. The currents I_1 and $I_{\rm LV}$ for Mode I and Mode II are the same even though Mode I corresponds to $P < 0$. The circulating current definition is the same as that defined in (13). In the proposed modulation, the introduction of a new variable (α_s) limits the energy exchange between the series inductor and the HV capacitor ($C_{\rm HV}$) by reducing the (t_0–t_φ) interval. From Table I, it is clear that I_1 is dependent on α_s for a given operating condition. Hence, higher is the value of α_s lower is the peak current, which reduces the circulating current in the converter. Fig. 8(b) shows the plot of the peak current reflected to the HV side ($I_{1,\rm sec}$) for different output power. As can be observed from the plot, for the same output power, different combinations of φ and α_s are possible resulting in different peak currents. But the minimum peak current is obtained at the upper boundary condition of the converter shown by the gray solid line that corresponds to $\alpha_{s,\max}$ (21). This is expected because for a given power, as the value of φ decreases, the required value of α_s increases (19). This reduces the peak current and the resulting circulating current in the converter for that output power. Also, the reduction in the peak current reduces the antiparallel diode conduction on the LV side and the associated additional losses. The lower boundary of the converter operation shown by the black dotted line in the figure corresponds to the lower limit of α_s for $P > 0$ (19). Fig. 4(c) and (f) shows the simulation results for DPSM for 150 W at 42 V and 56 V $V_{\rm LV}$, respectively. As can be observed, the peak current reduces with the decrease in the output power. This decrease in the peak current helps improve the performance of the converter.

The RMS current is derived by integrating (18). Similar to the condition for minimum peak current, the minimum RMS current at any given power is obtained at the upper boundary where $\alpha = \alpha_{s,\max}$ as shown in Fig. 8(c). The above plot is obtained for fixed operating condition with $V_{\rm LV} = 48$ V and $V_{\rm HV} = 380$ V. As the output power required increases, the value of $\alpha_{s,\max}$ decreases to zero and the modulation converges to PSM.

TABLE II
COMPARISON BETWEEN PSM AND DPSM

	PSM	DPSM
Control variables	φ	φ and α_s
Peak current (I_1)	πx	$\pi(x\text{-}\alpha_s)$
Soft switching (LV side)	$x \geq \varphi$	$(x\text{-}\varphi) \geq \alpha_s$
Soft-switching range	LV: All load till $P_{\rm p.u.} \leq \pi x(1-2x)$ HV: Entire range	LV: Vary φ such that $P_{\rm p.u.} \leq \pi\varphi(1\text{-}2x)$ for each load HV: Entire range

V. COMPARISON BETWEEN THE MODULATION TECHNIQUES

The above sections detail the conventional and the proposed modulations in terms of their basic operation and their features. This section illustrates the differences between the modulations and the improvements in the proposed modulation. Table II compares the important features of the modulation techniques.

A. RMS and Circulating Current

In the case of the conventional PSM, the energy exchange between the converter and the HV capacitor ($C_{\rm HV}$) takes place for a time period of (t_0–t_x). The entire region contributes to the circulation current. In the proposed DPSM, the introduction of the zero state limits the energy exchange but rather circulates a smaller amount of excess current inside the converter for ($t_c - t_\varphi$) period. The reduction in t_φ, thus, reduces the time period for which the power is taken from the HV capacitor, which thus reduces the peak value of the current and the corresponding circulation energy.

As can be observed from Table II, the peak current $I_1 \propto (x - \alpha_s)$ for DPSM, whereas $I_1 \propto x$ for PSM. This gives an extra degree of freedom to control the peak current in DPSM as compared to PSM. Fig. 9(a) shows the variation of the peak current reflected to the HV side ($I_{1,\rm sec}$) for different power levels for both the modulations. The peak current for DPSM is plot for the upper boundary where it is minimum for a given output power. As can be observed from the figure, a reduction of around 70% in the peak is obtained by implementing DPSM at 0.1 p.u. output power. Thus, at light-load conditions, the circulating current in the converter is reduced by the proposed modulation. The difference between the modulations decreases as the output power increases. When $\alpha_{s,\max} = 0$ at higher loads, the proposed modulation reduces to conventional PSM. The green solid line in the figure marks the change from DPSM to PSM at higher loads. Fig. 4 shows the simulation results for both the modulations at

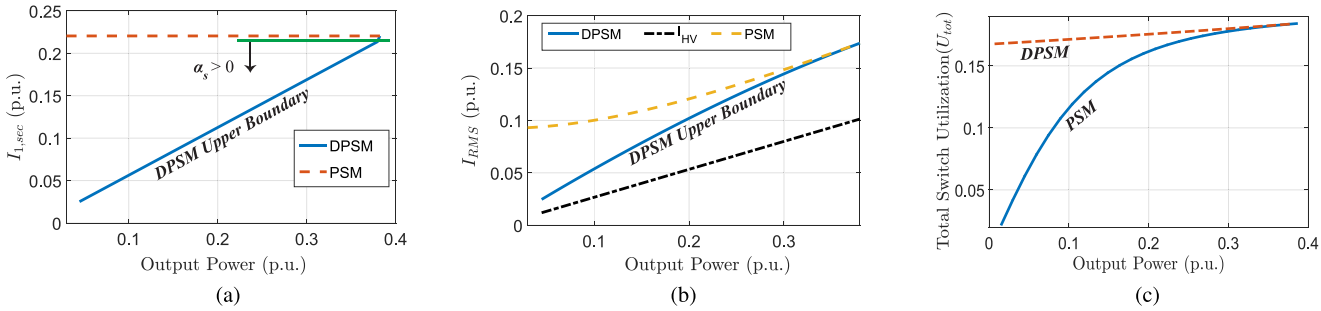

Fig. 9. (a) Plot of $I_{1,\mathrm{sec}}$ through the series inductor versus output power for DPSM (solid line) and PSM (dashed line); (b) plot of $I_{\mathrm{RMS,sec}}$ for DPSM (solid line) and PSM (dashed line) and the HV current (I_{HV}) for different output powers. The plot for DPSM is for the upper boundary condition given in (21). At around 0.37 p.u. output power, $\alpha_s = 0$ and DPSM reduces to PSM. (c) Plot of total LV switch utilization versus output power for DPSM (dashed line) and PSM (solid lines).

different LV voltages V_{LV} and output powers. At lower loads, α_s increases for DPSM because of which the peak current reduces by 76% and 67% at 150 W for 42 and 56 V, respectively, as compared to PSM.

Fig. 9(b) shows the comparison between the proposed DPSM and the conventional PSM in terms of their RMS currents. A reduction in the peak current for the proposed modulation at lower loads reduces the RMS current as compared to the PSM. This improves the I_{HV} / $I_{\mathrm{RMS,sec}}$ factor for DPSM at light-load conditions.

Thus, by introducing an additional independent variable, the RMS current is reduced at lighter loads, which improves the performance of the converter and makes it suitable for application where the output power and the LV voltage varies over a wide range.

B. Soft-Switching and Switch Utilization

The magnitude of the switch stress in PWM converters quantified as "switch stress" [21] is given for the ith switch in the converter as $S_i = V_{\mathrm{peak},i} I_{\mathrm{RMS},i}$. For a maximum output power of P_{max}, the switch utilization is given as

$$U_i = P_{\mathrm{max}}/S_i \tag{24}$$

and the total switch utilization U_{tot} is given as $P_{\mathrm{max}}/\sum S_i$. Hence, as the RMS current of the switch increases for the same output power, the switch utilization reduces. For CFDAB, $V_{\mathrm{peak}} = V_{\mathrm{HV}}/n$ in the LV side ignoring the reverse recovery of the antiparallel diodes and the effect of parasitic capacitances. Fig. 9(c) shows the plot of the total switch utilization in the LV devices for conventional PSM and the proposed DPSM for different output powers. From the earlier sections, it is clear that at lower loads, I_{RMS} in PSM is much higher than the proposed modulation, which results in poor switch utilization. In the case of DPSM, the switch utilization is rather uniform for the entire power range. Poor switch utilization leads to an increase of the total silicon area required to realize the power devices of the converter. Also, at the LV side the current is high and poor switch utilization means higher conduction losses in the switches for PSM.

The soft-switching conditions for both the modulations are given in Table II. In the case of CFDAB, it is necessary for the converter to maintain soft switching in the LV side to avoid the voltage spike as detailed in earlier sections. In the case of PSM, $P_{\mathrm{max}} \propto x$ (9) that is dependent only on the operating conditions. Thus, the soft switching is maintained for all loads lower than P_{max}. However for DPSM, $P_{\mathrm{max}} \propto \varphi$ (22) that varies for different loads. Hence, there is a possibility that the converter would lose ZCS even at lower loads if the soft-switching condition is not met in DPSM. To ensure the converter never loses ZCS and operates in Mode III, the converter is operated not at the upper boundary but rather a small margin is maintained. The soft-switching on the HV side is maintained for the entire range for both the conventional and the proposed modulation.

Thus, the proposed DPSM is implemented for the CFDAB to improve the performance of the converter at lower loads as compared to the conventional PSM. The improved performance of the converter with soft switching for the entire range of operation by the implementation of DPSM can help achieve a relatively flat efficiency profile for the converter over a wide variation of operating conditions.

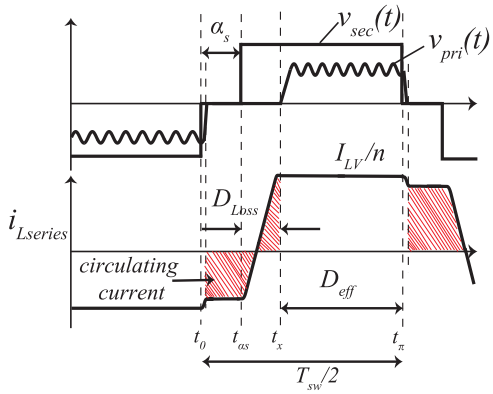

Fig. 10. Theoretical waveform for PSFB. The duty cycle loss D_{Loss} and the circulating current (shaded region) are shown in the waveform.

VI. Reverse Direction of Operation

The circulating current and the duty cycle loss D_{Loss} in the PSFB converter are shown in Fig. 10. The duty cycle loss reduces the effective duty (D_{eff}) of the LV transformer voltage.

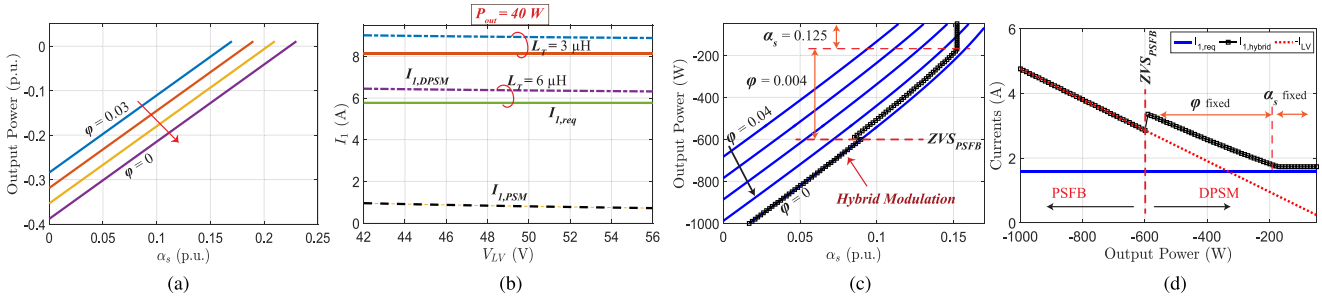

Fig. 11. Plot for DPSM in reverse direction: (a) Output Power versus α_s for different phase shifts φ in the reverse direction. $\alpha_s < (x–2\varphi)$ in this operation; (c) currents at the switching instant in PSFB and DPSM and the minimum current required for different values of L_T. The charge required is calculated based on the datasheet of IPP60R099CP; (c) output Power versus α_s for different φ and the proposed hybrid modulation, and (d) currents versus output power at 56 V $V_{\rm LV}$. The black solid line is the proposed hybrid modulation. The above plot are obtained for $V_{\rm HV} = 380$ V, and $n = 3.75$.

As the output power increases, the $D_{\rm eff}$ further decreases which means a large amount of power is transferred in a very small interval of time. This increases the circulating current through the converter. The situation is worse when the series inductance is increased to extend the ZVS range. Hence, the proposed active rectification through DPSM is implemented to extend the ZVS range with a smaller value of series inductance.

Fig. 5(a) shows the operating waveforms of the full bridge with active controlled rectification. A small phase shift (v_{g5} lagging v_{g1}) is introduced between the LV and HV bridges. The HV duty $d_{\rm HV}$ is kept fixed at 0.5 and the output power is controlled by α_s, which is defined as the phase difference between the diagonal switches on the HV side. The LV duty $d_{\rm LV}$ is maintained greater than 0.5 to utilize the MOSFET for synchronous rectification for maximum conduction period. It is derived from the independent control variables. The equations for I_1 and $I_{\rm LV}$ are the same as Mode II in the forward direction. Equation (18) gives the current equations at different intervals and the power transfer equation is given in (19) with

$$\alpha_s < x - 2\varphi, \text{ for reverse operation.} \tag{25}$$

Fig. 11(a) shows the plot of output power versus α_s for different values of φ. As the output power transfer increases in the reverse direction, the value of α_s should be decreased for a given φ. From Table I, the peak current $I_1 \propto (x–\alpha_s)$. Hence, with the increase in φ, the α_s required is reduced and thus, the circulating current in the converter increases specially at higher loads. The duty cycle loss in DPSM is given by

$$D_{\rm loss} = \frac{(I_1 - I_{\rm LV})}{V_{\rm HV}} L_T f_{\rm sw.} \tag{26}$$

Note that for reverse direction, $I_{\rm LV} < 0$. Since, the current I_1 is higher for DPSM than PSFB, the loss of duty is higher for the proposed modulation at higher loads as compared to the latter given all the design parameters are the same.

The lagging leg devices S_7 and S_8 in the HV side are ZVS turned ON if

$$I_1 > \sqrt{\frac{2Q_{\rm coss}(v_{\rm ds})V_{\rm HV}}{L_T}} \tag{27}$$

where $Q_{\rm coss}(v_{\rm ds})$ is the total charge required by the HV switch capacitor to change its voltage to opposite rail at the boundary between ZVS and non-ZVS. Fig. 11(c) shows the variation of the current available for the lagging leg transition for both the modulations with LV voltage for different values of series inductance. With the decrease in the value of the inductance, the current required to achieve ZVS increases and hence, ZVS cannot be achieved with the conventional PSM. It should be noted that the theoretical study of PSFB assumes the current at the freewheeling state is equal to the LV current. However, practically the current is lower due to the energy required in charging/discharging the LV devices' and diode clamps' capacitors. Hence, the converter loses soft switching at a higher load than theoretically calculated.

In the proposed active controlled rectification, the peak current can be regulated by modulating the control variable α_s so that the lagging leg in the HV side is ZVS turned-on even at 4% load with a small value of series inductance.

Hence, the ZVS is achieved at very light loads with the proposed DPSM with a reduced value of L_T. The decrease in the series inductance required in the controlled rectification helps reduce the effect of the series inductance in the duty cycle loss and the associated circulating current at higher loads. However, the current I_1 is higher for the proposed modulation than PSFB and thus, for given design parameters the loss of duty is higher for the proposed modulation as compared to the latter. Also, the backflow of the current in the LV side leads to higher circulating current for the proposed controlled rectification than the conventional PSFB at higher loads.

Hence, to improve the overall performance of the converter and reduce the absolute losses at higher loads, a hybrid modulation is proposed where the conventional PSM with synchronous rectification is implemented at higher loads and controlled rectification using proposed DPSM is implemented at lower loads where the conventional modulation loses ZVS.

For the low loads, different combinations of the control variables are possible for the given output power in DPSM as can be observed from Fig. 11(a). The circulating current is: $I_{\rm cir} = (I_1\text{-}I_{\rm LV}) \propto \varphi$. Hence, to reduce the loss due to the excess circulation energy in the converter, φ is kept fixed at minimum and the output power is regulated by α_s. This helps reduce the peak current I_1 which is $\propto (x–\alpha_s)$ as the output power decreases. Once the peak current is close to the minimum current required for ZVS, the current I_1 is fixed by fixing α_s and φ is varied

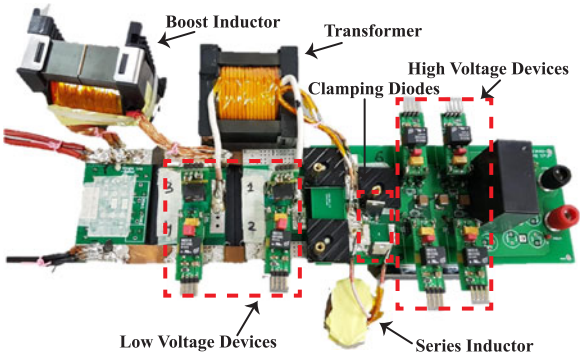

Fig. 12. Experimental prototype of the CFDAB.

TABLE III
CIRCUIT PARAMETERS OF THE CONVERTER

Descriptions	Specifications
Rated output power ($P_{\mathrm{out,max}}$)	1 kW
Input voltage (V_{LV})	42–56 V
DC-link voltage (V_{HV})	380 V
Transformer turns (n), magnetizing inductance (L_m) and leakage inductance (L_{lk})	3.75, 0.32 mH and
ETD 54, 3C90 with $N_p = 8$ of AWG 38/(660/38) and $N_s = 30$ of AWG 42/(660/42)	0.88 μH
Series inductance (L_{series}) RM12, 14 turns of AWG 42/ (660/42)	65.09 μH
Boost inductor (L_{boost}) ETD 59, 14 turns of AWG 29 (2 in parallel)	78.5 μH
LV dc capacitor (C_{LV})	100 μF
HV dc-link capacitor (C_{HV})	0.1 μF
Switching frequency (f_{sw})	100 kHz

to regulate the output power. At loads higher than the boundary where the PSFB loses ZVS (P_{ZVS}), the power transfer is shifted to conventional PSM where α_s alone regulates the output power. A hysteresis band is added to prevent bouncing between the modulations at the boundary.

Fig. 11(c) shows the theoretical waveform for the output power versus α_s and Fig. 11(d) shows the current at the switching instant available and the minimum current required for ZVS with the black solid line indicating the proposed hybrid modulation. Thus, the proposed hybrid modulation helps extend the ZVS range till very light load while maintaining lower circulation energy at medium to low loads and lower duty and conduction loss at high loads.

VII. EXPERIMENTAL RESULTS

A 1 kW laboratory prototype of the CFDAB converter was built as shown in Fig. 12. The circuit parameters are listed in Table III. It is controlled by a TM320F28335 digital signal processor. The dead time between the switches in HV is fixed to 0.4 μ s for both the modulations.

Two voltage sources were used at the two ports of the converter. Since, none of the two sources can sink power, a passive resistor is connected on the part that has to sink power. All the design parameters are designed taking into consideration the safe operation of the converter for the highest LV current, i.e., 42 V

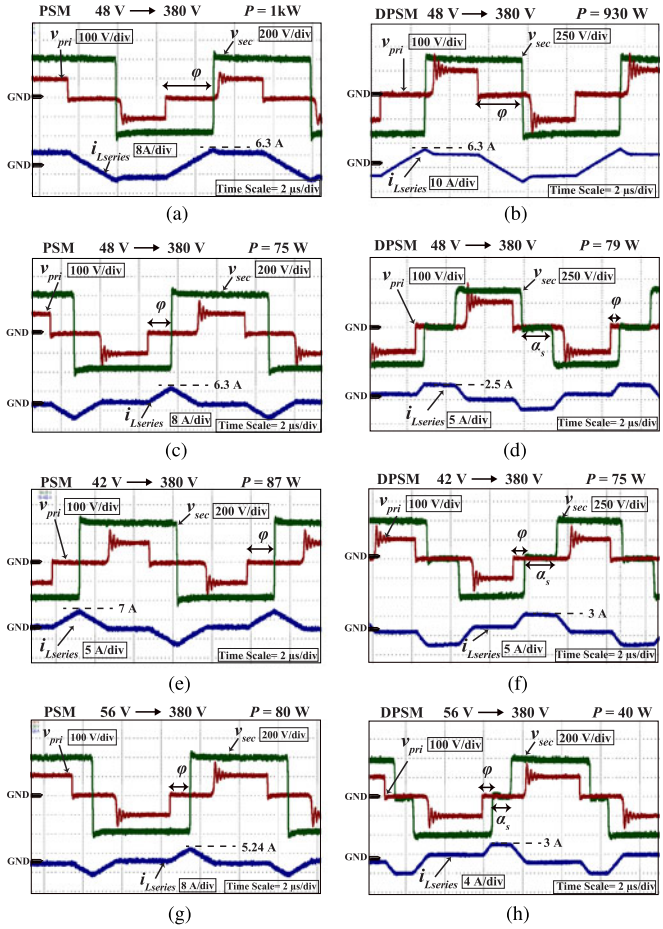

Fig. 13. Forward direction: Experimental waveforms of the transformer voltages and the series inductor at different voltages and output powers highlighting the reduction in the peak current with the proposed DPSM. The peak current is 52% lesser for DPSM as compared to PSM at the highest current (42 V).

LV voltage and 1-kW output power. IPP110N20N3 is selected for the LVS switches based on the figure of merit R_{dson}*Q_g to minimize the conduction losses and the turn-on losses and IPP60R099CP for HVS to minimize the losses due to the rectification and conduction. Two ultrafast diodes MURS320T3G are used as clamping diodes.

A. Experimental Waveforms

Fig. 13 shows the transformer voltages and the series inductor current for both the modulations at different output powers at $V_{\mathrm{LV}} = 42$ V (lowest voltage), 48 V (nominal voltage), and 56 V (highest voltage). To ensure that there is no voltage spike in the LV side at any operating point in DPSM, the converter does not operate at the boundary condition but below it. For 48 V V_{LV}, α_s is chosen as $(0.225-\varphi)$ even though $x = 0.265$ to keep a safe margin. Hence, for $P_{\mathrm{out}} \geq 950$ W, $\alpha_s = 0$ and the DPSM converges to PSM. This can be observed in Fig. 13(a) and (b) where φ alone controls the power flow. The peak current for both the modulation is the same (6.3 A). The difference between the modulations is observed at lighter loads where the peak current is limited to a lower value in DPSM by the introduction of the zero state. Fig. 13(c) shows that for loads as low as 75 W, the

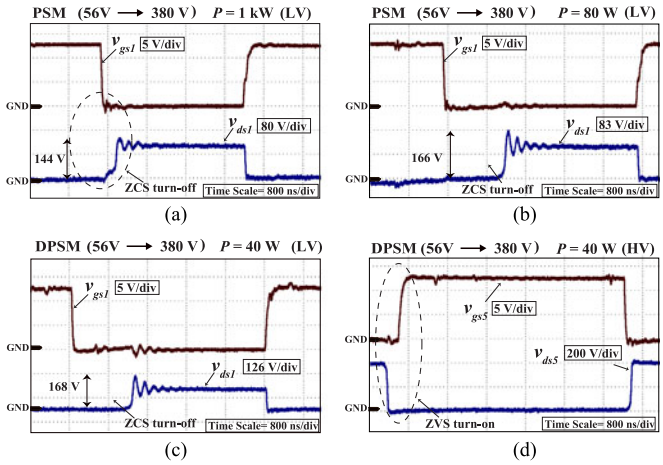

Fig. 14. Forward direction: Experimental waveforms of the gate voltage v_{gs} and device voltage $v_{\rm ds}$ at $V_{\rm LV} = 56$ V for the LV side implementing both conventional PSM and proposed DPSM. The ZCS turn-off of the LV devices is shown for 4% load by the proposed DPSM with reduced peak current and ZVS turn-on for the HV side (d) at 40 W at 4% load.

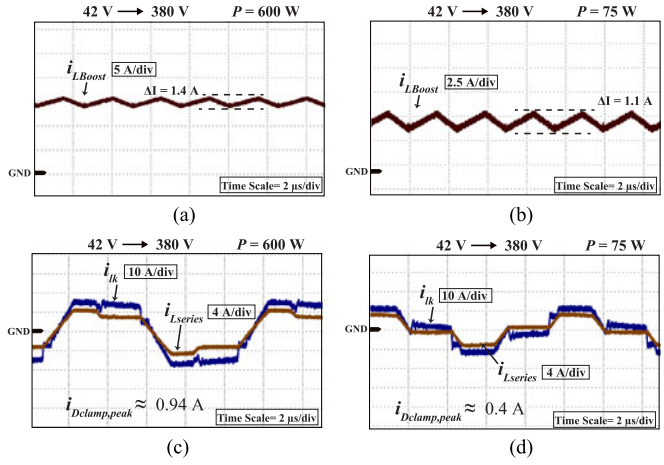

Fig. 15. Forward direction: Experimental waveforms implementing DPSM at $V_{\rm LV} = 42$ V of $i_{\rm LBoost}$ for (a) 600 W and (b) 75 W; $i_{\rm Lseries}$ and $i_{\rm lk}$ for (c) 600 W and (d) 74 W. The peak current through the $D_{\rm clamp}$ is less than 1 A at 60% load.

peak current is still 6.3 A for PSM whereas, the peak value is reduced to 2.5 A in DPSM at $V_{\rm LV} = 48$ V as shown in Fig. 13(d). This difference further increases as $V_{\rm LV}$ decreases. As can be observed from Fig. 13(e) and (f), the peak current for DPSM at 74 W is reduced by almost 52% at 42 V. On the other hand, an increase in $V_{\rm LV}$ reduces the difference in the peak currents. This can be seen in Fig. 13(g) and (h) where the peak current is reduced by 52% at 40 W and the difference reduces with the increase in the load. Hence, the improvement in the performance is observed with the increase in the efficiency specially at lower loads by the implementation of DPSM. The minimum value of φ is limited by the time taken by $i_{\rm lk}(t)$ to change its direction. Thus, $\varphi_{\rm min}$ value is limited to 0.038 p.u. and α_s alone regulates the output power. This means that the loss incurred at lower loads is higher because the converter is now operating farther from the boundary. This ensures the reliability of the converter but at the cost of increased losses than expected at very light loads. Even then, DPSM performance is superior to the PSM counterpart.

Fig. 14(a)–(c) shows the gate and the switch voltages of the LV device for both PSM and DPSM. As discussed in the earlier sections, the increased peak current not only results in increased conduction losses of the antiparallel body-diode but also increased losses due to the reverse-recovery of the poor body-diodes and increased switch voltage. This can be observed in Fig. 14(a) and (c) where the peak of the LV switch voltage is increased to 166 V from 144 V at 80 W in PSM. This further increases as the load decreases. Hence, a higher voltage rated switch has to be selected to ensure a safe margin even though the blocking voltage is ≈ 105 V ($V_{\rm HV}$/n). A decrease in the peak current results in lower recovery losses due to the body-diode and reduced switch peak voltage. Hence as expected, Fig. 14(c) shows a peak of around 168 V at 40-W output for DPSM. Fig. 14(d) shows the ZVS of the HV switches even at 4% load for the highest $V_{\rm LV}$ where HV devices usually lose ZVS. This validates the theoretical claim that the ZVS is maintained for very light loads on the HV side. As mentioned in Section V, the ZCS turn-off of the PSM is easier than DPSM as $P_{\rm max} \propto \varphi$ in the latter. Hence, a safe margin is chosen and the converter is operated a little below the boundary and thus, ZCS turn-off is obtained even at 4% load in DPSM as shown in Fig. 14(c).

Fig. 15(a) and (b) shows the boost inductor current for 42 V input at 600 W and 75 W for DPSM. As can be observed, the ripple current increases with the output power. This is due to the drop in the permeability as the current through the magnetic material increases [22]. However, the use of ferrite material for the boost inductor design results in an increase of only 0.3 A, which results in a marginal increase in the conduction losses. The diode clamp takes the difference in the currents $i_{\rm lk}(t)$ and $i_{\rm Lseries}(t)$. Fig. 15(c) and (d) shows the current for 42 V at 60% and 7.5% load. As observed, the peak current is lower than 1 A through the $D_{\rm clamp}$. Thus, a low-rated diode clamp circuit can be used which incurs lower losses as compared to RC snubber across each LV device. Hence, the diode clamp is a more efficient solution for eliminating the voltage oscillations in the LV device voltage.

Fig. 16 shows the HV side gate and device voltages for the reverse direction of operation. Since ZVS is limited for the highest LV voltage, the results are shown for $V_{\rm LV} = 56$ V. Fig. 16(a) and (b) shows the lagging and leading leg device voltages at 400 W implementing only phase shift (α_s) control. As can be observed, the lagging leg loses ZVS at around 40% load. However, by modulating both φ and α_s, the ZVS range can be extended to loads as low as 6.7% as shown in Fig. 16(c) and (d).

Fig. 17 shows the experimental results for the conventional PSM with synchronous rectification and the proposed DPSM with controlled rectification. At higher loads, the current at the switching instant is sufficient for the lagging leg soft switching. As the load decreases, the current falls below the required current and the converter loses soft switching. From the experiment, the converter loses ZVS when the current at the switching instant falls below 1.7 A (reflected to the HV side), which is

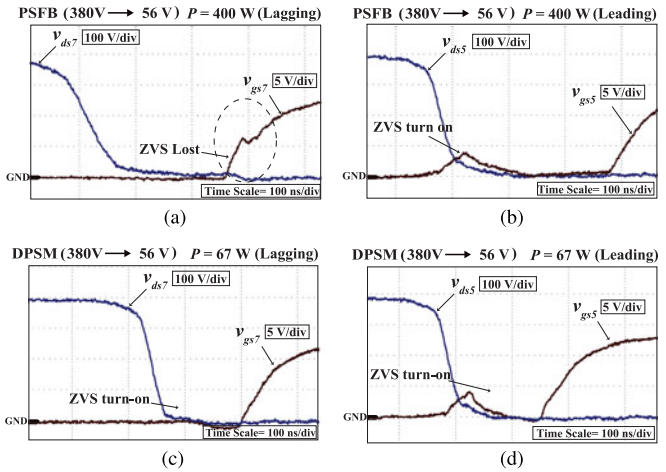

Fig. 16. Reverse direction: Experimental waveforms of the gate voltage $v_{\rm gs}$ and device voltage $v_{\rm ds}$ of the HV devices at the highest voltage $V_{\rm LV} = 56$ V for lagging and leading leg for both the modulations. The ZVS is maintained for DPSM even at 6.7% load whereas, ZVS is lost at 40% load in PSFB.

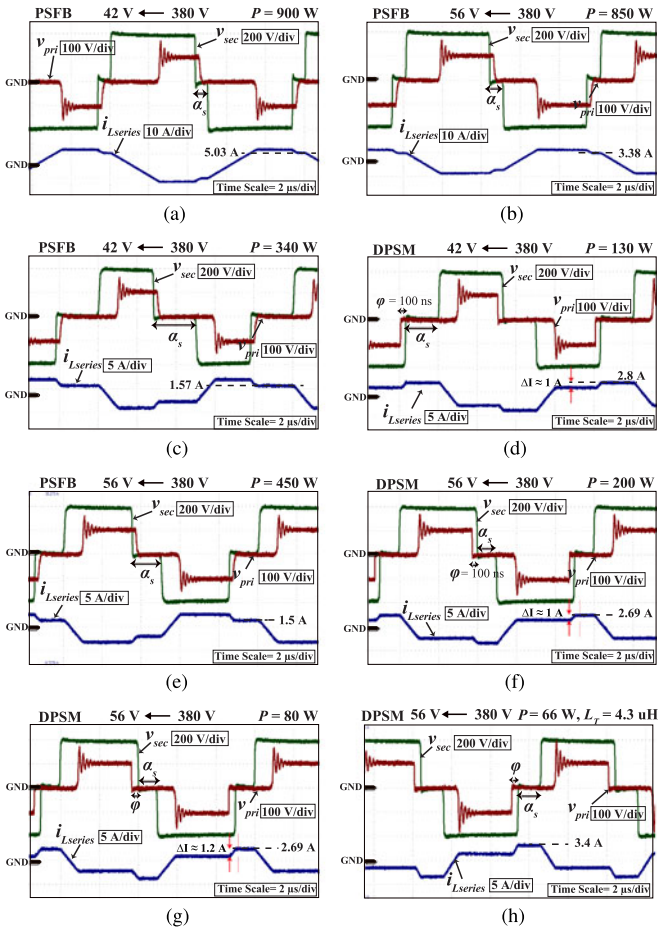

Fig. 17. Reverse direction: Experimental waveforms of the transformer voltages and series inductor current at different voltage and power levels for both the modulation. The power rating at which PSFB loses ZVS and soft switching maintained for very low power with DPSM is illustrated. To reduce the circulating current in DPSM, $\varphi = 0.01$ is maintained till the peak current reaches the minimum ZVS current required; (h) highlights ZVS maintained even at 6% with 4.3 μH series inductance with the proposed controlled rectification. The experiment is conducted for $\rm V_{HV} = 380$ V.

close to the theoretically calculated value 1.6 A using (27). In PSFB, α_s alone could not maintain the current required at the switching instant and thus, the converter loses soft switching at around 450 W at 56 V $V_{\rm LV}$ as shown in Fig. 17(e). Keeping some margin, the boundary power ($P_{\rm ZVS}$) is calculated and the modulation is shifted to the proposed controlled rectification.

In the proposed DPSM, the phase shift φ is kept fixed at minimum till the peak current reaches close to the minimum current required to keep the circulation energy low. The time taken for the LV transformer voltage $v_{\rm pri}$ to fall to zero is around 40 ns. Hence, leaving some margin, φ is fixed at 100 ns and α_s is increased to decrease the output power. Hence, $I_{\rm cir}$ is maintained at almost 1 A from the medium to light load as shown in Fig. 17(d) at 42 V and Fig. 17(f) at 56 V. This decrease in the peak current as the load current decreases, improves the performance of the converter by minimizing the circulation energy and the associated conduction losses specially in the high current side.

Once the peak current is close to 2.7 A, α_s is fixed to maintain the required peak current as shown in Fig. 17(g). Even though the switching instant current required is 1.6 A, a margin is maintained to ensure the converter is soft turned on even at loads as low as 5%. φ is increased to decrease the output power in this operating range. Thus, the ZVS is maintained even for very light loads but at the cost of increased circulating current. Fig. 17(h) shows the waveform of the proposed controlled rectification for $L_T = 4.3$ μH. With the flexibility of active control of the switching instant current by the proposed modulation, soft switching is achieved at 6% even with a small value of L_T.

B. Efficiency

Fig. 18 shows the theoretical and measured efficiency plots for minimum, nominal, and maximum LV voltages for the conventional PSM and the proposed DPSM. Power meter WT110 is used in the high current side and the digital multimeter in the HV side to measure the efficiency. As shown in the figure, the difference in the performance between DPSM and PSM is observed at low loads between (5–60)% load where the circulating current is higher. The difference between the modulations at lower power decreases as the LV voltage increases. As can be observed, the efficiency improved from 0.8 to 0.92 at 42 V $V_{\rm LV}$ whereas, at 56 V, the efficiency improved from 0.864 to 0.93 at around 10% by implementing the proposed DPSM. This improvement is due to the reduced peak current through the converter at lower loads. Since at higher $V_{\rm LV}$ the current is smaller, the difference in the efficiency between the modulations is lesser. The reduction in the peak current, apart from reducing the conduction losses also reduces the core losses in the external series inductance. This can be observed from Fig. 19. The total loss in the series inductor is reduced by almost 83% at 42 V, 300-W output power by the proposed modulation. Also, due to the reduced volt–sec balance applied across the transformer windings, the flux density is lower for DPSM leading to reduced core losses in the transformer. Hence, the total transformer loss is reduced by almost 55% at 300 W for the smallest LV volt-

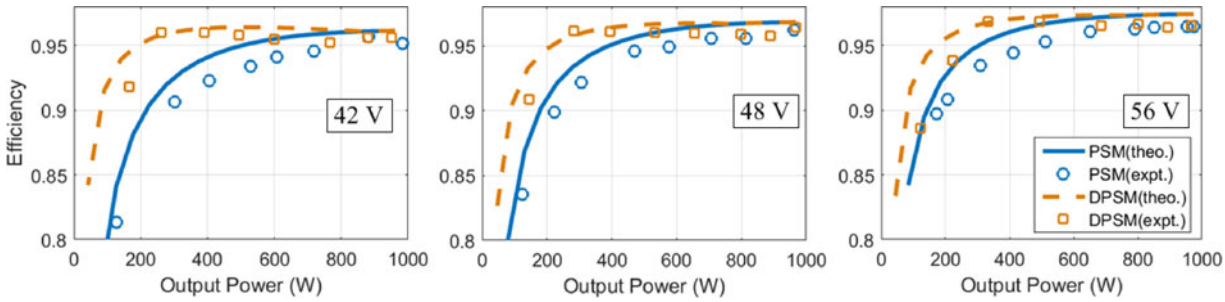

Fig. 18. Efficiency curves for PSM and DPSM at 42 V, 48 V, and 56-V LV voltages.

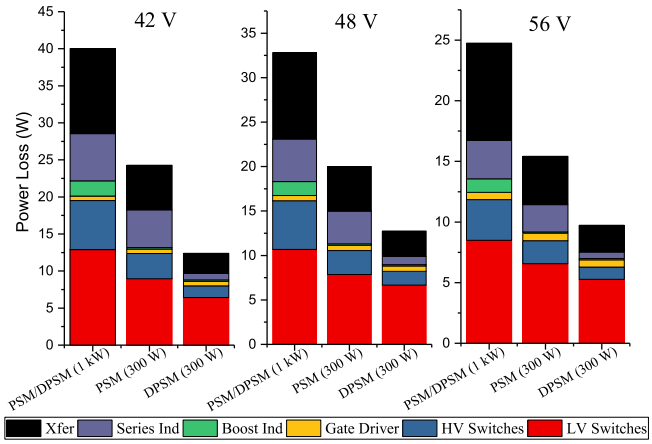

Fig. 19. Loss distribution between different components at 1 kW, 300 W PSM and DPSM at all the three voltages.

age. The core loss is calculated using the improved generalized Steinmetz equation [23] and the ac losses are calculated using the proximity loss factor given in [24]. Another major contributor to the difference in the efficiency is the reverse recovery losses due to the poor antiparallel body diode. The loss due to the current dependent recovered charge (Q_{rr}) is calculated using [21]. The loss due to the reverse recovery is reduced by 35% at 300 W by the proposed modulation and by around 50% at 1 kW. Hence, the proposed modulation reduces not only the conduction losses but also the core losses and the reverse recovery losses at lower loads. Thus, regulating the peak current by implementing the proposed DPSM helps maintain a near flat efficiency profile till 20% load. At higher output power, the control variable α_s reduces to zero and the modulation converges to PSM. An efficiency of 97.5% and 96.1% is obtained at 56 and 42 V, respectively, at 1 kW.

VIII. Conclusion

This paper proposed DPSM for the active commutated CFDAB. The phase shift between the legs in the HV side helped reduce the LV diode current to decrease the circulating current in the converter. The choice of the control variables are constrained by the necessary condition that the current through the LV devices is negative before the gating pulse is removed to avoid the voltage spike across the LV devices. The two degrees of freedom in the proposed modulation helped improve the performance of the converter by regulating the peak current with load as compared to the simple single variable control, PSM. The reduction in the RMS current at light loads by implementing DPSM improved the total switch utilization of the LV devices by 55% at 20% load and an almost flat efficiency at 96% is maintained till 20% load even at the highest LV current (42 V). The proposed DPSM is implemented in the reverse direction to extend the ZVS range of the HV devices. The turning on of the LV device channel before its body-diode is forward biased, increases the current available for the voltage commutation of the HV lagging devices. At higher output power, the modulation shifts to phase shift to reduce the circulating current and the duty cycle loss. Thus, the proposed modulation increased the ZVS range by achieving ZVS even at 6% load whereas, the conventional phase shift could maintain soft switching only till 40% load in the buck operation.

The proposed DPSM for CFDAB offers the desired performance by regulating the peak current in the forward operation and extending the ZVS range in the reverse operation. This is achieved without shifting between modes for different loads, thus providing a simple yet effective solution.

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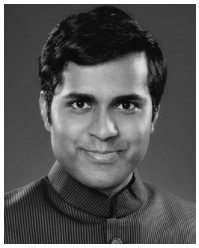

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