Manchester decoding algorithm for Multifunction Vehicle Bus

J. Jiménez, J.L. Martín, A. Astarloa and A. Zuloaga
Universidad del País Vasco
Escuela Técnica Superior de Ingeniería de Bilbao
Alameda Urquijo s/n, 48.013 Bilbao, España
{jtpjivej, jtpmagoj, jtpascua, jtpzuiza}@bi.ehu.es

Abstract– **The Multifunction Vehicle Bus (MVB) is a local area network for telematic applications of trains. It uses Manchester encoding in order to interchange data among field devices on board. The physical level is accurately defined since RS-485 standard is followed. So electrical signal are bipolar and the point-to-multipoint structure is the most common topology. The railway communication systems must be hardly reliable, so any error in a received frame supposes discarding it. The decoding algorithm in this paper detects wrong values of voltage along a defined symbol and compares the placement of edges with the theoretical right position. It is based on an over-sampling process, by taking into account the admitted tolerance in the medium.**

A C model of an MVB circuit has been created in order to validate the decoding algorithm and establish the start point in the design flow. Exhaustive simulations have proved that the decoder can detect any error in the symbol level with a resolution of 41.67 ns , 12.5 % of the symbol time and that all misplaced edges are rejected and correct ones might be discarded in a range of 25 ns, 7.5 % of the symbol time. In addition, the decoder has been described in VHDL and synthesized in a EPM3032ALC44 of Altera. It has been arranged in the following modules: the start bit detector, a clock signals generator, a shift register and the edges detector.

1 Introduction

Communication networks bring important profits to public transport, specially to railways. As train manufacturers have realized how complex the device interconnection on board is, they have asked equipment suppliers easier networking resources and to use a common standard [1-2]. This has led the IEC (International Electrotechnical Commission) to define a standard for railway: TCN (Train Communication Network) [3]. The general architecture of TCN includes two bus types (Fig. 1):

· MVB (Multifunction Vehicle Bus), which is used for attaching the electronic equipment inside a train vehicle.
· WTB (Wired Train Bus), which is used for inter-connecting the different vehicles of a train.

The MVB is the industrial data network in charge of interconnecting several devices in a local environment (up to 200 meters). Among these devices there are a Master, which is the bus administrator, and multiple Slaves, which perform different services at the Master command. Among the MVB characteristics, these must be highlighted: physical redundancy, signaling -frame start and end delimitation flags-, encoding: Manchester II, data rate: 1.5 Mbit/s, frame size (of the useful information): 16, 32, 64, 128, or 256 bits.

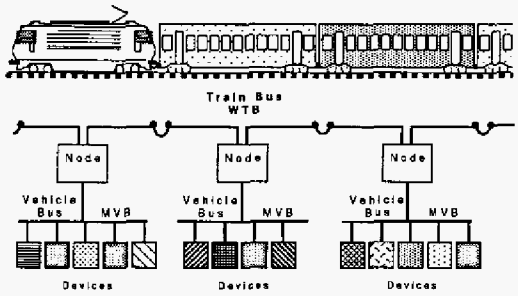

Fig. 1. Train Bus and Vehicle Bus.

The MVB allows two kinds of frames, each of them with a different start delimiter:

· Master Frames, which are sent by the Master node. They have a fixed length of 34 bits, including the start delimeter (9 bits) and the end delimiter (1 bit), a 16-bit data in which 12 bits are an Slave device address and 4 bits are the F_code, which indicates the type and size of the expected Slave frame, and the Check Sequence of 8 bits (fig. 2).

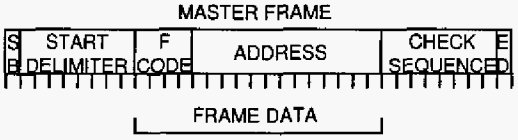

Fig. 2: Master_Frame Format.

· Slave frames, which are sent by the Slave nodes in response to Master frames. Their length can be one out of five sizes: 34, 50, 82, 154, or 298 bits, including the start frame and end delimiters (9 and 1 bit respectively), 16, 32, 64, 128, or 256 data bits and the 8-bit Check Sequence for each group of up to 64 information bit sequence (fig. 3).

In addition to these characteristics, the TCN standard establishes the maximum time that can elapse between a received frame and the frame sent in response (6 ms) and the maximum time that may elapse between the reception of a Master frame and a Slave one (42.7 ms). In case of detecting an error, the frame that has generated it must be ignored, as well as the following Slave frames until a correct Master frame is received.

0-7803-8662-0/04/$20.00 ©2004 IEEE

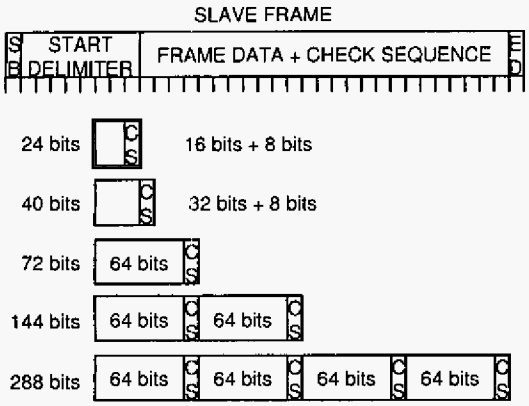

Fig. 3: Slave_Frame Format.

In MVB bus different classes of devices can be used in order to carry out various functions and services both for the vehicle and for the bus itself. Class 1 devices play Slave role, receive Master and Slave frames and, when polled, send a Slave frame. Such a device is able to send its Device_Status as well as Process Data when polled and to receive Process Data from other devices.

The MVB characteristics involve using a module especially dedicated to the access control of the Slave devices to the Bus. The tasks that must be performed can be divided into two groups: bit level tasks (imposed by the standard that regulates the MVB) and word (16 bits) level tasks:

· Bit level tasks:
Manchester encoding and decoding.
Serial to parallel and parallel to serial conversion.
Error detection.
Time control.

· Word level tasks:
Transmission of answers to the Master node commands.
Data reading or writing for transmission through the Bus.
Received data processing.
Obtaining the data to be sent.

All these tasks must be carried out efficiently and at high speed. In addition, the received bits must be synchronized and the signal must be oversampled to verify that the total length of each bit is within the allowed range.

In all MVB media, signalling speed shall be 1.5 Mbit/s ± 0,01 %, using Manchester encoding (bit rate = 1.5 MHz or 1.5 Mbit/s, bit time = 666,7 ns). Individual data bits, "1" and "0" shall be encoded as follows [4]: a "1" by a high level during the first half of a bit cell followed by a low level during the second half; and a "0" shall be encoded by a low level during the first half of a bit cell followed by a high level during the second one (fig. 4).

2 Classic Manchester decoders

Manchester encoding involves two main advantages: the average voltage level is zero in the case of equally likely binary digits, so the bus line suffers from no polarization, and sender's carrier clock can be recovered straightforward from the received signal [5-6]. In the context of optical communications, this format produces an extra benefit when using wavelength division multiplexed (WDM) techniques: it is an appropriate way of suppressing the cross-gain modulation in high bit rate communications [7]. On the other hand, it presents a poorer bandwidth efficiency when comparing with other common coding techniques, as unipolar non-return-to-zero format or delay modulation [8-9].

Most Manchester decoders look for the relative time origin as soon as they detect activity in the communication line. From that start, the receiver must simply sample the line periodically in the middle of each symbol, after some signal processing in order to adapt the electrical levels at the decoder input [10-12] (fig. 5 a). Accurate timing is obtained by means of a PLL or using the previously established clock frequency –if it is known, as in MVB. This method is not reliable enough for railway applications [13-14], as an only sample per symbol does not ensure that the voltage level is right during all the symbol. In addition, in the MVB context, the accurate placement of the edges in the received signal must be compared with the theoretical right position in order to determine the correctness of the whole frame. An improvement for this algorithm is to take some samples per symbol. Nevertheless, the second drawback is not resolved, as observed points tend to place far from the edge, in order to ease decoding (fig. 5 b).

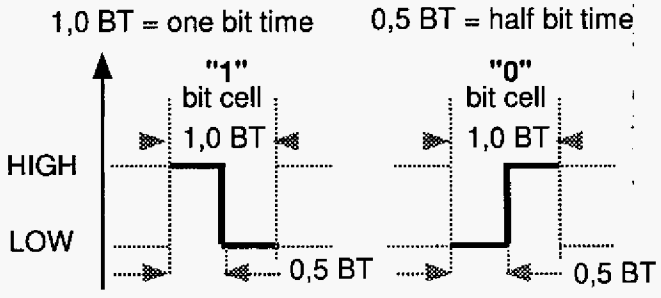

Fig. 4: "0" and "1" data encoding.

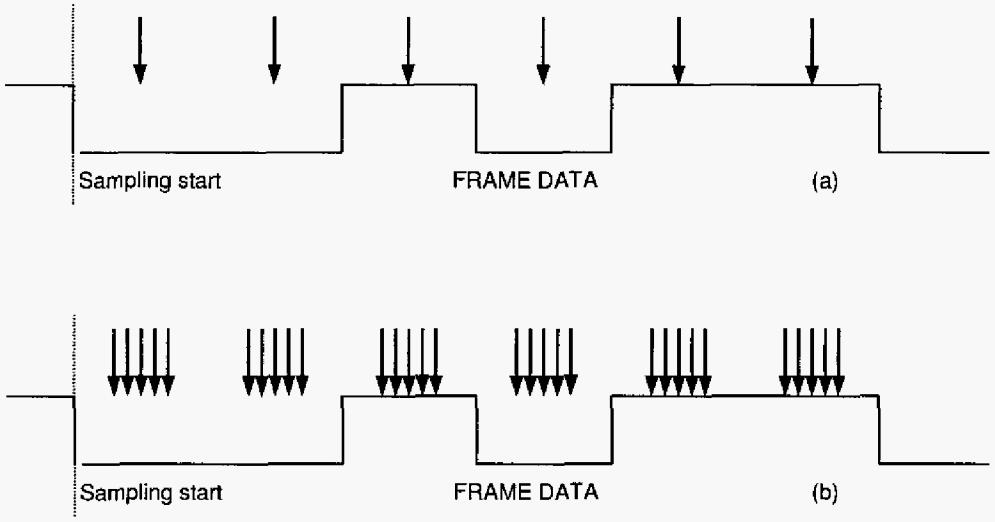

Fig. 5: Classic decoding: one sample (a) and various samples (b) per symbol.

3 The new decoder

The decoder block described in this paper waits until a *start bit* is detected. After that, it identifies the *start delimiter* as "slave" or "master". Next, the *data frame* must be decoded. For this purpose, the line is continuously oversampled in order to determine the location of the edges with an accuracy of the sampling period. Two features must be checked: first, whether the length of the symbol is acceptable, and, second, whether the edge is located in the right position relatively to the time start point. As symbol rate in MVB is 3 Mbps, a sampling frequency of 24 MHz (period = 41,67 ns) has been used [15]. In this way there are 8 samples per symbol and 16 per bit; so perfect bits would have 8 "low" samples and 8 "high" ones (fig. 6 a). The TCN standard establishes that edges may be displaced 0,1 bit time (66,67 ns) in the electrical media and 125 ns in optical fibre. This means that an edge can be, in the electrical media, between 266,67 ns and 400 ns from the theoretical start point of the symbol; in optical fibre, the values are 208,33 and 458,33 respectively. If these lengths are turned into amounts of samples, the new values are 6 and 10 in electrical media and 5 and 11 in the optical one. The conclusion is that an edge can be displaced ± 2 "samples" in the first case and ± 3 in the second one (fig. 6 b). This number of tolerance samples will be refer generically as "D".

Nevertheless, acceptable symbol lengths will be any in the range of ± 2D, as previous edge may be misplaced forward or backward, independently where is the present one. Therefore the decoding process will begin as soon as a correct start symbol is detected by sampling the line continuously. On one hand, symbol lengths must be sensed to check whether they are 8 ± 2D samples. So a counter stores the number of samples whose electrical level is equal, until logical value changes or maximum acceptable length, tolerance included, is reached. This counter may be reset after each symbol. Additionally, on the other hand, the position of the edges must be accurately checked in order to know whether they are in the range of ± D around the theoretical right point (fig. 7). This means that the decoding algorithm must count how many samples are between the start edge and everyone in the frame. A more efficient way is to count the excess, positive or negative, in the amount of samples for the final edge of each symbol and use its value in order to calculate the new excess in the next symbol. Therefore, this second count cannot be reset until the next excess has been calculated.

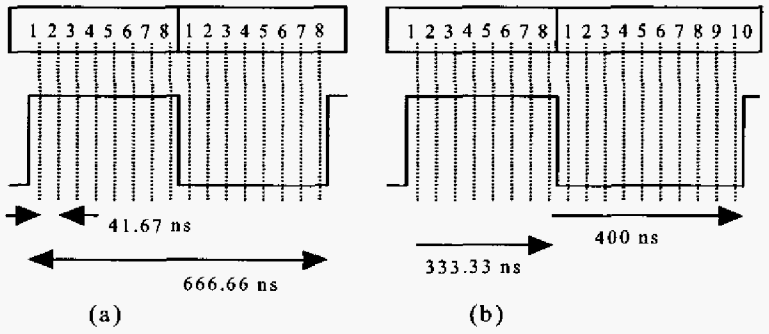

Fig. 6: Samples in a perfect bit (a) and in an imperfect but admissible one (b).

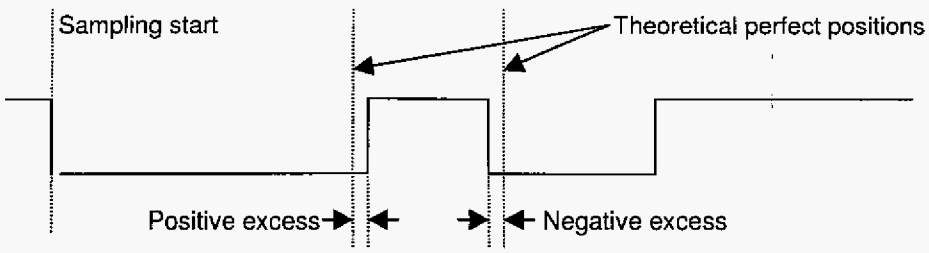

Fig. 7: Misplaced edges in a frame and associated excesses.

4 Results

Resolution in the sampling process is 41.67 ns, 12.5 % of the symbol time; all misplaced edges are rejected and correct ones might be discarded in a range of 25 ns, 7.5 % of the symbol time. Nevertheless, the probability of rejecting correct ones is really low, since edges will tend to appear in the middle of the acceptable interval and not in the ends. The decoding algorithm has been modelled as a function in C language, inside the description of an MVB device [16]. This last one will be the initial model in order to design the whole node and has been simulated until validation. A set of functions and subroutines, which can be seen as independent modules, has been added so that reading and understanding the description may be eased. Anyway, those blocks can be reused in future designs, and this is the most powerful feature of the code. System-on-a-chip style of design involves creating virtual components and reusing them, and it is a natural way in TCN devices synthesis.

A crucial problem in the C testbench has been how to simulate the communication channel and how to show results. In order to represent the incoming signal, a text file is used; another one to write the outgoing signal, and a last text file is in charge of storing the address map of the device as well as data bits. They enable the simulation of the algorithmic model's behavior when receiving Master frames, Slave frames to ports subscribed as sink and sending Slave frames from ports subscribed as source. In the case of a master frame, the system must read the address, so that it can find whether the device is subscribed to it and which register has to be written or read. "tx_status" and "tx_process" are used to send the Device_Status or the Process_Data of the device, respectively, in response to a master frame. If a slave frame is expected to be received, the appropriate register is written in "rx_process". The four collision states are reached after any decoding task has failed and each one reports about a kind of error. Besides, don't care ordinary traffic and noisy frames have been simulated, as well as data interchanging. Both, the testbench and the C description have been written in parallel.

The particular decoding function has been edited in 38 C lines. A specific variable is in charge of counting the sample number excess. Exhaustive simulations have proved that the model is correct; starting from a perfect MVB frame, all acceptable displaces of the edges have been decoded right and when tolerances have been exceeded in one sample anywhere, the model has detected the error.

In addition, the decoder has been described in VHDL and synthesized by a software design tool –MAX-plus II of Altera- in a EPM3032ALC44. It has been arranged in the following modules: the start bit detector, a clock signals generator, a shift register and the edges detector. The most complex one is the start bit detector: a finite state machine described in 233 VHDL lines to code 26 states. Some details about implementation are: logic cells used: 30, 93% of the PLD; shareable expanders: 20; peak memory allocated during compilation: 2,909K.

This electronic design in VHDL language has been verified before prototypes have been produced. For this purpose, a virtual communication network has been described as a bus-functional model where MVB "devices" access to interchange data [17]. At least one bus administrator and one Class 1 device, with a behavioural hardware description, have been connected. Such virtual nodes generate VHDL signals that simulate real traffic of Master and Slave frames (fig. 8). Besides these elements, the device under test, the presented decoder inside, has been connected to the virtual network. There is no way we can observe all possible situations, but the testbench lets us supply traffic patterns to the device under test and then visualize whether the network responds as expected. Hence, the VHDL description of a device which will be synthesised has been validated before configuring the FPGA. A user interface software facilitates the verification engineer work throughout four tasks: configuring the virtual network, addressing devices and registers, generating traffic and visualizing data. Intermediate ASCII files are used for the communication between the user interface and the VHDL network.

5 Conclusion

The Multifunction Vehicle Bus (MVB) is an industrial data network for interconnecting sensors, actuators and control systems on trains. The sent frames are coded in Manchester format, with start bit, start delimiter and delimiter. The master-slave architecture is used in order to interchange data among field devices on board.

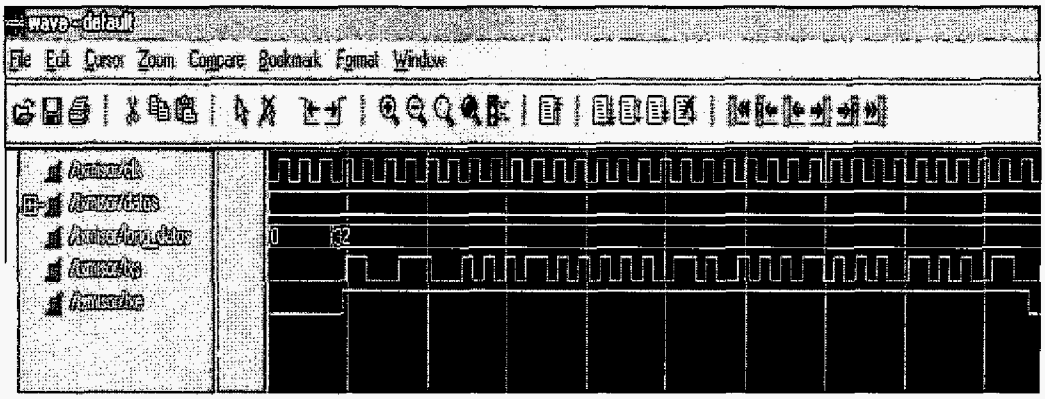

Fig. 8: A view of one simulation of the virtual network.

The physical level is defined in detail, following the RS-485 standard. So electrical signal are bipolar and the point-to-multipoint structure is the most common topology. Specific transceivers and drivers are used, depending upon the transmission media: Electric Short Distance (ESD), Electric Middle Distance (EMD) or Optical Glass Fibre (OGF).

The railway communication systems must be hardly reliable, so any error, great or minor, in a received frame supposes discarding it. Concerning the detection process, there are two kinds of possible faults: not Manchester symbols and misplaced edges. The decoding algorithm in this paper detects wrong values of voltage along a defined symbol (333,33 ns). In addition, it compares the placement of edges with the theoretical right position. It is based on an over-sampling process, by taking into account the admitted tolerance in the medium: 0,1 bit time (66,67 ns) in the electrical media and 125 ns in optical fibre.

A C model of an MVB circuit has been created in order to validate the decoding algorithm and establish the start point in the design flow. Exhaustive simulations have proved that the decoder can detect any error in the symbol level with a resolution of 41.67 ns , 12.5 % of the symbol time and that all misplaced edges are rejected and correct ones might be discarded in a range of 25 ns, 7.5 % of the symbol time.

In addition, the decoder has been described in VHDL and synthesized in a EPM3032ALC44 of Altera. It has been arranged in the following modules: the start bit detector, a clock signals generator, a shift register and the edges detector.

Acknowledgement

The work described in this paper has been supported by the Ministerio de Ciencia y Tecnología of Spain and FEDER in the framework of the TIC2001-0062 research project.

References

[1] P. Umiliacchi, "The Role of European research in the railways modernisation process: The ROSIN project," Proceedings of World Congress on Railway Research, 1997.

[2] G. Fadin et al., "ROSIN, Railway Open System Interconnection Network - Web Technologies for Railways" Proc. of Automation in Transportation, 1998.

[3] International Electrotechnical Commission, IEC 61375-1, *Train Communication Network*, 1999.

[4] Bellamy, J. *Digital telephony:* John Wiley & Sons, Inc., New York, 1991.

[5] Al-Sammak, A.J. "Encoder circuit for inverse differential Manchester code operating at any frequency", *Electronics Letters*, 6th June 2002, vol. 38, pp. 567–568.

[6] Carlson, A. B. *Communication systems. An introduction to signals and noise in electrical communication*: McGraw-Hill International Editions, New York, 1986.

[7] Shibata, Y.; Yamada, Y.; Habara, K.; Yoshimoto, N. "Semiconductor laser diode optical amplifiers/gates in photonic packet switching", *Journal of Lightwave Technology*, vol. 16, no. 12, December, 1998, pp. 2228-2235.

[8] Benedetto, S.; Biglieri, E.; Castellani, V. *Digital transmission theory*: Prentice Hall International Editions, Englewood Cliffs, New Jersey, 1987.

[9] Haykin, S. *Digital communications*: John Wiley & Sons, Inc., New York, 1988.

[10] Inoue, K. "Waveform distortion in a gain-saturated semiconductor optical amplifier for NRZ and Manchester formats", *IEE Proc. Optoelectronics*, December 1997, vol. 144, pp. 433–437.

[11] Di Rocco, A. "Manchester co-decoder fits into 32-macrocell PLD", *EDN*, January, 6, 2000, vol. 45, p. 122.

[12] Yamada, Y.; Shibata, Y.; Habara, K. "10Gbit/s differential receiver for large optical power fluctuation", Electronics Letters, vol. 33, no. 19, 11th September, 1997, pp. 1642-1643.

[13] Hill, R.J. and Bouillevaux, J. "Safety and reliability of comma-free digital coding for railway track circuits", *IEE Proc. Electric Power Applications*, May 1999, vol. 146, pp. 350–360.

[14] Schiano, L.; Metra, C.; Marino, D. "Self-checking design, implementation and measurement of a controller for track-side railway systems", *IEEE Transactions on Instrumentation and measurement*, vol. 52, no. 6, December 2003.

[15] Chavarría, A et alter: Slave node architecture for Train Communications Networks, Proceedings of the 2000 IEEE International Conference on Industrial Electronics, Control and Instrumentation, 2000, pp. 2431-2436.

[16] Jiménez, J. et alter: A Top-Down Design for the Train Communication Network, Proceedings of the 2003 IEEE International Conference on Industrial Technology, SS4.2, 2003.

[17] Jiménez, J. et alter: Simulation environment to verify industrial communication circuits, Proceedings of the 2002 IEEE International Conference on Industrial Electronics, Control and Instrumentation, IIT-07, 2002.