Research and Design of MVB Bus Administrator Based on SOPC Technology

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***Abstract*—Bus Administrator capability is the key characteristic of MVB Class 4 Device, which is the main equipment in the MVB network. A novel MVB Bus Administrator Controller design method based on the SOPC technology is presented, which each function is realized by the Nios II application software. Finally, the performance of the Bus Administrator is evaluated in the TCN hardware-in-loop simulation platform in lab and the results indicate that the design accorded with IEC61375 protocol. This design also has been applied to the Distributed Locomotive Fault Detecting and Recording System, and it has reached the expectation of design. This work has great significance for promoting China's train network construction and the localization of locomotive.**

Keywords- Train Communication Network; MVB Bus Administrator; SOPC; FPGA

I. INTRODUCTION

TCN is a data communication network that is intended to connect programmable electronic equipment on-board rail vehicles. It encompasses two serial buses: 1) the MVB (1.5 Mb/s), which interconnects devices within a vehicle (or equipment within an inseparable group of vehicles); and 2) the WTB (1 Mb/s), which interconnects the vehicles in trains of variable composition [1]. The MVB bus is optimized for rapid process control of the bus, can provide the necessary response speed for train control, it is suitable for use as vehicle bus. Compared with several other field buses (Lonworks, WordFIP, CAN, etc.) in application of the train, MVB has certain advantages of real-time, reliability, manageability, medium access control, addressing method and so on [2]. MVB devices are divided into five categories according to the performance, of which the class 4 device is the MVB bus administrator. It shall offer the capabilities: Device Status, Process Data, Message Data and Bus Administrator, and plays an important role in MVB system.

IEC61375-1 has also been adopted as the national standard of China and one of the railway industry standards (Train Communication Network TB/T3035-2002), and many research institutions and schools have purchased TCN products and development tools produced by foreign companies, we also have applied TCN on projects such as the "China Star" EMU, "Central China Star" EMU and SS3B multi_locomotive [3]. However, the research and development of train control network is relatively later in China, the development and application level is still at an early stage; plus all the connected devices need to access the MVB bus by MVB network interface card, whereas the foreign companies monopolize the core chip MVBC, all of these has brought great difficulties to promote the use of MVB in domestic locomotives and other applications of MVB. The implementation of MVBC by using general FPGA, not only can greatly facilitate the internal application of MVB, but also has important significances for promoting China's construction of the train communication network as well as the localization of locomotive.

II. DESIGN METHOD

Overview of the current development of MVB at home and abroad, it is different in the development methods of MVB controller. Abroad, TCN's key technology developed by the joint development team, which consists of Siemens, FIREMA, AEG and ABB, and applied to their own TCC system. Therefore, the control chip used is mostly self-developed specific integrated chip.

With regard to domestic, there are two approaches. The first is to carry out the design and development using the MVB specific integrated chip produced by foreign company. The second method is to design using FPGA. The most manufacturers adopt the second way because it avoids the difficulty of import and the high cost. Figure 1 is a typical MVB network interface card d113 of Duagon, its hardware mainly consists of high-performance 32-bit ARM processor, non-volatile program memory Flash and the data memory RAM, the MVB transceiver and external PC/104 bus interface are achieved in the programmable device [4].

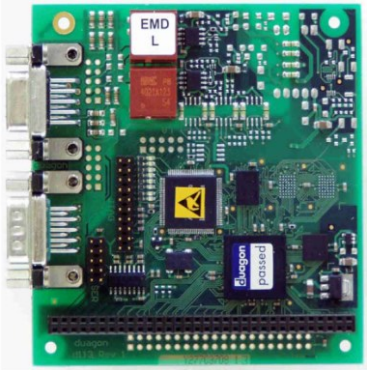

Figure 1. The MVB adapter of Duagon

This paper takes the second technical approach, designs the MVB Bus Administrator using SOPC technology: 32-bit high-performance soft-core processor, ROM, RAM, Traffic

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Memory, MVB bus access IP core are integrated into an FPGA to achieve a true system on chip (shown in Figure 2), this method has simple hardware structure, high reliability and strong flexibility [5].

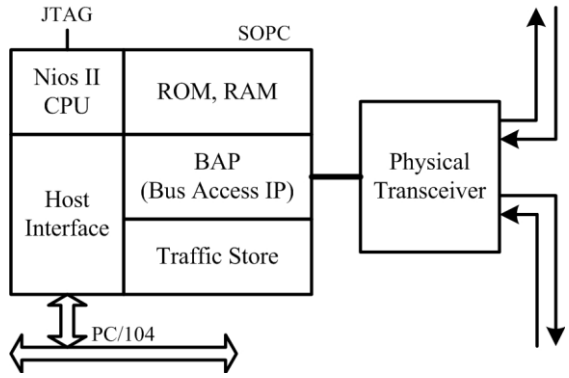

Figure 2. Structure of MVB Bus Administrator

III. BOTTOM DESIGN

At the bottom, MVB Bus Administrator (MVB BA) in need of basic MVB transceiver to implement the physical layer interface and the data link layer functions, it communicates with the upper software through traffic storage, to complete communication of the master frame and slave frame on the MVB bus. MVB transceiver IP core comprises coding logic control module, decoding logic control module, traffic storage and bus interface. MVB Bus Administrator is different from the ordinary MVB device, it requires control the MVB bus, it needs to add sign signals and control signals used to determine bus status and control transmission of master-slave frame at the bottom, in order to achieve that CPU's completely control of the data frame. Figure 3 shows the system integration in the SOPC Builder, which include 32bit processor, On-Chip Memory for system boot, MVB frame transceiver IP module, various control signals, timers and so on.

Use	..	Module Name	Description	Clock	Base	End	I...
☑		cpu	Nios II Processor	clk	0x00005000	0x000057ff	
☑		epcs_controller	EPCS Serial Flash Controller	clk	0x00005800	0x00005fff	0
☑		onchip_mem	On-Chip Memory (RAM or ROM)	clk	0x00002000	0x00003fff	
☑		mvb_encoder_inter	ramway0	clk	0x00006080	0x000060ff	
☑		mvb_decoder_inter	mvbdecoder_inter	clk	0x00006000	0x0000607f	
☑		pio_slave_rxdtotal	PIO (Parallel I/O)	clk	0x00006200	0x0000620f	
☑		pio_dtotal	PIO (Parallel I/O)	clk	0x000061a0	0x000061af	
☑		pio_pen	PIO (Parallel I/O)	clk	0x000061b0	0x000061bf	
☑		pio_msflag	PIO (Parallel I/O)	clk	0x000061c0	0x000061cf	
☑		pio_in_valid	PIO (Parallel I/O)	clk	0x000061a0	0x000061af	
☑		pio_in_msflag	PIO (Parallel I/O)	clk	0x000061f0	0x000061ff	
☑		timer_1ms	Interval Timer	clk	0x00006100	0x0000611f	1
☑		timer_42us	Interval Timer	clk	0x00006140	0x0000615f	2
☑		timer_4us	Interval Timer	clk	0x00006160	0x0000617f	3
☑		pio_TI	PIO (Parallel I/O)	clk	0x00006210	0x0000621f	
☑		pio_RI	PIO (Parallel I/O)	clk	0x00006220	0x0000622f	
☑		timer_25us	Interval Timer	clk	0x00006180	0x0000619f	4
☑		pio_LED	PIO (Parallel I/O)	clk	0x00006140	0x000061df	
☑		uart	UART (RS-232 Serial Port)	clk	0x00006120	0x0000613f	5

Figure 3. Integration of SOPC system

IV. TOP DESIGN

In the TCN network environment, MVB bus administrator required to provide a higher level services, including medium access distribution (setting and modification of periodic list, the basic period, the macro-period, etc.) and telegram timing (sending the master frame periodically, completion of the communication of the master frame and slave frame within a specified time) and many other functions, thus achieves the information transmission of train control and diagnostic, all of these need to accomplish at the application layer.

A. The send of master frame

The master frame is a frame sent by the bus administrator. The most basic function of BA is to poll the various ports and devices, MVB network communication must be initiated by the transfer of master frame by BA, so the send of master frame is the primary design element of the MVB BA.

The MVB codec module packaged at the bottom is different from the past class 1 device's. To achieve complete control of bus, it needs to lead some signals, such as MSFLAG (to distinguish between master frame and slave frame), Dtotal (data length identifier) and P_EN (to enable transmission).

The send of master frame mainly consists of Start_Frame and Frame_Data two parts at the top layer, the rest master start delimiter and check sequence are automatically added by the bottom layer, finally form a complete master frame to send. The main task of Start_Frame part is to be able to send, combined with the requirement of bottom layer, the master frame needs a falling edge of P_EN to enable the send. Frame_Data part is the data area of the master frame, it send a dataset with 16 bits, with the four most significant bits shall be the F_code, the least significant 12 bits shall represent an address or parameters as specified by the F_code.

B. Process data telegram

Process data is source-addressed data broadcast periodically by the link layer in relation with process variables transmission, it is transmitted periodically at an interval which is the individual period, also is the most important and basic data format in the MVB network.

We designed the process data function in term of agreement, namely Period_Data (alt_u8 Period_List, alt_u8 Total_Num). Wherein Period_List indicated the location of the basic period in the macro cycle, Total_Num on behalf of the number of ports polled in this basic period, the program flow is shown in Figure 4.

Dotted box in the figure indicates whether received the slave frame. 42.7us refers to the reply delay T_reply defined in the agreement, this parameter tells the master how long it shall wait before sending the next master frame if it receives no slave frame or if it expects a collision. If there has no response within 42.7us, then to give up this frame; if has any response, RI flag bit becomes 0, then exits from timer to receive the response frame, once it has been received the correct frame after check, flag Valid_flag will set to 1, the master will clear the refresh time of this port; otherwise, plus one each time, until the count is 0xFFFF.

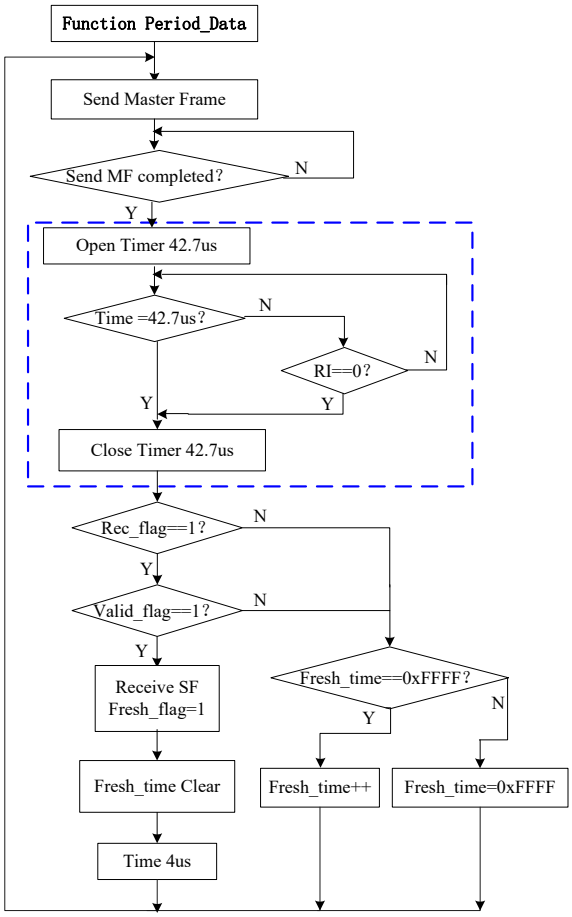

Figure 4. Program flow of the Period Data

C. *Message data telegram and supervisory data telegram*

The master shall request the transmission of message data by sending a message data request, the device addressed in the master frame shall respond with a message data response. Also a master shall request supervisory data from a node or shall send supervisory data to a node with a supervisory data request, to which the addressed source shall respond with a supervisory data response.

There are two means of transmission of message data: the first one is during the sporadic phase of polling, master device sends a message data request to the nodes with message data capability, if there have response in a special time, and then to start the message data telegram transmission; if not then to begin the next polling. The second method is to be achieved in combination with a general event request frame, a device will set device status register's Message_Data_Capability bit to "1" when it need to transfer the message data, during the time at which the master device detects the message request of this device, it will send message data request frame to begin the communication.

Taking into account the practical and real-time, this design adopts the second method. Message data, which is a master frame with F_code = 12, receives data and sends data through the FIFO, length of frame data is 256 bits. According to the different requirements, supervisory data has different function code, the length of response frame is 16 bits.

D. *Periodic list*

Bus activity is divided into periods, in which the shortest is the basic period. The periodic list shall define the master frames sent out periodically and the time left for the sporadic phase for each basic period of a turn. During periodic polling, the master shall send a predefined sequence of master frames according to its periodic list.

Individual period is known as the interval between two successive transmissions of the same process data from the same source, denoted as T_ip. The master polls each periodic data with its individual period T_ip. An individual period shall be equal to the basic period multiplied by a power of 2, but shall not exceed 1024 T_bp, or in general:

$$T\_ip = T\_bp \times 2^{\lambda}, \qquad \lambda \in \{1, 2...10\} \tag{1}$$

The longest individual period in the periodic list, called the macro period, shall not exceed 1024 ms.

As shown in table I, we calculate the propagation delay of ports with various F_code according to the agreement, it is to be taken into account when design the periodic list.

TABLE I. PROPAGATION DELAY OF DIFFERENT F_CODE

F_code	SF(bits)	Telegram(bits)	Propagation delay
0	16	1+8+16+8=33bits	22us(33/1.5)
1	32	1+8+32+8=49bits	32.67us
2	64	1+8+64+8=81bits	54us
3	128	1+8+128+8*2=153bits	102us

V. EXPERIMENT

In order to verify the correctness of the design, we applied this MVB bus administrator to the distributed locomotive fault detecting and recording system. This system consists of instant fault detection recorder (JCY), logic control module (LCM), data acquisition modules (COLM, COLS) and locomotive display (DISP). To prove the accuracy of the data frame format, we carried out the following experiment: build a network including four logic ports of four devices, port 0x20 of DISP1, port 0x30 of DISP2, port 0x10 of JCY and port 0x13 of TEMP are set to sink ports, the system also includes MVB BA and a terminal display device. Network structure is shown in figure 5, and each logical port was defined in the following table II.

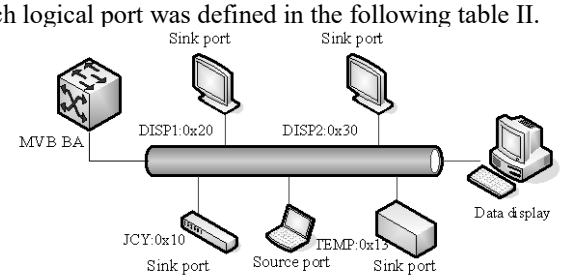

Figure 5. Network structure of experimental system

TABLE II. LOGIC PORT DEFINITION

Port NO.	Scan cycle	Data width	Device	Data
0x10	1-cycle time	16 bits	JCY	0x12,0x34
0x13	2-cycle time	16 bits	TEMP	0x56,0x78
0x20	4-cycle time	16 bits	DISP1	0x9a,0xbe
0x30	8-cycle time	16 bits	DISP2	0x26,0x27

By polling these modules MVB bus administrator realizes the exchange of process data. Macro period of polling includes nine basic periods, each of the basic period polls different logical ports respectively, in the first period would also like to poll the supervisory data for seven devices. The number of process data ports are 5,3,2,4,3,4,4,2,3, respectively in each basic period. The waveform of polling is shown in figure 6.

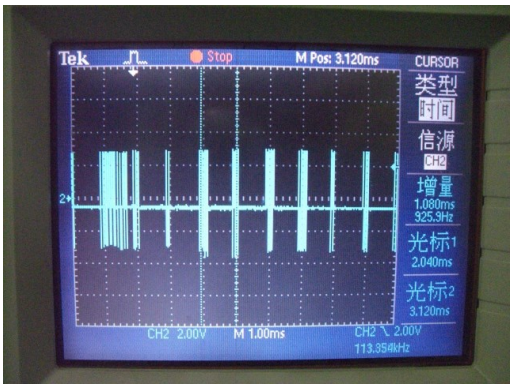

Figure 6. Measured waveform of polling

The polling data and polling time can be seen through the terminal display also. The figure 7 shows the name of each module of the detection system, the relevant logical port addresses, refresh time and the exchange of data. Because their fresh time of 0x0000, we can see that the 0x10, 0x13, 0x20 and 0x30 four nodes are connected to the bus. The process data of four connected nodes can be clearly seen in the chart, they are consistent with the results read through the oscilloscope and the expectations. Since other nodes have not connected to the bus, there is no response to the master polling.

Figure 7. Picture of terminal display

VI. CONCLUSIONS

This paper designed a MVB bus administrator with SOPC technology. Currently TCN hardware-in-loop simulation system with this MVB BA as core has been built completely, and completed the conformance testing with the standard network interface card and other MVB devices. Through the test waveform and data not only confirms the correctness of the agreement understanding, but also confirms that the proposed design's accuracy and practicality. The successful development of MVB bus administrator based on SOPC technology has great practical significance of further self-development of distributed train control system.

VII. ACKNOWLEDGMENT

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