Pratik Padalia

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Education

School Of Engineering and Applied Science (SEAS), Ahmedabad University

B.Tech, Information and Communication Technology (ICT), 2015 – 2019
CGPA – 3.72/4.33 **(Rank 1)**

Atul Vidyalaya

HSC 2015 - 91.60%
SSC 2013 - 82.83%

Positions

Google Facilitator

Applied CS with Android, Google

P Club Coordinator

Programming Club, SEAS

Committee Member

Ingenium (Technical Festival), Ahmedabad University

Achievements

Conducted 2 Workshops, Applied CS (Course on Data Structures by Google)

Winner, Ingenious **Hackathon**, 2017

Winner, Warmup for **Codefi**, 2017

Runners up, **Codefi**, 2017

SnackDown 2017 elimination round.

Problem setter, Codefi 2018.

Problem setter, Codefeeder 2018.

National Level, **Rural IT Quiz** 2011.

Interests

Competitive Coding
Data Structures & Algorithms
Data Science

Skills

Languages : C, C++, Java, Python
MATLAB, Android, Verilog

Links

LinkedIn:// 15Pratik
Codeforces:// pratik15
Codechef:// pratik15

Experience

Internship at IIT Bombay

May 2017 - July 2017 (2 months)
Worked on Group Learning Environment under the guidance of **Prof D. B. Phatak**

Internship at SculptSoft

May 2016 - July 2016 (3 months)
Prepared Admin Panel for their live app (available on iOS and Android)

Projects

Online Outlier Detection on FPGA

Nov 16 - Nov 17 Team Size : 2
Detects the outliers from real time data in linear time using Cook's Distance in order to have minimal memory utilizations.

Hand Gesture Recognition

Jan 17 Team Size : 4
Python based Hand Gesture recognition using OpenCV. Configured it for utility tools like switching through windows, web browsers and play simple games.

Process Migration and Load Balancing

Dec 17 Team Size : 2
Simple implementation of load balancing for fixed two machines and live process migration using checkpointing technique.

AnGLE - Analytics for Group Learning Environment

May 17 - July 17 Team Size : 6
A learning management system with the capability to track all activities of the user and flexible group formation to be used by institutions as well as people with same interest to form study groups or for business purposes.

8 bit Pipelined Processor on FPGA

Dec 16 Team Size : 3
RISC based 5-stage pipelined architecture with 28 instructions having 3 addressing formats (R-type, I-type and J-Type).

Extracurricular Activities

National Level **TAE-KWON-DO (Karate),** 2006

State Level, **Badminton**, 2008

State Level, Semi Finalist - **Football**, 2010

Bronze Medallist, **High Jump**, Maharashtra Region, AISM 2012