NOTE: This is a "Work In Progress"; implement at your own risk.

Sheet: OSv4_logic

Logic

File: OSv4_logic.sch

Sheet: OSv4_H-bridge

H-bridge

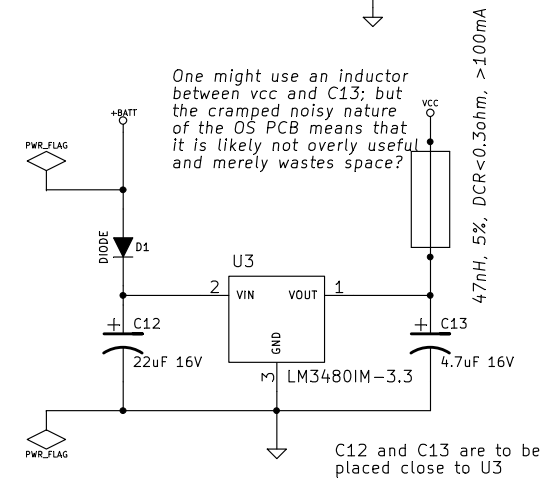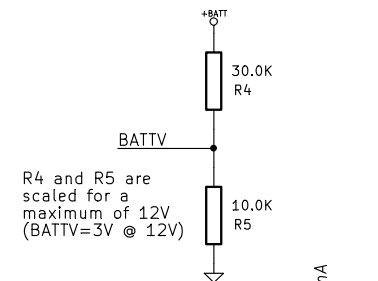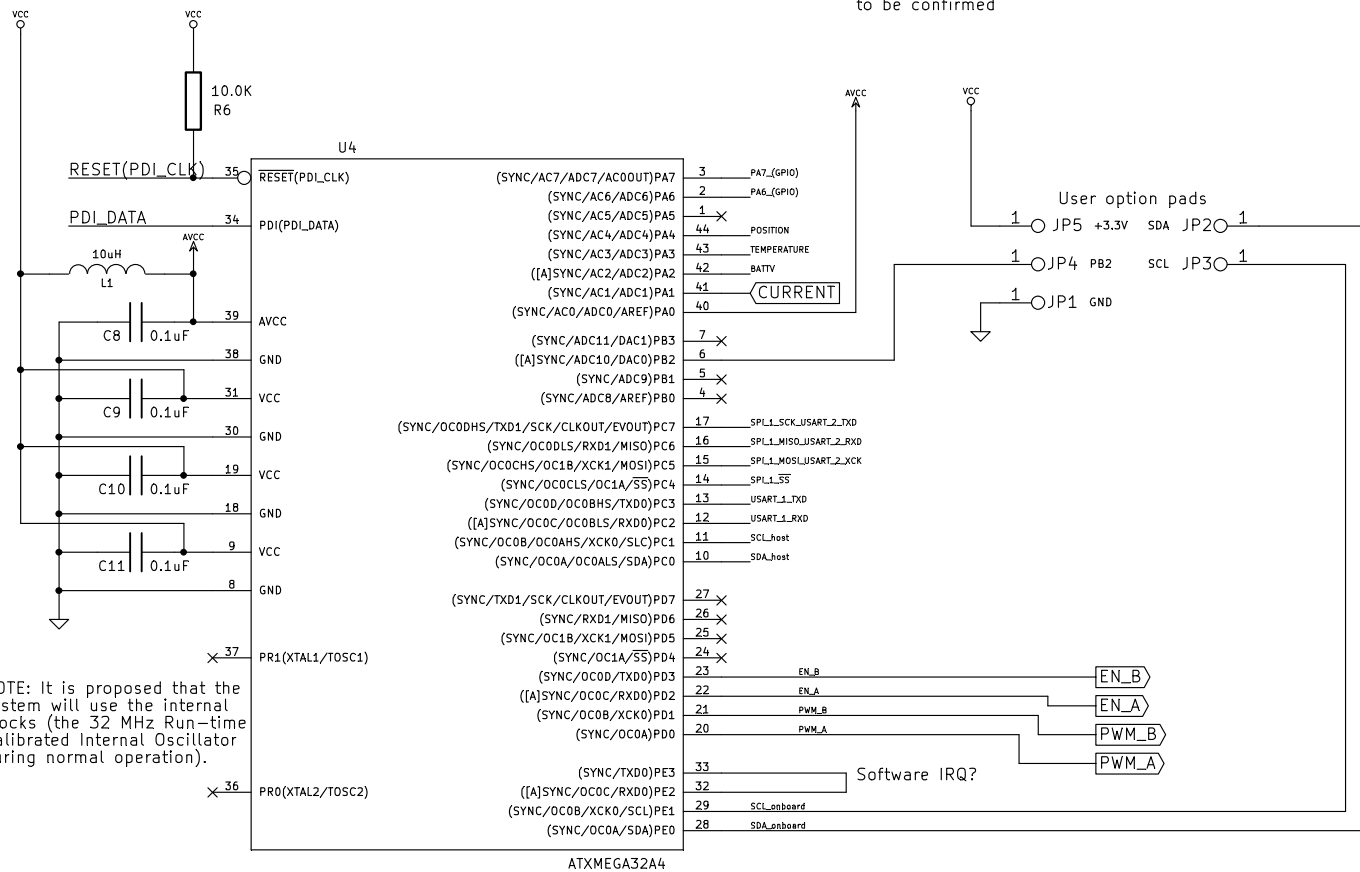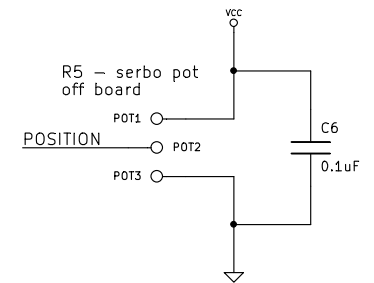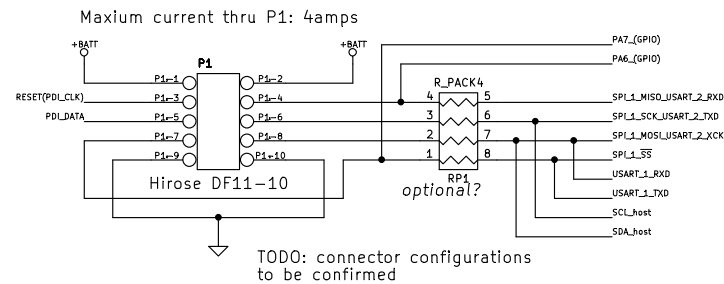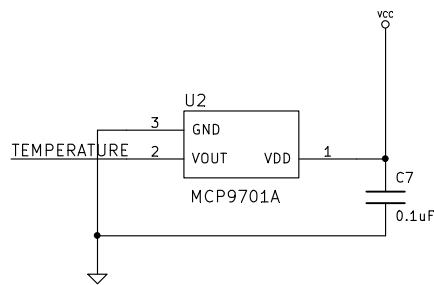File: OSv4_H-bridge.sch

NOTE: This is the latest schematic and does not match the PCB and other items which you may currently find in the same location as this document— the PCB design is being redone.

Note also that this is most definitely a "Work In Progress" that is in a state of flux... It is presented for review purposes only and does not represent an end product!

NOTE: This is a "Work In Progress"; implement at your own risk.

U2 — TEMPERATURE

MCP9701A
- 3 GND
- 2 VOUT
- VDD 1
- C7 0.1uF

Maxium current thru P1: 4amps

P1 — Hirose DF11-10
- +BATT
- RESET(PDI_CLK) P1-3
- PDI_DATA P1-5
- P1-7
- P1-9
- +BATT
- P1-1 / P1-2
- P1-4
- P1-6
- P1-8
- P1-10

R_PACK4 (RP1 optional?)
- 4 — 5 SPL_1_MISO_USART_2_RXD
- 3 — 6 SPL_1_SCK_USART_2_TXD
- 2 — 7 SPL_1_MOSI_USART_2_XCK
- 1 — 8 SPL_1_SS
- PA7_(GPIO)
- PA6_(GPIO)
- USART_1_RXD
- USART_1_TXD
- SCL_host
- SDA_host

TODO: connector configurations to be confirmed

R5 — serbo pot off board

POSITION
- POT1
- POT2
- POT3
- C6 0.1uF

U4 — ATXMEGA32A4

VCC — 10.0K R6

- RESET(PDI_CLK) 35 — RESET (PDI_CLK)
- PDI_DATA 34 — PDI(PDI_DATA)
- 10uH L1
- AVCC
- C8 0.1uF — 39 AVCC
- 38 GND
- C9 0.1uF — 31 VCC
- 30 GND
- C10 0.1uF — 19 VCC
- 18 GND
- C11 0.1uF — 9 VCC
- 8 GND
- 37 PR1(XTAL1/TOSC1)
- 36 PR0(XTAL2/TOSC2)

Right side pins:
- (SYNC/AC7/ADC7/AC0OUT)PA7 3 — PA7_(GPIO)
- (SYNC/AC6/ADC6)PA6 2 — PA6_(GPIO)
- (SYNC/AC5/ADC5)PA5 1
- (SYNC/AC4/ADC4)PA4 44 — POSITION
- (SYNC/AC3/ADC3)PA3 43 — TEMPERATURE
- ([A]SYNC/AC2/ADC2)PA2 42 — BATTV
- (SYNC/AC1/ADC1)PA1 41 — CURRENT
- (SYNC/AC0/ADC0/AREF)PA0 40
- (SYNC/ADC11/DAC1)PB3 7
- ([A]SYNC/ADC10/DAC0)PB2 6
- (SYNC/ADC9)PB1 5
- (SYNC/ADC8/AREF)PB0 4
- (SYNC/OC0DHS/TXD1/SCK/CLKOUT/EVOUT)PC7 17 — SPL_1_SCK_USART_2_TXD
- (SYNC/OC0DLS/RXD1/MISO)PC6 16 — SPL_1_MISO_USART_2_RXD
- (SYNC/OC0CHS/OC1B/XCK1/MOSI)PC5 15 — SPL_1_MOSI_USART_2_XCK
- (SYNC/OC0CLS/OC1A/SS)PC4 14 — SPL_1_SS
- (SYNC/OC0D/OC0BHS/TXD0)PC3 13 — USART_1_TXD
- ([A]SYNC/OC0C/OC0BLS/RXD0)PC2 12 — USART_1_RXD
- (SYNC/OC0B/OC0AHS/XCK0/SLC)PC1 11 — SCL_host
- (SYNC/OC0A/OC0ALS/SDA)PC0 10 — SDA_host
- (SYNC/TXD1/SCK/CLKOUT/EVOUT)PD7 27
- (SYNC/RXD1/MISO)PD6 26
- (SYNC/OC1B/XCK1/MOSI)PD5 25
- (SYNC/OC1A/SS)PD4 24
- (SYNC/OC0D/TXD0)PD3 23 — EN_B
- ([A]SYNC/OC0C/RXD0)PD2 22 — EN_A
- (SYNC/OC0B/XCK0)PD1 21 — PWM_B
- (SYNC/OC0A)PD0 20 — PWM_A
- (SYNC/TXD0)PE3 33 — Software IRQ?
- ([A]SYNC/OC0C/RXD0)PE2 32
- (SYNC/OC0B/XCK0/SCL)PE1 29 — SCL_onboard
- (SYNC/OC0A/SDA)PE0 28 — SDA_onboard

NOTE: It is proposed that the system will use the internal clocks (the 32 MHz Run-time Calibrated Internal Oscillator during normal operation).

User option pads
- 1 JP5 +3.3V — SDA JP2 1
- 1 JP4 PB2 — SCL JP3 1
- 1 JP1 GND

+BATT — 30.0K R4

BATTV

R4 and R5 are scaled for a maximum of 12V (BATTV=3V @ 12V)

10.0K R5

One might use an inductor between vcc and C13; but the cramped noisy nature of the OS PCB means that it is likely not overly useful and merely wastes space?

47nH, 5%, DCR<0.3ohm, >100mA

PWR_FLAG — +BATT

DIODE D1

U3 — LM3480IM-3.3
- 2 VIN
- VOUT 1
- 3 GND
- C12 22uF 16V
- C13 4.7uF 16V

PWR_FLAG

C12 and C13 are to be placed close to U3

NOTE: Decoupling capacitors to be placed close to the device for each supply pin pair in a signal group.

NOTE: This is a "Work In Progress"; implement at your own risk.

TODO: R1 and R3 need adjustment for V4.

U1
ZXCT1009

TODO: Change R2 for 0.5W 1% SM1206?

CURRENT

R1 R

D2 3.6V

C5 0.1uF

R3 R

Iout

Vsen− Vsen+

+BATT

R2 0.05

C1 10uF

C2 10uF

C3 1uF

C4 0.1uF

+BATT

U7B
NP_MOSFET

U8B
NP_MOSFET

M1 M2

M3

NP_MOSFET
U7A

NP_MOSFET
U8A

+BATT

U5
TC4428A

1	NC	NC	5
2	IN_A	OUT_A	6
3	GND	VDD	7
4	IN_B	OUT_B	8

U6
TC4428A

5	NC	NC	1
6	OUT_A	IN_A	2
7	VDD	GND	3
8	OUT_B	IN_B	4

PWM_A

EN_B

PWM_B

EN_A

RP2
R_PACK4

1		8
2		7
3		6
4		5

Potential MOSFETs for U7 & U8:
SP8M4
FDS8858CZ
FDS9934C??